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The Practical Limits of MASH Delta-Sigma Modulators Designed to Maintain Very Long Controllable Sequence Lengths for Structured Tone Mitigation

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Abstract

The Delta-Sigma Modulator (DSM) is an essential block for a Fractional-N (FN) frequency synthesizers and is used for generating the fractional part of the division ratio. Digital DSMs (DDSM) with rational input and rational initial conditions can be thought as Finite State Machines (FSM) and they always produce finite length sequences in accordance with the applied input. To provide smooth quantization noise power distribution (tone free) and to get rid of structured tones, the modulator should complete its cycle and return to initial starting state. This method is called maintaining controllable sequence length. In this paper, the practicality of this method will be investigated for DDSMs composed of up to 5th order MASH 1-1-1-1 structures by considering lock time requirements of the synthesizers designed for wireless transceiver applications such as GSM900, DCS-1800, UMTS(WCDMA), WLAN, ZigBee and Bluetooth .

1. Introduction

For multi-band multi-channel wireless transceiver (TRX) one of the most important blocks is the frequency synthesizer since it is used to produce the local oscillator frequency for channel selection. The phase noise performance and the spur content of the frequency synthesizer are vital since their undesirable effects fundamentally degrade the entire TRX systems [1]. In today's wireless systems, the frequency synthesizer should satisfy both conditions that are narrow channel spacing (high frequency resolution) for spectrum concerns and fast switching time between frequencies (low settling/lock time) for high speed requirements. By deploying a dual modulus FN Phase Locked Loop (PLL) as depicted in Figure 1, it is possible to solve and eliminate these two conflicting problems by providing increased reference frequency and Loop Filter (LF) bandwidth [1]-[2]. In FN-PLL synthesizer, the division ratio can be any number and is not restricted to be an integer as in the case of Integer-N PLL frequency synthesizer. This characteristic provides the ability for the frequency synthesizer to have higher frequency resolutions with a highly flexible frequency range to select from, giving the wireless system designers the freedom to painlessly define narrow channel bandwidths amongst others.

In FN-PLL synthesizers, due to the switching behaviour of the dual modulus divider between N and $N+1$, the spurs appear at Phase Frequency Detector (PFD) frequency offsets from the carrier and at their harmonics [1]. By randomizing the frequency division ratio in the loop to get rid of reference frequency spurs, the quantization noise of the fractional-divider can be pushed away to the higher frequencies by the aid of using DSMs [1]-[2]. This type of FN-PLL frequency synthesizer is called as a Delta-Sigma FN-PLL (DS-FN-PLL) frequency synthesizer and its general block diagram is given in Figure 2.

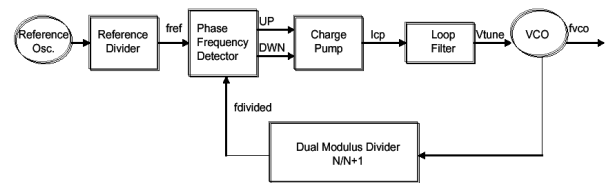


Figure 1. Dual Modulus FN-PLL Frequency Synthesizer

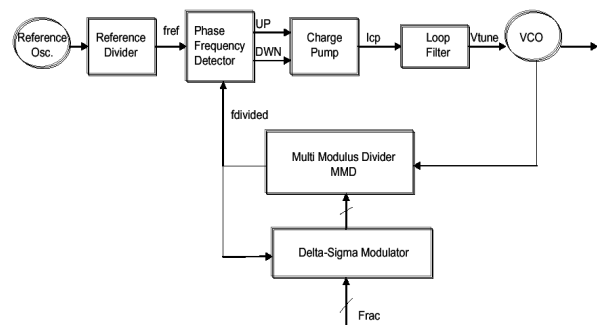


Figure 2. Delta-Sigma FN-PLL Frequency Synthesizer

In DS-FN-PLL synthesizer applications, the input of the DSM (fractional part of the division ratio) is always constant, DC. A DSM is a nonlinear system and it is well known that it produces spurs for DC inputs [2] - [3]. By increasing the order of the MASH modulator, the in-band tones can be effectively suppressed. It has been shown by the authors of [3] that, if the modulator order is 3 or above, this is guaranteed. In the literature, some methods have been

developed to minimize/eliminate DSM tonal behaviour. One of the common methods deployed is maintenance of very long controllable sequence [4-6].

2. Maintaining very long controllable sequence length for structured tone mitigation

DDSMs with rational input and rational initial conditions can be thought as FSMs and they always produce finite length sequences in accordance with the applied input [4-6]. To provide smooth quantization noise power distribution and to get rid of structured tones, the modulator should traverse through all its states returning to its initial starting state. The sequence length of the modulator can be controlled by setting odd initial conditions and applying modulator scaling [4]. However, for a dynamically changing input, the set of initial conditions should be changed at power up and the modulator should be operating for at least the required period defined by the input and the initial conditions for tone free operation. It has been proven by the authors of [4] that if the modulator is loaded with the preferred odd initial conditions and the input signal is even (extending the input by one LSB bit that is set to 0), the state stores (registers) remain at all time within the preferred initial conditions providing long enough sequence lengths for tone free operation and eliminating the problem of loading initial conditions when the input is changed. For example, for a 3rd order MASH 1-1-1, the guaranteed sequence length is given by 2^{k+1} , where k is the number of bits at input [4]. The authors of [5] presented a modified MASH structure called the HK-MASH. In this work, the authors declare that by dramatically increasing the sequence length $\approx 2^{kl}$ where k is the number of bits used to represent input and l is the order of the modulator, the tone free operation can be guaranteed for all DC inputs and for all initial conditions. For maximizing the sequence length, another way is to use prime number for the modulus of the quantizer [6-9]. It has been shown by the authors of [6] that if the quantizer modulus is prime and if it is greater than the number of stages in the MASH, the sequence length of any order MASH is equal to the sequence length of the first stage, N that is also equal to the quantizer modulus, M . However, it has the advantage that it has the guaranteed minimum sequence length for all DC inputs and for all initial conditions. In [5], by adding simple feedback to the first order Error Feedback Modulator (EFM) the sequence length is maximized and first order EFM effectively gives a prime modulus while the modulus of the quantizer itself is a power of 2.

3. Lock time for DS-FN-PLL frequency synthesizer

The lock time (or settling time) is the time for the DS-FN-PLL frequency synthesizer to be locked from

one frequency to the other in its operation band and it is largely determined by the loop filter bandwidth in the PLL loop. Since it also determines the chip area of the synthesizer due to its relatively large capacitors and also contributes to the output phase noise characteristics, the loop-filter design is a challenge. As mentioned before, frequency synthesizers are used to produce a stable and precise local oscillator frequency for channel switching and are one of the most important blocks for wireless transceiver. In the wireless transceiver system, the frequency synthesizer lock time should be less than the required time for channel switching according to the wireless standards [11-25]. For voice and data communication, there are many standards which define how devices communicate with each other. Some examples are AMPS, DECT, GSM, DCS, GPRS, EDGE, UMTS (WCDMA), CDMA2000, 802.11a/b/g/n WLAN, Bluetooth, ZigBee, and HomeRF. The lock time requirements of standards differ from each other. For GSM and DCS-1800 systems, this time is set to be around 1ms [10] (available time slot is 577 μ s for DCS-1800 [12]), for the ZigBee system, it is less than 192 μ s [25], and for the Bluetooth system, it is less than 254 μ s [27]. By the way, since GPS is a single frequency system, a start-up time of less than 5ms is acceptable for GPS. Therefore, for a stand alone GPS system, the synthesizer settling time is not a critical design factor [26]. Today's wireless communication market drives engineers to design devices that are usable for many applications allowing both data and voice transfer and supporting more than one standards. It is also desirable to have frequency synthesizers with low lock times in order to increase the capacity and the quality of the communication link. By these drives and also with the aid of developing technology and scaling, the frequency synthesizers with lower lock times are sited in the open literature as given in Table 1.

Table 1. The literature survey of frequency synthesizers and associated lock times

Lock Time (μ s)	Standard
<300	DCS-1800 (For 100MHz Freq Step) [11]
150	DCS-1800 [12]
<220	Tri-Band GSM/GPRS [13]
150	GSM900 [14]
95	GSM900/DCS-1800 [15]
<100	GSM900 [16]
<15	GSM900 [17]
<30	2.5GHz Band [18]
7	WCDMA [19]
10	GSM/EDGE (For Base Stations) [20]
43	Quad Band GSM/GPRS [21]
40	5GHz WLAN (For 300MHz Freq Step) [22]
<10	WLAN 802.11a/WiMAX802.16e [23]
<3.3	915 ISM Band [24]
25	2.4GHz ZigBee (For 75MHz Freq Step) [25]

4. Maintaining a very long controllable sequence length for DS-FN-PLL frequency synthesizers

To investigate how practical the use of the controllable sequence length technique for DS-FN-PLL frequency synthesizers, the question of ‘How long can the sequence length for the modulator be?’ should be answered. The operation time of the modulator used in DS-FN-PLL frequency synthesizer is limited by the synthesizer lock time that is defined by the standards. It is clear that the operating time of the modulator should be less than the lock time of the synthesizer. We define the operation time required for the modulator to guarantee a tone free spectrum as a Modulator Tone Free Period (MTFP) and is given by the equation (1) below:

$$\text{MTFP} = \text{Sequence Length} * (1/f_m) \quad (1)$$

where, f_m is the modulator clock frequency. Please note that for a DS-FN-PLL frequency synthesizer, f_m is equal to the reference frequency, f_{ref} . So, for DS-FN-PLL frequency synthesizers, the condition “MTFP \leq Lock Time” should be satisfied, otherwise the spectrum of the modulator will have a high number of tones due to insufficient randomization of the quantization noise. If the reference frequency of the DS-FN-PLL synthesizer is increased, its MTFP will be decreased. In addition, since the power of the quantization noise is concentrated around $f_m/2$, the noise power around DC will also be decreased [5].

In Figure 3, first order EFM structures for both MASH and HK-MASH are given.

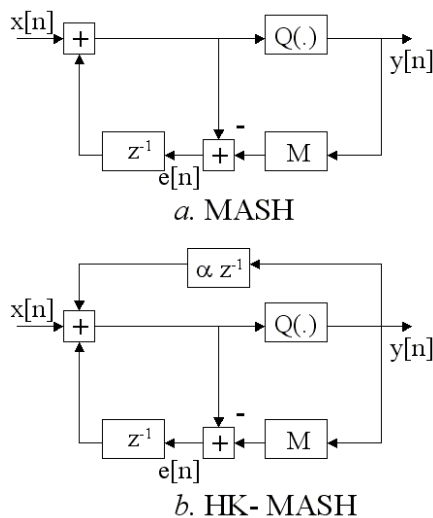


Figure 3. 1st Order EFM Structures for MASH and HK-MASH

According to [4]-[5], the guaranteed sequence lengths for MASH and HK-MASH structures are given

in Table 2, where k is the number of bits at the input of the modulator. Please note that for the MASH structure, these values are valid for odd initial condition on the first stage, and for the HK-MASH, for all inputs and initial conditions.

Table 2. Guaranteed Sequence Lengths

Modulator Order	MASH	HK-MASH
2	$2^{(k-1)}$	$2^{(2*k)}$
3	$2^{(k+1)}$	$2^{(3*k)}$
4	$2^{(k+1)}$	$2^{(4*k)}$
5	$2^{(k+2)}$	$2^{(5*k)}$

A graph of MTFP values for standard MASH and HK-MASH structures are given in Figure 4. In this figure, $k=8$ and $f_{ref}=30\text{MHz}$ were assumed in our calculations. As it is clear from the Figure 4, the values for HK-MASH are quite high. Please note that for a 2nd order HK-MASH, the MTFP value is found as 21.845ms. For any order MASH (1-1 to 1-1-1-1-1), the values are less than 35 μs that is fast enough for most of the wireless standards and satisfy settling time requirements. By increasing the reference frequency, it is also possible to decrease this value. In Figure 5, for a MASH structure (1-1 to 1-1-1-1-1), the change of MTFP with respect to the reference oscillator frequency is given. The lock time requirements of GSM, DCS-1800, Bluetooth and ZigBee standards are also put into the figure to realize the practical window for MTFP values. Please note that, in this figure, $k=9$ was taken as the number of input bits.

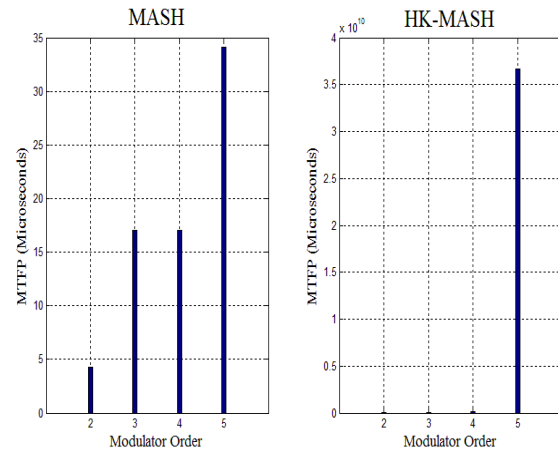


Figure 4. MASH and HK-MASH MTFP Values

For a 3rd and 4th order standard 1-1-1 and 1-1-1-1 MASH structure, the effect of number of input bits on MTFP is shown in Figure 6. It is clear from the figure that for reference frequencies higher than 10 MHz, for all k values from 5 to 8 bits, the MTFP is under 50 μs . It is also clear that for $k=8$ bits for a 1 MHz reference

frequency, MTFP is around 500 μ s that is still sufficient for GSM and DCS-1800 lock time requirements.

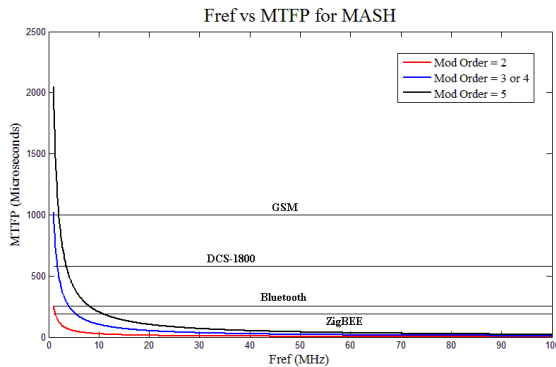


Figure 5. MTFP vs. Reference Frequency for MASH

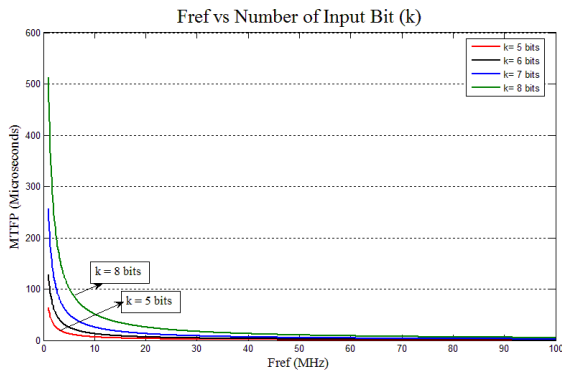


Figure 6. MTFP vs. Number of Input Bits for MASH

5. Conclusion

For a DS-FN-PLL frequency synthesizer, the DSM is an essential block that is used for generating the fractional part of the division ratio. DDSM with rational inputs and rational initial conditions are FSMs and they always produce finite length sequences according to the applied input. To provide smooth quantization noise power distribution, the modulator should complete its cycle and return to a starting initial state. This method is called maintaining controllable sequence length. In this paper, the practicality of this method has been investigated for DDSMs composed of up to 5th order standard MASH (1-1 to 1-1-1-1-1) and HK-MASH structures. A measure called MTFP has been defined and it has been shown that for proper operation, the condition $MTFP \leq \text{Lock Time}$ should be satisfied. In this paper, MTFP values have been calculated and compared with the lock time requirements for the various wireless standards. It has been further shown that f_{ref} should be kept high for both noise and MTFP concerns, but there is a trade off

for k since it is known that if k is kept high the noise performance is improved, but as shown if it is increased the MTFP also increases.

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