A new bulk-driven input stage design for sub 1-volt CMOS op-amps.

Yasutaka Haga[1]
Richard C.S. Morling[1]
Izzet Kale[1,2]

[1] School of Informatics
[2] Applied DSP and VLSI Research Centre, Eastern Mediterranean University

A New Bulk-Driven Input Stage Design for Sub 1-Volt CMOS Op-Amps

Yasutaka Haga*, Richard C. S. Morling*, and Izzet Kale*+
*Applied DSP & VLSI Research Group, Department of Electronic Systems, University of Westminster, London, United Kingdom
+Applied DSP and VLSI Research Centre, Eastern Mediterranean University, Gazimagusa, Mersin 10, Turkey
y.haga@student.westminster.ac.uk, {morling, kalei}@westminster.ac.uk

***Abstract*— This paper presents a new design approach for a rail-to-rail bulk-driven input stage using a standard single-well (n-well in this paper) CMOS technology. This input stage can provide nearly constant transconductance and constant slew rate over the entire input common-mode voltage, operating with a wide supply voltage ranging from sub 1-volt (V_{T0}+3V_{DSsat}) to the maximum allowed for the CMOS process, as well as preventing latch-up.**

I. INTRODUCTION

Lowering of the supply voltage in portable electronics has always been a priority for many years, as it allows reduction in the number of battery cells rendering the products more compact and light, and leading to decreased power consumption of the digital circuits. However, in analog circuits, particularly op-amps in unity-gain configuration, lowering the supply voltage degrades the signal-to-noise ratio. As a consequence, those op-amps require rail-to-rail input and output stages.

For the input stage, it is essential that its effective transconductance (g_m) is nearly constant over the rail-to-rail Input Common-Mode Range (ICMR), as the large variation introduces signal distortion and creates difficulty in the frequency compensation of the multi-stage op-amps [1], [7]. Traditionally, complementary differential pairs are used to achieve the rail-to-rail operation, and the tail current is controlled with current switches to keep the g_m constant [1]. However, the mobility ratio of the complementary pairs (μ_n/μ_p) is process- and temperature-dependent, causing the g_m variation to deviate by approximately 12% [2]. This motivates designers to come up with new circuit topologies using only a single type of the differential pair. Currently three candidates have been proposed – level-shifting [2], floating-gate [3], and the bulk-driven [4] techniques.

At the present time, the bulk-driven technique is probably the least popular, since the transconductance of a bulk-driven MOSFET (g_{mbs}) is dependent on the bulk-to-source voltage (V_{BS}). The level-1 model of the g_{mbs} is given by:

$$g_{mbs} = \gamma \, (2\beta I_{DS})^{0.5} / 2 \, (2|\Phi_F| - V_{BS})^{0.5} \qquad (1)$$

where γ is the bulk-threshold parameter, β is the small-signal transconductance parameter, I_{DS} is the drain current, and $2|\Phi_F|$ is the surface potential. The g_{mbs} is typically only 20-40% of the gate-driven transconductance [4]. However, the beauty of a bulk-driven MOSFET is that it removes the threshold voltage constraint. This property makes the bulk-driven approach worthy of development to improve its performance.

So far three proposals are available for improving the g_m variation of the Bulk-Driven Differential Pair (BDDP) – the complementary BDDP [5], the Replica-Biased Scheme (RBS) [5], and the feedback techniques [6]. The complementary BDDP technique utilizes the complementary behavior of the pairs to reduce the g_m variation. However, a special CMOS technology (e.g. a twin-well process) is required for the implementation. The RBS, as illustrated in Fig. 1, biases the gates of the pair to keep $V_{BS} = 0$ so that the g_{mbs} becomes constant. The problem is, however, $V_{BS} = 0$ means $V_B = V_S$, and it is impossible for the source-coupled voltage to swing rail-to-rail. Thus the g_m is constant over only a portion of the rail-to-rail ICMR. The feedback technique senses the input common-mode voltage (V_{ICM}) and adjusts the tail current to reduce the g_m variation; however, this causes the Slew Rate (SR) to become V_{ICM} dependent.

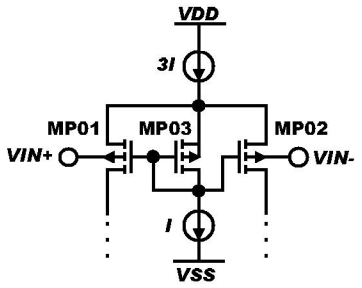

Figure 1. The bulk-driven RBS proposed in [5]

This paper presents a new bulk-driven rail-to-rail input stage using a standard single-well (n-well in this paper) CMOS process. This input stage achieves almost constant-g_m and constant-SR, working with a wide supply voltage

ranging from sub 1-volt (V_{T0}+3V_{DSsat}) to the maximum allowed by the CMOS process, and also diminishes the latch-up likelihood.

II. The New Bulk-Driven Input Stage

A. Topology

The idea of our bulk-driven input stage comes from utilizing two pairs of the RBS to cover all portions of the rail-to-rail ICMR. Fig. 2 illustrates the topology of our approach, which we call the Bulk-Driven Double Replica-Biased (BDDRB) input stage.

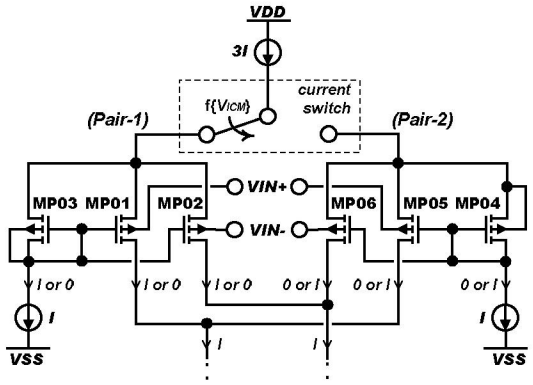

Figure 2. Topology of the BDDRB input stage

The BDDRB input stage consists of pair-1 (MP01~MP03) and pair-2 (MP04~MP06), which are assigned for the low and high portions of the ICMR, respectively, and a current switch.

The device sizes of pair-1 are all the same, and the same dc current runs through each device when the pair is selected. This leads MP03 to be the replica of the input pair, and $V_{BS1,2}$ to be equal to V_{GS3} (= constant). The same argument goes to pair-2 except that $V_{BS5,6}$ would be zero instead. The pair-1 would be operational for the ICMR between VDD-V_{SDsat}-V_{SG3} and VSS+V_{DSsat}, and for pair-2 the operational range would be between VDD-V_{SDsat} and VSS+V_{DSsat}+V_{SG4}. To maximize the ICMR a current switch is implemented so that the effective ICMR would be between VDD-V_{SDsat} and VSS+V_{DSsat}.

B. Principle of Operation

Fig. 4(a) illustrates how the BDDRB input stage can be realized as a transistor circuit. Again, MP01~MP03 (pair-1) and MP04~MP06 (pair-2) are the replica-biased input pairs for the low and high portions of the ICMR, respectively. MP09~MN12 form a current switch and work as a function of V_{ICM}. This input stage is configured such that it normally operates with pair-1. When V_{ICM} becomes high and causes V_{SG9} to be greater than the threshold voltage ($|V_{T0}|$), the switch deactivates pair-1 and activates pair-2 instead. Conversely, when V_{ICM} becomes low and causes $V_{SG9} < |V_{T0}|$, pair-1 turn on and pair-2 turns off. The bias-voltage, V_{SWITCH}, controls the crossover voltage between the two points.

To verify the operation of the BDDRB input stage, it was necessary to implement it in an op-amp. For this we chose a folded-cascode two-stage op-amp, as illustrated in Fig. 4(b), to present as an application example.

III. Simulation Results

Using the BSIM3 MOSFET models of a 0.18μm CMOS process, we simulated the op-amp of Fig. 4 with a supply voltage of 0.8-volt and a load resistance and capacitance of 1MΩ and 5pF, respectively. Table I shows the summary of the simulation results.

TABLE I. Simulation Results of the Overall Performance of the Op-amps in Figure. 4

Characteristics	Simulated Results
Open-loop DC gain	60dB
Unity-gain frequency	0.6MHz
Phase margin	58°
ICMR	0.6V
Total current consumption	61~74μA (V_{ICM} dependent)
SR	SR+ = 1.0V/μs, SR- = -0.5V/μs
Output voltage swing	0.6V
Common-mode rejection ratio	63dB (when V_{ICM} = 0.5(VDD+VSS))
Power Supply Rejection Ratio (PSRR)	PSRR+ = 58dB, PSRR- = 79dB
Input referred noise voltage	146~169nV/√Hz (white noise only, V_{ICM} dependent)
Total harmonic distortion, A_{VCL}=+1V/V	0.014% (-77.1dB) for 0.6Vp-p, 1kHz sine wave 0.093% (-60.6dB) for 0.6Vp-p, 10kHz sine wave
Measurement condition: VDD = 0.8V, VSS = 0V, C_L = 5pF, R_L=1MΩ	

The simulation confirmed the rail-to-rail ICMR operation (VDD-$V_{SDsat14}$ to VSS+$V_{Dssat07}$ precisely). Fig.3 and Fig. 5 show the simulation results of the open-loop gain frequency response and the effective tail current of the op-amp in Fig. 4, which indicate that both characteristics are nearly V_{ICM} independent. Fig. 6 gives the simulation results of the effective transconductance [g_m(eff)] of the op-amp versus V_{ICM}.

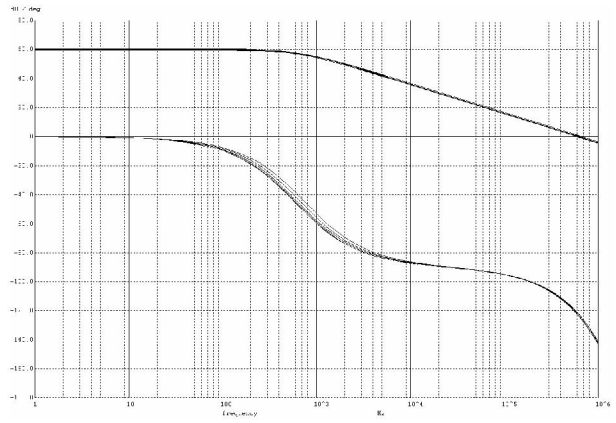

Figure 3. Simulated frequency response of the op-amps for V_{ICM} varying from 0.1 to 0.7V with a 0.1V step

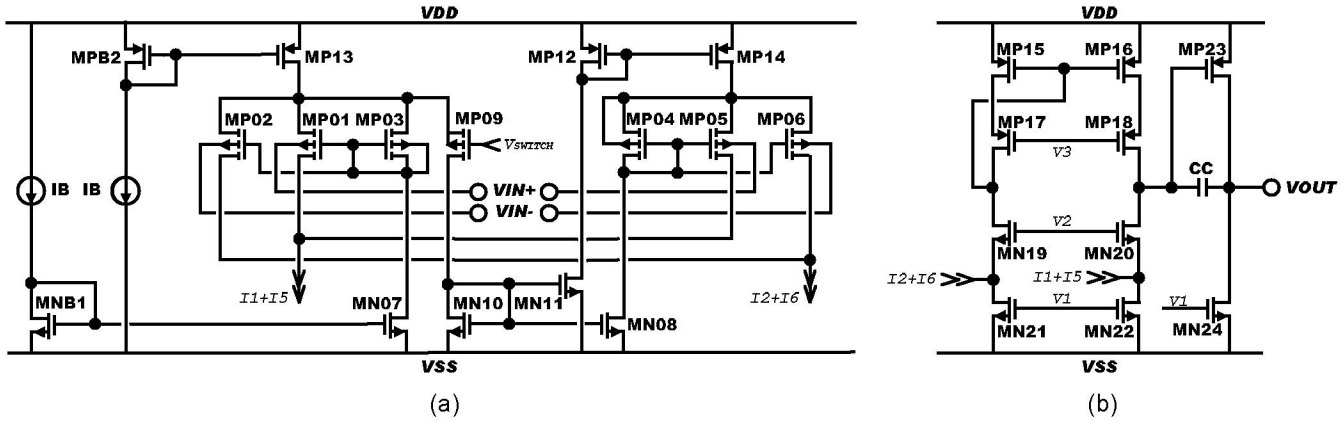

Figure 4. An application example of the BDDRB input stage in a folded-cascode two-stage op-amps (a) the BDDRB input stage, and (b) a folded-cascode two-stage op-amps

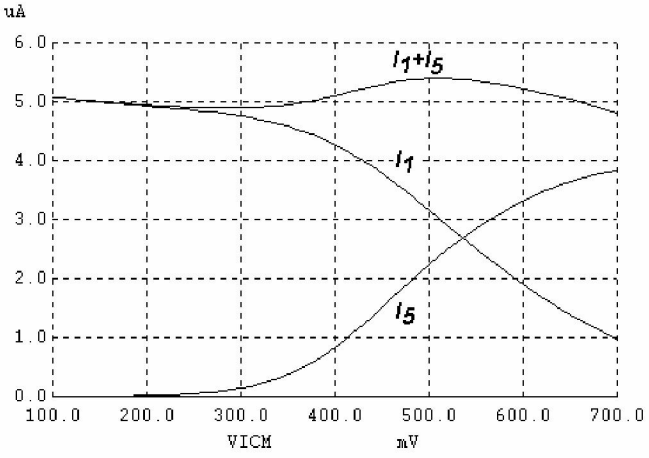

Figure 5. Simulated tail current vs V_{ICM}

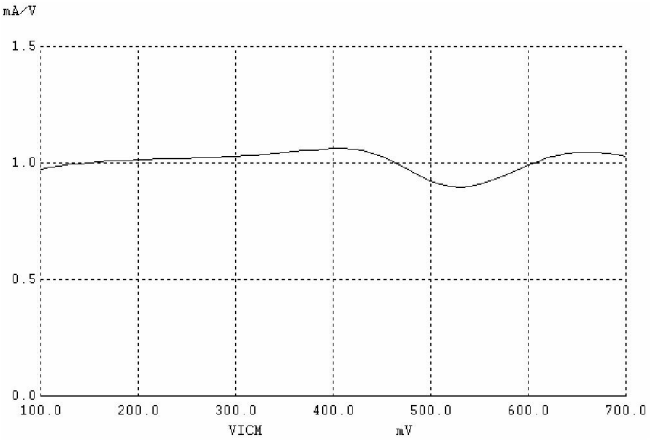

Figure 6. Simulated g_m(eff) vs V_{ICM}

Fig. 6 indicates that the g_m variation is approximately 10% over the rail-to-rail ICMR operation. This variation peaks at the transition point between the two pairs, i.e. when the pairs are partially on and off. It is worth noting that the source-to-bulk voltage of the input pairs (V_{SB1} and V_{SB5}) change at the transition stage, which should also have created a major impact in the g_m variation according to (1). Fig. 7 shows the simulation results of V_{SB1} and V_{SB5} versus V_{ICM}.

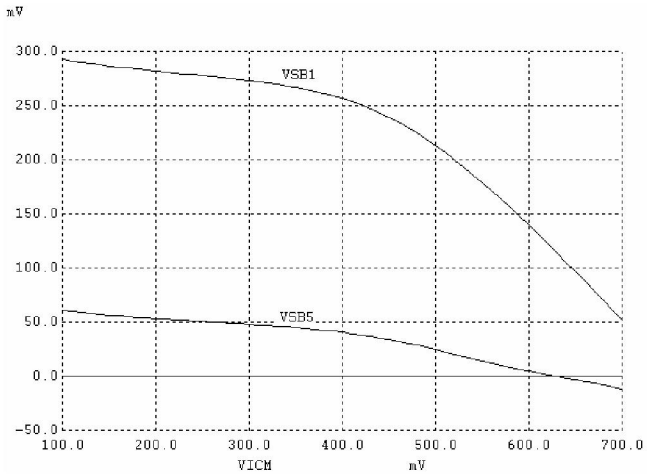

Figure 7. Simulated V_{SB1} and V_{SB5} vs V_{ICM}

IV. Advantages and Disadvantages

An important practical advantage of the BDDRP input stage is that it requires no special CMOS process. Other advantages are g_m(eff) and SR of the op-amp remain relatively constant with respect to V_{ICM}, and the circuit prevent latch-up. Conventional BDDP techniques require very low supply voltages, otherwise the rail-to-rail ICMR operation would cause the bulk terminals to be strongly forward-biased. With the BDDRB input stage, the bulk-to-source voltages remain as the same condition as the replica device regardless of the supply voltage condition. For confirmation, we simulated the circuit of Fig. 4 with a 3-volt power supply and observed that the rail-to-rail ICMR operations did not result in any significant input current or substantial forward-biased pn junctions.

However, in comparison to previously mentioned bulk-driven techniques, our proposal increases input referred

noise. Previously mentioned bulk-driven techniques utilize the depletion-mode characteristics of a MOSFET so that the input pair can be always on for rail-to-rail. In contrast, our input stage has two pairs connected in parallel, and except in the transition stage one of the pair is off. The off-pair contributes additional thermal noise, as it is inversely proportional to g_{mbs} [11].

Another drawback to previously mentioned bulk-driven techniques is the increase in input capacitance, since two input pairs are utilized in our proposal. The input capacitance of a bulk-driven MOSFET consists of C_{bsub} and C_{bs}, where C_{bsub} is the well-to-substrate capacitance and C_{bs} is the bulk-to-source capacitance. C_{bsub} depends on layout design, and a detail description is given in [4]. C_{bs}, on the other hand, can be controlled by circuit designers to some extent as it is directly related to its source-to-bulk voltage. Reducing the forward-bias of the bulk-terminal results in decreased C_{bs} as well as increased input resistance. With the BDDRB input stage, this can be easily achieved by decreasing the source-to-bulk voltage of the replica device (V_{SB3} of Fig 4(a), which is equivalent to V_{SG3}). Fig. 8 illustrates the simulation results of the input impedance measurements for the op-amp shown in Fig. 4.

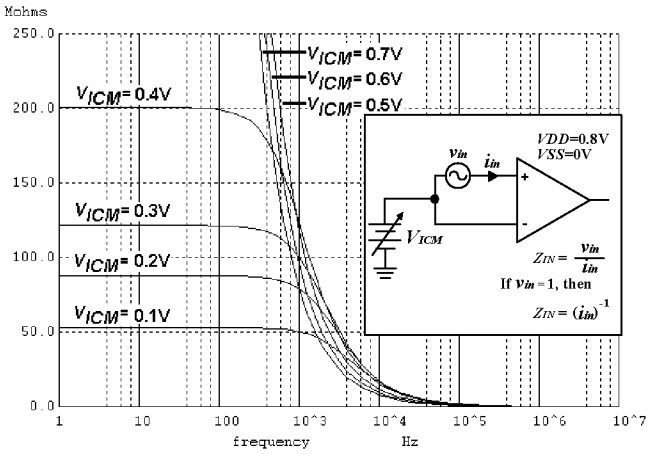

Figure 8. Simulation results of the circuit-level input impedance characteristic

V. CONCLUSION

A new approach for the bulk-driven input stage called BDDRP to achieve rail-to-rail ICMR operation has been presented. This approach leads the operational supply voltage to be from under 1-volt to the maximum allowed by the CMOS process used, as well as diminishing the latch-up problem. SPICE simulations indicate that the g_m is nearly constant (within 10%) over the entire ICMR whilst the effective tail current remains almost unchanged. The additional hardware implemented to achieve this performance is only a replica circuit for each pairs and a current switch.

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