A high-speed, low-power interleaved trace-back memory for Viterbi decoder.

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Abstract— **This paper presents a high-speed, low-power trace-back memory structure for a Viterbi Decoder. The new memory is based on an array of registers connected with trace-back signals that decode the output bits on the fly. The trace-back memory is internally interleaved such that high-speed characteristic is achieved while low-power consumption is maintained. The structure is used together with appropriate clock and power-aware control signals. The design is 100% portable and is suitable for a SoftIP approach. Based on the AMS 0.35 µm CMOS implementation the trace-back memory is estimated to consume energy of 232 pJ, which is 53.6% less than a conventional RAM based design, with a maximum throughput of 1.1 Gbps.**

I. INTRODUCTION

Convolution coding is widely used in modern digital communication systems such as mobile or satellite communications to achieve low-error rate data transmission. The Viterbi algorithm [1], in particular, is known to be an efficient method for the realisation of maximum- likelihood (ML) decoding of the convolutional codes. Today the Viterbi Decoder is widely used in established systems such as GSM mobile or the IEEE 802.11a wireless LANs standard. With emerging applications such as the DAB, DVB or wearable personal entertainment devices, wireless communication is also increasingly becoming more pervasive. These applications require devices with ultra low-power consumption. Already it has been shown that the Viterbi decoder can account for more than one third of the power consumption during baseband processing in second-generation cellular telephones [2]. Power consumption is therefore the critical design criterion to be tackled.

A conventional Viterbi decoder consists of 3 major parts that are:

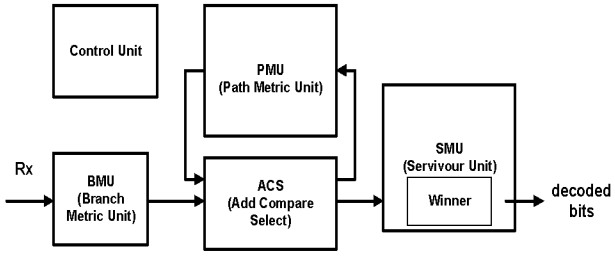


Figure 1. Viterbi Decoder

- Branch metric computation unit (BMCU)
- Add-compare-select unit (ACSU) containing ACS cells(s) and PMU
- Survivor memory unit (SMU)

For an encoder with constraint length L =K, the BMCU works to find the likelihood of each of the $2^{(K-1)}$ states of the decoder transferring to a next state under particular set of input symbols. The ACSU compares the results to find maximum likelihood for each state, updates its path metrics, and generates a decision bit that uniquely identifies the previous or surviving states. These decision bits are stored in the SMU and used to reconstruct the most likely state sequence. The transitions of the states at different points in times can be visualized using a Trellis diagram [1].

Viterbi decoders have been subjects of ongoing research, the most recent ones being [3-5], dealing with high-speed implementations. Approaches for power reduction have also been proposed [6-11]. In this paper we introduce high-speed, low-power design techniques targeting specifically the key power hungry block within the Viterbi decoder, which is the SMU. An SMU usually employs either register exchange or trace back techniques. In the register exchange designs [12]

the decoded bits for each state given maximum likelihood path are stored directly onto the state registers. The approach consumes significant power and is suitable only for designs with short decoder length, as the decoded data stored, which needs constant read/write updates, increases with the length of the decoding process. For systems that require longer decoding length for better bit error rate, such as those in GSM or CDMA, the trace-back technique [13] is usually employed. Using trace-back algorithm, only information that identifies previous unique states is kept in the memory, meaning only one bit/state/stage is required. After a certain decoder length the information is read out and decoded to find the most likely incoming bit sequences received during that period. The trace-back SMU is conventionally realized using RAM, and has been shown to contribute to more than half of the power consumption in a conventional Viterbi decoder due to the expensive memory accesses [8].

In our recently reported design [11], a new memory structure where decoded bits are presented without having to be read out was proposed. The structure was based on an array of registers connected with trace-back signals that decode the output bits on the fly. Two structures that are parallel and systolic based are employed, together with appropriate clock and power-aware control signals to achieve the low-power goal. The results showed that power reduction of as much as 60% was possible in the parallel structure. One problem with the design, however, was that the speed was relatively slow due to long critical paths. This paper proposes an improved architecture based on a memory interleaving technique. In the next section the review of the low-power design in [11] is provided. The proposed high-speed improvement is then discussed in Sec. III, followed by results and discussion in Sec. IV. Sec. V is the conclusions.

II. LOW POWER TRACE-BACK MEMORY ARCHITECTURE

The low-power memory structure in [11] was based on connections of new cell elements; each has a structure as shown in the Figure 2. The cell consists of a register with additional logics to allow the stored trace-back information to be read. The logic is also connected to other cells such that, based on the bit information stored, it can uniquely identify the previous or surviving state so that the decoded bit can be found. An example of the memory structure for a 64-state Viterbi decoder with a decoding length of 35 is shown in Figure 3. Power consumption is minimized as, once stored in the register bits, the result is already presented without having to be read out again as is the case of using RAM. The memory structure is also designed such that only once the winner is decided upon that the signals are to be propagated through the array to decode the output bits. Apart from that period, no switching of decoding logic occurs. In terms of writing the data onto the registers, two approaches were considered. The first approach, termed systolic was when the data propagates through the stage (or column) resisters under the same clock rate (Fig 4). For the second approach, termed parallel (Fig 5), data is connected to all the column registers in parallel; each clocked at clk/35 rate and appropriately skewed. The results showed that the parallel structure gives a better result with the power reduction of as much as 60% compared to conventional RAM based design.

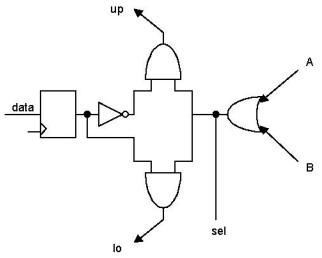


Figure 2. Cell structure

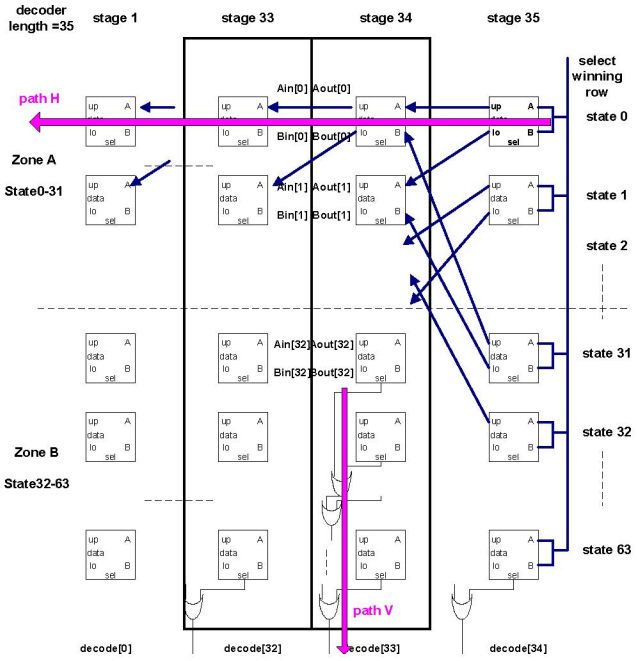


Figure 3. New trace-back memory connection

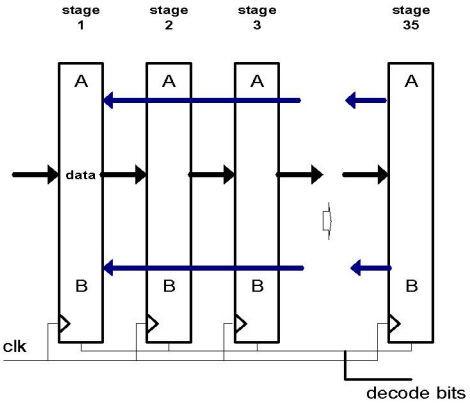


Figure 4. Systolic architecture

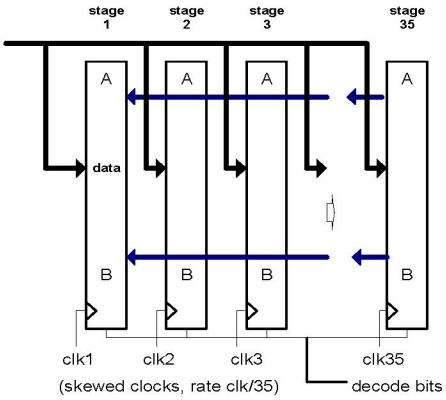
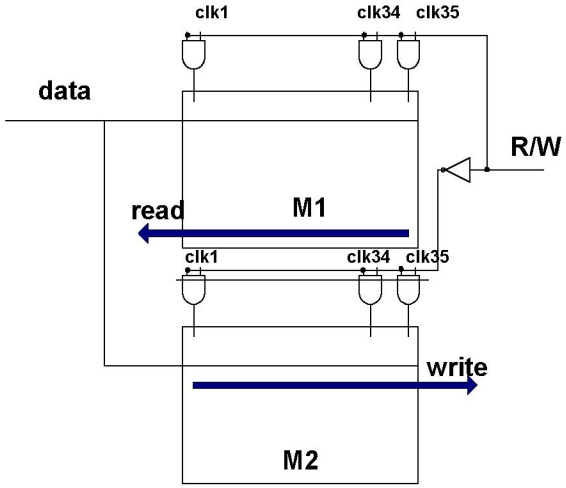


Figure 5. Parallel architecture

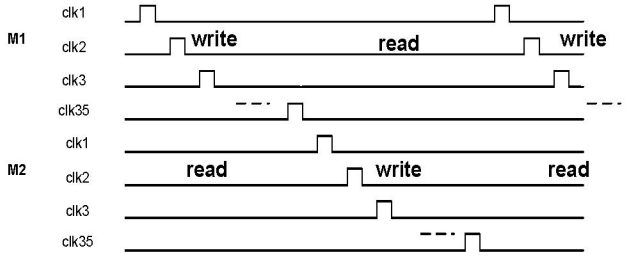
III. HIGH-SPEED, LOW POWER SMU

It can be seen from Figure 3 that major critical paths that dictate the maximum clock speed are the paths H and V, which run horizontally and vertically respectively. After the memory registeres all the information to decode a 35-bit data, the signals need to completely propagate through the paths H and V before the first bit of a new set of data can be registered. This bottleneck severely limits the clock speed of the memory. The delay of path H depends on the number of stages (memory depth), where as the path V depends on the number of states. Although the design was shown to have adequate speed for a number of applications, its maximum speed is still quite limited by these critical paths. In this paper we propose an improvement for a high-speed low-power solution based on simple interleaved trace-back architecture. The structure we propose is as in Figure 6. To overcome the problem of propagation in horizontal direction, we use two memories (Fig 6a) that are complementarily alternating between read (track-back read out) and write states, each with the duration of decoding length (35 bits in this case) (Fig 6b). The operation is controlled by R/W signal that appropriately gates the clocking signals used when writing data to the memories. In doing so, the traced-back result of the previous 35 bits can be read out while the new data is updated to the other memory. Even though the critical path H remains the same, it no longer affects the clocking speed of the stages in writing. As the critical path H is the time taken to decode all 35 bits, so effectively the critical delay of the memory in reading state is only (T_{AND} + T_{OR}) per stage, where T_{AND} and T_{OR} are respectively the delays of AND and OR gates within the cell structure. It is clear that the memory can now operate at a much higher speed, effectively D times faster, where D is the decoder length.

The same argument goes for the vertical path V, where the *sel* signal from each state in the column needs to be logical ORed together to produce the decoded bit for that column (Fig 3). Under the same scenario as with the horizontal case, effectively the critical delay of the memory in reading the state in the V direction is only (T_{OR1} + T_{OR2}) per stage, where T_{OR1} is the delay of the OR gate within the cell structure, and T_{OR2} the delay of OR gate used in each pair of *sel* states.



a) High-speed, low-power memory structure



b) Write sequences for memory M1 and M2

Figure 6. New trace-back memory connection

IV. RESULTS AND DISCUSSIONS

To test the effectiveness of the new memory structure, a Viterbi decoder that complies with the DAB specifications was constructed. The DAB specifications have a constraint length L of 7 (hence 64 states) and a rate R of ¼. Although the memories considered can be easily adapted for both single and multiple ACU cells approaches, for simplicity the Viterbi structure implemented here has a single state ACS unit, requiring 64 clocks per one stage operation. Also, as it is generally considered that the decoder length should be about five times the constraint length, the trace-back has a memory depth of 35.

The Viterbi decoder based on the two SMU architectures that are the low-power version reported in [11] and the new high-speed low-power version are implemented using Verilog HDL and are functionally verified using Mentor Graphic's ModelSim. The designs are synthesised for ASIC implementation of SMU using Mentor Graphic's Leonardo Spectrum based on 0.35µm CMOS technology. Power dissipation is estimated by observing switching activities and using information provided by [14]. The results are given in Table 1.

TABLE I. ASIC IMPLEMENTATIONS

ASIC 0.35 µm	Low power	High-speed low power
Trace-back memory		
Total Energy/sample , pJ	182	232
- Registers	23.6	26
- Gates	30.5	33
- Nets	61	98
- Clock	67	75
%Energy/Sample compare to RAM	36.4	46.4
Area, mm^2	1.20	2.5
Longest delay, ns	20.45	21
Delay per stage, ns	20.45	0.9
Max bit rate (memory part), Mbps	50	1111
System with one ACS		
Max bit rate, Mbps	1.1	1.1
Area, mm^2	1.8	3.02

It can be seen that the new memory design is 22.7 times faster than the original design. The critical delay per stage of the memory path is 0.9 ns. That corresponds to the maximum bit rate of 1111 Mbps. Compare to the requirement for DAB which can be as high as 5 Mbps [15], it can be seen that the new memory design can easily handle the DAB requirement without the need to employ deep sub micron technology. The bottleneck is now the ACS unit especially where a single unit is used as in this example, for which immediate improvements can be achieved by using techniques such as multiple ACS designs. For power consumption, the power dissipated in the new memory design is slightly increased due to the additional logic and routing, but it is still significantly less than the RAM based equivalent. Given that the SMU contributes more than 50% of the total power consumed by a Viterbi decoder, by using the new memory structure the reduction in power in total is potentially more than 25%. All these advantages are achieved at the expense of a sizable increase in terms of area, which is acceptable in most cases as silicon is now plentiful given sub micron implementations. The register-based design is also more appropriate for a soft IP approach as the code can be 100% portable. This is favorably compared to designs using RAM where a macro RAM block usually needs to be provided by the vendor. The benefit of this flexibility is even more apparent when compared to other approaches such as analog implementation. Deeper sub-micron technology will allow the memory to be used in even more demanding, ultra high-speed low-power applications.

V. CONCLUSIONS

A new high-speed low-power trace-back memory structure for a Viterbi Decoder is proposed. The new memory is based on two arrays of registers interleaved and connected with trace-back signals that decode the output bits on the fly. The structure is used together with appropriate clock gating and power-aware control signals. Based on 0.35 µm CMOS implementation the trace-back back memory consumes and energy of 232 pJ with amaximum bit rate of 1.1 Gbps.

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