Continuous time delta sigma modulators with reduced clock jitter sensitivity.

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Abstract—**In this paper, a technique and method is presented to suppress the effect of clock-jitter in continuous-time delta-sigma modulators with switched-current (current-steering) digital to analogue converters. A behavioural, transistor-level and noise analysis are presented followed by circuit-level simulations. The proposed approach which is a switched-current type of digital to analogue conversion is fully compatible with CMOS processes and multi-bit operations which are widely used in high speed applications. Moreover, having a pulse-shaped output signal does not introduce extra demands on the modulator and hence does not increase the modulator's power consumption. A third-order continuous-time ΔΣ modulator with the proposed digital-to-analogue converter in its feedback was used for circuit-level simulations. Results proved the robustness of the technique in suppressing the clock-jitter effects.**

I. INTRODUCTION

The demands for high-speed, low-power analog to digital conversion have recently made Continuous-Time Delta-Sigma Modulators (CT-ΔΣMs) the most suitable alternative to other Analog to Digital Converter (ADC) techniques. In high-speed applications, CT ΔΣMs show their role off by introducing higher sampling rate/bandwidth, lower thermal noise, built in antialiasing filtering and lower-power consumptions [1],[2]. However, they are susceptible to some nonidealities such as the quantizer and feedback delay and more importantly clock jitter in their feedback Digital to Analog Converters (DACs). The former limitation has been studied well and some robust techniques and solutions have been proposed to resolve them. Also, there have been some proposed techniques to alleviate the clock jitter effects [3], [7].

In this paper, a technique is exposed that suppresses the effects of clock-jitter in the switched-current (SI) DACs and in particular for the CT-ΔΣMs. Comparing to the other techniques, applying the proposed technique to the CT modulators' feedback does not impose any power consumption increase in the modulator (integrators) and is fully compatible with Switched-Current (SI) multi-bit DACs which are widely used in high speed applications.

In section two, the effect of clock-jitter on CT-ΔΣMs with different DAC topologies such as SI, Switched-Capacitor (SC) and Sine (SIN) structures is discussed. The proposed Switched-Shaped-Current (SSI) DAC is presented in section three followed by simulation results, evaluations and conclusions.

II. DEPENDENCY OF THE CLOCK-JITTER EFFECTS ON THE DAC'S OUTPUT SHAPE

A. SI DACs

Referring to Fig. 1(a), in CT-ΔΣMs, clock jitter changes the feedback value by altering the pulse-width of the feedback DAC's output signal. So, clock-jitter causes a slight random variation on the amount of charge fed back to the loop-filter in each clock cycle. This charge error strongly depends on the shape of the DAC output signal and consequently, the performance of the modulator will be dependent on the shape of the DAC output.

In the case of the SI DAC, shown in Fig. 1(b), the output of the DAC has constant values $\pm I_{SI}$. Due to

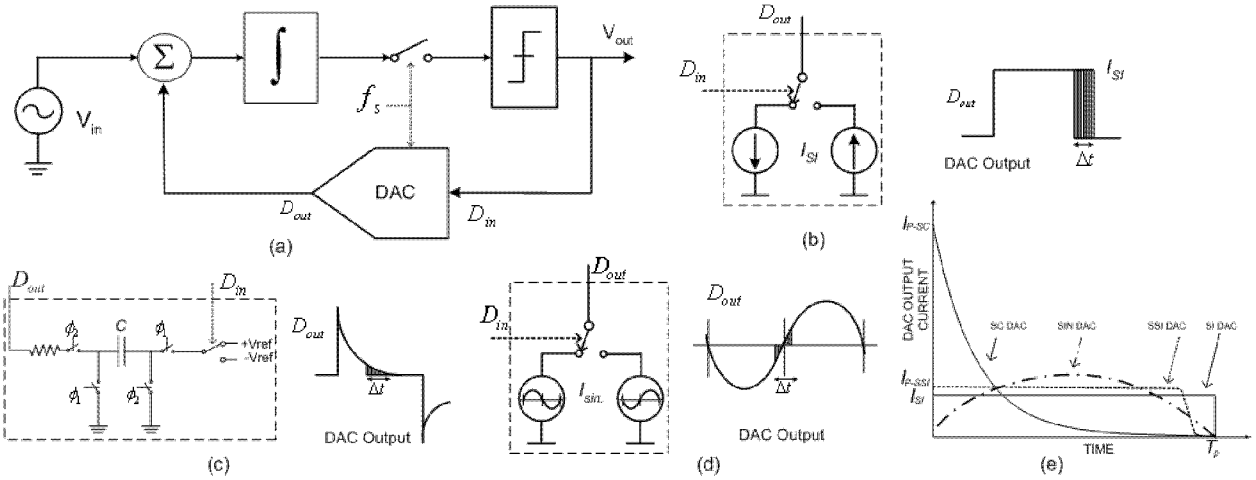

Fig. 1. a) A CT ΔΣM with a general DAC scheme. b) SI DAC c) SC DAC d) SIN DAC e) Output current of SI, SC, SIN and the proposed SSI DAC.

time jitter in the clock signal, both the width and the position of the feedback pulse changes. The latter one, i.e. the pulse position jitter, has much less effect than the pulse-width error [4] and is not considered throughout this paper. Supposing the clock jitter causes a timing error of Δt with a variance of σ_j^2, and the DAC output current levels are $\pm I_{SI}$, the variance of the charge transferred into the loop-filter is:

$$\sigma_{q_{SI}}^2 = \frac{\sigma_j^2 . I_{SI}^2}{\delta^2} \quad (1)$$

where δ is the pulse-width duration per cycle. For a Non-Retun-to-Zero (NRZ) pulse, δ=1 and for a Return-to-Zero (RZ) one, $0<\delta<1$. For the sake of simplicity and comparison with other feedback shapes, throughout this paper, we assume to have a RZ pulse with 50% duty cycle, i.e. δ=0.5.

The maximum signal amplitude is assumed to be -3dB compared to the DAC output signal, so the maximum variance of the signal charge is:

$$\sigma_s^2 = \frac{I_{SI}^2 T_s^2}{4} \quad (2)$$

where T_s is the clock period. If jitter noise is white and is the dominant noise at the output of the modulator, the maximum achievable SNR is the maximum input power divided by the noise power in the signal band, f_b. So the maximum SNR of the modulator with an SI feedback DAC is:

$$SNR_{\max_{SI}} = 10Log\left(\frac{\sigma_s^2}{\sigma_{q_{SI}}^2 / OSR}\right) = 10Log\left(\frac{1}{64 OSR\, f_b^2 \sigma_j^2}\right) \quad (3)$$

B. SC DACs

In [3], using an SC DAC instead of an SI one for CT modulators has been proposed to reduce the effects of clock jitter followed by some reported studies in [4], [5].

Fig. 1(c) shows an SC DAC. During the first phase, the capacitor C is charged and during the second phase, it is discharged to the resistor. This function produces an exponential shape signal fed-back to the modulator. As seen in Fig. 1(c), at the time of clock transition, almost all the capacitor charge has been fed back to the modulator and the time jitter in the clock signal causes a small charge error in comparison to the SI DAC in Fig.1(b). Following the same analytical procedure as was done for the SI DAC, we have:

$$SNR_{\max_{SC}} \approx 10Log\left(\frac{1}{8 OSR\, f_b^2 \sigma_j^2}\left(\frac{1-e^{\frac{T_s}{2\tau}}}{\frac{T_s}{\tau}}\right)^2\right) \quad (4)$$

where $\tau=R.C$ and $\sigma_j << T_s, \tau$. Comparing equations (3) and (4) shows the improvement of the jitter insensitivity of this structure. The bigger T_s/τ, the more the improvement.

This technique is simple and suppresses clock-jitter adequately. However, it has some fundamental drawbacks. The main problem of this architecture is the increase in the power consumption of the integrator which it feeds. It is essential that the integral of the analogue feedback signal undertaken in each clock period is the same as the integral of the one in the ordinary SI. Hence, due to the exponential shape of the analogue feedback of this technique, and considering the pulsing shape of the SI feedback, it can be easily seen that the peak of the current feeding back to the integrator(s) with this technique is much bigger than the one in the SI method. This phenomenon is demonstrated in Fig. 1(e) wherein the current shape in this technique with a peak of $I_{P\text{-}SC}$ is compared to the current shape of a typical SI feedback with an amplitude of I_{SI}. For instance, if at the end of the second phase, the feeding current is around one percent of the one in SI (I_{SI}), the peak of the current in this technique ($I_{P\text{-}SC}$) is more than six times bigger than I_{SI}. Indeed, this technique uses the SC feedback and requires an integrator with a higher Slew-Rate (SR) and Unity-Gain-Bandwidth (UGBW) in comparison to the SI DAC feedback.

On the other hand, the SC DAC technique is not fully CMOS compatible and is not suitable for multi-bit operations because of the matching issues and linearization difficulties. This issue especially gets important in very high-speed applications where the stability is achieved by the multi-bit DAC in the feedback. Moreover, the input (virtual ground) of the integrator that is linked to the output node of the DAC affects the DAC output shape and its jitter insensitivity.

C. SIN DACs

The other proposed technique to alleviate clock-jitter noise effects is to use a Sine-shaped DAC [7]. A simplified schematic of this technique is depicted in Fig. 1(d). As seen in Fig. 1(d), the clock transition acts when the DAC output is almost minimum and hence the time jitter in the clock signal causes a small charge error in comparison to the SI DAC. An analytical analysis of this kind of feedback DAC in CT ΔΣMs can be found in [7], [8].

From the jitter suppression point of view, SIN DACs are not as effective as SC DACs. On the other hand, from the realization point of view, this technique suffers from some drawbacks such as difficulty in realization, sensitivity to the pulse position jitter (unlike the other mentioned DACs), sensitivity to feedback delay, higher power consumption and also noise issues.

III. SWITCHED SHAPED-CURRENT (SSI) TECHNIQUE

To reduce the effects of clock-jitter in the CT-ΔΣMs with no extra demands for SR, DC-gain and UGBW of the integrators, we need to find a DAC that while it has a reasonable amplitude, the most part of its charge has been fed back to the modulator at the time of clock transitions.

A. SSI Structure

In the proposed technique, a **switched** DAC structure is used with an elegant **shaped-current** output named SSI [6]. In this technique, we benefit

from the behavior of a biased-transistor in its saturation and triode regions. For instance, in the CMOS technology, in the saturation region of a transistor, regardless of the drain-to-source voltage, the drain-to-source current is almost constant. When the transistor goes to the triode region, it acts like a resistor and its drain-to-source voltage may diminish to zero. Therefore, if a capacitor is discharged through a biased-transistor, one can expect a current shape that is like a pulse with an almost exponential shape in its falling edge as shown in Fig. 1(e). As a simple explanation of the SSI technique, shown in Fig. 2(a), first a constant amount of charge is stored in capacitor C and then it discharges through a biased-transistor, $M1$. The output will therefore be set to the function of the transistor's current, I_{ref1}.

There can be many ways to realize this technique obtaining similar results without departing from the spirit of the SSI method. Fig. 2(b) shows a single-bit realization [6]. It includes a cascode current mirror which its current comes from a capacitor during the second phase.

During the first phase, Φ_1, capacitor C is fully charged to a reference signal V_{ref}. During the second phase, Φ_2, capacitor C is discharged through transistor $M1$ which is cascoded by transistor $M3$. This cascode tail in parallel with a tail of two diode-connected transistors $M2$&$M4$ constitute a cascode current-mirror. As it is shown in Fig. 2(b), the transistors $M1$ and $M3$ are biased such that in the saturation region, their drain-to-source currents I_{ref1} is a multiple of the reference current I_{ref0}.

To produce the output current of the DAC, a typical switched-current block, X_1, is used as shown in Fig. 2(b). To mirror and sense the current of $M1$, the transistor $M5$ is used in which its gate is coupled to the source of $M3$. The transistor $M5$ acts as a mirror transistor of $M1$ or $M2$.

The circuit works in the following regions as shown in Fig. 2(c):

- **Region R.1**: At the start of the discharging of capacitor C at the second phase, Φ_2, $M1$, $M3$ and $M5$ are in the saturation region and the voltage across capacitor C, V_c, linearly decreases with the rate of nearly I_{ref1}/C. It remains in this mode till V_c meets the saturation voltage of $M3$.

- **Region R.2**: When $M3$ starts going to the triode region, V_c still decreases linearly with a slight slower rate of nearly $I_{ref1}/(C+C_{M3})$ where C_{M3} is the drain capacitance of triode-$M3$. The circuit remains in this mode till $M3$ enters deep triode region ($V_{dsM3} \approx 0$).

- **Region R.3**: After $M3$ goes to deep triode, V_c reaches the gate-source voltage of $M5$ (node $a1$ in Fig. 2(b)) and still decreases linearly but with a rate of $I_{ref1}/(C+C_{M3}+C_{gM5})$ where C_{gM5} is the gate capacitance of $M5$. Hence, the voltage of node $a1$ starts to decrease linearly and $M5$ starts going to weak inversion causing its current I_{SSI} to drop off. In this region, $M1$ is still in the saturation region. The time interval of regions R.1-R.2 (T_{sat}) and region R.3 (T_{lin}) can be roughly estimated by:

$$\begin{cases} T_{sat} \approx \dfrac{C}{I_{ref1}}\left(V_{ref} - V_{GS5}\right) & C_{M3} \ll C \\ T_{lin} \approx \dfrac{C + C_{gM5}}{I_{ref1}}\left(V_{GS5} - V_{th}\right) \end{cases} \quad (5)$$

where V_{th} is the threshold voltage of $M5$.

- **Region R.4**: When the voltage of node $a1$ meets $M1$'s saturation point, it starts decreasing exponentially and makes $M5$ completely turn off. This is the region that the clock transition will take place.

As it is expected, the output current is almost a pulse-shaped. The pulse amplitude of this analogue current ($I_{P\text{-}SSI}$), shown in Fig 1(e), is slightly bigger than the I_{SI} from the SI DAC and is much smaller than the peak current of the SC DAC ($I_{P\text{-}SC}$).

The size of the capacitor, the analogue reference voltage V_{ref} and the cascode current mirror should be set properly to meet two criteria. Firstly, the output signal should fall to a low enough level before the end of the phase (T_p in 1(e)) to ensure that the clock transition time has a minimal effect on the output's integral. Secondly, the falling edge of the output signal should arrive just before (and not too early) the end of the phase (T_p in Fig. 1(e)). If the output signal goes down too early, although the clock jitter has a minimal effect, the output signal's amplitude ($I_{P\text{-}SSI}$ in Fig. 1(e)) should be increased to have the equivalent output signal's integral. The bigger the output signal, the more power consumption in the modulator.

Calculating the clock-jitter for this circuit is a complicated job as it needs analysing the transistors working in saturation, triode and week inversion modes. Using equation (5), one can start simulating the circuit with a rough operating point to determine the shape of the output signal at the clock transition followed by the

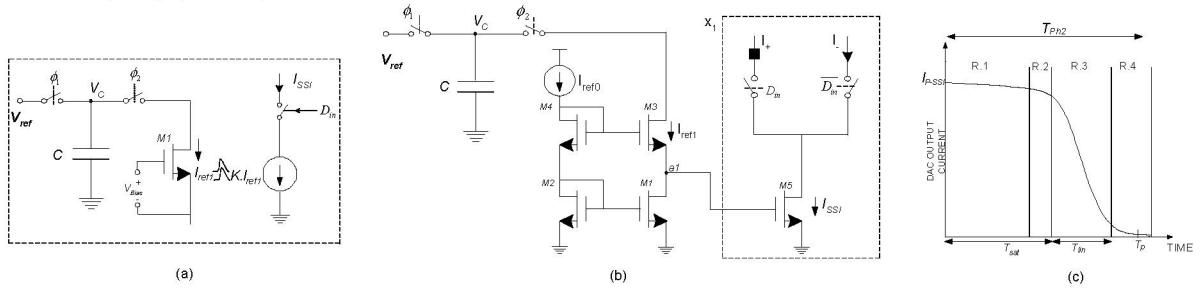

Fig. 2. (a) The basic structure of the SSI jitter-insensitive DAC. (b) A single-bit example of it can be used in a CT-ΔΣM(c) Its output current behaviour.

clock-jitter.

B. Noise Performance

Like the clock-jitter analysis, noise calculation of the structure is a difficult task as the system is dynamic and most of the transistors' operating points are changing between saturation and off regions.

The (KT/C) noise of the two switches contaminates the reference voltage and so changes the *M5*-on-duration. Transistors *M3* and *M4*'s noises go almost straight to node *a1* (Fig. 2(b)). Transistor *M1* has the most noise contribution. If voltage V_{n1} presents on its gate, on one hand *M5*'s current, I_{SSI}, decreases by a factor of $g_{m1}/g_{m3}.g_{m5}.V_{n1}$ and on the other hand, the *M5*-on-duration decreases nearly by a factor of $T_{sat}/I_{ref1}.g_{m1}.V_{n1}$ as the current of *M1* increases and capacitor *C* discharges more rapidly.

Looking at transistor *M2*, if voltage V_{n2} is present on its gate, while *M5*'s current, I_{SSI}, decreases by a factor of $(1-g_{m1}/g_{m3}).g_{m5}.V_{n2}$, the *M5*-on-duration increases nearly by a factor of $T_{sat}/I_{ref1}.g_{m1}.V_{n2}$. As it is seen, unlike *M1*, these two effects are in the opposite direction and result in *M2* having a minor noise contribution.

A very important point in this structure is the noise performance of the bias current I_{ref0}. Generally, bias currents in the current steering DACs are the main noise contributors. Suppose there is an unwanted current I_n in parallel with I_{ref0}. As shown in Fig. 2(b), although it increases *M5*'s current, I_{SSI}, the *M5*-on-duration decreases nearly by a factor of $T_{sat}.I_n/I_{ref1}$. Likewise for *M2*, these two effects are in the opposite direction and suppress the bias circuit noise.

IV. Simulation Results

In order to verify the robustness of the proposed SSI DAC and compare its jitter sensitivity with the conventional SI DAC, a third-order single-bit CT-ΔΣM operating at a sampling frequency of 2.56 MHz and an OSR=128 was used. Circuit-level simulations were performed for both the SI and a fully differential version of the proposed SSI DAC using a generic 0.35um CMOS technology with and without the presence of clock-jitter. A clock jitter with a standard deviation of σ_j=0.01*Ts* was used so that in the presence of jitter, the dominant noise at the output of the conventional modulator is clock-jitter instead of quantization noise. In order to see just the effects of the DACs' nonidealities, all the integrators were designed with a very high dc-gain and unity-gain bandwidth.

The output Power Spectral Density (PSD) of the modulator using SI and SSI DAC schemes with and without the presence of clock-jitter is shown in Fig. 3. As this measurement clearly shows, inducing clock jitter (σ_j=0.01*Ts*) degrades the SNDR of the modulator with the proposed SSI by just 1dB. In this case, using this technique improves the output SNDR by more than 40dB from 45dB for the modulator with a conventional SI DAC to 86.5dB for the modulator with the proposed SSI technique.

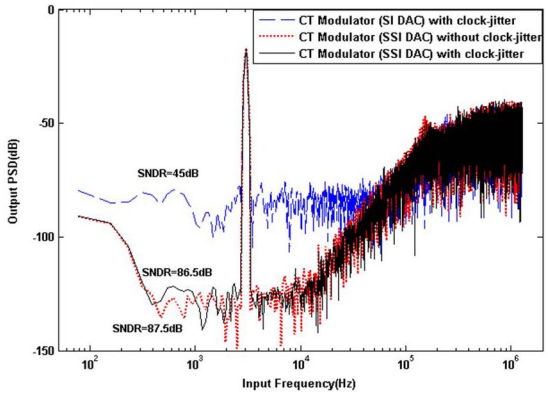

Fig. 3. The output PSD of the third order CT-ΔΣM using SI and SSI DAC schemes with and without the presence of clock-jitter.

It is worth mentioning that using a better technology improves the clock-jitter-rejection behaviour of the SSI DAC as the parasitic capacitors' sizes decrease and so the parasitic current flows diminish at the transition times.

V. Conclusion

A clock-jitter insensitive SI DAC has been presented which can be used in CT ΔΣMs. The technique does not introduce extra demands on the modulator and is fully compatible with CMOS processes and multi-bit operations. Circuit-level simulations demonstrated the high levels of immunity of the proposed technique to clock-jitter.

VI. References

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