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A New Structure for Capacitor-Mismatch-Insensitive Multiply-By-Two Amplification

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Abstract—A new approach to achieve a switched-capacitor multiply-by-two gain-stage with reduced sensitivity to capacitors' mismatches is presented in this paper. It is based on sampling fully differential input signals onto both plates of the input capacitors rather than sampling onto one plate of the capacitors with the other tied to a reference. It uses one operational amplifier (op-amp) in two phases to produce the gain of two ($\times 2$). Comparing to the conventional multiply-by-two gain-stage, the mismatches between the capacitors has a much smaller influence on the accuracy of the gain of two ($\times 2$). Analytical and circuit-level analysis of the architecture and the conventional structure are presented using a generic $0.35\mu\text{m}$ CMOS technology.

I. INTRODUCTION

Process variation in fabrication of high resolution, high speed Analogue to Digital Converters (ADCs) is one of the biggest sources of accuracy degradation. In Switched-Capacitor (SC) systems, it causes mismatches between the fabricated capacitors and changes the whole system's transfer function. Although some systems like delta-sigma modulators can tolerate these mismatches, high resolution ADCs like pipelined ones are highly influenced by the capacitors' mismatches [1]-[3].

A standard pipelined ADC is a cascaded of several serial converters made of one bit ADCs. In each stage, one bit is extracted. Each stage performs the same function of sampling the output of the pervious stage, multiplies it by two and adds to or subtracts from a reference voltage. So, the fundamental function of each stage of a typical pipelined converter relies on a Multiply-By-Two (*MBT* ($\times 2$)) block. A gain error in this function results in nonlinearity in the ADC's transfer function and decreases the accuracy of the converter. Therefore, each *MBT* blocks needs an accuracy and linearity which is as much as the whole of the following stages [1].

As will be seen in the second section, the accuracy of the gain of two ($\times 2$) in the conventional *MBT* blocks which are implemented using the SC approaches is directly restricted by the mismatches between the capacitors. There have been some attempts to overcome this problem in the analogue domain especially in pipelined ADCs using CMOS processes [1]-[5]. Song et. al. in [1] performed capacitor error-averaging using two op-amps in three phases to cancel out the mismatch errors in the analogue domain. Chio in [2]

performed the same technique using just a single op-amp but in four phases designed to be used just in pipelined ADCs. A technique has been presented in [3] operating in four phases using two op-amps designed to be used just in the pipelined ADCs too. Lee et. al. has proposed a technique using one op-amp in two phases by swapping a number of sampling and feedback capacitors [4]. We have proposed a technique using one operational amplifier in three phases which can be applied to a general SC *MBT* amplifiers [5].

In this paper, another new *MBT* Gain Stage (*GS*) is presented which suppresses the dependency of the input-gain of two ($\times 2$) to the capacitors' mismatches. It uses one op-amp in two phases to produce a gain of two using just four capacitors (in fully differential mode) avoiding a complicated switching scheme. While having one op-amp gives the benefit of lower power consumption for the block, operating just in two phases results in more capability for higher speed and lower power consumption too.

In section two, the conventional *MBT-GS* and the effects of the capacitors' mismatches are presented. Section three describes the proposed *GS* and the circuit technique used for compensation. Simulation results and evaluations are presented in section four, with conclusions given in section five.

II. CONVENTIONAL MBT-GS

A conventional *MBT* block is illustrated in Fig. 1. During the first phase, the differential input signal is sampled by four nominally identical capacitors. In the second phase, two of the capacitors are connected to the feedback paths and the others are bottom-plate-sampled by the reference voltages. So, nominally the output will be $(2 \times V_{in} \pm 1 \times V_{ref})$. However, the accuracy of input-signal-gain ($\times 2$) and the reference-signal-gain ($\times 1$) are strongly related to the mismatches between the four input capacitors. Considering just the mismatches, to have 60dB (nearly 10-bit) resolution for the whole converter, the capacitors' mismatches of these *GSs* must be better than 0.05%. Such a matching-requirement especially when other nonidealities and nonlinearities are taken into accounts is the biggest problem and bottleneck to achieving higher resolutions in such converters.

This paper concentrates the correction of the input-signal gain ($\times 2$) rather than the reference-voltage gain (used in

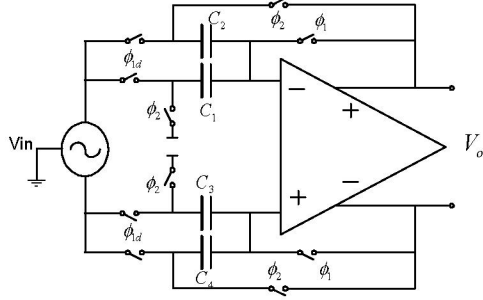


Fig. 1. The schematic of the conventional *MBT-GS* (ϕ_{1d} is the delayed version of ϕ_1).

pipelined-ADCs' stages). So, for the sake of generalization, the reference voltages are considered to be zero throughout the paper. However, it is worth mentioning that the precision of the reference voltages' gain in pipelined-ADCs is an important issue and affects the whole ADC's performance.

To demonstrate the effect of the capacitors' mismatches at the output of the conventional *MBT* ($\times 2$) block shown in Fig. 1, the capacitors are assumed to be slightly mismatched from their ideal value, C , i.e. :

$$C_i = C(1 + \delta_i), \quad i = 1, 2, 3, 4 \quad (1)$$

where $|\delta_1|, |\delta_2|, |\delta_3|, |\delta_4| \ll 1$ are the Gaussian random variables of the relative mismatch error with a mean of zero and a variance (actual variance divided by the square of the mean value) of σ_c^2 . Applying the charge conservation law and assuming an ideal op-amp, the output voltage will be:

$$V_o = \left(\frac{C_1 + C_2}{C_2} + \frac{C_3 + C_4}{C_4} \right) \frac{V_{in}}{2} \Rightarrow \quad (2)$$

$$g = \frac{V_o}{V_{in}} \cong 2 + \frac{(\delta_1 - \delta_2 + \delta_3 - \delta_4)}{2}$$

Assuming $\delta_1, \delta_2, \delta_3,$ and δ_4 are uncorrelated, we have $E[g] = 2$ and $Var_{rel}[g] = \sigma_c^2/4$ where $E[\cdot]$ and $Var_{rel}[\cdot]$ denote the mean (expectation) and the relative variance. It is clear from this that the capacitors' mismatches affect the accuracy of the gain directly.

III. THE PROPOSED MISMATCH-INSENSITIVE MBT-GS

Sampling the differential input signal via both plates of the input capacitors can be used to reduce the mismatch sensitivity of the gain in the conventional *MBT-GSs*, (which was shown in equation (2)). The simple realization of the proposed technique is shown in Fig. 2. Unlike the conventional one in which the charge stored on the capacitors in the sampling phase are transferred between the different capacitors, in this structure, the charge in each capacitor is retained and is almost constant during the two phases and hence the voltage across them remains almost constant.

In the sampling phase (ϕ_1), as shown in Fig. 2(c), the differential input signal is sampled via both plates of capacitors C_1 and C_3 . So;

$$Q_{C_1}(\phi_1) = C_1 V_{in}, \quad Q_{C_3}(\phi_1) = -C_3 V_{in} \quad (3)$$

In this phase the op-amp is not loaded and can be reset. Capacitors C_2 and C_4 do not play a big role in storing or transferring the charge (in both phases). They are considered here as they could be used for amplifying the reference voltages in pipelined ADCs or in the general case can be treated as the op-amp's input capacitances.

During the holding phase (ϕ_2), two capacitors C_1 and C_3 are placed on the feedback path of the op-amp. As has been mentioned earlier, for the sake of generalization, the reference voltages are set to zero and so during phase (ϕ_2) capacitors C_2 and C_4 remains connected to the ground terminal. Assuming an ideal op-amp, the output voltage is:

$$V_o = \frac{Q_{C_1}(\phi_2)}{C_1} - \frac{Q_{C_3}(\phi_2)}{C_3} = \frac{V_{in} C_1}{C_1} - \frac{-V_{in} C_3}{C_3} = 2V_{in} \quad (4)$$

Equation (4) shows that the output voltage does not depend on the capacitors and therefore does not suffer from the mismatches between the capacitors, as was the case in the conventional *MBT-GS*.

Like all other analogue circuits, the performance of the system could be affected by many unwanted nonidealities and nonlinearities. Although in the ideal case of the proposed architecture, it seems that the mismatch problem is completely removed, there are some nonidealities degrading its precision. There are two main obstacles: the charge injection and the parasitic capacitors.

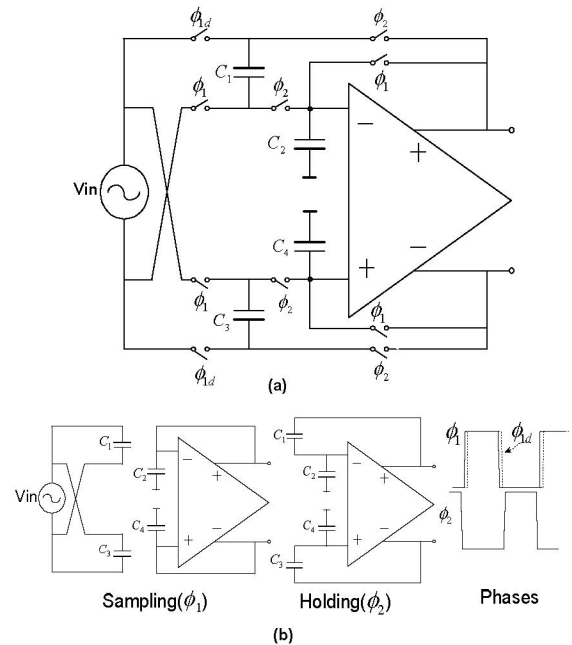


Fig. 2. The proposed *MBT-GS* technique (a) the whole schematic (b) the structure in each phase.

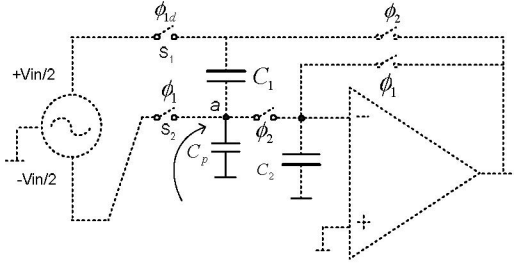


Fig. 3. The nonlinear parasitic capacitor affecting the precision of the GS.

Charge injection is due to mobile channel charge, which is a function of the channel voltage, injected into the sampling capacitors when the input switches turn off. A fraction of the charge goes to each terminal of the switch depending on the ratio of the terminal's capacitances, the switch parameters and the rise and fall time of the clock. So, the charge going to the sampling capacitor can not be predicted easily. If the clock is sharp enough or the terminals have the same impedance, the channel charge will split symmetrically, otherwise, it will mostly flow to the terminal having the lower impedance [6]. Several techniques are used to minimize this problem such as using fully differential structure, bigger capacitors, dummy switches and delayed clocks (Bottom Plate Sampling (BPS))[6]. BPS, the most effective and widely used mechanism, is not beneficial in our structure as the input capacitors are sampled on both plates and none of their plates are connected to a constant/reference voltage (which is the fundamental basis of the BPS technique). As shown in Fig. 3 (the single-ended version of the proposed technique), whether the switch S_1 or S_2 is getting turned off first, because they are both connected to the input source signal, the portion of their channel charge (ηQ_{ch}) which follows to the sampling capacitor C_1 will be input-signal-dependent. Therefore, the accuracy of the sampling and so the precision of the gain of two ($\times 2$) will be degraded.

Another problem of the proposed technique arises from the parasitic capacitors at node a as shown in Fig. 3. This capacitance that is the summation of the parasitic plate capacitance of C_1 and the two parasitic ones of the connected switches is modeled by C_p . The latter term, i.e. the switches' parasitic capacitances are nonlinear and have the worst effect [7]. In the first phase (ϕ_1), C_p is charged by the voltage of around $-V_{in}/2$. In the next phase (ϕ_2), this undesirable charge is completely induced to the inverting input node of the op-amp and so is pushed into C_1 which is now in the feedback. Considering both the charge injection and the parasitic capacitors, for a fully differential structure, the output voltage is almost:

$$V_o \cong 2 \left(1 + \frac{C_p}{2C_1} \right) V_{in} + 2 \frac{\eta Q_{ch}}{C_1} \quad (5)$$

To compensate these errors, an opposite amount of charge equal to the charge induced parasitically by C_p plus the switches' charge-injection to the feedback capacitors during the second phase (ϕ_2) should be induced into the inverting and non-inverting input nodes of the op-amp.

Using this method, the unwanted charge will appear as a common-mode input and will be attenuated in the differential mode output by the Common Mode Rejection Ratio (CMRR). Fig. 4 shows the whole proposed technique with the compensation circuit which circumvents the identified shortcomings.

As shown in this figure, the complementary version of each sampling circuit is added to the op-amp. In the holding phase (ϕ_2) each complementary circuit is connected to an input node of the op-amp which its corresponding pair is connected to another one. For example, in the holding phase (ϕ_2), while the C_1 -circuit is connected to the inverting input node of the op-amp, its complement (the C_{11} -circuit) is connected to the non-inverting one.

As shown in Fig. 4, during the first phase (ϕ_1), both plates of C_{11} are connected to the same potential, In_n . So, the parasitic capacitor in the node a_{11} is charged to a similar level as the one in node a_1 . Likewise, the parasitic capacitor in the node a_{33} is charged to a similar level as the one in node a_3 . On the other hand, at the end of this phase, as delayed clocks (ϕ_1 and ϕ_{1d}) are used (Fig. 4), first one plate of the capacitors is disconnected from the input signal (the one connected to a_x node) followed by the other plate. So, having the same capacitors and switches, the charge injections into C_1 and its counterpart C_{11} (both come from the switches driven by ϕ_1) is almost the same and similarly the same for C_3 and C_{33} .

During the holding phase (ϕ_2), while C_1 is placed in the feedback between the output and the inverting input, its counterpart C_{11} is connected to the non-inverting input. So the same charge error that enters into the inverting node is injected to the non-inverting node. It works in the same way for C_3 and C_{33} . Having this, the output of the GS will be:

$$V_o(\phi_2) = 2V_{in} + \frac{\Delta Q_{ch} + \Delta Q_{Cp}}{C} \quad (6)$$

where ΔQ_{ch} and ΔQ_{Cp} are the charge errors in the compensation of charge-injection and parasitic capacitors, respectively. The complementary circuits were designed with the same structures and sizes as their counterparts and

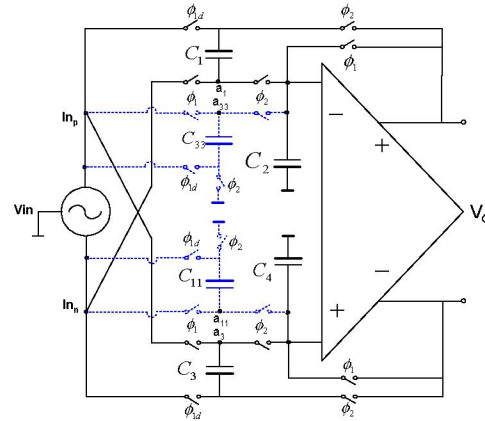


Fig. 4. The proposed technique including the compensation circuit.

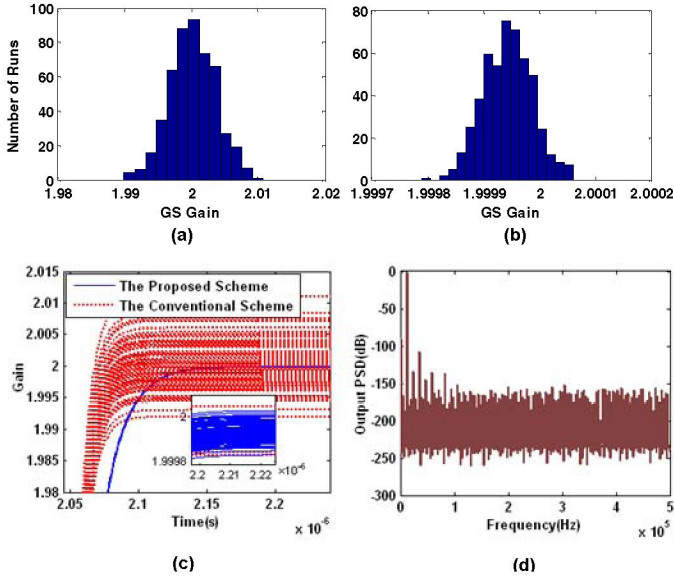


Fig. 5. Evaluation of the proposed structure using 500 Monte-Carlo simulations with a 1% relative-mismatch for the capacitors and switches, (a) The histograms of the gain of the typical (b) and the proposed architecture. (c) The transient gain variation of both topologies. (d) The output PSD for a single tone input signal.

should be laid out carefully to have the best matching between the parasitic capacitors and make their charge-injections identical. With this, the whole error will appear as a common-mode signal and will hence be decreased by a factor equal to the *CMRR* of the op-amp.

It is a difficult task to derive a straight equation like equation (2) for this circuit. However, it can be seen from equation (6) that the charge-error is not caused by the mismatch between the big sampling capacitors (as was the case in the ordinary *GSs*) and comes from the mismatches in the switches' charge-injections and parasitic capacitors. Therefore a much more accurate gain is expected and was proved by the circuit level simulations, as seen Fig. 5.

IV. SIMULATION RESULTS

HSPICE circuit-level Monte-Carlo simulations were performed on the conventional (Fig. 1) and the proposed (Fig. 4) *GS* to evaluate and validate the proposed structure's precision and performance. To see just the effects of the capacitors and switches' mismatches, the op-amp was realized employing ideal components model configuration while all of the switches were realized using a generic 0.35 μm CMOS technology. The sampling capacitor values were set to 2pF and the parasitic capacitors of nodes a_i in Fig. 4 were considered to 20fF. For all the capacitors and switches, the relative mismatch ($3\sigma/E[\cdot]$) of 1% was used. Fig. 5(a) and 5(b) show the histograms of the gain of the conventional and the proposed structures using 500 Monte-Carlo simulations for the two architectures with the same mismatches in the components. Fig. 5(c) also shows the transient results for both. As it is observed, while the gain of the conventional *GS* varies in the span of almost 20mV

around 2, the gain of the proposed one just varies in the span of almost 0.2mV. In these circuit-level simulations, the 3σ -relative-mismatch of the gain for the conventional was 5.1×10^{-3} while it was 6.4×10^{-5} for the proposed one, which is 80 times smaller. The smaller the switches and the parasitic capacitors of nodes a_i in Fig. 4, the more improvement one get. The output Power Spectral Density (*PSD*) of the proposed architecture for a single tone, shown in Fig. 5(d), assures us that the new architecture does not introduce linearity problems. It has around 107dB Spurious-Free-Dynamic-Range (*SFDR*) in the worst case of 500 Monte Carlo simulations.

Using the bigger capacitors, smaller switches (i.e. better technology) and careful layout could also reduce the gain mismatch further. Employing this technique, the accuracy of *MBT-GSs* will be mostly limited by the op-amps' DC gain and linearity not by the capacitors' mismatches as was the case in the conventional ones previously reported.

V. CONCLUSION

In this paper, a new SC multiply-by-two ($\times 2$) gain-stage with reduced sensitivity to capacitors' mismatches has been presented. The technique is based on sampling fully differential input signals via both the plates of the sampling capacitors using one op-amp in two phases. To reduce the unwanted effects of the parasitic capacitors and also the switches' charge injections, a compensation circuit has been incorporated. Performing Monte-Carlo circuit-level simulations clearly showed the mismatch-relaxation of the new architecture compared to the conventional structure.

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