Modeling of switched-capacitor delta-sigma Modulators in SIMULINK.

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Modeling of Switched-Capacitor Delta–Sigma Modulators in SIMULINK

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***Abstract*—Precise behavioral modeling of switched-capacitor $\Delta\Sigma$ modulators is presented. Considering noise (switches' and op-amps' thermal noise), clock jitter, nonidealities of integrators and op-amps including finite dc-gain (DCG) and unity gain bandwidth, slew-limiting, DCG nonlinearities and the input parasitic capacitance, quantizer hysteresis, switches' clock-feedthrough, and charge injection, exhaustive behavioral simulations that are close models of the transistor-level ones can be performed. The DCG nonlinearity of the integrators, which is not considered in many $\Delta\Sigma$ modulators' modeling attempts, is analyzed, estimated, and modeled. It is shown that neglecting this parameter would lead to a significant underestimation of the modulators' behavior and increase the noise floor as well as the harmonic distortion at the output of the modulator. Evaluation and validation of the models were done via behavioral and transistor-level simulations for a second-order modulator using SIMULINK and HSPICE with a generic 0.35-μm CMOS technology. The effects of the nonidealities and nonlinearities are clearly seen when compared to the ideal modulator in the behavioral and actual modulator in the circuit-level environment.**

***Index Terms*—Charge injection, clock feedthrough, correlated double sampling, delta–sigma modulators, hysteresis, nonideality, nonlinearity, SIMULINK, switched capacitor.**

I. Introduction

Among the oversampling converters, $\Delta\Sigma$ ones have achieved the most attraction recently in high-resolution applications due to their noise shaping behavior that leads them to inherent superior linearity, simple realization, and low sensitivity to circuit imperfections [1]. Such converters reduce the need for complex analog circuit implementation and, due to their oversampling nature, act as the most suitable architectures for accurate low to moderately high frequency applications.

$\Delta\Sigma$ modulators can be realized in either the continuous-time (CT) or switched-capacitor (SC) approach. While CT modulators have the advantages of lower power consumption, higher speed, and intrinsic anti-aliasing filtering, they suffer from the difficulty of designing, sensitivity to clock jitter, and also excess loop delay [2]. As far as the implementation technique is concerned, SC modulators are preferred to CT modulators because they can be more efficiently realized in standard CMOS technology [1], [3]. Moreover, they provide a highly controllable design as well as being more robust to clock jitter and feedback delay problems. In this paper, the SC $\Delta\Sigma$ modulators are considered.

Although $\Delta\Sigma$ modulators have relatively straightforward realizations, the appropriate architecture selection, including single loop or MASH, loop filter type, order and coefficients, and the number of bits of the quantizer, would be a difficult task. Also, the requirements of the building blocks such as integrators' bandwidth, dc-gain (DCG), slew rate and output swings, the quantizer threshold, the digital-to-analog converter (DAC), the switches, and the clock and power supply accuracy cannot be easily estimated. Several techniques have been used for time-domain analysis of these modulators listed and discussed briefly in [3], such as SPICE, SWITCAP, and table-lookup models. For instance, the SPICE simulations are precise, but they take extremely long times especially for very high-resolution narrow-band modulators because of both long period cycles and the high accuracy needed. Hence, choosing the optimized architecture and estimating the requirements of building blocks is a very time-consuming procedure in transistor-level design and simulation (SPICE). There is a need for a time-efficient and accurate simulation environment. To this effect, the user friendly, versatile SIMULINK tool was chosen to develop detailed models of the modulators' building blocks. The popular SIMULINK simulator proved to be an excellent time-efficient candidate for this initial task.

In this paper, detailed analytical models of the basic building blocks (integrators and op-amps) and also the nonidealities of a typical modulator are presented, followed by SIMULINK models of them. Most previous $\Delta\Sigma$ modulator models have not considered the effect of DCG nonlinearity in integrators, leading to a significant underestimation of the modulators' behavior and harmonic distortion. In this paper, this is analyzed, estimated, and modeled in SIMULINK, as well as other blocks of a typical $\Delta\Sigma$ modulator. Moreover, several behavioral and transistor-level simulations were performed in SIMULINK and HSPICE using a generic 0.35-μm CMOS technology to validate the analyses and models. Since in the first stage of very high-resolution modulators correlated-double-sampled (CDS) integrators are routinely used to attenuate the effect of offset and flicker noise, for comparison purposes, both typical and CDS integrators are discussed in this paper.

In Section II, the integrator characteristics such as finite DCG, nonlinear DCG, and settling behavior are presented. Section III presents noise contributors such as sampling and op-amp thermal noise. Switch nonidealities are considered next following with a discussion about clock jitter. In Section VI, a brief review of quantizer nonidealities are discussed. Then the

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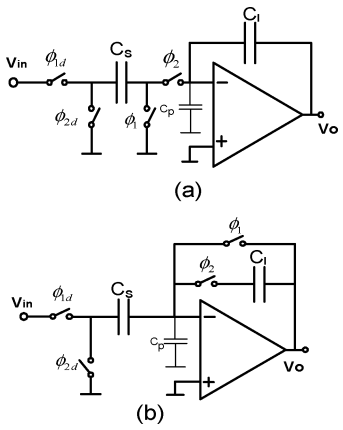

Fig. 1. Single-ended SC integrators. (a) Typical and (b) CDS.

simulation results and evaluation of the models will be presented in Section VII.

II. Integrator Nonidealities

The z-domain transfer function of an ideal delayed integrator is

$$H(z) = g\frac{z^{-1}}{1-\alpha z^{-1}} \quad \alpha = 1 \tag{1}$$

where g and α are the integrator's gain and leakage, respectively [4]. Although zero delay integrators can be used to realize the desirable filter, most often delay integrators are used in the first stage of the modulators as they are easily implemented in circuit level. In the case of a nonideal integrator, α deviates from unity. There are several architectures to realize this transfer function of the integrator. Fig. 1 shows a typical and a CDS integrator (for simplicity of illustration, we have opted to deploy the single-ended configuration. However, all our practical investigations were carried out on full differential versions of these integrations). While the typical integrators are widely used in moderate accuracy $\Delta\Sigma$ modulators, the CDS ones are used for very high-resolution approaches for attenuating offset and Flicker noise of the front-end integrator [4]. The size of the op-amp's input transistors are kept large to minimize the op-amp's noise in very high-resolution $\Delta\Sigma$ modulators; consequently the op-amp's input capacitance is also increased. These capacitors have also been considered in the models of the integrators.

There are many nonidealities that alter the ideal transfer function of (1), including the integrator's finite DCG and bandwidth, slew-limiting, and DCG nonlinearities. These effects, which are the major causes of performance degradation in SC $\Delta\Sigma$ modulators, are discussed in this section.

A. Finite DCG

The finite DCG moves the pole of the ideal integrator in (1) from dc ($z = 1$) to another frequency. This effect is known as a leakage in the integrator. The precise transfer function of the two integrators shown in Fig. 1(a) and (b) is

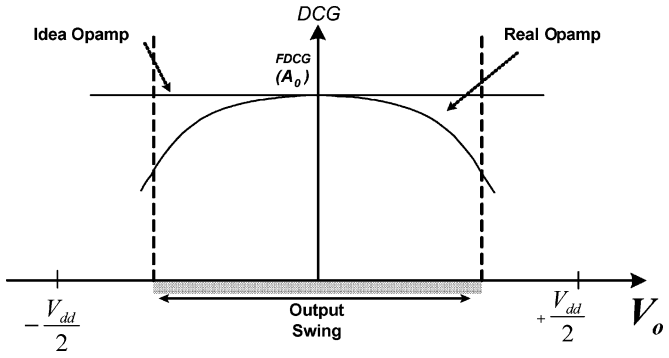

Fig. 2. A typical op-amp's DCG versus output voltage with the rail-to-rail voltage of V_{dd}.

$$H_{\text{typ}}(z) = \underbrace{k_s\left(1-\frac{1+k_s+k_p}{A_0}\right)}_{g_{\text{typ}}}\frac{z^{-1}}{1-\left(\underbrace{1-\frac{k_s}{A_0}}_{\alpha_{\text{typ}}}\right)z^{-1}} \tag{2}$$

$$H_{\text{CDS}}(z) = \underbrace{k_s\left(1-\frac{1+k_s+k_p}{A_0}\right)}_{g_{\text{CDS}}}\frac{z^{-1}}{1-\left(\underbrace{1-\frac{k_s+k_p}{A_0}}_{\alpha_{\text{CDS}}}\right)z^{-1}} \tag{3}$$

where $k_s = C_s/C_I$, $k_p = C_p/C_I$, and C_p and A_0 are the op-amp's input parasitic capacitance and the finite DCG, respectively. Equations (2) and (3) clearly show that the finite DCG degrades the integrator's gain and moreover introduces leakage which is different in the two integrators.

B. Settling Behavior

Slew rate (SR) and unity-gain bandwidth (UGBW) are the two distinct parts of the settling behavior of the op-amps. While in SR-limited region, the output of the op-amp operates in its nonlinear part, in the bandwidth-limited region (small-signal settling period) it behaves linearly [5], [6]. In the high-resolution applications, the integrator is forced to settle in fast regime wherein the settling time constant τ is smaller than an upper limit and the SR is larger than a lower limit [7]. Therefore, for an integrator, in the presence of its op-amp's UGBW and SR, its settling behavior will be linearly/nonlinearly affected. With the assumption of a single-pole model for the integrator, (4) and (5) show the output voltages of the integrators in Fig. 1 in the n^{th} integrating phase, respectively

$$V_{o\_\text{typ}}(t) = V_{o\_\text{typ}}(nT_s - T_s) + k_s V_i\left(1-e^{-t/\tau}\right) \tag{4}$$

$$V_{o\_\text{CDS}}(t) = (V_{o\_\text{CDS}}(nT_s - T_s) + k_s V_i)\left(1-e^{-t/\tau}\right) \tag{5}$$

where τ is the integrator time-constant, $V_i = V_m(nT_s - T_i)$, T_s, and T_i are the clock period and the integrating period (phase ϕ_2 in Fig. 1), respectively. The settling behavior of the two integrators is different because the CDS integrator resets at each sampling phase while the typical one does not. If the integrator

SR is greater than the maximum slope of the output voltage (at $t = 0$), slew-limiting never occurs. Otherwise, the output will slew before the time instant t_0 where the slew-limitation ends and is derived from the relation [5]

$$\left.\frac{d}{dt}V_o(t)\right|_{t_0} = SR. \tag{6}$$

The output voltages of the integrators in Fig. 1 in the nth integrating phase are obtained from (7) and (8), respectively, as shown at the bottom of the page.

For implementing the above equations in single expressions to be incorporated as a SIMULINK functions, (7) and (8) can be merged and resume up to

$$V_{o\_\mathrm{typ}}(nT_s) = V_{o\_\mathrm{typ}}(nT_s - T_s) + k_s V_i - \mathrm{sgn}(V_i) SR\tau \times \exp\left(-\left(1 + \frac{T_i}{\tau} - \frac{k_s |V_i|}{SR\tau}\right)\right) \tag{9}$$

$$V_{o\_\mathrm{CDS}}(nT_s) = V_{o\_\mathrm{CDS}}(nT_s - T_s) + k_s V_i - \mathrm{sgn}(V_i) SR\tau \times \exp\left(-\left(1 + \frac{T_i}{\tau} - \frac{V_{o\_\mathrm{CDS}}(nT_s - T_s) + k_s |V_i|}{SR\tau}\right)\right) \tag{10}$$

where $\mathrm{sgn}(\cdot)$ denotes the Signum function. The Signum function and the absolute value of V_i are incorporated to contemplate both the rise and fall slopes.

In the above analysis of settling behavior for both integrators, it is assumed that the valid data are produced at the end of the second phase (nT_s). However, this is only true for the CDS one. For the typical integrator, the output data are sampled by the next stage of the modulator at the end of the next phase. As the integrator characteristic in this phase is changed (the input capacitor is disconnected and also the output capacitance is changed), the integrator will show a transient behavior which will affect the output voltage. The output at the end of this phase can be derived in the same way as for the previous phase using (9). This dynamic transient behavior is discussed in [8]. Moreover, there is a more precise settling behavior analysis in [6].

C. Nonlinear DCG

Although the finite DCG of the integrators affects the position of the dominant pole and changes the integrator's gain, it does not directly contribute to distortion. Distortion is introduced by the integrator's DCG nonlinearity resulting from its dependency on the output voltage as shown in Fig. 2, where the rail-to-rail output swing is assumed to be V_{dd}. This important effect is not considered in the previous $\Delta\Sigma$ modeling attempts, for example, as was the case with [3].

The op-amp's DCG can be expressed as that in [9]

$$A \cong A_0\left(1 + \alpha_1 |V_o| + \alpha_2 |V_o|^2 + \alpha_3 |V_o|^3 + \cdots\right). \tag{11}$$

From (11) and Fig. 2 it is apparent that the op-amp's DCG in fully differential configurations is nearly an even function and will hence produce the odd harmonic in the output, as will be seen in the results section of this paper. In [10], for the sake of simplicity, we have extracted the DCG-nonlinearity equations without using the absolute value function. However, from the SIMULINK modeling point of view, we can use this function in the blocks' modeling.

To derive the output voltage of the typical integrator in Fig. 1(a), the nonlinear DCG in (11) is substituted into terms g and α in (2)

$$\alpha_{\mathrm{typ}} = \left(1 - \frac{k_s}{A_0}(1 - \alpha_1 |V_{o\_\mathrm{typ}}(nT_s)| - \alpha_2 V_{o\_\mathrm{typ}}^2(nT_s) + \cdots)\right)$$

$$g_{\mathrm{typ}} = k_s\left(1 - \frac{1 + k_s + k_p}{A_0}(1 - \alpha_1 |V_{o\_\mathrm{typ}}(nT_s)| - \alpha_2 V_{o\_\mathrm{typ}}^2(nT_s) + \cdots)\right). \tag{12}$$

Using the SIMULINK function, direct estimation of the output voltage of an integrator with the nonlinear-DCG is a very difficult task because α and g are functions of instantaneous output voltage that itself depends on α and g at the same time and so creates a delayless loop. Here, for first-order estimation of α and g, $|V_o(nT_s)|$ is approximated by its ideal value that is the term $|V_o(nT_s - T_s) + k_s V_{\mathrm{in}}(nT_s - T_s)|$. As a result, the terms α_{typ} and g_{typ} in (12) will be

$$\alpha_{\mathrm{typ}} = \left(1 - \frac{k_s}{A_0}(1 - \alpha_1 |V_{o\_\mathrm{typ}}(nT_s - T_s) + k_s V_{\mathrm{in}}(nT_s - T_s)| - \alpha_2 |V_{o\_\mathrm{typ}}(nT_s - T_s) + k_s V_{\mathrm{in}}(nT_s - T_s)|^2 + \cdots)\right)$$

$$g_{\mathrm{typ}} = k_s\left(1 - \frac{1 + k_s + k_p}{A_0}(1 - \alpha_1 |V_{o\_\mathrm{typ}}(nT_s - T_s) + k_s V_{\mathrm{in}}(nT_s - T_s)| - \alpha_2 |V_{o\_\mathrm{typ}}(nT_s - T_s) + k_s V_{\mathrm{in}}(nT_s - T_s)|^2 + \cdots)\right). \tag{13}$$

Likewise, the term α_{CDS} in (3) will be

$$\alpha_{\mathrm{CDS}} = \left(1 - \frac{k_s + k_p}{A_0}(1 - \alpha_1 |V_{o\_\mathrm{CDS}}(nT_s - T_s) + k_s V_{\mathrm{in}}(nT_s - T_s)| - \alpha_2 |V_{o\_\mathrm{CDS}}(nT_s - T_s) + k_s V_{\mathrm{in}}(nT_s - T_s)|^2 + \cdots)\right) \tag{14}$$

and g_{CDS} will be like g_{typ} in (13).

The discussed DCG nonlinearity can be taken into account by the integrator model shown in Fig. 3. As shown, the nonlinear DCG introduces an additional loop to the single-loop configuration of the integrator. Furthermore, although the effect of the nonlinear DCG, modeled by g and α, is taken into account, the saturation levels of the op-amp are ensured by the saturation block as shown in Fig. 3.

This DCG nonlinearity model enables us to estimate the maximum permitted output swing of the integrators. Two ways

$$V_{o\_\mathrm{typ}}(t) = \begin{cases} V_{o\_\mathrm{typ}}(nT_s - T_s) + SRt & t \le t_0 \\ V_{o\_\mathrm{typ}}(t_0) + (k_s V_i - SRt_0)\left(1 - e^{-(t-t_0)/\tau}\right) & t > t_0 \end{cases} \tag{7}$$

$$V_{o\_\mathrm{CDS}}(t) = \begin{cases} SRt & t \le t_0 \\ V_{o\_\mathrm{CDS}}(t_0) + (V_{o\_\mathrm{CDS}}(nT_s - T_s) + k_s V_i - SRt_0)\left(1 - e^{-(t-t_0)/\tau}\right) & t > t_0 \end{cases} \tag{8}$$

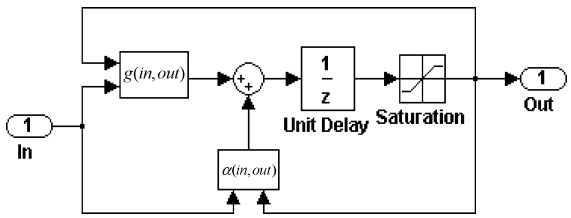

Fig. 3. Model of an integrator with nonlinear DCG.

can decrease the effect of it: first, decreasing the integrator's output swing that can lead to the decrement of the modulator's signal-to-(noise plus distortion) ratio (SNDR), and second, increasing the finite DCG and designing an op-amp with high linear DCG which both increase the power consumption of the integrator. So, a tradeoff between these two factors should be considered.

III. Noise

Sampling noise and the op-amp's thermal and flicker noise of the first integrator are the fundamental limitation in the design of high-resolution $\Delta\Sigma$ modulators [4]. The noise of the other stages is suppressed and shaped due to the nature of the $\Delta\Sigma$ modulator. In our models, flicker noise is not considered because some techniques like CDS approach substantially reduce its effect [11].

A. Sampling Noise

Sampling noise is defined as the thermal noise of the switch resistance sampled by a capacitor [1]. It is bandlimited by the equivalent time-constant of the sampling circuit and has the power of

$$e_N^2 \cong \frac{kT}{C_s} \tag{15}$$

where k, T, and C_s are Boltzmann's constant, the temperature in kelvin, and the sampling capacitor, respectively [5]. To model the effect of kT/C noise, the input-referred sampling noise of the integrator should be calculated and consequently added to the input signal. The input-referred sampling noise of the integrators in Fig. 1 is approximately

$$e_{N-\text{in}}^2 \cong 2\frac{kT}{C_s} \tag{16}$$

which results from the thermal noise of the input switches in both sampling and integrating phases.

B. Op-Amp's Thermal Noise

This noise that is due to the thermal noise of its transistors is modeled in a similar fashion to the sampling noise. The input-referred thermal noise of the typical integrator shown in Fig. 1(a) is [7]

$$V_{N\text{th}-\text{in}}(z) = \left(1 + \frac{(1-z^{-1})}{k_s}\right) V_N(z) \tag{17}$$

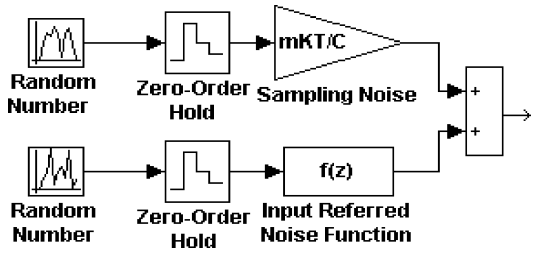

Fig. 4. Model of sampling and input referred op-amp's noise sources in SIMULINK.

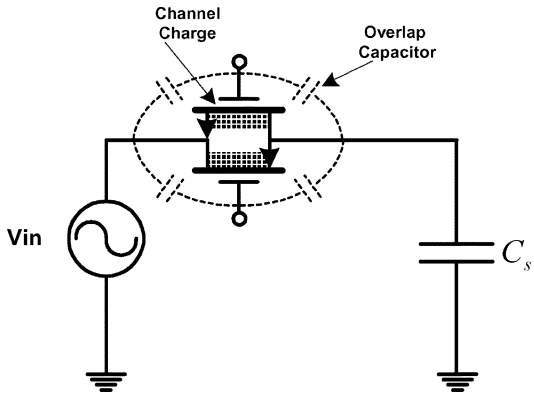

Fig. 5. A typical S/H.

and for the CDS one shown in Fig. 1(b) is

$$V_{N\text{th}-\text{in}}(z) = \left((1-z^{-1/2}) + \frac{(1-z^{-1})}{k_s}\right) V_N(z) \tag{18}$$

where V_N denotes the input-referred thermal noise of the op-amp.

Both the sampling and thermal noise can be taken into account by the SIMULINK model shown in Fig. 4.

IV. Switch Nonidealities

Switches are one of the major elements in SC circuits. The ideal role of them is to have zero or infinite resistance when they are on or off. However, as switches in CMOS technology are realized by using nMOS and pMOS transistor, they manifest some nonidealities such as nonlinear on-resistance, clock-feedthrough, and charge injection [12].

Nonlinear on-resistance which is a signal-dependent variation of the on-resistance of the switch introduces harmonic distortion into the circuit. There are many ways to degrade this nonlinearity, such as decreasing the sample and hold (S/H) time constant, using transmission gates, clock-boosting and bootstrapping (in low-voltage applications), etc. [12], [13].

Clock-feedthrough is due to the charge of the gate-to-source overlap capacitors of the switch injected to the sampling capacitor when it turns off. The error charge due to the clock-feedthrough for the S/H shown in Fig. 5 is

$$\begin{aligned}\Delta Q_{\text{out}} &= -C_{ovn}(V_{dd} - V_{ss}) + C_{ovp}(V_{dd} - V_{ss}) \\ &= -(C_{ovn} - C_{ovp})(V_{dd} - V_{ss})\end{aligned} \tag{19}$$

where C_{ovn} and C_{ovp} represent the overlap capacitors on nMOS and pMOS transistors, respectively. This error is signal

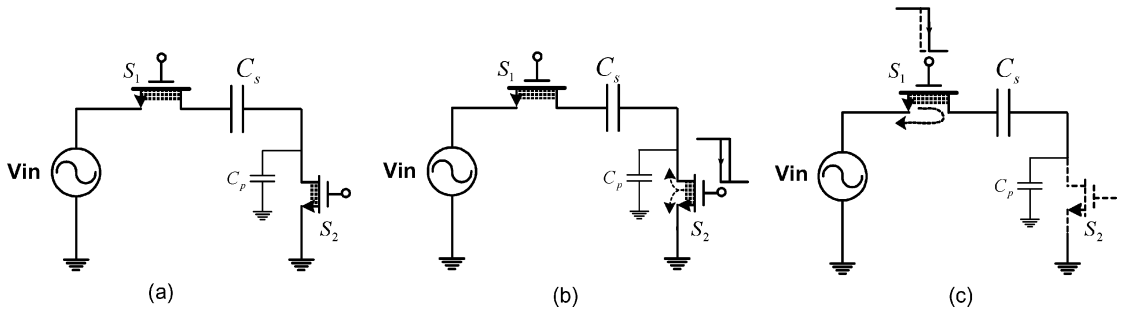

Fig. 6. The BPS realization. (a) An S/H schematic. (b) First, switch S_2 turns off and releases some signal-independent charge into the sampling capacitor C_s. (c) Then, while C_s is almost floating, the input switch S_1 turns off and releases some signal-dependent charge that mostly folds back to the input source.

independent and in a fully differential integrator is attenuated by the common-mode rejection ratio (CMRR) of its op-amp.

Charge injection is due to mobile channel charge injected to the sampling capacitor when the switch turns off. This charge flows out from the channel mostly to the drain and the source and a little to the substrate [11]. The fraction of the charge going to each terminal depends on the ratio of the terminal's capacitance, the switch parameters, and the slope of the clock. So, the charge going to the sampling capacitor cannot be predicted easily. If the clock is sharp enough or the terminals (the drain and the source) have the same impedance, the channel charge will split symmetrically; otherwise, it will mostly flow to the terminal showing the lower impedance [11]. For the CMOS switch shown in Fig. 5, the error charge due to this nonideality is

$$\Delta Q_{\text{out}} = -\eta_l W_n L_n C_{ox} \left(V_{dd} - V_{tn} - V_{\text{in}}\right) + \eta_l W_p L_p C_{ox} \left(V_{\text{in}} - V_{ss} - |V_{tp}|\right) \quad (20)$$

where C_{ox}, W_x, L_x, and V_{tx} are the gate-to-oxide capacitance, channel width, channel length, and threshold voltage of the nMOS or the pMOS transistor, respectively. The factor η_l is the fraction of the charge coming into the sampling capacitor rather than coming back to the input source. Taking a quick look, (20) shows that the error charge is linearly proportional to the input signal. However, as V_{tx} is a function of the input signal [5], the charge error will be a nonlinear function of the input signal and introduces harmonic distortion into the circuit. If the nMOS and the pMOS transistor have the same dimension size, this error will be eliminated. However, to have a linear on-resistance in the CMOS switch, i.e., to have a switch with maximum dynamic range, different sizes are considered for these two transistors resulting to the charge injection. A more precise charge-injection modeling can be found in [13]. Several techniques are used to attenuate this problem such as using fully differential structure, bigger capacitors, dummy switches, and shifting clocks [bottom plate sampling (BPS)] [11].

A BPS mechanism widely used in $\Delta\Sigma$ modulators is shown in Fig. 6. As demonstrated in this figure, when the switches are going off, first, the bottom switch (S_2) turns off and a few moments later, the input switch (S_1) turns off. The amount of charge injected to the sampling capacitor when S_2 turns off is signal-independent as it is connected to the ground. When S_1 turns off, the sampling capacitor is floating and so the switch charge flows back to the input source. Therefore, in this mechanism, only some signal-independent charge enters into the circuit, which can be greatly attenuated using fully differential configuration.

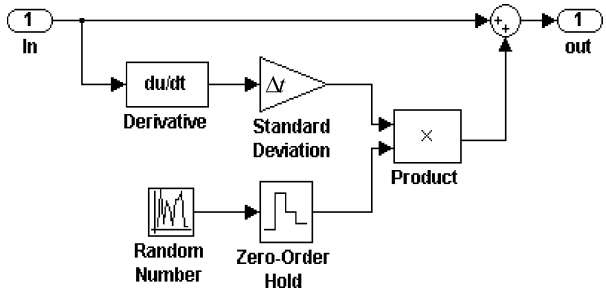

Fig. 7. Clock-jitter modeling in the input front-end of the modulator.

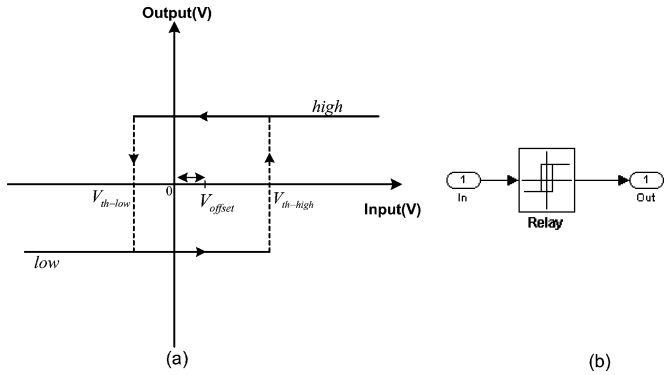

Fig. 8. (a) Quantizer functions including hysteresis and offset. (b) SIMULINK model of it.

Although BPS reduces the switch charge injection, there are still some leakages. When S_2 is off, the sampling capacitor is not ideally floated and is in series with the capacitor C_p, the parasitic capacitance of switch S_2, and the following stage of it. Hence, a portion of the charge will flow to the sampling capacitor. To model this leakage, the factor η_l in (20) should be replaced by

$$\eta_{\text{BPS}} = \eta_l \frac{C_p}{C_p + C_s}. \quad (21)$$

For first-order estimation, in the integrators of Fig. 1, this leakage charge is compensated in the integrating phase (ϕ_2) as the parasitic capacitor C_p becomes in parallel with the sampling capacitor C_s. For second-order estimation these charge errors leak to the integrating capacitor as a function of op-amp's DCG and CMRR.

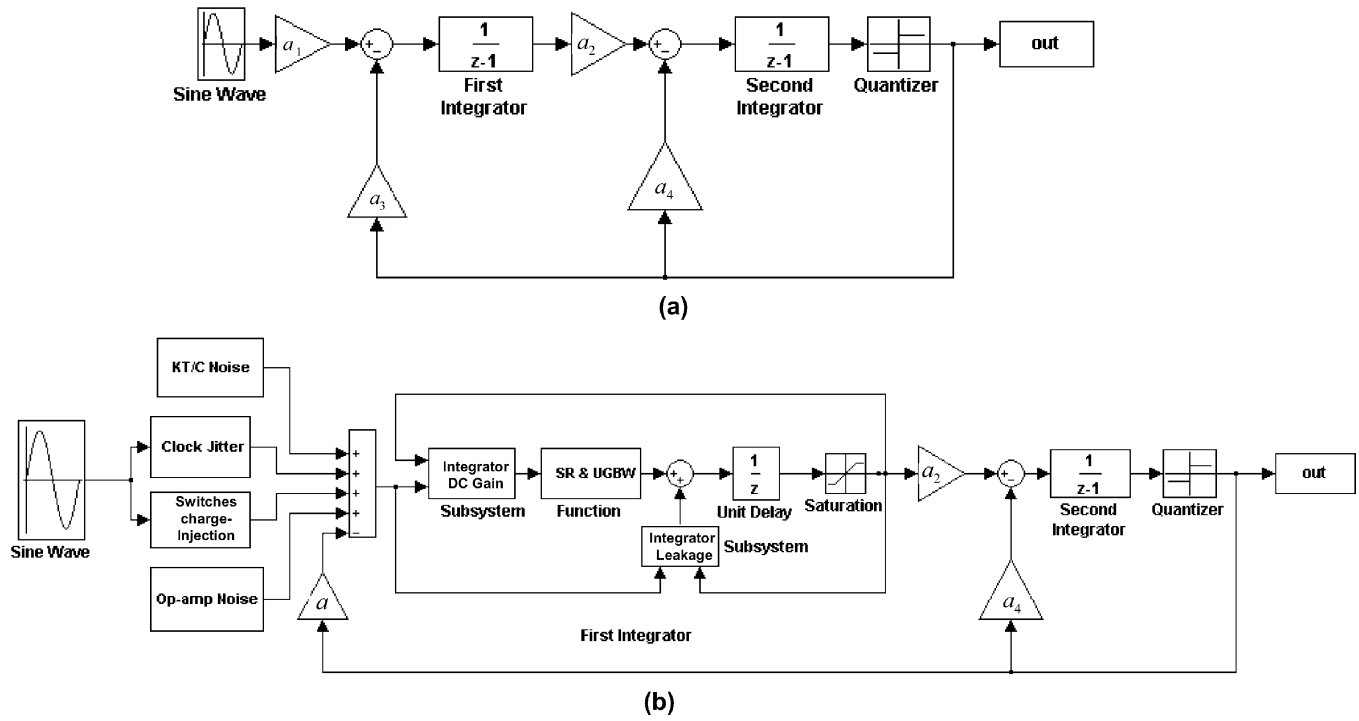

Fig. 9. (a) Ideal second-order single-loop single-bit $\Delta\Sigma$ modulator. (b) Its nonideal model.

TABLE I
PARAMETERS OF THE MODULATOR SHOWN IN FIG. 9

Parameters	Value
Oversampling Ratio (*OSR*)	256
Clock Frequency (MHz)	12.28
Input Sinusoidal Frequency (kHz)	7.3
a_1, a_3	0.2
a_2	0.5
a_4	0.25
a	1

V. CLOCK JITTER

Clock jitter, the intrinsic uncertainty in the transition time of the clock, increases the in-band noise of the modulator [1]. It has less effect on the sampled-data part of the modulators. The effect of clock jitter on an SC modulator is dominated by its effect on the sampling time of the analog input signal. If $V_{\rm in}$ is the analog input signal, the error resulting from an inaccuracy of δ in the clock transition time will be

$$V_{\rm in}(\delta + t) - V_{\rm in}(t) \cong \delta \frac{dV_{\rm in}(t)}{dt} \qquad \delta \ll T_s. \tag{22}$$

Under the assumption that the time jitter δ is an uncorrelated Gaussian random process having standard deviation Δ_t, implementation of (22) can be done in SIMULINK by the model shown in Fig. 7. The upper bound of the in-band error power at the output of the modulator for a sinusoidal input will be [1]

$$S_{\max} \cong \frac{\Delta^2}{8} \frac{(2\pi B \Delta_t)^2}{\rm OSR} \tag{23}$$

where OSR, B, and Δ are the oversampling ratio, the maximum input signal frequency, and its amplitude, respectively. This equation shows the well-known fact that the total in-band error power is decreased by either increasing OSR or decreasing the input bandwidth [1].

VI. QUANTIZER

A quantizer suffers from some nonidealities such as offset and hysteresis. For 1-bit $\Delta\Sigma$ modulators, the quantizer is a comparator. Offset of the comparator is attenuated by the dc gain of the previous stages, and so the modulator is almost insensitive to it. The hysteresis occurrence shown in Fig. 8(a) has a twofold worsening effect: increasing the noise power and shifting the noise spectrum toward the signal band [14]. Both offset and hysteresis were modeled in SIMULINK using the simple Relay block shown in Fig. 8(b). Their effects were found to be insignificant for moderately small level of deviation from ideal. It was further observed that to have a noticeable effect, the hysteresis parameters had to be substantially increased.

VII. SIMULATION AND EVALUATION RESULTS

In order to validate the behavioral model derived in this paper and compare the effects of nonidealities and nonlinearities with the ideal modulator, first, the second-order low-pass $\Delta\Sigma$ modulator shown in Fig. 9 with the parameters listed in Table I was used. As mentioned before, in the behavioral simulations, only the nonidealities of the first integrator were considered, as the others are substantially shaped and suppressed.

Fig. 10 shows the output SNDR of the modulator as a function of the integrator time-constant τ and SR of the first integrator. It shows that decreasing the SR or increasing τ will decrease the output SNDR. In the case of non-slew-limiting, the large τ (finite UGBW) ideally acts as an integrator gain-reducer that $\Delta\Sigma$ modulators are less sensitive to. However, in an actual modulator, because of the nonlinear DCG of the integrators,

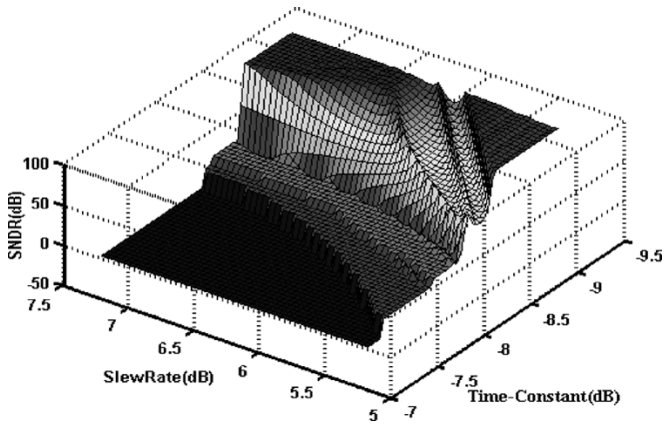

Fig. 10. The output SNDR as a function of time-constant and SR.

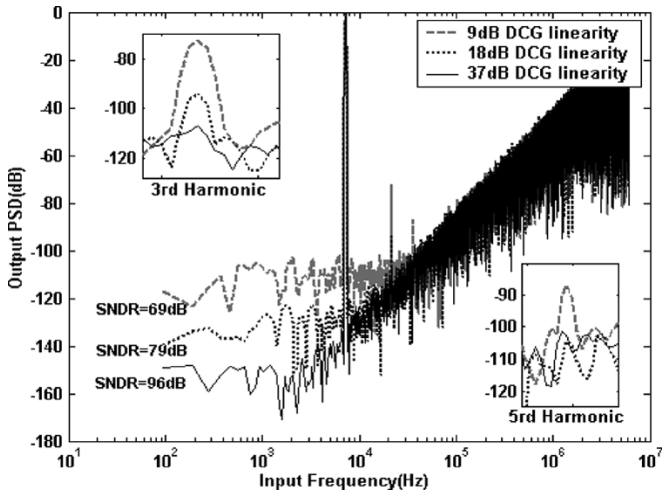

Fig. 11. The PSDs of the modulator output with the first integrator nonlinear DCG of 9, 18, and 37 dB.

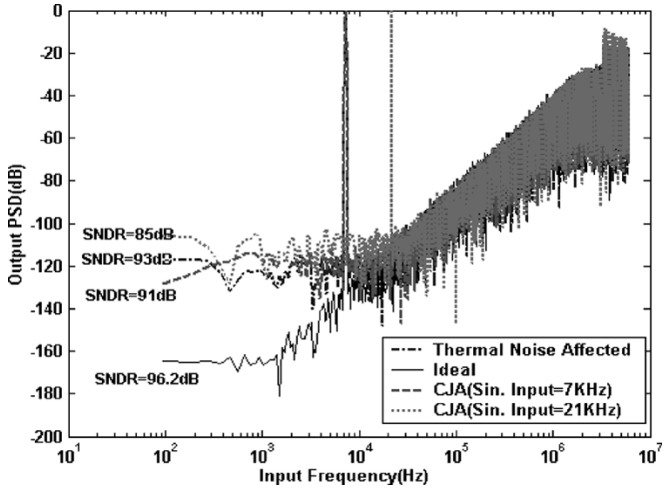

Fig. 12. The output PSDs of the ideal, thermal noise affected, and CJA modulator with the parameters shown in Table II.

this nominally ideal gain-reducer will be nonlinear [7] and so introduces harmonic distortion into the output, as will be shown in the next paragraph.

Fig. 11 shows the output spectrum of the modulator with the first integrator's nonlinear DCG. It is clearly seen that the nonlinear DCG introduces odd harmonic distortion to the output of the modulator and moreover increases the in-band noise level. The amount of linearity needed for the DCG of the first integrator is subject to the whole desired SNDR, and as shown in Fig. 11, with 37 dB linearity, the SNDR equals 96 dB. The most efficient way to increase the DCG linearity is to decrease the output levels of the integrators, which can be done by signal-scaling [7].

TABLE II
SPECIFICATION OF THE MODULATOR SHOWN IN FIG. 9 WITH THE PARAMETERS LISTED IN TABLE I USED FOR SIMULINK SIMULATIONS

Parameters	Value
Sampling Capacitance (pF)	2
Input-Referred Op-amp's Thermal Noise (μV_{rms})	30
Clock Jitter (ns) (standard deviation (Δ_t))	1

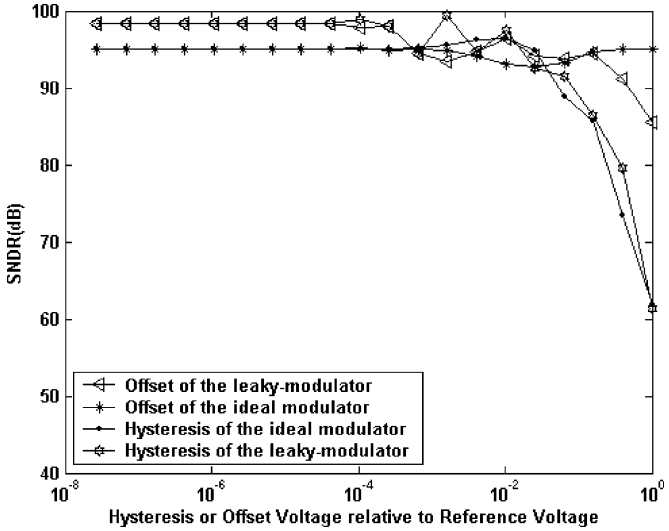

Fig. 13. The output PSD of the ideal and leaky modulator ($\alpha = 0.001$ for both stages) of Fig. 9 with parameters of Table I versus hysteresis or offset voltage relative to the reference voltage.

Fig. 12 shows the output power spectral densities (PSDs) of the ideal, thermal noise affected, and clock jitter affected (CJA) modulator with the parameters shown in Table II. It is clearly seen that these nonidealities increase the in-band noise floor as expected. In the case of clock jitter, it is shown that the noise floor is dependent on the input sinusoidal frequency as suggested by (22).

To see the effect of the quantizer hysteresis and offset, the output SNDR of the modulator versus hysteresis and offset relative to the reference voltage is shown in Fig. 13. The ideal and leaky modulators (the modulator with leaky integrator modeled) were used to illustrate how leakages in integrators worsen the effect of these imperfections on the output SNDR. It has been observed that the modulators are almost insensitive to the offset voltage of the quantizer, and they are more sensitive to hysteresis than offset. Moreover, it is clearly seen that the less the integrator leakage in the modulator stages, the more the output SNDR. However, this is not a big constraint, and such a quantizer can be easily designed.

To be more precise, for the comparison between the behavioral models, derived in this paper, and the circuit-level (transistor-

TABLE III
PARAMETERS OF THE MODULATOR SHOWN IN FIG. 9 USED FOR CIRCUIT-LEVEL SIMULATION

Parameters	Value
Oversampling Ratio (*OSR*)	128
Clock Frequency (MHz)	25.6
Input Sinusoidal Frequency (kHz)	15.625
a_1, a_3	0.28
a_2	0.648
a_4	0.274
a	1
First Integrator's *DCG* linearity (for its limited output-swing)	11dB
DCG	74dB
SR(V/μs)	560
UGBW (MHz)	670

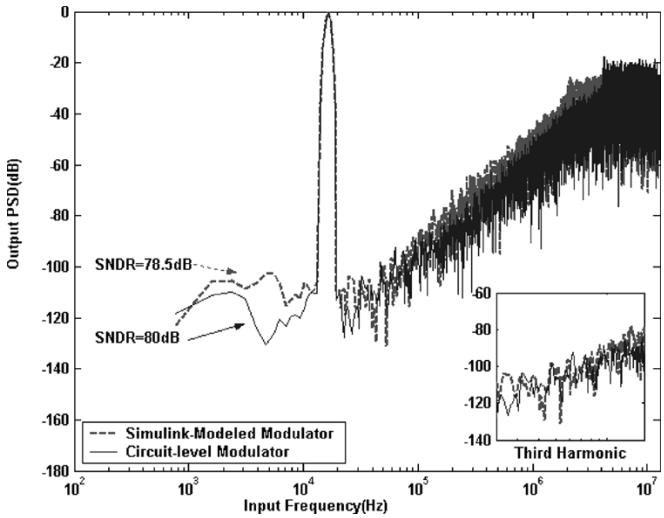

Fig. 14. Output PSD of the ideal, SIMULINK-modeled, and HSPICE (circuit-level) modulator shown in Fig. 9 with the parameters of Table III.

level) modulator, the second-order modulator shown in Fig. 9 with the parameters listed in Table III for GSM application was performed and simulated in HSPICE using a generic 0.35 μm CMOS technology. Fig. 14 shows the output PSD of the SIMULINK modeled and transistor-level modulators. The SNDRs of the transistor-level and the SIMULINK behavioral-level modulators are 80 and 78.5 dB, respectively. These outputs show a good agreement between the behaviorally modeled and circuit-simulated modulator.

VIII. CONCLUSION

In this paper, a discussion and precise behavioral model of the SC $\Delta\Sigma$ modulator including noise (switches' and op-amp's thermal noise), clock jitter, the finite DCG and UGBW of the integrators, slew-limiting, DCG nonlinearities, input parasitic capacitance, hysteresis, switches' clock-feedthrough, and charge injection are presented. The effect of DCG nonlinearity in integrators, which most $\Delta\Sigma$ modulator modeling attempts undertaken in the past did not consider, has been analyzed, estimated, and modeled in SIMULINK, as well as the other blocks of a typical $\Delta\Sigma$ modulator. It is shown that neglecting DCG nonlinearity leads to a significant underestimation of the modulators' behavior and harmonic distortion. Evaluation and validation of the models were done via behavioral and circuit-level simulations for two second-order modulators using SIMULINK and HSPICE with a generic 0.35-μm CMOS technology. The effects of the nonidealities and nonlinearities which were modeled are clearly seen when compared to the ideal and transistor-level simulated modulator.

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REFERENCES

[1] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 22, no. 12, pp. 1298–1308, Dec. 1988.
[2] O. Shoaei, "Continuous-time delta-sigma A/D converters for high speed applications," Ph.D. dissertation, Carleton Univ., Ottawa, ON, Canada, 1996.
[3] P. Malcovati *et al.*, "Behavioral modeling of switched-capacitor sigma–delta modulators," *IEEE Trans. Circuits Syst.*, vol. 50, no. 3, pp. 352–364, Mar. 2003.
[4] S. R. Northworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters*. Piscataway, NJ: IEEE Press, 1997.
[5] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.
[6] Y. Geerts, M. S. J. Steyaert, and W. Sansen, "A high-performance multibit $\Delta\Sigma$ CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829–1840, Dec. 2000.
[7] S. Rabii and B. A. Wooley, *The Design of Low-Voltage, Low-Power Sigma-Delta Modulators*. Norwell, MA: Kluwer, 1999.
[8] R. del Rio *et al.*, "Reliable analysis of settling errors in SC integrators: Application to $\Sigma\Delta$ modulators," *Electron. Lett.*, vol. 36, pp. 503–504, Mar. 2000.
[9] F. Medeiro *et al.*, "Modeling opamp-induced harmonic distortion for switched-capacitor SD modulator design," in *IEEE Int. Symp. Circuits Systems*, vol. 5, May-Jun. 1994, pp. 445–448.
[10] H. Zare-Hoseini and I. Kale, "On the effects of finite and nonlinear DC-gain on the switched-capacitor delta-sigma modulators," in *Proc. IEEE Int. Symp. Circuits Systems*, May 2005, pp. 2547–2550.
[11] C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 48, no. 11, pp. 1584–1614, Nov. 1996.
[12] J. Shieh, M. Patil, and A. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 4, pp. 277–281, Apr. 1987.
[13] X. Weize and E. G. Friedman, "Clock-feedthrough in CMOS analog transmission gate switches," in *Annu. IEEE Int. ASIC/SOC Conf.*, Sep. 2002, pp. 181–185.
[14] R. Khoini-Poorfard and D. A. Johns, "On the effect of comparator hysteresis in interpolative $\Sigma\Delta$ modulators," in *IEEE Int. Symp. Circuit Syst.*, vol. 2, May 1993, pp. 1148–1151.

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