Design and Implementation of Novel FPGA Based Time-Interleaved Variable Centre-Frequency Digital Sigma-Delta Modulators

Kalafat Kizilkaya, I., Al-Janabi, M. and Kale, I.

This is the publisher version of an article published in the Special Issue of ACTA IMEKO Journal 4 (1) 68-76 2015. The final definitive version is available online at: https://acta.imeko.org/index.php/acta-imeko/article/view/IMEKO-ACTA-...

ACTA IMEKO
February 2015, Volume 4, Number 1, 68 – 76
www.imeko.org

Design and implementation of novel FPGA based time-interleaved variable centre-frequency digital Σ–Δ modulators

Işıl Kalafat Kızılkaya, Mohammed Al-Janabi, Izzet Kale

University of Westminster, 115 New Cavendish Street, W1W 6UW, London, UK

ABSTRACT
Novel, multi-path, time-interleaved digital sigma-delta modulators that can operate at any arbitrary frequency from DC to Nyquist are designed, analysed and synthesized in this study. Dual- and quadruple-path fourth-order Butterworth, Chebyshev, Inverse Chebyshev and Elliptical based digital sigma-delta modulators, which offer designers the flexibility of specifying the centre-frequency, pass-band/stop-band attenuation as well as the signal bandwidth are presented. These topologies are compared in terms of their signal-to-noise ratios, hardware complexity, stability, tonality and sensitivity to non-idealities. Detailed simulations performed at the behavioural-level in MATLAB are compared with the experimental results of the FPGA implementation of the designed modulators. The signal-to-noise ratios between the simulated and empirical results are shown to be different by not more than 3-5 dBs. Furthermore, this paper presents the mathematical modelling and evaluation of the tones caused by the finite wordlengths of these digital multi-path sigma-delta modulators when excited by sinusoidal input signals.

Section: RESEARCH PAPER

Keywords: Sigma- Delta modulator; Time-Interleaved; D/A conversion; Tonality; VHDL; FPGA

Citation: Işıl Kalafat Kızılkaya, Mohammed Al-Janabi, Izzet Kale, Design and implementation of novel FPGA based time-interleaved variable centre-frequency digital Σ–Δ modulators, Acta IMEKO, vol. 4, no. 1, article 11, February 2015, identifier: IMEKO-ACTA-04 (2015)-01-11

Editor: Paolo Carbone, University of Perugia

Received December 16th, 2013; **In final form** April 28th, 2014; **Published** February 2015

Funding: (none reported)

Corresponding author: Işıl Kalafat Kızılkaya, e-mail: i.kalafat_kizilkaya@my.westminster.ac.uk

1. INTRODUCTION

Sigma-Delta (Σ-Δ) modulators have been used in many applications such as in data converters [1] and frequency synthesizers [2]. They employ relatively simple hardware in combination with oversampling and noise-shaping to acquire high resolution [3], [4]. However, conventional discrete-time and digital single-stage Σ–Δ modulators are mostly limited to narrowband signal applications due to their high oversampling requirements [3-6]. On the other hand, emerging technologies such as GSM, GNSS, CDMA, DECT have accelerated the need for designers to implement Σ-Δ modulators that have extended bandwidths while also maintaining relatively relaxed OverSampling Ratios OSRs [1], [2], [7].

The Time-Interleaving (TI) technique overcomes this limitation by using M inter-connected Σ–Δ modulators working in parallel, where the processing speed of the modulator can be reduced by M times. A further advantage of the TI approach is that it offers an elegant means to increase the signal bandwidth for both A/D and D/A applications without the need to use faster or higher-order Σ–Δ modulators [5-7].

There are several behavioural- and circuit-level TI Σ–Δ modulator topologies reported in the open literature but to the best knowledge of the authors, all these topologies have concentrated on LowPass (LP) and mid-band resonator based Σ–Δ modulators [5-9].

In recent studies, analog multi-path TI variable-centre frequency Σ–Δ modulators were designed, analysed, evaluated and compared using ideal and non-ideal behavioural-level models [10], [11]. In [12], the concepts proposed on discrete-time TI variable-centre frequency Σ–Δ modulators were extended to Digital Sigma-Delta Modulators (DDSMs), whose Noise Transfer Functions (NTFs) employed Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters. The first objective of this paper is to implement these designed behavioural-level DDSMs on the Xilinx® Spartan™-3 Development Kit. The second objective is to evaluate and compare the

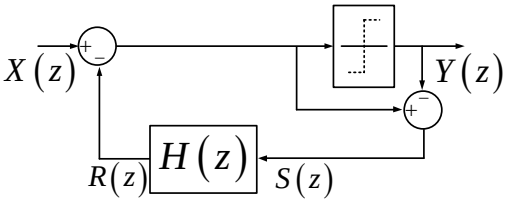


Figure 1. Block diagram of the EF topology.

performance of these DDSMs with their behavioural level counterparts, therefore further validating the design process published in [12].

A major challenge associated with the design of high-resolution single-bit quantizer DDSMs is that they are highly tonal [13-17]. However, it is a well-known phenomenon that single-bit Σ–Δ D/A converters require significantly less hardware when compared to their multi-bit counterparts, as the latter need extra Dynamic Element Matching (DEM) circuitry [3], [18]. Digital MASH Σ–Δ modulators, whose constituent Σ–Δ modulators employ single-bit quantizers, overcome this problem by reducing the quantization bits step-by-step in each block, therefore substantially alleviating the occurrence of spectral tones as well as ensuring modulator stability [16], [17], [19].

In [12], the tonal behaviour caused by the finite wordlengths of digital variable centre-frequency single-bit based Σ–Δ modulators when excited by sinusoidal input signals was mathematically modelled. As this is an extension of the reported work in [12], the mathematical model is discussed covering the tonal behaviour of the TI topologies.

2. TI VARIABLE-CENTRE FREQUENCY DDSM DESIGN

The TI Σ–Δ modulator design starts with the conventional SinglePath (SP) Σ–Δ modulator prototype, which involves two main steps: the synthesis of the NTF followed by the mapping of the NTF to an appropriate topology [4].

The generalized transfer function of an L^{th}-order BandStop (BS) NTF is given in (1) which can be obtained for a given design by specifying the filter type (i.e. Butterworth, Chebyshev, etc.), centre frequency, bandwidth as well as the attenuation parameters.

$$NTF(z) = \frac{\prod_{k=1}^{L}(1-2\alpha_k z^{-1}+z^{-2})}{1+b_1 z^{-1}+\cdots+b_{L-1}z^{-L+1}+z^{-L}} \quad (1)$$

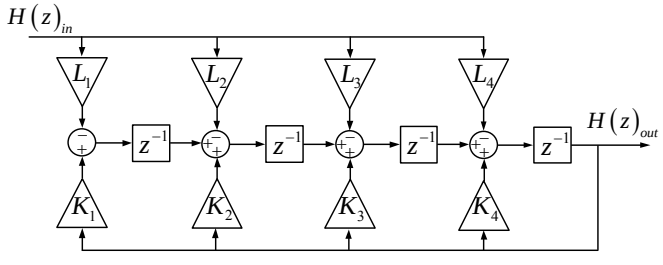


Figure 2. The TDA topology.

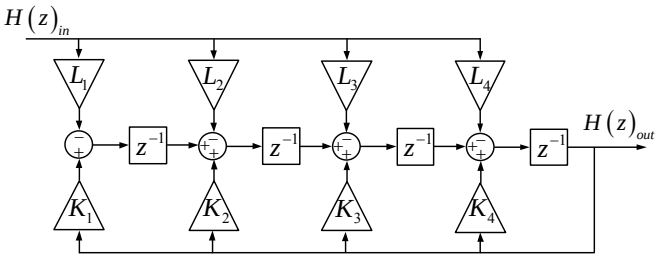


Figure 3. Designed 2-Path TI topology.

In [12], a 4th-order Error-Feedback (EF) topology was chosen for the D/A modulators as this topology does not cause any signal corruption for its unity-gain Signal Transfer Function (STF).

The final design step involves assigning an appropriate loop-filter topology. The Time Delay and Accumulate (TDA) topology, commonly known as the Direct Form-1 IIR filter topology, shown in Figure 2, is preferred for the loop-filter as this topology uses smaller feedback and feedforward coefficients. Note that in this study, fixed-point arithmetic is used where these implementations are likely to result in overflow due to the recursive nature of the IIR filters. Also instead of accumulators, delayers are used as the main building blocks to contain the internal signals, therefore preventing overflow and hence resulting in fewer internal data paths. Table 1 summarizes the designed filter specifications and Table 2 shows their corresponding coefficients.

As proposed in [12], the node-equation method is applied to convert the designed SP Σ–Δ modulator to its N-path TI counterpart. It is an easy-to-apply technique and results in fewer components when compared to the polyphase decomposition method [6], [7]. The main idea of the node equation method is to write the node equations of the SP topology in the time-domain and individually convert these equations in a time-interleaved manner to construct the corresponding N-path topology. Figure 3 depicts the 2-Path TI topology of the SP Σ–Δ modulator given in Figures 1, 2. Moreover, a 4-Path topology using this developed technique was designed, modelled and evaluated as will be reported in Section 4.

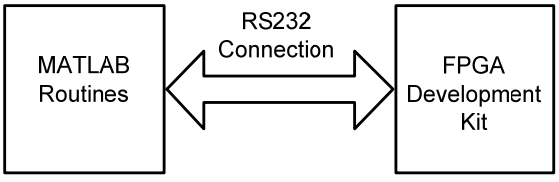


Figure 4. Set-up environment.

Table 1. Designed Filter Specifications.

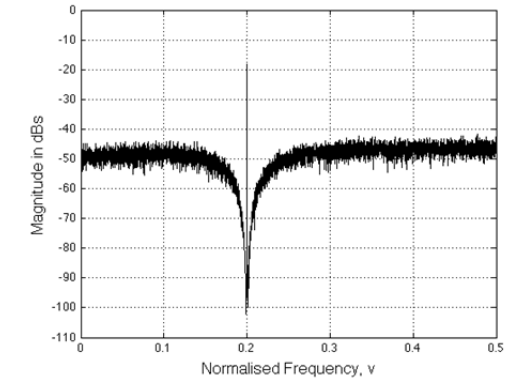
Design Specs.	Butterworth	Chebyshev	Inv. Chebyshev	Elliptical
Centre-Frequency	0.2	0.2	0.2	0.2
Bandwidth	0.02	0.004	0.02	0.02
Passband Ripple	-	1 dB	-	1 dB
Stopband Ripple	-	-	60 dB	80 dB

Table 2. Feedback and Feedforward Coefficient.

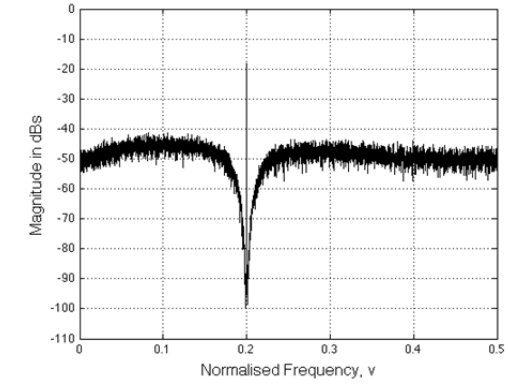
		K_1	K_2	K_3	K_4	L_1	L_2	L_3	L_4
Butterworth	Fractional	0.0549	-0.2099	0.1557	-0.1628	-1.1836	2.1736	-1.0828	0.8372
	sD.15-bit	1799	-6878	5103	-5335	-38785	71223	-35481	27433
Chebyshev	Fractional	0.0406	-0.1548	0.1133	-0.1175	-1.1980	2.2287	-1.1252	0.8825
	sD.15-bit	1329	-5072	3713	-3850	-39255	73030	-36870	28918
Inverse Chebyshev	Fractional	0.2323	-0.8750	0.5650	-0.5381	-1.0037	1.5067	-0.6711	0.4619
	sD.15-bit	7613	-28672	18513	-17634	-32890	49370	-21991	15134
Elliptical	Fractional	0.0406	-0.1548	0.1133	-0.1175	-1.1980	2.2287	-1.1252	0.8825
	sD.15-bit	1329	-5072	3713	-3850	-39255	73030	-36871	28918

Table 3. Allocated FPGA Sources.

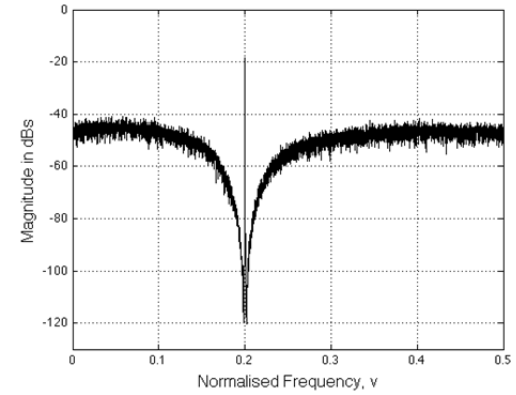
Design Specs.		Butterworth	Chebyshev	Inv. Chebyshev	Elliptical
SP	# Slices Used	$^{158}/_{40,960}$ ~1%	$^{158}/_{40,960}$ ~1%	$^{162}/_{40,960}$ ~1%	$^{158}/_{40,960}$ ~1%
	# LUTs	$^{289}/_{40,960}$ ~1%	$^{281}/_{40,960}$ ~1%	$^{294}/_{40,960}$ ~1%	$^{282}/_{40,960}$ ~1%
	# Mult. 18x18	$^{8}/_{40} = 20\%$	$^{8}/_{40} = 20\%$	$^{8}/_{40} = 20\%$	$^{8}/_{40} = 20\%$
2-Path	# Slices Used	$^{174}/_{40,960}$ ~1%	$^{174}/_{40,960}$ ~1%	$^{179}/_{40,960}$ ~1%	$^{174}/_{40,960}$ ~1%
	# LUTs	$^{435}/_{40,960}$ ~1%	$^{435}/_{40,960}$ ~1%	$^{458}/_{40,960}$ ~1%	$^{435}/_{40,960}$ ~1%
	# Mult. 18x18	$^{16}/_{40} = 40\%$	$^{16}/_{40} = 20\%$	$^{16}/_{40} = 20\%$	$^{16}/_{40} = 40\%$
4-Path	# Slices Used	$^{196}/_{40,960}$ ~1%	$^{196}/_{40,960}$ ~1%	$^{201}/_{40,960}$ ~1%	$^{196}/_{40,960}$ ~1%
	# LUTs	$^{747}/_{40,960}$ ~1%	$^{747}/_{40,960}$ ~1%	$^{794}/_{40,960}$ ~1%	$^{747}/_{40,960}$ ~1%
	# Mult. 18x18	$^{32}/_{40} = 80\%$	$^{32}/_{40} = 80\%$	$^{32}/_{40} = 80\%$	$^{32}/_{40} = 80\%$



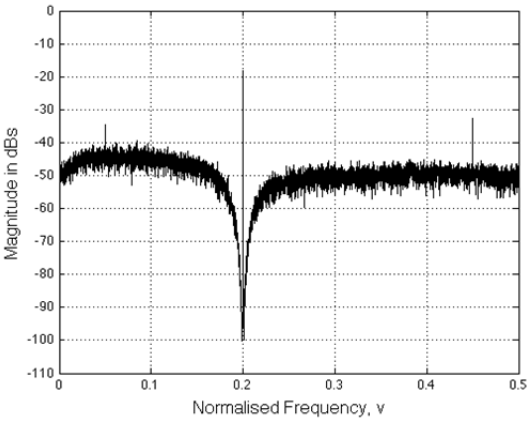
a) Butterworth, SP



b) Chebyshev, 2-Path



c) Inv. Chebyshev, 4-Path



d) Elliptical, 4-Path

Figure 5. Output spectrums of the FPGA implementations.

3. FPGA IMPLEMENTATION

The designed 4th-order SP, 2-Path and 4-Path D/A Σ–Δ modulators are implemented in VHDL and synthesized on the Xilinx® Spartan™-3 Development Kit. As explained in Section 2, fixed-point arithmetic is chosen and a 16-bit single sinusoidal input signal is applied to the system using look-up tables. Note that the 16-bit signal is composed of a 1-bit sign and 15-bits for the fractional component, hence any internal path with a bit number bigger than 16 has an integer part. In

Table 3 this arithmetic is symbolized as *sD.15-bit* where *s* represents the sign bit, *D* represents the decimal bits and the *15-bit* represents the fractional part of the number. In other words, the total bit number can be calculated as $s+D+15$. For instance: to represent a value of 1.6537, 15-bits for the fractional part, 1-bit for the decimal part and 1-bit for the sign are needed resulting in a 17-bit fixed point representation. The binary value is '01101001110101100' which equates to an integer number of 54190 that can easily be calculated by multiplying 1.6537 with 2^{15}.

The output data is taken via an RS232 connection and processed in the MATLAB environment including the decimation filtering. Figure 4 shows the block diagram of the designed set-up.

There are two universal clocks on Xilinx® Spartan™-3 Development Kit, 66 MHz and 100 MHz. In this study, it is preferred to clock the modulators at 66 MHz. This results in a clock frequency of 33 MHz and 16.5 MHz for the 2-Path and 4-Path modulators' individual paths respectively. Since a normalized input frequency of 0.2 is needed, a sinusoid with a frequency of 26.4 MHz is sampled at 66 MHz and sample values are restored in a look-up table.

The tonality behaviour of D/A Σ–Δ modulators will be discussed in Section 4. It should be pointed out that dithering will be used to alleviate the tonal behaviour of the designed Σ–Δ modulators.

A 16-bit Fibonacci Linear Feedback Shift Register (LFSR) is built for its relatively white output spectrum. The first 14-bits are taken as output to lower the applied noise power. As depicted in Figure 6, -70 dB of white noise is obtained for normalized frequencies above 0.055.

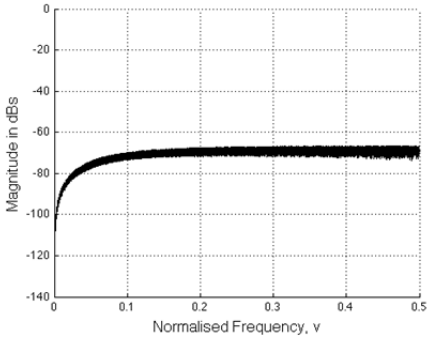
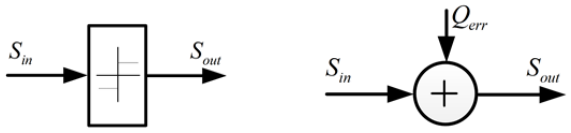


Figure 6. Output spectrum of the Fibonacci LFSR.

In Figure 5, the output spectrums of the implemented Σ–Δ modulators are illustrated for different filter types. The occurrence of the tones observed for the elliptical based DDSM topology will be explained in Section 4.

The allocated FPGA sources are summarized in

Table 3. It should be pointed out that the number of slices given in



a) Quantization block diagram b) Linear model of the quantization

Figure 7. Additive White Noise Block Diagram.

Table **3** includes the number of flip-flops and latches used. Since delayers are chosen as the main building blocks to confine the internal path number within the minimum range, the adding blocks of the integrators are already eliminated.

The number of multipliers can be easily calculated for a TI topology using its corresponding SP prototype as $m \times N$, where m is the number of multipliers used in the SP prototype and N is the path number of the TI topology. However, all other components are realized using the slices and LUTs of the FPGA, including the upsamplers, downsamplers, adders, input LUT, reset circuitry and RS232 circuitry. Therefore, it is hard to estimate number of slices and LUTs used for a TI topology using its corresponding SP prototype.

4. TONALITY

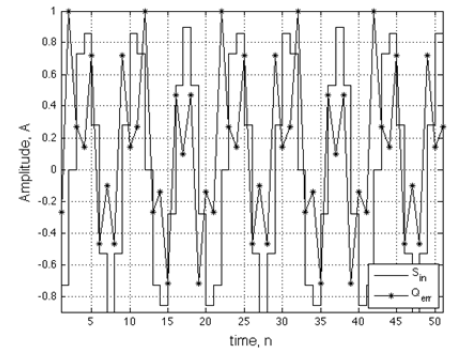
The quantization of a sinusoid creates tones, whose amplitudes and frequencies can be mathematically determined. This applies to variable-centre frequency Σ–Δ modulators when excited by sinusoidal inputs. Extra care must be taken especially in the case of digital Σ–Δ modulators as these tones are caused both by the quantizer and finite wordlengths. These tones can be modelled using the sawtooth quantization error model [20]. However, since the quantization error is highly input signal dependent, the actual power of these tones may become extremely difficult to predict.

The first step of the sawtooth quantization noise model is to use the additive noise model. Figure 7 depicts the additive noise approximation of the quantizer [4].

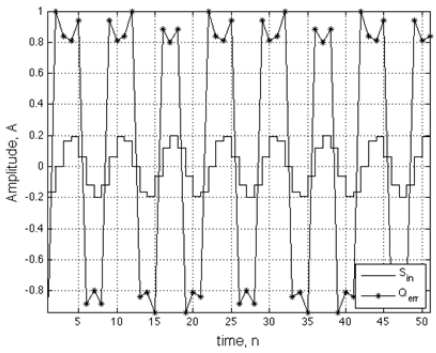
The second step is to define this additive quantization error as an input signal dependent sawtooth function. To have better understanding of this theory, the simulated quantization error of a sinusoid for a 1-bit quantizer is shown in Figure 8. As seen, the quantization error of a sinusoid is a sawtooth signal with a frequency of $2f_c$ multiplied by a sinusoidal signal with a frequency of f_c, where f_c is the input signal frequency.

Note that for an *m*-level quantizer, the frequency of the sawtooth signal will be $2mf_c$ as expressed in (2), where Q is the quantization step size and A is the input amplitude. Also, ε_1 and ε_2 are the input amplitude dependent errors that are assumed to have a white distribution. However, in this case they are assumed to be negligible and are approximated to zero.

$$Q_{err} = \left(\frac{A}{2} - \varepsilon_1\right) sawt(n) \frac{Q}{\left(\frac{A}{2} - \varepsilon_2\right)} cos(2\pi f_c n) \quad (2)$$



a) $A = 0.9$



b) $A = 0.2$

Figure 8. Quantization error of a sinosoid for a 1-bit quantizer.

$$sawt(n) = \frac{2}{\pi}\sum_{k=1}^{\infty}(-1)^{k+1}\frac{sin(2\pi(2mf_c)n)}{k} \quad (3)$$

$$Q_{err} = \frac{2Q}{\pi} cos(2\pi f_c n) \sum_{k=1}^{\infty}(-1)^{k+1}\frac{sin(2\pi(2mf_c)n)}{k} \quad (4)$$

An ideal sawtooth wave function can be written as the sum of sinusoids with integer multiples of the fundamental frequency which is $2mf_c$ in this case (3). Hence, the sawtooth signal is multiplied by a cosine (4), the process of calculating the quantization error signal is similar to double-sided AM modulation.

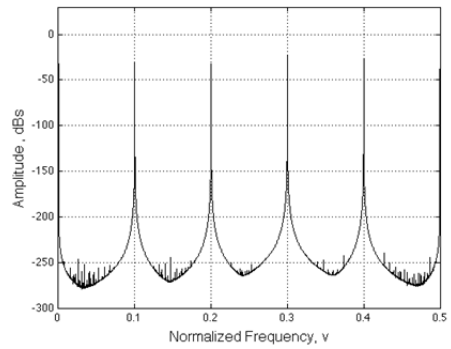
It is well known that, if a sinusoidal signal with a frequency of f_1 is AM-modulated by another sinusoid with a frequency of f_2, the resulting tones will be at $(f_2 - f_1)$, f_2, $(f_2 + f_1)$. Since $f_1 = 2mf_c, 4mf_c, 6mf_c$ ... and $f_2 = f_c$, the resulting tones will be at $[\ldots(6m-1)f_c, (4m-1)f_c, (2m-1)f_c, (2m)f_c, (2m+1)f_c, (4m+1)f_c, (6m+1)f_c \ldots]$.

In order to explain it clearly, an example of the sawtooth quantization error model is given. It is assumed that a sinusoid with a normalized frequency of 0.15 (5) is applied to a 1-bit quantizer. This results in a quantization error of (6). For the ideal case, the quantization error is not input amplitude dependent.

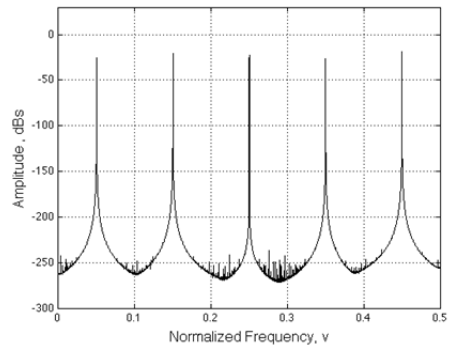
$$S_{in} = A\, cos(2\pi\ 0.15n) \quad (5)$$

$$Q_{err} = \frac{2Q}{\pi} cos(2\pi\ 0.15n) \sum_{k=1}^{\infty}(-1)^{k+1}\frac{sin(2\pi\ 0.3n)}{k} \quad (6)$$

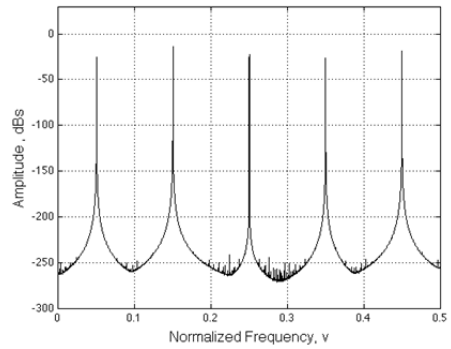
Figure 9a shows the spectrum of the sawtooth with a fundamental frequency of 0.3 and Figure 9b depicts its AM



a) Sawtooth signal's harmonics



b) The resulting quantization error



c) Output of the quantizer

Figure 9. 1-bit quantizer under sinusoidal excitation.

modulation by a cosine with a frequency of 0.15. It should be remembered that tones beyond 0.5 are folded back and added to the already existing tones within the range of [0, 0.5] as their frequency is mapped to $f_N - \lfloor f_N + 0.5 \rfloor$. The operator $\lfloor x \rfloor$ represents the largest integer less than or equal to $\lfloor x \rfloor$ and f_N is the normalized frequency of the signal.

Finally, Figure 9c shows the output of the quantizer that is equal to the sum of the quantization error shown in (6) and the input signal given in (5). The only difference between Figure 9b and Figure 9c is the amplitude increase of the input frequency tone.

The sawtooth quantization error model can be summed up as follows:

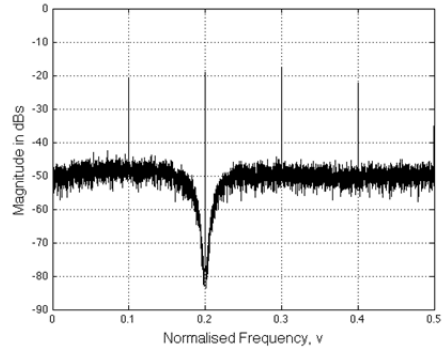
1. The expected high tones in a Σ–Δ modulator resulting from the quantization of a sinusoid, not the limit cycle tones, can be calculated in terms of their frequency and amplitude.

2. These tones can be whitened by dithering, especially for multi-level quantizers due to their smaller Q resulting in lower amplitude tones when compared to the 1-bit quantizer. However, at some particular frequencies such as 0.25, 0.125, 0.375...etc dithering may not work sufficiently for all the tones. This is because harmonics of the sawtooth signal are mapped and added to each other at the same frequencies resulting in higher amplitude tones. On the other hand, variable centre frequency Σ–Δ modulators exhibit more but smaller amplitude tones that can be reduced sufficiently when dithering is employed. This makes the proposed topologies more attractive compared with their mid-band counterparts.

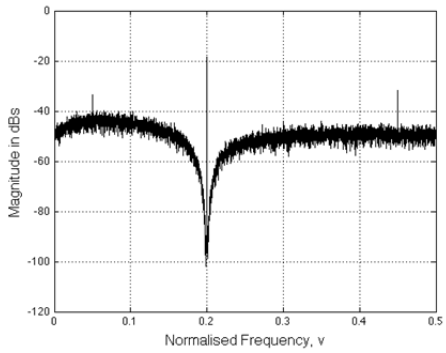
3. Input frequencies, whose values are irrational, result in a higher number of tones since the harmonics of the sawtooth signal are not folded back to the same frequencies. Therefore, the resulting tones are expected to have lower amplitudes. On the other hand, it is apparent from (3) that the amplitude series of the sawtooth harmonics is divergent. Besides, irrational frequency tones are mapped close to each other and may not be sufficiently suppressed within the signal-band, thus resulting in significant SNR reduction.

4. The white noise approximation still applies as can easily be seen from the noise floor of Figure 9. This noise floor is caused by ε_1 and ε_2 errors. Needless to say that in a Σ–Δ modulator, both the quantization noise and the tones will be accumulated and shaped.

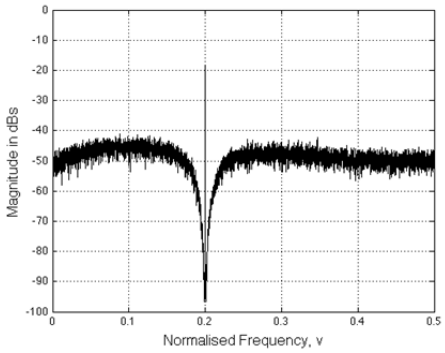
5. As already explained, both the quantizer and the finite wordlengths of the D/A Σ–Δ modulators cause the sawtooth signal tones. Interestingly, the tones created by the finite wordlength effects are whitened during the accumulation process of the loop-filter since their amplitudes are very small for a 16-bit or higher wordlength quantization. However, for shorter wordlengths, they are not whitened sufficiently well and are subsequently processed by the 1-bit quantizer. Since these resulting tones' amplitudes are not input amplitude dependent, these finite wordlength based tones create extra tonality, which may result in Σ–Δ modulator instability. Moreover, using EF modulator topologies, as already explained, helps to diminish the finite wordlength based tones since the already whitened/accumulated feedback signal is extracted from the finite wordlength input sinusoid.



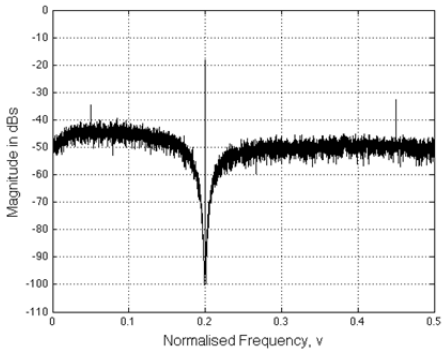
a) Butterworth, 2-Path



b) Butterworth, 4-Path



c) Elliptical, 2-Path



d) Elliptical, 4-Path

Figure 10 Output spectrums of the FPGA implementation.

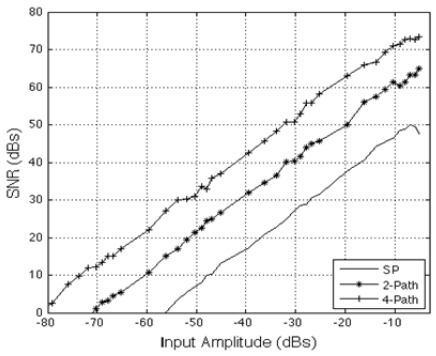
4.1. Quantization Tones in TI Σ–Δ modulators

The sawtooth quantization error is caused both by the quantizer and the finite wordlengths of the DDSMs as mentioned earlier. Hence, both SP and TI DDSMs are excited by a quantized sinusoid. The quantization tones are also given as input to these modulators and may affect the stability and the SNRs especially for the TI DDSMs.

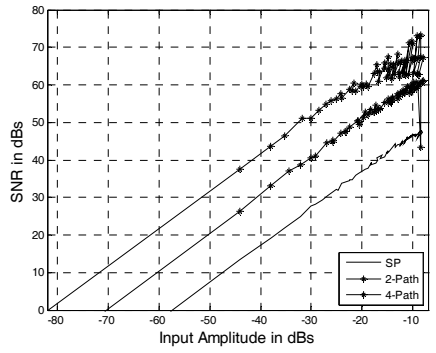
The TI concept depends on the idea of the perfect cancellation of the signal images created by the downsampling process [5-7]. However, the quantization tones' images and the input signal images produced by downsampling cannot be cancelled perfectly due to the finite wordlength of the internal paths. This situation can be analogous to the path mismatches that characterize discrete-time A/D Σ–Δ modulators [20-23].

The input normalized signal frequency is 0.2 thus causing quantization tones at frequencies: 0.1, 0.3, 0.4 and 0.5. Figure 10 depicts some of the FPGA implementation output spectrums of the designed DDSMs. It is apparent that the power of the quantization error tones depends on the topology coefficients as well as the path number of the DDSM. Unfortunately, Σ–Δ modulators are non-linear therefore making it hard to mathematically model the effects of the coefficients and the path number on the amplitude of these tones.

Consequently, the tones seen in Figure 10a are quantization tones whilst the tones seen at random frequencies in Figure 10b, Figure 10c and Figure 10d are caused by the limit cycle oscillations.

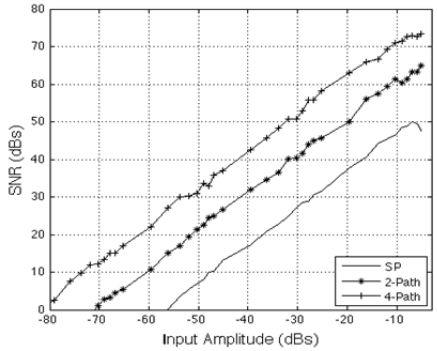


a) Butterworth, behavioural model

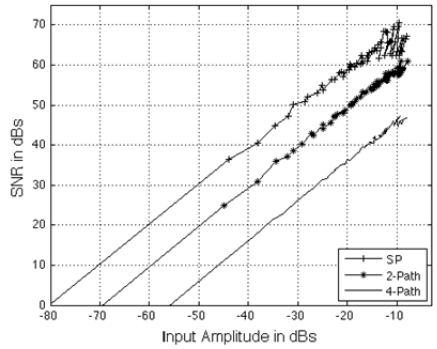


b) Butterworth, FPGA implementation

Figure 11. SNR Plots for the Butterworth Filter.

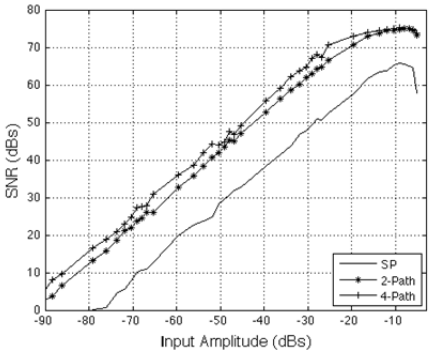


a) Chebyshev, behavioural model

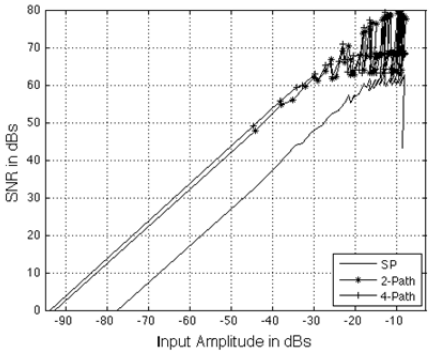


b) Chebyshev, FPGA implementation

Figure 12. SNR Plots for the Chebyshev filter.



a) Inv. Chebyshev, behavioural model



b) Inv. Chebyshev, FPGA implementation

Figure 13. SNR plots for the Inv. Chebyshev filter.

5. SIMULATIONS AND EXPERIMENTAL RESULTS

The SNR curves of the SP, 2-Path and 4-Path DDSMs for an OSR of 64 are shown in Figure **11**-Figure **14** both for the behavioural-level models and FPGA implementations. The effective OSR of the SP is 64, whilst it is 128 for the 2-Path and 256 for the 4-Path topologies.

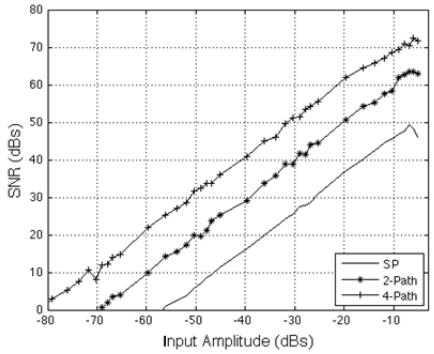
Extensive behavioural-level simulations for various centre frequencies and bandwidths demonstrate that the Inverse Chebyshev and Elliptical filters provide superior SNR values compared to their Butterworth and Chebyshev counterparts. This is attributed to the evenly distributed zeros and steeper transition bands of the former two which result in lower quantiztion noise power over the signal bandwidth. Furthermore, Inverse Chebyshev filters can be designed to have normalized bandwidths up to 0.001 (asuming Nyquist to be at 0.5) without causing the Σ–Δ modulator to become unstable.

On the other hand, the highest SNR difference occurs for the Chebyshev filter. This is due to the chosen design specifications and resulting coefficients of the loop-filter. Therfore it is intended to further extend the work for different frequencies and different design specifications in order to have a better understanding of this discrepancy. For the remaining filter types, an SNR decrement of 3-5 dB is observed when implemented on FPGA due to the circuit imperfections and clock jittering effects.

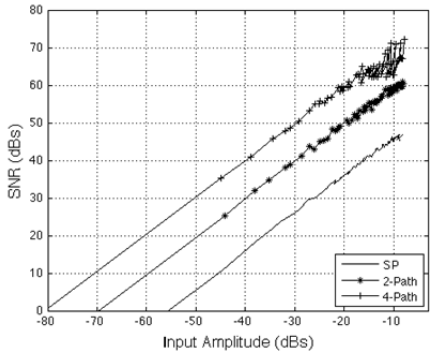
6. CONCLUSIONS

Novel variable centre frequency dual- and quadruple TI Σ–Δ modulators, which employ an assortment of filter types and topologies, were designed, modelled and analysed. The proposed TI Σ–Δ modulators are well suited for a wide range of applications as they offer designers and practitioners the flexibility of defining the centre-frequency, bandwidth as well as the pass-band and stop-band parameters. The topology complexity, SNRs, stability and tonality of the aforementioned multi-path topologies were evaluated and compared with each other and against their single-path counterparts.

The designed topologies were implemented and synthesized on Xilinx® Spartan™-3 Development Kit using fixed-point arithmetic. Circuit outputs were taken via RS232 connection provided on the FPGA board and evaluated using the MATLAB routines developed by the authors. These routines included the decimation process as well. The experiments undertaken by the authors further validated the design methodology presented in the paper. Furthermore, the implemented topology outputs also confirmed the proposed mathematical model of the quantization tones of these digital multi-path Σ–Δ modulators, when excited by sinusoidal input signals.



a) Inv. Elliptical, behavioural model



b) Elliptical, FPGA implementation

Figure 14, SNR Plots for the Inv. Elliptical filter.

REFERENCES

[1] Ostrovskyy, P.; Gustat, H.; Ortmanns, M.; Christoph Scheytt, J., "A 5-Gb/s 2.1–2.2-GHz Bandpass Δ-Σ Modulator for Switch-Mode Power Amplifier," *Microwave Theory and Techniques, IEEE Transactions on* , vol.60, no.8, pp.2524,2531, Aug. 2012.

[2] Heng-Yu Jian; Xu, Z.; Yi-Cheng Wu; Chang, M.-C.F., "A Fractional-N PLL for Multiband (0.8–6 GHz) Communications Using Binary-Weighted D/A Differentiator and Offset-Frequency Δ-Σ Modulator," *Solid-State Circuits, IEEE Journal of* , vol.45, no.4, pp.768,780, April 2010.

[3] Candy, J., Temes, G., *"Oversampling Delta-Sigma Data Convert- ers:Theory, Design, and Simulation"*. "Wiley-IEEE Press", 1992.

[4] Norsworthy, S., Schreier, R., Temes, G., *"Delta-Sigma Data Convert- ers:Theory, Design, and Simulation"*. "Wiley-IEEE Press", 1997.

[5] A. Eshraghi and T. Fiez, "A comparative analysis of parallel delta- sigma adc architectures," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 51, no. 3, pp. 450 – 458, March 2004.

[6] M. Kozak and I. Kale, "Novel topologies for time-interleaved delta- sigma modulators," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 47, no. 7, pp. 639 –654, July 2000.

[7] R. Khoini-Poorfard, L. Lim, and D. Johns, "Time-interleaved oversampling a/d converters: theory and practice," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 44, no. 8, pp. 634 –645, Aug 1997.

[8] X. Wu, V. A. Chouliaras, J. L. Nunez, and R. M. Goodall, "A novel control system processor and its VLSI implementation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 3, pp. 217–228, Mar. 2008.

[9] M. Kwon, J. Lee, and G. Han, "A time-interleaved recursive loop band-pass delta-sigma modulator for a digital if cdma receiver," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 52, no. 7, pp. 389 – 393, July 2005.

[10] Kizilkaya, I.K.; Al-Janabi, M.; Kale, I., "Design and evaluation of time-interleaved variable center-frequency sigma-delta modulators," Digital Signal Processing (DSP), 2013 18th International Conference on , vol., no., pp.1,6, 1-3 July 2013.

[11] Kizilkaya, I.K.; Janabi, M.-A.; Kalei, I., "Novel Time-Interleaved variable-center frequency Δ-Σ modulators-design, analysis and critical evaluation," Instrumentation and Measurement Technology Conference (I2MTC), 2013 IEEE International , vol., no., pp.480,483, 6-9 May 2013.

[12] Kizilkaya, I.K.; Al-Janabi, M.; Kale, I., *"Novel Time-Interleaved Variable Centre-Frequency, Single-Bit A/D and D/A Sigma-Delta Modulator Topologies,"* IMEKO, 2013 19th International Conference on , , vol., no., pp.599,604, July 2013.

[13] I. Galton, "One-bit dithering in delta-sigma modulator-based D/A conversion," in *Proc. IEEE Int. Symp, Circuits Syst.,* 1993, pp. 1310–1313.

[14] K. Hosseini and M. P. Kennedy, "Maximum sequence length MASH digital delta-sigma modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 54, no. 12, pp. 2628–2638, Dec. 2007.

[15] Karema, T.; Ritoniemi, T.; Tenhunen, H., "Intermodulation in sigma-delta D/A converters," *Circuits and Systems, 1991., IEEE International Sympoisum on* , vol., no., pp.1625,1628 vol.3, 11-14 Jun 1991.

[16] Fitzgibbon, B.; Kennedy, M.P.; Maloberti, F., "Hardware Reduction in Digital Delta-Sigma Modulators via Bus-Splitting and Error Masking—Part II: Non-Constant Input," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.59, no.9, pp.1980,1991, Sept. 2012.

[17] Fitzgibbon, B.; Kennedy, M.P.; Maloberti, F., "Hardware Reduction in Digital Delta-Sigma Modulators Via Bus-Splitting and Error Masking—Part I: Constant Input,"*Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.58, no.9, pp.2137,2148, Sept. 2011.

[18] Chen, A.J.; Yong-Ping Xu, "Multibit Delta-Sigma Modulator With Noise-Shaping Dynamic Element Matching," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.56, no.6, pp.1125,1133, June 2009.

[19] Bornoosh, B.; Afzali-Kusha, A.; Dehghani, R.; Mehrara, M.; Atarodi, S.M.; Nourani, M., "Reduced complexity 1-bit high-order digital delta-sigma modulator for low-voltage fractional-N frequency synthesis applications," *Circuits, Devices and Systems, IEE Proceedings* - , vol.152, no.5, pp.471,477, 7 Oct. 2005.

[20] Abuelma'atti, M.T., "Spectrum of a nonlinearly quantised equal-amplitude dual-tone signal," *Circuits, Devices and Systems, IEE Proceedings* - , vol.148, no.1, pp.11,18, Feb 2001.

[21] T. Salo, S. Lindfors, and K. Halonen, "A double-sampling sc-resonator for low voltage bandpass delta; sigma;-modulators," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 49, no. 12, pp. 737 – 747, Dec 2002.

[22] Hwi-Ming Wang; Tai-Haur Kuo, "The design of high-order bandpass sigma-delta modulators using low-spread single-stage structure," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.51, no.4, pp.202,208, April 2004.

[23] Reekmans, S.; Rombouts, P.; Weyten, L., "Mismatch Insensitive Double-Sampling Quadrature Bandpass Δ-Σ Modulation," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.54, no.12, pp.2599,2607, Dec. 2007.