Low Complexity All-Pass Based Polyphase Decimation Filters for ECG Monitoring

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***Abstract*—This paper presents a low complexity high efficiency decimation filter which can be employed in EletroCardioGram (ECG) acquisition systems. The decimation filter with a decimation ratio of 128 works along with a third order sigma delta modulator. It is designed in four stages to reduce cost and power consumption. The work reported here provides an efficient approach for the decimation process for high resolution biomedical data conversion applications by employing low complexity two-path allpass based decimation filters. The performance of the proposed decimation chain was validated by using the MIT-BIH arrhythmia database and comparative simulations were conducted with the state of the art.**

Keywords—decimation filter; polyphase filter; halfband allpass filter; ECG signal; health monitoring; low power; low complexity.

I. INTRODUCTION

One of the main research interests in the medical engineering field is the acquisition and processing of the ElectroCardioGram (ECG) signals for long term real-time health monitoring. ECG signals are the electrical representation of contractile activity of the heart that have very low signal amplitude ranging from 100 μV to 4 mV and low frequency bandwidth spanning between 0.1 Hz and 250 Hz, making them susceptible to noise [1]. The Sigma-Delta (ΣΔ) oversampling Analog-to-Digital Converters (ADCs) are commonly used for biosignal acquisition systems which are suitable for low-power and low-voltage applications and can easily achieve 12-16 bits or higher resolution with simple hardware architecture [2]. The modulated pulse signal from the ΣΔ ADC is fed into a decimator being composed of cascaded Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filters and downsamplers which plays an essential role in de-modulating the signal and attenuating the out-of-band quantization noise. The decimation process reduces the number of samples to be processed, reducing the hardware complexity and power consumption.

Several decimators have been studied in the literature for ECG monitoring that employ Canonical Signed Digit (CSD) representation for their decimation filter coefficients in order to reduce the hardware complexity and power consumption. In [3] a four stage decimator was described and implemented comprising a fourth order 'comb filter', two Half- Band (HB) FIR filters, and a compensation filter which were implemented using a one multiplier FIR structure. In this work the filter coefficients were stored in a memory unit and a general purpose multiplier was used to perform the multiplications required for the filtering process. In [4], a three stage decimator without a compensation filter was presented. Similar to [3] a fourth order Cascade Integrator-Comb (CIC) assumed to be assumed the same as the so called 'comb' filter followed by two 22^{nd} order half-band filters was proposed. Studies in [1] and [5] both have presented a 3 stage decimation filter containing a CIC, and two half-band FIR filters, where [5] implemented its coefficients in CSD in order to reduce the hardware complexity. In addition to these, [6] presented a 4 stage decimator containing a 'comb filter', followed by a compensator and two FIR filters.

In all of these works cited in the previous paragraph, the decimation chain is built around higher order FIR or IIR filters, which in turn increase the number of multiplications required per output sample. On the other hand reducing the number of multipliers as in [3] only contributes towards low hardware complexity but because the number of multiplications stays the same, power dissipation savings is minimal. CSD only helps replace multiplications with a series of additions/subtractions avoiding the use of general purpose multiplier units. Therefore it is only an efficient implementation rather than a solution to avoid the need for higher order digital filters in the decimation stage for ECG monitoring.

This paper describes the design of a highly efficient decimation filter to be deployed in ECG signal acquisition systems using all-pass based polyphase IIR filters. These filters have shown great success in reducing the number of filter coefficients, and therefore reducing the number of multiplications as well as the additions within the filtering process in various applications [7]. The main objective of the work reported in this paper is to achieve low power consumption therefore; the proposed design consists of four stages being a Slink filter (also spuriously referred to as a CIC

filter [8]) and two all-pass based polyphase HB IIR filters with multiplier free structures and a compensation filter. These stages are described in detail in section 2. Section 3 presents the floating-point precision simulation results of the decimator together with a third-order single loop Σ−Δ modulator and the performance comparisons between the proposed decimator and the decimator provided in [6].

II. Specifications and Structure of the ADC and Decimation Filter Simulation Models

The block diagram of the decimation filter chain is shown in Fig. 1. As mentioned before, the proposed decimation filter consists of four stages, which are the fourth order slink, two tenth order all-pass based HB IIR and compensation filters with a decimation ratio of 128. Performing decimation in multiple stages balances the trade-off between the hardware complexity and computational efficiency [9]. In the following subsections more details are provided on the simulation models of the Σ-Δ ADC and decimation filtering stages.

A. The Σ−Δ ADC Modulator Used

In this work, a single loop sigma-delta modulator is employed together with the proposed digital decimation filter in order to provide the appropriate single-bit input to the decimator. In most ECG signal applications, the desired dynamic range can be up to 60 dB and the minimum required resolution is 8-bits [2]. Thus to meet these requirements a 3rd order single-loop Σ-Δ ADC with l-bit quantization and an oversampling ratio (OSR) of 128 is modeled. The system level simulation is performed in the MATLAB environment.

B. First Stage Decimation – Slink Decimator

Considering the high sampling rate at the first stage of the decimation filter, a slink filter is preferred with a large decimation ratio and a low circuit complexity. It has the advantage of being multiplier free and the shifted downsampler in between the accumulators and differencers enable the filter to operate at rates lower than the input rate. The order of the slink filter is determined with respect to the order of the ΣΔ modulator used. The decimator gain should roll-off faster than the ΣΔ modulation noise rises, which necessitates the use of $(N+1)^{th}$ order slink filter following an N^{th} order modulator [8]. A higher order filter will cause additional droop in the in-band magnitude response. Therefore, a 4th order slink filter with decimation factor of 32 was designed. The z-domain transfer function of the aforementioned filter is given in (1) and the corresponding magnitude response is given in Fig. 4 (a) [8].

$$H_{slink}(z) = \frac{1}{32^4}\left(\frac{1-z^{-32}}{1-z^{-1}}\right)^4 \quad (1)$$

C. Second and Third Stage Decimation – Polyphase All-pass Based HB IIR Decimator

The next two stages of the decimation filter are the polyphase all-pass based HB IIR filters where each stage decimates the signal by two in order to return back to

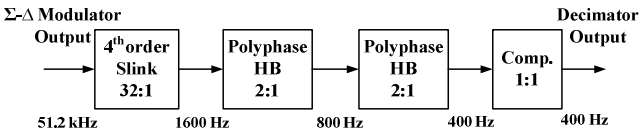


Fig. 1. Block diagram of the decimation filter.

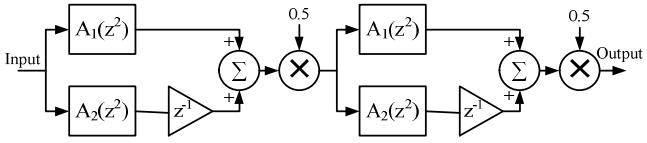


Fig. 2. Double Polyphase HB Lowpass filter structure

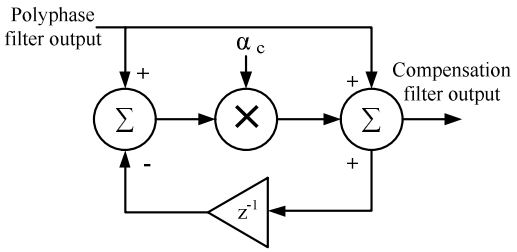


Fig. 3. Structure of the compensation filter.

baseband. These filters are very high fidelity minimum-phase lowpass filters which introduce only minimal group delays with micro-dB passband ripple and deep stopband attenuation in the region of signal activity. The polyphase IIR decimators are implemented as a two-path structure by using two HB allpass filters, which are then cascaded as shown in Fig. 2, in order to get higher level of stopband attenuation, without deteriorating the passband characteristics.

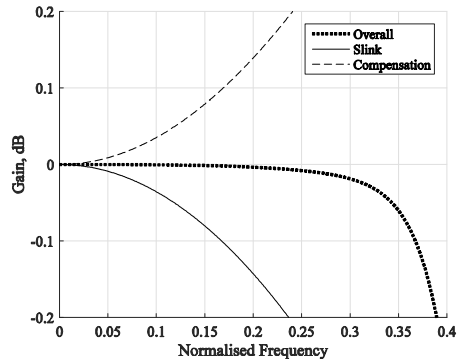
The z-domain transfer function for HB all-pass filters are given by (2), where the coefficients for both top and bottom branches are powers-of-two [10].

$$A_i(z^2) = \frac{\alpha_i + z^{-2}}{1 + \alpha_i z^{-2}} \quad (2)$$

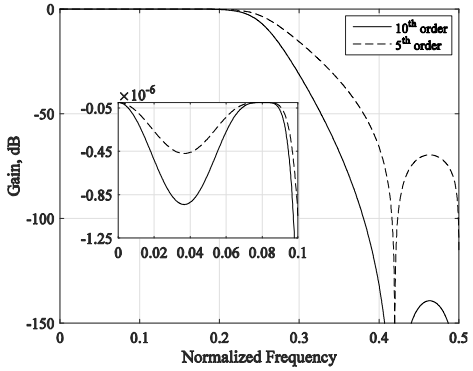
Where $i = 1,2$ .According to the system requirements the second and third stage of decimation are implemented as 10th order double polyphase lowpass HB IIR filters with two coefficients. Each stage provides a passband ripple of $1\ \mu dB$ and stopband attenuation of $140\ dB$. The magnitude responses of the 5th (single) and 10th (double) order polyphase IIRs are shown in Fig. 4 (b).

D. Compensation Filter

The passband roll-off caused by the slink filter distorts the passband characteristics which necessitates a roll-up filter. Thus, the final stage of the decimation process is the compensation filter with an inverse slink response in the band of interest from DC to 200 Hz. The structure of the compensation filter has a similar structure to an allpass filter and requires only one coefficient, i.e. α_c as shown in Fig. 3 [10, 11].



(a)



(b)

Fig. 4. Magnitude response of (a) 4th order slink and compensation filter as well as the achieved overall response and (b) the 5th and 10th order polyphase HB IIR filter.

III. Simulation Results

In order to validate and evaluate the proposed decimation filter's performance an overall behavioural floating point model of the decimator shown in Fig. 1 as well as the aforementioned Σ-Δ modulator were implemented using MATLAB. The magnitude response of the proposed decimator at the input, third decimation stage and output are shown in Fig. 5 (a), (b) and (c) respectively. For evaluation purposes the proposed decimator was tested using the ECG data records from the MIT-BIH database which were digitized at a sampling frequency of 360 Hz via a unipolar ADC with 11-bits resolution [12, 13]. According to the American Heart Association recommendations the minimum bandwidth for ECG recordings is 150 Hz [14]. Considering these recommendations, the input data was resampled with an oversampling ratio of 128 and was fed into the 1-bit single loop 3rd order Σ-Δ modulator.

The performance of the proposed decimator is also compared with the decimation filter chain designed in [6]. The specifications for both filters are given in Table I. For comparative simulations, floating point models of the decimation filter was implemented using MATLAB. The 3rd and 4th stages of this decimator were implemented using the symmetric HB FIR filter structure where the number of the distinct coefficients for each filter can be calculated via (5).

TABLE I. Specifications Of Each Stage Of The Decimation Chain

Parameters	Slink Filter	HB Filter I		HB Filter II		Compensation Filter	
		This Work	[6]	This Work	[6]	This Work	[6]
Filter order	4	10	14	10	74	1	278
Sampling Frequency (Hz)	51200	1600	1600	800	800	400	1600
Decimation Rate	32	2	2	2	2	1	1
Passband edge (Hz)	N.A	200	180	200	180	N.A	180
Stopband edge (Hz)	N.A	323	620	323	220	N.A	200
Passband ripple (dB)	N.A	$< 1\times 10^{-6}$	< 0.01	$< 1\times 10^{-6}$	< 0.01	N.A	< 0.01
Stopband attenuation (dB)	N.A	> 140	≥ 60	> 140	≥ 60	N.A	≥ 60
Output Sampling Frequency (Hz)	1600	800	800	400	400	400	1600

$$M = \frac{T+1}{2} \quad \text{and} \quad N = \frac{M}{2} + 1 \tag{5}$$

where T is the number of taps in an FIR filter, and N is the number of non-zero coefficients of an HB FIR filter. The HB FIR filters given in [6] require 5 and 20 distinct coefficients respectively. In addition, the number of multiplications and additions per input sample for 3rd stage FIR are 5 and 8 and for 4th stage FIR are 20 and 38 respectively.

However, our proposed 10th order polyphase HB all-pass based IIR filters require only two distinct coefficients. The number of additions per input sample for each decimation stage is 10. For these filter multiplication is not required since, the coefficients of the all-pass sections are powers-of-two which can be implemented by using simple hard wired shift-and-add method without using any multipliers thus reducing the cost and power consumption. The simulation results of the two aforementioned decimators when the MIT-BIH *data 105* is fed into the Σ-Δ modulator are shown in Fig. 6 and 7. Fig. 6 (a) illustrates the first ten seconds of the MIT-BIH *data set 105*, where (b) and (c) show the data at the output of the two decimation chains. On the other hand, Fig. 7 (a) and (b) show the magnitude error between *data set 105* and output of the proposed decimation filter and decimation filter given in [6]. The magnitude error introduced by our proposed decimator is calculated as 0.48% where this percentage rises to 0.83% with the decimator given in [6]. As mentioned in the previous paragraph the number of additions and multiplications required by [6] is much higher than our decimator. Therefore, a better performance with a lower complexity and power consumption compared to what is reported in [6] is achieved in this work.

IV. Conclusion

A decimation filter with a highly effective filtering performance with a low hardware complexity that can be deployed in wearable ECG acquisition systems is proposed.

The proposed decimator satisfies the requirements for data processing of 180 Hz baseband ECG signal with stopband attenuation sufficient enough to attenuate the out-of-band high

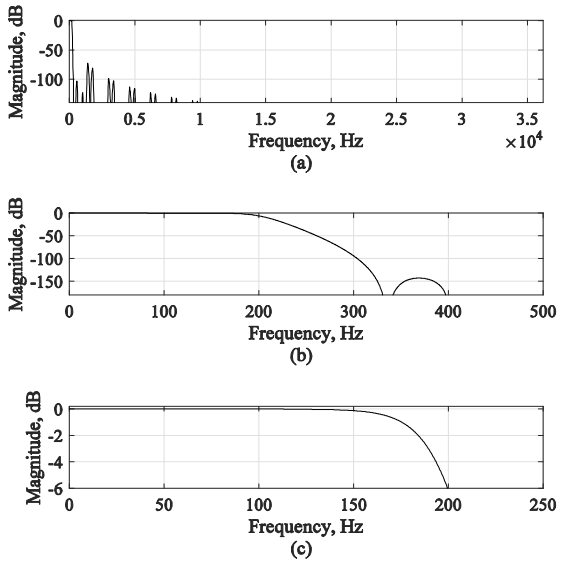


Fig. 5. Magnitude response of the proposed decimator, (a) full band, (b) at the third stage of decimation and (c) at the output.

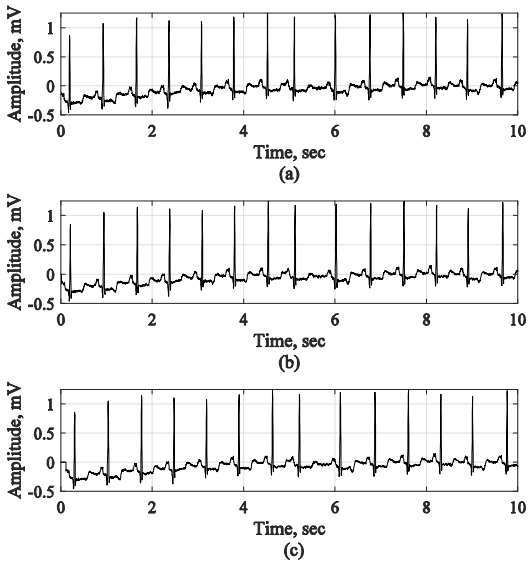


Fig. 6 10 seconds of ECG signals, (a) MIT-BIH data, (b) output of the proposed decimation chain, and (c) output of the decimation chain given in [6].

frequency noise while demodulating the Σ-Δ modulated signal. Moreover, the proposed decimator is cost effective for hardware implementation due to the filter structures used that do not require any multipliers.

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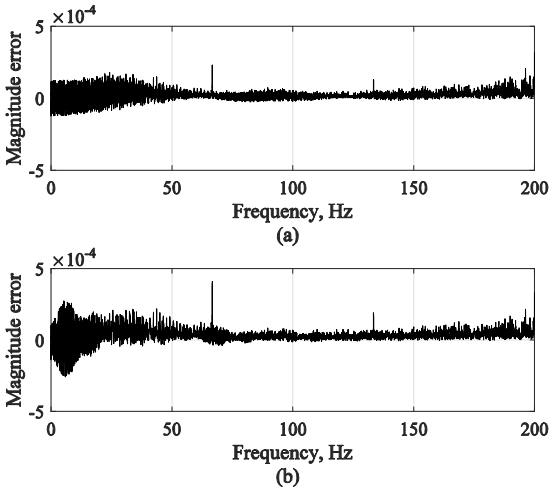

Fig. 7 Magnitude error between the MIT-BIH data and the output from the (a) proposed decimator and (b) decimator given in [6].

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