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Faults Affecting Energy Harvesting Circuits of Self-Powered Wireless Sensors and Their Possible Concurrent Detection

M. Omaña, D. Rossi, D. Giaffreda, R. Specchia, C. Metra, M. Marzencki, B. Kaminska

Abstract— *We analyze the effects of faults affecting an energy harvesting circuit providing power to a wireless biomedical multisensor node. We show that such faults may prevent the energy harvesting circuit from producing the power supply voltage level required by the multisensor node. Then, we propose a low cost (in terms of power consumption and area overhead) additional circuit monitoring the voltage level produced by the energy harvesting circuit continuously, and concurrently with the normal operation of the device. Such a monitor gives an error indication if the generated voltage falls below the minimum value required by the sensor node to operate correctly, thus allowing the activation of proper recovery actions to guarantee system fault tolerance. The proposed monitor is self-checking with respect to the internal faults that can occur during its in field operation, thus providing an error signal when affected by faults itself.*

Index Terms—Energy Harvesting, High Reliability, Fault Tolerance, Self-Powered Sensors.

1 Introduction

Wireless sensing systems are gaining increasing interest, and their employment opens new possibilities in large scale, easy and low cost data capture. They are used for environmental and habitat monitoring, as well as for health surveillance [1, 2]. The main challenge in the use of such systems is associated with their power supply, still mainly provided by batteries. Due to the often required small size and remote deployment of the wireless sensor, any servicing linked with battery replacement is impractical. Therefore, systems using ambient energy as additional energy source have recently gained a considerable interest. They employ a circuit that harvests energy from the environment in which they are embedded to obtain the required energy.

Systems exploiting Energy Harvesting (EH) would also feature higher reliability than those using a fixed battery. In fact, they are less likely to suffer from common problems of depleted energy supply, and therefore limited lifetime. This is of great importance in case of powering biomedical wearable sensors monitoring critical human vital parameters (e.g., breathing, heart activity, etc.). For such applications, mechanical vibrations are a promising source of energy, due to their relatively high energy density and widespread existence [3].

Although energy harvesting circuits (EHCs) could in principle be more reliable than fixed batteries, they are generally composed of many components (e.g., diodes, switching transistors, capacitors, inductors, etc.) that may fail during in field operation, due to material degradation, electromagnetic interference, or other effects [4-6].

Up to now, multiple architectures of mechanical EH systems have been proposed [3, 7, 8]. Nevertheless, to our knowledge, none of them has yet considered the effects of faults possibly affecting its components, but for the preliminary analysis presented in [9]. Such an analysis has been performed considering an EHC implemented with discrete components and accounting for a reduced set of faults possibly affecting such components.

Based on these considerations, in this paper we analyze in details the effects of faults affecting an integrated circuit performing energy harvesting from mechanical vibrations, and powering a wireless

- *M. Omaña, D. Rossi, D. Giaffreda and C. Metra are with the University of Bologna, Bologna, Italy. E-mail: {martin.omana; d.rossi; daniele.giaffreda2; cecilia,metra}@unibo.it.*
- *R. Specchia is with the University of Bologna, Bologna, Italy. E-mail: Roberto.Specchia@gidi.it*
- *M. Marzencki and B. Kaminska are with the Simon Fraser University, Vancouver, Canada. E-mail: {mjm; kaminska}@sfu.ca.*

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biomedical multisensor node. We assume that the EHC is implemented using the same CMOS technology as the multisensor node, and we analyze the effects of all possible faults affecting the EHC. We show that they may make the EHC fail to produce the required supply voltage level to the sensor node, with consequent dramatic impact on reliability.

To cope with this problem, we propose a low cost (in terms of area overhead and power consumption) circuit, whose electrical structure is based on the monitor that we recently introduced [9]. Its purpose is to monitor continuously, and concurrently with the sensor operation, the correctness of the power supply voltage level provided by the EHC. When an incorrect voltage level is detected, an error message is generated, that can be used to activate a proper self-healing (or recovery) mechanism to guarantee that the required level of energy is provided to the multisensor node. For example, the power supply can be automatically switched to a small, rechargeable battery, till repair, or replacement, of the faulty EHC. Our circuit is also self-checking with respect to its possible internal faults, thus providing an output error message also in case of faults affecting itself during in field operation.

The paper is organized as follows. In Section 2, we describe the considered EHC. In Section 3, we analyze the effects of faults and parametric variations affecting the EHC components. In Section 4, we propose a low cost circuit to monitor concurrently the power supply voltage provided by the EHC. Section 5 reports some of the results of the electrical simulations performed to verify the correct operation of our monitor. In Section 6, we verify the self checking ability of our circuit with respect to its possible internal faults, while in Section 7, we evaluate its costs. Finally, we give conclusive remarks in Section 8.

2. Case Study: Self-Powered Wearable Multisensor

As a case study, we consider the wireless biomedical multisensor node described in [10]. The node features three different operating modes: i) the stand-by mode, in which it consumes approximately $3\mu W$; ii) the data acquisition (DA) mode, in which a power consumption of less than 1mW is reported; iii) the radio transmission (TX) mode, during which the power consumption reaches a value of 10mW [10]. The node is in the DA mode most of the time, with short, periodic TX phases.

The considered multisensor node is self-powered by both an EHC exploiting human vibrations and a rechargeable battery. The sensor is normally powered by the EHC, whose produced power supply voltage is monitored by our monitoring circuit. When our monitor detects an incorrect voltage level, it triggers an error message that is employed to switch the sensor power supply to the rechargeable battery till repair, or replacement, of the faulty EHC. This self-healing technique allows to guarantee that the required power supply is provided to the sensor, despite incorrect voltage levels produced by the EHC due to faults affecting itself.

The EHC is shown in Fig. 1. It employs a piezoelectric generator to convert the kinetic energy generated from human vibrations into electrical energy [8]. Since the piezoelectric generator produces an AC voltage (V_{piezo}), this needs to be rectified in order to be used for powering the multisensor node, here represented as an equivalent resistance *Rload*. Particularly, the AC voltage V_{piezo} is first rectified to a DC voltage by a full-wave AC/DC rectifier. Then the produced DC voltage is regulated to the desired value by a step-down DC/DC converter (Fig. 1).

The full-wave AC/DC rectifier consists of a diode bridge (D1-D4) and a storage capacitor (C_{stor}) that converts the AC voltage V_{piezo} into the DC voltage V_1, which is maintained at the terminals of C_{stor}. The AC/DC converter includes also an inductor L2 in series with a Synchronized Switch Harvesting on Inductor (SSHI) block [11], connected between the nodes $V_{in}+$ and $V_{in}-$. The SSHI block increases the voltage between nodes $V_{in}+$ and $V_{in}-$, thus reducing the energy loss across the four diodes of the AC/DC rectifier (D1-D4), and consequently increasing the overall efficiency of the EHC [11].

The DC voltage at V_1 is regulated to a lower value (V_{out}) by the step-down DC/DC converter composed of a control circuit, a transistor M1, a capacitor C_{out} and an in-

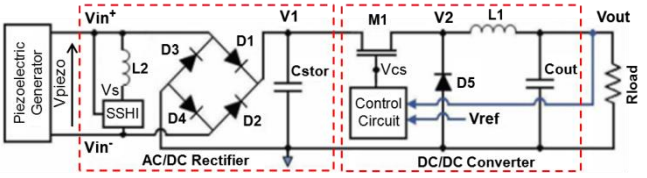

Fig. 1. Considered EHC.

ductor L1 (Fig. 1). The *Control Circuit* generates a periodic control signal (V_{CS}) that turns M1 on and off with a fixed frequency f_{CS}. This circuit compares the output voltage V_{out} with a reference voltage (V_{ref}) and, based on such comparison result, modifies the duty-cycle of signal V_{CS}, in order to make V_{out} equal to V_{ref}. A typical range of f_{CS} is 1kHz - tenths of kHz. As for V_{out}, it should be kept in the range [1.5V–2.1V] to guarantee the correct operation of the considered biomedical multisensor node [10, 12, 13].

The EHC in Fig. 1 has been implemented using the same 180nm standard CMOS technology as the considered multisensor node, and with discrete capacitors and inductors. In particular, we have implemented all diodes (D1-D5) by MOS transistors with shorted drain – gate terminals, while we have considered C_{stor}=180μF, C_{out}=500μF and L1=22mH. Our implementation guarantees a nominal V_{out} value of 2.1V, independently of the power consumed by the multisensor node.

As for the reference V_{ref}, it has been obtained by means of a circuit of the kind in [14, 15], using a stable Zener diode with a breakdown voltage equal to 2.1V, which is the maximum value in the voltage range [1.5V - 2.1V] required for the sensor correct operation. Therefore, since the minimum value in the required voltage range is 1.5V, there is a margin of 30% variation in the Zener diode breakdown voltage before V_{ref} falls below 1.5V. As reported in [14, 15], stable Zener diodes guarantee a value of their breakdown voltage with 5%-10% variations with respect to the nominal value. This way, we can guarantee that V_{ref} will never fall below 1.5V. Moreover, we included a clamping circuit of the kind in [16] in the EHC to prevent V_{out} from rising above the maximal allowed value (2.1V). Therefore, an increase in the breakdown voltage of the Zener diode will not affect the EHC correct operation.

3. Faults Affecting the Energy Harvesting Circuit and their Effects

For our analysis, we have assumed that the EHC is exhaustively tested after fabrication, thus fault-free at the beginning of its operation, and with its capacitor C_{stor} properly charged. We have considered faults affecting the EHC in Fig.1 during in field operation, and we have evaluated their impact on the provided V_{out}. For each EHC sub-circuit, we have also considered possible parameter variations affecting the transistors during fabrication, and the discrete components due to aging.

As for faults occurring in the field, for each sub-circuit we have considered all possible: i) node stuck-at 0 (SA0); ii) resistive bridgings (BFs), with realistic values of connecting resistance (R_{BF}) in the range [0..6kΩ] [17]; iii) transistors stuck-on (SON); iv) transistors stuck-open (SOP).

It is worth noticing that the traditional node stuck-at 1 (SA1) fault model, in which the affected node is shortcircuited to the power supply, does not apply to the EHC internal nodes. This because our EHC generates itself the power supply voltage V_{out} and, as shown later, ideal shorts between EHC internal nodes and V_{out} modify considerably also the produced V_{out} voltage. Therefore, we have modeled SA1 faults affecting the internal nodes by a resistive bridge to V_{out}, with a value of connecting resistance of 0Ω (i.e., a short circuit).

For each sub-circuit of the EHC, we have considered also parametric variations up to: i) 30% in transistors widths, lengths, threshold voltages and thickness occurring during manufacturing; ii) 50% in the nominal values of the discrete capacitors and inductors due to aging.

In addition, we have assumed that faults/parameter variations occur one at a time in the field, and that the time elapsing between the occurrence of two following faults/parameter variations is longer than the time interval between two following sensor transmissions.

In order to evaluate the fault effects on the provided V_{out}, we have performed electrical level simulations by means of HSPICE. The results of our analyses are reported in details in the following subsections.

3.1 Faults Affecting the AC/DC Rectifier and DC/DC Converter

A. Stuck-At-0 (SA0) Affecting the AC/DC

They may affect the following nodes: i) $V_{in}+$; ii) $V_{in}-$; iii) V_1; iv) V_S.

We have verified that the SA0 of kind i) is activated during the positive half-waves of V_{piezo} (Fig. 1), independently of the EHC operating mode. When the SA0 is activated, the AC/DC rectifier fails in rectifying the positive V_{piezo} half-waves, thus failing in charging C_{stor} (thus also C_{out}) to the expected value. Therefore, the

provided V_{out} is lower than the fault-free value. We have verified that, due to the rapid drop to ground of V_{out}, the correct operation of the EHC (whichever its operating mode) and of the multisensor node are compromised.

As for the SA0 of kind ii), it is activated during the negative half-waves of V_{piezo}, independently of the EHC operating mode. When this SA is activated, the AC/DC converter fails in rectifying the negative V_{piezo} half-waves. Analogously to SA0 of kind i), C_{stor} and C_{out} are not charged to their expected values. Therefore, the V_{out} value turns out to be lower than that provided under fault-free conditions, and is insufficient for the correct operation of the driven multisensor node, whichever the EHC operating mode. As a consequence, the correct operation of EHC and multisensor node are compromised.

The SA0 of kind iii) is activated when $|V_{piezo}| > |V_{Cstor}|$, for every EHC operating mode. The capacitor C_{stor} turns out to be not connected to the EHC, and the whole current produced by the piezoelectric generator flows to ground, being V_1 SA0. Consequently, the capacitor C_{out} is quickly discharged and the voltage V_{out} drops rapidly to ground. Therefore, the EHC and the multisensor node do not behave correclty.

Finally, SA0s of kind iv) are activated when $|V_S| \neq 0$, independently of the EHC operating mode. When this SA is activated, the inductor L2 is constantly connected between $V_{in}+$ and ground, thus decreasing the amount of current flowing to C_{stor} through D1-D4. As a result, C_{stor} and C_{out} cannot be charged up to their expected values by the AC/DC and DC/DC, respectively. As a consequence, V_{out} drops gradually to ground, compromising the correct operation of multisensor node.

B. Stuck-At-0 (SA0) Affecting the DC/DC

They may affect nodes: i) V_2; ii) V_{out}; iii) V_{CS}.

The SA0 of kind i) is activated when V_{CS} presents a high logic value (i.e., V_{CS}=2.1V) and M1 is conductive. This SA0 prevents the current coming from the AC/DC from flowing through the inductor L1. Consequently, the capacitor C_{out} is quickly discharged and the voltage V_{out} drops rapidly to ground. As a consequence, the correct operation of both the EHC and multisensor node is compromised. Similar results have been obtained for SA0s of kind ii) and iii).

C. Bridging Faults (BFs) Affecting the AC/DC

We consider all possible BFs, with realistic values of connecting resistance (R_{BF}) in the [0..6kΩ] range [17]. Their activating conditions, as well as their produced effects during both the DA and TX operating modes are summarized in Table 1.

Particularly, we have verified that, when activated, each BF (except for the $V_{in}^+ - V_S$ and the $V_1 - V_{out}$ BFs discussed below) results in a gradual drop of the V_{out} voltage to ground, thus making it insufficient for the correct operation of the driven multisensor node. As an example, Fig. 2(a) reports the V_{out} behavior obtained considering a BF between $V_{in}+$ and GND, with a value of connecting resistance R_{BF} = 1kΩ and the multisensor node operating in the DA mode for $t < t_1$, and in the TX mode for $t \geq t_1$. As can be seen, after the multisensor enters the TX mode at t_1, the voltage V_{out} quickly drops to a value slightly higher than 1.5V, which is the minimum voltage value required by the multisensor node to operate correctly. Afterward, it continues to drop gradually to ground, reaching 1.5V soon after t_1.

TABLE 1
EFFECTS OF BFS AFFECTING THE AC/DC CONVERTER BEHAVIOR.

BF	Activating Condition	Gradual Degradation to GND		Overshoot
		DA	TX	DA
$V_{in}^+ - GND$	$V_{piezo} > 0V$	–	[0,6kΩ]	–
$V_{in}^- - GND$	$V_{piezo} < 0V$	–	[0,6kΩ]	–
$V_{in}^+ - V_{in}^-$	$V_{piezo} \neq 0V$	–	[0,6kΩ]	–
$V_{in}^- - Vs$	$V_{piezo} \neq V_{piezo\_max} = 6V$	–	[0,6kΩ]	–
$V_{in}^+ - V_1$ / $V_{in}^- - V_1$	$\|V_{piezo}\| > \|V_{Cstor}\|$	–	[0,6kΩ]	–
$V_{in}^+ - V_{out}$ / $V_{in}^- - V_{out}$	$V_{piezo} \neq 2.1V$	–	[0,6kΩ]	–
$V_1 - V_{out}$	$V_{Cstor} \neq 2.1V$	–	[0,6kΩ]	[0,6kΩ]
$V_1 - GND$	$V_{Cstor} > 0$	[0,6kΩ]	[0,6kΩ]	–
$Vs - V_{out}$	$Vs \neq 2.1V$	–	[0,6kΩ]	–
$Vs - GND$	$\|Vs\| \neq 0V$	–	[0,6kΩ]	–

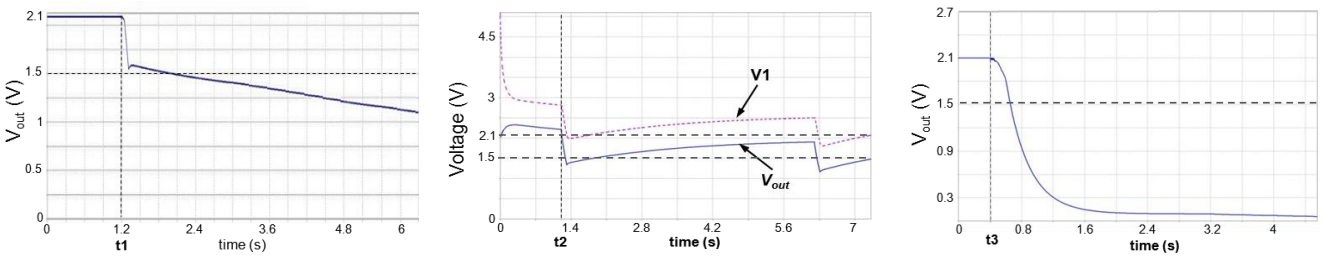

Fig. 2. (a) V_{out} variation due to a BF (with R_{BF} = 1kΩ) between V_{in}+ and GND. (b) Variation of V_{out} (solid line) and V1 (dashed line) in case of a BF (with R_{BF} = 500Ω) between them. (c) Variation of V_{out} due to a BF (with R_{BF} = 500Ω) between V_{out} and GND.

As for the BF between V_{in}^+ - V_S, it is activated each time the SSHI switch is closed, thus making V_S equal to V_{in}-. This BF, connecting a resistor in parallel to the inductor L2, reduces the current flowing through L2. However, neither the voltage on C_{stor}, nor V_{out} are affected.

Finally, the BF between V_1 and V_{out} is activated each time the voltage value on V_1 (i.e., the voltage across C_{stor}) differs from the voltage value on V_{out} (i.e., 2.1V). This BF connects the positive terminals of C_{stor} and C_{out}, thus originating a charge distribution process between them. As depicted in Fig. 2(b), this BF generates an initial voltage overshoot (for $t < t_2$) on V_{out}, which reaches 2.4V (a value higher than the maximum tolerated voltage of 2.1V). Meanwhile, the voltage V_1 across C_{stor} is reduced because of a decrease in the charge stored on C_{stor}. This makes the EHC fail in keeping V_{out} above 1.5V, when the multisensor node switches from the DA to the TX mode at time t_2. When following commutations of the multisensor node from the DA to the TX mode occur, V_{out} is further reduced, decreasing gradually to GND, thus compromising the correct operation of the multisensor node.

From Fig. 2(b), we can also observe that V_{out} can exceed the maximum value (2.1V) allowed for the sensor correct operation. As previously clarified, in order to set such a maximum voltage to 2.1V, we included in the EHC a low cost clamping circuit [16]. Such a circuit also avoids that possible sudden voltage bursts on V_{out}, induced by capacitive or inductive coupling can exceed 2.1V.

D. Bridging Faults (BFs) Affecting the DC/DC

We consider BFs with values of connecting resistance (R_{BF}) in the range [0..6kΩ] [17]. The activating conditions, as well as the produced effects during both DA and TX operating modes are reported in Table 2.

We can observe that the BF between V_2 and ground affects V_{out} only during the TX mode, resulting in a gradual degradation to ground for all R_{BF} in the considered range. As a consequence, the correct operation of the multisensor node may be compromised. Similar results have been obtained for BFs between nodes V_{CS}- V_{out}, V_{CS} - *GND*, V_{ref} - V_{CS}, and V_{CS} - V_2, the latter for values of R_{BF} in the range [4kΩ..6kΩ].

As for the BF between V_1 and V_{CS}, it makes M1 permanently ON. Therefore, this BF produces effects similar to the BF between V_1 and V_{out} affecting the AC/DC (Sect. 3.1C). As a result, the multisensor node correct operation is compromised. A similar behavior has been observed also for the BF between V_1 and V_2.

The BF between V_{out} and GND always affects V_{out} (Table 2). Fig. 2(c) shows the effects on V_{out} after the occurrence of this BF at time t_3, with R_{BF} = 500Ω. We can observe that V_{out} quickly drops to ground after t_3, thus compromising the correct operation of the multisensor node. A similar behaviors has been verified also for BFs between V_{CS} and V_2, for values of R_{BF} in the range [0.. 4kΩ].

Finally, the BF between V_{ref} and V_{out} is never activated, independently of the multisensor operating mode. In fact, during the multisensor normal operation it is always V_{ref} = V_{out} = 2.1 V. Therefore, this fault does not produce any effect on V_{out}. Moreover, we have verified that, if this fault is followed by any of the faults analyzed before, the resulting effect on V_{out} is the same as that generated by such a following fault only (which has been pre-

TABLE 2
EFFECTS OF BFS AFFECTING THE DC/DC CONVERTER BEHAVIOR.

BF	Activating Condition	Drop to GND		Gradual Degradation to GND	Overshoot
		DA	TX	DA	TX
V_2 – gnd / V_{CS} – gnd	V_{CS} = 2.1V	–	–	[0,6kΩ]	–
V_1 – V_{CS}	V_{CS} = 0V	–	–	[0,6kΩ]	[0,6kΩ]
V_1 – V_2	V_{CS} = 2.1V	–	–	[0,6kΩ]	[0,6kΩ]
V_{CS} – V_2	V_{CS} = 2.1V	[0,4kΩ]	–	(4k,6kΩ]	–
V_{out} – gnd	$V_{out} \neq$ 0V	[0,6kΩ]	[0,6kΩ]	–	–
V_{CS} – V_{out} / V_{ref} – V_{CS}	V_{CS} = 0V	–	–	[0,6kΩ]	–

viously reported). A similar behavior has been observed also for the BF between nodes V_2 and V_{out}.

E. Transistor SONs / SOPs Affecting the AC/DC

They may affect the transistors implementing (Fig. 1): i) diodes D1, D4; ii) diodes D2, D3.

As for SONs/SOPs of kind i), they are activated when $|V_{piezo}| > |V_{Cstor}|$, and they reduce the average current charging C_{stor}. As a result, a temporary voltage drop on V_{out} is produced when the multisensor starts a transmission, thus compromising its correct operation.

As for SONs/SOPs of kind ii), they are activated when $|V_{piezo}| < |V_{Cstor}|$. We have verified that these SONs/SOPs produce the same effects as SONs/SOPs of kind i) above, causing a temporary voltage drop on V_{out} during the TX operating mode, thus compromising the correct operation of the multisensor node.

F. Transistor SONs / SOPs Affecting the DC/DC

They may affect (Fig.1): i) M1; ii) D5. SON of kind i) is activated when V_{CS}=0V. It connects permanently nodes V_1 and V_2, and its effect on the output of the EHC is similar to that of a BF between V_1 – V_{out}, whose effect is depicted in Fig. 2(b). Therefore, a SON of kind i) produces an initial overshoot on V_{out}. Then, after successive commutations of the multisensor node from the DA to the TX operating mode, V_{out} starts a gradual drop to ground, compromising the multisensor node correct operation.

The SON of kind ii) is activated when V_{CS}=0V. It gives rise to a permanent conductive path from V_2 to ground, thus preventing C_{out} from charging. Consequently, V_{out} drops to ground after the next transmission of the multisensor node, thus compromising its correct operation.

As for the SOP of kind i), it is activated when V_{CS}=2.1V, and induces operating conditions similar to the SA0 affecting node V_2. In this case, the DC/DC is disconnected from the AC/DC, since M1 is always off. Consequently, C_{out} is quickly discharged and the voltage V_{out} drops rapidly to ground, thus compromising the correct operation of the multisensor node.

Finally, the SOP of kind ii) is activated when V_{CS}=0V. Due to this SOP, D5 is always OFF, and after V_{CS} flips to 0 switching off M1, no current flows through L1, as in the fault-free case. This prevents the DC/DC from charging C_{out} up to its expected voltage value. Therefore, V_{out} turns out to be lower than what expected under fault-free conditions, and it does not suffice for the correct operation of the multisensor node.

3.2 Parametric variations Affecting the AC/DC Rectifier and the DC/DC Converter

D. Parametric Variations Affecting the AC/DC

We have considered: i) the diodes D1-D4; ii) the transistors composing the SSHI; iii) L2; iv) C_{stor}.

Parametric variations of kind i), ii) and iii) do not affect the correct operation of the EHC, and V_{out} remains correctly fixed at 2.1V. In fact, as expected, the DC/DC tries to keep its output voltage equal to V_{ref}, independently of the voltage value at its input. As discussed in the previous section, the Control Circuit of the DC/DC compares V_{out} with a reference voltage V_{ref} and, based on the comparison result, it adjusts the duty-cycle of V_{CS} in order to make V_{out} equal to V_{ref}. Thus, parametric variations of kind i), ii) and iii) affecting the AC/DC are compensated by the DC/DC, so that they do not alter V_{out}.

Parametric variations of kind iv) do not affect the correct operation of the EHC, as long as they are smaller than 35%. For higher values, the EHC fails in keeping V_{out} above 1.5V, when the multisensor node switches from the DA to the TX mode at time t_1 (Fig. 3(a)), thus compromising the correct operation of the multisensor node.

D. Parametric Variations Affecting the DC/DC Converter

We have considered: i) the transistor M1; ii) the diode D5; iii) L1; iv) C_{out}.

Parametric variations of kind i), ii), iii) and iv) never affect the correct operation of the EHC. In fact, V_{out} may slightly vary when the sensor switches from the DA to the TX mode, but the EHC is able to keep V_{out} within the voltage interval required for the sensor correct operation. As an example, Fig. 3(b) shows the V_{out} variation when the sensor switches from DA to TX mode at time t_1, for -30% variations of the M1 channel width with respect to its nominal value. As can be seen, V_{out} slightly decreases when the sensor enters the TX mode, but the minimum voltage reached is considerably higher than the minimum value (1.5V) required for

the sensor correct operation.

As observed for the AC/DC, parametric variations on the components of the DC/DC do not modify the voltage V_{out}. In fact, the Control Circuit of the DC/DC adjusts the duty-cycle of signal V_{CS} in order to counteract V_{out} variations. Therefore, parametric variations of kind i), ii), iii) and iv) do not alter the V_{out} value.

4. Proposed Energy Harvesting Concurrent Monitoring Circuit

We propose a circuit to monitor continuously, and concurrently with the system operation, the correctness of the voltage V_{out} provided by the EHC. The proposed monitor, whose electrical structure is based on the circuit that we introduced in [9], generates an error signal when V_{out} drops below 1.5V, or when it is affected by internal faults (as will be shown in Section 6). In fact, since our monitor is employed for high reliability applications, it should be able to detect also faults affecting itself. This is achieved by implementing the monitor as a self-checking circuit employing two output signals assuming alternating logic values. If a single output only had been considered, a simple output stuck-at fault at the fault-free indication would have made the whole circuit useless.

Our circuit is shown in Fig. 4. The pMOS M1 and the capacitor C1 generate an auxiliary voltage V_{aux}, which is used as power supply for our circuit. In fact, the proposed monitor cannot use V_{out} as power supply, since it should provide an error indication V_{out} drops below the required voltage value. Under fault free conditions, it is $V_{aux} \cong V_{out}$. Transistor M1 operates as a diode, allowing current to flow from V_{out} to V_{aux}, thus charging C1, when $V_{out} > V_{aux}$ (i.e., when the circuit is turned on). Meanwhile, M1 prevents current from flowing from V_{aux} to V_{out} when $V_{out} < V_{aux}$, due to a fault affecting the EHC, thus avoiding the discharge of C1. Therefore, when V_{out} drops, C1 allows to keep V_{aux} approximately constant for a chosen time interval, that is a function of the C1 value, thus allowing the circuit to provide an error indication.

It is worth noticing that, prior to fault occurrence, the voltage across C1 is maintained to the correct value by M1, which acts as a diode, in spite of leakage current affecting C1. In fact, if leakage current starts discharging C1, diode M1 turns on and starts charging C1 up to the correct voltage value.

Multiplexers MUX1 and MUX2 receive V_{out} and ground (GND) as inputs, and the system clock (CK) as control signal. When CK=0, it is $O_{MUX} = V_{out}$ and $O_{MUX2} = 0$, while when $CK = 1$, it is $O_{MUX1} = 0$ and $O_{MUX2} = V_{out}$. Each multiplexer has been implemented using two transfer gates (TGs). They are driven by CK and its complement (CK'), which are properly synchronized.

As for INV11 and INV21, they are pMOS dominant, and designed to have a nominal logic threshold voltage (denoted as V_{LT-PD}) equal to the 72% of their power supply voltage (V_{aux}). Finally, INV12 and INV22 are minimum sized and symmetric inverters, employed to reshape the signals on nodes $I1$ and $I2$.

In the fault-free case, V_{out} is approximately equal to V_{aux}. When CK=0, it is $O_{MUX1} = V_{out}$ ($\cong V_{aux}$), thus INV11 produces a low logic value ($I1$=0). Instead, INV21 produces a high logic value ($I2$=1), since it is O_{MUX2}=0. Therefore, when CK=0, it is $(E_{rr1}, E_{rr2}) = (1, 0)$. Analogously, when CK=1, it is $(E_{rr1}, E_{rr2}) = (0, 1)$. Therefore, under fault-free conditions, the outputs of our monitor present always alternating and complementary logic values $(E_{rr1}, E_{rr2}) = (1, 0)$ or $(0, 1)$), as required for its reliable operation.

Let us consider the case of a fault affecting EHC, and making V_{out} drop below 1.5V. Let us refer to this value as V_{outmin}. In this case, it is $V_{out} < 0.72 * V_{aux}$, with V_{aux} maintained equal to 2.1V by C1. Since V_{aux} acts as power supply for INV11 and INV21, it is $V_{outmin} = V_{LT-PD} = 1.5V$, where V_{LT-PD} is the logic threshold voltage of the two inverters.

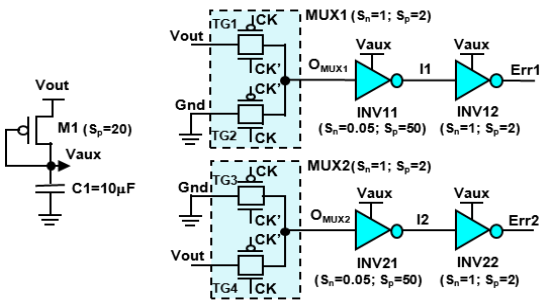

Fig. 4. Proposed monitoring circuit.

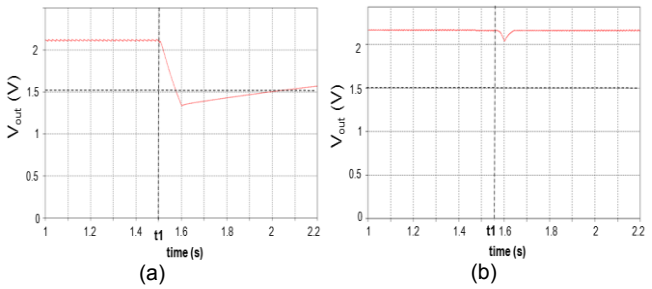

Fig. 3. (a) V_{out} in case of 50% variation in C_{stor}. (b) V_{out} in case of -30% variation in the M1 channel width.

When CK=0, it is O_{MUX1}=V_{out} < V_{outmin} = V_{LT-PD}. Consequently, INV11 gives a high logic value as output ($I1$=1). On the other hand, it is O_{MUX2}=0, so that also INV21 produces a high logic value ($I2$=1). Thus, when CK=0, it is (E_{rr1}, E_{rr2}) = (0, 0).

When CK=1, it is O_{MUX1}=0, thus INV11 produces a high logic value ($I1$=1). Meanwhile, it is O_{MUX2} = V_{out} < V_{outmin} = V_{LT-PD}, so that $I2$=1. Therefore, also when CK=1, it is (E_{rr1}, E_{rr2}) = (0, 0).

Therefore, when V_{out} drops below 1.5V, our monitor gives equal values on E_{rr1} and E_{rr2} during the whole CK cycle. We consider (E_{rr1}, E_{rr2}) = (0, 0) or (1, 1) as indications of either faults affecting EHC or, as shown in Section 6, faults affecting our monitor itself.

5. Implementation and Verification

We have implemented our monitor considering a standard 180nm CMOS technology. The proposed scheme is reported in Fig. 4, where also the n,pMOS transitor shape factors (S_n, S_p) are reported. The value of C1 is high enough to allow our monitor to work correctcly for many seconds after V_{out} goes below 1.5V, thus allowing the activation of proper recovery actions. We have analyzed the behavior of our monitor by conventional and Monte Carlo electrical simulations, considering 20% statistical variations, with uniform distribution, of oxide thickness, transistor threshold voltage and electron/hole mobility.

Fig. 5(a) reports the simulation results obtained under nominal values of electrical parameters in case of faults making V_{out} temporary lower than V_{outmin} = 1.5V. We can observe that, during the time interval in which V_{out} is lower than V_{outmin}, it is (E_{rr1}, E_{rr2}) = (0, 0), thus indicating the presence of an incorrect voltage value on V_{out}.

Fig. 5(b) shows the Monte Carlo simulations results. As can be seen, V_{outmin} varies between 1.55V and 1.3V. Therefore, parameter variations can make our monitor generate: i) false error indications (if V_{outmin} > 1.5V); ii) false indications of correct operation (if V_{outmin} < 1.5V). In order to avoid these conditions, the logic thresholds of the inverters of our monitor should be programmable after fabrication, for instance by adopting the approach in [19]. This would imply an extra cost in area which, however, has a negligible impact the EHC area, as shown in Section 7.

TABLE 3
Activating conditions for SAs affecting our monitor.

	Kind of SA								
	1)		2)		3)		4)		5)
	O_{MUX1}	O_{MUX2}	I1	I2	E_{rr1}	E_{rr2}	CK	CK'	V_{aux}
SA0	CK=0	CK=1	CK=0	CK=1	CK=1	CK=0	CK=1	CK=0	CK=0 or CK=1
SA1	CK=1	CK=0	CK=1	CK=0	CK=0	CK=1	CK=0	CK=1	–

6. Self-Checking Ability

Our monitor may be affected by faults itself. To guarantee system high reliability, similarly to checkers of self-checking circuits (SCCs) [18], our monitor should check itself with respect to internal faults, and satisfy either the *Totally Self-Checking* (*TSC*) [18], or the *Strongly Code-Disjoint* (*SCD*) [20] property with respect to such faults. As usual with SCCs, we assume that faults occur one at a time, and that the time elapsing between two following faults is long enough to allow the application of all possible input codewords (i.e., the correct V_{out} value) [18].

We have considered a set of faults $\mathcal{F}$ possibly affecting our monitor composed by node stuck-ats (SAs), transistor stuck-opens (SOPs), transistor stuck-ons (SONs) and resistive bridgings (BFs), with values of connecting resistance R in the range [0..6kΩ] [17]. We have analyzed their effects by means of logical and electrical simulations. The achieved results are summarized below.

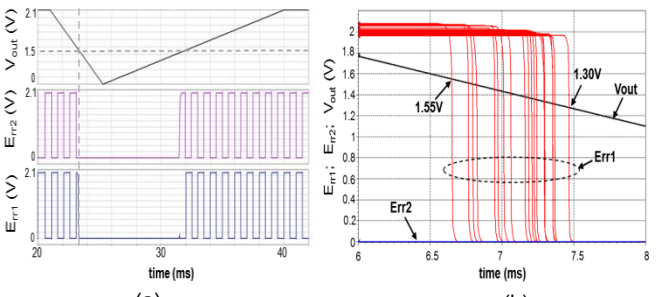

Fig. 5. (a) Results with nominal values of electrical parameters and temporary drop of V_{out}. (b) Monte-Carlo simulations showing the minimum voltage value on V_{out} resulting in an error indication.

6.1 Stuck-At Faults (SAs)

They may affect: i) O_{MUX1}, O_{MUX2}; ii) $I1$, $I2$; iii) E_{rr1}, E_{rr2}; iv) CK, CK'; v) V_{aux}. The activating conditions of the considered SAs 1/0 are summarized in Table 3.

As for SAs of kind i), we have verified that, when they are activated, an error indication is produced during one of the CK semi-periods, so that our circuit is TSC with respect to them. Analogous considerations hold true for SAs of kind ii), iii) and iv).

A SA0 affecting V_{aux} is activated immediately after its occurrence and results in the generation of an error message $(E_{rr1}, E_{rr2}) = (0, 0)$. Our circuit is therefore TSC with respect to such a fault.

Instead, a SA1 on V_{aux} is never activated, thus not resulting in the generation of any error message. Moreover, our circuit is not able to indicate an incorrect voltage value on V_{out}. Therefore, our circuit is neither TSC, nor SCD with respect to it. The occurrence of such a fault should be avoided by properly designing the circuit layout [21].

6.2 Transistor Stuck-Open Faults (SOPs)

They may affect: i) MUX1 and MUX2; ii) INV11, INV12, INV21 and INV22; iii) M1. As for SOPs of kind i), they may affect: i-a) the pMOS or nMOS of TG2 and TG3, or the nMOS of TG1 and TG4; i-b) the pMOS of TG1 and TG4. The activating conditions of the considered SOPs are summarized in Table 4.

When activated, SOPs of kind i-a) do not result in the generation of any error message. However, our circuit continues to detect incorrect V_{out} values. Moreover, if such SOPs are followed by other faults in $\mathfrak{F}$, our circuit continues to work properly and produces an error message after the following fault activation. Therefore, our circuit is SCD with respect to SOPs of kind i-a).

In case of SOPs of kind i-b), the correct operation of our monitor is not modified before their activation. Instead, their activation results in the generation of an error message, so that our circuit is TSC with respect to them. Similar considerations apply to SOPs of kind ii) and iii).

6.3 Transistor Stuck-On Faults (SONs)

They may affect: i) the transistors of MUX1, MUX2; ii) the pMOS of INV11 and INV21; iii) the nMOS of INV11 and INV21; iv) the nMOS and pMOS of INV12 and INV22; v) transistor M1. As for SONs of kind i), they may affect transistors of: i-a) TG1 or TG4; i-b) TG2 or TG3. The activating conditions of the considered SONs are summarized in Table 5.

SONs of kind i-a), when activated, do not result in the generation of an error message. Our circuit continues to detect incorrect V_{out} values and, if SONs of this kind are followed by other faults in $\mathfrak{F}$, it correctly produces an error message when the following fault is activated. Therefore, our circuit is SCD with respect to SONs of kind i-a).

In case of SONs of kind i-b), when they are activated, an error indication is produced during one of the CK semi-periods. Therefore, our circuit is TSC with respect to them. Similarly, as for SONs of kind ii).

SONs of kind iii) do not give rise to the generation of any error message when activated. However, they do not affect the correct behavior of our monitoring circuit. If another fault in $\mathfrak{F}$ occurs, our circuit continues to detect incorrect V_{out} values before the the fault is activated, while it produces an error message after its activation. Therefore, our circuit is SCD with respect to SONs of kind iii).

As for SONs of kind iv), when activated, they result in the generation of an intermediate voltage value on E_{rr1} or E_{rr2} during one of the CK semi-periods. Depending on the logic threshold of the downstream logic, an error indication may be generated. Instead, if no error message is generatied, our circuit continues to work properly. Moreover, if other faults in $\mathfrak{F}$ follow these SONs, our circuit keeps on working correctly, producing an error message after the following fault is activated. Therefore, our circuit is TSC or SCD with respect to this kind of SONs.

Finally, as for a SON of kind v), it produces the same effect as the SA1 affecting node V_{aux}, so that the same considerations apply.

6.4 Bridging Faults (BFs)

TABLE 4
ACTIVATING CONDITIONS FOR SOPS AFFECTING OUR MONITOR.

Kind of SOP	Affected transistor	Activating Condition
1-a)	nMOS, pMOS of TG2 & nMOS of TG4	CK=0 → CK=1
	nMOS, pMOS of TG3 & nMOS of TG1	CK=1 → CK=0
1-b)	pMOS of TG1	CK=1 → CK=0
	pMOS of TG4	CK=0 → CK=1
2)	pMOS of INV11 or INV22 nMOS of INV21 or INV12	CK=0 → CK=1
	nMOS of INV11 or INV22 pMOS of INV21 or INV12	CK=1 → CK=0
3)	pMOS M1	CK=0 → CK=1 / CK=1 → CK=0

TABLE 5
ACTIVATING CONDITIONS FOR SONS AFFECTING OUR MONITOR.

Kind of SON	Affected transistor	Activating Condition
1-a)	nMOS - pMOS of TG1 nMOS - pMOS of TG4	CK=1 CK=0
1-b)	nMOS - pMOS of TG2 nMOS - pMOS of TG3	CK=0 CK=1
2)	pMOS of INV11 pMOS of INV21	CK=0 CK=1
3)	nMOS of INV11 nMOS of INV21	CK=1 CK=0
4)	pMOS of INV12 nMOS of INV12 pMOS of INV22 nMOS of INV22	CK=1 CK=0 CK=0 CK=1

All possible BFs affecting our monitor have been considered (Fig. 6(a)). The maximum resistance value for which each BF results in an error message is reported in Fig. 6(b), along with the activating conditions. When BFs with R_{max}=6kΩ are activated, an error indication is produced during one of the *CK* semi-periods, so that our circuit is *TSC* with respect to them. Instead, BFs R_{B1}, R_{B3} and R_{B10} result in an error message for values of R lower than 3.6kΩ, 5.1 kΩ and 0.6kΩ, respectively. For higher values of R, our circuit continues to detect incorrect V_{out} values. If such BFs are followed by other faults in $\mathfrak{F}$, our circuit continues to work properly before the following fault is activated, and when this occurs it produces an error message. Therefore, our circuit is *SCD* with respect to them.

As for R_{B4}, R_{B6}, and R_{B13}, they are never activated, thus they do not result in an error indication. Due to these BFs, our circuit is no longer able to detect incorrect V_{out} values. Therefore, the occurrence of such faults should be avoided by properly designing the circuit layout [21].

7. COST EVALUATION

We have evaluated the power consumption and area overhead of our monitor. We have implemented it as described in Section 5, with programmable inverters designed as described in [19]. We have compared the area and power required by our monitor to those of the considered EHC, implemented as described in Section 2.

Table 6 shows how the power consumed by our monitor (P_{mon}) and by EHC (P_{EHC}) increase with their respective operating frequencies (i.e., the frequency of CK signal, and the frequency f_{CS} of the EHV control signal V_{CS}). As can be seen, P_{mon} is considerably lower than P_{EHC} for all considered, realistic frequencies. Table 6 reports also P_{mon} relative increase over P_{EHC}. As can be seen, such an increase is negligible

TABLE 6
POWER CONSUMED BY OUR MONITOR (P_{MON}) AND BY EHC (P_{EHC}) AND RELATIVE POWER CONSUMPTION INCREASE.

Monitor/EHC operating frequency	Power consumption		
	EHC (μW)	Our monitor (nW)	ΔP (%)
1 kHz	480	7.68	0.0016
2 kHz	490	8.25	0.0016
3 kHz	490.8	8.7	0.0017
4 kHz	492	9.28	0.0018
5 kHz	492.2	9.79	0.0019
6 kHz	492.4	10.2	0.0020
7 kHz	492.7	10.8	0.0021
8 kHz	493	11.5	0.0023

for all considered frequencies.

According to the implementation in Section 5, our monitor requires an area of 500 squares (16μm^2) for the 41 transistors (Fig 7). Since the AC/DC and DC/DC converters of EHC (Fig. 1) require 5920 squares (189μm^2), we can conclude that the area increase required by our monitor is approximately 8.5%.

As for C1 (Fig 7), due to its relatively large capacitance value (C1 = 10μF), it may be implemented as a discrete component, together with other discrete capacitors, C_{stor} and C_{out}, and inductors, (L1 and L2), of the EHC. Since the two capacitors of the EHC are considerably larger than C1 (C_{stor}=180μF and C_{out}=500μF), the implementation of C1 negligibly impacts the EHC area. Therefore, we can conclude that our proposed monitor induces a very small area increase in the total area of the considered EHC.

8. CONCLUSIONS

We have addressed the concurrent detection of faults possibly affecting an EHC powering a wearable biomedical sensor. We have analyzed the effects of possible faults and parametric variations affecting the components of the EHC, showing that they may make it fail in producing the supply voltage level required by the sensor.

We have then proposed a novel low cost circuit to monitor continuously, and concurrently with normal operation, the power supply voltage produced by the EHC. Our circuit gives an error indication if the provided supply voltage falls below the minimum value required by the sensor to work correctly, thus allowing the activation of proper recovery actions.

Our monitor requires very low costs in terms of power consumption and area overhead. Moreover, it features self-checking ability with respect to its possible internal faults, but for a few faults, whose likelihood can be reduced by means of proper layout design.

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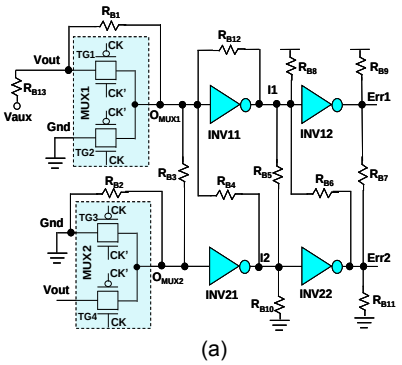

(a)

R_{Bi}	R_{max} (kΩ)	Activating condition
R_{B1}	3.6	CK=1
R_{B2}	6	CK=0
R_{B3}	5.1	CK=0 or 1
R_{B5}	6	CK=0 or 1
R_{B7}	6	CK=0 or 1
R_{B8}	6	CK=0
R_{B9}	6	CK=1
R_{B10}	0.6	CK=0
R_{B11}	6	CK=1
R_{B12}	6	CK=0 or 1

(b)

Fig. 6. Considered BFs (a), and maximum R value for which they can be detected (b).

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Martin Omaña received the degree in electronic engineering from the University of Buenos Aires in 2000. In 2002 he was awared a MADESS grant and joined the University of Bologna, where he obtained the PhD in Electronic Engineering and Computer Science in 2005. He is currently a Post Doctoral fellow at the same University. His research interests are in the field of fault modeling, on-line test, robust design, fault tolerance and photovoltaic systems.

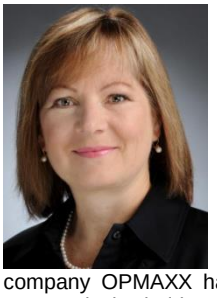
Daniele Rossi received the degree in electronic engineering and the PhD degree in electronic engineering and computer science from the University of Bologna in 2001 and 2005, respectively. He is currently a Post Doctoral fellow at the same University. His research interests include fault modeling and fault tolerance, focusing on coding techniques for fault-tolerance and low-power, signal integrity for communication infrastructures, robust design for soft error resiliency.

Daniele Giaffreda received the M.S. degree in electronic engineering from the University of Bologna, Italy in 2009. He is currently working as Ph.D. student at the Advanced Research Center on Electronic Systems for Information and Communication Technologies (ARCES) E. De Castro, University of Bologna, Bologna, Italy. His research interests include faults modelling and electrical simulations with particular emphasis on the silicon photovoltaic solar cell.

Roberto Specchia received the bachelor degree in electrical Engineering in 2006 and the Master degree in Electrical and Automation engineering in 2009, from the University of Bologna, Italy. He peformed a reseach period focused on energy harvesting systems and fault tolerance analysis in collaboration with Cyber LAb at Simon Fraser University, Vancouver, Canada. Since 2009, he is a software and electrical engineer, designing automatic machines for packaging.

Cecilia Metra is a Professor in Electronics of the Univ. of Bologna. She is a member of the Bpard of Governorns of the IEEE CS 2013-2015. She is Editor-in-Chief of the IEEE CS on-line publicationComputing Now (starting 2013) and Associate Editor-in-Chief of the IEEE CS Transactions on Computers. Her research interests are in the field of fault modeling, on-line test, robust design, fault tolerance, energy harvesting and photovoltaic systems.

Marcin Marzencki graduated from the AGH University of Science and Technology in Cracow, Poland, in electronics and telecommunications. He obtained the PhD degree in microelectronics from Joseph Fourier University in Grenoble, France in 2007. Now he is with the CIBER lab at Simon Fraser University in Vancouver, Canada. His main fields of interest focus on environmental energy harvesting, distributed sensor systems and MEMS devices.



Bozena Kaminska, Ph.D. is Professor and Canada Research Chair in wireless sensor networks at Simon Fraser University, focusing on the research and development of innovative micro and nano devices. She leads CIBER, the Centre for Integrative Bio-Engineering Research at Simon Fraser University. At present she serves as Chairman of the Board of Directors for CMC Microsystems. She has been at Simon Fraser University since 2005 after her company OPMAXX has been acquired by Credence Corporation. Dr. Kaminska holds multiple patents. She was recognized with the 2010 Entrepreneurship Fellow Award by the British Columbia Innovation Council for her leadership and initiative in developing multiple commercially attractive wireless technologies for healthcare, security, asset tracking, and document verification.