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A 28mW 320MHz 3rd–Order Continuous-Time Time-Interleaved Delta-Sigma Modulator with 10MHz Bandwidth and 12 Bits of Resolution

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***Abstract*—this paper presents a 3rd-order two-path Continuous-Time Time-Interleaved (CTTI) delta-sigma modulator which is implemented in standard 90nm CMOS technology. The architecture uses a novel method to solve the delayless feedback path issue arising from the sharing of integrators between paths. The clock frequency of the modulator is 320MHz but integrators, quantizers and DACs operate at 160MHz. The modulator achieves a dynamic range of 12 bits over a bandwidth of 10MHz and dissipates only 28mW of power from a 1.8-V supply.**

Keywords-time-interleaved; ΔΣ modulator; signal-to-noise ratio

I. INTRODUCTION

The rapid growth of the portable communication device markets such as audio systems and consumer electronics has led to an increasing demand for ADC designs with bandwidths up to 10-20MHz and medium resolutions of 10 to 12 bits [1]. In this paper we present an ADC which has potential to operate at high sampling rate with medium resolution.

The signal bandwidth ΔΣ modulators can deal with is narrow and restricted by the OverSampling Ratio (OSR) and technology deployed. The maximum achievable sampling rate in Discrete-Time (DT) ΔΣ modulators which are implemented using Switched-Capacitor (SC) techniques, is approximately 100-200MHz [1] but for Continuous-Time (CT) ΔΣ modulators which are implemented through the use of active-RC or gm-c filters [2], a maximum sampling rate of 300-400MHz is indeed feasible [3].

By using the time-interleaving technique and M interconnected parallel modulators that are working concurrently, the effective sampling rate and the OSR becomes M times the clock rate and the OSR of each modulator respectively [4],[5],[6]. It should be noted that the required resolution can be acquired without increasing the order of the modulator or the number of bits for the quantizer and also without utilizing a state of the art technology.

By using time-interleaving techniques and CT loop filters, a 3rd-order CTTI ΔΣ modulator is designed. One set of integrators is shared between paths in order to save the power dissipation, silicon area and to eliminate the instability arising from DC offset mismatch of the two individual integrator sets based the two-channel interleaving case [5].

This paper is organized as follows. In section II, a two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator is derived from a 3rd-order conventional DT ΔΣ modulator using the time domain equations and then it is converted to a CTTI ΔΣ modulator. The delayless feedback path problem and our proposed solution are both discussed in detail in this section. In section III, MATLAB simulation results are presented. In section IV, circuit design of the modulator is discussed. Finally, conclusions are given in section V.

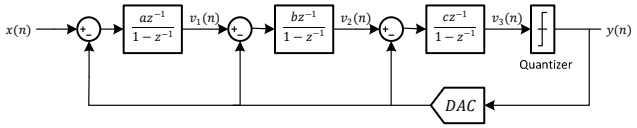


Figure 1. A 3rd-order conventional single-loop DT ΔΣ modulator.

II. DERIVATION OF TIME-INTERLEAVED ΔΣ MODULATOR

The 3rd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator is derived directly from the time domain node equations of the conventional DT ΔΣ modulator as shown in Figure 1. The general method was described in detail in [7]. It is assumed that the DAC in the feedback loop is ideal ($H_{DAC}(z)=1$).The time domain equations of the modulator are written for two consecutive time slots as (2n)th and (2n+1)th and by sharing only one set of integrators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. Equation sets (1) and (2) are derived as follows:

$$v_{11}(n) = ax(n) \quad - ay_2(n) + v_{12}(n) \tag{1.a}$$
$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \tag{1.b}$$
$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \tag{1.c}$$
$$y_1(n) = Q[v_{31}(n)] = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \tag{1.d}$$

and

$$v_{12}(n) = ax(n-1) \quad - ay_1(n-1) + v_{11}(n-1) \tag{2.a}$$
$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \tag{2.b}$$
$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \tag{2.c}$$
$$y_2(n) = Q[v_{32}(n)] \tag{2.d}$$

where $Q[.]$ represents the quantization function. Equation set (3) is derived by further substituting equation set (1) into equation set (2).

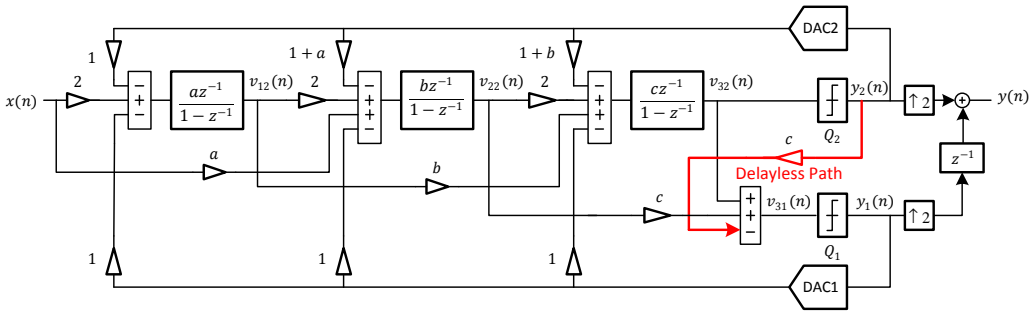


Figure 2. A 3rd-order two-path DTTI ΔΣ modulator with shared integrators.

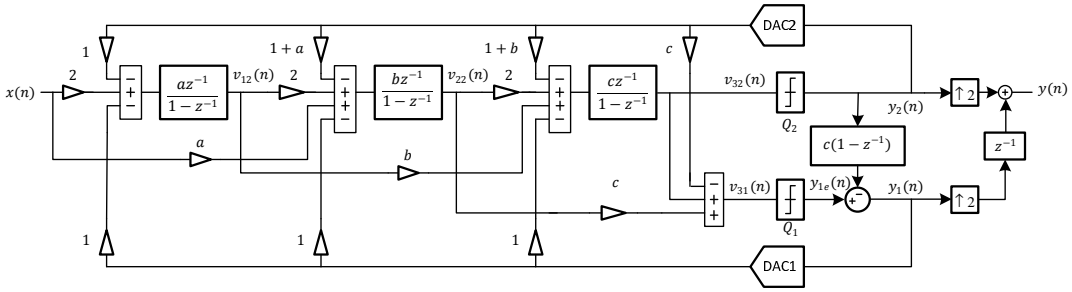


Figure 3. The proposed 3rd-order two-path DTTI ΔΣ modulator with shared integrators.

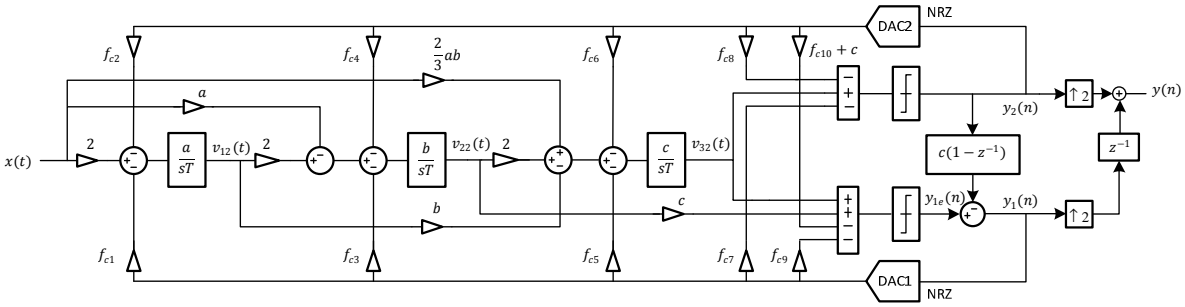


Figure 4. The proposed 3rd-order two-path CTTI ΔΣ modulator with shared integrators.

$$v_{12}(n) = 2ax(n-1) - ay_1(n-1) - ay_2(n-1) + v_{12}(n-1) \quad (3.a)$$

$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \quad (3.b)$$

$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - cy_1(n-1) - c(1+b)y_2(n-1) + v_{32}(n-1) \quad (3.c)$$

The DTTI ΔΣ modulator which is shown in Figure 2 is derived directly from the time domain equation sets (1) and (3).

A. *Delayless Feedback Path Issue in TI ΔΣ Modulators*

In order to save power, silicon area and to eliminate the instability arising from DC offset mismatch of the individual integrator sets in multi-path TI ΔΣ modulators, one set of integrators is shared between paths but it causes a problem which is called the "delayless feedback path" problem. In DTTI ΔΣ modulator which is shown in Figure 2 and expressed by equation (1.c) in which $v_{31}(n)$ (the input of quantizer Q1) is directly linked to $y_2(n)$. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay [8]. The novel method proposed in this paper resolves this issue and is based on an error correction technique. We intentionally induce an error in the analog domain through the use of the output of DAC2 as shown in Figure 3. Quantizer Q1 quantizes the signal $v_{31}(n)$ as follows:

$$y_1(n) = Q[v_{31}(n)] \quad (4)$$

Equation (5) is derived by substituting (1.c) into (4):

$$y_1(n) = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \quad (5)$$

The output of DAC2 is used in (6) and equation (5) is rewritten as:

$$y_1(n) = Q[cv_{22}(n) - cy_2(n-1) + v_{32}(n)] + cy_2(n-1) - cy_2(n) \quad (6)$$

The output of Q1 is called $y_{1e}(n)$ in (7):

$$y_1(n) = y_{1e}(n) + cy_2(n-1) - cy_2(n) \quad (7)$$

$$error = c\Delta y = c(y_2(n) - y_2(n-1)) \quad (8)$$

$$Y_1(z) = Y_{1e}(z) - c(1 - z^{-1})Y_2(z) \quad (9)$$

As stated in (7), $y_{1e}(n)$ (the output of Q1) requires to be corrected before it is applied to the input of DAC1; otherwise it causes instability in the modulator as it will change the modulators dynamics by increasing its order. A first order differencer block $(1 - z^{-1})$ is used to perform this correction as described in (9). The proposed 3rd-order two-path DTTI ΔΣ modulator with shared integrator is shown in Figure 3.

B. *Derivation of CTTI ΔΣ Modulator*

The CTTI ΔΣ modulator equivalent of the DTTI ΔΣ modulator of Figure 3 can be obtained in three steps as follows: The first step is to determine the DT loop filters of the DTTI ΔΣ modulator. The second step is to convert the DT loop filters into equivalent CT loop filters by using the impulse-invariant transformation [1],[4],[6]. The third step is to convert the modulator into a 3rd order CTTI ΔΣ modulator as shown in Figure 4. Two DACs with Non-Retrun-To-Zero (NRZ) implementation and intentional delay of $0.25T$ ($T = 1/160MHz$) have been used. To overcome the excess-loop delay issue, two additional feedback paths from the outputs of DAC1 and DAC2 to the inputs of each quantizer (Q1 and Q2) are used.

III. MATLAB Simulation

The proposed CTTI ΔΣ modulator has been simulated using the SIMULINK toolbox of MATLAB. All specifications of the CTTI ΔΣ modulator are as follows.

$\{a, b, c\} = \{0.27639, 0.76393, 2.0\}$

$\{f_{c1}, f_{c3}, f_{c5}, f_{c7}, f_{c9}\} = \{1.0, 1.0, 0.9648, 0.6708, 1.3291\}$

$\{f_{c2}, f_{c4}, f_{c6}, f_{c8}, f_{c10}\} = \{1.0, 1.2764, 1.7287, 1.3291, 2.1986\}$

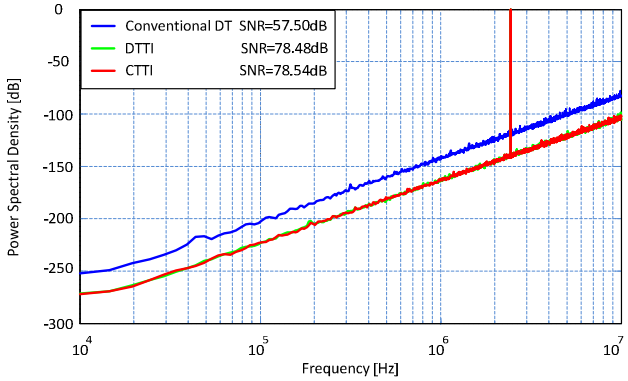


Figure 5. The output spectra of the conventional DT, the DTTI and the CTTI ΔΣ modulator for a 2.4462MHz input with clock frequencies of 160MHz, 320MHz and 320MHz respectively.

The output spectrum of this CTTI ΔΣ modulator is compared with the conventional DT and the DTTI ΔΣ modulators in Figure 5. The output spectra of the DTTI and CTTI ΔΣ modulators are the same and their in-band noise are shaped more than the conventional DT ΔΣ modulator. The SNDRs of the conventional DT, the DTTI and CTTI ΔΣ modulators are 57.50dB, 78.47dB and 78.54dB respectively. Therefore in this particular case, the SNDRs of the time-interleaved ΔΣ modulators are improved by 21dB. As can be seen in Figure 5, non-idealities have not been included in this comparison.

IV. Circuit Design and Simulation

The modulator circuit has been designed using the 90nm CMOS TSMC technology with the supply voltage of 1.8-V. Figure 6 shows the block diagram of the 3rd-order two-path CTTI ΔΣ modulator. The operating frequency of the two quantizers, DACs and all other blocks except for the output multiplexer is 160MHz but the output multiplexer operates at 320MHz. The OSR of the modulator is 16, allowing a maximum input signal bandwidth of $10MHz$. The major circuit blocks of the modulator include three active-RC integrators, ten 4-bit current steering DACs, one 4-bit and one 5-bit flash ADC, two summation circuits, a clock generator, a biasing circuit, an output multiplexer and a digital error correction block $(1 - z^{-1})$.

As can be seen in Figure 6, three active-RC integrators have been used and RC time constant varies up to 50% in CMOS technologies. A tuneable capacitor array will be used to tune up the RC time constant of the integrators and to compensate for process variations.

One popular opamp architecture is a two-stage Miller-compensation opamp which has been utilized for the first, second and third integrator and opamp4 and is shown in Figure 7. A PMOS input differential pair is used as the input stage for two reasons: First, the second pole is determined by the transconductance of the input transistors of the second stage and the NMOS transistor is faster than the PMOS one therefore the whole opamp will be more stable. Second, the input and output common mode voltage of the opamp is set to be 0.8V instead of VDD/2 (0.9V). The tail transistor in the first stage will have more VDS voltage and will not be pushed to triode region. The benefit of using PMOS transistors as input in the differential pair is low flicker noise, but in our wideband design, the flicker noise is of less concern.

This modulator requires two ADCs. The first ADC has 5bit resolution and 31 comparators and the second ADC has 4bit resolution and 15 comparators. As shown in Figure 8, each latched comparator is composed of a single preamplifier stage and a latch. The preamplifier is used to amplify the input signal and to minimize the input capacitance of the comparator. The preamplifier stage isolates the latch and the resistor ladder; therefore it reduces the kick-back noise seen in reference string during switching times of the comparator. The latch is used to compare the two amplified input signals comping from the preamplifier and to provide a digital rail-to-rail output signal.

The whole CTTI ΔΣ modulator has been simulated with a $F_{in} = 1.005MHz$ input frequency, $1.6V_{pp}$ (-2dBFS) amplitude and 320MHz sampling rate across process corners and temperatures. Due to the excessive long simulation times, these circuit simulation results were obtained by using only 16384-point FFTs. Since the signal bandwidth is 10MHz, up to 512 frequency bins will be included in the

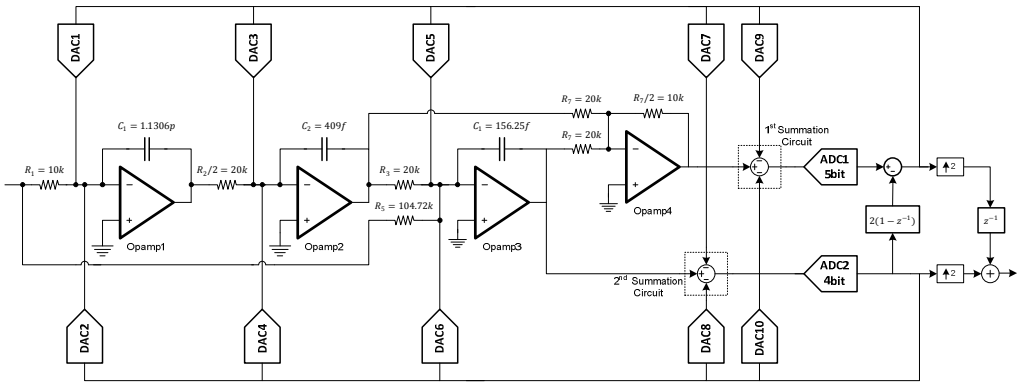
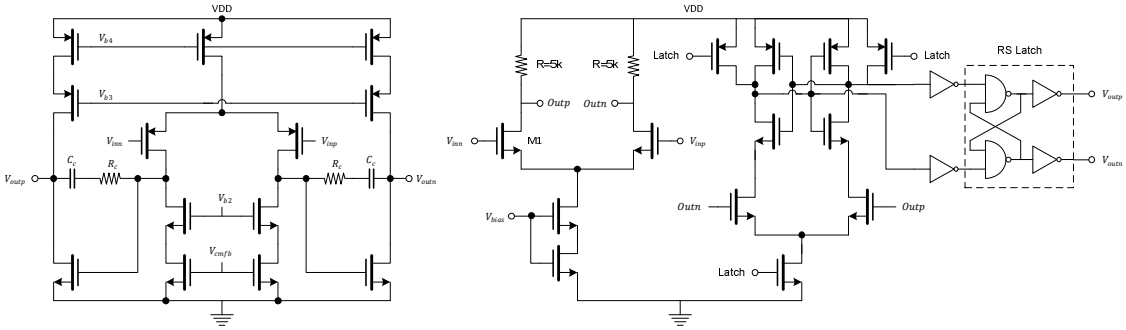


Figure 6. Block Diagram of the 3rd-order CTTI ΔΣ Modulator.



(a) (b)

Figure 7. Schematic of (a) opamp and (b) comparator of the 3rd-order CTTI ΔΣ Modulator.

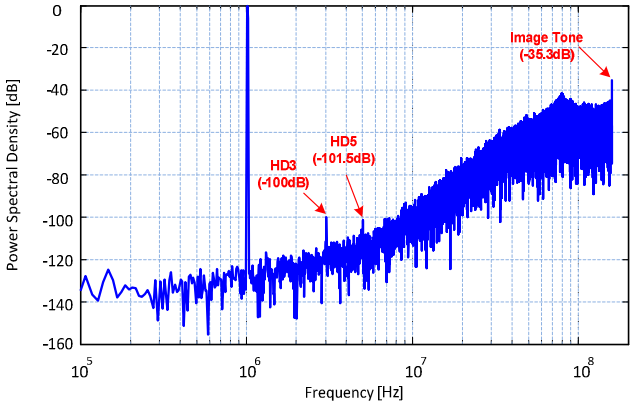


Figure 8. The output spectra of the CTTI ΔΣ modulator for a 1.005MHz input with clock frequencies of 320MHz simulated in TT corner and 27'C.

calculation of the SNDR. The circuit-level simulations have been run to make sure that the modulator is stable across process corners and temperatures. The SNDR of the modulator obtained from circuit simulations in TT 27'C, FF 120'C and SS -40'C are 75.3dB, 75.9dB and 74.5dB respectively.

The output spectrum obtained from the circuit simulation at TT corner and 27'C temperature is shown in Figure 8. From the output spectrum shown in Figure 8, it can be seen that big tones reside at around the half clock frequency (160MHz). Those tones are images and are created due to utilizing the time-interleaving technique in the modulator. Those tones are dangerous because they will fold the out-of-band noise into the band of interest and hence increase the in-band noise floor. The image tone located at $0.5F_{clk} - F_{in}$ has -35.3dB amplitude and should be attenuated enough in the decimation filter following this modulator.

V. Conclusion

In this paper the design of a 3rd-order CTTI ΔΣ modulator with one set of integrators in 90nm CMOS technology has been presented. A novel method to resolve the delayless feedback path issue has been proposed [9]. The results obtained from the circuit simulation confirm that the theory behind the proposed method works very well without any degradation in the output performance.

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