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The Design of Low Complexity Low Power Pipelined Short Length Winograd Fourier Transforms

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***Abstract*— In this paper a novel pipelining approach applicable to Winograd Fourier transforms is presented. The novel approach makes use of reconfigurable multiplier blocks to implement the real multipliers required for the transform as well as sharing the hardware resources among additions. The additions are realized using modified forms of butterfly circuits. The novel approach is tested on a 5-point Winograd Fourier transform and the circuit area and power dissipation of the design are estimated using an in-house power estimation tool and compared to the state-of-the-art approaches.**

I. Introduction

Winograd Fourier Transform (WFT) [1] algorithm is highly preferable in designs that involves Discrete Fourier Transform (DFT). Twiddle factor multiplication is not required for WFT, which in turn reduces the number of real multipliers needed. Because multipliers are more resource demanding than other circuit components, WFT is regarded as a power efficient transform covering a smaller circuit area. Especially WFTs with blocklengths of 2, 3, 5, 7, 8, 9 and 16 are widely used in Digital Signal Processing (DSP) applications, the details of which can be found in [7],[6].

It is possible to pipeline several short length WFTs to generate transforms of larger sizes [2], [3]. However, realizing a pipelined structure for short length WFTs is difficult due to the irregularity in the flow of the signal within these transforms. In the next section we will give more details on WFT and present our novel approach on a 5-point WFT.

II. Winograd Fourier Transform Algorithm

The WFT [1] algorithm allows the DFT matrix

$$\mathbf{W} = \begin{bmatrix} 1 & 1 & 1 & 1 & \cdots & 1 \\ 1 & \omega & \omega^2 & \omega^3 & \cdots & \omega^{N-1} \\ 1 & \omega^2 & \omega^4 & \omega^6 & \cdots & \omega^{2(N-1)} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & \omega^{(N-1)} & \omega^{2(N-1)} & \omega^{3(N-1)} & \cdots & \omega^{(N-1)^2} \end{bmatrix} \tag{1}$$

of size $N\times N$ to be decomposed into three matrices as follows

$$\mathbf{W} = \mathbf{S}_1 \times \mathbf{M} \times \mathbf{S}_2, \tag{2}$$

where $\omega = e^{-\frac{j2\pi}{N}}$, $\mathbf{S}_1$ and $\mathbf{S}_2$ are of size $N\times M$ and $M\times N$ and composed of only $-1, 0$ and 1. $\mathbf{M}$ is a $M\times M$ diagonal matrix being composed of either purely real or purely imaginary numbers. For $N = 5$, which is taken as the reference design for this paper,

$$\mathbf{S}_1 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & -1 & 0 & -1 & 1 \\ 1 & -1 & 1 & -1 & 1 & 0 \\ 1 & -1 & 1 & 1 & -1 & 0 \\ 1 & -1 & -1 & 0 & 1 & -1 \end{bmatrix}, \mathbf{S}_2 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & -1 & -1 & 1 \\ 0 & 1 & 0 & 0 & -1 \\ 0 & 1 & 1 & -1 & -1 \\ 0 & 0 & 1 & -1 & 0 \end{bmatrix} \tag{3}$$

and

$$\begin{aligned} \mathbf{M} &= diag[\ m_0,\ \ m_1,\ \ m_2,\ \ m_3,\ \ m_4,\ \ m_5\ ] \\ &= diag[\ 1,\ \ 1 - \frac{\cos(u) + \cos(2u)}{2},\ \ \frac{\cos(2u) - \cos(u)}{2}, \\ & j(\sin(u) + \sin(2u)),\ \ j(\sin(u)),\ \ j(\sin(u) - \sin(2u))], \end{aligned} \tag{4}$$

where $diag[m_0, ..., m_M]$ represents a diagonal matrix, m_i, for $i = 0, .., M$, being its diagonal components and $u = 2\pi/5$. Matrix $\mathbf{W}$ is used to obtain $\mathbf{X} = \mathbf{W}\mathbf{x}$, where $\mathbf{x} = [x_0,\ x_1,\ x_2,\ x_4,\ x_3]^T$ is the data samples. Please note here that both $\mathbf{x}$ and $\mathbf{X}$ are not in their natural order, which can easily be arranged by designing the address generators to pick the right locations at the input and the output buffer for the 5-point WFT.

The top plot in Fig.1 shows the signal flow graph for 5-point WFT given in (3) and (4). Stages 1 to 3, Stage 4 and Stage 5 to 7 are to implement operations required by $\mathbf{S_2}$, $\mathbf{M}$ and $\mathbf{S_1}$ respectively. Here the components of vector $\mathbf{x}$ is applied to the system all in parallel. However, this is just the representation and in fact the samples are assumed to arrive sequentially. The black triangles (▶) indicate multiplications by constants. The black dots (•) are the additions. As can be seen for 5-point WFT 17 complex additions and 5 real-by-complex multiplications are needed if the data samples vector

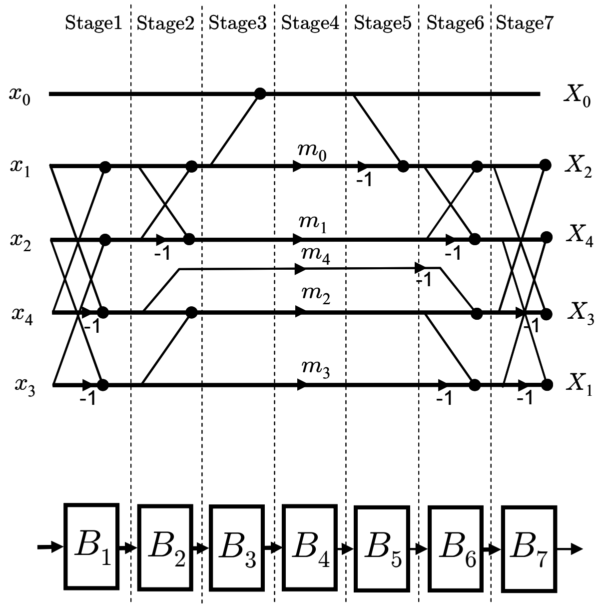


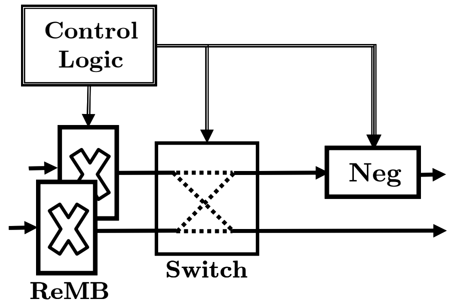
Fig. 1. The plot on the top is the signal flow graph for 5-point WFT and the plot on the bottom is the representation of our pipelined design with seven stages.

$\mathbf{x}$ is complex. Pay attention to the irregularity in this graph, which avoids a pipelined design to be deployed straightaway. In [5] the structure of the 5-point WFT has been modified in order to set the symmetry in its signal flow graph. However, this modification brought the need for complex-by-complex multiplications in the multiplier stage (i.e. Stage 4 in Fig.1), which of course increases the complexity of the structure. In our design given in the following section the pipelining is introduced to the WFT without modifying its signal flow graph.

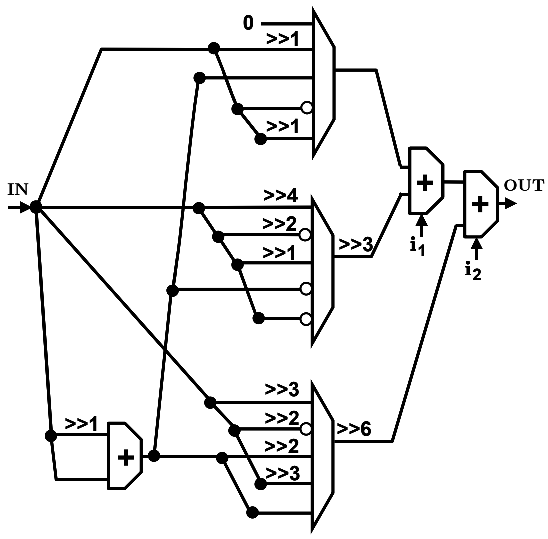
III. Pipelined 5-point WFT

Our design is a 7-stage pipelined architecture $(B_1, B_2, \ldots, B_7)$, which is depicted in the plot at the bottom of in Fig.1. What stage of the pipelined architecture corresponds to which part of the 5-point WFT signal flow graph is clearly shown in Fig.1 with vertical dashed lines. It is pipelined and the components of $\mathbf{x}$ are fed sequentially into the pipelined circuit in the same order that $\mathbf{x}$ is formed. There are two types of components comprising the structure of the novel design. The Reconfigurable Multiplier Block (ReMB) [8] and modified butterfly circuits.

Designing the ReMB: In Fig.1, B_4 is the stage where the multiplications take place. Therefore, it corresponds to the operations required by the diagonal matrix $\mathbf{M}$. As the data samples fed into the pipelined structure sequentially, B_4 should be capable of performing one distinct multiplication at a time instance. This can be achieved using a ReMB [9], [10]. Here we assume each data sample is quantized using 11 bits (2 being integer and 9 for fractional bits). From their



(a)



(b)

Fig. 2. (a) The structure of the circuit that implements operations required by $\mathbf{M}$ (b) The ReMB which implements the multiplication with the coefficients $m_1, ..., m_5$.

Canonical Signed Digit (CSD) representations, each multiplication coefficient, i.e. $m_1, ..., m_5$, can be implemented using the ReMB given in Fig.2(b). Fig.2(b) is composed of 3 adders and 3 multiplexers, each having 5 inputs. The order of the inputs to each multiplexer is set in accordance with the order of the multiplication coefficients used for the 5-point WFT. For example; if m_1 is to be implemented, the first inputs for all three multiplexers should be activated. Carry-in inputs i_1 and i_2 are selected based on if the adder is to be implemented as a subtractor or not. As can be seen, some inputs to the multiplexers are inverted right before multiplexing. This also serves the need for the use of a subtractor in generating multiplications. The symbol $>>$ represents hard-wired shift operation with the value following this sign showing how many shifts are needed. Each shift operation in Fig.2(b) belongs to the branch that goes right below them.

Due to multiplication with complex signals, two ReMBs are needed, one for the real and the second for the imaginary part of the incoming complex signal. Fig.2(a) shows two ReMBs, the internal architectures of which are given in Fig.2(b). The

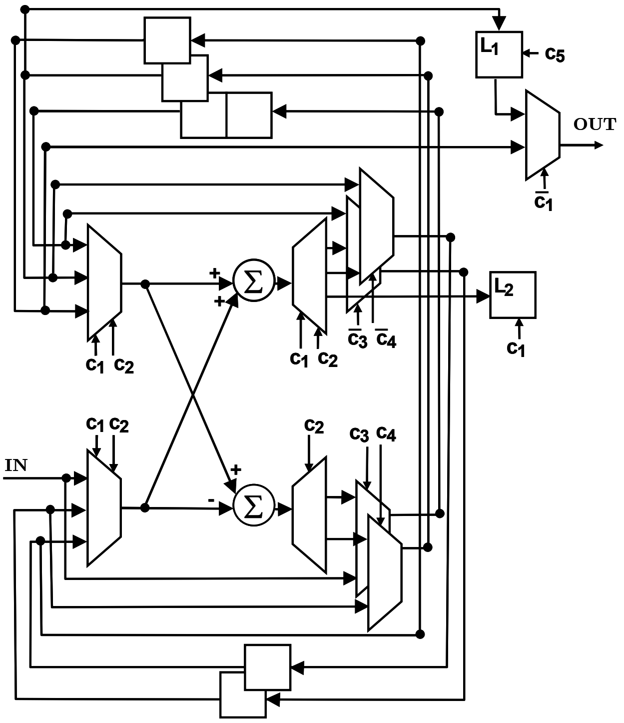


Fig. 3. Butterfly circuit that implements the additions required by matrix $\mathbf{S_1}$

rest of Fig.2(a) is the negator and a 2x2 switch, which are needed due to the multiplication with j as required in (4), for m_3, m_4 and m_5. For the other two multiplication coefficients these two components are deactivated by the control logic, which also provides the control signals and carry-in values for each one of the ReMBs.

Modified butterfly circuit: The first three stages in Fig.1 implements the operations needed by $\mathbf{S_2}$, where there are 3 full and 2 half butterfly circuits (i.e. 5 butterfly operations). It is in fact possible to accommodate only one butterfly circuit and perform all of the 5 operations making use of this single butterfly circuit, which will save a lot of hardware as this will get rid of most of the adders and subtractors needed. Because it is a 5 point Fourier transform, all of the 5 butterfly operations will be accomplished within the duration of the transform without causing any delays. Fig.3 shows the modified butterfly circuit, being composed of an adder and a subtractor, along with several multiplexers and registers to operate the processed signals inside the processing element. The square-shaped components are registers and where concatenated they represent shift-registers. These registers are assumed to be enabled at every clock signal. On the other hand the latches L_1 and L_2 are enabled on when control signals c_5 and c_6 are active.

To operate the whole system synchronously, a 3-bit counter is required that counts from 001 to 101 bit-wise. The control signals needed to operate the system in Fig.3 are given in Table I. In total of 6 signals are needed and Table I shows which of these control signals are active at which counter instance.

The solution for the modification of a butterfly circuit is summarized in Fig.4. The modified butterfly circuit has two

TABLE I

CONTROL SIGNALS IN THE PIPELINED 5-POINT WFT CIRCUIT

Counter Value	Control Signals that are active
001	c_2, c_3
010	c_1, c_3, c_4
011	c_2, c_3, c_5
100	c_4
101	c_4

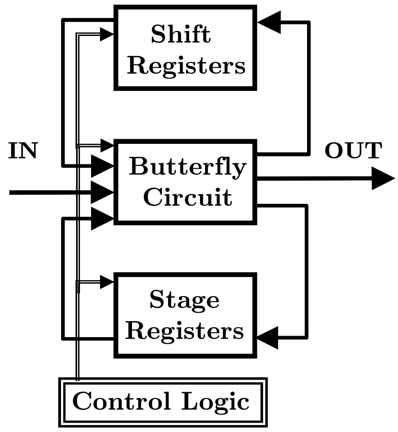


Fig. 4. The structure of the modified butterfly circuit that is designed to merge several stages within a WFT. Three of these circuits are needed to realize a 5-point WFT.

sets of registers, one that coordinates the butterfly operations (shown as *shift registers* in Fig.4) and the other guides the samples from one stage to the next stage in the signal flow graph (named *shift registers* in Fig.4). The maximum number of stage registers is equal to the number of stages that are combined under one modified butterfly circuit. Due to the irregularity of the WFT, extra multiplexers and registers/latches are required in addition to the components depicted in Fig.4. The timing is under the control of the control logic same as Fig.2(a).

One butterfly circuit is enough to implement stages B_5 and B_6, which is in similar structure shown in Fig.4. Note that these two stages need for 4 butterfly operations (1 full and 3 half butterfly operations), which justifies the use of only one butterfly circuit to realize B_5 and B_6. We leave it to the reader to derive the lay-out of this modified butterfly circuit. A conventional butterfly circuit without any modifications would be enough to implement the last stage.

IV. COMPARATIVE STUDY

In order to understand the possible savings with the use of our novel approach, in terms of both power dissipation and circuit area, we have implemented several approaches from the literature to realize a 5-point WFT by using an in-house cost estimation tool and created the content for Table II. Power dissipation for the designed circuits are estimated in mW and the circuits area is in terms of gates. Power dissipation

TABLE II

COMPARISON OF APPROACHES FOR IMPLEMENTING 5-POINT WFT

Approach	Power Dissipation (mW)	Circuit Area (gates)
WFT	5.69	35.46k
KolbaWFT	5.45	33.87k
MlessWFT	4.58	20.74k
RegWFT	7.71	18.90k
PipelinedWFT	3.67	7.70k

has been evaluated considering the activation rate of each processing component in the circuit individually.

In Table II, WFT is the straightforward implementation of the 5-point Winograd Fourier transform. This structure is still in use [11],[12] and needs for 5 multipliers. Kolba and Park's design [3] (which we name KolbaWFT) on the other hand needs for only 4 multipliers and a shift operation. Therefore, it is less complex. Rather than using general purpose multipliers, a multiplierless approach may also be accommodated, as suggested in [13], because of the fact that the coefficients for the multiplication is fixed. This approach appears as MlessWFTA in Table II. The savings if a multiplierless approach is obvious over the conventional approaches.

Pipelining the 5-point WFT using the approach in [5] (which appears as RegWFT in Table II, named with respect to the regularity that is with the signal flow graph) would of course decrease size of the circuit as the components are re-used by making use of butterfly circuits. However, the power dissipation of this circuit would be huge as the butterfly circuits will consume too much power along with many registers and multiplexers. That is in fact why our approach both reduced the size of the circuit and decreased the power consumed at the same time. Our approach, as we named it PipelinedWFT in Table II, appears to have a superiority over the other conventional methods.

V. CONCLUSION AND FUTURE WORK

In this paper a novel approach to pipeline the structure the 5-point WFT is shown. The novel approach makes use of ReMB and the rest of the circuit utilizes only 3 complex adders and 3 complex subtractors with several registers and multiplexers attached to the design. The ReMB itself is composed of 3 multiplexers and 3 real adders only. The savings over the approaches taken from the open literature is obvious. We have employed an in-house design tool to estimate the cost of the novel approach. We have observed that the novel approach consumes lower power and occupies a smaller area on the circuit compared to other possible solutions to realize a 5-point WFT circuit. The work we have presented here can be expanded to WFTs with different sizes and a generalized approach applicable to all WFT sizes can be proposed, which will be aimed at a later study. Although we have implemented the circuit on FPGA, the realization of the circuit on a real life chip solution is also aimed as later research objective.

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