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Raghav, H., Bartlett, V. and Kale, I.

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Energy Efficiency of 2-Step Charging Power-Clock for Adiabatic Logic

Himadri Singh Raghav, Vivian A. Bartlett and Izzet Kale
Applied DSP and VLSI Research Group, Department of Engineering
University of Westminster

Email: himadri.s.rahav@my.westminster.ac.uk, {v.bartlett, kalei}@westminster.ac.uk

Abstract—The generation of power-clocks in adiabatic integrated circuits is investigated. Specifically, we consider the energy efficiency of a 2-step charging strategy based on a single tank-capacitor circuit. We have investigated the impact of various parameters such as tank-capacitance to load capacitance ratio, ramping time, transistors sizing and power supply voltage scaling on energy recovery achievable in the 2-step charging circuit. We show that energy recovery achievable depends on the tank-capacitor and load capacitor size concluding that tank-capacitance (C_T) versus load capacitance (C_L) is the significant parameter. We also show that the energy performance depends on the ramping time and improves for higher ramping times (lower frequencies). Energy recovery also improves if the transistors sizes in the step charging circuit are sized at their minimum dimensions. Lastly, we show that energy recovery decreases as the power supply voltage is scaled down. Specifically, the decrease in the energy recovery with decreasing power supply is significant for lower ramping times (higher frequencies). We propose that a C_T/C_L ratio of 10, keeping the width of the transistors in the step charging circuit minimum, can be chosen as a convenient ‘rule-of-thumb’ in practical designs.

Keywords—power-clocks; adiabatic circuits; stepwise charging; tank-capacitor; energy recovery; ramping time

I. INTRODUCTION

Adiabatic circuit techniques are known to have the potential to achieve energy efficient operation [1]–[8]. Adiabatic circuits operate using a slowly changing combined power-supply and clock the so-called “power-clock” of a form allowing approximately constant current charging/discharging. This eliminates current surges, thereby reducing the energy dissipated as heat. The use of a power-clock also makes possible the recovery of charge, enabling energy to be recycled [9]–[13]. To produce approximately constant current charging/discharging, the power-clock should ideally be a voltage ramp which rises and falls linearly. Such a ramp can be approximated using resonant inductor circuits [14]–[17] and step charging circuits [18], [19]. The use of inductors presents a problem with on-chip integration; therefore, step charging circuits suggest a more promising solution. Such a power-clock which is an approximation of an ideal ramp is shown simplified in Fig. 1 [19].

There are several papers, in literature that addressed the design of step charging circuits for adiabatic charging and discharging of the capacitive load. Mostly, the consideration is given to circuit topology, step charging waveform generation and the stability of the step charging circuits [20]–[26]. Most of the papers in the literature suggest that stability of the step

charging circuit can be ensured if the tank-capacitor value is much larger compared to the load capacitor.

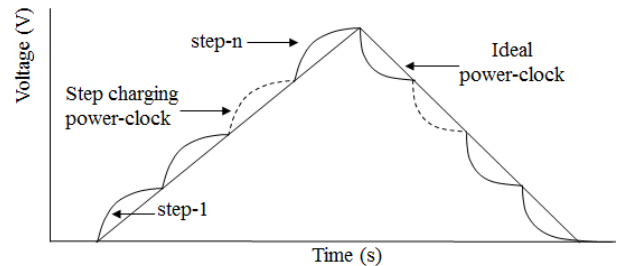


Fig. 1. An approximation of an ideal ramp using n-step charging power-clock.

The authors in [20] have presented a step charging circuit which is independent of the tank-capacitor topology that generates the step charging waveform. However, the ratio of the tank-capacitors to load capacitor used in the step charging circuit is 270. In [21] and [22] the authors have discussed the stability of a step charging circuit which uses tank-capacitors connected in the series. However, the ratio of the tank-capacitors to load capacitor used in the step charging circuit is 750 which is quite big and therefore will consume a large silicon area. In [23] a step charging circuit with an equalizing capacitor that equalizes the node voltages of the tank-capacitors by connecting “touching” them with the equalizing capacitor is presented. The stability of the step charging circuit is also investigated by changing the order in which the tank-capacitor nodes were connected “touched” [23] with the equalizing capacitor. However, the ratio between tank-capacitors and the equalizing capacitor used in the step charging circuit is 300. The authors in [24] have presented a step charging circuit and the stability of the step charging circuit is considered. It has been mentioned in the paper that the step charging circuit stays stable even if the value of the load capacitor changes significantly when the size of the tank-capacitor is much larger than the load capacitor. However, nothing has been mentioned about how large the size of the tank-capacitance should be in comparison to the load capacitance in order to ensure stability of the step charging circuit. In [25] and [26] the adiabatic stepwise charging and discharging of a capacitor with an inductor current that controlled the switching transistors was demonstrated experimentally and the power consumption was investigated as the function of the number of steps.

So far all the above cited references work around using large tank-capacitor values for stability. Large tank-capacitors

incur high silicon area cost and presents with the difficulty of on-chip integration. This can be a problem for the applications that require low power operation and have area constraint. Therefore, it is worth investigating what should be the relationship of total tank-capacitance to load capacitance that can deliver potential energy benefits with lower silicon area cost and ensure stable operation.

Also, the important considerations that have been found to be missing in all of the above mentioned papers are; i) the energy recovery achievable in the step charging circuits and ii) what should be the ratio of tank-capacitance to load capacitance, which can deliver potential energy benefits. iii) the impact of ramping time on the energy recovery of the step charging circuit. iv) The impact of transistors sizing on the energy recovery of the step charging circuit and v) The impact of power supply voltage scaling on the energy recovery of the step charging circuit.

Energy recovery determines the efficiency of the adiabatic circuits, therefore an important parameter to be considered for the design of adiabatic circuits. In adiabatic circuits, the step charging power-clock makes possible the recycling of charge, enabling energy to be recovered. Thus it is important to study the factors that decide the energy recovery achievable in step charging circuits.

The energy performance of the adiabatic circuits is additionally a function of ramping time. Therefore, it would be worth looking if increasing the ramping time of the step charging circuit influences the percentage energy recovery achievable in step charging circuit.

In a step charging circuit pMOS transistor is used for charging the load capacitor from the power supply, CMOS transmission gates (TG) are used for the charging/discharging of the load capacitor to/from tank-capacitor and an nMOS transistor is used to discharge the load capacitor to the ground. Sizing of these transistors used as switches can affect the charging/discharging of the load capacitor and in turn affect the energy recovery achievable in step charging circuits specifically at lower ramping times (high frequency). Therefore, it would be worth investigating that what should be the transistor sizes in the step charging circuit that can deliver potential energy benefits and how transistor sizing influences the energy recovery achievable in the step charging circuits at different ramping times.

An easy and powerful way to reduce losses in static CMOS is by reducing the power supply voltage, V_{DD} . It is because of the quadratic dependence of the energy dissipation on the V_{DD} due to dynamic losses.

$$E_{CMOS} \propto V_{DD}^2 \quad (1)$$

Energy dissipation in adiabatic circuits is also proportional to the square of the supply voltage.

$$E_{ADIABATIC} = (2RC_L/T)C_L V_{DD}^2 \quad (2)$$

Thus energy dissipation reduces as the supply voltage is scaled down. With the decrease in supply voltage, energy supplied to the circuit will also decrease. Energy recovery, E_R in an adiabatic circuit can be defined as the portion of the energy supplied to the circuit that can be recovered from the

circuit and can be reused for the subsequent cycles. It is calculated as the difference of energy supplied, E_S and energy dissipation, E_D ;

$$E_R = E_S - E_D \quad (3)$$

And the percentage energy recovery is calculated as:

$$E_R = (E_R / E_S) \times 100 \quad (4)$$

For low power operation, it is worth investigating that how power supply voltage scaling influences the energy recovery achievable in the step charging circuits.

In this paper we have defined a new metric called “ C_T/C_L ratio” which denotes the ratio of tank-capacitance to load capacitance. Simulations were performed to investigate the appropriate ratio of tank-capacitance to load capacitance which can deliver potential energy benefits in 2-step charging circuit based on tank-capacitor circuit. Simulations were performed for two cases; i) C_T/C_L ratio when C_L is fixed and C_T is varied; ii) C_T/C_L ratio when C_T is fixed and C_L is varied. Simulations were also performed to investigate if ramping time, sizing of the CMOS transmission gate (TG) and the power supply voltage scaling influence the energy recovery achievable in the step charging circuit.

The work presented in this paper has not been compared with any of the previously mentioned references[20]-[26] because none of the above mentioned references considered and reported results relating to energy recovery for their step charging circuits. Also no discussion about the appropriate ratio of tank-capacitance to load capacitance, impact of ramping time, transistor sizing and power supply voltage scaling was mentioned in any of the above cited references. To the author’s best knowledge this is a first in this area. This paper is organized as follows; In section II, the step charging circuit is discussed. In section III, simulation results are discussed. The paper is concluded in section IV.

II. STEP CHARGING CIRCUIT

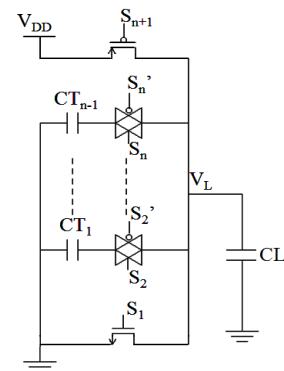


Fig. 2. n-step charging circuit [19].

In n-step charging as shown in Fig. 2, the load capacitor is charged from 0 to V_{DD}/n , under the constant voltage, V_{DD}/n then from V_{DD}/n to $2V_{DD}/n$, under the constant voltage, $2V_{DD}/n$ and finally from $(n-1)V_{DD}/n$ to V_{DD} under V_{DD} . This implies that supply, V_{DD} , charges the load capacitance from $(n-1)V_{DD}/n$ to V_{DD} instead of charging from 0 to V_{DD} . Therefore, the

current from the supply to the load capacitance is reduced to $1/n$ of that of a conventional case, which means that the energy from the V_{DD} supply is decreased to $1/n$.

The energy dissipation in a step charging circuit depends on the number of steps, n . Each step, in a step charging circuit dissipates $C_L V_{DD}^2 / 2n^2$ Joules of energy, assuming all the voltage steps are equal. Thus, the total energy dissipated in a circuit powered by a stepwise charging circuit is given by the expression below:

$$E_D = nE_{\text{step}} = C_L V_{DD}^2 / 2n \quad (5)$$

Where, $E_{\text{step}} = C_L V_{DD}^2 / 2n^2$ and n is the number of steps. The above expression illustrates that the energy dissipation is reduced to $1/n$ in n -step charging compared to the conventional direct charging. The conventional direct charging corresponds to $n=1$. This means a 2-step charging circuit ($n=2$) saves 50% of the energy compared to the conventional case.

III. SIMULATION RESULTS

A 2-step charging circuit driving a capacitive load, C_L using a single tank-capacitor is shown in Fig. 3(a). Each switch is momentarily closed in the sequence $S_1, S_2, S_3, S_2, S_1, \dots$ under the control of a Finite State Machine (FSM). In steady state, this produces a step-like waveform as shown in Fig. 3(b).

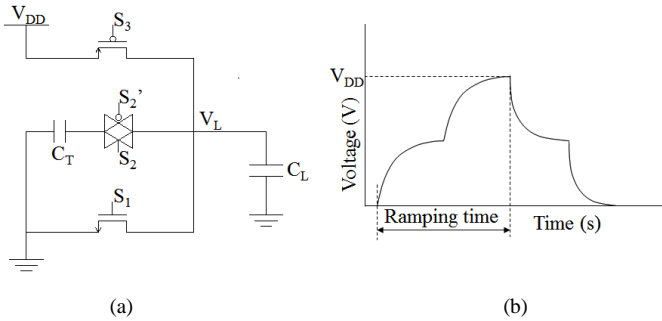


Fig. 3. (a) a 2-step charging circuit [19] (b) 2-step charging output waveform.

In Fig. 3(a), the pMOS switch, S_3 , is used for charging the load capacitor, C_L , to V_{DD} and the nMOS switch, S_1 , is used for discharging C_L to Gnd. A CMOS TG is used for charging/discharging C_L to the intermediate voltage stored on the tank- capacitor, C_T . For our investigations, a TSMC 180nm CMOS process was used and all the transistors were sized at minimum dimensions ($W_{\min}=220\text{nm}$, $L_{\min}=180\text{nm}$) except for the width of the pMOS switch to V_{DD} which was sized at 440nm , in an attempt to equalise its performance with respect to the nMOS switch S_1 .

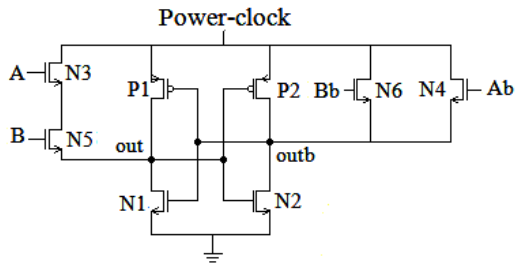


Fig. 4. Test circuit: PFAL Adiabatic AND/NAND gate [27].

To measure the energy recovery achievable, a 2-input Positive Feedback Adiabatic Logic [27] AND/NAND gate as shown in Fig. 4 was used as the test circuit of Fig. 5. The PFAL adiabatic AND/NAND gate was chosen for this study because amongst the most energy efficient quasi-adiabatic logics such as Efficient Charge Recovery Logic, ECRL [28],[29], Improved Efficient Charge Recovery Logic, IECRL [30],[31] and Positive Feedback Adiabatic Logic, PFAL, the PFAL adiabatic logic exhibits the most energy efficient operation as can be observed from the table 1.

TABLE I. COMPARISON OF ENERGY CONSUMPTION OF ENERGY EFFICIENT ADIABATIC LOGIC FAMILIES

Logic Gates	Energy Consumption (fJ) @ Load 10fF		
	ECRL	IECRL	PFAL
NOT/BUF	19.31	10.31	7.37
AND/NAND	21.04	17.65	13.24
NOR/OR	20.80	17.58	13.20
XOR/XNOR	21.62	21.08	17.03

These simulations were performed using TSMC 180nm CMOS process at 1.8V power supply. The load capacitance was chosen as 10fF and all the transistors for each gate in each of the adiabatic logic family were sized at minimum dimensions ($W_{\min}=220\text{nm}$, $L_{\min}=180\text{nm}$).

The point worth noting is that the simulations for above table have been performed using a trapezoidal power-clock, because the aim was to choose the most energy efficient adiabatic logic family which can later on be used as a test circuit for the investigation of energy efficiency of the 2-step charging circuit.

Another point worth noting is that adiabatic logic families uses different number of phases for instance, single, two, four and eight phases. These phases are required in the case where cascading of the gates is done for example, PFAL adiabatic logic gates use four phase power-clocking scheme when used in the cascade manner for realising a complex design. For using a single PFAL adiabatic logic gate as a test circuit, single phase power-clock is required.

For calculating the energy efficiency of the 2-step charging power-clock all transistors of the test circuit were sized at minimum dimensions ($W_{\min}=220\text{nm}$, $L_{\min}=180\text{nm}$). The power-clock generator comprises the 2-step charging circuit of Fig. 3(a) together with its FSM. Fig. 5 shows this generator driving the test circuit.

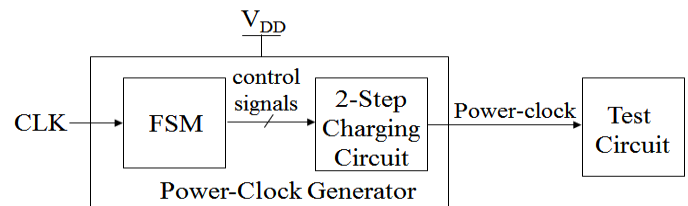


Fig. 5. General block diagram of an Adiabatic System.

Simulations were carried out in a ‘typical-typical’ process corner using the CMOS process mentioned above at 1.8V power supply. The tank-capacitor of the 2-step charging circuit of Fig. 3(a) requires a few cycles to settle. For this reason, all measurements were taken after the circuit had reached steady state. All the simulations were performed with equal L-H (Low-to-High) and H-L (High-to-Low) ramping times of 10ns, 25ns, 50ns, 100ns, 200ns and 400ns.

A. Energy recovery Vs C_T/C_L ratio (for fixed C_L and varying C_T) at different ramping times.

Energy recovery achievable at various tank-capacitor to load capacitor (C_T/C_L) ratios (for fixed C_L at 1pF and varying C_T) was measured at different ramping times of 10ns, 25ns, 50ns, 100ns, 200ns and 400ns. The simulation results shown in Fig. 6 illustrate the relationship between C_T/C_L ratio and percentage energy recovery at different ramping times. The plot shows the “diminishing returns” of increasing C_T/C_L ratio. The “knee” of the curve occurs at around the $C_T/C_L = 10$ region and increasing the C_T/C_L ratio above 10, offers relatively little improvement (less than 1%) in energy recovery in each case. This suggests that as a design rule, a C_T/C_L ratio of 10 is appropriate.

From Fig. 6 it can also be observed that if we use the C_T/C_L ratio of 270, 300 and 750 as used in the references [18], [19]-[20] and [21] respectively there will not be any significant improvement in the energy recovery.

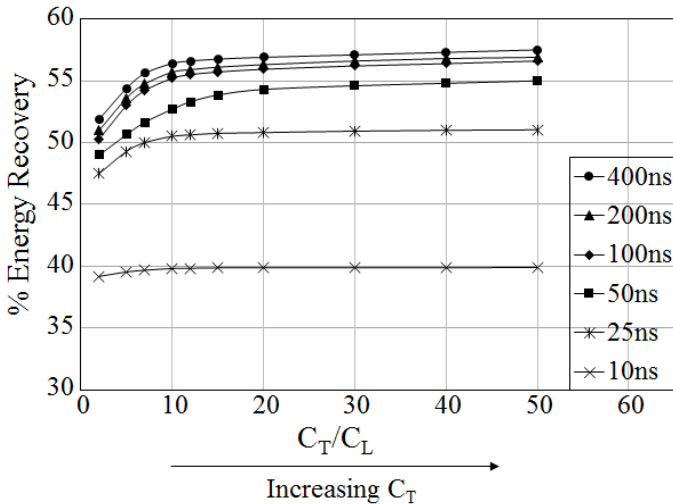


Fig. 6. Energy Recovery Vs C_T/C_L ratio (fixed C_L and varying C_T) at different ramping times.

Energy performance of adiabatic circuits is additionally a function of ramping time. Fig. 6 also compares energy recovery achievable by 2-step charging circuits at ramping times of 10ns, 25ns, 50ns, 100ns, 200ns and 400ns.

The ramping time is varied from 10ns to 400ns and not below 10ns; it is because the potential energy benefits of the adiabatic circuits can be obtained at low frequencies i.e. at higher ramping times as the adiabatic logic is a function of

ramping time as depicted by the equation 1. Moreover, they are used for ultra-low power applications where speed is not the major concern.

Fig. 6 shows that as the ramping time is increased above 100ns, the improvement in energy recovery is relatively small. But as the ramping time is reduced from 50ns to 10ns there is a significant decrement in energy recovery. This can be illustrated from equation 2 where it can be observed that if the ramping time, T is reduced the energy dissipation increases which causes energy recovery to decrease thus adiabatic losses dominates the energy dissipation at lower ramping times (higher speed) and the energy recovery decreases.

Also, as in this paper a PFAL adiabatic AND/NAND gate was used as the test circuit because we intended to investigate the energy efficiency of the 2-step charging circuit. If in place of AND/NAND gate a more complex design using any adiabatic logic family which requires single phase power-clock is used, then same 2-step charging circuit can be used and the value of the tank-capacitance C_T , can be adjusted according to the load capacitance, to make the C_T/C_L ratio of 10.

If in case, an adiabatic logic family which requires a two phase power-clocking scheme is used, a two phase 2step charging power clock generator will be required. For implementing a two phase 2step charging power-clock generator, two 2 step charging circuits will be used and the phases will be generated by the FSM controller. The values of the tank-capacitor in the two 2-step charging circuits can be adjusted according to the load capacitances each power-clock is driving to make the C_T/C_L ratio of 10.

Similarly, if a four phase adiabatic logic family is used, 4 2-step charging circuits will be used and their phases will be generated using the FSM controllers. The values of the tank-capacitor in the 4 2-step charging circuits will be adjusted according to the load capacitance each power-clock drives.

By using the C_T/C_L ratio of 10 in each of the above mentioned cases the expected energy recovery would be the same.

In these results the energy cost of operating the switches in the 2-step charging circuit/FSM controller has not been included. It is because in a big design with a significant adiabatic core, these are largely fixed overheads and will become a relatively insignificant factor in energy performance of the whole circuit.

B. Energy recovery Vs C_T/C_L ratio (for fixed C_T and varying C_L) at different ramping times.

Next, energy recovery achievable at various C_T/C_L ratios (for fixed C_T at 10pF and varying C_L) was measured at ramping times of 10ns, 25ns, 50ns, 100ns, 200ns and 400ns. The simulation results shown in Fig. 7 illustrate the relationship between C_T/C_L ratio and the percentage energy recovery at different ramping times. The plot shows that at C_T/C_L ratio of 1, 2 and 5 the energy recovery is small in comparison to the energy recovery at C_T/C_L ratio above 5. This is because the value of the C_L at C_T/C_L ratio of 1, 2, and 5 is 10pF, 5pF and 2Pf respectively. The large values of the C_L increases the time constant of the circuit at the output node

thus, preventing the output voltage of the step charging circuit to reach V_{DD} .

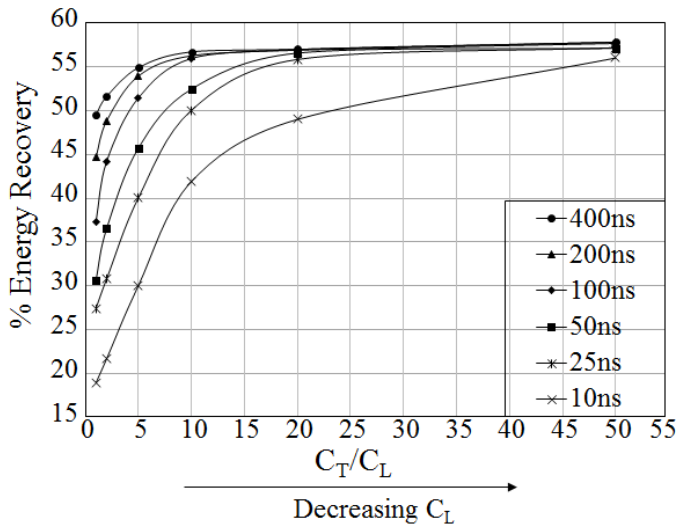


Fig. 7. Energy Recovery Vs C_T/C_L ratio (fixed C_T and varying C_L) at different ramping times.

There is no significant improvement in the energy recovery for the C_T/C_L ratio above 10 at the ramping times of 50ns, 100ns, 200ns and 400ns, whereas there is an improvement of about 12% and 6% approximately in the percentage energy recovery for the C_T/C_L ratio above 10 at the ramping times of 10ns and 25ns respectively. This is because as the value of C_L decreases the percentage energy recovery improves irrespective of the ramping time, because the time constant of the circuit at the output node becomes less than or equal to the ramping time.

Fig. 7 also compares energy recovery achievable by 2-step charging circuit at ramping times of 10ns, 25ns, 50ns, 100ns, 200ns and 400ns. It shows that as the ramping time is increased above 100ns, the improvement in energy recovery is relatively small. But as the ramping time is reduced from 50ns to 10ns there is a significant decrement in the percentage energy recovery at lower C_T/C_L ratio. There is no significant decrease for the energy recovery at C_T/C_L ratio of '50' for all the ramping times. This is because at C_T/C_L ratio of '50' the value of the load capacitance, C_L , is .2pF, this makes the time constant of the circuit at the output node less than or equal to the ramping time. Thus, percentage energy recovery improves irrespective of the ramping times.

C. Energy recovery Vs Ramping time at different TG widths

Simulations were performed to investigate the effect of changing the width of the CMOS transmission gate, TG, on energy recovery achievable in 2-step charging circuit. It is because the energy recovery from the load to the tank-capacitor is done through the transmission gate (TG) and it would be worth looking if the size of the CMOS TG influences the energy recovery achievable in 2-step charging circuit. Here the sizes of the pMOS and nMOS transistors which are connected to the supply voltage, V_{DD} and ground

respectively were not changed. As on increasing the width of the pMOS transistor the current through the transistor will increase causing an increase in the total energy supplied and energy dissipation. Similarly increasing the width of the nMOS transistor, connected between output and ground, will cause more current to flow from output node to the ground thus dissipating more energy.

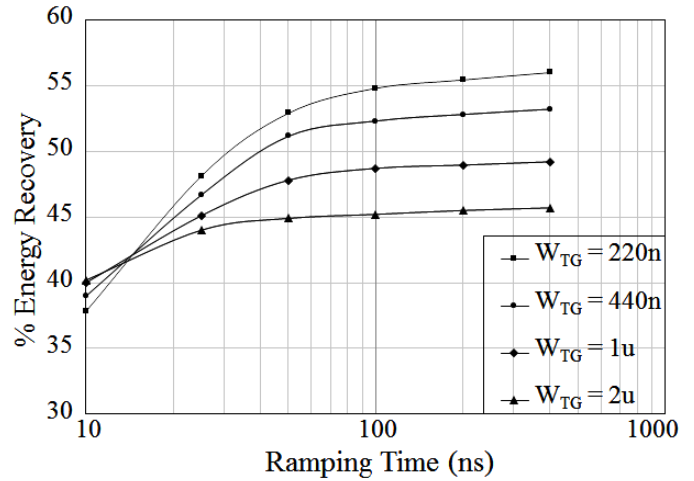


Fig. 8. Energy Recovery Vs Ramping Time at different transmission gate widths.

From the simulation results shown in Fig. 6 and 7, the C_T/C_L ratio was chosen at '10'. The simulation results shown in Fig. 8 shows the relationship between ramping time and percentage energy recovery at different TG widths (W_{TG}). The plot also shows that percentage energy recovery at the ramping time of 10ns, improves as the width of the transmission gate is increased from $W_{TG} = 220n$ to $W_{TG} = 2\mu$. This is because at higher frequency (lower ramping time) the switching time of the transistor is small which doesn't allow the load capacitor to charge/discharge to the required levels of voltages thus reducing the energy supplied and energy recovery.

For ramping times of 25ns to 400ns the energy recovery improves as the width of the TG is reduced. This is because at smaller width, the TG cause the current to decrease which in turn reduces the dissipation in the switch (TG). Also, as the ramping time increases from 10ns to 50ns it shows a significant improvement in energy recovery. However, there is a small improvement (approximately 2%) in energy recovery as the ramping time is increased from 100ns to 400ns. Fig. 7 suggests that for working with lower ramping times (high frequency) the widths of the TG should be increased to allow enough current for the load capacitor to charge and discharge to the required voltage levels. For higher ramping times (lower frequency), the width of the TG should be enough to allow the load capacitor to reach the required voltage levels.

D. Impact of supply voltage scaling on percentage energy recovery

Lastly, simulations were performed to investigate the impact of supply voltage scaling on the energy recovery achievable in the step charging circuit. Energy dissipation is proportional to the square of supply voltage. As the supply voltage is scaled down energy dissipation and energy supplied to the circuit

decreases. For ultra-low power operation it would be worth investigating if the supply voltage scaling influences the percentage energy recovery in step charging circuits. The simulations were performed at different ramping times keeping the C_T/C_L ratio at '10'. All the transistor sizes in the step charging circuit were kept at minimum, excluding the pMOS, connected to the supply voltage which was sized at $W_P = 440\text{nm}$ as mentioned earlier. The supply voltage was scaled down from 1.8V to 0.7V. The supply voltage was not scaled down below 0.7V because the threshold voltage of the transistors used in the step charging circuit is 0.5V and the transistors would go in subthreshold conduction.

The simulation results shown in Fig. 9 shows the relationship between supply voltage and percentage energy recovery at different ramping times. The plot also shows that the percentage energy recovery decreases as the supply voltage is scaled down from 1.8V to 0.7V. There is no significant decrease in the percentage energy recovery for the supply voltage range 1.8V to 1V at the ramping times of 200ns and 400ns, whereas the decrease in the percentage energy recovery for the supply voltage range 1V to 0.7V is about 30% and 10% respectively. For the ramping times of 10ns, 25ns, 50ns and 100ns the decrease in the percentage energy recovery is significant as the supply voltage is scaled down.

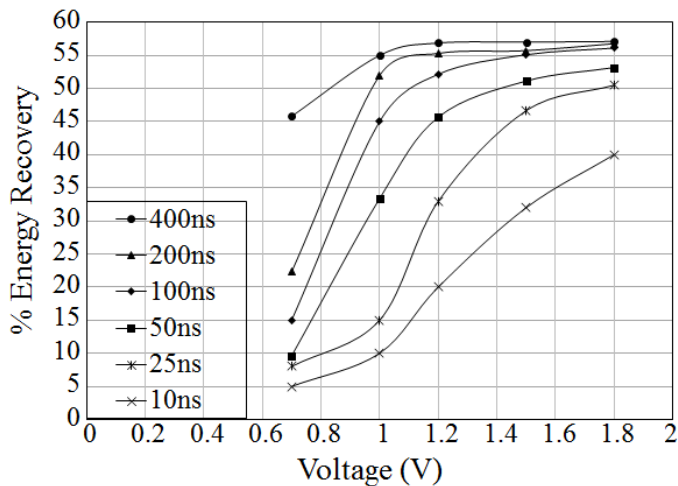


Fig. 9. Energy Recovery Vs Supply Voltage Scaling at different Ramping Times.

Energy supplied and energy dissipated decreases as the supply voltage is scaled down and so does the energy recovery. The decrease in the energy recovery with the supply voltage scaling is significant for the lower ramping times (higher frequency). It is because at lower ramping times and as the supply voltage is scaled down; i) the switching time of the transistors is not enough to charge/discharge the load capacitor to the required voltage levels ($V_{DD}/2$). ii) Also, due to the smaller switching time the peak voltage level doesn't reach to the maximum voltage (V_{DD}). Therefore, ramping time should be increased to attain higher energy recovery as the supply voltage is scaled down. But this will lead to a slower circuit speed.

The plot also shows there is a significant decrease in the percentage energy recovery as the power supply voltage is scaled down from 1V to 0.7V at all ramping times. It is because as the supply voltage moves closer to the threshold voltage of the transistors, the overdrive voltage ($V_{GS}-V_{th}$) is reduced, causing the transistors to be turned off when V_{GS} falls below the threshold voltage (approximately 0.5V). Thus, percentage energy recovery reduces. At this stage even if the ramping time is increased it will not lead to any significant improvement in the energy recovery.

In addition, the leakage related dissipation also increases for higher ramping times (lower frequencies), as leakage losses are accumulated over a slowly ramping power-clocks.

IV. CONCLUSION

In this paper, the energy efficiency in the 2-step charging circuit was investigated. The impacts of factors such as tank-capacitance to load capacitance ratio, C_T/C_L , ramping time, transistor sizing and supply voltage scaling on the energy recovery achievable in the step charging circuit was studied in detail. The simulation results show that a C_T/C_L ratio of '10' can be used as an appropriate "rule-of-thumb" design rule in practical circuits, and increasing this ratio would yield relatively little benefit.

For potential energy benefits in the step charging circuit the width of the transistors should be kept at minimum dimensions at higher ramping times (lower frequency). At lower ramping times (high frequency) the widths of the transistors should be increased to allow enough current for the load capacitor to charge and discharge to the required voltage levels.

Furthermore, the energy recovery achievable in the step charging circuit improves at higher ramping times (lower frequencies). After a limit, further increasing the ramping time would yield relatively little benefits.

Energy recovery reduces as the power supply voltage is scaled down. The decrease in the energy recovery is significant at lower ramping times (higher frequency). Also, energy recovery decreases significantly as the power supply voltage moves closer to the threshold voltage of the transistors.

FUTURE WORK

In future, these simulation results will be used to analyze the energy performance of the power-clock generator of 3, 4, 5, 6, 7 and 8-step charging circuits. If the C_T/C_L ratio of '10' can be used with the larger steps, such a strategy has the advantage that the amount of silicon area dedicated to the tank-capacitors can remain largely constant regardless of the number of steps.

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