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Adiabatic Flip-Flops and Sequential Circuit Design using Novel Resettable Adiabatic Buffers

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Abstract— We propose novel resettable adiabatic buffers for five adiabatic logic families namely; Efficient Adiabatic Charge Recovery Logic (EACRL), Improved Efficient Charge Recovery Logic (IECRL), Positive Feedback Adiabatic Logic (PFAL), Complementary Pass-transistor Adiabatic Logic (CPAL) and Clocked Adiabatic Logic (CAL). We present the design of resettable flip-flops using the proposed buffers. The proposed flip-flops alleviate the problem of increased energy and area consumption incurred by the existing mux-based resettable flip-flops. We then design the 3-bit up-down counters and extended our comparison beyond energy dissipation using the above five adiabatic logic families. PFAL based sequential circuit designs gives the best performance trade-offs in terms of complexity, energy, speed and area compared to the other adiabatic designs.

Keywords— adiabatic logic; energy consumption; flip-flop; performance; power-clocking scheme.

I. INTRODUCTION

The adiabatic technique is one of the innovative solutions at logic and circuit level to achieve a reduction in energy dissipation, where the timing conditions are not so critical. The use of slowly changing power-clock which allows approximately constant current charging/discharging and by avoiding current surges, the circuit dissipates less energy [1]. The energy dissipation using a ramp is given as [2];

$$E_D = RC_L / T_r (C_L V_{DD}^2) \quad (1)$$

Where E_D is the energy dissipation, T_r is the ramping time, C_L is the effective output load capacitance, R is the charging path resistance and V_{DD} is the supply voltage. Based on the literature review, five most energy-efficient adiabatic logic; namely PFAL, IECRL, EACRL, CPAL and CAL are chosen. In literature [3], [4], the resettable flip-flops has been designed using single-phase, CAL and 2-phase, CPAL. It uses multiplexer as their second resettable stage, shown in Fig 1 (a) and (b) respectively, causing the output of the flip-flop to be fed to any subsequent logic only after the multiplexer stage. This gives rise to an increased latency by one power-clock phase and one power-clock period for 2-phase and single-phase logic designs respectively. Moreover, the extra input terminal in the multiplexer results in extra area overhead of the layout place and route causing more energy to dissipates.

In this paper, we propose a single-phase and 2-phase resettable buffers as the solution of the previously designed mux-based resettable adiabatic flip-flops. We also present resettable buffers for the design of resettable flip-flops for 4-

phase adiabatic logic families. All the five proposed resettable flip-flops give the flexibility of tapping the outputs from the required phase, hence results in increased throughput. It also gives an advantage in terms of transistor counts and additional input terminal pin. The paper is structured as follows. In section II, the five non-resettable and proposed resettable adiabatic logics buffer circuits are presented. In section III, the comparison of adiabatic flip-flops in terms of energy and area are discussed. The design example of 3-bit up-down Counter along with its performance trade-offs result is presented in section IV. Finally, the paper is concluded in section V.

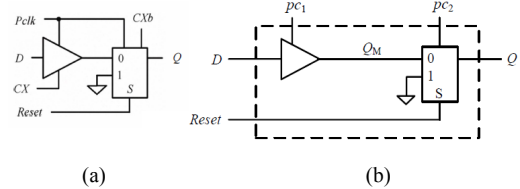


Fig. 1. Mux-based resettable flip-flops using (a) CAL [3] (b) CPAL[4].

II. ADIABATIC LOGIC FAMILIES

A. Improved Efficient Charge Recovery Logic (IECRL)

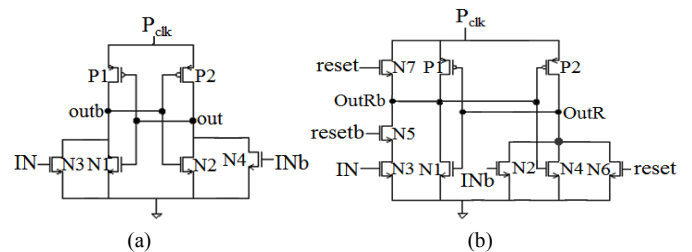


Fig. 2. IECRL buffer (a) Non-resettable [5] (b) Proposed resettable.

Fig. 2 (a) shows an Improved ECRL structure as an improvement over ECRL logic. It is also called 2N-2N2P logic [5]. The Basic operation and working of IECRL are described in [6], [7]. The IECRL resettable buffer circuit is shown in Fig. 2 (b) with transistors N6 and N7 as the input 'reset' pin and transistor N5 as its complement input 'resetb' pin. When reset is true, transistor N6 and N7 turns 'ON', pulling down the node 'OutR' to the ground and the node 'OutRb' to follow the power-clock respectively. Whereas, transistor N5 is turned 'OFF' disconnecting the path between the node 'OutRb' and ground. The transistor N7 eliminates the non-adiabatic loss at node 'OutRb' during the reset operation and reduces energy dissipation. When the reset is false in Fig. 2 (b), IECRL works similar to the non-resettable buffer.

B. Clocked Adiabatic Logic (CAL)

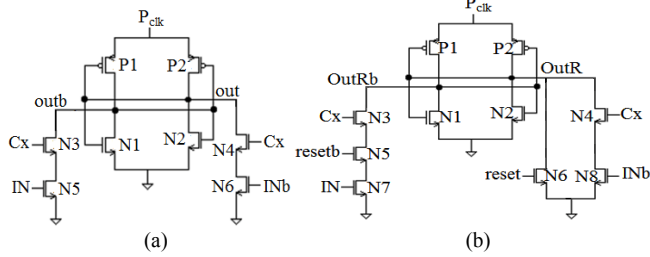


Fig. 3. CAL buffer (a) Non-resettable [8] (b) Proposed resettable.

The CAL buffer is similar to 2N-2N2P but has clocked nMOS transistors (N3, N4) between the evaluation nMOS transistors (N5, N6) and the output as shown in Fig. 3 (a). The clocked nMOS transistors use a pair of non-overlapping auxiliary clocks for cascaded logic. In Fig. 3(b), when reset is true, and the signal Cx starts rising, the node ‘OutR’ is pulled down to the ground, which turns ‘ON’ the transistor P1, forcing the node ‘OutRb’ to follow the power-clock. The reset is an asynchronous signal having priority over the other input signals. When the reset is false, CAL behaves similarly to Fig. 3(a). A more detailed description can be found in [3], [8].

C. Efficient Adiabatic Charge Recovery Logic (EACRL)

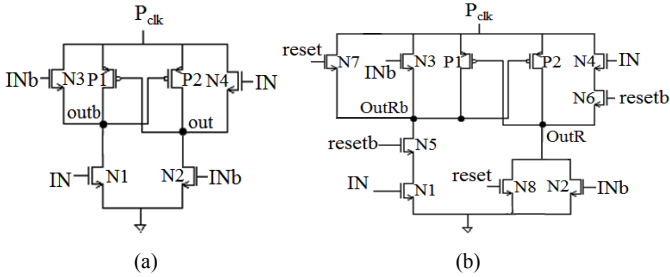


Fig. 4. EACRL buffer (a) Non-resettable [9] (b) Proposed resettable.

Since the EACRL buffer is based on the duplicate evaluation, as shown in Fig. 4 (a), EACRL resettable buffer, shown in Fig. 4 (b), uses duplicate reset inputs; one connected between the output and ground and the other, driven in anti-phase, is connected between the input and the output. When reset is true, transistors N7 and N8 are turned ‘ON’ and N6 and N5 are turned ‘OFF’, the path from power-clock to node ‘OutR’ and ground to node ‘OutRb’ is cut-off. At this instant, N7 and N8 transistors help in reducing the adiabatic loss (AL) by reducing the equivalent resistance at the two output nodes. The EACRL provides a stable output, due to the duplicate evaluation network. A detailed operation and working can be found in [7], [9].

D. Positive Feedback Adiabatic Logic (PFAL)

PFAL is very similar to IECRL but has lesser equivalent resistance at the two output nodes due to the formation of transmission gates pairs between P1, N3 and P2, N4 as seen from Fig. 5 (a). In Fig. 5 (b), when reset is true the transistors N6 and N7 turns ‘ON’, as a result, node ‘outRb’ follows the power-clock albeit not all the way to the supply voltage and the node ‘outR’ pulled down to the ground. Whereas, the transistor

N3 is turned ‘OFF’ disconnecting the path of node ‘outR’ from the power supply. A more detailed description of its non-adiabatic losses can be found in [7], [10].

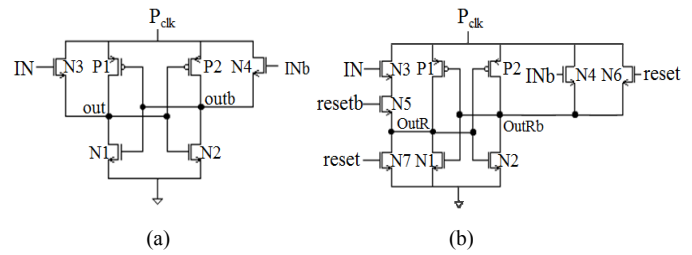


Fig. 5. PFAL buffer (a) Non-resettable [10] (b) Proposed resettable.

E. Complementary Pass-transistor Adiabatic Logic (CPAL)

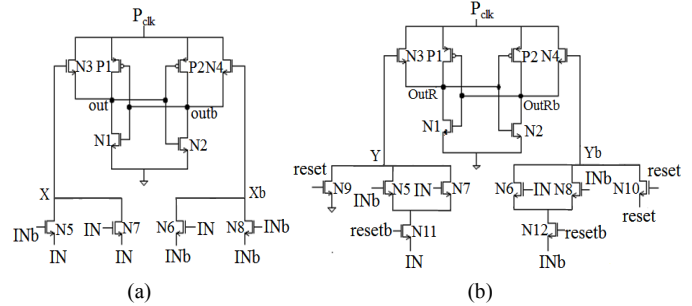
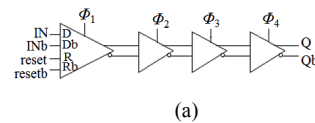


Fig. 6. CPAL buffer (a) Non-resettable [3] (b) Proposed resettable.

As shown in Fig 6 (a), the main part of CPAL evaluation tree (N5-N8) is designed using the pass-transistors which are connected to the gates of the nMOS transistors (N3, N4) representing the PFAL buffer. In Fig. 6 (b), when reset is high (resetb low), transistor N9 and N10 turns ‘ON’ and passing logic ‘0’ to the gate of N3 transistors which turns it ‘OFF’ and at the same time passing logic ‘1’ (reset high) with one threshold voltage less, but high enough to turn ‘ON’ transistor N4. As a consequence, the node ‘OutRb’ follows the power-clock, P_{clk} and ‘OutR’ is pulled down to ground through the transistor, N1. The resetb signal connected to transistors N11 and N12 disconnects the path of IN and INb signals. For more detailed description of its Non-Adiabatic Loss (NAL) on internal nodes X (or Xb) and Y (or Yb) are analysed in [3].

III. ADIABATIC FLIP-FLOPS

The adiabatic D flip-flop is constructed using a cascaded buffer chain. An n-phase power-clock will have n-stages of buffers to construct a flip-flop. The D flip-flops designed using IECRL, PFAL and EACRL uses 4-phase power-clock, whereas, CPAL and CAL use 2-phase and a single-phase power-clock respectively. The first stage of each of the resettable flip-flops are composed of the resettable adiabatic buffer and the other stages use the non-resettable adiabatic buffers as shown in Fig. 7. The comparison of the layout area between non-resettable, existing mux-based and proposed resettable flip-flop are summarised in Table I.



(a)

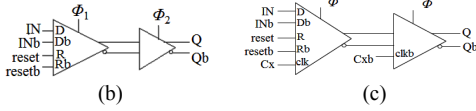


Fig. 7. Proposed resettable flip-flops using (a) 4-phase (b) 2-phase (c) Single-phase power-clocking scheme.

TABLE I. COMPARISON OF THE LAYOUT AREA

Adiabatic Logic Families	Layout Area (μm^2)		
	Non-Resettable Flip-flop	Existing Mux-based Resettable Flip-Flop	Proposed Resettable Flip-flop
CPAL	5.68 x 17.28	6.44 x 17.32	8.99 x 18.40
CAL	6.44 x 9.68	7.71 x 12.48	6.44 x 10.91
PFAL	6.46 x 18.75	7.72 x 23.16	6.98 x 19.29
EACRL	6.07 x 20.89	8.24 x 30.75	6.97 x 24.75
IECRL	6.24 x 17.68	7.51 x 22.35	6.56 x 18.73

From Table I, it can be seen that except CPAL, the rest four proposed resettable flip-flops consume less area as compared to the existing mux-based design due to the following reasons; Firstly, the less number of transistors used in resettable buffer compared to the multiplexer stage. Secondly, due to the extra input pin in the multiplexer which leads to an overhead in the routing of the complementary and non-complementary signals.

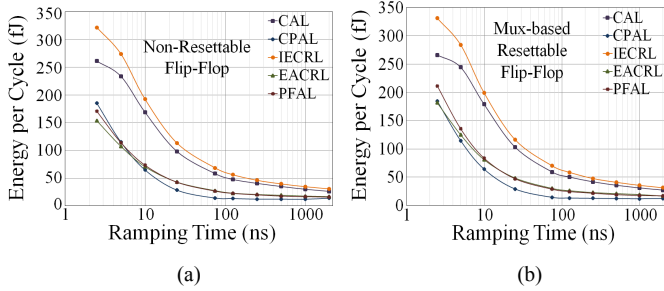


Fig. 8. Energy consumption of flip-flops (a) Non-resettable (b) Mux-based

The power-clock generator can be implemented using a stepwise charging circuit [11] but for the ease of simulation a trapezoidal wave, ramping from 0V to 1.8V is taken [7]. We use minimum sized transistors for all the designs based on TSMC 180nm CMOS technology. The energy consumption per power-clock cycle is calculated at typical-typical corner for each of the adiabatic flip-flops. The energy consumption of the flip-flops was derived through simulation for the periodic sequence of “101010...” thereby, giving the maximum energy consumed. It is clearly evident from Fig 8 (a), (b) and 9 (a) that the energy of the proposed flip-flops for the entire ramping times range under load capacitance of 100fF is less compared to the existing mux-based design. On an average, the mux-based EACRL and PFAL flip-flops consume approximately 15%, more energy, whereas IECRL and CAL consume approximately 4% more energy compared to the non-resettable counterparts across the ramping time. The energy consumption of the mux-based CPAL is similar to that of the non-resettable flip-flop for the entire range of ramping time with an increment of approximately 0.5%.

From Fig. 9 (a), the proposed PFAL, CPAL, CAL and IECRL resettable flip-flops consume on an average

approximately 0.5% more energy compared to the non-resettable flip-flop. On the other hand, due to the decrease in the output resistance of the proposed EACRL buffer, its energy consumption shows a decrement of approximately 5% compared to the non-resettable flip-flop at a ramping time longer than 25ns. Although, the proposed CPAL flip-flop consumes minimum energy at the longer ramping time, but as the ramping time becomes shorter its energy dissipation increase above EACRL and PFAL.

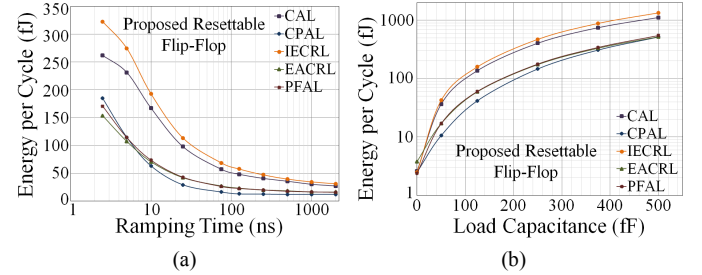


Fig. 9. Energy consumption at varying (a) ramping time (b) load capacitance

Fig. 9 (b) shows the effect of loading on energy consumption for the proposed resettable flip-flops at 25ns ramping time. IECRL and CAL energy consumption are maximum due to the presence of NAL during the evaluation and recovery phase, whereas EACRL and PFAL consume the same amount of energy for the load capacitance value higher than 50fF, as both have NAL only during the recovery phase. The advantage of the zero NAL at the output nodes makes CPAL consume the least energy at small values of capacitance. At load capacitance increases, AL starts dominating the NAL, thus CPAL energy consumption becomes almost similar to PFAL and EACRL.

IV. DESIGN EXAMPLE AND PERFORMANCE RESULT

In the past, various examples like 16-bit CLA [9], 8-bit multiplier [10], mode-10 counter [3] and 2-bit twisted ring counter [7] has been implemented to show the comparison between different adiabatic logic families and CMOS design in terms of energy efficiency. The existing designs lacked to give a comparison which encompasses performance issues among adiabatic logic families using different power-clocking scheme [12]. Since the flip-flop doesn't have any combinational logic gates it is difficult to evaluate the performance between multi-phase adiabatic logic, thus a 3-bit up-down counter is designed. The counter counts up when UD signal is low and counts down when it is high only when reset is low. The Boolean expression for Q_0 - Q_2 is given by;

$$\begin{aligned}
 D_0 &= Q_0^{n+1} = \text{resb} \cdot Q_0^n \\
 D_1 &= Q_1^{n+1} = \text{resb} \cdot [Q_1^n \oplus (Q_0^n \oplus \text{UD})] \\
 D_2 &= Q_2^{n+1} = \text{resb} \cdot [Q_0^n \cdot \text{UDb} (Q_1^n \oplus Q_2^n) + Q_{b0}^n \cdot \text{UD} (Q_1^n \oplus Q_2^n) + Q_2^n \cdot \overline{(\text{UD} \oplus Q_0^n)}]
 \end{aligned} \tag{2}$$

As seen from (2), to implement a function D_2 a minimum of three levels are required. In the case of a single phase, 2-phase and 4-phase designs; 3 power-clocks periods that is 12Tr , 1.5 power-clock period that is 9Tr and $3/4$ power-clock period that is 3Tr respectively are required. The energy consumption of

the counter is averaged over fifteen counts, counting from seven down to zero and back to seven. Fig. 10 (a) shows the average energy consumption per count of the five adiabatic logic designs and static CMOS under a load capacitance of 10fF at a ramping time ranging from 2.5ns to 250ns.

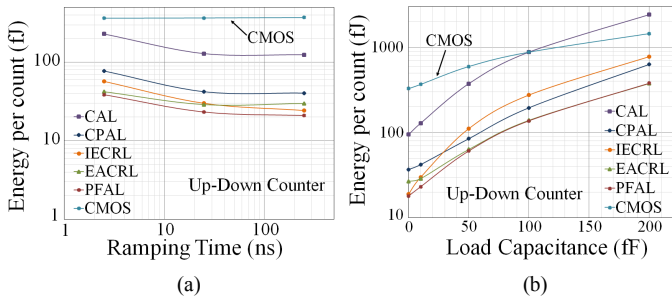


Fig. 10. Energy consumption at varying (a) ramping time (b) load capacitance.

Due to the fact that, each state of the CAL design takes four power-clock cycles, the energy benefits of CAL counter is least at all ramping times. Similarly, the CPAL design, which takes two power-clock cycles for each count, has energy as second worst as shown in Fig. 10(a). As EACRL logic has dual-rail evaluation network, the leakage losses dominate over AL and NAL at longer ramping times and thus its energy increases compared to IECRL. Fig. 10 (b) shows the effect of loading on energy consumption of counter at 25ns ramping time. However, the CAL design is less complex but due to the low throughput, it is the least energy efficient. It is also worth mentioning that the CMOS design outperforms CAL at higher load. In Fig. 10 (b), the increase of the IECRL energy consumption is due to the fact of higher NAL. On the other hand, at load capacitance higher than 100fF, the energy consumption of EACRL is exactly similar to that of PFAL. This is due to the fact that as the load capacitance value increases, the effective load at the output node will mainly be comprising of the load capacitance rather than its internal load capacitance. Based on the simulation results of the up-down counter the performance of the multi-phase adiabatic logic design is summarised in Table II. It can be seen that the 4-phase PFAL and IECRL designs are more efficient in terms of area, throughput and energy consumption.

TABLE II. COMPARISON OF THE PERFORMANCE OF MULTI-PHASE ADIABATIC UP-DOWN COUNTER DESIGN

Adiabatic Logic Families	Area: no. of transistors	Computation Time per count	Throughput	Complexity
CPAL	238	12Tr	Low	High
CAL	212	16Tr	Very Low	Low
PFAL	189	4Tr	High	High
EACRL	222	4Tr	High	Very High
IECRL	189	4Tr	High	High

V. CONCLUSION

The proposed adiabatic resettable buffers used for the design of resettable flip-flops leads to higher throughput and decrease energy and area consumption compared to the mux-

based resettable adiabatic flip-flops. The proposed resettable flip-flops consume approximately same energy compared to their non-resettable counterparts, despite having a larger area and using more number of transistors. CPAL is the most energy efficient at mid-frequency range and at low capacitive load, but as the complexity of the sequential system increases and due to its long idle period, it consumes high energy and large area compared to the 4-phase adiabatic designs. The CAL logic design is least beneficial in comparison to the other adiabatic logic designs, however having the lowest power-clock complexity. IECRL and PFAL show promising results in terms of energy, speed and area but however IECRL energy increases as load capacitance increases.

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