A Continuous-Time Time-Interleaved Delta-Sigma Modulator with a Novel Solution to the Delayless Feedback Path Problem for High Bandwidth Applications

Talebzadeh, J.

A Continuous-Time Time-Interleaved Delta-Sigma Modulator with a Novel Solution to the Delayless Feedback Path Problem for High Bandwidth Applications

Jafar Talebzadeh

A thesis submitted in partial fulfilment of the requirements of the University of Westminster for the degree of Doctor of Philosophy

December 2017

Abstract

In this PhD program, a new method of implementation of time-interleaved continuous-time ΔΣ modulators is investigated. This thesis proposes a novel solution to the ***delayless feedback path issue*** which is a restriction for circuit implementation of time-interleaved ΔΣ modulators. To verify the theory behind our method, first, a 3rd-order two-path continuous-time time-interleaved ΔΣ modulator has been behaviourally modelled with non-idealities included with the use of MATLAB and then the circuit has been designed with using Cadence and 90nm TSMC CMOS technology. The design details as well as the simulation results are presented in the thesis. By exploiting the concept of time-interleaving techniques, a conventional 3rd-order discrete-time ΔΣ modulator is converted into a two-path corresponding discrete-time time-interleaved counterpart, leading to the equivalent continuous-time time-interleaved version derived from the discrete-time equivalent. Sharing the integrators between two paths of the reported modulator makes it robust to path mismatch effects compared to the typical Time-Interleaved (TI) modulators which have individual integrators in all paths. Practical issues like finite dc gain and bandwidth of the opamps, the clock jitter effect, RC time constant variation, the DAC mismatches and offsets of the quantizers have been analyzed and included in the behaviour simulation model. The resulting modulator has been implemented using 90nm TSMC CMOS technology. All results obtained from this study confirm that the proposed approach works very well with no noticeable degradation in performance even in the presence of non-idealities. The whole CTTI ΔΣ modulator has been simulated with an input frequency of $F_{in} = 1.005MHz$ and $1.6V_{pp}$ (-2dBFS) amplitude at 320MHz sampling frequency across process corners and temperatures. The SNDR is in range from 74.5dB at SS and -40°C temperature to 75.9dB at FF and 120°C temperature.

Acknowledgements

I would like to express my sincere gratitude to my PhD supervisor, Professor Izzet Kale, for the continuous support of my PhD study, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of my PhD research.

I would like to show my special gratitude to my colleagues in Qualcomm, Huawei and Ignis Innovation Company. I really appreciate their willing and patience to help me whenever I had problems. Without their help, I could not develop my knowledge and skill and made any progress in my work.

A special thank you goes to my wife, Somayeh Izadi, for her love, being supportive and believing in me. I would like to thank my beautiful daughter, Tania, who has been so inspiring for me during my PhD study.

Last but not least, I would like to express my gratitude to my parents. Even thousands of kilometres apart, they have been present through every step of my life, providing support in difficult times and encouraged me to pursue and complete my PhD study. This thesis is dedicated to my family.

Table of Contents

List of Figures

List of Tables

ABBREVIATIONS

AA	Anti-Aliasing
AAF	Anti-Aliasing Filter
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous-Time
CTTI	Continuous-Time Time-Interleaved
ΔΣ	Delta-Sigma
D/A	Digital-to-Analog
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DR	Dynamic Range
DSP	Digital Signal Processing
DT	Discrete-Time
DTTI	Discrete-Time Time-Interleaved
DWA	Data Weighted Averaging
ELD	Excess Loop Delay
Hz	Hertz
HRZ	Half Return to Zero
IBN	In-Band Noise
IC	Integrated Circuit
IIT	Impulse Invariant Transformation
LNA	Low Noise Amplifier
LP	Low Pass

LPF	Low Pass Filter
LSB	Least Significant Bit
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
NMOS	N-channel MOS
NRZ	Non-Return to Zero
NTF	Noise Transfer Function
OSR	OverSampling Ratio
OTA	Operational Transconductance Amplifier
PMOS	P-channel MOS
PSD	Power Spectral Density
RF	Radio Frequency
RZ	Return to Zero
SC	Switched Capacitor
S&H	Sample and Hold
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise and Distortion Ratio
SR	Slew Rate
STF	Signal Transfer Function
THD	Total Harmonic Distortion
TI	Time Interleaved

Author's Declaration

I, Jafar Talebzadeh, declare that all the material contained in this thesis is my own work.

Chapter 1:
Introduction

1.1 Motivation

The rapid growth of the portable communication device markets such as audio systems and consumer electronics has led to an increasing demand for low power high resolution ADC designs over the last decade [1]. The ΔΣ modulator can achieve a very high resolution analog-to-digital conversion for relatively low-bandwidth signals by using the oversampling and the noise shaping techniques. It is known that ΔΣ modulators don't require precise analog components and sharp cut-off frequencies for their analog anti-aliasing filters. The noise-shaping loop filter of a ΔΣ modulator can be implemented as either a Discrete-Time (DT) structure by using Switched-Capacitor (SC) techniques [76] or as Continuous-Time (CT) through active-RC [79] or gm-c filters [80][81]. SC circuits are insensitive to clock jitter and the frequency response of the noise-shaping filter can be accurately set by capacitor ratios [2].

The signal bandwidth the ΔΣ modulators can deal with is narrow and restricted by the OverSampling Ratio (OSR) and technology deployed. To increase the signal bandwidth the modulator can process, a variety of methods are used: Increase the order of the modulator; however the stability problem needs to be dealt with very carefully. A second method is to increase the number of bits for the quantizer, which makes the design of the modulator more complicated. A third method is to increase the sampling frequency. Where, the major disadvantages of this method are limitations in technology. The fourth method is to deploy a continuous-time loop filter coupled with the time-interleaving technique. This method is more practical in comparison to previous methods.

The goal of this thesis is to extend the idea of time-interleaving DT ΔΣ modulators to work with CT ΔΣ modulators, while reaching higher signal bandwidth than conventional ΔΣ modulators. To reach this goal, first,

a 3rd-order two-path Continuous-Time Time-Interleaved (CTTI) ΔΣ modulator has been behaviourally modelled with the use of MATLAB, where all non-idealities are included in the model. Then the circuit level has been designed with the use of Cadence and 90nm TSMC CMOS technology. The resulting modulator operates at 320MHz clock frequency with the OSR of 16 and a time-interleaving factor of 2. The signal bandwidth of this modulator is 10MHz. The time-interleaving technique is not limited and could be extended to more than two channels to obtain more signal bandwidth.

Table 1.1: Recently published high-bandwidth ΣΔ modulators

Paper	*CMOS Technology*	*Topology*	*Clock Frequency (MHz)*	*SNDR (dB)*	*Bandwidth (MHz)*	*Power (mW)*	*Published Year*	*Simulation (S) Or Measurement (M)*
[3]	$0.13\mu m$	1-2 Cascaded DT	160	50	20	87	2003	M
[4]	$0.18\mu m$	2-2 Cascaded CT	160	57	10	122	2004	M
[5]	$0.18\mu m$	5th order CT	200	72	12.5	200	2004	M
[6]	$0.13\mu m$	4th order CT	300	64	15	70	2004	M
[7]	$0.18\mu m$	3rd order CT	200	49	20	103	2006	M
[8]	$90nm$	5th order CT	400	52	10	7	2007	M
[9]	$0.13\mu m$	3rd order CT	950	72	10	40	2008	M
[10]	$0.18\mu m$	3rd order CT	640	66	10	7.5	2007	S
[11]	$0.13\mu m$	3rd order CT	640	74	20	54	2006	M
[12]	$0.25\mu m$	Complex CT	320	53.5	20	32	2006	M
[13]	$0.13\mu m$	2nd order CT	640	51.4	20	6	2008	S
[14]	$90nm$	2nd order CT	340	77	20	56	2007	M
[15]	$0.13\mu m$	3rd order CT	900	78	20	87	2009	M
[16]	$0.18\mu m$	3rd order CT	320	74	10	36	2010	S
[17]	$0.18\mu m$	5th order CT	320	83.69	5	19.8	2010	S
[67]	$0.13\mu m$	3rd order CT	640	75.3	10	7.2	2016	M
[57]	$28nm$	3rd order CT	640	70.1	20	6	2017	M

1.2 Related Works

Some related works on CT ΣΔ modulators in the CMOS technology have been listed in Table 1.1. These ΣΔ Modulators have been published recently and have the potential to operate at a higher sampling frequency. Table 1.1 summarizes some recent low-pass ΣΔ modulators in CMOS technology along with their measurement results. Most of them have a bandwidth of 10MHz or more and except for the first two, the rest of them use the single loop architecture with the order of two and more. The minimum SNDR of these modulators is 49dB and the power consumption range is from 6mW to 200mW.

1.3 Novelty and Performance Benefits:

1.3.1 Novel Error Correction Solution to Solve the Delayless Feedback Path Problem:

A novel solution method to delayless feedback path issue in TI ΣΔ modulators has been proposed in this PhD program. This delayless feedback path is the major restriction to develop TI ΣΔ modulators. To verify the theory behind my method, TI ΣΔ modulators with 2^{nd} to 4^{th} order and two and four paths have been modelled, designed and simulated through the use of MATLAB and Cadence. All results obtained from this study confirm that the proposed method to solve the delayless feedback path problem works well with no noticeable degradation in performance even in the presence of non-idealities. Finally, a 3^{rd}-order two-path CTTI ΔΣ modulator has been implemented using Cadence and 90nm CMOS TSMC technology. The effects of approximately all non-idealities on the performance of the modulator have been investigated. This modulator meets the specification of WiFi application of 5MHz to 20MHz input signal bandwidth. This novel method was patented at the British Patent Office (UKPO) in 26^{th} March 2014 with the reference number of PAUWT1549GB.

1.3.2 Novel Generic Mapping Equations From DT to CT:

In this PhD study, a generalised novel formula for Impulse Invariant Transformation has been proposed which can be used to map an nth-order DT ΣΔ modulator to an nth-order equivalent CT one. The simulation results confirm that the CT ΣΔ modulator which has been derived from the mapping formulas work in accordance with the initial DT ΣΔ modulator without any noticeable degradation in performance.

1.3.3 Single Path (Shared Integrators) Solution:

Sharing integrators between paths is another method which has been used to increase the performance, to save silicon area and power consumption. By sharing integrators between paths, the sensitivity to the offset mismatch of integrators is eliminated.

1.3.4 Low-Power Performance Compared to Single Path:

Power consumption plays an important role in choosing the architecture of an ADC. All components except for the output multiplexer work with half the sampling frequency in the 3rd-order two-path TI ΣΔ modulator with shared integrators but the output multiplexer operates at the sampling frequency. Therefore, sub-blocks of this modulator such as integrators, DACs and quantizers can be designed with much low power than a conventional ΣΔ modulator which works with the same sampling frequency. Power consumption of the TI ΣΔ modulators is considerably lower than the power consumption of pipeline ADCs.

1.3.5 Novel Generic Formula to Derive Signal and Noise Transfer Function:

Novel formulas have been proposed to derive and analysis the signal and noise transfer function of TI ΣΔ modulators. First, six loop filters of Discrete-Time Time-Interleaved (DTTI) ΣΔ modulator are derived and then its signal and noise transfer function are derived and plotted. Then, six loop filters of CTTI ΣΔ modulator have derived by using Impulse Invariant Transformation. Finally, the signal and noise transfer function of equivalent CTTI ΣΔ modulator have been derived and plotted.

1.4 Outline

This Thesis is organized as follows. In Chapter 2, the CT ΔΣ modulators and the concept of the impulse-invariant transformation are reviewed. In Chapter 3, a single-path DTTI ΣΔ modulator from a 3rd-order conventional DT ΔΣ modulator is derived using the time domain equations and then it is converted to a CTTI ΔΣ modulator. The delayless feedback path problem and our proposed solution are both discussed in detail in this Chapter. In Chapter 4, MATLAB simulation results are presented. Chapter 5 will present the circuit design and simulation results for this modulator and finally conclusion is given in Chapter 6.

Chapter 2:

Delta Sigma Modulators

2.1 Introduction

The ΔΣ modulators are oversampling converters such that sampling frequency is higher than twice the Nyquist frequency. As a result, the quantization noise power is spread over a wider range of frequencies, compared to the signal power which remains within the signal band. The ΔΣ modulator behaves differently for the quantization noise and for the signal. The signal would pass unaltered through the modulator, while the quantization noise was shaped to higher frequencies by a high-pass filter. In this way the quantization noise is separated from the signal in the frequency domain and can be removed by a high precision digital filter which is called a decimation filter [1],[2],[7],[9],[11],[12],[13],[17],[18].

2.2 The Concept of Noise Shaping

A general structure of a noise-shaped ΔΣ modulator is shown in Figure 2.1(a), while Figure 2.1(b) illustrates the modulator as a linear model [30]. In this architecture, $H(z)$ is a loop filter transfer function and the order of this filter will determine the order of ΔΣ modulator. Therefore, a 3rd-order low-pass ΔΣ modulator deploys a 3rd-order low-pass filter. The loop filter shapes the noise spectrum, however, leaving the signal spectrum unchanged.

The linear model shown in Figure 2.1(b) has two independent inputs: the input signal $x(n)$ and the quantization error $e(n)$. We can derive a Signal Transfer Function (STF) from the input signal $x(n)$ to the output signal $y(n)$ and also a Noise Transfer Function (NTF) from the quantization error $e(n)$ to the output signal $y(n)$ as follows.

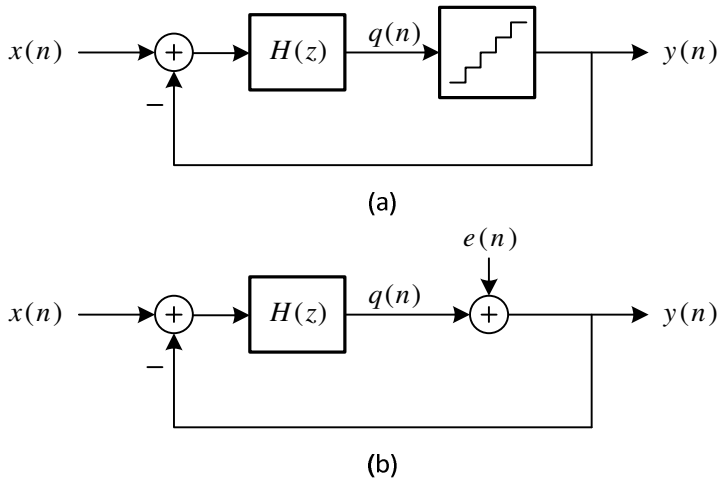


Figure 2.1: a) a general noise-shaped ΔΣ modulator and b) its linear model.

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \tag{2.1}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{2.2}$$

Equation (2.2) shows that the zeroes of $NTF(z)$ are equal to the poles of $H(z)$. In other words, when $H(z)$ goes to infinity, $NTF(z)$ will go to zero. The z-transform of the output signal $Y(z)$ can be written as the combination of the z-transform of the input signal $X(z)$ and the quantization noise $E(z)$ and their correspondence filter transfer functions as follows.

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2.3}$$

The ΔΣ modulator uses a high pass filter NTF to shape the noise and shift the majority of the noise power to higher frequencies. This noise shaping reduces the In-Band Noise (IBN) power and increases the SNR of the modulator. The modulator uses a low pass filter STF which has a unity gain over the signal band in order to pass input signal unchanged. Figure 2.2 shows the effect of oversampling and noise-shaping on the signal and noise spectrum in a ΔΣ modulator [30].

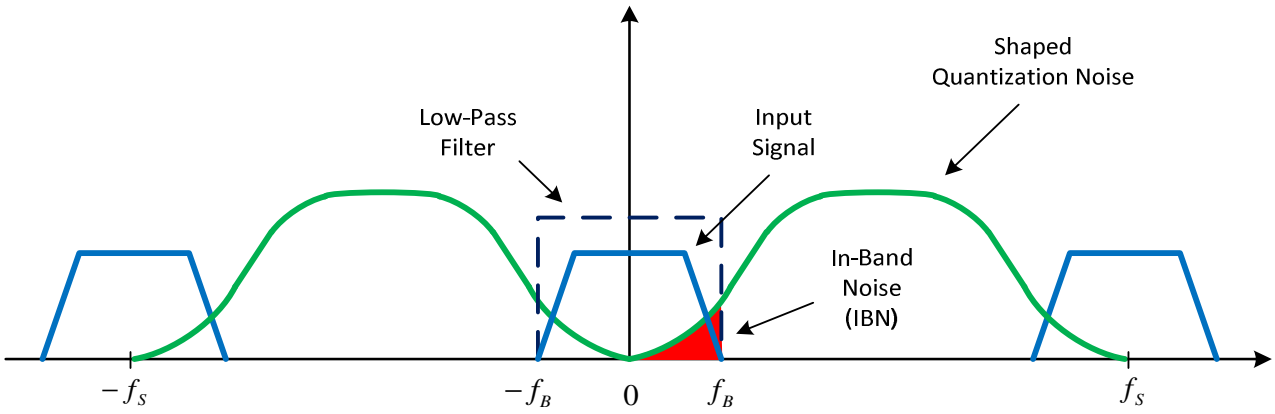


Figure 2.2: Illustration of the effect oversampling with noise shaping on the signal and noise spectrum in a ΔΣ modulator [30].

2.3 First-Order Noise Shaping

To realize first-order noise shaping, $NTF(z)$ should have a zero at dc ($z = 1$) so that the quantization noise is high-pass filtered. The loop filter, $H(z)$, is realized by a simple first-order DT integrator [30]:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.4}$$

The resulting architecture is the first-order ΔΣ modulator. $NTF(z)$ and $STF(z)$ are derived from (2.1) and (2.2) as follows.

$$STF(z) = z^{-1} \tag{2.5}$$

$$NTF(z) = 1 - z^{-1} \tag{2.6}$$

Where the signal transfer function, $STF(z)$, is simply a delay, while the noise transfer function, $NTF(z)$, is a DT differentiator (a high-pass filter). By substituting $z = e^{j2\pi f/f_s}$ in (2.6), where f_s is sampling frequency, the magnitude of the noise transfer function $|NTF(z)|$ is given by (2.7):

$$|NTF(z)| = 2\sin(\pi f/f_s) \tag{2.7}$$

The noise transfer function is a high-pass filter. The IBN power (P_e) is calculated by (2.8) and given by (2.9).

$$P_e = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}(2\sin(\pi f/f_s))^2 df \tag{2.8}$$

and making the approximation that $f \ll f_s$ (i.e., $OSR \gg 1$), so that we can approximate $\sin(\pi f/f_s)$ to be $\pi f/f_s$, we have

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_B}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{2.9}$$

where Δ is the quantizer step width. The maximum SNR for this case is given by (2.12).

$$SNR_{max} = 10\log_{10}\left(\frac{P_s}{P_e}\right) \tag{2.10}$$

$$SNR_{max} = 10\log_{10}\left(\frac{3}{2}2^{2B}\right) + 10\log_{10}\left(\frac{3}{\pi^2}(OSR)^3\right) \tag{2.11}$$

$$SNR_{max} = 6.02B + 30\log_{10}(OSR) - 3.41 \tag{2.12}$$

Where P_s is the signal power and B is the number of bits for the quantizer. Note that doubling the OSR increases the SNR by 9dB or equivalently 1.5bit/octave. This improvement is better than 0.5bit/octave when oversampling with no noise shaping is used. So a combination of noise shaping and oversampling is more favourable to achieve a high resolution ADC.

2.4 Higher-Order ΔΣ Modulators

The principle of ΔΣ modulators is based on shaping the quantization noise away from in-band to higher frequencies by using the loop filter. An Nth order ΔΣ modulator has a loop filter $H(z)$ which is realized by an Nth order DT integrator [30]:

$$H(z) = \left(\frac{z^{-1}}{1-z^{-1}}\right)^N \tag{2.13}$$

$STF(z)$ and $NTF(z)$ of this Nth order ΔΣ modulator have been derived from (2.1) and (2.2) as follows.

$$STF(z) = z^{-N} \tag{2.14}$$

$$NTF(z) = (1-z^{-1})^N \tag{2.15}$$

$STF(z)$ is a delay and $NTF(z)$ is a Nth order DT differentiator. The magnitude of $NTF(z)$ is derived by substituting $z = e^{j2\pi f/f_s}$ in (2.15) and given by (2.16). A plot of $|NTF(f)|$ for 1st to 4th order ΔΣ modulator has

been shown in Figure 2.3 [1]. The possible decrease of the IBN through higher order filtering is seen. As can be seen in Figure 2.3, the out-of-band gain of the higher order $|NTF(f)|$ increases rapidly, therewith it results in instability through the overloading of the quantizer. Thus, as generally done in control systems, in order to increase the stability the loop gain is commonly reduced by scaling [1].

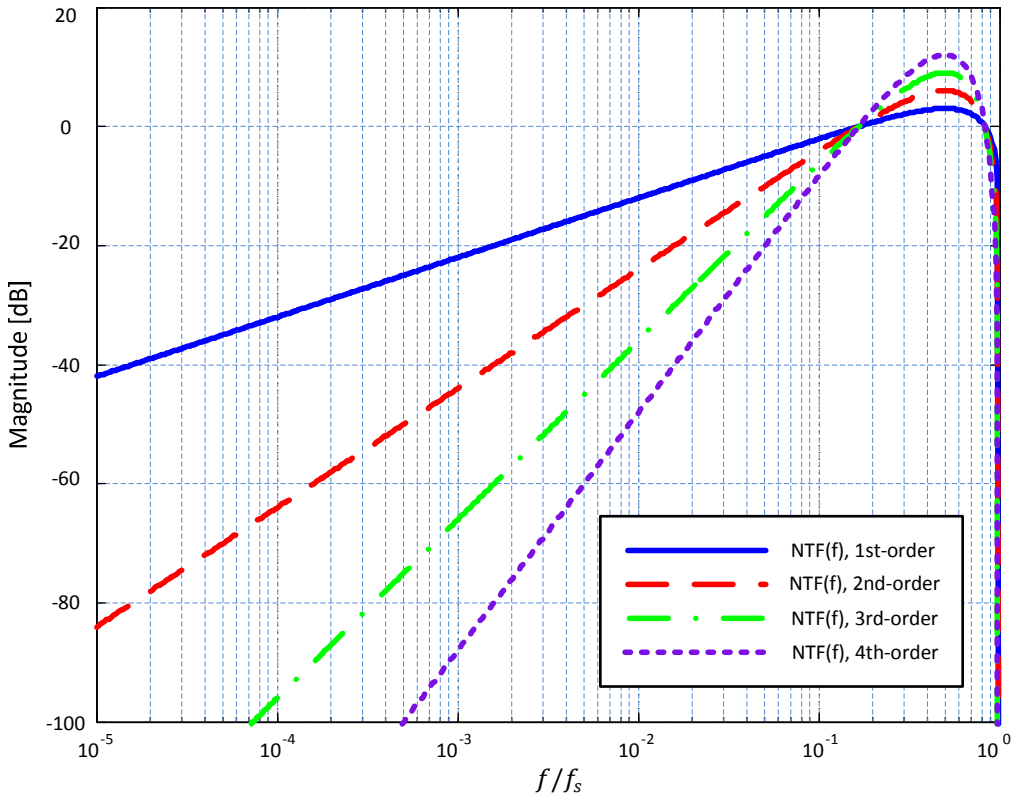


Figure 2.3: $NTF(f)$ for 1st to 4th order ΔΣ Modulator.

$$|NTF(f)| = \left(2\sin\left(\frac{\pi f}{f_s}\right)\right)^N \tag{2.16}$$

Similarly, the IBN power (P_e) and the maximum SNR are calculated for an Nth order ΔΣ modulator as follows.

$$P_e = \frac{\Delta^2}{12}\frac{\pi^{2N}}{2N+1}\left(\frac{1}{OSR}\right)^{2N+1} \tag{2.17}$$

The maximum SNR for an Nth order ΔΣ modulator is given by (2.18) and (2.19) as follows.

$$SNR_{max} = 10\log_{10}\left(\frac{3}{2}2^B\right) + 10\log_{10}\left(\frac{2N+1}{\pi^{2N}}(OSR)^{2N+1}\right) \tag{2.18}$$

$$SNR_{max} = 6.02\text{B} + 1.76 + 10\log_{10}\left(\frac{2N+1}{\pi^{2N}}(OSR)^{2N+1}\right) \tag{2.19}$$

Where N and B are the order of a modulator and the number of bits for the quantizer, respectively.

There is a trade-off between choosing the order of modulator, N, the number of bits for the quantizer, B and the OSR in order to design a ΔΣ modulator. Increasing the order of a modulator greatly increases the SNR but it may cause a stability problem which needs to be dealt with carefully. Multi-bit quantization improves the stability and SNR of a ΔΣ modulator, but it also necessitates the use of Dynamic Element Matching (DEM) [82] to filter the nonlinearity error in the signal band. Data Weighted Averaging (DWA) [83] is the most widely used DEM algorithm, due to its simplicity and low hardware overhead. DWA shapes the nonlinear errors with the first-order function $1 - z^{-1}$ over the whole frequency band. The achievable performance a ΔΣ modulator increases exponentially with OSR as can be seen in (2.19) but for higher OSR the sampling frequency has to be increased which obviously leads to needing faster circuits and also extremely increasing power consumption of the ΔΣ modulator.

2.5 Continuous-Time ΔΣ Modulators

The loop filter of ΔΣ modulators can be realized in either DT or CT. In the last decades, the majority of the published literatures on ΔΣ modulators have been realized in DT by using either the SC [76] or the Switched Current (SI) technique [77][78]. This is because these methods can be more readily and painlessly realized in standard CMOS technologies. Moreover they provide much more tolerance to process variations, clock jitter and the elusive feedback delay problem [1]. Beyond the DT implementation methods, the loop filter can be implemented using CT circuits such as: active-RC [79] and $g_m C$ filters [80][81]. The CT ΔΣ modulators benefit from operating at higher sampling frequencies due to the lack of switching activity. As a result, the bandwidth and Slew Rate (SR) requirements of the opamps can be relaxed. This results in improving power consumption and other speed parameters in comparison to their DT counterparts [1]. The sampling operation is performed by the internal quantizer at the modulator's sampling frequency. So, the errors of the Sample-and-Hold (S&H) circuit are shaped by the loop filter and attenuated at the output of the modulator. The CT ΔΣ modulators

have an implicit anti-aliasing filter in their forward signal path. However, CT ΔΣ modulators suffer from several drawbacks such as: excess loop delay, jitter sensitivity and RC time constant variations in the loop filter and the rest of the circuitry.

2.6 DT-to-CT Conversion of ΔΣ Modulators

A CT loop filter of a CT ΔΣ modulator can be directly designed for a desired NTF and it is carried out by using MATLAB [36]. Another method to design a CT ΔΣ modulator is to initially design a DT ΔΣ modulator and then apply a conversion to map the DT to an equivalent CT loop filter to realize a CT ΔΣ modulator. One way to convert a DT ΔΣ modulator to an equivalent CT ΔΣ modulator is by applying the impulse-invariant transformation [1]. Another is the use of the modified z-transform [1].

2.6.1 The Impulse Invariant Transformation

Principally if the DT and CT ΔΣ modulator as shown in Figure 2.4 behave in exactly the same way, their loop filters will be equivalent. Therefore, applying the same input signal to both modulators should result in the same output bit stream. Having the same output bit stream means that the input signal of the quantizer in CT ΔΣ modulator should be the same as the input of the quantizer in DT ΔΣ modulator at the sampling instants [1].

$q(n) = q_c(t)|_{t=nT}$ for all n (2.20)

This condition would be satisfied if the impulse responses of the open-loop diagrams in Figure 5 were equal at the sampling times. As a result (2.20) translates directly into (2.21):

$$\mathcal{Z}^{-1}\{H_{dDAC}(z)H_d(z)\} = \mathcal{L}^{-1}\{R(s)H_c(s)\}\big|_{t=nT} \quad (2.21)$$

Because $H_{dDAC}(z) = 1$, equation (2.21) can be simplified to give (2.22):

$$\mathcal{Z}^{-1}\{H_d(z)\} = \mathcal{L}^{-1}\{R(s)H_c(s)\}|_{t=nT} \quad (2.22)$$

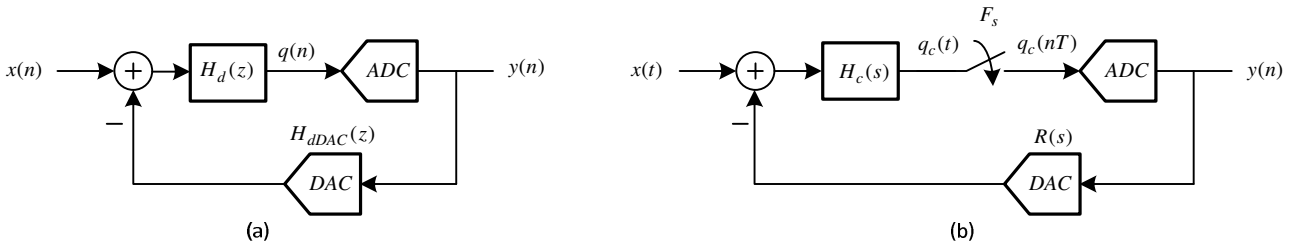


Figure 2.4: The block diagrams of a) The DT ΔΣ modulator and b) The CT ΔΣ modulator.

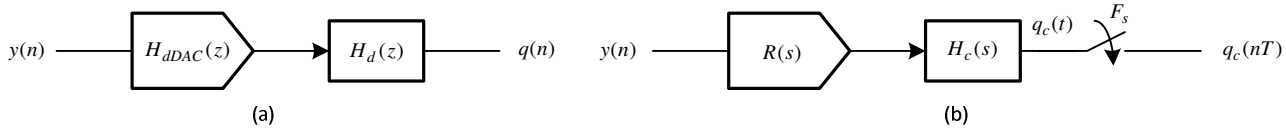


Figure 2.5: a) The open-loop DT ΔΣ modulator and b) The open-loop CT ΔΣ modulator.

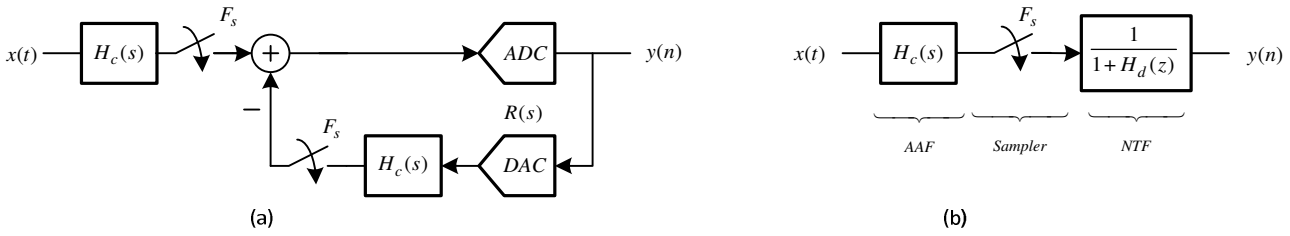
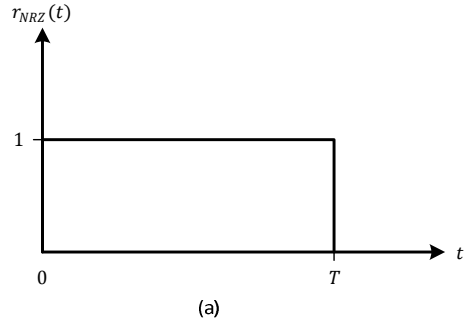


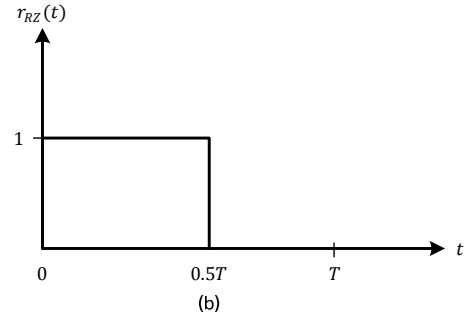
Figure 2.6: a) An equivalent representation of the CT ΔΣ modulator and
b) Another equivalent representation of the CT ΔΣ modulator.

The transformation in (2.22) is called the impulse-invariant transformation where $\mathcal{Z}^{-1}$, $\mathcal{L}^{-1}$, $R(s)$, $H_d(z)$ and $H_c(s)$ represent the inverse Z-transform, the inverse Laplace transform, the CT DAC transfer function, the DT and the CT loop filter respectively [1], [7]. Depending on the output waveform of the CT DAC, there would be an exact mapping between the DT and the CT ΔΣ modulator. The popular feedback-DAC waveforms have rectangular shapes. If the DAC output remains constant during a whole period of the clock cycle, it is called Non-Return-to-Zero (NRZ) DAC and shown in Figure 2.7(a). If the DAC output returns to zero after half of a period of the clock cycle it is called Return-to-Zero (RZ) and is shown in Figure 2.7(b). In general, a rectangular DAC waveform has been illustrated in Figure 2.7(c). The time and frequency (Laplace) domain responses of these waveforms are shown in Figure 2.7 [1][18].



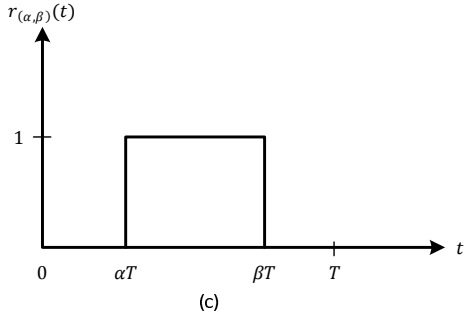
$$r_{NRZ}(t) = \begin{cases} 1, & 0 \le t \le T, \quad 0 \le t \le T \\ 0, & otherwise \end{cases} \tag{2.23}$$

$$R(s) = \frac{1 - e^{-Ts}}{s} \tag{2.24}$$



$$r_{RZ}(t) = \begin{cases} 1, & 0 \le t \le 0.5T, \quad 0 \le t \le T \\ 0, & otherwise \end{cases} \tag{2.25}$$

$$R(s) = \frac{1 - e^{-0.5Ts}}{s} \tag{2.26}$$



$$r_{(\alpha,\beta)}(t) = \begin{cases} 1, & \alpha T \le t \le \beta T, \quad 0 \le t \le T \\ 0, & otherwise \end{cases} \tag{2.27}$$

$$R(s) = \frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s} \tag{2.28}$$

Figure 2.7: Common rectangular DAC waveforms a) NRZ b) RZ C) general form.

2.6.2 Rectangular RZ/NRZ DAC

In CT ΔΣ modulators with a rectangular RZ DAC, the DAC output returns to zero for a portion of time in every cycle regardless of the output value. In contrast for NRZ, as shown in Figure 2.7(a), the output is held during the entire cycle and does not fall to zero [18].

In the RZ DAC, the output needs to settle and recover within each cycle. In contrast, for the NRZ DAC, the output needs to settle only during the transition times which are much less than the number of transitions

compared to the RZ case. Consequently, the NRZ DAC is much less sensitive to clock jitter than the RZ as the number and scale of the transitions are much lower than for the RZ [18].

Comparing to NRZ DAC, RZ DAC is a preferred approach in high resolution CT ΔΣ modulators because of their insensitivity to the output code. In other words, CT ΔΣ modulators with a rectangular RZ DAC are less sensitive to memory effects compared to CT ΔΣ modulators with a rectangular NRZ DAC [18].

In CT ΔΣ modulators with a rectangular RZ DAC, It should be noted that the performance degradation due to the excess loop delay is negligible when this delay is relatively small compared to the clock period; however in CT ΔΣ modulators with a rectangular NRZ DAC, the story is very different compared to CT ΔΣ modulators with a rectangular RZ DAC. Any excess loop delay shifts the DAC output data to the next period and consequently increases the order of the modulator. The excess loop delay affects the modulator's dynamics and it changes the depth of modulation and hence decreases the modulator's stability [18]. Table 2.1 summarizes the advantages and disadvantage of RZ and NRZ DACs.

Table 2.1: The advantages and disadvantages of RZ and NRZ DACs.

	Advantages	*Disadvantages*
RZ DACs	• Tolerate small excess loop delay • Good for high resolution modulators	• More sensitive to clock jitter
NRZ DACs	• Less sensitive to clock jitter • Good for high frequency modulators	• Sensitive to any excess loop delay

As illustrated in Figure 2.4(b), the input signal $x(t)$ of the CT ΔΣ modulator is CT but its output $y(n)$ is DT. Consequently defining a pure s-domain signal transfer function for the CT ΔΣ modulator is impossible. To calculate the STF and the NTF, the loop filter $H_c(s)$ and implicit sampler are relocated across the summation point and placed in front of the CT ΔΣ modulator and in the feedback path as shown in Figure 2.6(a). The NTF of the CT ΔΣ modulator is the same as its DT counterpart. Thus, the NTF remains unchanged:

$$NTF(j2\pi f) = \frac{1}{1 + H_d(e^{j2\pi f})} \tag{2.29}$$

Figure 2.6(b) shows another equivalent representation of the CT ΔΣ modulator. It consists of an Anti-Aliasing Filter (AAF), a sampler and the NTF of its DT equivalent. The STF of the CT ΔΣ modulator will be [18]:

$$STF(j2\pi f) = \underbrace{H_c(j2\pi f)}_{AAF}\underbrace{e^{-j\pi fT}\frac{\sin(\pi fT)}{\pi f}}_{Sampler}\underbrace{\frac{1}{1 + H_d(e^{j2\pi f})}}_{NTF} \tag{2.30}$$

By using (2.22) and (2.28) and manipulating algebraically, the CT-to-DT and DT-to-CT conversion formulas for the 1st to 4th order terms are derived for rectangular DAC waveform and listed in Table 2.2 and 2.3 (Appendix B). In this thesis, a general and novel formula for Impulse Invariant Transformation has been derived and presented in Table 2.2. By using the general formula, an nth-order DT ΔΣ modulator can be converted to an nth-order equivalent CT ΔΣ modulator [1].

Table 2.2: The CT-to-DT transformation for rectangular DAC waveforms [1].

s-domain	*z-domain equivalent for a rectangular DAC waveform*
$\frac{1}{sT}$	$\frac{y_0}{z-1} \quad y_0 = \beta - \alpha$
$\frac{1}{s^2T^2}$	$\frac{y_1 z - y_0}{(z-1)^2} \quad y_0 = \frac{1}{2}(\beta^2 - \alpha^2) \quad y_1 = \frac{1}{2}\{\beta(2-\beta) - \alpha(2-\alpha)\}$
$\frac{1}{s^3T^3}$	$\frac{y_2 z^2 + y_1 z + y_0}{(z-1)^3} \quad y_0 = \frac{1}{6}(\beta^3 - \alpha^3)$
	$y_1 = \frac{-1}{3}(\beta^3 - \alpha^3) + \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$
	$y_2 = \frac{1}{6}(\beta^3 - \alpha^3) - \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$
$\frac{1}{s^4T^4}$	$\frac{y_3 z^3 + y_2 z^2 + y_1 z + y_0}{(z-1)^4} \quad y_0 = \frac{1}{24}(\beta^4 - \alpha^4)$
	$y_1 = \frac{-1}{8}(\beta^4 - \alpha^4) + \frac{1}{6}(\beta^3 - \alpha^3) + \frac{1}{4}(\beta^2 - \alpha^2) + \frac{1}{6}(\beta - \alpha)$
	$y_2 = \frac{1}{8}(\beta^4 - \alpha^4) - \frac{1}{3}(\beta^3 - \alpha^3) + \frac{2}{3}(\beta - \alpha)$
	$y_3 = \frac{-1}{24}(\beta^4 - \alpha^4) + \frac{1}{6}(\beta^3 - \alpha^3) - \frac{1}{4}(\beta^2 - \alpha^2) + \frac{1}{6}(\beta - \alpha)$
$\frac{1}{s^kT^k}$	$\left\{\frac{1}{T^k k!}\frac{\partial^k}{\partial\lambda^k}\left(\frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z - e^{\lambda T}}\right)\right\}\Big\|_{\lambda=0} \quad k \geq 1$

Table 2.3: The DT-to-CT transformation for rectangular DAC waveforms [1].

z-domain	*s-domain equivalent for a rectangular DAC waveform*
$\frac{1}{z-1}$	$\frac{k_0}{s}$ $\quad k_0 = \frac{F_s}{\beta-\alpha}$
$\frac{1}{(z-1)^2}$	$\frac{k_1 s + k_0}{s^2}$ $\quad k_0 = \frac{{F_s}^2}{\beta-\alpha}$ $\quad k_1 = \frac{F_s}{2}\frac{\alpha+\beta-2}{\beta-\alpha}$
$\frac{1}{(z-1)^3}$	$\frac{k_2 s^2 + k_1 s + k_0}{s^3}$ $\quad k_0 = \frac{{F_s}^3}{\beta-\alpha}$ $\quad k_1 = \frac{{F_s}^2}{2}\frac{\alpha+\beta-3}{\beta-\alpha}$ $\quad k_2 = \frac{F_s}{12}\frac{\beta(\beta-9)+\alpha(\alpha-9)+4\alpha\beta+12}{\beta-\alpha}$
$\frac{1}{(z-1)^4}$	$\frac{k_3 s^3 + k_2 s^2 + k_1 s + k_0}{s^4}$ $\quad k_0 = \frac{{F_s}^4}{\beta-\alpha}$ $\quad k_1 = \frac{{F_s}^3}{2}\frac{\alpha+\beta-4}{\beta-\alpha}$ $\quad k_2 = \frac{{F_s}^2}{12}\frac{\beta(\beta-12)+\alpha(\alpha-12)+4\alpha\beta+22}{\beta-\alpha}$ $\quad k_3 = \frac{F_s}{12}\frac{\beta^2(\alpha-2)+\alpha^2(\beta-2)+11(\alpha+\beta)-8\alpha\beta-12}{\beta-\alpha}$

2.6.3 Design Example

In order to show the DT-to-CT transformation procedure through the use of the Impulse Invariant Transformation, the 2nd-order DT ΔΣ modulator shown in Figure 2.8(a) will be converted to the 2nd-order CT ΔΣ modulator as shown in Figure 2.8(b) [1]. The DT loop filter is given by (2.31):

$$H_d(z) = -\frac{a_2}{z-1} - \frac{a_1 a_2}{(z-1)^2} \tag{2.31}$$

The CT loop filter is derived by using Table 2.3 and substituting the 1st and 2nd s-domain equivalent term into (2.31) as follows:

$$LP(s) = -a_2\frac{\frac{1}{\beta-\alpha}}{sT} - a_1 a_2\frac{\frac{T(\alpha+\beta-2)}{2(\beta-\alpha)}s + \frac{1}{\beta-\alpha}}{(sT)^2} = -\frac{\frac{a_2}{\beta-\alpha} + a_1 a_2\frac{(\alpha+\beta-2)}{2(\beta-\alpha)}}{sT} - \frac{\frac{a_1 a_2}{\beta-\alpha}}{(sT)^2} \tag{2.32}$$

If an ideal NRZ DAC pulse $\{\alpha = 0, \beta = 1\}$ is used, the equation (2.32) will result in (2.33):

$$LP(s) = -\frac{a_2 - \frac{a_1 a_2}{2}}{sT} - \frac{a_1 a_1}{(sT)^2} \tag{2.33}$$

Equation (2.33) represents the equivalent CT loop filter. The loop filter, $LP(s)$, is implemented in the 2nd-order CT ΔΣ modulator as shown in Figure 8(b). The loop filter of the 2nd-order CT ΔΣ modulator is given by (2.34):

$$LP(s) = -k_2 \frac{1}{sT} - k_1 \frac{1}{(sT)^2} \tag{2.34}$$

The CT loop filter expressed by (2.34) must be equal to (2.33) to find the 2nd-order CT ΔΣ modulator coefficients. The resulting modulator behaves exactly the same as its DT counterpart.

$$k_1 = a_1 a_2, \qquad k_2 = a_2 - \frac{a_1 a_2}{2} \tag{2.35}$$

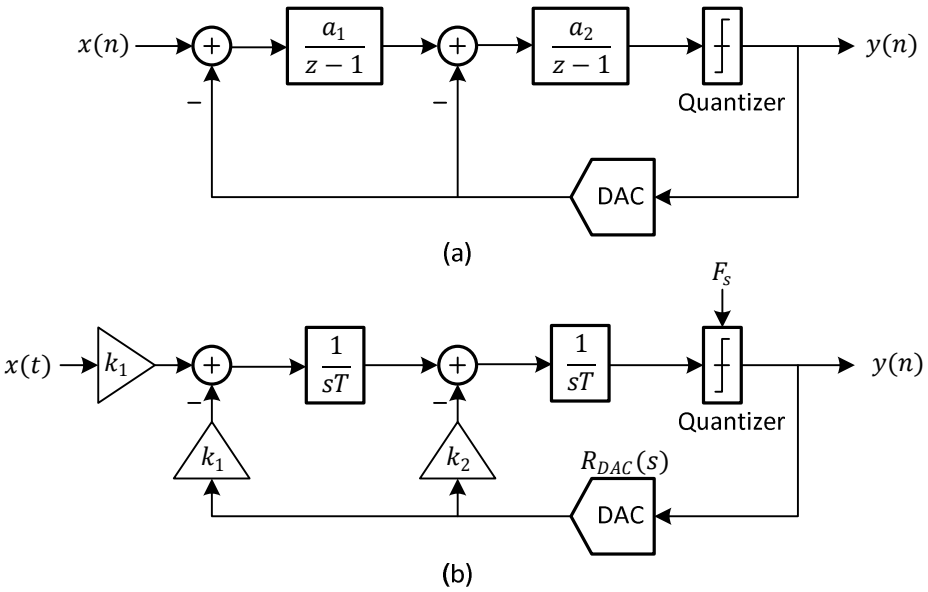


Figure 2.8: a) a 2nd-order DT ΔΣ modulator and b) its 2nd-order CT ΔΣ modulator counterpart with distributed feedback.

2.6.4 The Modified Z-Transform

Another method to convert a DT loop filter to an equivalent CT one is the modified Z-transform [19][20]. In many discrete systems, continuous signals are considered at discrete values with respect to time, usually for $t = nT$, with $n = 0, 1, 2, \ldots$, and with T a fixed positive number usually defined as the sampling period. The analysis of such discrete systems may be carried through the use of the Z-transform method. In some applications the output between sampling instants is very important and thus the Z-transform method is not quite adequate for a critical study of such systems. However, the Z-transform can be easily modified to cover

the systems' behaviour at all instants of time; such an extension of the method is called the modified Z-transform. To obtain the values of $f(t)$ other than the ones at the sampling instants $t = nT$, the following change of variables is performed:

$t = (n - 1 + m)T, \qquad n = 0,1,2, \dots, \quad 0 \leq m \leq 1$

The definition of the modified Z-transform of the time function $f(t)$ is [20]:

$$F(z,m) = z^{-1} \sum_{n=0}^{\infty} f[(n+m)T]\, z^{-n} \tag{2.36}$$

The relationship between the modified Z-transform and the Z-transform is easily obtained by putting $m = 0$ as follows:

$$zF(z,0) = \sum_{n=0}^{\infty} f(nT) z^{-n} = F(z) \tag{2.37}$$

In some applications such as CT ΔΣ modulators, it is useful to evaluate the modified Z-transform of a function $f(t)$ starting from its Laplace transform rather than assessing it directly from (2.36). According to (2.22), the modified Z-transform can be used and the equivalency of the DT and CT loop filter can be rewritten as [1]:

$$H_d(z) = \sum_i Z_{m_i}\{H_c(s)R(s)\} \tag{2.38}$$

In general case, for every time instant, in which the CT loop filter function changes its behaviour, an additional delay factor m_i is introduced. For example, the equation (2.38) for a rectangular DAC waveform shown in Figure 2.7(c) has two delay factors m_1 and m_2 which are defined as follows [18]:

$$H_d(z) = Z_{m_1}\left\{\frac{H_c(s)}{s}\right\} - Z_{m_2}\left\{\frac{H_c(s)}{s}\right\}, \quad m_1 = 1 - \alpha, \quad m_2 = 1 - \beta \;\; and \;\; 0 \leq m_1, m_2 \leq 1 \tag{2.39}$$

The first modified Z-transform has been written for the rising edge of the rectangular DAC waveform at $t = \alpha T$, which leads to $m_1 = 1 - (\alpha T/T) = 1 - \alpha$. The second modified Z-transform has been written for the falling edge of the rectangular DAC waveform at $t = \beta T$, which results in $m_2 = 1 - (\beta T/T) = 1 - \beta$ as given by (2.39). Table 2.4 presents the modified Z-transform equivalents of the s-domain terms. Finally, the equation (2.39) and Table 2.4 are used to determine the CT ΔΣ modulator coefficients from its original DT ΔΣ modulator.

Table 2.4: Modified Z-transform for the corresponding s-domain terms [1].

s-domain	*The modified Z-transform*
$\frac{1}{s}$	$\frac{1}{z-1}$
$\frac{1}{s^2}$	$\frac{mT}{z-1}+\frac{T}{(z-1)^2}$
$\frac{1}{s^3}$	$\frac{T^2}{2}\left[\frac{m^2}{z-1}+\frac{2m+1}{(z-1)^2}+\frac{2}{(z-1)^3}\right]$
$\frac{1}{s^4}$	$\frac{T^3}{6}\left[\frac{m^3}{z-1}+\frac{3m^2+3m+1}{(z-1)^2}+\frac{6m+6}{(z-1)^3}+\frac{6}{(z-1)^4}\right]$
$\frac{1}{s^5}$	$\frac{T^4}{24}\left[\frac{m^4}{z-1}+\frac{4m^3+6m^2+4m+1}{(z-1)^2}+\frac{12m^2+24m+14}{(z-1)^3}+\frac{24m+36}{(z-1)^4}+\frac{24}{(z-1)^5}\right]$

2.6.5 Design Example

Figure 2.9 illustrates a 3rd-order DT ΔΣ modulator and its equivalent CT ΔΣ modulator with a Half-Return-to-Zero (HRZ) feedback DAC [18]. The modified Z-transform method is deployed to find the CT ΔΣ modulator coefficients.

According to the 3rd-order DT ΔΣ modulator shown in Figure 2.9(a), the DT loop filter is given by (2.40):

$$H_d(z) = -\frac{f_{d1}}{z-1} - \frac{f_{d2}}{(z-1)^2} - \frac{f_{d3}}{(z-1)^3} \tag{2.40}$$

The CT loop filter of the 3rd-order CT ΔΣ modulator shown in Figure 2.9(b) and also the HRZ DAC impulse response are given by (2.41) and (2.42):

$$H_c(s) = -\frac{f_{c1}}{sT} - \frac{f_{c2}}{(sT)^2} - \frac{f_{c3}}{(sT)^3} \tag{2.41}$$

$$R_{HRZ}(s) = \frac{e^{-0.5Ts}(1-e^{-0.5Ts})}{s} \tag{2.42}$$

Substituting (2.41) into (2.39) gives (2.43):

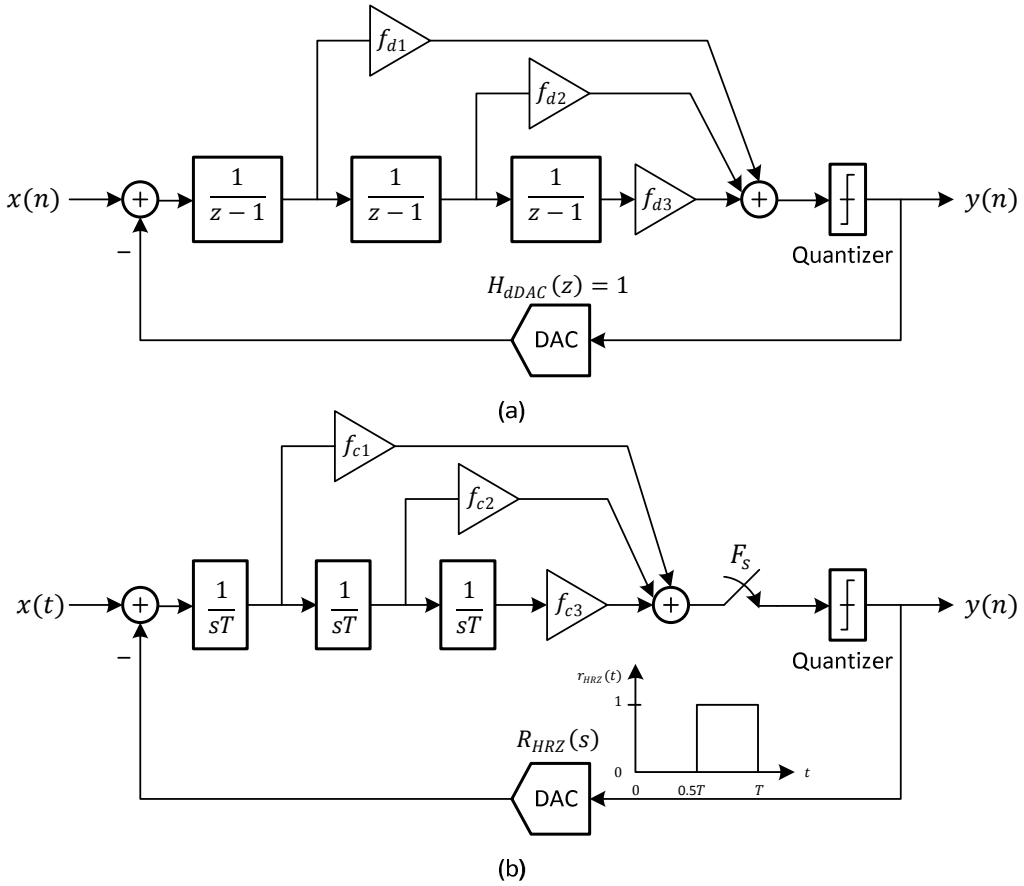


Figure 9: a) a 3rd-order DT ΔΣ modulator and b) its 3rd-order CT ΔΣ modulator counterpart with HRZ DAC feedback.

$$H_d(z) = Z_{m_1}\left\{\frac{1}{s}\left(-\frac{f_{c1}}{sT} - \frac{f_{c2}}{(sT)^2} - \frac{f_{c3}}{(sT)^3}\right)\right\} - Z_{m_2}\left\{\frac{1}{s}\left(-\frac{f_{c1}}{sT} - \frac{f_{c2}}{(sT)^2} - \frac{f_{c3}}{(sT)^3}\right)\right\} \tag{2.43}$$

By using Table 2.4, (2.40) and (2.43) yield (2.44):

$$\frac{f_{d1}}{z-1} + \frac{f_{d2}}{(z-1)^2} + \frac{f_{d3}}{(z-1)^3} = \tag{2.44}$$

$$(m_1 - m_2)\left\{\frac{f_{c1+}(m_1+m_2)\frac{f_{c2}}{2} + (m_1^2 + m_2^2 + m_1 m_2)\frac{f_{c3}}{6}}{z-1} + \frac{f_{c2+}(m_1+m_2+1)\frac{f_{c3}}{2}}{(z-1)^2} + \frac{f_{c3}}{(z-1)^3}\right\}$$

The delay factors for the HRZ DAC feedback are $m_1 = 0.5$ and $m_2 = 0$. Thus, the 3rd-order CT ΔΣ modulator coefficients can be calculated dependent on the DT loop filter coefficients, which they are:

$$f_{c3} = 2f_{d3}$$
$$f_{c2} = 2f_{d2} - \frac{3}{2}f_{d3} \tag{2.45}$$
$$f_{c1} = 2f_{d1} - \frac{1}{2}f_{d2} + \frac{7}{24}f_{d3}$$

In some cases, the DAC impulse responses may not be limited within one clock cycle and continue to the next. Therefore, equation (2.39) is not valid because the second delay factor becomes negative ($m_2 = 1 - \beta < 0$). In this case, the equation (2.39) can be rewritten as follows [18]:

$$\begin{aligned} H_d(z) &= Z\left\{\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s}H_c(s)\right\} = Z\left\{\frac{e^{-\alpha Ts} - e^{-Ts}e^{-(\beta T - T)s}}{s}H_c(s)\right\} \\ &= Z\left\{\frac{e^{-\alpha Ts}}{s}H_c(s)\right\} - z^{-1}.Z\left\{\frac{e^{-(\beta T - T)s}}{s}H_c(s)\right\} \\ &= Z_{m_1}\left\{\frac{H_c(s)}{s}\right\} - z^{-1}.Z_{m_2}\left\{\frac{H_c(s)}{s}\right\}, \quad m_1 = 1 - \alpha, \quad m_2 = 2 - \beta \end{aligned} \tag{2.46}$$

If an NRZ DAC with t_d delay and $\{\alpha T, \beta T\} = \{t_d, t_d + T\}$ is used, equation (2.46) leads to (2.47):

$$H_d(z) = (1 - z^{-1})Z_{m_1}\left\{\frac{H_c(s)}{s}\right\}, \quad m_1 = 1 - \alpha \tag{2.47}$$

Equation (2.47) illustrates that when the DAC pulse responses continue to the next clock cycle, the order of the CT ΔΣ modulator is increased by one and may cause instability. To have the same loop impulse response between the CT and DT ΔΣ modulator, the CT ΔΣ modulator should be modified which will be explained in detail in DAC non-idealities in CT ΔΣ modulators section.

2.7 DAC Non-idealities in CT ΔΣ modulators

In addition to the non-idealities of the integrators such as noise, distortion, finite dc gain and bandwidth in CT ΔΣ modulators, the second major error arises from the nonidealities of the feedback DAC [1]. All DAC errors are directly added to the input of the modulator through the first outermost feedback path and can

degrade the performance of the whole CT ΔΣ modulator due to the fact that the DAC errors are not shaped or attenuated by the CT loop filter [1].

The rectangular DAC waveforms are popular and widely used by designers [1]. The feedback DAC pulse is affected by timing errors, which varies the rising and falling edges and also the length of the DAC pulse. There are two different effects: first, the constant delay of the pulse by t_d, which is known as **"*excess loop delay*"** and second, the statistical variation of the any of the edge timing or even the duration of the sampling period T which are caused by clock jitter [1].

2.7.1 Excess Loop Delay in CT ΔΣ modulators

Any practical ADC takes time to make a decision. Thus, the feedback DAC will have to be clocked at a time t_d delayed from the sampling instant of the ADC. This delay, t_d, is termed as the excess loop delay [21].

$$t_d = \tau_d T \tag{2.48}$$

Excess loop delay is a problem in all CT ΔΣ modulators which needs to be dealt with carefully. This delay degrades the performance of the loop and too much delay can result in an unstable modulator [21]. Excess loop delay causes two different non-ideal effects in CT ΔΣ modulators which use RZ and NRZ DACs. Loop delay shifts the DAC pulse by t_d but retains the entire pulse in the actual sampling period in CT ΔΣ modulators with RZ DAC pulse as shown in Figure 2.10.

In this case, excess loop delay shifts feedback pulse from $\{\alpha T, \beta T\}$ to $\{\alpha T + t_d, \beta T + t_d\}$ which means that it affects the equivalence between the CT and DT loop filter. This delay causes a mismatch between designed and required modulator coefficients. Therefore, excess loop delay increases quantization IBN and reducing the stability of the modulator due to coefficients mismatch. However, the order of the modulator remains unchanged [1].

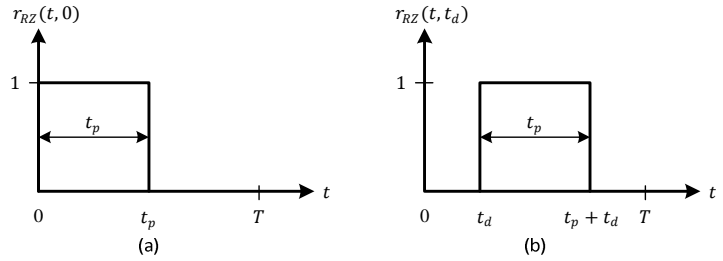


Figure 2.10: The RZ DAC pulse a) without delay and b) with t_d loop delay.

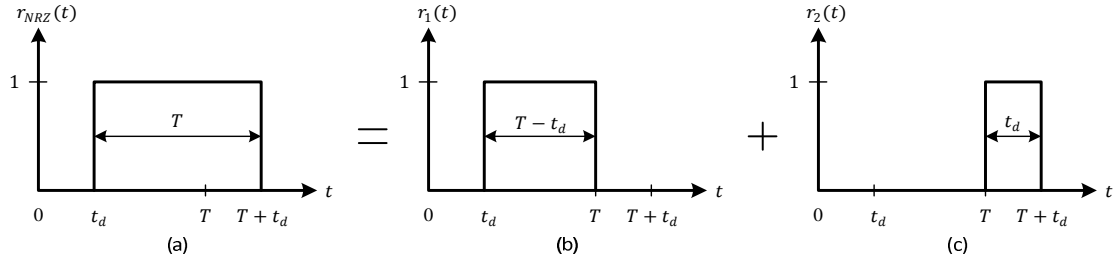


Figure 2.11: a) An NRZ DAC pulse with an excess loop delay t_d which is split into b) a DAC pulse in the present sample and c) a DAC pulse in the next sample interval.

In Contrast to RZ DAC pulses, any loop delay in CT ΔΣ modulators with NRZ DACs shifts a part of the feedback pulse into the next clock cycle as shown in Figure 2.11 and consequently increases the order of the modulator and decreases the depth of modulation, the noise shaping performance and also the stability of the modulator [34]. This happens in an RZ DAC pulse, if the delay t_d exceeds the time slot between the end of the pulse and the end of the sample: $t_d + \beta T > T$.

2.7.2 The Mitigating Effect for Excess Loop Delay in CT ΔΣ modulators

Several techniques for mitigating the effect of the excess loop delay have been proposed. For RZ DAC pulses, excess loop delay causes the coefficient mismatch and can be compensated by coefficient tuning which has been proposed in [22]. So the coefficients are calculated for new pulse positions $\{\alpha T + t_d, \beta T + t_d\}$ instead of the ideal ones $\{\alpha T, \beta T\}$. It should be noted that this technique only works when RZ pulses remain inside the one clock cycle and are not shifted to the next clock cycle [1][22].

For NRZ DAC pulses, excess loop delay causes the order of the modulator to be increased by one. In order to compensate the effect of excess loop delay, a technique has been proposed in [22] and shown in

Figure 2.12 can be utilized. An auxiliary HRZ DAC is added to the modulator to alleviate the influence of excess loop delay.

To calculate the new modulator coefficients k_i^*, the CT loop filter of the modulator shown in Figure 2.12 must be equal to the CT loop filter of the 2nd-order CT ΔΣ modulator with an ideal NRZ DAC feedback illustrated in Figure 2.8(b) and also the DT loop filter of the 2nd-order DT ΔΣ modulator shown in Figure 2.8(a). The new modulator coefficients are given by (2.49) [22].

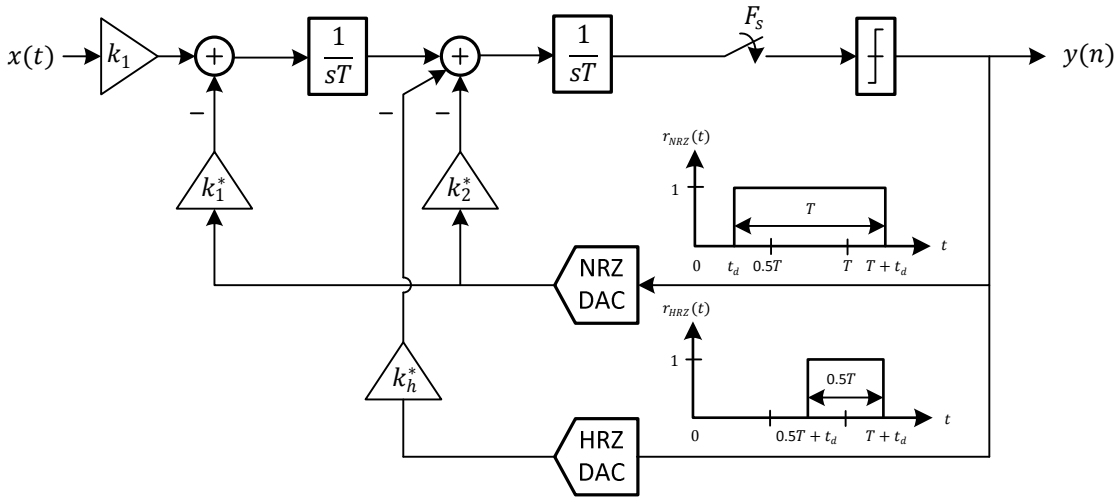


Figure 2.12: a 2nd-order CT ΔΣ modulator with an auxiliary HRZ DAC to compensate excess loop delay.

$$k_1^* = k_1, \quad k_2^* = \frac{3}{2}k_1\tau_d + 2k_2, \quad k_h^* = k_1\tau_d + 2k_2 \tag{2.49}$$

Where k_1^*, k_2^* and k_h^* are the coefficients of the compensated modulator in Figure 2.12, while $k_1$and k_2 are the coefficients of the ideal modulator in Figure 2.8(b).

Another method has been proposed in [23], is to add an additional feedback path as shown in Figure 2.13. The new modulator coefficients can be calculated like what has been done for the previous method and are given by (2.50).

$$k_1^* = k_1, \quad k_2^* = k_1\tau_d + k_2, \quad k_h^* = \frac{k_1{\tau_d}^2}{2} + k_2\tau_d \tag{2.50}$$

Where k_1^*, k_2^* and k_h^* are the coefficients of the compensated modulator in Figure 13, while $k_1$and k_2 are the coefficients of the ideal modulator in Figure 2.8(b) [1][23].

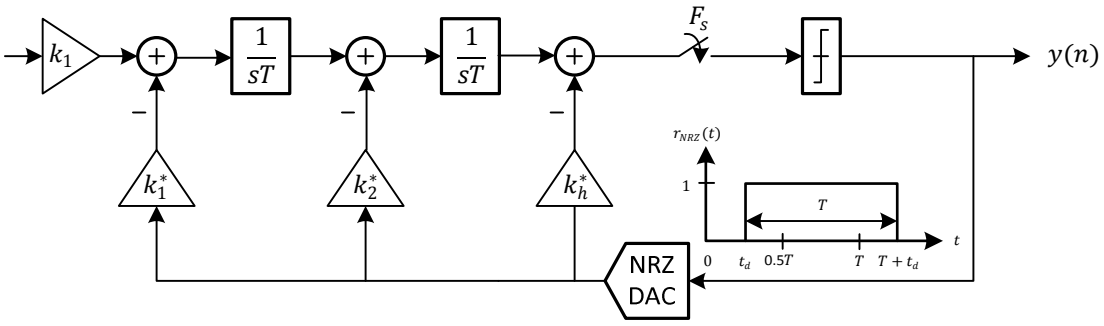


Figure 2.13: a 2nd-order CT ΔΣ modulator with an additional feedback path to compensate excess loop delay.

To cancel the influence of the excess loop delay, two techniques have been presented. The first technique shown in Figure 2.12 requires an auxiliary HRZ DAC to compensate the excess loop delay while the second technique shown in Figure 2.13 requires an additional feedback path from the same DAC block. The disadvantage of the first technique in comparison to the second is that it requires significant hardware in order to implement the auxiliary HRZ DAC which is really important in the design and implementation of CT ΔΣ modulators. It turns out that the compensation with either the additional feedback path or DAC even improves the modulator robustness.

2.8 Simulation Results on the Excess Loop Delay

Both 2nd-order CT ΔΣ modulators shown in Figure 2.8(b) and 2.13 have been simulated versus different values of the excess loop delay (τ_d). The excess loop delay is not compensated in the first modulator while it is compensated in the second modulator through the use of an additional feedback path. Both modulators are the CT equivalent of the 2nd-order DT ΔΣ modulator shown in Figure 2.8(a). The DT ΔΣ modulator has following specifications:

$a_1 = 0.5$ and $a_2 = 2.0$

$B = 3$ the number of bits of the quantizer

$OSR = 32$

In the first step, the coefficients of the 2nd-order CT ΔΣ modulator shown in Figure 2.8(b) are calculated from equations (2.35). The resulting coefficients are $k_1 = 1$ and $k_2 = 1.5$. In the second step, the resulting coefficients of the 2nd-order CT ΔΣ modulator shown in Figure 2.13 are calculated based on equations (2.50). The modulator's coefficients k_1^*, k_2^* and k_h^* are plotted in Figure 2.14 versus the excess loop delay (τ_d).

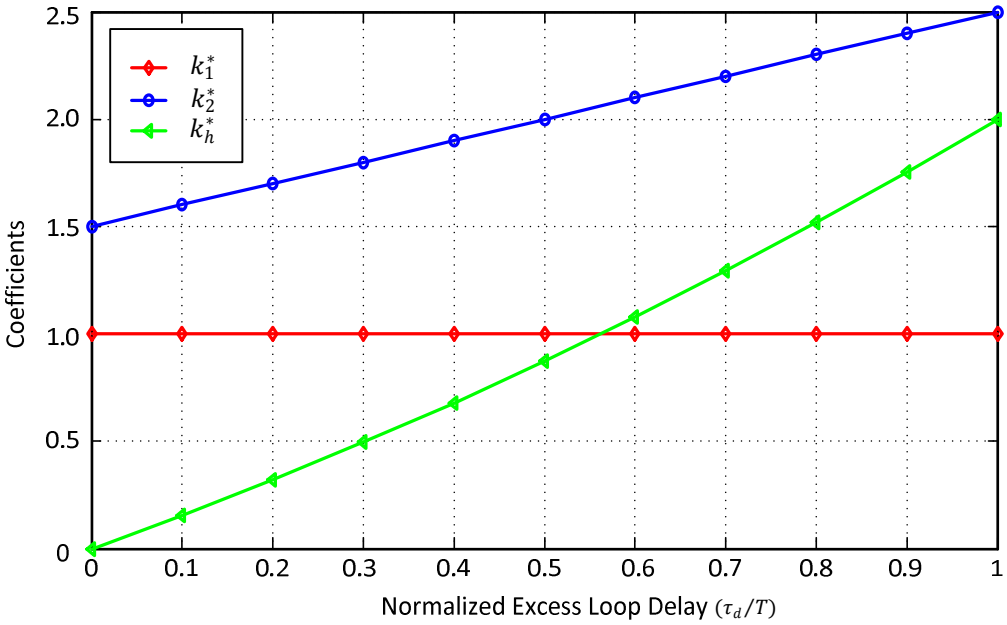


Figure 2.14: The modulator's coefficients k_1^*, k_2^* and k_h^* versus the excess loop delay (τ_d).

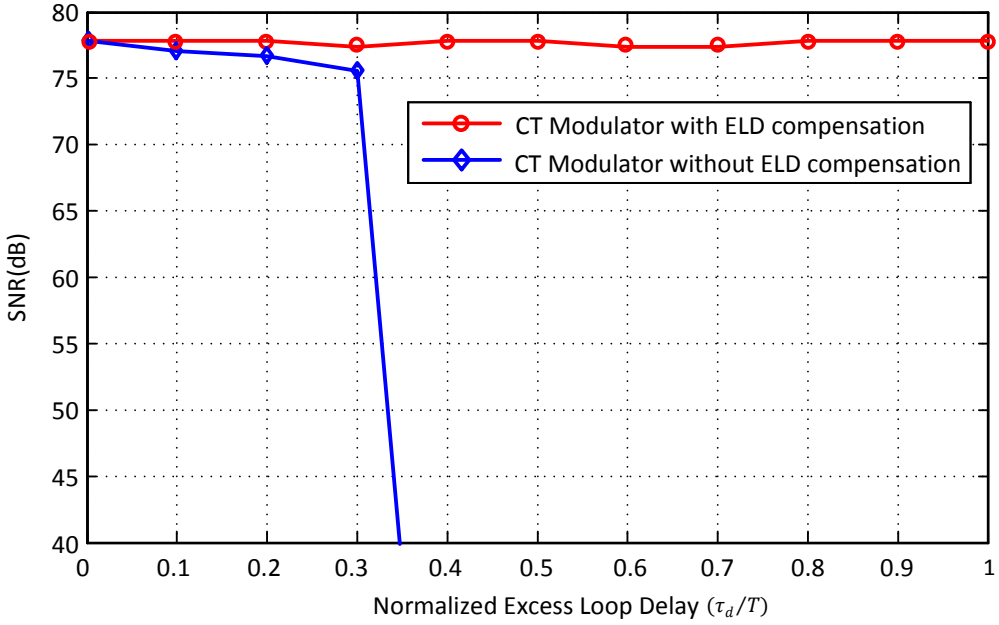


Figure 2.15: The SNRs of the both CT modulators versus the excess loop delay (τ_d).

Both CT modulators have been simulated versus different values of the excess loop delay (τ_d) and the SNRs are plotted in Figure 2.15. As can be seen, the SNR of the compensated modulator is flat and around 77.5dB versus different values of the excess loop delay (τ_d), but the SNR of the uncompensated modulator is flat when τ_d is less than $0.3T$ and when τ_d increases from $0.3T$, the modulator goes to an unstable mode and the SNR drops sharply.

2.9 Conclusion

In this chapter, a general structure of a noise-shaped ΔΣ modulator is presented and a linear model is deployed to obtain the STF and the NTF of the ΔΣ modulator. The effect of oversampling with noise-shaping on the signal and noise spectrum is illustrated in Figure 2.2. A formula is derived for calculating the maximum SNR of an Nth-order ΔΣ modulator and given by equation (2.19) which shows that the maximum SNR greatly depends on the OSR, the order of a modulator and the number of bits of the quantizer.

In this chapter, CT ΔΣ modulators are discussed and advantages and disadvantages of CT ΔΣ modulators in comparison to DT ΔΣ modulators are presented. Different types of popular DAC waveforms in time and s-domain are shown in Figure 2.7. There are two methods of converting a DT ΔΣ modulator to an equivalent CT ΔΣ modulator: the Impulse Invariant Transformation and the modified Z-transform which both methods are discussed in detail and a design example for each method is presented in section 2.6.3 and 2.6.5. A general formula for the CT-to-DT transformation is presented in Table 2.2 and the way this formula is derived is discussed in detail in Appendix B.

Finally, the last section of this chapter is dedicated to DAC non-idealities in CT ΔΣ modulators. The excess loop delay problem in CT ΔΣ modulators is introduced in this chapter and two techniques for mitigating the effect of the excess loop delay have been proposed.

Chapter 3:
TI ΔΣ Modulators

3.1 TI ΔΣ modulators

The procedure for the design of a ΔΣ modulator is based on choosing: the order and architecture of the ΔΣ modulator, the OSR and the number of bits for the quantizer. By using the time-interleaving technique and M interconnected parallel modulators that are working concurrently, the effective sampling rate and the OSR become M times the clock rate and the OSR of each modulator respectively [24][25]. It should be noted that the required resolution can be acquired without increasing the order of the modulator or the number of bits for the quantizer and also without utilizing a state of the art technology.

According to equation (2.19), the maximum SNR is calculated and presented in Table 3.1 for a ΔΣ modulator with OSR=16 which the order of the modulator (N) varies from 1 to 5 and the number of bits for the quantizer (B) changes from 1 to 5. To avoid complexity and dealing with the stability problem of the ΔΣ modulators, the minimum order which satisfies the system requirements is chosen. This work is designed for WIFI applications of 12bit or more resolution. Therefore a ΔΣ modulator with the order of three and 4-bit resolution is chosen. The maximum SNR of this modulator is 88.75dB based on the equation (2.19).

Table 3.1: The maximum SNR of a ΔΣ modulator based on the equation (2.19).

$SNR_{max}(dB)$	$N=1$	$N=2$	$N=3$	$N=4$	$N=5$
$B=1$	38.73	55.09	70.69	85.92	100.93
$B=2$	44.75	61.11	76.71	91.94	106.95
$B=3$	50.77	67.13	82.73	97.96	112.97
$B=4$	56.79	73.15	88.75	103.98	118.99
$B=5$	62.81	79.17	94.77	110.00	125.01

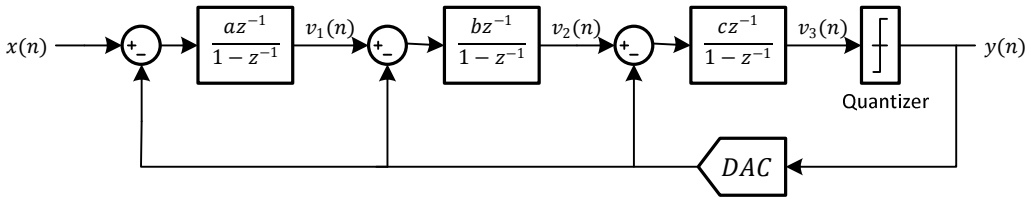


Figure 3.1: A 3rd-order conventional single-loop DT ΔΣ modulator.

3.2 Derivation of the DTTI ΔΣ modulator

The 3rd-order single path DTTI ΔΣ modulator is derived directly from the time domain node equations of its conventional DT ΔΣ modulator as shown in Figure 3.1. It is assumed that the DAC in the feedback loop is ideal ($H_{DAC}(z) = 1$). The time domain equations of the modulator are written for two consecutive time slots (2n)th and (2n+1)th as follows [26]:

$$v_1(2n) = ax(2n-1) - ay(2n-1) + v_1(2n-1) \quad (3.1.a)$$

$$v_2(2n) = bv_1(2n-1) - by(2n-1) + v_2(2n-1) \quad (3.1.b)$$

$$v_3(2n) = cv_2(2n-1) - cy(2n-1) + v_3(2n-1) \quad (3.1.c)$$

$$y(2n) = Q[v_3(2n)] \quad (3.1.d)$$

and

$$v_1(2n+1) = ax(2n) - ay(2n) + v_1(2n) \quad (3.2.a)$$

$$v_2(2n+1) = bv_1(2n) - by(2n) + v_2(2n) \quad (3.2.b)$$

$$v_3(2n+1) = cv_2(2n) - cy(2n) + v_3(2n) \quad (3.2.c)$$

$$y(2n+1) = Q[v_3(2n+1)] \quad (3.2.d)$$

where $Q[.]$ represents the quantization function. The input $x(n)$ is distributed between two channels through an input multiplexer which operates at twice the clock frequency of each channel. The input $x(n)$ is relabelled as follows:

$$x_1(n) = x(2n) \ , \ x_2(n) = x(2n-1) \quad (3.3)$$

Similarly, the other nodes of the modulator are relabelled:

$$v_{11}(n) = v_1(2n) \ , \ v_{12}(n) = v_1(2n-1) \quad (3.4.a)$$

$$v_{21}(n) = v_2(2n) \ , \ v_{22}(n) = v_2(2n-1) \tag{3.4.b}$$

$$v_{31}(n) = v_3(2n) \ , \ v_{32}(n) = v_3(2n-1) \tag{3.4.c}$$

$$y_1(n) = y(2n) \ , \ y_2(n) = y(2n-1) \tag{3.4.d}$$

Equation sets (3.5) and (3.6) are derived by substituting equation set (3.4) and equation (3.3) into equation sets (3.1) and (3.2) respectively as follows:

$$v_{11}(n) = ax_2(n) - ay_2(n) + v_{12}(n) \tag{3.5.a}$$

$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \tag{3.5.b}$$

$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \tag{3.5.c}$$

$$y_1(n) = Q[v_{31}(n)] \tag{3.5.d}$$

and

$$v_{12}(n+1) = ax_1(n) - ay_1(n) + v_{11}(n) \tag{3.6.a}$$

$$v_{22}(n+1) = bv_{11}(n) - by_1(n) + v_{21}(n) \tag{3.6.b}$$

$$v_{32}(n+1) = cv_{21}(n) - cy_1(n) + v_{31}(n) \tag{3.6.c}$$

$$y_2(n) = Q[v_{32}(n)] \tag{3.6.d}$$

Equation set (3.7) can be rewritten as equation set (3.7):

$$v_{12}(n) = ax_1(n-1) - ay_1(n-1) + v_{11}(n-1) \tag{3.7.a}$$

$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \tag{3.7.b}$$

$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \tag{3.7.c}$$

Equation set (3.8) is derived by substituting equation set (3.7) into equation sets (3.5) as follows:

$$v_{11}(n) = ax_2(n) - ay_2(n) + ax_1(n-1) - ay_1(n-1) + v_{11}(n-1) \tag{3.8.a}$$

$$v_{21}(n) = bv_{12}(n) - by_2(n) + bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \tag{3.8.b}$$

$$v_{31}(n) = cv_{22}(n) - cy_2(n) + cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \tag{3.8.c}$$

The z-transform of the equation sets (3.5) and (3.8) are given by the equation set (3.9) as follows:

$$V_{11}(z) = \frac{a\{(X_1(z) - Y_1(z))z^{-1} + X_2(z) - Y_2(z)\}}{1 - z^{-1}} \tag{3.9.a}$$

$$V_{21}(z) = \frac{b\{(V_{11}(z) - Y_1(z))z^{-1} + V_{12}(z) - Y_2(z)\}}{1 - z^{-1}} \tag{3.9.b}$$

$$V_{31}(z) = \frac{c\{(V_{21}(z) - Y_1(z))z^{-1} + V_{22}(z) - Y_2(z)\}}{1 - z^{-1}} \tag{3.9.c}$$

$$V_{12} = a\big(Y_2(z) - X_2(z)\big) + V_{11}(z) = \frac{az^{-1}}{1 - z^{-1}}(X_1(z) + X_2(z) - Y_1(z) - Y_2(z)) \tag{3.9.d}$$

$$V_{22} = b\big(Y_2(z) - V_{12}(z)\big) + V_{21}(z) = \frac{bz^{-1}}{1 - z^{-1}}(V_{11}(z) + V_{12}(z) - Y_1(z) - Y_2(z)) \tag{3.9.e}$$

$$V_{32} = c\big(Y_2(z) - V_{22}(z)\big) + V_{31}(z) = \frac{cz^{-1}}{1 - z^{-1}}(V_{21}(z) + V_{22}(z) - Y_1(z) - Y_2(z)) \tag{3.9.f}$$

The 3rd-order two-path DTTI ΔΣ modulator which is shown in Figure 3.2 is derived directly from the frequency domain equation set (3.9).

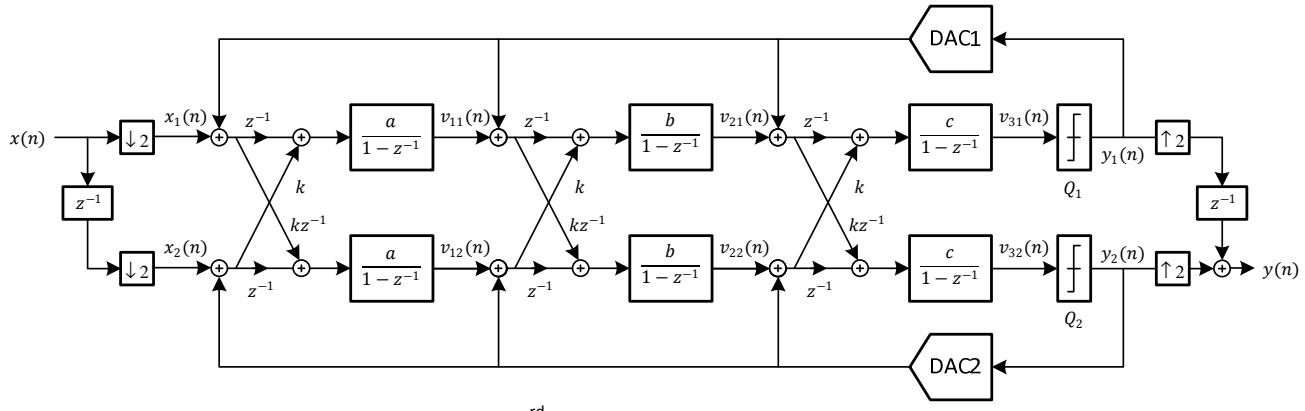


Figure 3.2: A 3rd-order two-path DTTI ΔΣ modulator.

DC offsets of integrators do not typically pose any problem for conventional modulators since they only cause an offset error in the overall dc characteristic function of the converter [24]. Also, the outputs of the integrators stay in the non-clipping range due to feedback. The effect of offsets on a TI modulator is not quite the same as they have on the conventional single-loop modulator. Consider the 3rd-order two-path DTTI ΔΣ modulator depicted in Figure 3.2 and assume that the cross-coupling coefficients $k = 1$, $x(n) = 0$, $y_1(n) = L$ and $y_2(n) = -L$, the offset of the first path is positive and the offset of the second path is negative, then $y_1(n)$ and $y_2(n)$ cancel each other and the first path is saturated to the positive supply and the second path is saturated to the negative supply. When the cross-coupling coefficients are less than unity ($k < 1$), then

each branch has more control on its own feedback as compared to the cross-coupling branch. The total feedback $L(1-k)$ is cable of cancelling the effect of offsets the same way as in a conventional modulator. Note that the deviation of k from unity does not cause aliasing since the pseudo-circulant condition is still satisfied and hence the structure remains time-invariant. However, the poles and zeros of the STF and NTF are displaced [24].

By sharing only one set of integrators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. The effect of offset mismatch between integrators is also cancelled by using single-path technique. Hence equation (3.3) results in (3.10) as follows:

$$x_1(n) = x_2(n) = x(n) \tag{3.10}$$

Equation sets (3.11) and (3.12) are derived by substituting equation (3.10) into equation sets (3.5) and (3.7) respectively as follows:

$$v_{11}(n) = ax(n) - ay_2(n) + v_{12}(n) \tag{3.11.a}$$

$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \tag{3.11.b}$$

$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \tag{3.11.c}$$

and

$$v_{12}(n) = ax(n-1) - ay_1(n-1) + v_{11}(n-1) \tag{3.12.a}$$

$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \tag{3.12.b}$$

$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \tag{3.12.c}$$

Equation set (3.13) is derived by further substituting equation set (3.11) into equation set (3.12).

$$v_{12}(n) = 2ax(n-1) - a(y_1(n-1) + y_2(n-1)) + v_{12}(n-1) \tag{3.13.a}$$

$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - b(y_1(n-1) + (1+a)y_2(n-1)) + v_{22}(n-1) \tag{3.13.b}$$

$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - c(y_1(n-1) + (1+b)y_2(n-1)) + v_{32}(n-1) \tag{3.13.c}$$

The 3rd-order single-path DTTI ΔΣ modulator which is shown in Figure 3.3 is derived directly from the time domain equation sets (3.11) and (3.13).

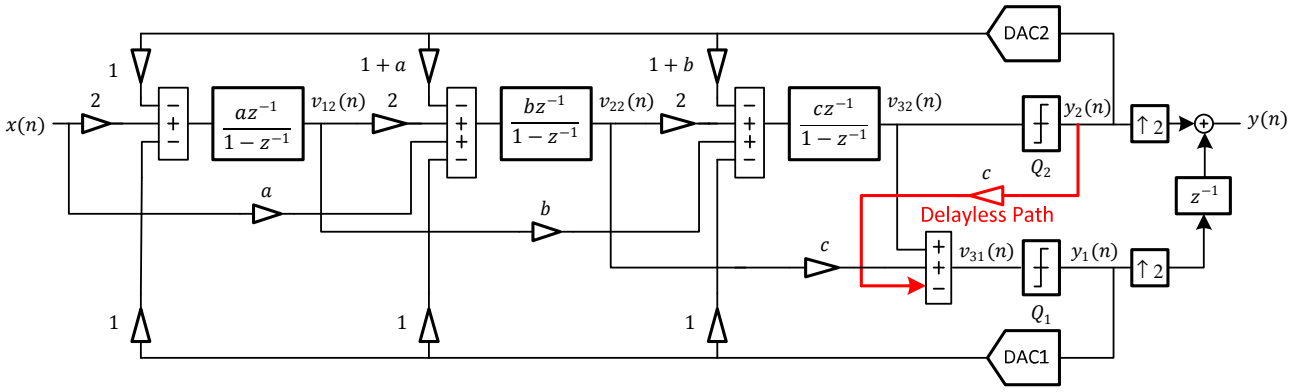


Figure 3.3: A 3rd-order single-path DTTI ΔΣ modulator.

The motive behind sharing one set of integrators is to eliminate the instability that can arise due to the DC offset mismatch of the two individual integrator set based two channel interleaving case. The DTTI ΔΣ modulators need an input demultiplexer which samples the input signal at the highest clock frequency of the DTTI ΔΣ modulator and distributes it between channels. This fast demultiplexer is a limiting factor for the performance of the DTTI ΔΣ modulators. This architecture does not need an input demultiplexer and the input signal is shared between channels [7][25]. Removing the input demultiplexer has no effect on the NTF of the DTTI ΔΣ modulator but it causes some notches in its STF at the following frequencies: $0.5F_{clk}, 1.5F_{clk}, 2.5F_{clk}$, $3.5F_{clk}$, … which is shown in Figure 3.11 where F_{clk} is the clock frequency of the DTTI ΔΣ modulator [25].

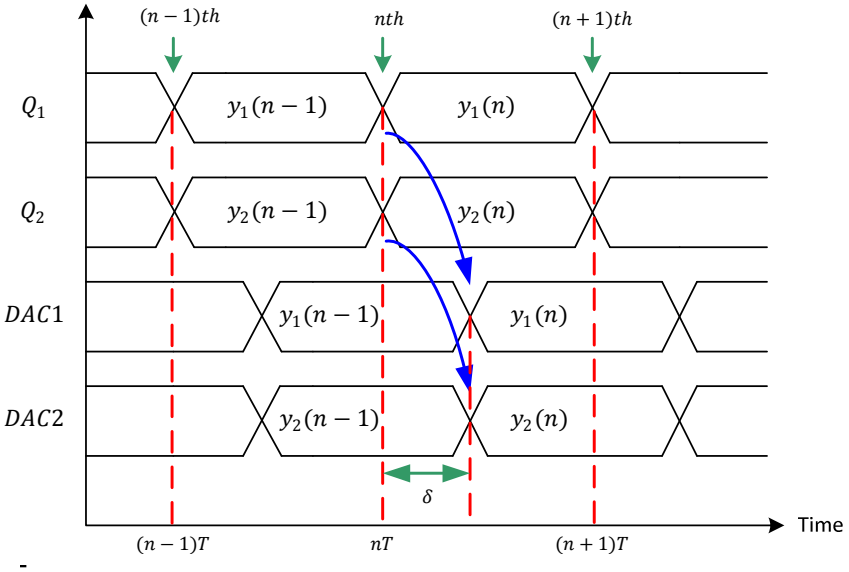


Figure 3.4: The outputs of Q1, Q2, DAC1 and DAC2.

3.3 Delayless Feedback Path Problem in TI ΔΣ Modulators

This is the issue that forms the focus of this PhD program which to our best knowledge, has not been effectively solved and reported in the open literature. This issue makes implementation of the single-path TI ΔΣ modulators impractical and it is called the **"delayless feedback path"** problem that comes from equation (3.11.c) in which $v_{31}(n)$ (the input of quantizer Q1) is directly linked to $y_2(n)$. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay [27]! One method to eliminate the delayless path is to move this feedback to the digital domain instead of performing it in the analog domain [27] as shown in Figure 3.5. The disadvantage of this method is that the first quantizer (Q1) requires more comparators than the number of the comparators in the second quantizer (Q2) [27]. The second method is to use a sample-and-hold in front of the first quantizer (Q1) and quantizing the signal when the output of DAC2 is ready [7] as shown in Figure 3.6. This method needs a complicated timing generator, a sample-and-hold and also faster integrators.

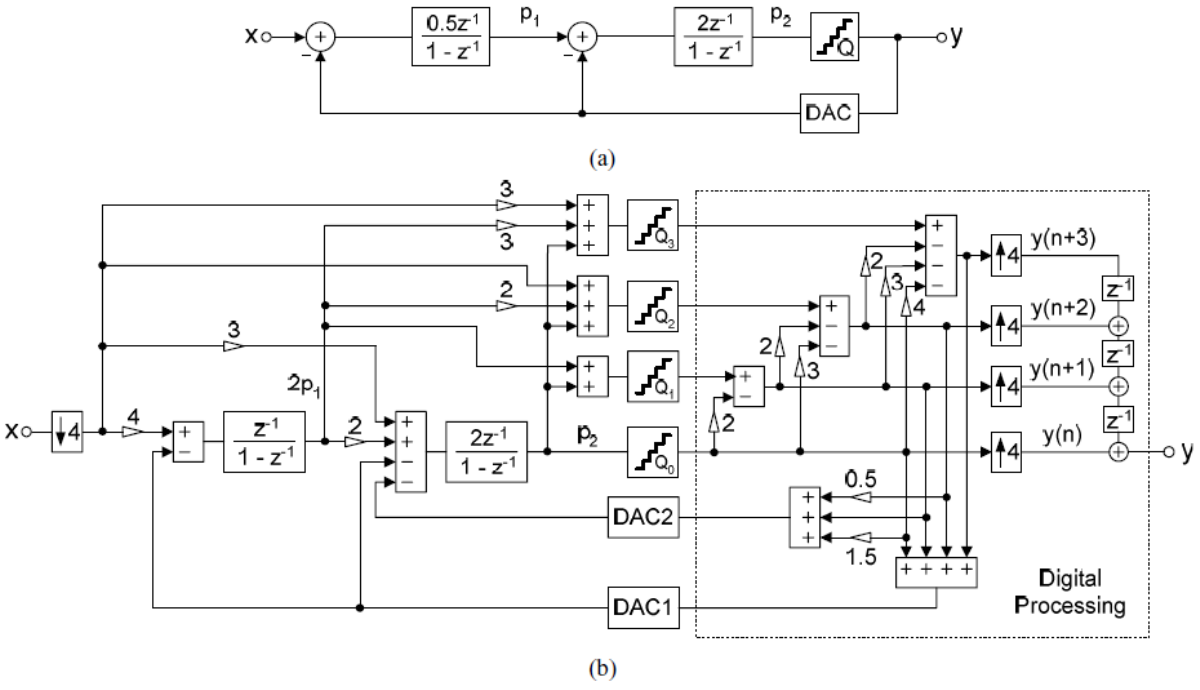


Figure 3.5: 2nd-order ΔΣ modulator. (a) Conventional single-path. (b) 4-path TI based on the first method [27].

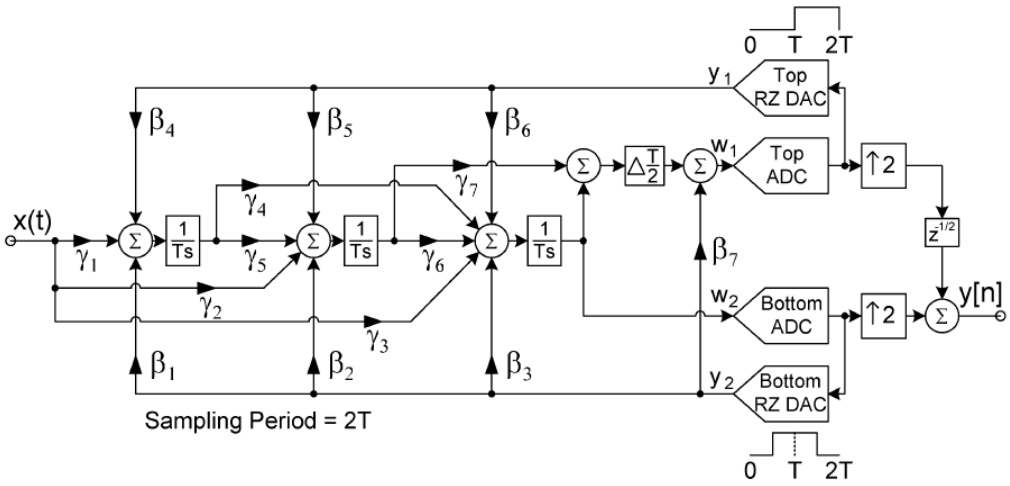


Figure 3.6: A 3rd-order CTTI ΔΣ modulator based on the second method [7].

The third method which is our proposed novel method is based on an error correction technique. We intentionally induce an error in the analog domain through the use of the output of DAC2 as shown in Figure 3.7. The error is substantially corrected in the digital domain which effectively eliminates the delayless feedback path. To better understand how this works we shall perform a step by step mathematical analysis of what happens. The timing diagram as depicted in Figure 3.4 shows the delay from the outputs of quantizers Q1 and Q2 and their propagation through to the outputs of DAC1 and DAC2 as δ. As a result the output of DAC2 that is sampled at the nth time slot is $y_2(n-1)$ where in practice we should have had $y_2(n)$. To overcome this inconsistency we look at the input and output of Q1, as depicted in Figure 3.3. Quantizer Q1 quantizes the signal $v_{31}(n)$ as follows:

$$y_1(n) = Q[v_{31}(n)] \tag{3.14}$$

Equation (3.15) is derived by substituting (3.11.c) into (3.14):

$$y_1(n) = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \tag{3.15}$$

The output of DAC2 is used in (3.16) and equation (3.15) is rewritten as:

$$y_1(n) = Q[cv_{22}(n) - cy_2(n-1) + v_{32}(n)] + cy_2(n-1) - cy_2(n) \tag{3.16}$$

The output of Q1 is called $y_1^*(n)$ in (3.17):

$$y_1(n) = y_1^*(n) + cy_2(n-1) - cy_2(n) \tag{3.17}$$

$$error = c\Delta y = c(y_2(n-1) - y_2(n)) \tag{3.18}$$

$$Y_1(z) = Y_1^*(z) - c(1 - z^{-1})Y_2(z) \tag{3.19}$$

As stated in (3.17), $y_1^*(n)$ (the output of Q1) needs to be corrected before it is applied to the input of DAC1; otherwise it causes instability in the modulator as it will change the modulator's dynamics by increasing its order by one. A first order differencer block $(1 - z^{-1})$ is used to perform this correction as described in (3.19).

Equation (3.19) illustrates the point that Q1 is able to quantize its input without any additional circuit in the analog domain by merely using the output of DAC2. The differencer block $(1 - z^{-1})$ only corrects the error in equation (3.17) and it has no effect on the quantization error or the signal in the proposed structure. The proposed 3rd-order single-path DTTI ΔΣ modulator is shown in Figure 3.7.

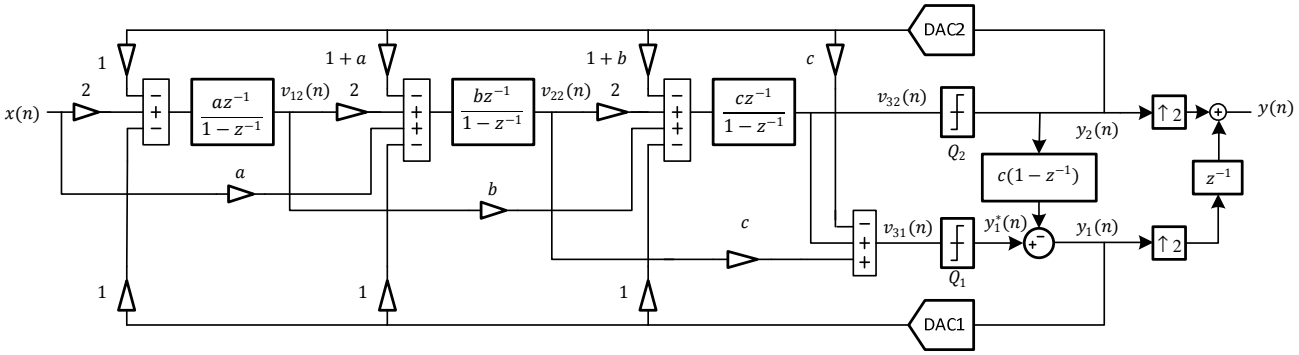


Figure 3.7: The proposed 3rd-order single-path DTTI ΔΣ modulator.

Table 3.2: Comparison of the first, the second and our proposed method.

	Comparators count for Q_1	*Comparators count for Q_2*	*Advantage*	*Disadvantage*
First Method [27]	48	16	Less hardware required	32 more comparators required for Q_1
Second Method [7]	16	16	Less comparators required	A sample-and-hold, a complicated timing generator and faster integrators required.
Proposed Method	32	16	Less hardware required	16 more comparators required for Q_1

The signal swing at the input of quantizer Q1 is increased in the first and the proposed methods because scaling is not an option and it will lead to loss of SNR, the first and the proposed methods require 48 and 32 comparators for quantizer Q1 respectively, in comparison to the second method which requires 16

comparators as depicted in Table 3.2. The significant advantages and disadvantages of all three methods have been summarized in Table 3.2.

3.4 Derivation of CTTI ΔΣ Modulators

The CTTI ΔΣ modulator equivalent of the DTTI ΔΣ modulator of Figure 3.7 can be obtained in three steps and the modulator's additive white noise model for quantizers is used as follows: The first step is to determine the loop filters of the DTTI ΔΣ modulator. In this design, the DTTI ΔΣ modulator has six loop filters $FF_{1d}(z)$, $FF_{2d}(z)$, $H_{1d}(z)$, $H_{2d}(z)$, $H_{3d}(z)$ and $H_{4d}(z)$ which can be determined with the help of the symbolic toolbox of MATLAB. These loop filters for the DTTI ΔΣ modulator are depicted in Figure 3.8(a). The second step is to convert the DT loop filters into equivalent CT loop filters through the use of either the impulse-invariant transformation or the modified z-transform [1][7][25]. The equivalent CTTI ΔΣ modulator is shown in Figure 3.8(b) where the DT loop filters of Figure 3.8(a) have been replaced with the equivalent CT loop filters $FF_{1c}(s)$, $FF_{2c}(s)$, $H_{1c}(s)$, $H_{2c}(s)$, $H_{3c}(s)$ and $H_{4c}(s)$. The third step is to convert the modulator of Figure 3.8(b) into a CTTI ΔΣ modulator which has the same order as the DTTI ΔΣ modulator.

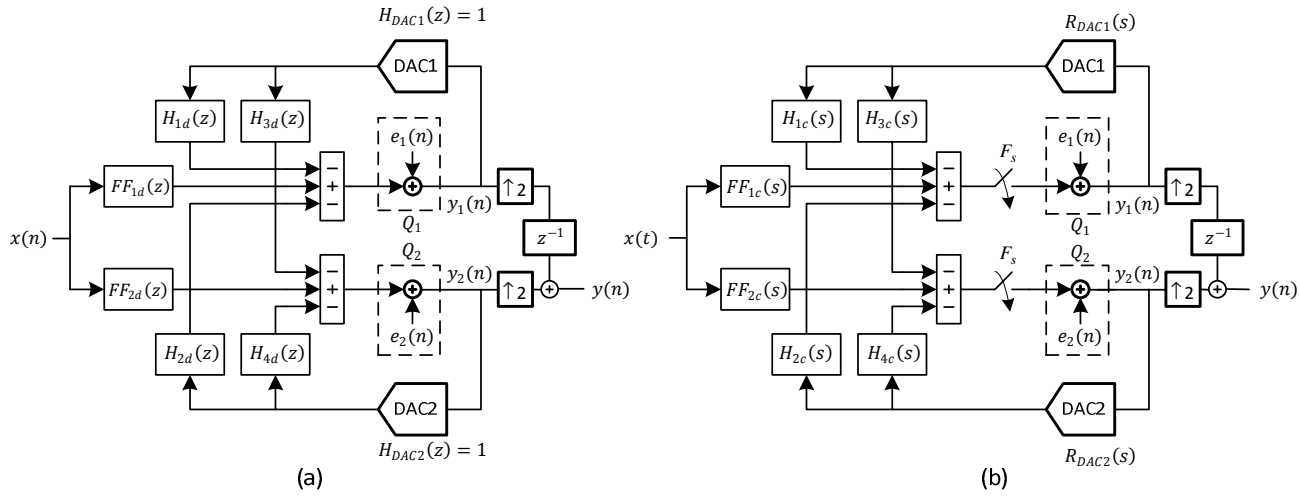


Figure 3.8: The block diagrams of a) a DTTI ΔΣ modulator and b) a CTTI ΔΣ modulator which shows their loop filters.

The six loop filters $FF_{1d}(z)$, $FF_{2d}(z)$, $H_{1d}(z)$, $H_{2d}(z)$, $H_{3d}(z)$ and $H_{4d}(z)$ of the 3rd-order DTTI ΔΣ modulator shown in Figure 3.7 are given by the equation set (3.20) as follows:

$$H_{1d}(z) = \frac{4abc}{(z-1)^3} + \frac{(3a+2)bc}{(z-1)^2} + \frac{(b+1)c}{z-1} \tag{3.20.a}$$

$$H_{2d}(z) = \frac{4abc}{(z-1)^3} + \frac{(5a+2)bc}{(z-1)^2} + \frac{abc+2bc+c}{z-1} + c \tag{3.20.b}$$

$$H_{3d}(z) = \frac{4abc}{(z-1)^3} + \frac{(a+2)bc}{(z-1)^2} + \frac{c}{z-1} \tag{3.20.c}$$

$$H_{4d}(z) = \frac{4abc}{(z-1)^3} + \frac{(3a+2)bc}{(z-1)^2} + \frac{(1+b)c}{z-1} \tag{3.20.d}$$

$$FF_{1d}(z) = \frac{8abc}{(z-1)^3} + \frac{8abc}{(z-1)^2} + \frac{abc}{z-1} \tag{3.20.e}$$

$$FF_{2d}(z) = \frac{8abc}{(z-1)^3} + \frac{4abc}{(z-1)^2} \tag{3.20.f}$$

An equivalent 3rd-order CTTI ΔΣ modulator of the DTTI ΔΣ modulator in Figure 3.7 which uses NRZ DACs with delay time t_d has been shown in Figure 3.9. To overcome the excess-loop delay issue, two additional feedback paths from the outputs of DAC1 and DAC2 to the inputs of each quantizer (Q1 and Q2) are used. The loop filters of the modulator as shown in Figure 3.9 can be found and matched to those in Figure 3.8(a) to determine the CTTI ΔΣ modulator coefficients k_1, k_2, k_3, k_4, k_5, k_6, k_7, f_{c1}, f_{c2}, f_{c3}, f_{c4}, f_{c5}, f_{c6}, f_{c7}, f_{c8}, f_{c9} and f_{c10} in Figure 3.9 by using the modified z-transform. This is achieved by using the symbolic toolbox of MATLAB.

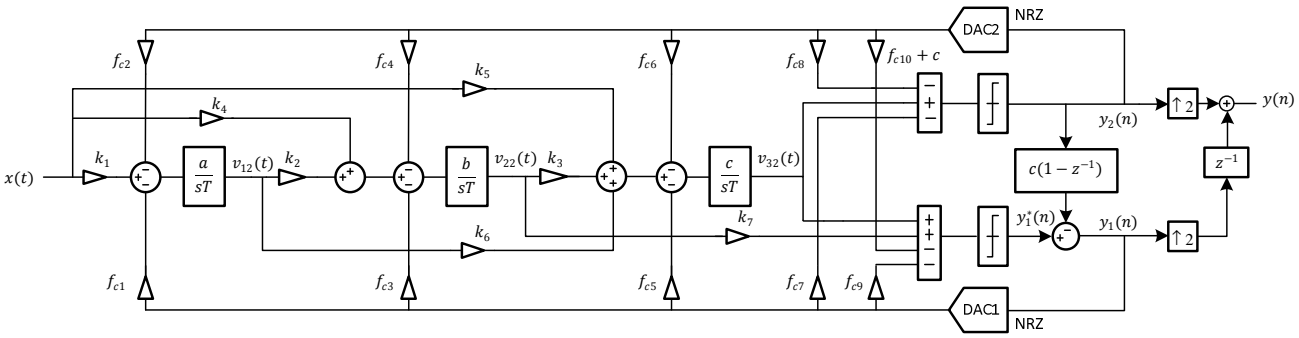


Figure 3.9: The proposed 3rd-order single-path CTTI ΔΣ modulator.

The six loop filters $FF_{1c}(s)$, $FF_{2c}(s)$, $H_{1c}(s)$, $H_{2c}(s)$, $H_{3c}(s)$ and $H_{4c}(s)$ of the 3rd-order CTTI ΔΣ modulator shown in Figure 3.9 are given by the equation set (3.21). For sake of simplicity, we assume that $T = 1$.

$$H_{1c}(s) = \frac{f_{c1}k_2k_3abc}{(sT)^3} + \frac{f_{c1}k_2k_7ab + f_{c1}k_6ac + f_{c3}k_3bc}{(sT)^2} + \frac{f_{c3}k_7b + f_{c5}c}{sT} + f_{c9} \tag{3.21.a}$$

$$H_{2c}(s) = \frac{f_{c2}k_2k_3abc}{(sT)^3} + \frac{f_{c2}k_2k_7ab + f_{c2}k_6ac + f_{c4}k_3bc}{(sT)^2} + \frac{f_{c4}k_7b + f_{c6}c}{sT} + f_{c10} + c \tag{3.21.b}$$

$$H_{3c}(s) = \frac{f_{c1}k_2k_3abc}{(sT)^3} + \frac{f_{c1}k_6ac + f_{c3}k_3bc}{(sT)^2} + \frac{f_{c5}c}{sT} + f_{c7} \tag{3.21.c}$$

$$H_{4c}(s) = \frac{f_{c2}k_2k_3abc}{(sT)^3} + \frac{f_{c2}k_6ac + f_{c4}k_3bc}{(sT)^2} + \frac{f_{c6}c}{sT} + f_{c8} \tag{3.21.d}$$

$$FF_{1c}(s) = \frac{k_1k_2k_3abc}{(sT)^3} + \frac{k_1k_2k_7ab + k_1k_6ac + k_4k_3bc}{(sT)^2} + \frac{k_4k_7b + k_5c}{sT} \tag{3.21.e}$$

$$FF_{2c}(s) = \frac{k_1k_2k_3abc}{(sT)^3} + \frac{k_1k_6ac + k_4k_3bc}{(sT)^2} + \frac{k_5c}{sT} \tag{3.21.f}$$

The z-domain equivalents of the CT loop filters have been presented by the equation set (3.21) can be found by using the modified z-transform and matched to those in the equation set (3.20) in order to determine the CTTI ΔΣ modulator coefficients $k_1,\ k_2,\ k_3,\ k_4,\ k_5,\ k_6, k_7,\ f_{c1},\ f_{c2},\ f_{c3},\ f_{c4},\ f_{c5},\ f_{c6},\ f_{c7},\ f_{c8},\ f_{c9}$ and f_{c10} in Figure 3.9. Theses coefficients are given by the equation set (3.22).

$$m = 1 - \frac{t_d}{T} = 1 - \tau_d \tag{3.22.a}$$

$$k_1 = k_2 = k_3 = 2, \quad k_4 = -a, \quad k_5 = \frac{2}{3}ab, \quad k_6 = -b, \quad k_7 = c \tag{3.22.b}$$

$$f_{c1} = f_{c2} = 1 \tag{3.22.c}$$

$$f_{c3} = 1 + a(1 - 2m) \tag{3.22.d}$$

$$f_{c4} = 1 + a(2 - 2m) \tag{3.22.e}$$

$$f_{c5} = ab\left(2m^2 - m - \frac{1}{6}\right) + b(1 - 2m) + 1 \tag{3.22.f}$$

$$f_{c6} = ab\left(2m^2 - 3m + \frac{5}{6}\right) + b(2 - 2m) + 1 \tag{3.22.g}$$

$$f_{c7} = abc\left(-\frac{2}{3}m^3 + \frac{1}{2}m^2 + \frac{1}{6}m\right) + bc(m^2 - m) + c(1 - m) \tag{3.22.h}$$

$$f_{c8} = abc\left(-\frac{2}{3}m^3 + \frac{3}{2}m^2 - \frac{5}{6}m\right) + bc(m^2 - 2m + 1) + c(1 - m) \tag{3.22.i}$$

$$f_{c9} = abc\left(-\frac{2}{3}m^3 + \frac{3}{2}m^2 - \frac{5}{6}m\right) + bc(m^2 - 2m + 1) + c(1 - m) \tag{3.22.j}$$

$$f_{c10} = abc\left(-\frac{2}{3}m^3 + \frac{5}{2}m^2 - \frac{17}{6}m + 1\right) + bc(m^2 - 3m + 2) + c(1 - m) \tag{3.22.k}$$

The resulting 3rd-order CTTI ΔΣ modulator has been shown in Figure 3.10. The OSR of the overall modulator shown in Figure 3.9 from $x(t)$ to $y(t)$ is 16 and has been designed to operate at 320MHz clock frequency for a 10MHz signal bandwidth. The resolution of Q1 and Q2 are 5bits and 4bits respectively. After correcting the error as stated by equation (3.18) in the digital domain, $y_1(n)$ will be 4bits in length. Therefore, DAC1 and DAC2 both require 4bit DACs. In general, to simplify the design, the scaling coefficient c which is multiplied by the first order differencer $(1 - z^{-1})$ in the digital domain should be chosen to be a number which is a power of two. This choice results in replacing the potentially complicated multiplier with a simple hard-wired shift.

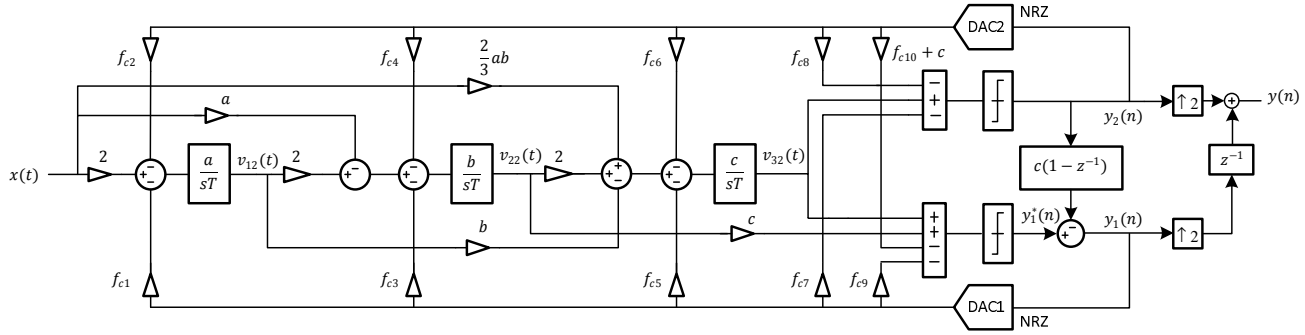


Figure 3.10: The 3rd-order single-path CTTI ΔΣ modulator.

3.5 STFs and NTFs of the DTTI and CTTI ΔΣ Modulators

The signal and noise transfer functions of the DTTI ΔΣ modulator of Figure 8(a) can be formulated by performing the following algebraic analysis:

$$Y(z) = Y_1(z^2)z^{-1} + Y_2(z^2) \tag{3.23}$$

$$Y(z) = STF_d(z)X(z) + NTF_{1d}(z)E_1(z) + NTF_{2d}(z)E_2(z) \tag{3.24}$$

$$NTF_{1d} = \frac{H_{3d}(z^2) + [1 - H_{4d}(z^2)]z^{-1}}{[1 - H_{1d}(z^2)][1 - H_{4d}(z^2)] - H_{2d}(z^2)H_{3d}(z^2)} \tag{3.25}$$

$$NTF_{2d} = \frac{[1 - H_{1d}(z^2)] + H_{2d}(z^2)z^{-1}}{[1 - H_{1d}(z^2)][1 - H_{4d}(z^2)] - H_{2d}(z^2)H_{3d}(z^2)} \tag{3.26}$$

$$STF_d(z) = FF_{1d}(z^2)NTF_{1d}(z) + FF_{2d}(z^2)NTF_{2d}(z) \tag{3.27}$$

Where $STF_d(z), NTF_{1d}(z)$ and $NTF_{2d}(z)$ represent the signal transfer function from $x(t)$ to $y(n)$, the noise transfer function from $e_1(n)$ to $y(n)$ and the noise transfer function from $e_2(n)$ to $y(n)$ respectively. The z^2 terms in (3.23) show the effect of the up-samplers in the modulator. The NTFs of the DTTI ΔΣ modulator of Figure 3.8(a) and its equivalent CTTI ΔΣ modulator of Figure 3.8(b) are the same. To derive the *STF* of the CTTI ΔΣ modulator ($STF_c(s)$), both $NTF_{1d}(z)$ and $NTF_{2d}(z)$ are used and the $STF_c(s)$ is given in (3.28):

$$STF_c(s) = FF_{1c}(s)NTF_{1d}(z) + FF_{2c}(s)NTF_{2d}(z) \tag{3.28}$$

By substituting $z = e^{j2\pi f}$ and $s = j2\pi f$ in (3.25), (3.26), (3.27) and (3.28), the STFs of the DTTI and CTTI ΔΣ modulator are plotted in Figure 3.11. $STF_c(s)$ has some notches in $F_{clk}, 2F_{clk}, 3F_{clk}, \ldots$ frequency. As explained in chapter 2 by equation (2.30), the effect of sampler is noticeable because $STF_c(s)$ is attenuated over the frequency. Since both $NTF_{1d}(z)$ and $NTF_{2d}(z)$ have an identical amplitude, only $NTF_{1d}(z)$ is plotted in Figure 3.12 and is compared to the NTF of the conventional DT ΔΣ modulator of Figure 3.1. $NTF_{1d}(z)$ and $NTF_{2d}(z)$ shape the quantization errors more than the NTF of the conventional DT ΔΣ modulator due to the fact that the OSR in the DTTI is double than the OSR in the conventional DT ΔΣ modulator.

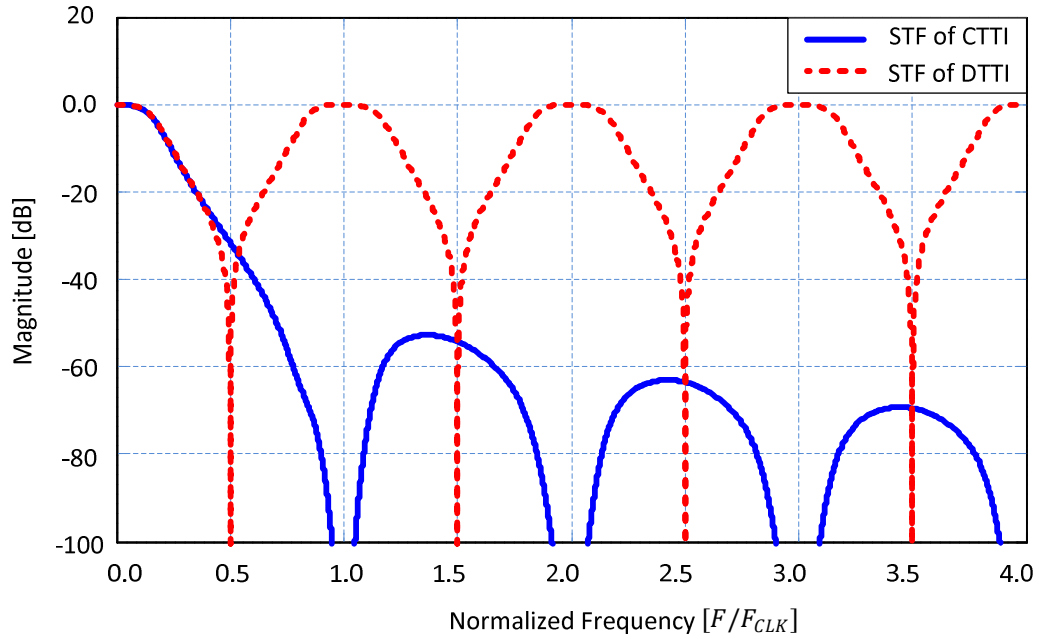


Figure 3.11: The signal transfer functions of the DTTI and the CTTI ΔΣ modulator.

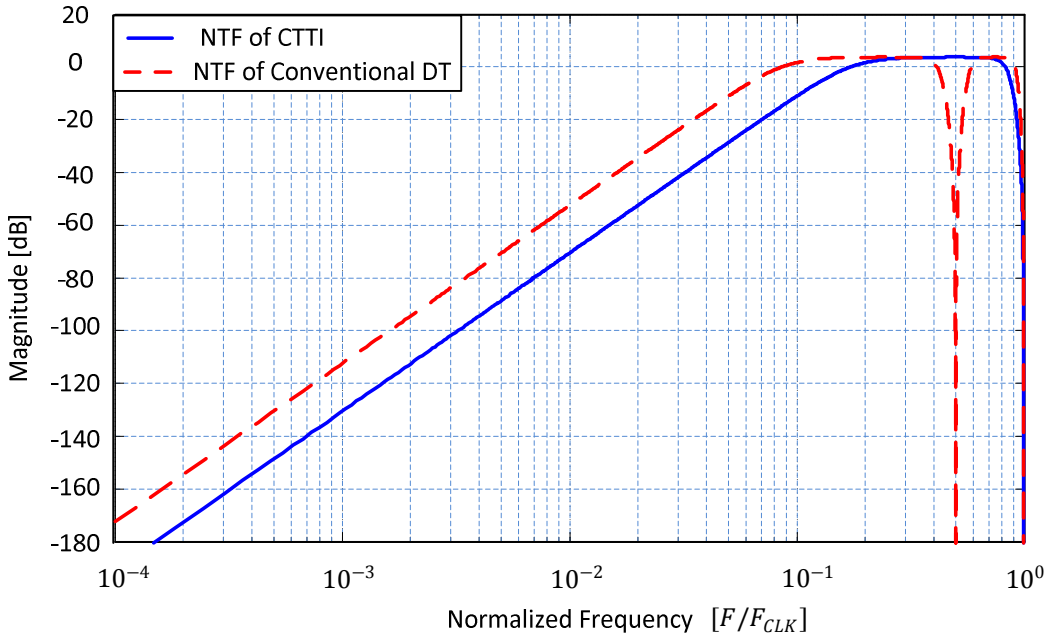


Figure 3.12: The noise transfer functions of the CTTI and the conventional DT ΔΣ modulator.

3.6 Conclusion:

In this chapter, a DTTI ΔΣ modulator is derived directly from the time domain node equations of its conventional DT ΔΣ modulator. To save the power and silicon area, one set of integrators is shared between channels and the input demultiplexer is removed but it causes a problem which is called “delayless feedback path” in which the input of the the quantizer Q1 is directly linked to the output of the quantizer Q2 without any delay block. Three methods to solve this problem are presented and advantages and disadvantage of each method is discussed.

A CTTI ΔΣ modulator equivalent of the DTTI ΔΣ modulator is obtained in three steps as follows: the first step is to determine the DT loop filters; the second step is to convert the DT loop filters into equivalent CT loop filters through the use of either the Impulse Invariant Transformation or the modified Z-transform. The last step is to convert the modulator into a CTTI ΔΣ modulator which has the same order as the DTTI ΔΣ modulator.

Finally, the STFs and the NTFs of the DTTI and the CTTI ΔΣ modulator are formulated. The STFs and the NTFs of the DTTI, the CTTI and the conventional DT ΔΣ modulator are plotted and compared.

Chapter 4:
MATLAB Simulation

The proposed CTTI ΔΣ modulator has been simulated using the SIMULINK toolbox of MATLAB and all non-idealities such as finite DC gain and bandwidth of the opamps, the DAC mismatches, offsets of the quantizers and the clock jitter of the DACs have been modelled and their effects on the performance of the modulator have been investigated. The Simulink model of the proposed CTTI ΔΣ modulator has been shown in Figure 4.1 and 4.2 where *wu* and *A* are the unity gain bandwidth and the DC gain of the opamp respectively. The modulator coefficients have been scaled in Figure 4.1. All specifications of the CTTI ΔΣ modulator have been summarized in Table 4.1.

4.1 Output Spectra Comparison of CTTI, DTTI and DT ΔΣ modulator

The output spectrum of the CTTI ΔΣ modulator is compared with the output spectra of the conventional DT and the DTTI ΔΣ modulator in Figure 4.3. The output spectra of the DTTI and CTTI ΔΣ modulator are the same and their IBN are shaped more than the conventional DT ΔΣ modulator. The SNDRs of the conventional DT, the DTTI and CTTI ΔΣ modulator are 57.5dB, 78.47dB and 78.54dB respectively. Therefore in this particular case, the SNDRs of the TI ΔΣ modulators are improved by 21dB. As given by equation (2.19) in chapter 2, SNDR is exponentially proportional to the OSR of the modulator. The OSR of the DTTI and the CTTI ΔΣ modulator is 16 which is double the OSR of the DT ΔΣ modulator. Therefore, an increase of 21dB in SNDR of TI ΔΣ modulators is expected.

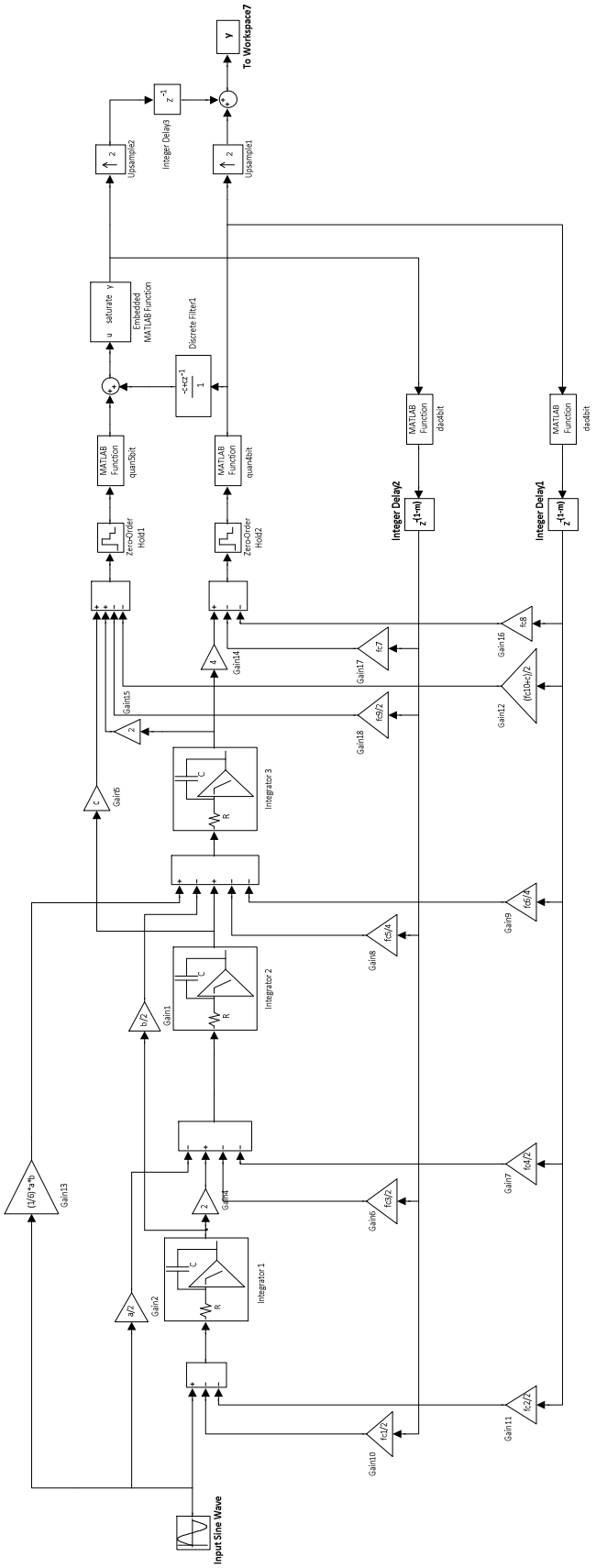


Figure 4.1: The SIMULINK model of the 3rd-order CTTI ΔΣ modulator.

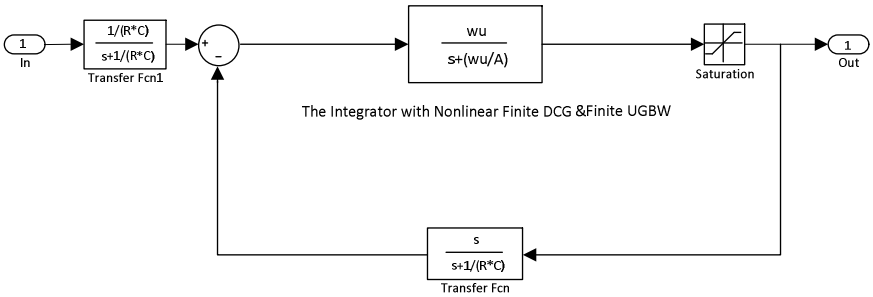


Figure 4.2: The integrator model of the 3rd-order CTTI ΔΣ modulator.

Table 4.1: The specifications of the CTTI ΔΣ modulator.

Parameter	*Value*
a	0.2764
b	0.7639
c	2.0000
f_{c1}	1.0000
f_{c2}	1.0000
f_{c3}	1.0000
f_{c4}	1.2764
f_{c5}	0.9648
f_{c6}	1.7287
f_{c7}	0.6708
f_{c8}	1.3292
f_{c9}	1.3292
f_{c10}	2.1987
OSR	16
Clock Frequency	320MHz
Signal Bandwidth	10MHz
DAC1 Resolution	4bit
DAC2 Resolution	4bit
Q1 Resolution	5bit
Q2 Resolution	4bit
Excess Loop Delay (intentional)	0.5T

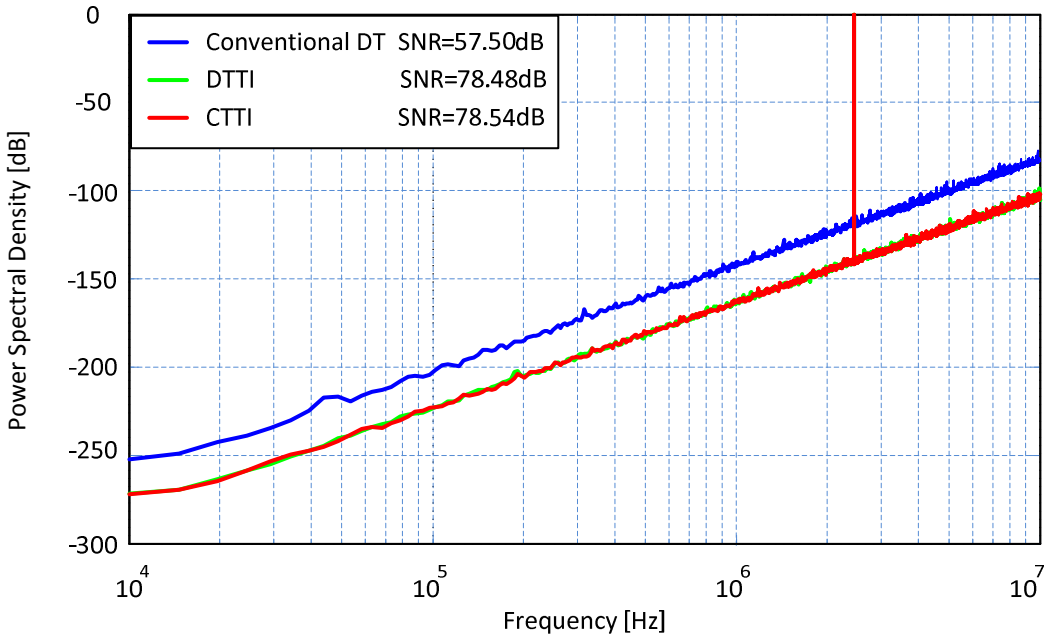


Figure 4.3: The output spectra of the conventional DT, the DTTI and the CTTI ΔΣ modulator for a 2.4462MHz input with clock frequencies of 160MHz, 320MHz and 320MHz respectively.

4.2 DACs Matching Requirements

In order to obtain the matching requirement for coefficients of DAC1 and DAC2, the CTTI ΔΣ modulator has been simulated using the SIMULINK toolbox of MATLAB eleven times. In each simulation, one of the coefficients was deviated from its ideal value while other coefficients were set to their ideal values. Then the SNDR of the CTTI ΔΣ modulator measured versus the accuracy of the DAC coefficient. Figure 4.4 and 4.5 show the SNDR of the CTTI ΔΣ modulator versus the matching of the DAC1 and DAC2 coefficients respectively. The minimum matching requirements for the coefficients of DAC1, f_{c1}, f_{c3}, f_{c5}, f_{c7} and f_{c9} are 10bits, 7bits, 4bits, 4bits and 4bits respectively and for the coefficients of DAC2, f_{c2}, f_{c4}, f_{c6}, f_{c8} and f_{c10} they are 10bits, 7bits, 4bits, 4bits and 4bits respectively. The coefficient c has the minimum matching requirement which is 4bits between the analog and the digital domain as shown in Figure 4.5. Hence there will be no need to use the DWA block if the coefficients of DAC1 and DAC2 meet the minimum matching requirements. This will make the circuit design of the CTTI ΔΣ modulator much easier as a result.

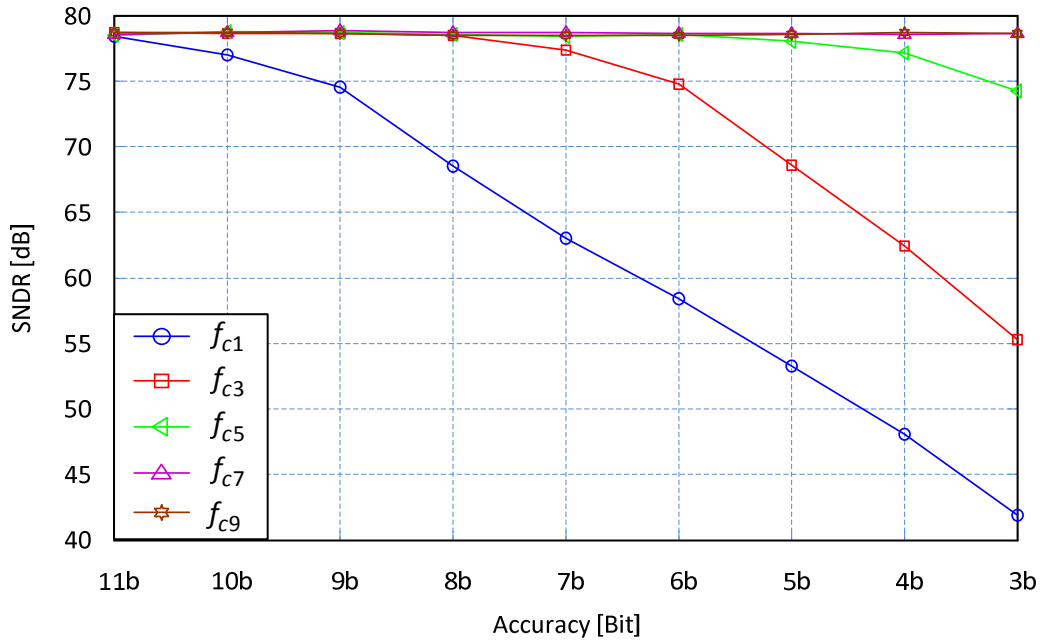


Figure 4.4: The SNDR versus the matching of the DAC1 coefficients.

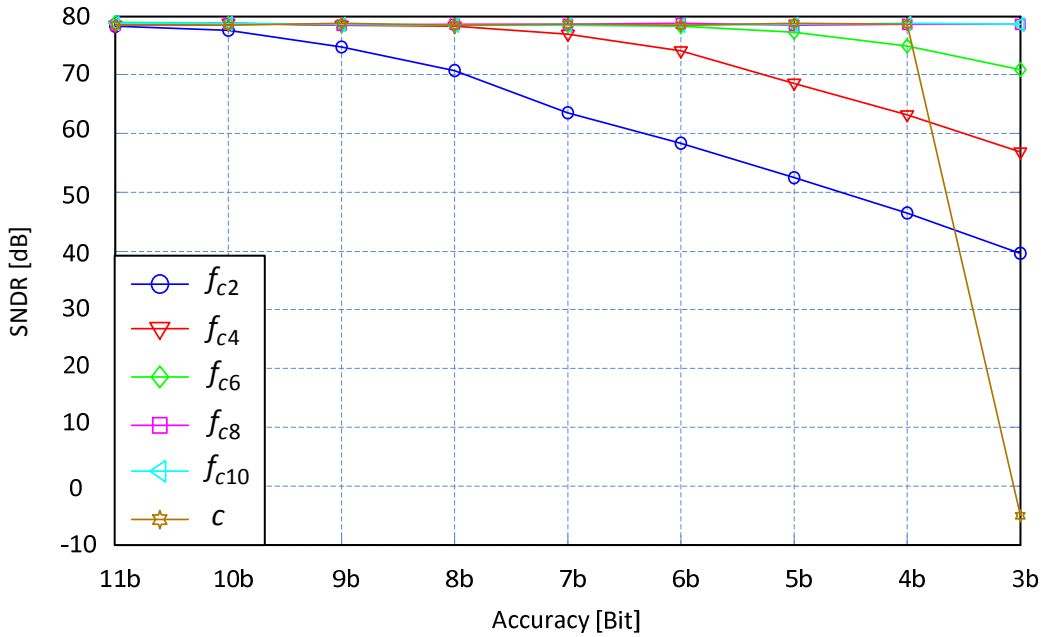


Figure 4.5: The SNDR versus the matching of the DAC2 coefficients.

4.3 Dynamic Range of the CTTI Modulator

Figure 4.6 shows the dynamic range plot of the CTTI modulator for a 2.4462MHz input and a clock frequency of 320MHz. The SNDR increases linearly with the input amplitude and maximum SNDR of 78dB occurs at -1dBFS of the input. After this point the SNDR drops sharply owing to the saturation of the integrators.

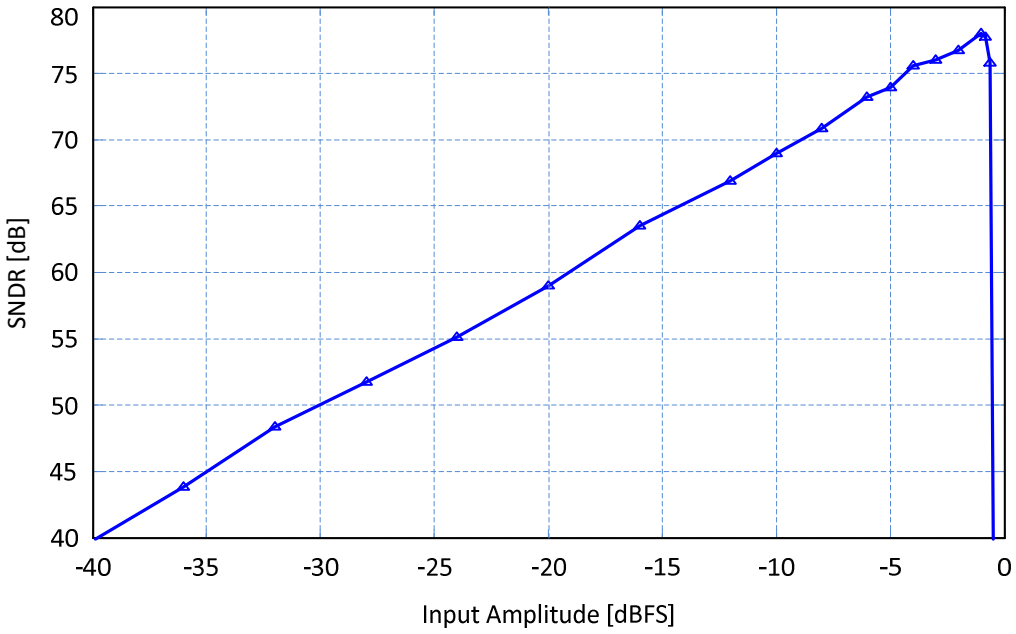


Figure 4.6: Dynamic range plot for a 2.4462MHz input and a clock frequency of 320MHz.

4.4 RC Time Constant Variations

The accuracy of the integrator transfer function depends on the RC time constant precision. Unfortunately, in current CMOS technologies, the absolute value of resistors and capacitors can vary as large as $\pm 15\%$ independently which results in up to $\pm 30\%$ RC time constant variation [28][46][47]. A system-level simulation has been performed in order to investigate the effect of the RC time constant variation on the SNDR of the CTTI ΔΣ modulator. The normalized time constant is swept in the range from 0.65 to 1.5. From the simulation results shown in Figure 4.7, we find that when the time constant deviates from its nominal value T_s (the

sampling frequency), the SNDR of the CTTI ΔΣ modulator will degrade. Decreasing the time constant results in higher loop filter gain and better SNDR. The system becomes unstable when the time constant decreases further more to a value around 0.71. When time constant increases (more than T_s), the modulator will become more stable. However, the noise shaping will be less effective due to the smaller loop filter gain and therefore IBN power increases. Consequently, the SNDR decreases gradually by increasing the time constant.

If only $\pm 3\%$ time constant variation is allowed then the SNDR degrades 2.5dB. To make sure that the RC time constant variation is as small as $\pm 3\%$, a kind of tuning technique has to be used [28][46][47]. The RC time constants are adjusted up to $\pm 3\%$ by using a calibration circuit which contains some switches, binary-weighted capacitors and five control bits. This calibration process is achieved by tuning the integrator feedback capacitors and will be explained in detail in chapter 5.

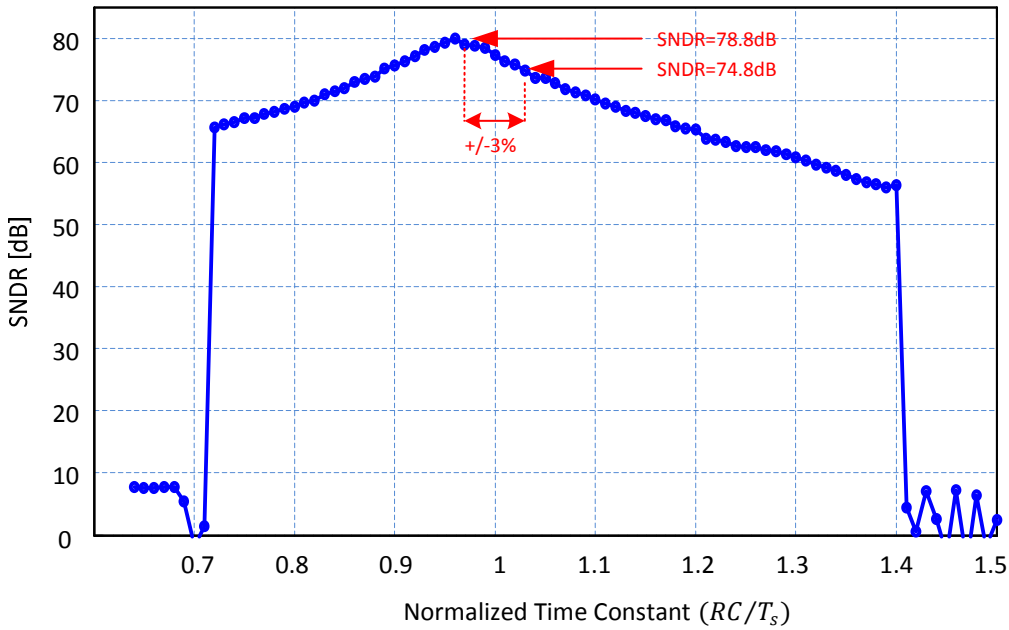


Figure 4.7: The effect of RC time constant variation on the SNDR of the CTTI ΔΣ modulator.

4.5 Clock Jitter

It is well known that in comparison to the DT ΔΣ modulators, the CT ΔΣ modulators are sensitive to the clock jitter of their DACs [29]. We assume there is timing jitter in the clock of the quantizer. A typical feedback current waveform for a SC DT ΔΣ modulator is depicted on the left-hand side of Figure 4.8. Most of the charge transfer occurs at the start of the clock period, so that the amount of charge Δq_d lost due to a timing error is relatively small. In contrast, the DAC output current in a CT ΔΣ modulator is shown on the right-hand side of Figure 4.8. The charge is transferred at a constant rate over a clock period, and so charge loss Δq_c from the same timing error is a larger proportion of the total charge. Moreover, In a DT ΔΣ modulator, jitter in the input sample-and-hold (S&H) clock only affects the input signal. In a CT ΔΣ modulator, the sampling occurs at the quantizer rather than the input, which means the jitter, affects the sum of the input plus quantization noise. Therefore, CT ΔΣ modulators are more sensitive to clock jitter than DT ΔΣ modulators. Clock jitter causes a slight random variation in the amount of charge fed back per clock cycle. In an oversampled converter, the spectrum of the output stream is very noisy outside the (narrow) signal band; a random phase modulation causes the noise outside the signal band to fold back into the signal band, raising the converter noise floor and degrading its resolution [29].

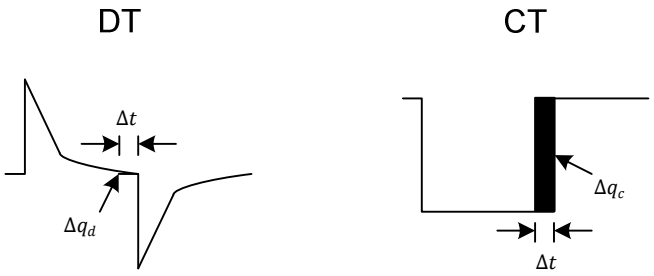


Figure 4.8: Clock jitter effect in DT versus CT ΔΣ modulator.

The effect of the clock jitter on the CTTI ΔΣ modulator has been modelled and simulated in MATLAB. Figure 4.9 shows the SNDR of the modulator versus the clock jitter of the DAC and as expected the SNDR decreases by increasing the clock jitter. A CTTI ΣΔ modulator integrates the feedback DAC waveforms over time. Thus, a statistical variation of the feedback DAC waveforms results in a statistical integration error and consequently

increased the noise level. A variation of the length of a feedback DAC pulse directly modulates the amount of feedback charge, which appears during the corresponding clock cycle. This error is directly proportional to the clock jitter variance σ_t^2 , while it adds directly to the modulator input through the outermost feedback branch. As can be seen in Figure 4.9, when the clock jitter increases, the resulting jitter noise increases and SNDR of the CTTI ΣΔ modulator decreases. When the clock jitter is increased to 1psec, the SNDR of the CTTI ΣΔ modulator drops by 1dB from 78dB to 77dB.

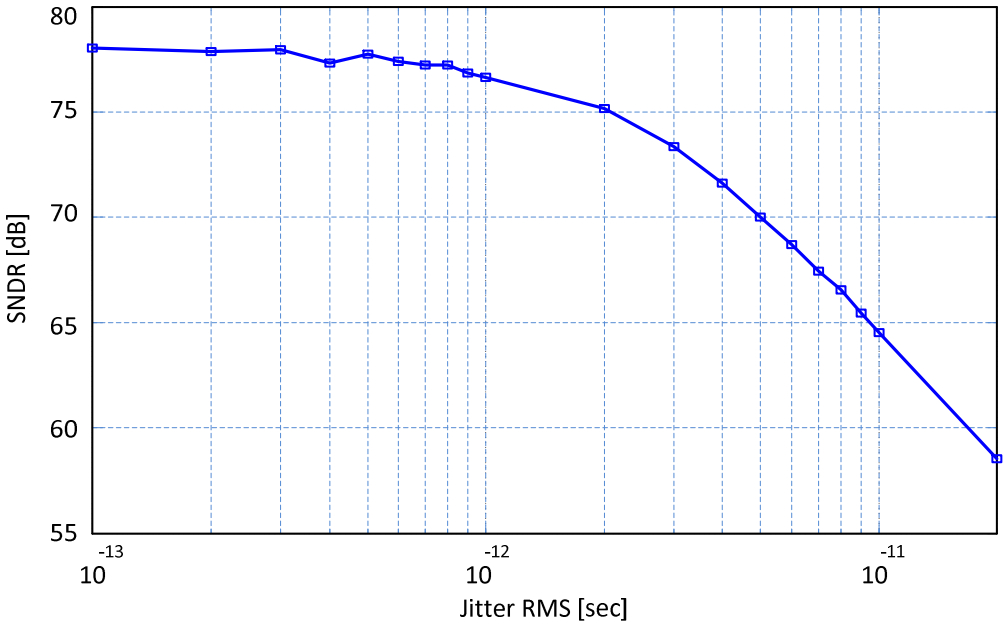


Figure 4.9: The SNDR versus the clock jitter of the DAC.

4.6 Integrators Bandwidth and DC Gain Requirements

In order to design the circuit level of the CTTI ΔΣ modulator, the minimum bandwidths and DC gains of the integrators are required. These parameters have been modelled and simulated in MATLAB and all required design parameters established using the simulation results as a guide. Figure 4.10 shows the SNDR versus the normalized bandwidth of the integrators for the same CTTI modulator. The minimum bandwidth requirement for the first and the second integrator is $2F_{clk}$ (the clock frequency) and for the third integrator is F_{clk}. Figure 4.11 shows the SNDR of the CTTI ΔΣ modulator versus the DC gains of the integrators. The minimum DC gain requirement for the first integrator is 40dB and for the second and the third integrator is 50dB.

In order to obtain the bandwidth requirements for the first, the second and the third integrator, the CTTI ΔΣ modulator has been simulated using the SIMULINK toolbox of MATLAB three times. When the bandwidth of one of the integrators was sweeping from $0.25F_{clk}$ to $4F_{clk}$, the bandwidths of the other integrators were assumed to have an ideal value of 10G (rad/sec). The DC gains of the integrators were 100dB in this simulation. The SNDR of the CTTI ΔΣ modulator was measured and plotted versus the bandwidths of the integrators in Figure 4.10.

To obtain the DC gain requirements for the integrators, the CTTI ΔΣ modulator has been simulated three more times again. In this simulations, when the DC gain of one of the integrators was sweeping from 20dB to 100dB with a step of 5dB, DC gains of the other integrators were assumed had an ideal value of 100k and all integrators bandwidth were 10G (rad/sec). The SNDR of the CTTI ΔΣ modulator was measured and plotted versus the DC gains of the integrators in Figure 4.11.

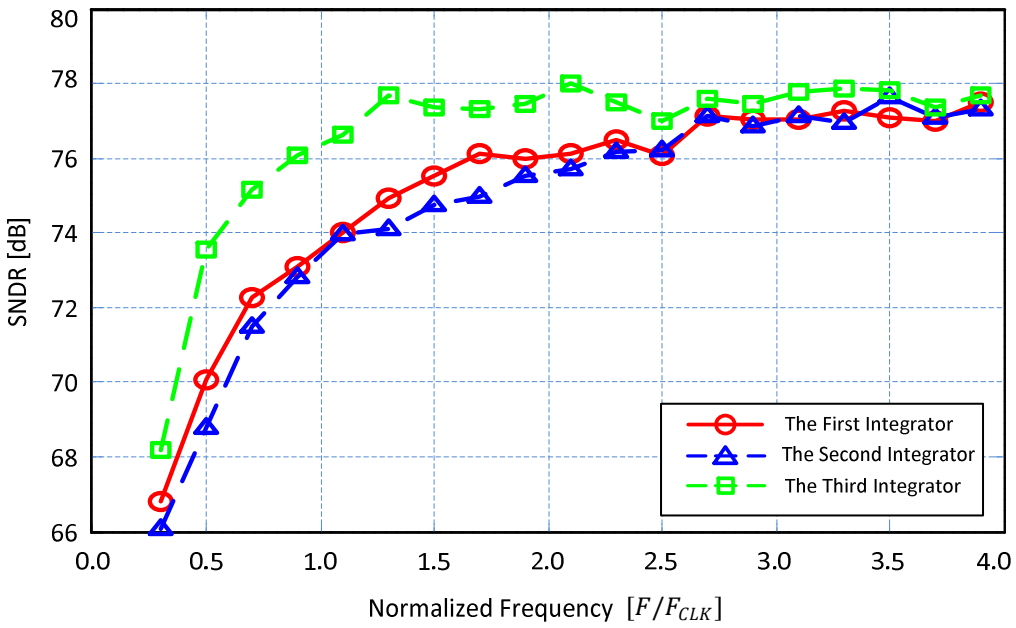


Figure 4.10: The SNDR versus the normalized bandwidths of the integrators.

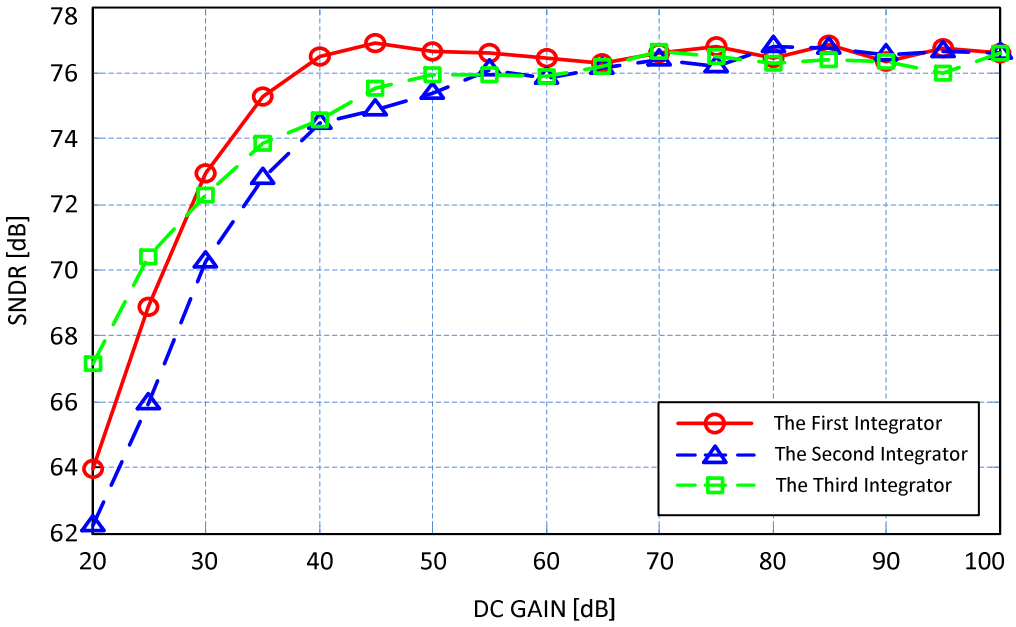
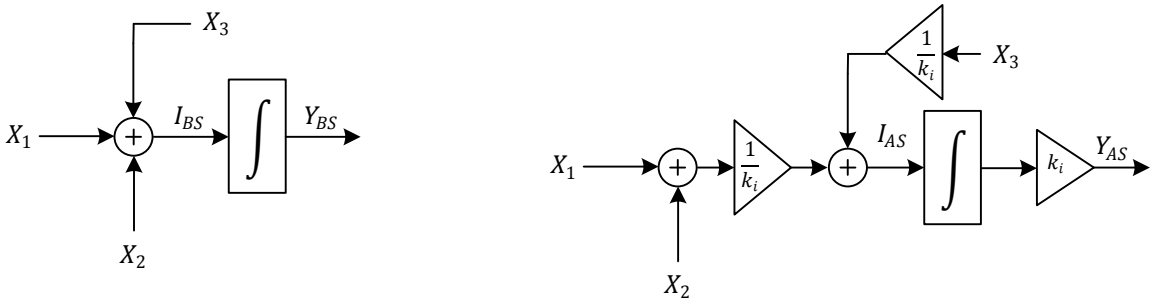


Figure 4.11: The SNDR versus DC gains of the integrators.

4.7 $1/k_i$ Signal Scaling Method

Figure 4.12(a) shows the general structure of an integrator before the application of $1/k_i$ signal scaling method. The input signals (X_1, X_2 and X_3) to the summing unit are linearly scaled down by division using a "k_i" factor (resulting in a reduced signal swing at the input of the integrator), and then the output signal of the integrator is scaled up by multiplication with the same "k_i" factor. Figure 4.12(b) illustrates the $1/k_i$ scaling method graphically [84].



(a) (b)

Figure 4.12: (a) General structure before the application of $1/k_i$ scaling method; (b) General structure after the application of $1/k_i$ scaling method.

The method can easily be proved mathematically as follows:

Before $1/k_i$ Scaling (BS):

$$I_{BS} = X_1 + X_2 + X_3 \tag{4.1}$$

$$Y_{BS} = \int I_{BS} dt \tag{4.2}$$

After $1/k_i$ Scaling (AS):

$$I_{AS} = \frac{1}{k_i}(X_1 + X_2 + X_3) = \frac{1}{k_i} I_{BS} \tag{4.3}$$

$$Y_{AS} = k_i \int I_{AS} dt = k_i \int \frac{1}{k_i} I_{BS} dt = \int I_{BS} dt = Y_{BS} \tag{4.4}$$

Although the proof is given for CT integrators, equations are also the same for DT integrators. It is clear from the above calculations that while we get a scaled signal (I_{BS}/k_i), at the input of the integrator, the output signal (Y_{AS}), remains unchanged which means that the input-output relation does not change with the addition of k_i factor; therefore, the method preserves all the transfer functions of the modulator and it is valid for any DT and CT ΔΣ Modulator topologies.

k_i factors are determined in two steps as follows:

1- Simulate the modulator and determine the critical integrators which have input signal swing peak amplitudes larger than the allowed limits.

2- For every critical integrator, use the formula (4.5), and calculate the k_i scaling factor.

$$k_i = \frac{maximum\ input\ swing\ of\ the\ ith\ critical\ integrator}{desired\ input\ swing\ of\ the\ ith\ critical\ integrator} \tag{4.5}$$

The simulations were carried out with saturation blocks at the output of integrators. In this design, $V_{ref} = \pm 1V$ and the integrators will be overloaded with output swing more than $+1V$ or less than $-1V$. It is clear that if the integrator is overloaded then it causes a degradation in the SNR of the modulator. Figure 4.13, 4.14 and 4.15 show the histogram plots of the output signals of the first, the second and the third integrator. As can be seen from these figures, the maximum output signal swings of the first, the second and the third

integrator are $\pm 0.5V, \pm 0.7V$ and $\pm 0.6V$. In this design, no overloading of integrators occurs and there is no need for signal scaling.

Figure 4.16 and 4.17 show the histogram plots of the two quantizers input signals. The input signal swings are in the range $\pm 1V$. If the signal swing grows more than $+1V$ or less than $-1V$ then more comparators are required to resolve the signal; otherwise, the signal is limited and causes degradation in the SNR of the modulator.

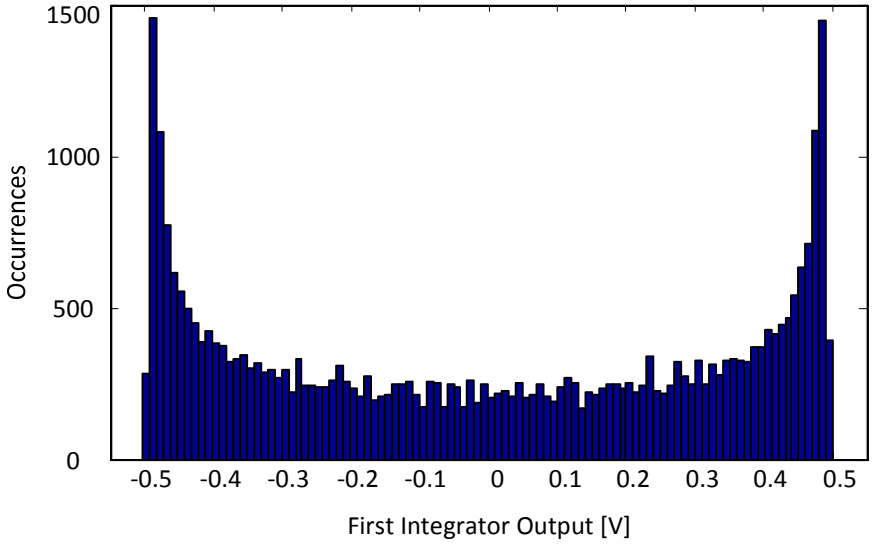


Figure 4.13: Histogram of the first integrator output.

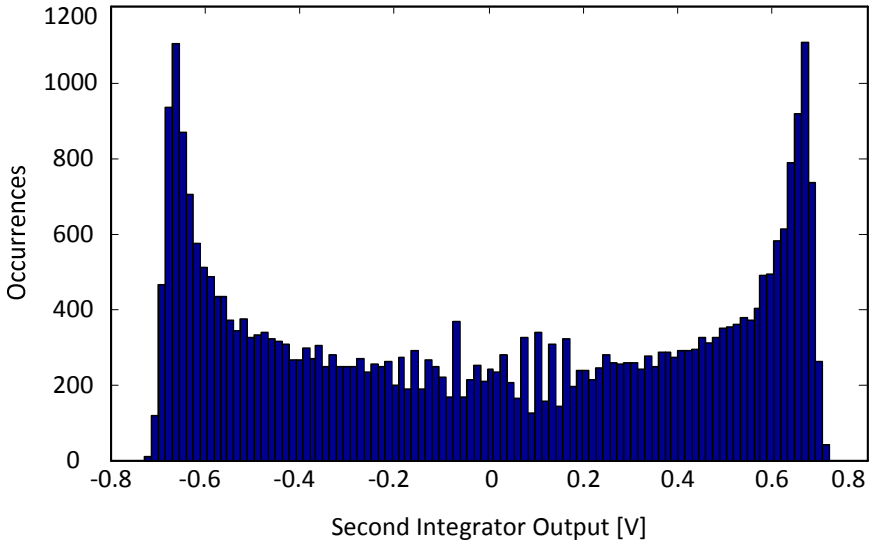


Figure 4.14: Histogram of the second integrator output.

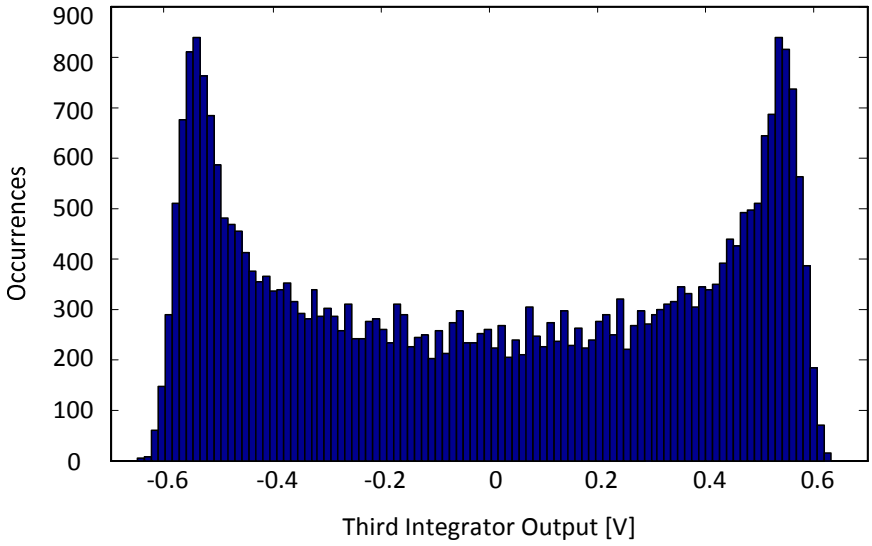


Figure 4.15: Histogram of the third integrator output.

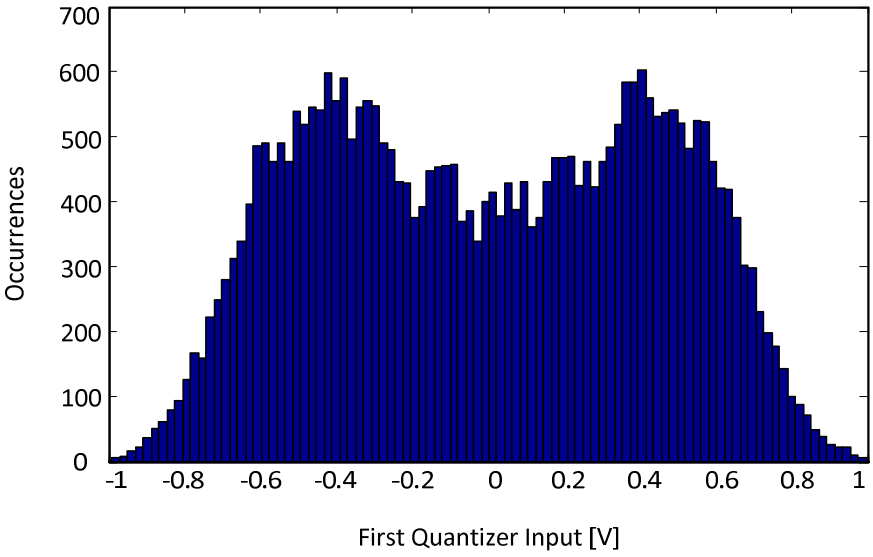


Figure 4.16: Histogram of the first quantizer input.

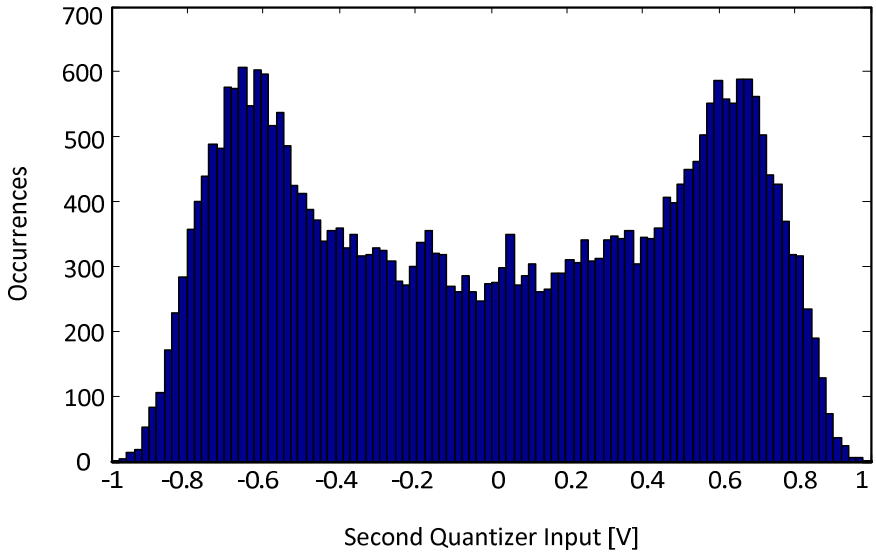


Figure 4.17: Histogram of the second quantizer input.

4.8 Comparator Offset Voltage

Figure 4.18 shows the SNDR versus the offset voltages of the first and second quantizer. The standard deviations of offset voltages of the comparators in the first and second quantizer must be less than 10mv and 20mv respectively otherwise they degrade the performance of the CTTI ΔΣ modulator and cause loss of SNDR.

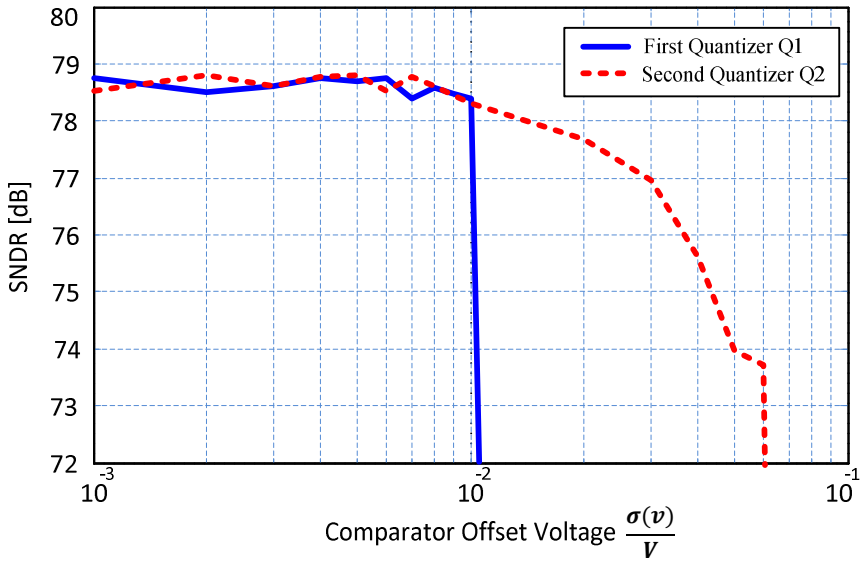


Figure 4.18: SNDR versus the offset voltages of the first and second quantizer.

4.9 Conclusion

In this chapter, the proposed CTTI ΔΣ modulator has been simulated using the SIMULINK toolbox of MATLAB and all non-idealities such as finite DC gain and bandwidth of the opamps, the DAC mismatches, offsets of the quantizers, RC time constant variations and the clock jitter of the DACs have been modelled and their effects on the performance of the modulator have been investigated. According to the simulation results, the minimum bandwidth requirement for the first and the second integrator is $2F_{clk}$ (the clock frequency) and for the third integrator is F_{clk}. The minimum DC gain requirement for the first integrator is 40dB and for the second and the third integrator is 50dB. The standard deviations of offset voltages of the comparators in the first and second quantizer must be less than 10mv and 20mv respectively otherwise they degrade the performance of the CTTI ΔΣ Modulator and cause loss of SNDR.

The output spectra of the DTTI, the CTTI and the conventional DT ΔΣ modulator are shown and compared in this chapter. The SNDRs of the TI ΔΣ modulators are improved by 21dB in comparison to the conventional DT ΔΣ modulator.

Chapter 5:

Circuit Design and Simulation Results

In this chapter, the circuit design of the 3rd-order two-path CTTI ΔΣ modulator is presented. The modulator has been designed through the use of 90nm CMOS TSMC technology with supply voltages of 1.8V for analogue part and 1.2V for digital part. Figure 5.1 shows the block diagram of the 3rd-order two-path CTTI ΔΣ modulator. The operating frequency of the quantizers, DACs and all other blocks except for the output multiplexer is 160MHz but the output multiplexer operates at 320MHz clock rate. The OSR of the modulator is 16, allowing a maximum input signal bandwidth of 10*MHz*. As illustrated in the chapter 4, a 13-bit modulator should be realized with this sampling frequency.

The major circuit blocks of the modulator include three integrators, ten 4-bit DACs, one 4-bit and one 5-bit flash ADC, two summation circuits, a clock generator, a biasing circuit, an output multiplexer and a digital error correction block ($1 - z^{-1}$).

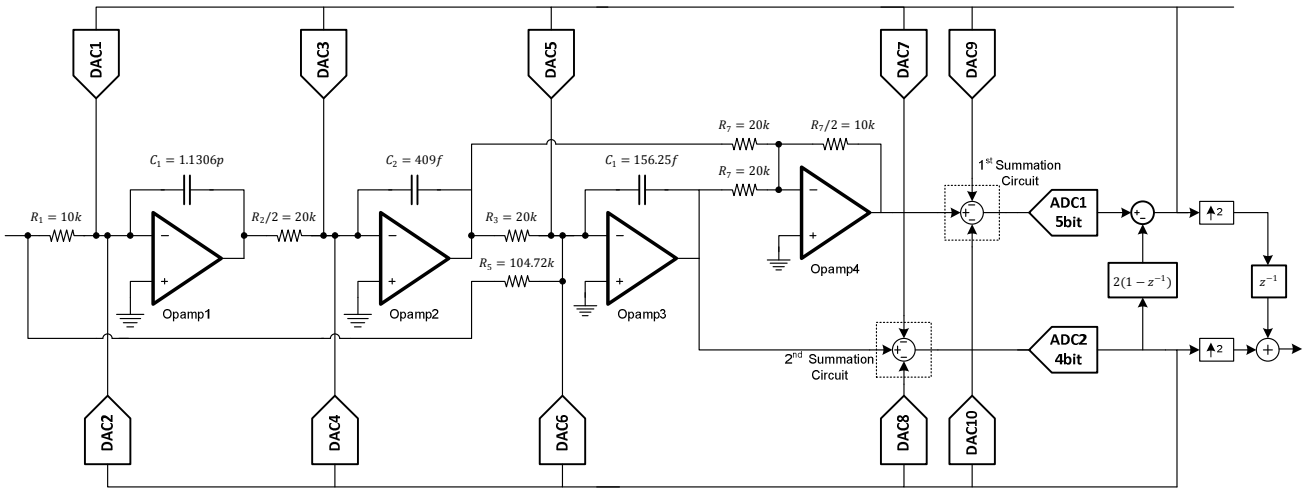


Figure 5.1: Block Diagram of the 3rd-order CTTI ΔΣ Modulator.

5.1 Integrators

To design three integrators, one approach is to use Gm-C integrators, which operate at higher speeds but suffer from low linearity [30]. To meet the specifications, three active-RC integrators are used. As explained in the chapter 4, CMOS technologies have up to 30% RC time constant variation [28] which the SNDR of the modulator decreases gradually by increasing RC time constant variation as shown in Figure 4.7. A tuneable capacitor array is used to tune up the RC time constant of the integrators and to compensate for process variations as well as change in the sampling frequency. In addition, a common-mode feedback circuit is required for each opamp due to the differential design, as well as a startup circuit to eliminate an initial state that could keep the outputs of the opamp at the positive supply rails.

The preliminary considerations for the design of the opamps are the unity gain bandwidth and DC gain. Based on MATLAB simulations which shown in Figure 4.10 and 4.11, a unity gain bandwidth of 640MHz (twice the clock frequency) and a DC gain of 50dB are required for each integrator. Moreover, maximum single-ended swings of approximately 500mV, 700mV and 600mV are required at the output of the first, second and third integrator respectively based on histogram plots of the outputs of the integrators shown in Figure 4.13, 4.14 and 4.15 and the dynamic range scaling used throughout the modulator.

5.2 Resistor and Capacitor Values

According to noise and bandwidth requirements, the resistor and capacitor values have been chosen. First, MATLAB simulations were run to determine the resistor values by considering the noise level to be less than −80*dBFS.* Therefore the first, second and third resistor have been chosen to be $R_1 = 10k\Omega$, $R_2 = 20k\Omega$ and $R_3 = 20k\Omega$. Based on these resistor values, the capacitors sizes are derived as shown in the SIMULINK model of the 3rd-order CTTI ΔΣ Modulator of Figure 4.1 and also the block diagram presented in Figure 5.1.

5.3 Operational Amplifier

One popular opamp architecture is a two-stage Miller-compensation opamp which has been utilized for the first, second and third integrator. A PMOS input differential pair is used as the input stage for two reasons: First, the second pole is determined by the transconductance of the input transistors of the second stage and the NMOS transistor is faster than PMOS one; therefore the whole opamp will be more stable. Second, the input and output common mode voltage of the opamp is set to be 0.8V instead of VDD/2 (0.9V). VDS voltage of the tail transistor in the first stage will have more headroom and will not be pushed to triode region. The benefit of using PMOS transistors as input in the differential pair is low flicker noise, but in our wideband design, the flicker noise is of less concern.

The opamps are designed to have a DC gain of 50dB and a unity gain bandwidth of 640MHz and output swing of more than 700mV according to the MATLAB simulation results have been done and shown in Figures 4.10, 4.11, 4.13, 4.14 and 4.15.

The schematic of a two-stage Miller-compensation opamp is shown in Figure 5.2. The sizes of transistors are illustrated in Table 5.1. The first and second opamp are identical.

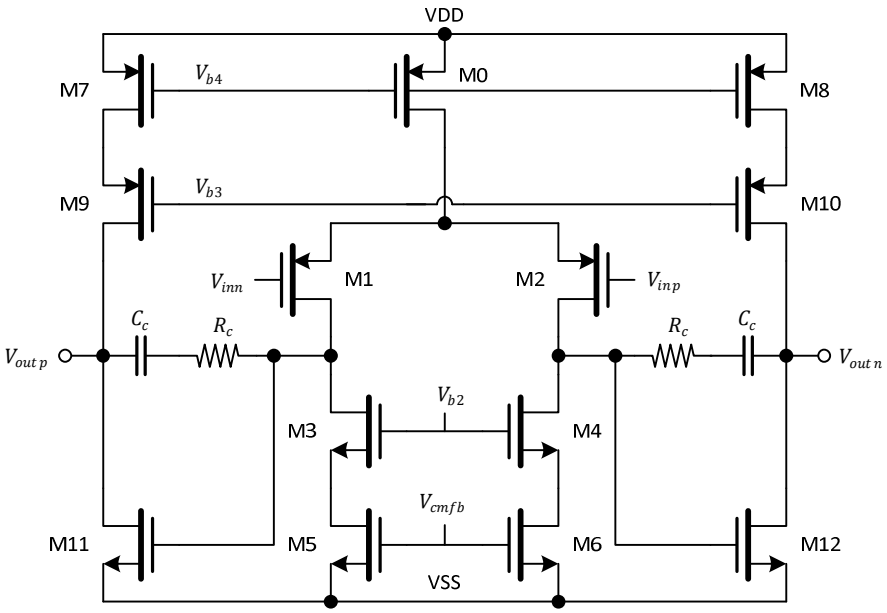


Figure 5.2: Schematic of the two-stage opamp.

Table 5.1: The sizes of transistors of the first, second and third opamp. The sizes (W and L) are in microns.

	M0	M1,M2	M3,M4	M5,M6	M7,M8	M9,M10	M11,M12	C_c	R_c
First Opamp	W=5 L=0.5 M=64	W=6 L=0.3 M=16	W=2 L=0.5 M=32	W=2 L=0.5 M=32	W=5 L=0.5 M=64	W=5 L=0.5 M=64	W=2 L=0.3 M=32	642f	350Ω
Second Opamp	W=5 L=0.5 M=64	W=6 L=0.3 M=16	W=2 L=0.5 M=32	W=2 L=0.5 M=32	W=5 L=0.5 M=64	W=5 L=0.5 M=64	W=2 L=0.3 M=32	642f	350Ω
Third Opamp	W=5 L=0.5 M=64	W=6 L=0.3 M=16	W=2 L=0.5 M=32	W=2 L=0.5 M=32	W=5 L=0.5 M=128	W=5 L=0.5 M=128	W=2 L=0.3 M=64	767f	250Ω

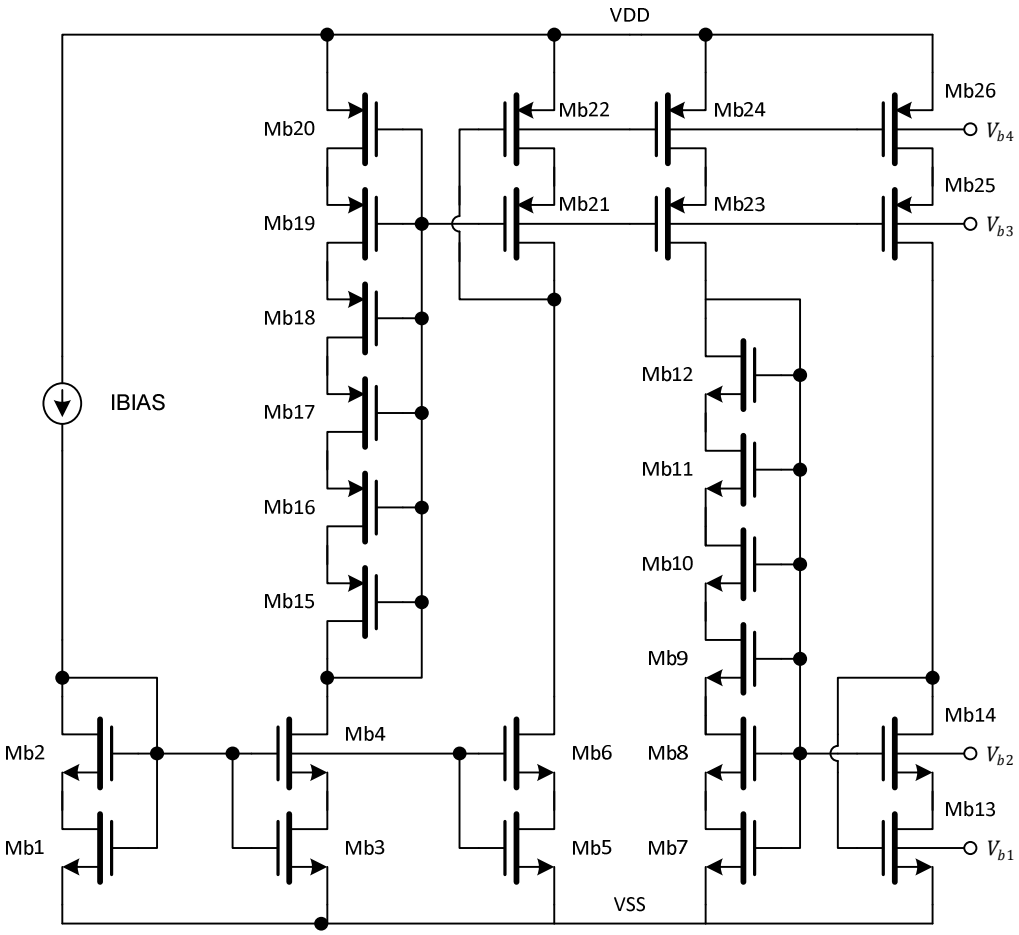


Figure 5.3: Schematic of biasing circuit.

In order to maximize performance, a robust biasing circuit must be employed. The high-swing cascoded current mirror [39] is used to maximize robustness over process and supply voltage variation while it provides

excellent current mirroring as shown in Figure 5.3. The initial device sizes are based on a VDSAT of 200mV. The sizes of transistors of the first, second and third biasing circuit are presented in Table 5.2.

Table 5.2: The sizes of transistors of the first, second and third biasing circuit. The sizes (W and L) are in microns.

	Mb1,Mb2,Mb3, Mb4,Mb5,Mb6	Mb7,Mb8,Mb9,Mb10 Mb11,Mb12,Mb13,Mb14	Mb15,Mb16,Mb17,Mb18,Mb19,Mb20 Mb21,Mb22,Mb23,Mb24,Mb25,Mb26	IBIAS
First Bias	W=4, L=2, M=1	W=2, L=0.5, M=1	W=5, L=0.5, M=1	$10\mu A$
Second Bias	W=4, L=2, M=1	W=2, L=0.5, M=1	W=5, L=0.5, M=1	$10\mu A$
Third Bias	W=4, L=2, M=1	W=2, L=0.5, M=1	W=5, L=0.5, M=1	$10\mu A$

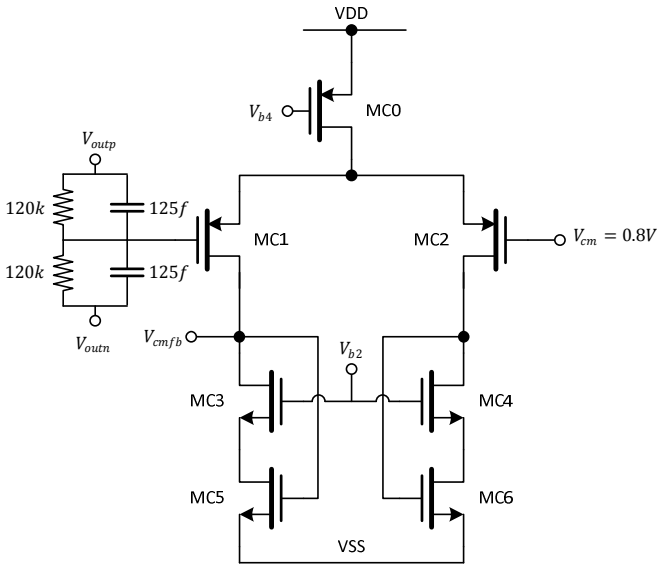


Figure 5.4: Schematic of CMFB circuit.

In the Common Mode Feedback (CMFB) circuit as shown in Figure 5.4, two resistors (and two capacitors for high frequency signal) are used to sense the common mode voltage of the opamp outputs, V_{outp} and V_{outn}. A simple differential amplifier with diode connected active loads is employed to compare the common mode voltage with the reference voltage of $V_{cm} = 0.8V$, and to generate the V_{cmfb} signal for the opamp. This signal is applied to first stage of the opamp and sets and controls the output common mode voltage of the opamp. To increase the phase margin of the CMFB loop, the DC gain of CMFB loop is reduced, so a trade-off should be made between the phase margin and DC gain of the CMFB loop. The sizes of transistors of the first, second and third CMFB circuit are illustrated in Table 5.3.

Table 5.3: The sizes of transistors of the first, second and third CMFB circuit. The sizes (W and L) are in microns.

	MC0	MC1,MC2	MC3,MC4	MC5,MC6
First CMFB circuit	W=5, L=0.5, M=16	W=5, L=0.3, M=8	W=2, L=0.5, M=8	W=2, L=0.5, M=8
Second CMFB circuit	W=5, L=0.5, M=16	W=5, L=0.3, M=8	W=2, L=0.5, M=8	W=2, L=0.5, M=8
Third CMFB circuit	W=5, L=0.5, M=16	W=5, L=0.3, M=8	W=2, L=0.5, M=8	W=2, L=0.5, M=8

Table 5.4 presents a summary of specifications of three integrators such as DC gain, Unity Gain BandWidth (UGBW), Phase Margin (PM) and current consumption of opamps after running AC simulation in TT 27°C, FF 120°C and SS -40°C corners. Figure 5.5, 5.6 and 5.7 show the AC responses of the first, second and third integrators respectively. As discussed in section 4.6, the UGBW requirement for the first and the second integrator is $2F_{clk}(= 640MHz)$ and for the third integrator is $F_{clk}(= 320MHz)$ and the minimum DC gain requirement for the first integrator is 40dB and for the second and the third integrator is 50dB. The results obtained from circuit simulations presented in Table 5.4 show that all three integrators meet above mentioned requirements for the UGBW and the DC gain.

Table 5.4: Specifications of the integrators.

	Corner	*Current Consumption(mA)*	*DC Gain(dB)*	*UGBW(MHz)*	*PM(‘C)*
First Integrator	TT 27°C	2.12mA	65.97	971	77.7
	FF 120°C	2.65mA	63.42	1171	75.2
	SS -40°C	1.696mA	68.11	820	78.7
Second Integrator	TT 27°C	2.12mA	65.97	1010	79.7
	FF 120°C	2.65mA	63.42	1213	76.1
	SS -40°C	1.696mA	68.11	855	81.5
Third Integrator	TT 27°C	3.4mA	67.25	866	90.5
	FF 120°C	4.25mA	64.73	1044	87.0
	SS -40°C	2.72mA	69.36	735	92.4

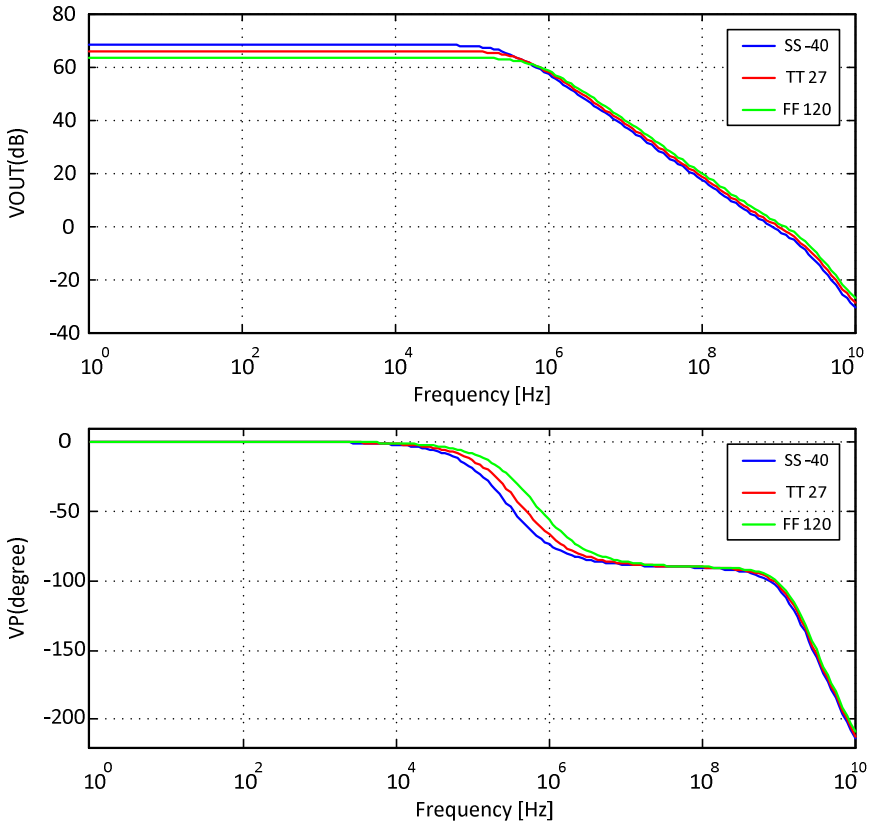


Figure 5.5: AC response of the first integrator in TT 27°C, SS -40°C and FF 120°C corners.

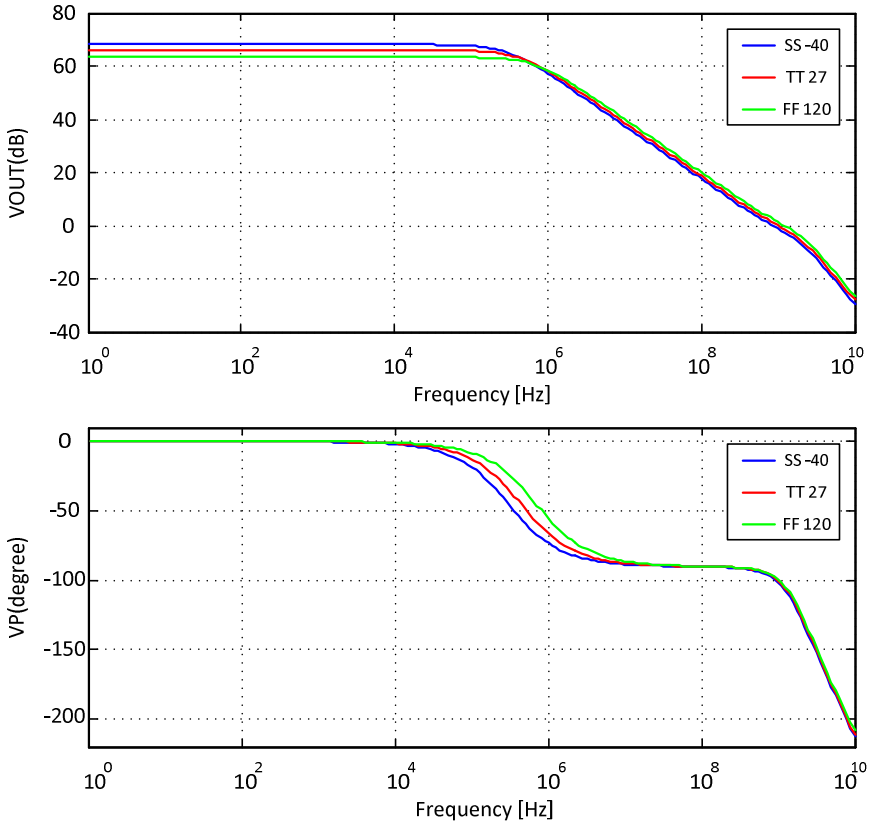


Figure 5.6: AC response of the second integrator in TT 27°C, SS -40°C and FF 120°C corners.

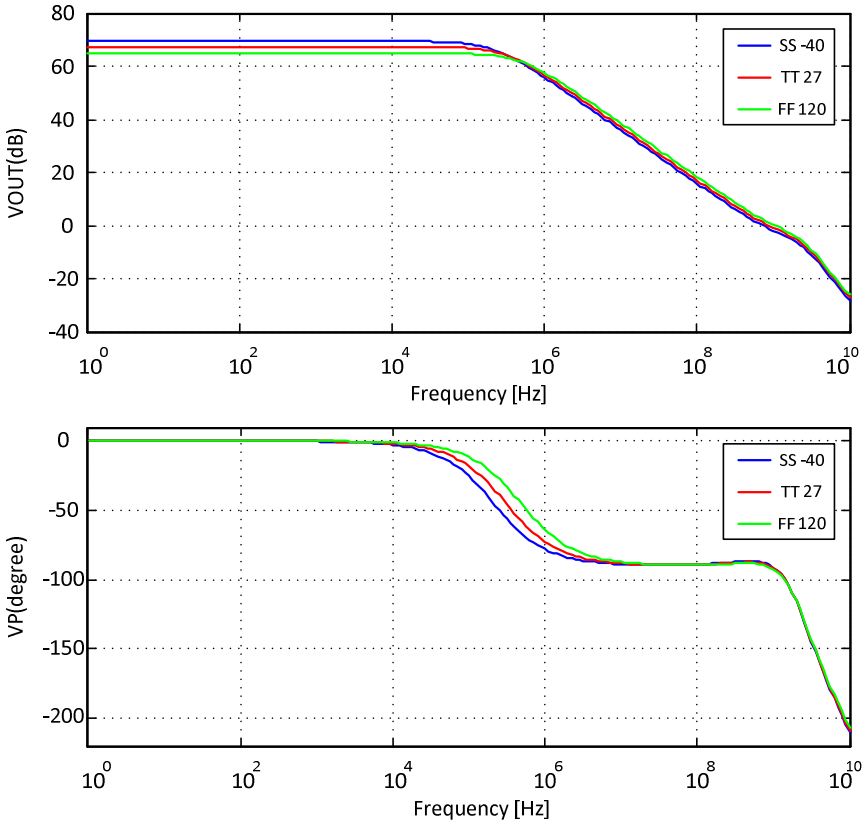


Figure 5.7: AC response of the third integrator in TT 27°C, SS -40°C and FF 120°C corners.

5.4 Digital-to-Analog Converters

Ten 4-bit current-steering DACs have been designed to operate at 160*MHz* with NRZ pulses. The magnitudes of the full-scale currents of these DACs have been calculated and given by equation set (5.1).

$$I_{DAC1} = \pm\frac{f_{c1}V_{ref}}{2R_1} = \pm\frac{1}{20k} = \pm 50\mu A \quad (5.1.a)$$

$$I_{DAC2} = \pm\frac{f_{c2}V_{ref}}{2R_1} = \pm\frac{1}{20k} = \pm 50\mu A \quad (5.1.b)$$

$$I_{DAC3} = \pm\frac{f_{c3}V_{ref}}{2R_2} = \pm\frac{1}{40k} = \pm 25\mu A \quad (5.1.c)$$

$$I_{DAC4} = \pm\frac{f_{c4}V_{ref}}{2R_2} = \pm\frac{1.2764}{40k} = \pm 31.91\mu A \quad (5.1.d)$$

$$I_{DAC5} = \pm\frac{f_{c5}V_{ref}}{4R_3} = \pm\frac{0.965}{80k} = \pm 12.06\mu A \quad (5.1.e)$$

$$I_{DAC6} = \pm\frac{f_{c6}V_{ref}}{4R_3} = \pm\frac{1.729}{80k} = \pm 21.61\mu A \quad (5.1.f)$$

$$I_{DAC7} = \pm\frac{f_{c7}V_{ref}}{4R_8} = \pm\frac{0.671}{4 * 250} = \pm 671\mu A \quad (5.1.g)$$

$$I_{DAC8} = \pm\frac{f_{c8}V_{ref}}{4R_8} = \pm\frac{1.329}{4 * 250} = \pm 1329\mu A \quad (5.1.h)$$

$$I_{DAC9} = \pm\frac{f_{c9}V_{ref}}{4R_{10}} = \pm\frac{1.329}{4 * 250} = \pm 1329\mu A \quad (5.1.i)$$

$$I_{DAC10} = \pm\frac{(f_{c10} + c)V_{ref}}{4R_{10}} = \pm\frac{4.199}{4 * 250} = \pm 4199\mu A \quad (5.1.j)$$

Figure 5.8 shows the schematic of the DAC unit current cell used for the first, second, third, fourth, fifth and sixth DAC. The current cell is composed of nine transistors which are current source M1, current sink M4, cascode transistors M2 and M3 and five switches (M5, M6, M7, M8 and M9). The cascode transistors are used to increase the output impedance of the current source and sink devices and at the same time, to prevent the dynamic glitches at the node A and B from impacting the current in M1 and M4. However, adding this cascode transistors reduces the allowable saturation voltage of M1 and M4 and hence the noise performance of the current DAC. The gates of the switch transistors are controlled by the complementary digital feedback signals, D and $\overline{D}$ and also by reset signal.

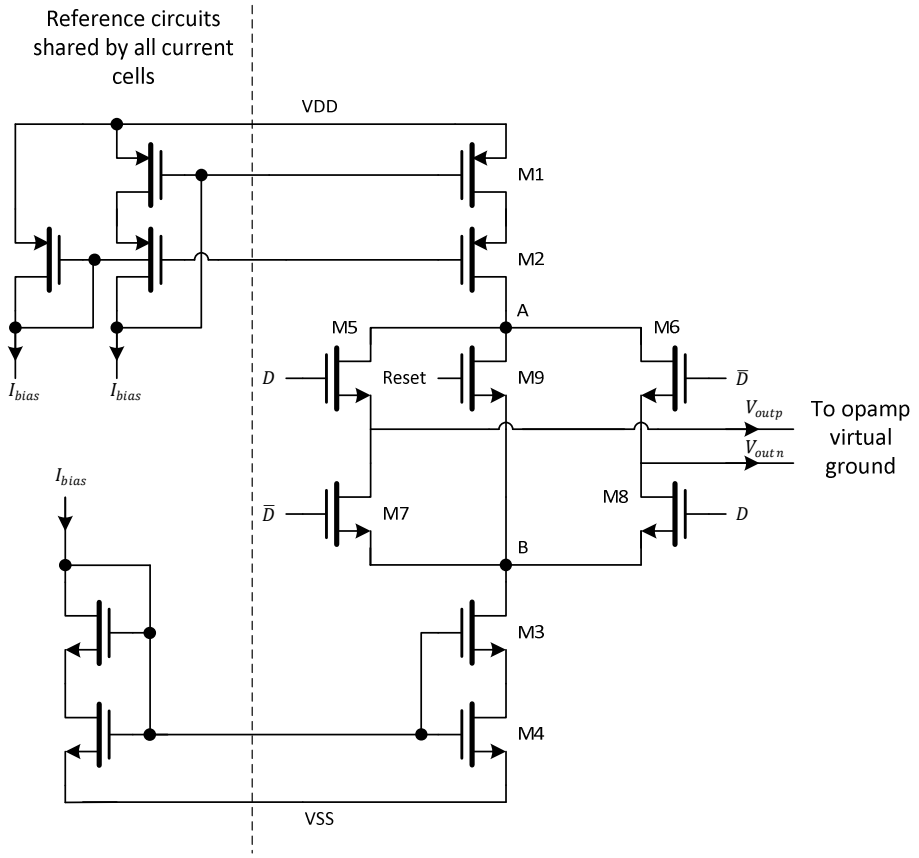


Figure 5.8: Schematic of the unit current cell used for the first, second, third, fourth, fifth and sixth DAC.

Figure 5.9 shows the schematic of the DAC unit current cell used for the seventh, eighth, ninth and tenth DAC. The current cell is composed of eight transistors which are current source M1, current sink M4, cascode transistors M2 and M3 and four switches (M6, M7, M8 and M9). The output currents of the seventh and eighth DAC are fed into the first resistor ladder and the output currents of the ninth and tenth DAC are fed into the second resistor ladder. The resistor ladder converts all the currents back into voltages and automatically provides the threshold levels required for the quantizer.

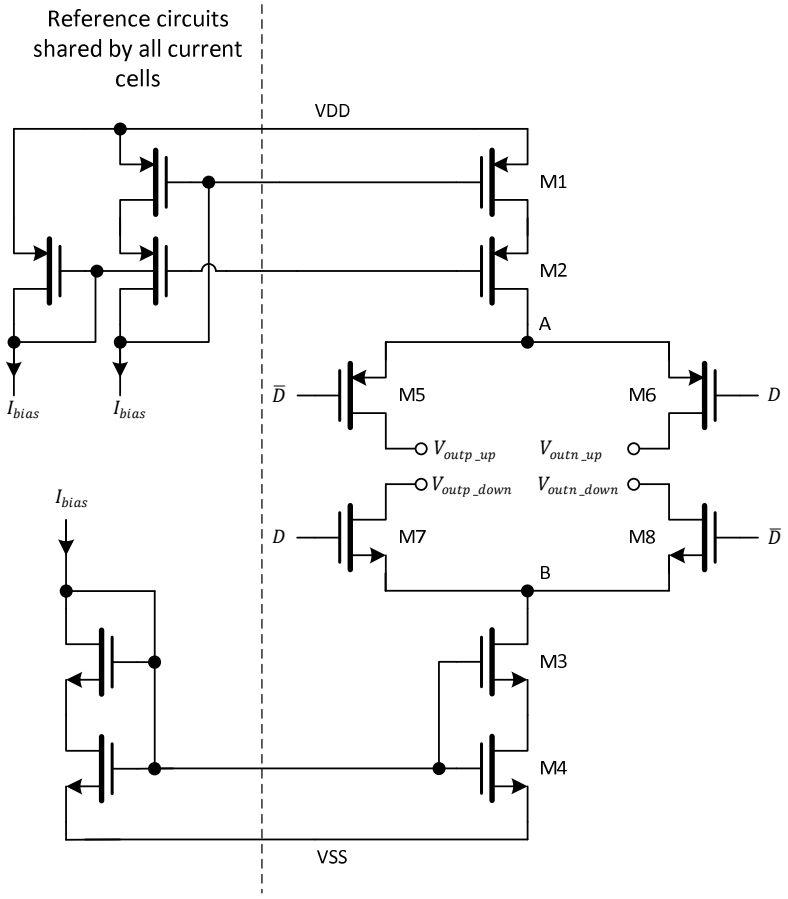


Figure 5.9: Schematic of the unit current cell used for the seventh, eighth, ninth, and tenth DAC.

In order to reduce the excess loop delay as well as the circuit complexity in this modulator, no DEM is used to shape the DAC error. Therefore, according to the MATLAB simulation results shown in Figure 4.5 and noise

budget, the mismatch error of the unit current cells should be as small as 0.1% for the first and second DAC, 0.78% for the third and fourth DAC and 6% for the remaining DACs.

For two MOS transistors with the same dimension and biasing conditions, the variance of the relative drain current mismatch error $\Delta I/I$ can be expressed as [40]:

$$\sigma^2_{\frac{\Delta I}{I}} = \sigma^2_{\frac{\Delta\beta}{\beta}} + \left(\frac{2}{V_{GS} - V_{TH}}\sigma_{\Delta V_{TH}}\right)^2 \tag{5.2}$$

where $\Delta\beta/\beta$ and ΔV_{TH} are the mismatches of the current factor β and the threshold voltage V_{TH} between those two transistors. If the mismatch is caused by the independent random disturbances of physical properties, and the correlation distance of the statistical disturbance is small compared to the active device area, then they can be approximated by

$$\sigma^2_{\frac{\Delta\beta}{\beta}} = \frac{A^2_\beta}{W.L} \text{ and } \sigma^2_{\Delta V_{TH}} = \frac{A^2_{V_{TH}}}{W.L} \tag{5.3}$$

where A_β and $A_{V_{TH}}$ are process dependant constants which is usually provided by the chip manufacturer. Using these equations, the minimum sizes of the devices are calculated by (5.4) as follows [41][42]:

$$(W.L)_{min} = \frac{\frac{1}{2}\left[A^2_\beta + \frac{4A^2_{V_{TH}}}{(V_{GS} - V_{TH})^2}\right]}{\sigma^2_{\Delta I}} \tag{5.4}$$

where, in our case, $\sigma_{\Delta I/I}$ of 0.1% should be used for the first and second DAC, 0.78% for the third and fourth DAC and 6% for the remaining DACs. In this design, the process dependant constants A_β and $A_{V_{TH}}$ were not provided by the foundry, therefore a monte-carlo simulation has been run 100 times to obtain the minimum size of the devices.

5.4.1 D Flip-Flop

The design of a fast D flip-flop is so important in CT ΔΣ modulators. The D flip-flop delivers NRZ data at the rising edge of the clock to DAC unit current cells. Here a very high speed and low jitter D flip-flop has been designed as shown in Figure 5.10. To achieve high speed, these transistors have been designed with minimum channel length and minimum size. Therefore it reduces the capacitor at the comparator output [44][45]. The delay of this D flip-flop is less than 100psec in all process corners and temperature. Therefore it is able to operate at the clock frequencies up to 10GHz.

The “Clock” pin is connected to the DAC clock and “IN” pin is connected to comparator outputs. The output of all 31 comparators in the first ADC and 15 comparators in the second ADC get synchronized with the DAC clocks.

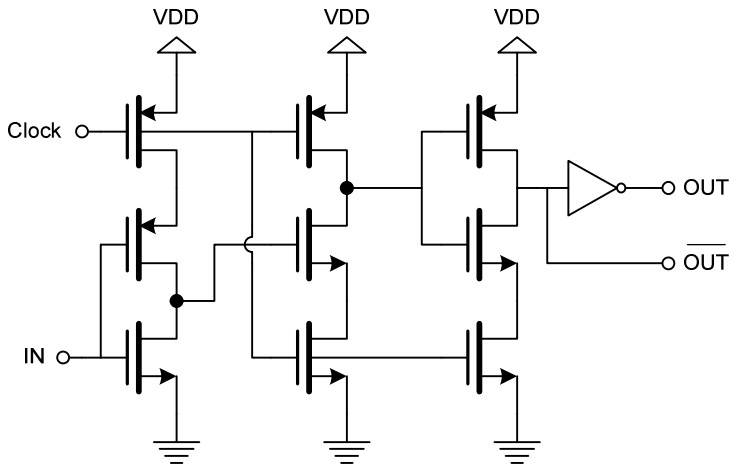


Figure 5.10: Schematic of D flip-flop.

5.5 Summation Circuits

This modulator requires two summation circuits. The first summation circuit is shown in Figure 5.11 and is placed before the first ADC and adds the direct feed-in signal coming from the output of the fourth opamp and the DAC feedbacks coming from the ninth and tenth DAC. The outputs of the second and third integrator are added together using the fourth opamp and then the output goes to the first summation circuit. The ninth and tenth feedback current DAC outputs are fed into the lower points of the first resistor ladder.

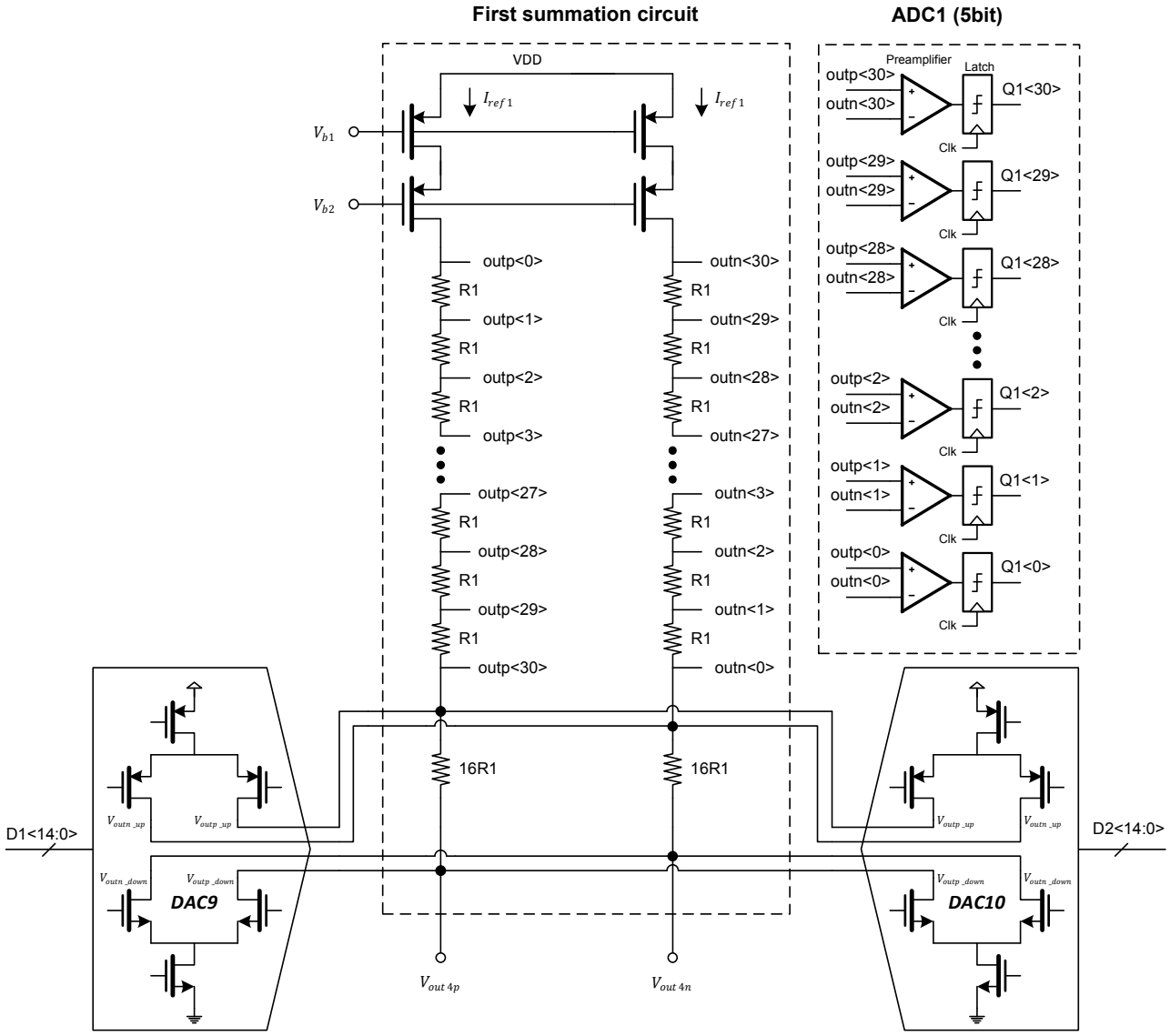


Figure 5.11: Schematic of the first ADC and the first summation circuit.

These DACs use the schematic shown in Figure 5.9. The resistor ladder converts all the DACs currents back into voltages and automatically generates the threshold voltages required by the quantizers of the first ADC. It can be shown that the input voltage of the *ith* comparator (*i* = 0, 1,..., 30) consists of four components and is given by (5.5).

$$V_{comp_i} = V_{out4} - V_{DAC9} - V_{DAC10} - V_{th_i} \quad (5.5)$$

The components V_{out4} , V_{DAC9} and V_{DAC10} represents the output of the fourth opamp, the ninth and tenth DAC voltage respectively. The ninth DAC voltage depends on I_{DAC9}, R_1(the unit resistance of the ladder) and $D1 < 14:0 >$ and the tenth DAC voltage relies on I_{DAC10}, R_1 and $D2 < 14:0 >$. The term V_{th_i} stands for the threshold voltage of the comparator *i* which is not dependent on the input signals, but is determined by the comparator number *i*, the bias current I_{ref1} and R_1 . Above mentioned components are given respectively by (5.6), (5.7) and (5.8).

$$V_{th_i} = (2i - 30)I_{ref1}R_1 \quad (5.6)$$

$$V_{DAC9} = 16R_1I_{DAC9}D1 \quad (5.7)$$

$$V_{DAC10} = 16R_1I_{DAC10}D2 \quad (5.8)$$

The second summation circuit is shown in Figure 5.12 and is placed before the second ADC and adds the direct signal coming from the output of the third integrator and the DAC feedbacks coming from the seventh and eighth DAC. The seventh and eighth feedback current DAC outputs are fed into the lower points of the second resistor ladder. Similarly, It can be shown that the input voltage of the *ith* comparator (*i* = 0, 1,..., 14) consists of four components and is given by (5.9).

$$V_{comp_i} = V_{out3} - V_{DAC7} - V_{DAC8} - V_{th_i} \quad (5.9)$$

The components V_{out3} , V_{DAC7} and V_{DAC8} represents the output of the third integrator, the seventh and eighth DAC voltage respectively. The seventh DAC voltage depends on I_{DAC7}, R_2(the unit resistance of the ladder) and $D1 < 14:0 >$ and the eighth DAC voltage relies on I_{DAC8}, R_2 and $D2 < 14:0 >$. The term V_{th_i} is determined by the comparator number *i*, the bias current I_{ref2} and R_2 . Above mentioned components are given respectively by (5.10), (5.11) and (5.12).

$$V_{th_i} = (2i - 14)I_{ref2}R_2 \quad (5.10)$$

$$V_{DAC7} = 16R_2I_{DAC7}D1 \quad (5.11)$$

$$V_{DAC8} = 16R_2I_{DAC8}D2 \quad (5.12)$$

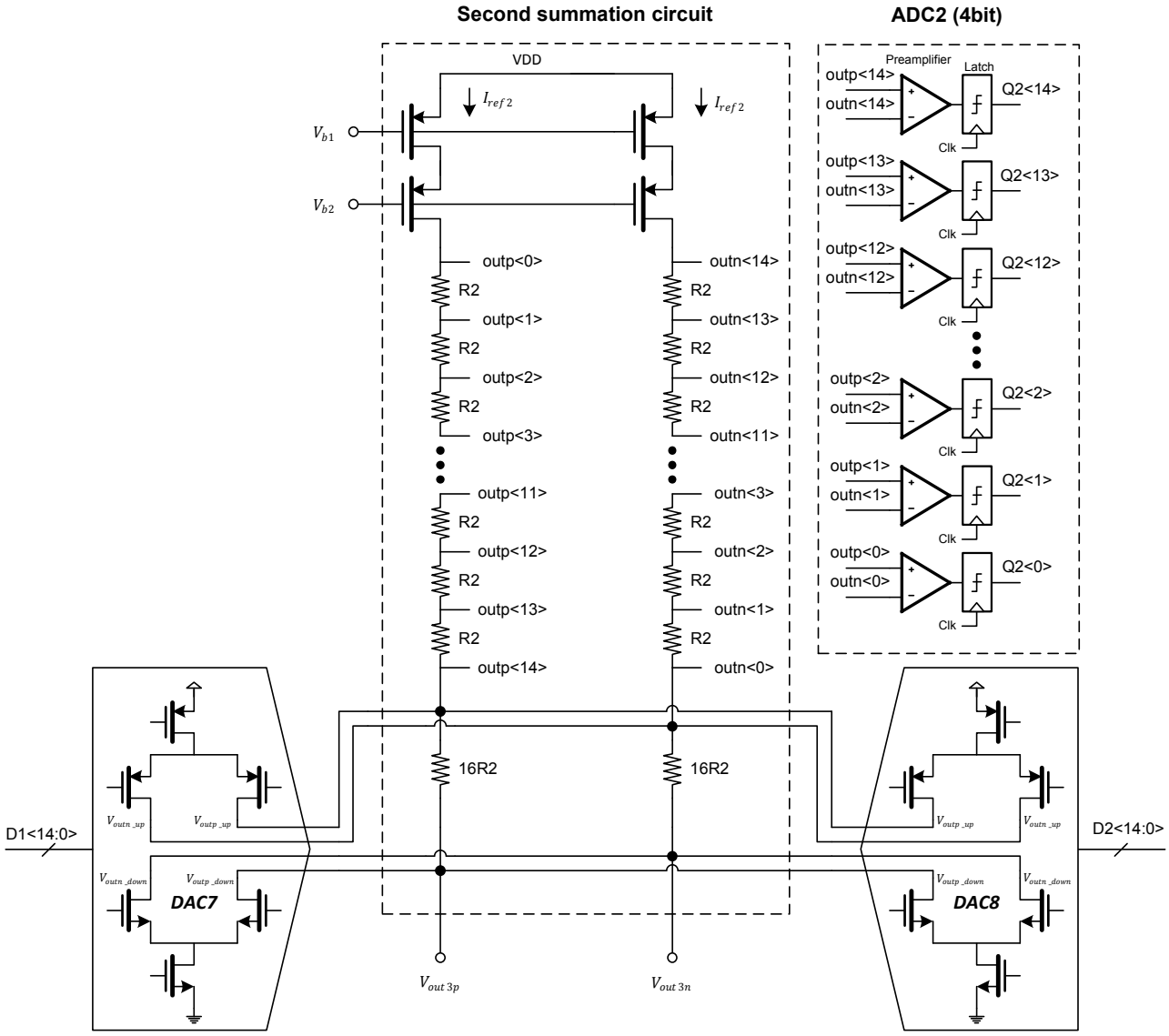


Figure 5.12: Schematic of the second ADC and the second summation circuit.

5.6 Analog-to-Digital Converters

This modulator requires two ADCs. The first ADC has 5-bit resolution and 31 comparators and the second ADC has 4-bit resolution and 15 comparators. These two ADCs were implemented as Flash ADCs and the general structures of them are shown in Figure 5.11 and 5.12 to perform the required conversion. Each latched comparator is composed of a single preamplifier stage and a latch. The preamplifier is used to amplify

the input signal and to minimize the input capacitance of the comparator. The preamplifier stage isolates the latch and the resistor ladder; therefore it reduces the kick-back noise seen in reference string during switching times of the comparator. The latch is used to compare the two amplified input signals comping from the preamplifier and to provide a digital rail-to-rail output signal.

5.6.1 Comparator Design

From the results obtained in the chapter 4, each comparator must have an accuracy of 10mV for the first ADC and 20mV for the second ADC to meet the 5-bit and 4-bit linearity requirements respectively. In addition, since there are a total number of 46 comparators in the prototype, a low power consumption comparator is desirable. As previously mentioned, each comparator has two circuits: a preamplifier and a latch circuit.

The preamplifier is implemented as a differential pair with a resistive load of $R = 5k\boldsymbol{\Omega}$ providing a gain of $g_{m_{IN}}R$ as shown in Figure 5.13. The input transistors have minimum length to increase the speed of the preamplifier. The comparator offset, which consists of the input offset of the preamplifier and the latch offset, will increase the quantization noise. The input referred offset of the latch is attenuated by the gain of the preamplifier usually 10 to 20) so it is negligible. The dimension of the input differential pair transistors of the preamplifier has to be enlarged to minimize this input offset. The large transistor size causes big parasitic capacitors C_p at the preamplifier input nodes. The sizes of the input transistors are chosen to reduce the mismatch to an acceptable level according to the equation $\sigma_{VT} = A_{VT}/\sqrt{WL}$ [40] where W and L are the width and length of the preamplifier input transistor. The acceptable σ_{VT} for the first and second ADC are 3mV and 6mV respectively. Based on $\sigma_{VT} = 3mV$, the width of $W = 28\mu m$ and the length of $L = 0.28\mu m$ are chosen for the input transistors of the preamplifiers of the first and second ADC.

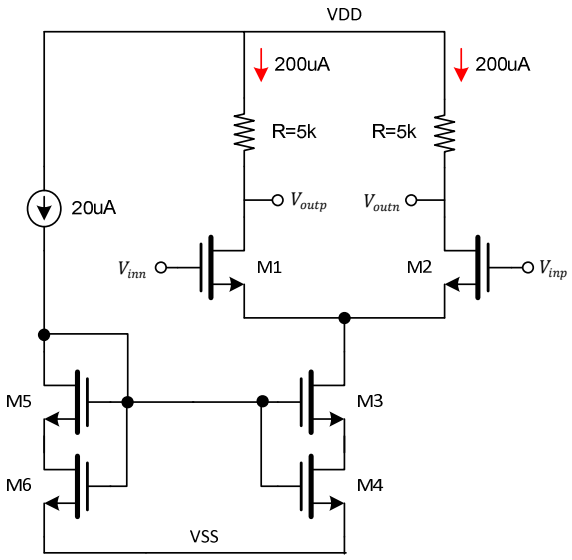


Figure 5.13: Schematic of the preamplifier.

The input signal is amplified by the preamplifier and fed into the regenerative latch. The latch is composed of a differential pair and two back-to-back inverters. When the latch phase occurs, the back-to-back inverters already have a starting point and form the positive feedback loop, will quickly amplify the input difference to the logic levels. The regenerative latch is shown in Figure 5.14.

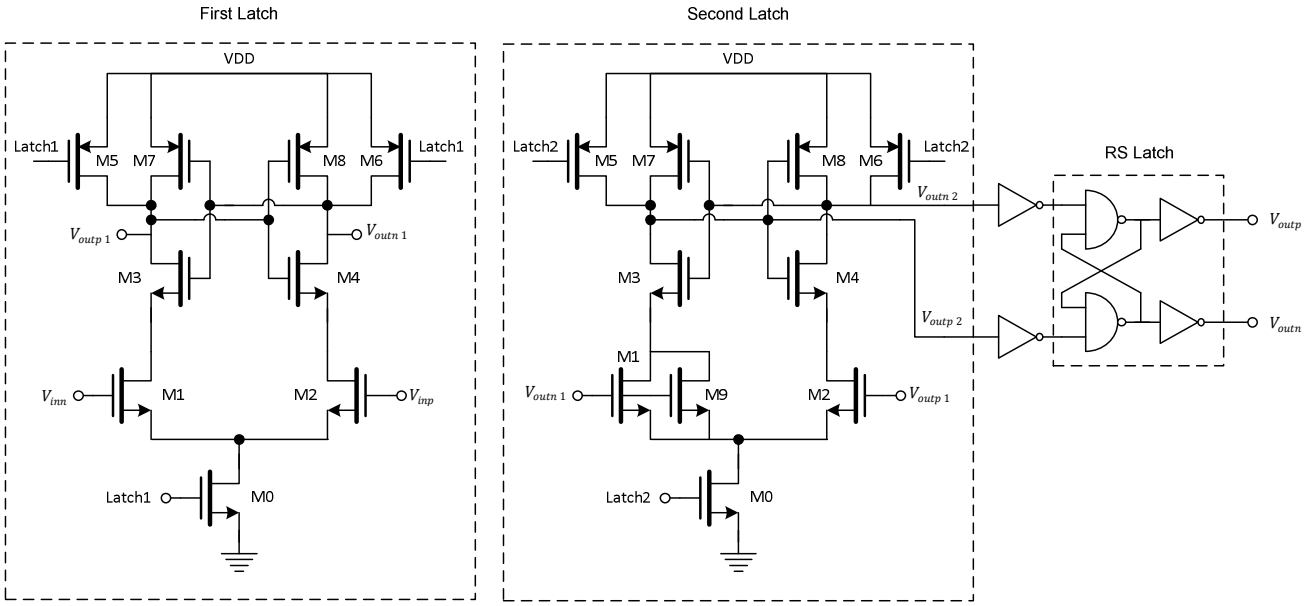


Figure 5.14: Schematic of the first, second and RS latch of the comparator.

To reduce the probability that the comparator goes into metastable mode, a second stage latch is added which is followed by the first latch. In order to decrease the signal dependency of the quantizer-delay, the second latch is derived with a different clock than the one is used for the first latch [14].

To make sure that the comparator always makes decision within the time constrain, the input transistors of the second latch M1 and M2 are slightly mismatched by adding a small size transistor M9 which has the same length like M1 and M2 as shown in Figure 5.14 [14]. The offset voltage created by the intentional mismatch is guaranteed to be greater than the output offset voltage of the first latch when the first latch goes into the metastable mode.

When the first latch is in the metastable mode, its outputs V_{outp1} and V_{outn1} stay very close together near $VDD/2$. As a result, the decision will be made by the second latch. This mode is illustrated in Figure 5.15. When the first stage is in the metastable mode, the decision taken by the quantizer can be true or false. However, it is worth mentioning that not making a decision would degrade the performance of a modulator much more than a wrongly taken decision.

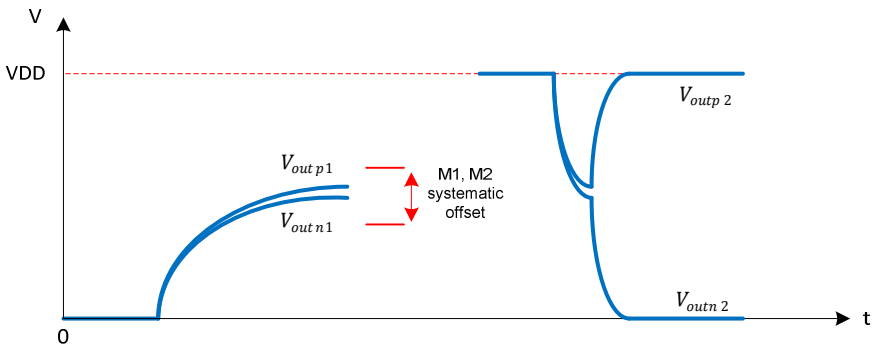


Figure 5.15: illustration of the output signals in metastable mode considering the second stage's systematic offset.

During the reset phase (when the latch signals is low), M5 and M6 are on and tying the two outputs to VDD. An RS latch follows the regenerative latch for two reasons. First, this latch can amplify the input difference further to reduce the metastability. Second, the RS latch will keep the quantizer output stable when the output of the regenerative latch is pulled up to the VDD during the reset phase.

A monte-carlo simulation has been run 200 times for the comparator circuit and the histogram of the offset voltage of the comparator is shown in the Figure 5.16. The mean value of the offset is around $65\mu V$ and the standard deviation of the offset voltage is around $\sigma = 2.2144mV$. The offset voltage of the comparator will be $V_{Offset} = 3\sigma = 6.64mV$.

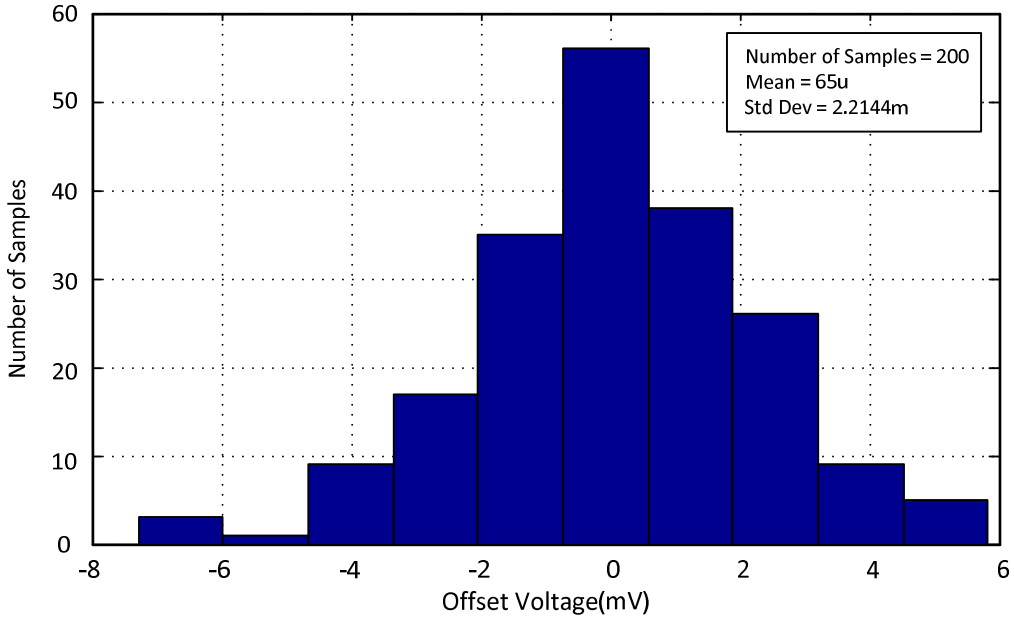


Figure 5.16: Histogram of the offset voltage of the comparator.

5.6.2 Thermometer-to-Binary Decoder

Two thermometer-to-binary decoders are used to convert the output of thirty one comparators of the first ADC and fifteen comparators of the second ADC which are in the form of thermometer code to four and five bit binary code using a digital encoder. There are several methods to implement the encoder like ROM [43], PLA etc. The encoder has been designed and implemented using dynamic CMOS logic method [44] and is described in the following pages. The truth table for direct conversion encoder for a 4-bit ADC is shown in Table 5.5.

Table 5.5: Truth Table for Direct Conversion Encoder for a 4-bit ADC.

Thermometer Code Input I_{14} to I_0	Encoder Output B_3 to B_0
000000000000000	0000
000000000000001	0001
000000000000011	0010
000000000000111	0011
000000000001111	0100
000000000011111	0101
000000000111111	0110
000000001111111	0111
000000011111111	1000
000000111111111	1001
000001111111111	1010
000011111111111	1011
000111111111111	1100
001111111111111	1101
011111111111111	1110
111111111111111	1111

For the 4-bit ADC, the equations for output binary bits are given by equation set (5.13). Clearly, these equations are realized using less number of gates compared to other methods [44].

$$B_0 = I_0 * \overline{I_1} + I_2 * \overline{I_3} + I_4 * \overline{I_5} + I_6 * \overline{I_7} + I_8 * \overline{I_9} + I_{10} * \overline{I_{11}} + I_{12} * \overline{I_{13}} + I_{14} \quad (5.13.a)$$

$$B_1 = I_1 * \overline{I_3} + I_5 * \overline{I_7} + I_9 * \overline{I_{11}} + I_{13} \quad (5.13.b)$$

$$B_2 = I_3 * \overline{I_7} + I_{11} \quad (5.13.c)$$

$$B_3 = I_7 \quad (5.13.d)$$

Similarly, the truth table for direct conversion encoder for the 5-bit ADC is presented in Table 5.6 and the equations for output binary bits of the 5-bit ADC are given by equation set (5.14).

$$B_0 = I_0 * \overline{I_1} + I_2 * \overline{I_3} + I_4 * \overline{I_5} + I_6 * \overline{I_7} + I_8 * \overline{I_9} + I_{10} * \overline{I_{11}} + I_{12} * \overline{I_{13}} + I_{14} * \overline{I_{15}} + I_{16} * \overline{I_{17}} + I_{18} * \overline{I_{19}} + I_{20} * \overline{I_{21}} + I_{22} * \overline{I_{23}} + I_{24} * \overline{I_{25}} + I_{26} * \overline{I_{27}} + I_{28} * \overline{I_{29}} + I_{30} \quad (5.14.a)$$

$$B_1 = I_1 * \overline{I_3} + I_5 * \overline{I_7} + I_9 * \overline{I_{11}} + I_{13} * \overline{I_{15}} + I_{17} * \overline{I_{19}} + I_{21} * \overline{I_{23}} + I_{25} * \overline{I_{27}} + I_{29} \quad (5.14.b)$$

$$B_2 = I_3 * \overline{I_7} + I_{11} * \overline{I_{15}} + I_{19} * \overline{I_{23}} + I_{27} \quad (5.14.c)$$

$$B_3 = I_7 * \overline{I_{15}} + I_{23} \quad (5.14.d)$$

$$B_4 = I_{15} \quad (5.14.e)$$

Table 5.6: Truth Table for Direct Conversion Encoder for a 5-bit ADC.

Thermometer Code Input I_{30} to I_0	Encoder Output B_4 to B_0
00000000000000000000000000000000	00000
00000000000000000000000000000001	00001
00000000000000000000000000000011	00010
00000000000000000000000000000111	00011
00000000000000000000000000001111	00100
00000000000000000000000000011111	00101
00000000000000000000000000111111	00110
00000000000000000000000001111111	00111
00000000000000000000000011111111	01000
00000000000000000000000111111111	01001
00000000000000000000001111111111	01010
00000000000000000000011111111111	01011
00000000000000000000111111111111	01100
00000000000000000001111111111111	01101
00000000000000000011111111111111	01110
00000000000000000111111111111111	01111
00000000000000001111111111111111	10000
00000000000000011111111111111111	10001
00000000000000111111111111111111	10010
00000000000001111111111111111111	10011
00000000000011111111111111111111	10100
00000000000111111111111111111111	10101
00000000001111111111111111111111	10110
00000000011111111111111111111111	10111
00000001111111111111111111111111	11000
00000011111111111111111111111111	11001
00000111111111111111111111111111	11010
00001111111111111111111111111111	11011
00011111111111111111111111111111	11100
00111111111111111111111111111111	11101
01111111111111111111111111111111	11110
11111111111111111111111111111111	11111

The dynamic CMOS circuit consists of a PMOS transistor, a bunch of NMOS transistors and an inverter. The PMOS transistor is used to pre-charge the output node and the NMOS logic is used to selectively discharge the output node. The schematic of an AND-OR gate implemented using dynamic CMOS logic is shown in Figure 5.17. It consists of a PMOS transistor driven by a clock signal and a NMOS transistor block defining the logic function. In NMOS evaluation logic, the transistors in series are ANDed and the branches in parallel are ORed.

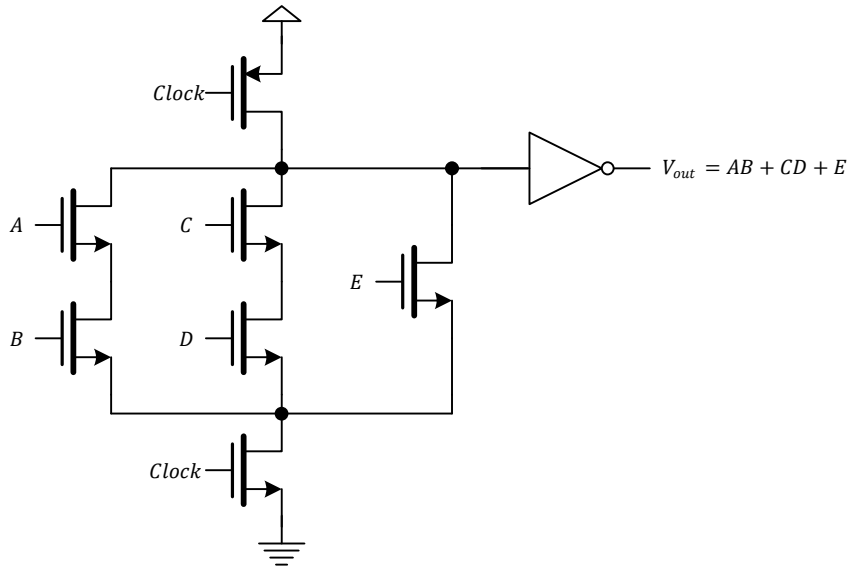
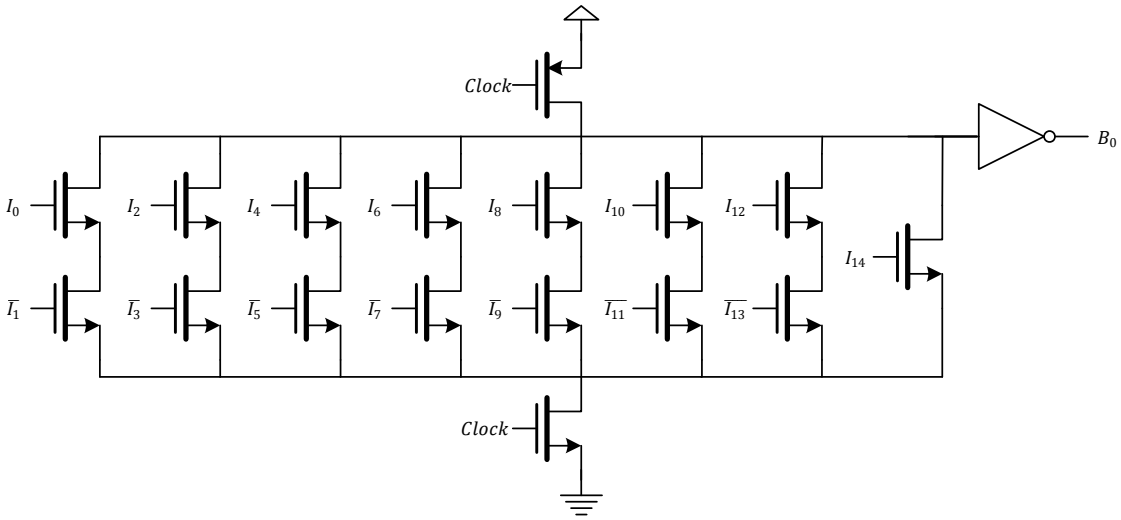
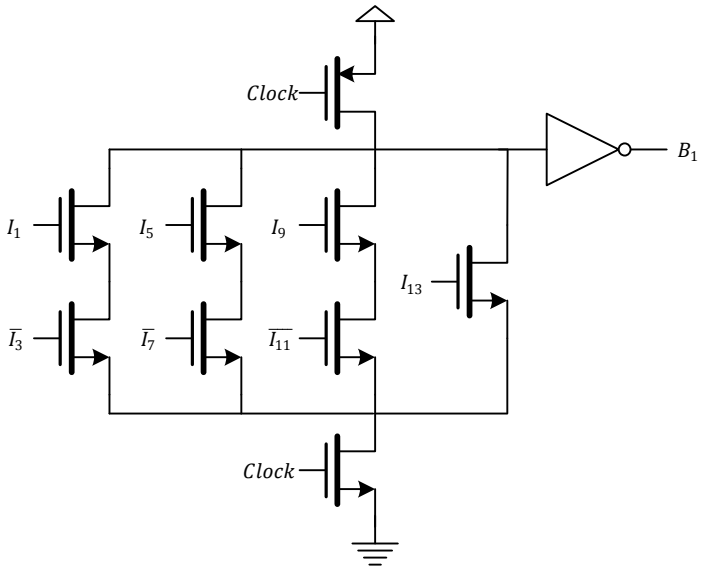


Figure 5.17: Schematic of dynamic CMOS AND-OR gates.

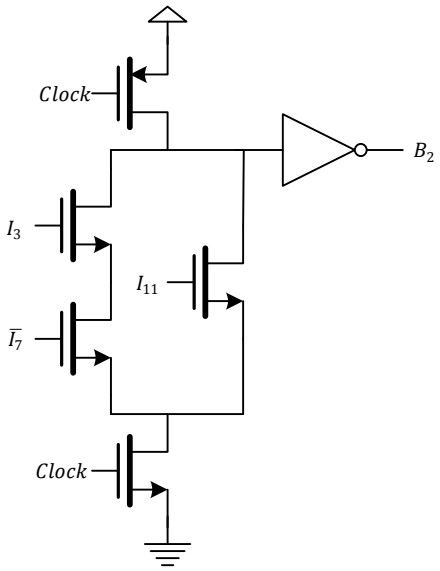
The thermometer-to-binary encoders have been implemented based on dynamic CMOS AND-OR gates topology. Figure 5.18 shows the encoder for the 4-bit ADC. B_0, B_1 and B_2 generation circuits are shown in sub-figure (a), (b) and (c) respectively.



(a) B_0 bit generation circuit.



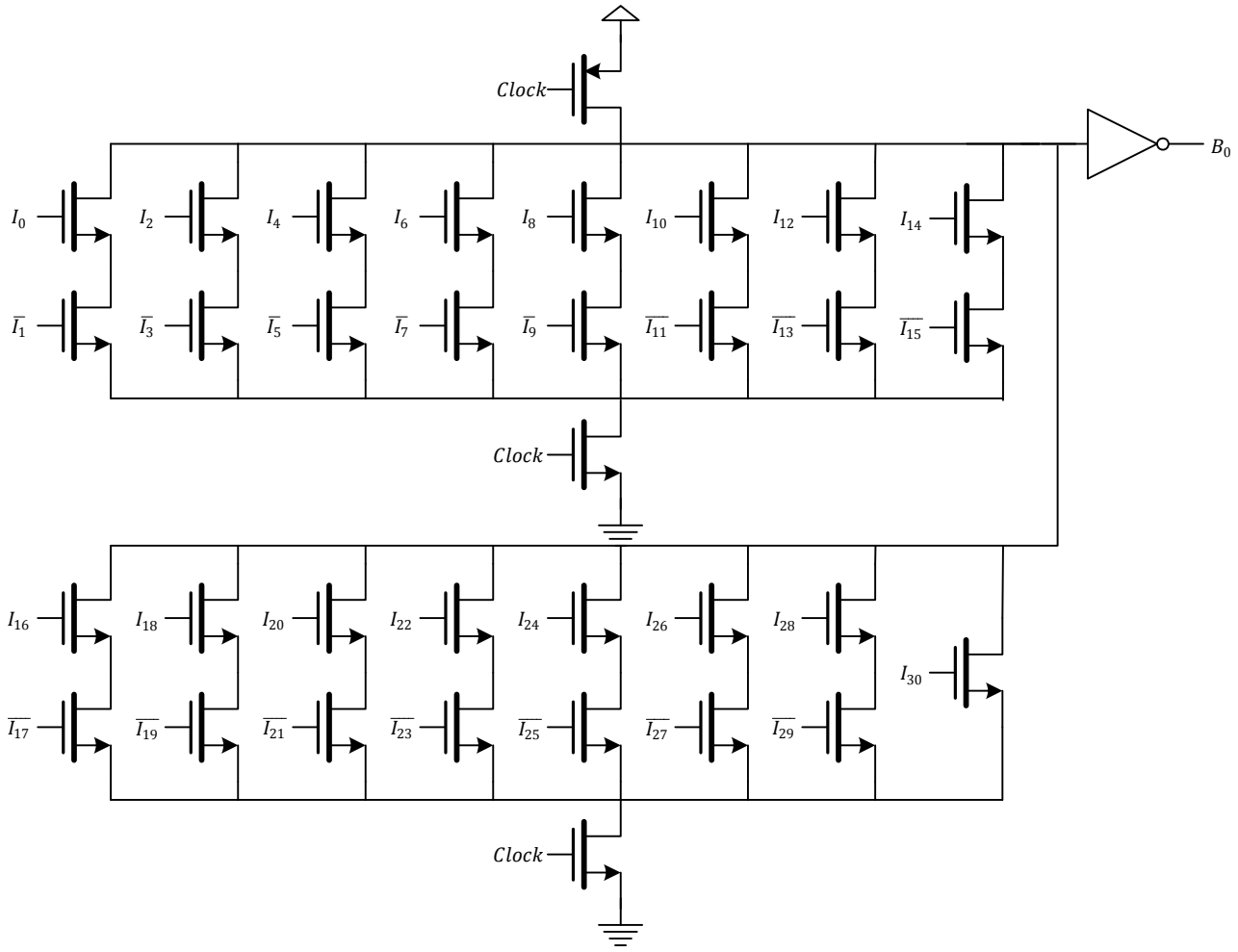
(b) B_1 bit generation circuit.



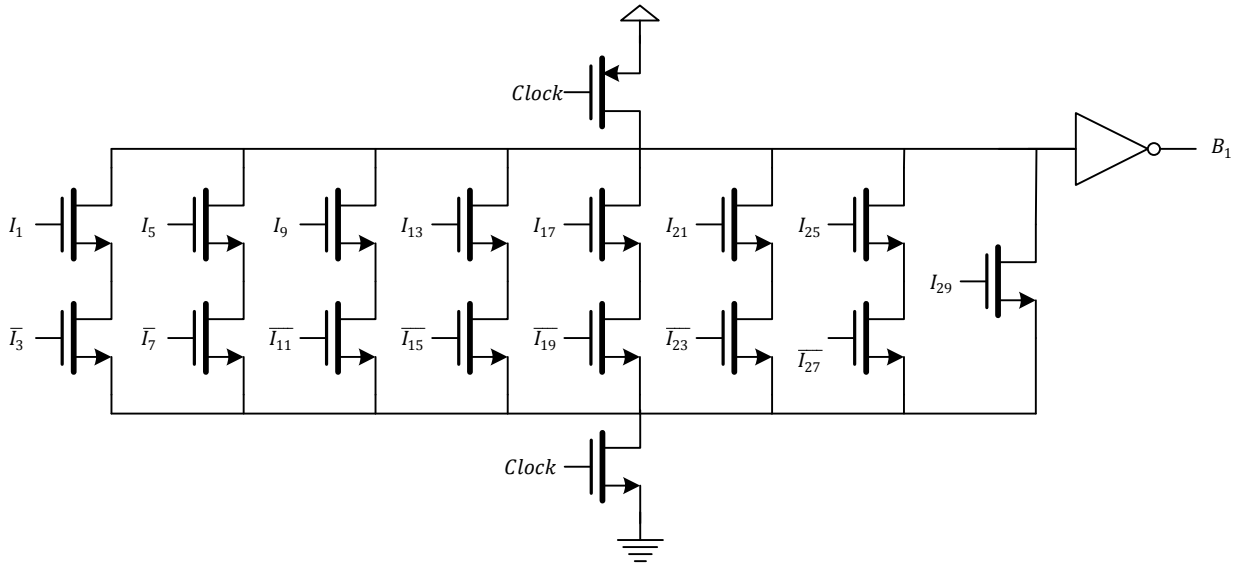
(c) B_2 bit generation circuit.

Figure 5.18: The encoder for the 4-bit ADC Based on dynamic CMOS AND-OR gates.

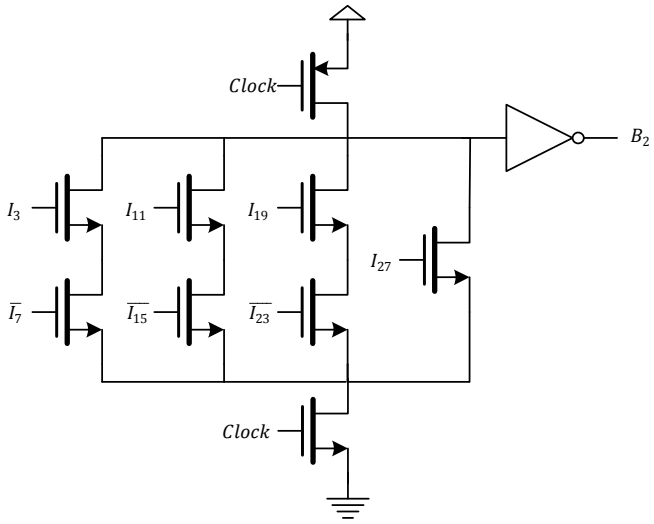
Figure 5.19 shows the encoder for the 5-bit ADC based on dynamic CMOS AND-OR gates topology. B_0, B_1, B_2 and B_3 generation circuits are shown in sub-figure (a), (b), (c) and (d) respectively.



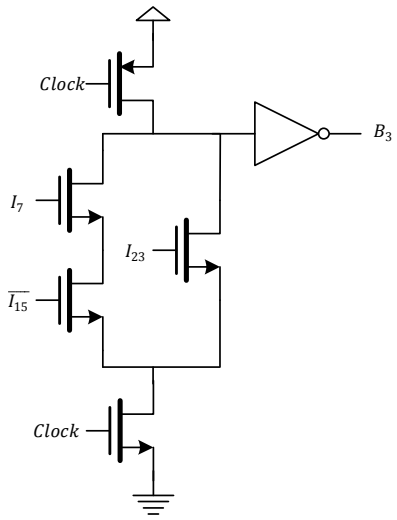
(a) B_0 bit generation circuit.



(b) B_1 bit generation circuit.



(c) B_2 bit generation circuit.



(d) B_3 bit generation circuit.

Figure 5.19: The encoder for the 5-bit ADC Based on dynamic CMOS AND-OR gates.

5.7 RC Time Constant Tuning

In modern semiconductor process, the absolute value of resistors and capacitors can vary as large as $\pm 15\%$ independently due to the change of process so the RC time constant of the integrators can vary as much as $\pm 30\%$ which causes the effectiveness of the noise shaping to be reduced and even drive the loop filters unstable. By considering the noise level to be less than -80dBFS, the accuracy of the RC time constant in

this CTTI ΔΣ modulator requires to be at most $\pm 3\%$ [46][47]. The schematic of the tuneable capacitor array is shown in Figure 5.20. The reset switch is used to short out the capacitors and reset the modulator.

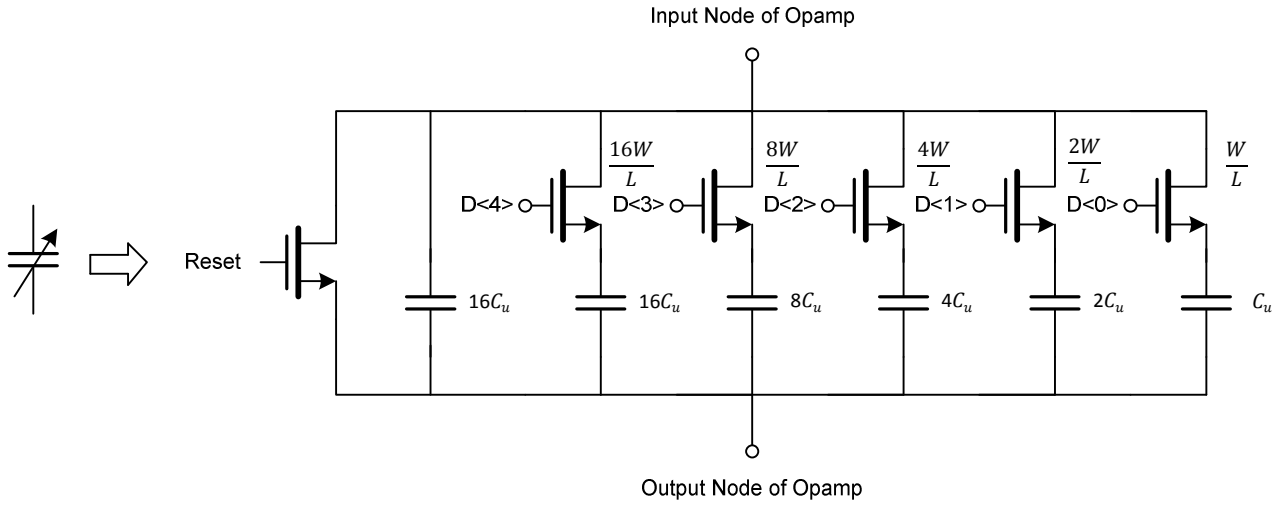


Figure 5.20: Tuneable capacitor array.

A 5-bit binary-weighted tuneable capacitor array is used for the integration capacitor of each integrator. The total capacitance is given by:

$$C_{total} = 16C_u + KC_u \ (K = 0,1,2,\dots,31) \tag{5.15}$$

The minimum, nominal and maximum capacitances of the capacitor array are:

$$C_{min} = 16C_u \tag{5.16}$$

$$C_{nom} = 32C_u \tag{5.17}$$

$$C_{max} = 47C_u \tag{5.18}$$

Therefore, the tuning range of capacitor array is:

$$\text{Tuning Range} = \left[\frac{C_{min}}{C_{nom}}, \frac{C_{max}}{C_{nom}}\right] \times 100\% = \left[\frac{16C_u}{32C_u}, \frac{47C_u}{32C_u}\right] \times 100\% = [50\%, 146.875\%] \tag{5.19}$$

and the tuning resolution is:

$$\text{Tuning Resolution} = \frac{Tuning\ Step}{C_{nom}} = \frac{C_u}{32C_u} = 3.125\% \tag{5.20}$$

Where C_{nom} and C_u stand for the nominal value of the integration capacitor and tuning step respectively. Five control bits $D < 4:0 >$ are required to realize the appropriate tuning code within a worse-case deviation

of 3.125% from the required RC time constant. As stated by (5.19), tuning range is from -50% to +46.875% of the nominal capacitance.

The tuning step capacitor value (C_u) for the first, second and third integrator are 35.33fF, 12.87fF and 4.88fF respectively. The width of $W = 1\mu m$ and the length of $L = 0.28\mu m$ are chosen for the switches.

5.8 Biasing Circuit

The biasing circuit generates all biasing currents for four opamps, two ADCs, ten DACs and two summation circuits. Each block including opamps, ADCs and DACs has its separate biasing circuit which uses cascaded current mirrors with large transistor lengths in order to increase the output impedance of mirroring devices. An external voltage of 0.8V enters the chip and it drops on an on-chip resistor through the use of a single-ended two-stage opamp which is self-biased. The reference voltage of 0.8V is accurate regardless of process variations but the currents generated will track the process variations of the on-chip resistors. The biasing circuit is shown in Figure 5.21 and generates four currents of $10\mu A$ for four opamps, two currents of $20\mu A$ for two ADCs, two currents of $25\mu A$ for two summation circuits, six currents of $10\mu A, 10\mu A, 5\mu A, 17\mu A, 2\mu A$ and $13\mu A$ for DAC1, DAC2, DAC3, DAC4, DAC5 and DAC6, two currents of $1\mu A$ and $11\mu A$ for DAC7, two currents of $3\mu A$ and $11\mu A$ for DAC8, two currents of $3\mu A$ and $11\mu A$ for DAC9 and one current of $35\mu A$ for DAC10.

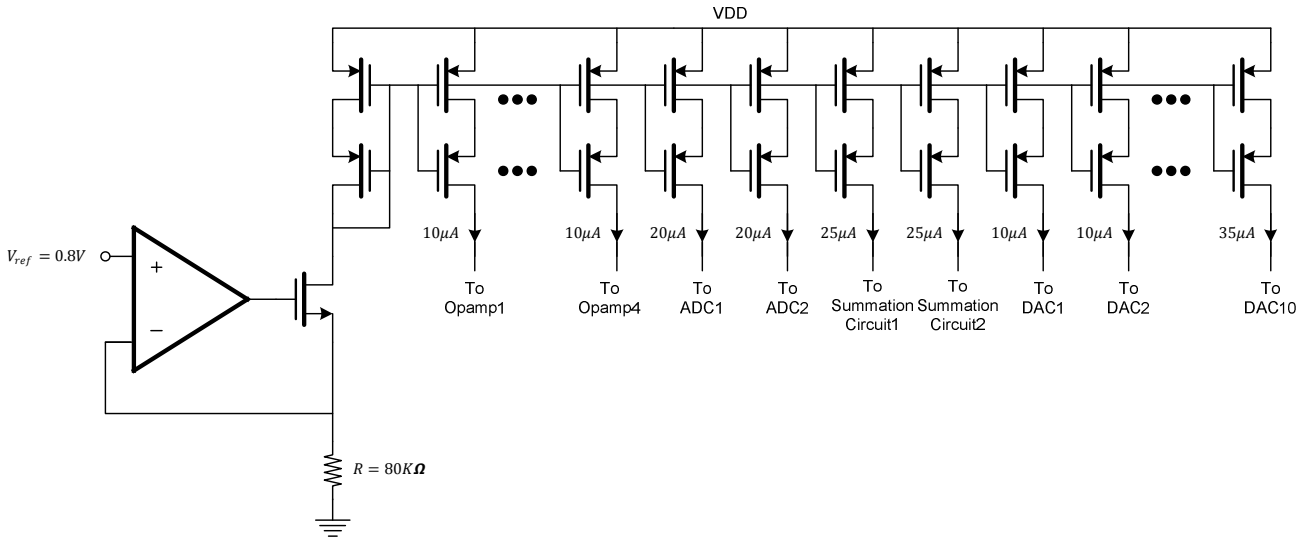


Figure 5.21: Schematic of the biasing circuit.

The opamp has been used in the biasing circuit is a single-ended two-stage opamp architecture and is shown in Figure 5.22. The sizes of transistors of the opamp are illustrated in Table 5.7.

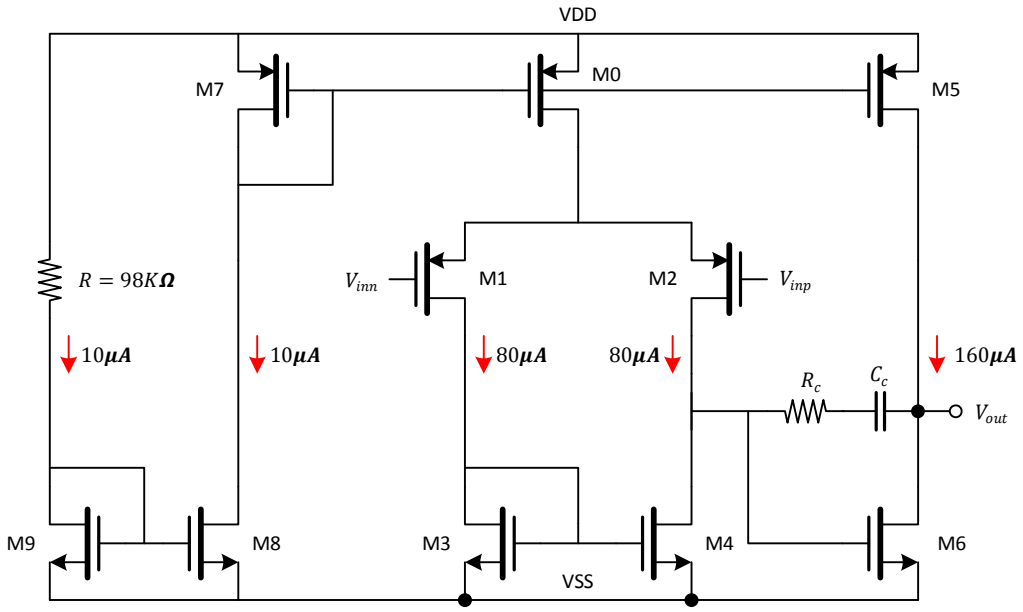


Figure 5.22: Schematic of the single-ended two-stage opamp used in the biasing circuit.

Table 5.7: The sizes of transistors of the single-ended two-stage opamp. The sizes (W and L) are in microns.

M0	M1, M2	M3, M4	M5	M6
W=10, L=1, M=16	W=5, L=0.3, M=8	W=2, L=0.3, M=16	W=10, L=1,M=16	W=2, L=0.3, M=32
M7	M8,M9	Cc	Rc	R
W=10, L=1, M=1	W=10, L=5, M=2	2pF	300	98K

5.9 Digital Error Correction

As explained in chapter 3, the output of the first ADC, $y_1(n)$ needs to be corrected before being applied to the inputs of DAC1, DAC3, DAC5, DAC7 and DAC9. A simple first order differencer $(1 - z^{-1})$ has been used to perform this correction as described in (3.19) and is shown in Figure 5.23.

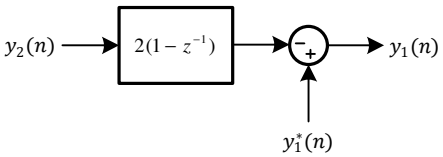


Figure 5.23: Block diagram of the error correction.

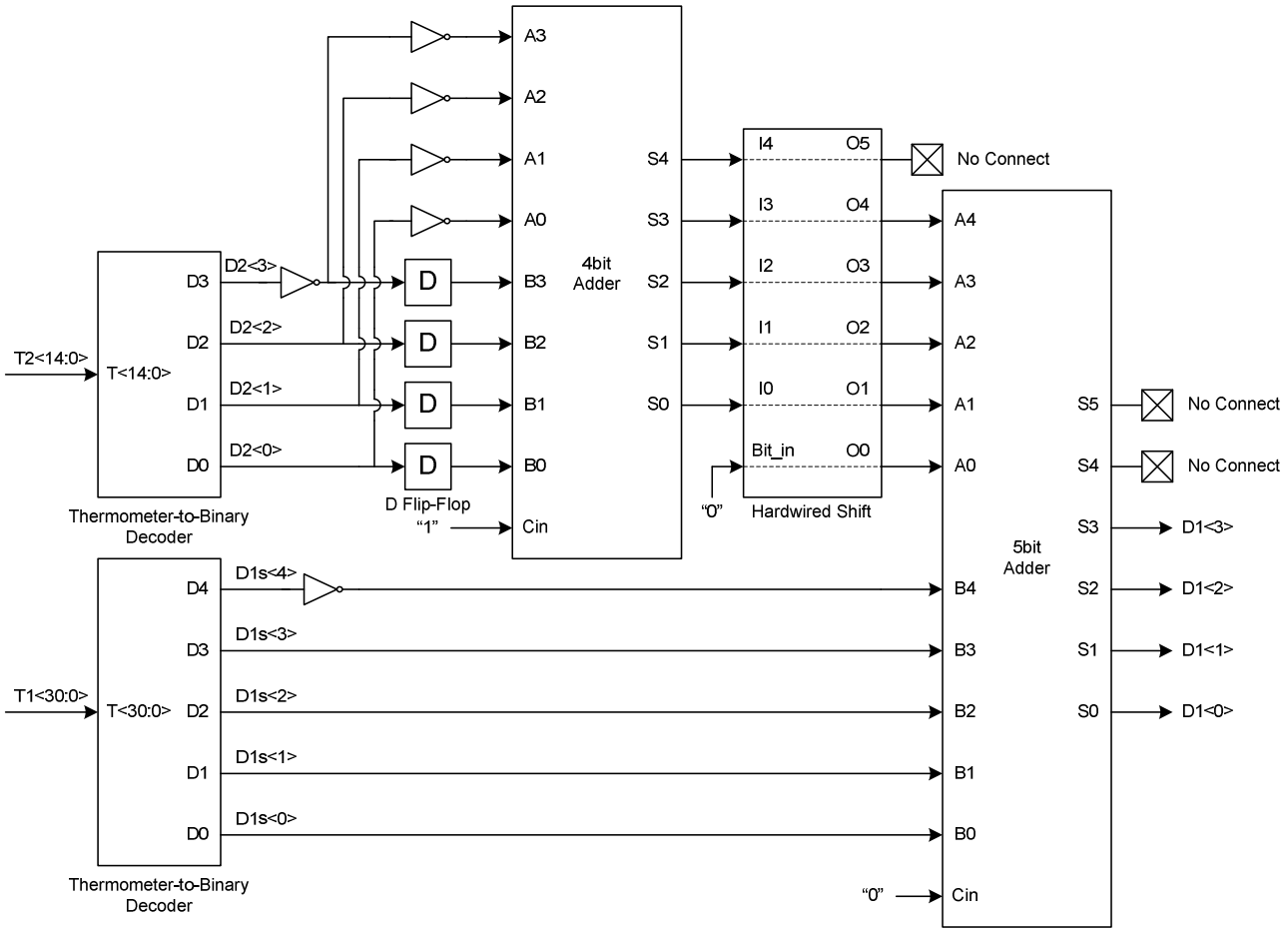


Figure 5.24: Schematic of the digital error correction circuit.

The digital error correction block has been implemented as shown in Figure 5.24. This circuit contains two thermometer-to-binary decoders, one 4-bit adder, one 5-bit adder, one 5-bit hardwired shift block, six inverters and four D flip-flops. The thermometer code T2<14:0> comes from the second ADC and is decoded to 4-bit binary code D2<3:0> then using an inverter and inverting the (Most Significant Bit) MSB (D2<3>), its two's-complement code is derived. These four bits go to four D flip-flops to make a delay and the outputs of these D flip-flops are fed into B3, B2, B1 and B0 input ports of the 4-bit adder. To perform subtraction operation, the other inputs A3, A2, A1 and A0 must be the two's-complements. Based on two's-complement theory, each bit is inverted by an inverter then one bit is added which the pin "Cin" (input carry) is connected to "1". These blocks make a simple first order differencer $(1 - z^{-1})$.

To multiply the outputs of the 4-bit adder to number two (c=2), it is required to use a simple 5-bit hardwired shift block to shift the input one bit to the right and connecting the input bit to “0” as shown in Figure 5.24. The outputs of the 5-bit hardwired shift block go the 5-bit adder. The thermometer code T1<30:0> comes from the first ADC and is decoded to 5-bit binary code D1<4:0> then using an inverter and inverting the MSB (D1<4>), its two’s-complement code is derived. These five bits go to the other inputs of the 5-bit adder. The pin “Cin” of the 5-bit adder is connected to “0”. The four (Least Significant Bit) LSBs of the outputs of the 5-bit adder will be D1<3:0> and go to DAC1, DAC3, DAC5, DAC7 and DAC9.

5.10 Clock Generator

The modulator requires clock signals for the two flash ADCs, ten DACs and the output multiplexer. Both flash ADCs are clocked at the same time and therefore their clock signals are the same. The clock signals of DACs are 180 degree phase shifted in comparison to the clock signals of the two ADCs. Both ADCs and ten DACs operate at 160MHz clock frequency but the output multiplexer works at 320MHz clock frequency. Figure 5.25 shows the simplified circuit diagram to generate clock signals. A D Flip-Flop is used as a frequency divider. One benefit of using toggle flip-flops for frequency division is that the output at any point has an exact 50% duty cycle. The final output clock signal will have a frequency value equal to the input clock frequency divided by two. The “Q” output of D Flip-Flop is used for the clock signals of the two ADCs (*CLK_ADC*) and the “QB” output of D Flip-Flop is used for the clock signals of DACs (*CLK_DAC*). *CLK_MUX* and

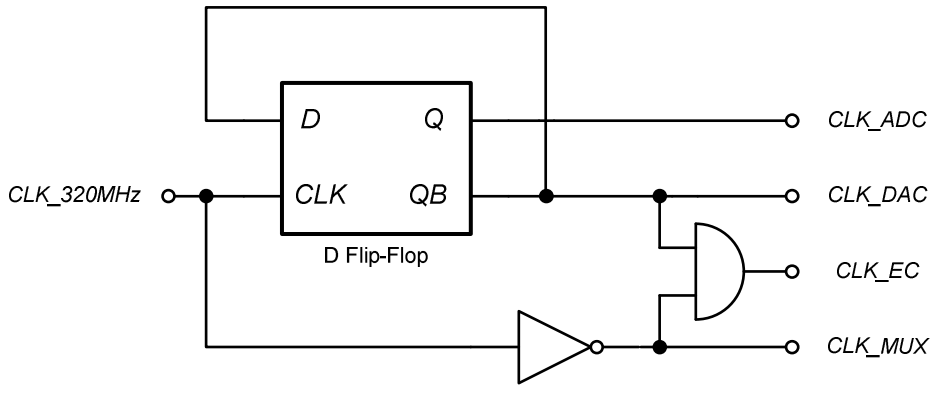


Figure 5.25: Clock generator.

CLK_EC are used as the clock signals for multiplexer and Error-Correction block respectively. Extreme process variations (slow model and fast model) have been taken into account in the design and simulations to make sure the timing is always correct. The clock signals are summarized in the timing diagram shown in Figure 5.26.

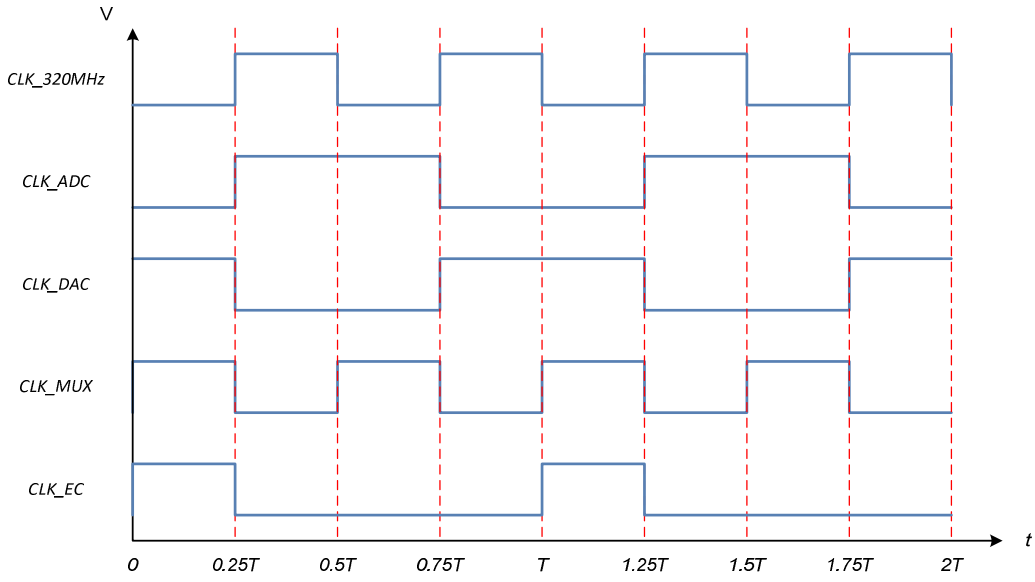


Figure 5.26: Clock signals (T=1/160MHz).

It is required to gain control over the time when DAC pulses are sent to the integrators with respect to the time when the flash ADC quantizes the signals, especially when ΔΣ modulators operate at high speeds and compensating for the loop delay [46]. A variable delay block used to accomplish this change in timing.

Ideally, the DAC pulses are sent to integrators 3.125*ns* (0.5T=0.5/160MHz) after quantization of the input signals by ADCs. Any small delay between the DAC and ADC clocks more than 3.125*ns* degrades the overall performance of the modulator. To accomplish this variable delay, a tuneable delay circuit between the DAC clocks and the flash ADC clocks is used to adjust the timing between these two sets of clocks so that an advance on the DAC clocks (with respect to the sampling instant of the flash ADC) of anywhere between 200*ps* to 3.0*ns* can be added. The circuit used to do this is shown in Figure 5.27, where there are two potential

paths that the clock signal may take, and there are various capacitors in the delayed path that may be added to slow down the signal [46].

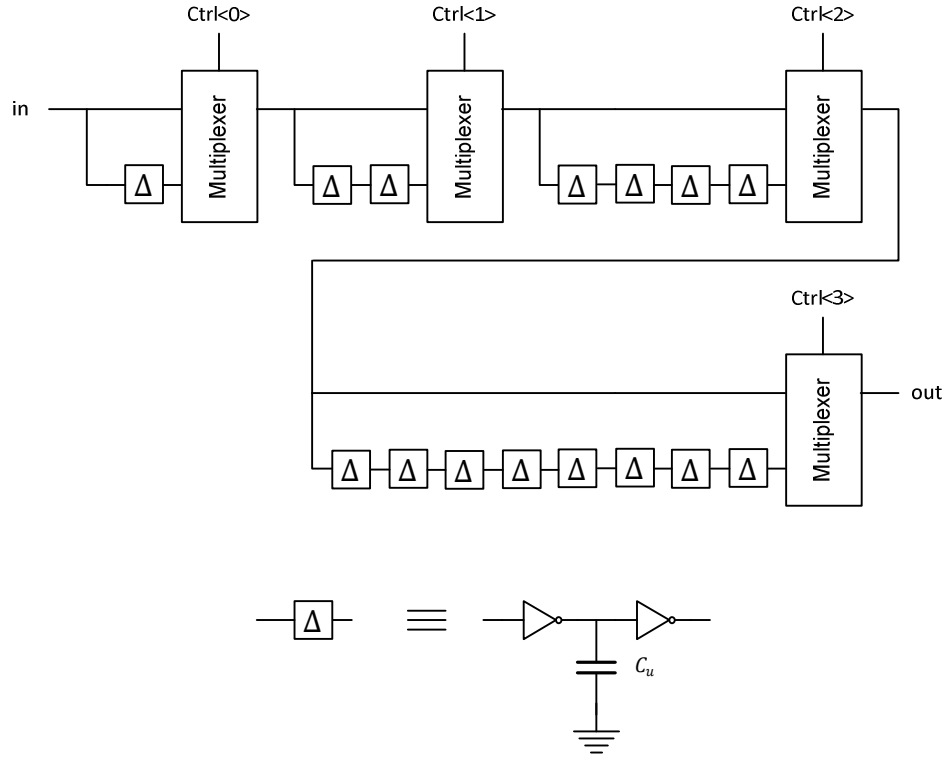


Figure 5.27: A variable delay block.

5.11 Modulator Front-End Noise Analysis

The device noise at the ΔΣ modulator front-end is not attenuated and thus it is a limiting factor in the total input referred noise of the modulator. There are three sources for the noise of the front-end:

1- Noise of the two input resistors,

2- Noise of the two-stage opamp, and

3- Noise of the current steering DAC1 and DAC2 to the virtual ground of the first integrator.

The equations from here on in this section use $K(=1.38\times10^{-23})$ to represent Boltzman constant; T to represent absolute temperature; $\Delta f(=10MHz)$ to represent the input signal bandwidth and g_{mi} to represent the transconductance of the ith transistor, respectively. The input referred noise of the two-stage opamp shown in Figure 5.28 can be expressed as:

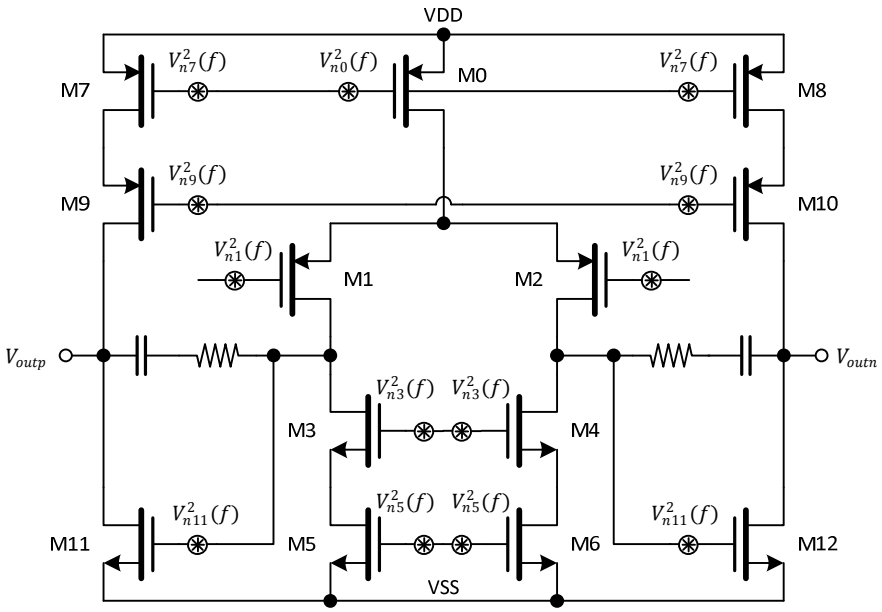


Figure 5.28: Noise sources in the two-stage opamp.

$$V_{neq}^2(f) = 2V_{n1}^2(f) + 2V_{n5}^2(f)\left(\frac{g_{m5}}{g_{m1}}\right)^2 \tag{5.21}$$

The noise coming from the second stage devices of the two-stage opamp is divided by the gain of the first stage and thus it is negligible and ignored in the noise calculation. If only thermal noise is considered, which means:

$$V_{neq}^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m} \tag{5.22}$$

Then the equivalent input referred noise can be expressed as below:

$$V_{neq}^2(f) = \frac{16kT}{3}\left(\frac{1}{g_{m1}}\right) + \frac{16kT}{3}\left(\frac{1}{g_{m5}}\right)\left(\frac{g_{m5}}{g_{m1}}\right)^2 \tag{5.23}$$

After referring the noise to the input of the modulator, we can get following input referred noise PSD of the opamp:

$$V_{opamp}^2(f) = V_{neq}^2(f)|1 + j2\pi f R_1 C_1|^2 \tag{5.24}$$

If only the band of interest is considered, which means $f \ll F_s$ with a normally high OSR, then the equation (5.24) can be simplified as below:

$$V_{opamp}^2(f) \cong V_{neq}^2(f) = \frac{16kT}{3}\left(1 + \frac{g_{m5}}{g_{m1}}\right) \cong 9.66 \times 10^{-18} \quad (5.25)$$

To obtain the SNR due to the opamp noise, the full-scale input signal power is divided by the noise as below:

$$SNR_{opamp} = 10log_{10}\left(\frac{P_{signal}}{P_{n_{opamp}}}\right) = 10log_{10}\left(\frac{V_{ref}^2/2}{V_{opamp}^2(f)\Delta f}\right) = 10log_{10}\left(\frac{0.5}{9.66 \times 10^{-18} \times 10MHz}\right) \quad (5.26)$$

$$SNR_{opamp} = 97dB$$

The total noise PSD of the two input resistors is:

$$V_{R_{in}}^2(f) = 8KTR_{in} \quad (5.27)$$

In this design, the values of the input resistors are chosen to be $10k\Omega$, these resistors generate thermal noise power which is:

$$P_{n_{R_{in}}} = 8KTR_{in}\Delta f = 8 \times 1.38 \times 10^{-23} \times 300 \times 10k\Omega \times 10MHz = 3.31 \times 10^{-9} \quad (5.28)$$

The SNR due to the resistors' noise is:

$$SNR_{R_{in}} = 10log_{10}\left(\frac{P_{signal}}{P_{n_{R_{in}}}}\right) = 10log_{10}\left(\frac{0.5}{3.31 \times 10^{-9}}\right) \cong 82dB \quad (5.29)$$

The noise from DAC1 and DAC2 can be derived as the following: It is assumed that the DAC full scale current is I_{DAC}. we look at one single current cell in the DAC shown in Figure 5.8, the major thermal noise is coming from transistors M1 and M4. The total in-band thermal noise current coming from M1 and M4 can be expressed as:

$$I_{DAC1}^2(f) = I_{DAC2}^2(f) = 4KT\left(\frac{2}{3}\right)(g_{m1} + g_{m4}) = 4KT\left(\frac{2}{3}\right)\left(\frac{2I_1}{V_{GS1} - V_{TH1}} + \frac{2I_4}{V_{GS4} - V_{TH4}}\right) \quad (5.30)$$

$$I_{DAC}^2(f) = I_{DAC1}^2(f) + I_{DAC2}^2(f) = \frac{16KT}{3}\left(\frac{2I_1}{V_{GS1} - V_{TH1}} + \frac{2I_4}{V_{GS4} - V_{TH4}}\right) \quad (5.31)$$

Here g_{m1} and g_{m4} are the transconductance of transistors M1 and M4 and $V_{GS1} - V_{TH1}$ and $V_{GS4} - V_{TH4}$ are the over-drive voltages of transistors M1 and M4, respectively. In this design, I_1 and I_4 are:

$$I_1 = I_4 = I_{cell} = \frac{I_{DAC}}{32} \quad (5.32)$$

I_{cell} is the DC current of each DAC cell and I_{DAC} is the full-scale current of the DAC. We assume $V_{GS1} - V_{TH1} = V_{GS4} - V_{TH4} = V_{GS} - V_{TH}$.

$$I_{DAC}^2(f) = \frac{16KT}{3}\left(\frac{2I_{cell}}{V_{GS1} - V_{TH1}} + \frac{2I_{cell}}{V_{GS4} - V_{TH4}}\right) = \frac{64KTI_{cell}}{3(V_{GS} - V_{TH})} \tag{5.33}$$

The total in-band thermal noise power coming from M1 and M4 can be expressed as:

$$P_{n_{DAC}} = V_{DAC}^2(f)\Delta f = I_{DAC}^2(f)R_{in}^2\Delta f = \frac{32KTI_{DAC}R_{in}^2}{3(V_{GS} - V_{TH})}\Delta f \tag{5.34}$$

The full scale input signal amplitude is $R_{in}I_{DAC}$, so the input signal power is:

$$P_{signal} = \frac{(I_{DAC}R_{in})^2}{2} \tag{5.35}$$

The SNR due to DAC1 and DAC2 is obtained as follows:

$$SNR_{DAC} = 10log_{10}\left(\frac{P_{signal}}{P_{n_{DAC}}}\right) = 10log_{10}\left(\frac{\frac{(I_{DAC}R_{in})^2}{2}}{\frac{32KTI_{DAC}R_{in}^2}{3(V_{GS} - V_{TH})}\Delta f}\right) = 10log_{10}\left(\frac{3I_{DAC}(V_{GS} - V_{TH})}{64KT\Delta f}\right) \tag{5.36}$$

By substituting $T = 300^0K, V_{GS} - V_{TH} = 0.4, I_{DAC} = 100\mu A$ and $\Delta f = 10MHz$, we get:

$$SNR_{DAC} \cong 77dB \tag{5.37}$$

The total input referred in-band noise due to the first stage integrator (including R_{in} and the two-stage opamp) and DAC1 and DAC2 is given by (5.38) and (5.39) as follows:

$$P_n = P_{n_{opamp}} + P_{n_{R_{in}}} + P_{n_{DAC}} \tag{5.38}$$

$$SNR = 10log_{10}\left(\frac{P_{signal}}{P_n}\right) \cong 76dB \tag{5.38}$$

5.12 Circuit Simulation Results

The whole CTTI ΔΣ modulator has been simulated with an input frequency of $F_{in} = 1.005MHz$ and $1.6V_{pp}$ (-2dBFS) amplitude at 320MHz sampling frequency across process corners and temperatures. Due to the excessive long simulation times, these circuit simulation results were obtained by using only 16384-point FFTs. Since the signal bandwidth is 10MHz, up to 512 frequency bins are included in the calculation of the SNDR. The circuit-level simulations have been run to make sure that the modulator is stable across process corners and temperatures. Table 5.8 summarizes the SNDR of the modulator obtained from circuit simulations

in typical, fast and slow process corners and at the room, low and high temperatures. The SNDR is in range from 74.5dB at SS and -40°C temperature to 75.9dB at FF and 120°C temperature.

Table 5.8: Summarized CTTI ΔΣ modulator's circuit simulation results.

Process Corners	*Temperature(°C)*	*SNDR(dB)*
TT	27	75.3
FF	-40	75.1
FF	120	75.9
SS	-40	74.5
SS	120	74.7

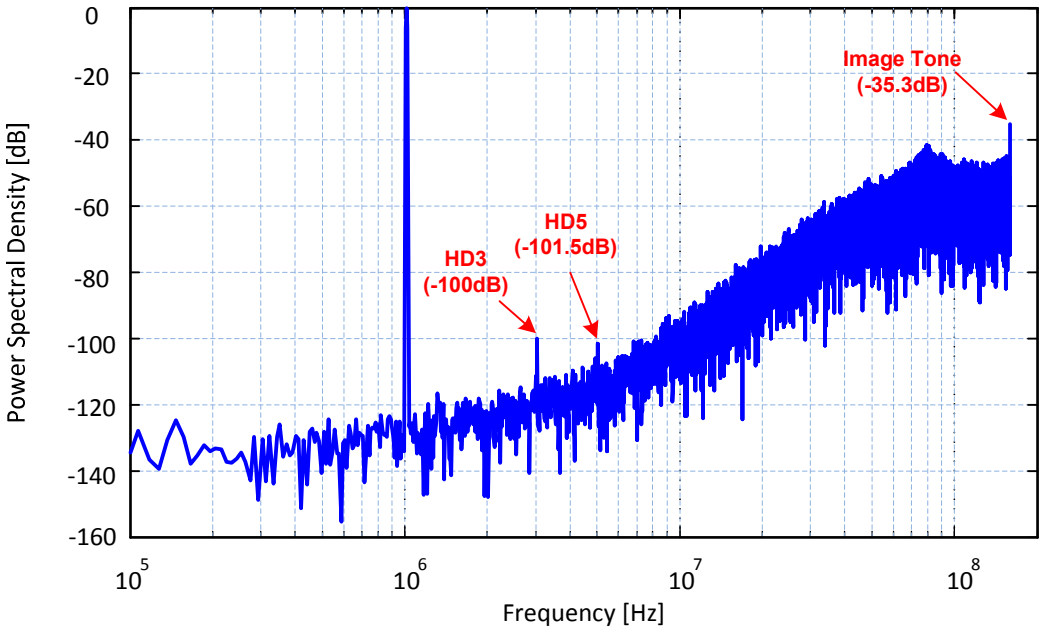


Figure 5.29: Output spectrum of the CTTI ΔΣ modulator in TT corner and 27°C temperature.

The output spectrum obtained from the circuit simulation at TT corner and 27°C temperature is shown in Figure 5.29. It can be seen that big tones reside at around the half clock frequency, 160MHz (Nyquist frequency). Those tones are images and they are created due to utilizing the time-interleaving technique in the modulator. Those tones are dangerous because they will fold back the out-of-band noise into the band of

interest and hence increase the in-band noise floor. The image tone located at $0.5F_{clk} - F_{in}$ has -35.3dB amplitude and should be attenuated enough in the decimation filter following this modulator.

The current consumption of the major blocks acquired from the circuit simulation in TT corner and 27'C temperature was summarized in Table.5.9. The total current consumption of the CTTI ΔΣ modulator in this process corner is 50.95mA. The ADCs consume more current than other circuit blocks in the modulator.

Table 5.9: Summarized current consumption of each block of the CTTI ΔΣ modulator.

Circuit	*Current Consumptiom (mA)*
Opamps	11.08
DACs	10.02
ADCs	17.6
Summation Circuits	4.15
Biasing Circuit	0.6
Digital	7.5
Total	50.95

5.13 Layout Considerations and Post-layout Simulation

The 3rd-order CTTI ΔΣ modulator is essentially a mixed signal system including a 3rd-order CT loop filter. The 3rd-order CTTI ΔΣ modulator has three active-RC integrators, two quantizers, ten DACs, the biasing circuit and two summation circuits. It also has purely digital blocks such the Error Correction block, the output multiplexer, the clock generator and clock buffers. To achieve a linear and a high resolution modulator, a great deal of caution should be taken in the layout design to reduce the effect of mismatch, parasitic and digital noise coupling to analog blocks.

Post-layout simulations were then run to ensure that the circuit was still operating according to the pre-layout simulations. Table 5.10 presents a summary of specifications of three integrators such UGBW and PM after running pre-layout and post-layout AC simulation in TT 27°C, FF 120°C and SS -40°C. As can be seen the

UGBW and PM of the integrators after running post-layout simulations are reduced in comparison to the pre-layout simulation results.

Table 5.10: Summarized integrators' pre-layout and post-layout circuit simulation results.

	Corner	*Pre-layout*		*Post-layout*	
		UGBW(MHz)	PM(deg)	UGBW(MHz)	PM(deg)
First Integrator	TT 27°C	971	77.7	842	68.5
	FF 120°C	1171	75.2	1007	67.2
	SS -40°C	820	78.7	820	68.7
Second Integrator	TT 27°C	1010	79.7	868	69.7
	FF 120°C	1213	76.1	1036	67.6
	SS -40°C	855	81.5	741	70.5
Third Integrator	TT 27°C	866	90.5	816	83.8
	FF 120°C	1044	87.0	975	80.9
	SS -40°C	735	92.4	696	85.3

Post-layout simulations were run for the whole modulator and it was simulated across corners and temperatures. Table 5.11 summarizes the SNDR of the modulator obtained from post-layout and pre-layout simulations. SNDR is in the range from 73.8dB at SS and -40°C temperature to 75.7dB at FF and 120°C temperature. As can be seen, SNDRs of the post-layout simulations have been dropped something between 0.2dB to 0.7dB in comparison to the pre-layout simulations.

Table 5.11: Summarized CTTI ΔΣ modulator's pre-layout and post-layout circuit simulation results.

Process Corners	*Temperature(°C)*	*Pre-layout*	*Post-layout*
		SNDR(dB)	SNDR(dB)
TT	27	75.3	74.8
FF	-40	75.1	74.9
FF	120	75.9	75.7
SS	-40	74.5	73.8
SS	120	74.7	74.1

5.14 Figure of Merit (FOM)

To find the optimal ΔΣ modulator implementation with respect to a minimal power consumption for a given modulator resolution (B bit) and signal bandwidth (f_B), a Figure of Merit is introduced. The fundamental equation employed in this approach is [1]:

$$FOM = \frac{P}{2^B 2 f_B} \tag{5.39}$$

Where P, B and f_B are the power consumption of the modulator, the number of bits of the quantizer and the signal bandwidth of the modulator respectively. The $FOMs$ were calculated for all modulators presented in Table 1.1 and also for the 3rd-order CTTI ΔΣ modulator designed in this PhD research. The results are illustrated in Table 5.12 as follows:

Table 5.12: Performance summary and resulting FOM according (5.21) of most recently published high-bandwidth ΣΔ modulators.

Paper	*CMOS Technology*	*Topology*	*Clock Frequency (MHz)*	*SNDR (dB)*	*Bandwidth (f_B)(MHz)*	*Power (P)(mW)*	*Number of Bits (B)*	FOM (pJ)
[3]	$0.13\mu m$	1-2 Cascaded DT	160	50	20	87	4	136
[4]	$0.18\mu m$	2-2 Cascaded CT	160	57	10	122	4	381
[5]	$0.18\mu m$	5th order CT	200	72	12.5	200	4	500
[6]	$0.13\mu m$	4th order CT	300	64	15	70	4	146
[7]	$0.18\mu m$	3rd order CTTI	200	49	20	103	4	160
[8]	$90nm$	5th order CT	400	52	10	7	1	175
[9]	$0.13\mu m$	3rd order CT	950	72	10	40	5	62.5
[10]	$0.18\mu m$	3rd order CT	640	66	10	7.5	1	187
[11]	$0.13\mu m$	3rd order CT	640	74	20	54	4	84
[12]	$0.25\mu m$	Complex CT	320	53.5	20	32	3	100
[13]	$0.13\mu m$	2nd order CT	640	51.4	20	6	2	37.5
[14]	$90nm$	2nd order CT	340	77	20	56	4	87.5
[15]	$0.13\mu m$	3rd order CT	900	78	20	87	5	68
[16]	$0.18\mu m$	3rd order CT	320	74	10	36	4	112.5
[17]	$0.18\mu m$	5th order CT	320	83.69	5	19.8	4	124
[67]	$0.13\mu m$	3rd order CT	640	75.3	10	7.2	4	22.5
[57]	$28nm$	3rd order CT	640	70.1	20	6	4	9.5
This work	$90nm$	3rd order CTTI	320	75	10	87	4	271

5.15 Conclusion

In this chapter, the circuit design and simulation results of the 3rd-order two-path CTTI ΔΣ modulator have been presented. The CTTI ΔΣ modulator has been designed through the use of 90nm TSMC CMOS technology with supply of 1.8V for analogue part and 1.2V for digital part. The operating frequency of all blocks except for the output multiplexer is 160MHz but the output multiplexer operates at 320MHz clock rate. Active-RC integrators are used in this modulator and a tuneable capacitor array is used for each integrator to tune up the RC time constant of the integrator. Three two-stage miller-compensated opamps have been utilized for the first, the second and the third integrator. Ten 4-bit current-steering DACs have been designed to operate at 160MHz with NRZ pulses.

The CTTI ΔΣ modulator has two flash ADCs. The first ADC has 5-bit resolution and 31 comparators and the second ADC has 4-bit resolution and 15 comparators. Each comparator has a preamplifier and two latches. To reduce the probability of the metastable mode in the comparator, the second latch is added and followed the first latch.

Finally, the pre-layout and post-layout simulation results of the whole CTTI ΔΣ modulator at 320MHz clock frequency across process corners and temperatures have been presented.

Chapter 6: Conclusion and Future Work

6.1 Conclusion Remarks:

The main motivation of this PhD research was to develop the time-Interleaving techniques for CT ΔΣ modulators. As explained previously, one of the restricting issues was the delayless feedback path problem. A novel technique has been proposed and reported in the thesis which substancially resolves this issue by inducing an error to the analog domain and corrects this error in the digital domain. To verify this method a 3rd-order two-path CTTI ΔΣ modulator with an OSR of 16 has been design using Cadence Virtuoso and 90nm CMOS TSMC technology.

The study resulted in six publications listed below:

1. J. Talebzadeh, and I. Kale, "Time-Interleaved Delta-Sigma Modulators" World Intellectual Property Organization WO2015/144771A1 Patent, 2015.
2. J. Talebzadeh, and I. Kale, "A Novel Two-Channel Continuous-Time Time-Interleaved 3rd-order Sigma-Delta Modulator with Integrator-Sharing Topology," IET, The Oxford Circuits and Systems Conference (OXCAS), September 2017, Oxford, UK.
3. J. Talebzadeh, I. Kale, "A 28mW 320MHz 3rd–order Continuous-Time Time-Interleaved Delta-Sigma Modulator with 10MHz Bandwidth and 12 Bits of Resolution," IEEE 7th International Conference on Circuits and Simulations (ICCSS), July 2017, London, UK.
4. J. Talebzadeh, I. Kale, "A general formula for impulse-invariant transformation for continuous-time Delta-Sigma Modulators," IEEE 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), June 2017, Giardini Naxos, Italy.
5. J. Talebzadeh, and I. Kale, "Design and Simulation of a 3rd-order Discrete-Time Time-Interleaved Delta-Sigma Modulator with Shared Integrators between Two Paths" IEEE Iranian Conference on Electrical Engineering (ICEE), May 2017, Tehran, Iran.

6. J. Talebzadeh, and I. Kale, “Design of a Delayless Feedback Path Free 2nd-order Two-Path Time-Interleaved Discrete-Time Delta-Sigma Modulator- a New Approach” IEEE 1st Conference on PhD Research in Microelectronics and Electronics Latin America (PRIME-LA), February 2017, Bariloche, Argentina.

In addition to the already published papers and patent, four more papers have been written which the first and second ones are the extended versions of the papers presented in PRIME-LA and OXCAS conference and were invited to be submitted to Advances in Science, Technology and Engineering Systems Journal and Springer Journal of Analog IC and Signal Processing respectively.

1) J. Talebzadeh, I. Kale, “Design of a delayless feedback path free 2nd-order two-path time-interleaved discrete-time delta-sigma modulator- a new approach,” Advances in Science, Technology and Engineering Systems Journal (ASTESJ).
2) J. Talebzadeh, I. Kale, “A Novel Two-Channel Continuous-Time Time-Interleaved 3rd-order Sigma-Delta Modulator with Integrator-Sharing Topology,” Springer Journal of Analog IC and Signal Processing.
3) J. Talebzadeh, and I. Kale, “A General Formula for Impulse-Invariant Transformation for Continuous-Time Delta-Sigma Modulators with an Arbitrary DAC Waveform,”
4) J. Talebzadeh, and I. Kale, “A 2-1 Cascaded Time-Interleaved Delta-Sigma Modulator,”
5) J. Talebzadeh, and I. Kale, “Comparison of the Impulse Invariant Transformation with the Modified Z-Transformation methods for converting DT to CT DS Modulators,”

The main accomplishments of the thesis on a chapter-by-chapter basis can be summarized as follow:

Chapter 1 is dedicated to explaining the motivation of this PhD research and presenting a table of the recently published high-band width ΔΣ modulators and summarizing the novelty and performance benefits.

In chapter 2, the concept of noise shaping, DT-to-CT conversion, CT ΔΣ modulators, Impulse Invariant Transformation, Z-Transform are presented along with some design examples. In this chapter a general formula for converting nth-order DT ΔΣ modulator to an nth-order equivalent CT ΔΣ modulator is presented.

In chapter 3, first a 3rd-order DTTI ΔΣ modulator with one set of integrators is derived using time domain equations and then it is converted to an equivalent 3rd-order CTTI ΔΣ modulator. The delayless feedback path problem is discussed in this chapter. The novel method to solve this issue is proposed and compared with other methods.

In chapter 4, The MATLAB simulation results for the 3rd-order CTTI ΔΣ modulator with proposed method are presented in this chapter.

In chapter 5, the circuit design of the 3rd-order two-path CTTI ΔΣ modulator is presented. The modulator has been designed using Cadence Virtuoso and 90nm CMOS TSMC technology with power supply of 1.8V for analogue and 1.2V for digital part.

6.2 Future Work:

The proposed CTTI ΔΣ modulator can be utilized in WIFI and wireless communication applications has a very good potential to operate at higher frequencies if newer technologies like 16nm technology with Finfet transistor is utilized. The number of paths can be easily increases to four or eight but it makes the design a bit complicated and needs a team of designers to implement it.

In this PhD research, 1.8V devices have been used which the minimum length for these transistors is $280nm$. If 1.2V devices are used for the future project or the research then the minimum length for low-voltage devices is $100n$ and the transistor width can be reduced by the ratio of $100n/280nm = 1/2.8$. The parasitic capacitors are reduced by the ratio of $2.8 \times 2.8 \cong 7.85$. Therefore, a ΔΣ modulator with higher sampling frequency can be implemented. Another advantage of using low-voltage device is that the power consumption will be reduced by the ratio of $1.2/1.8 = 0.67$ in the case the current consumption remains the same.

In this thesis a general formula is presented for a CT-to-DT conversion through the Impulse Invariant Transformation for CT ΔΣ modulators with rectangular DAC waveforms to map an nth-order DT ΔΣ modulator to an nth-order equivalent CT one. This formula can be expanded to cover any arbitrary DAC waveforms in CT ΔΣ modulators.

As explained in chapter 2, there are two methods to convert a DT ΔΣ modulator to an equivalent CT ΔΣ modulator, the modified z-transform and the Impulse Invariant Transformation; it can be shown that these two transformations conceptually are different but mathematically they result in the same CT ΔΣ modulator.

Appendix A:

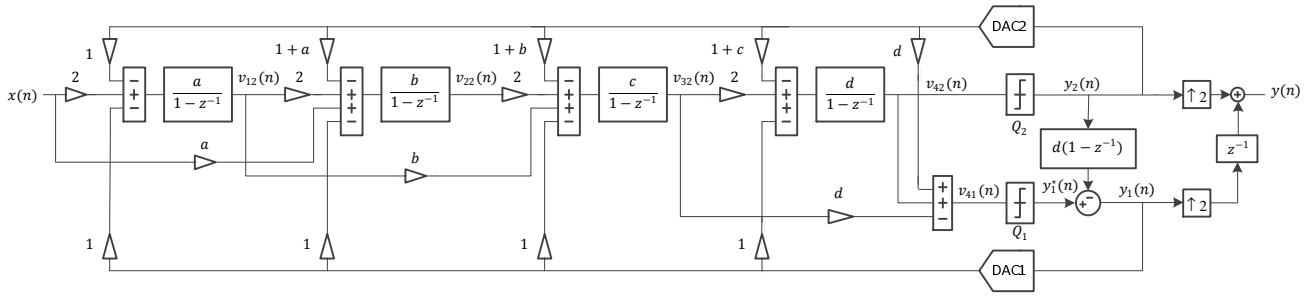


Figure A.1: a 4th-Order Two-Path DTTI ΔΣ Modulator.

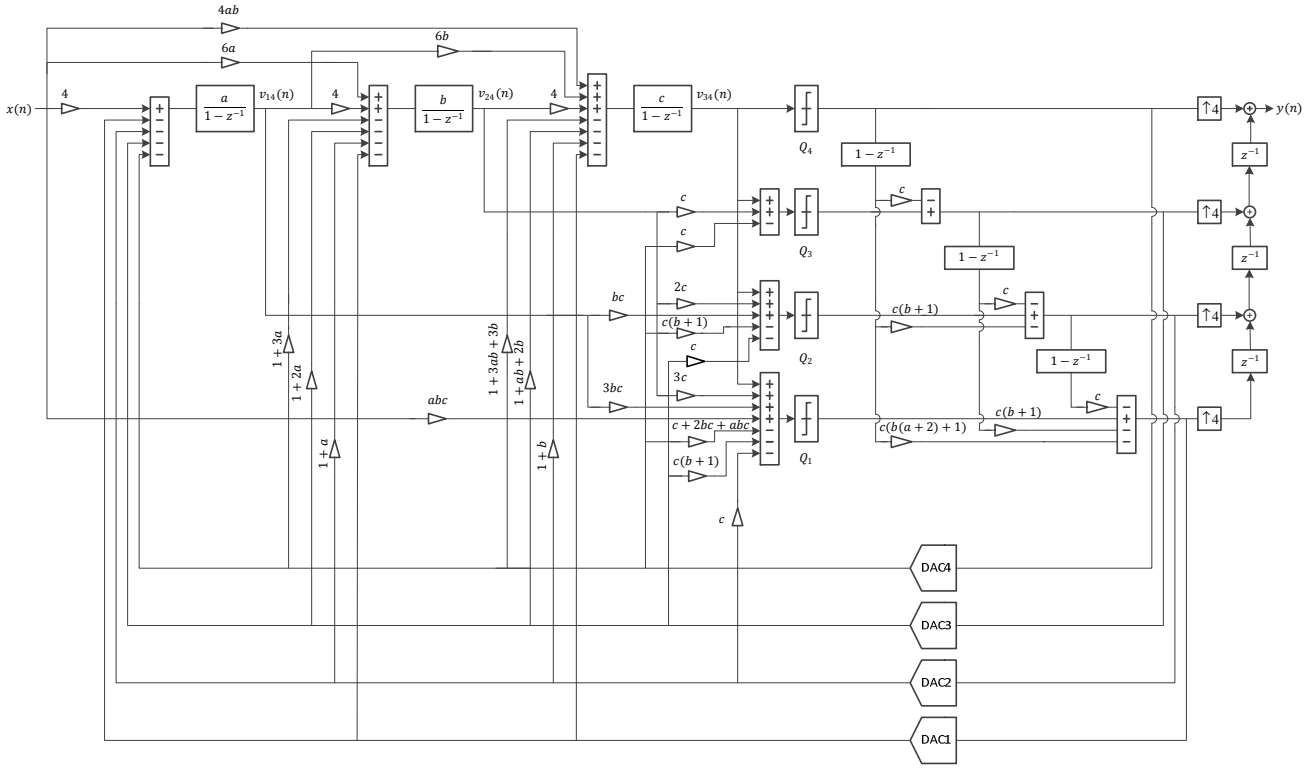


Figure A.2: a 3rd-Order Four-Path DTTI ΔΣ Modulator.

Appendix B:

B.1 CT to DT Conversion:

A DT ΔΣ modulator and a CT ΔΣ modulator are shown in Figure B.1, and are said to be equivalent when their quantizer inputs are equal at the sampling instants.

$$q(n) = q_c(t)|_{t=nT} \quad \text{for all n} \tag{1}$$

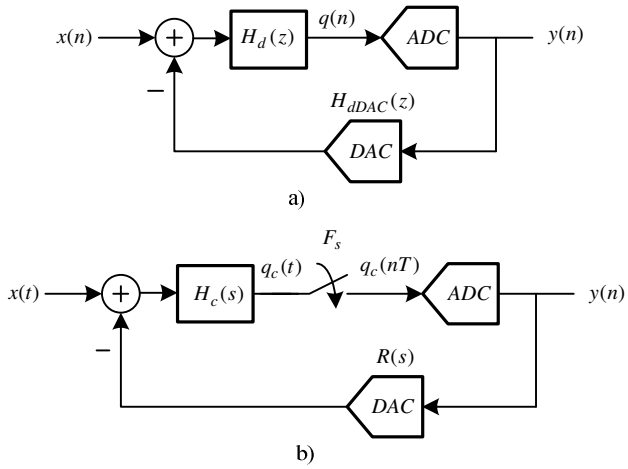


Figure B.1: The block diagrams of a) The DT ΔΣ modulator and b) The CT ΔΣ modulator.

Where $q(n)$ and $q_c(nT)$ are the quantizer inputs of the DT and CT ΔΣ modulators and T is the clock period of the ΔΣ modulators. This condition would be fulfilled if the impulse responses of the open-loop filter of the CT and DT ΔΣ modulators were equal at the sampling times. As a result (1) translates directly into (2):

$$\mathcal{Z}^{-1}\{H_{dDAC}(z)H_d(z)\} = \mathcal{L}^{-1}\{R(s)H_c(s)\}\big|_{t=nT} \tag{2}$$

Because $H_{dDAC}(z) = 1$, equation (2) can be simplified to give (3):

$$\mathcal{Z}^{-1}\{H_d(z)\} = \mathcal{L}^{-1}\{R(s)H_c(s)\}|_{t=nT} \tag{3}$$

The transformation in (3) is the well-known impulse-invariant transformation where $\mathcal{Z}^{-1}$, $\mathcal{L}^{-1}$, $R(s)$, $H_d(z)$ and $H_c(s)$ represent the inverse z-transform, the inverse Laplace transform, the CT DAC transfer function, the DT and the CT loop filters respectively [1][4]. Depending on the output waveform of the CT DAC, there would be an exact mapping between the DT and the CT ΔΣ modulators. The popular feedback-DAC waveforms have rectangular shapes. The time and frequency (Laplace) domain responses of these waveforms are:

$$r_{(\alpha,\beta)}(t) = \begin{cases} 1, & \alpha T \le t \le \beta T, \quad 0 \le \alpha, \beta \le 1 \\ 0, & otherwise \end{cases} \tag{4}$$

$$R(s) = \frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s} \tag{5}$$

In the cases where $\beta > 1$ the DAC equation is divided into two parts as expressed by (6) and the z-domain equivalents of each part is calculated separately.

$$r_{(\alpha,\beta)}(t) = r_{(\alpha,1)}(t) + r_{(0,\beta)}(t - T) \tag{6}$$

In order to derive the equivalent z-domain transfer function of CT ΔΣ modulators with rectangular DAC waveforms, we shall start with the 1st order s-domain term. Equation (7) is derived by substituting (5) and the 1st order s-domain term into (3) as follows.

$$H_{1d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s^2}\right)\Big|_{t=nT}\} \tag{7}$$

An auxiliary variable λ is deployed to derive a general formula step by step. Equation (8) is equal to (7) when $\lambda = 0$:

$$H_{1d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{(s-\lambda)^2}\right)\Big|_{t=nT}\}\Big|_{\lambda=0} = H_1(z)\Big|_{\lambda=0} \tag{8}$$

By using the Laplace transform properties, (8) leads to (9) where $u(t)$ represents a step function:

$$H_1(z) = \mathcal{Z}\left\{e^{\lambda t}(e^{-\alpha\lambda t}(t - \alpha T)u(t - \alpha T) - e^{-\beta\lambda t}(t - \beta T)u(t - \beta T))\big|_{t=nT}\right\} \tag{9}$$

The continuous time variable t in (9) is replaced with nT in (10).

$$H_1(z) = \mathcal{Z}\left\{e^{\lambda nT}(e^{-\alpha\lambda T}(nT - \alpha T)u(nT - \alpha T) - e^{-\beta\lambda T}(nT - \beta T)u(nT - \beta T))\big|_{t=nT}\right\} \tag{10}$$

The z-transform of (10) is expressed by (11) which results in (12).

$$H_1(z) = T\sum_{n=1}^{+\infty} e^{\lambda nT}(e^{-\alpha\lambda T}(n - \alpha) - e^{-\beta\lambda T}(n - \beta))z^{-n} \tag{11}$$

By doing some algebra and using the z-transform conversion, it is shown that equation (11) leads to equation (19) step-by-step through the use of equations (12) to (18) as follows:

$$H_1(z) = T\sum_{n=1}^{+\infty} e^{\lambda nT}\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)n + \left(-\alpha e^{-\alpha\lambda T} + \beta e^{-\beta\lambda T}\right)\right]z^{-n} \tag{12}$$

$$H_1(z) = T\sum_{n=1}^{+\infty} e^{\lambda nT}\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)n\right]z^{-n} + T\sum_{n=0}^{+\infty} e^{\lambda nT}\left[\left(-\alpha e^{-\alpha\lambda T} + \beta e^{-\beta\lambda T}\right)\right]z^{-n} \tag{13}$$

$$H_1(z) = T\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)\left(-z\frac{d}{dz}\left(\frac{e^{\lambda T}}{z - e^{\lambda T}}\right)\right)\right] + T\left[\left(-\alpha e^{-\alpha\lambda T} + \beta e^{-\beta\lambda T}\right)\frac{e^{\lambda T}}{z - e^{\lambda T}}\right] \tag{14}$$

$$H_1(z) = T\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)\frac{e^{\lambda T}z}{(z - e^{\lambda T})^2} + \left(-\alpha e^{-\alpha\lambda T} + \beta e^{-\beta\lambda T}\right)\frac{e^{\lambda T}}{z - e^{\lambda T}}\right] \tag{15}$$

$$H_1(z) = T\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)\frac{e^{\lambda T}\left(z - e^{\lambda T} + e^{\lambda T}\right)}{(z - e^{\lambda T})^2} + \left(-\alpha e^{-\alpha\lambda T} + \beta e^{-\beta\lambda T}\right)\frac{e^{\lambda T}}{z - e^{\lambda T}}\right] \tag{16}$$

$$H_1(z) = T\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)\frac{e^{2\lambda T}}{(z - e^{\lambda T})^2} + \left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)\frac{e^{\lambda T}}{z - e^{\lambda T}} + \left(-\alpha e^{-\alpha\lambda T} + \beta e^{-\beta\lambda T}\right)\frac{e^{\lambda T}}{z - e^{\lambda T}}\right] \tag{17}$$

$$H_1(z) = T\left[\frac{\left(e^{(2-\alpha)\lambda T} - e^{(2-\beta)\lambda T}\right)}{(z - e^{\lambda T})^2} + \frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z - e^{\lambda T}} + \frac{-\alpha e^{(1-\alpha)\lambda T} + \beta e^{(1-\beta)\lambda T}}{z - e^{\lambda T}}\right] \tag{18}$$

$$H_1(z) = T\left[\frac{\left(e^{(2-\alpha)\lambda T} - e^{(2-\beta)\lambda T}\right)}{(z - e^{\lambda T})^2} + \frac{(1-\alpha)e^{(1-\alpha)\lambda T} - (1-\beta)e^{(1-\beta)\lambda T}}{z - e^{\lambda T}}\right] \tag{19}$$

It can be proved that (19) can be obtained by calculating the 1st derivative with respect to the variable λ of equation (20).

$$H_1(z) = \frac{\partial}{\partial\lambda}\left(\frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z - e^{\lambda T}}\right) \tag{20}$$

By substituting $\lambda = 0$ into (19) the z-domain equivalent of the 1st order s-domain term is expressed by (21).

$$H_{1d}(z) = T\left(\frac{\beta - \alpha}{z - 1}\right) \tag{21}$$

The z-domain equivalent of the 2nd order s-domain term is derived by repeating all steps in the process mentioned above as follows.

$$H_{2d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s^3}\right)\Big|_{t=nT}\} \tag{22}$$

An auxiliary variable λ is deployed to derive a general formula step by step. Equation (23) is equal to (22) when $\lambda = 0$:

$$H_{2d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{(s-\lambda)^3}\right)\Big|_{t=nT}\}\Big|_{\lambda=0} = H_2(z)\Big|_{\lambda=0} \tag{23}$$

By using the Laplace transform properties, (23) leads to (24).

$$H_2(z) = \mathcal{Z}\left\{e^{\lambda t}\left(\frac{e^{-\alpha\lambda t}}{2}(t-\alpha T)^2 u(t-\alpha T) - \frac{e^{-\beta\lambda t}}{2}(t-\beta T)^2 u(t-\beta T)\right)\Big|_{t=nT}\right\} \tag{24}$$

The z-transform of (24) is given by (25).

$$H_2(z) = \frac{T^2}{2}\sum_{n=1}^{+\infty} e^{\lambda nT}(e^{-\alpha\lambda T}(n-\alpha)^2 - e^{-\beta\lambda T}(n-\beta)^2)z^{-n} \tag{25}$$

By doing some algebra and using the z-transform conversion, it is shown that equation (25) leads to equation (29) step-by-step through the use of equations (26) to (28) as follows:

$$H_2(z) = \frac{T^2}{2}\sum_{n=1}^{+\infty} e^{\lambda nT}\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)n^2 - 2\left(\alpha e^{-\alpha\lambda T} - \beta e^{-\beta\lambda T}\right)n + \left(\alpha^2 e^{-\alpha\lambda T} - \beta^2 e^{-\beta\lambda T}\right)\right]z^{-n} \tag{26}$$

$$H_2(z) = \frac{T^2}{2}\left[\left(e^{-\alpha\lambda T} - e^{-\beta\lambda T}\right)\left(-z\frac{d}{dz}\left(\frac{ze^{\lambda T}}{(z-e^{\lambda T})^2}\right)\right) - 2\left(\alpha e^{-\alpha\lambda T} - \beta e^{-\beta\lambda T}\right)\left(\frac{ze^{\lambda T}}{(z-e^{\lambda T})^2}\right) + \left(\alpha^2 e^{-\alpha\lambda T} - \beta^2 e^{-\beta\lambda T}\right)\frac{e^{\lambda T}}{z-e^{\lambda T}}\right] \tag{27}$$

$$H_2(z) = \frac{T^2}{2}\left[\left(e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}\right)\left(\frac{z^2 + ze^{\lambda T}}{(z-e^{\lambda T})^2}\right) - 2\left(\alpha e^{-\alpha\lambda T} - \beta e^{-\beta\lambda T}\right)\left(\frac{ze^{\lambda T}}{(z-e^{\lambda T})^2}\right) + \left(\alpha^2 e^{-\alpha\lambda T} - \beta^2 e^{-\beta\lambda T}\right)\frac{e^{\lambda T}}{z-e^{\lambda T}}\right] \tag{28}$$

$$H_2(z) = \frac{T^2}{2}\left\{\frac{(1-\alpha)^2 e^{(1-\alpha)\lambda T} - (1-\beta)^2 e^{(1-\beta)\lambda T}}{(z-e^{\lambda T})} + \frac{(3-2\alpha)e^{(2-\alpha)\lambda T} - (3-2\beta)e^{(2-\beta)\lambda T}}{(z-e^{\lambda T})^2} + \frac{2e^{(3-\alpha)\lambda T} - 2e^{(3-\beta)\lambda T}}{(z-e^{\lambda T})^3}\right\} \quad (29)$$

The 2nd derivative of equation (30) with respect to the variable λ is equal to (29).

$$H_2(z) = \frac{1}{2}\frac{\partial^2}{\partial \lambda^2}\left(\frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z-e^{\lambda T}}\right) \quad (27)$$

Substituting $\lambda = 0$ into (29) gives (31) which is the z-domain equivalent of the 2nd order s-domain term.

$$H_{2d}(z) = T^2\frac{[\beta(\beta-9) - \alpha(\alpha-9)]z + (\beta^2 - \alpha^2)}{2(z-1)^2} \quad (31)$$

Finally, the above-mentioned process is performed all over again for the 3rd and 4th order s-domain terms which are listed in Table B.1. To obtain the kth order s-domain term, the impulse-invariant transformation is written in (32).

$$H_{kd}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha T s} - e^{-\beta T s}}{s^{k+1}}\right)\Big|_{t=nT}\} \quad (32)$$

By utilizing the Laplace transform properties, (32) leads to (33).

$$H_2(z) = \mathcal{Z}\left\{e^{\lambda t}\left(\frac{e^{-\alpha\lambda t}}{k!}(t-\alpha T)^k u(t-\alpha T) - \frac{e^{-\beta\lambda t}}{k!}(t-\beta T)^k u(t-\beta T)\right)\Big|_{t=nT}\right\} \quad (33)$$

The z-domain equivalent for the kth order s-domain function is expressed by (34) where k represents the order of the s-domain term.

$$H_{kd}(z) = \left(\frac{1}{k!}\frac{\partial^k}{\partial \lambda^k}\left(\frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z-e^{\lambda T}}\right)\right)\Big|_{\lambda=0} \quad (34)$$

The z-domain equivalent for the 1st to 4th and the general kth order s-domain terms for a rectangular DAC waveform are presented in Table B.1.

One popular method to compensate the excess loop delay in CT ΔΣ modulators is to deploy negative feedback from the output of the DACs to the input of their quantizers. The z-domain equivalent of this feedback ($H_c(s) = 1$) is developed and given by (36) as follows.

$$H_{0d}(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s}\right)\Big|_{t=nT}\right\} = \sum_{n=0}^{+\infty}(u(nT - \alpha T) - u(nT - \beta T))z^{-n} \tag{35}$$

$$H_{0d}(z) = u(-\alpha T) - u(-\beta T) + (u(T - \alpha T) - u(T - \beta T))z^{-1} \tag{36}$$

One popular rectangular DAC waveform is the NRZ one. The z-domain equivalent of the NRZ DAC with $\alpha = \tau_d$ and $\beta = 1 + \tau_d$ is calculated from (36) and is given by (37).

$$H_{0d}(z) = z^{-1} \tag{37}$$

Table B.1: The CT-to-DT transformation for rectangular DAC waveforms.

s-domain	z-domain equivalent for a rectangular DAC waveform	
	Proposed Formulas	Formulas in [1]
1	$[u(-\alpha T) - u(-\beta T)] + [u(T - \alpha T) - u(T - \beta T)]$	
$\frac{1}{sT}$	$\frac{y_0}{z-1}$ $y_0 = \beta - \alpha$	$\frac{y_0}{z-1}$ $y_0 = \beta - \alpha$
$\frac{1}{s^2T^2}$	$\frac{y_1 z + y_0}{(z-1)^2}$ $y_0 = \frac{1}{2}(\beta^2 - \alpha^2)$ $y_1 = \frac{1}{2}(\beta(2-\beta) - \alpha(2-\alpha))$	$\frac{y_1 z + y_0}{(z-1)^2}$ $y_0 = \frac{1}{2}(\beta^2 - \alpha^2)$ $y_1 = \frac{1}{2}(\beta(1-\beta) - \alpha(1-\alpha))$
$\frac{1}{s^3T^3}$	$\frac{y_2 z^2 + y_1 z + y_0}{(z-1)^3}$ $y_0 = \frac{1}{6}(\beta^3 - \alpha^3)$ $y_1 = -\frac{1}{3}(\beta^3 - \alpha^3) + \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$ $y_2 = +\frac{1}{6}(\beta^3 - \alpha^3) - \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$	$\frac{y_2 z^2 + y_1 z + y_0}{(z-1)^3}$ $y_0 = \frac{1}{6}(\beta^3 - \alpha^3)$ $y_1 = -\frac{1}{3}(\beta^3 - \alpha^3) + \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$ $y_2 = -\frac{1}{6}(\beta^3 - \alpha^3) - \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$
$\frac{1}{s^4T^4}$	$\frac{y_3 z^3 + y_2 z^2 + y_1 z + y_0}{(z-1)^3}$ $y_0 = \frac{1}{24}(\beta^4 - \alpha^4)$ $y_1 = -\frac{1}{8}(\beta^4 - \alpha^4) + \frac{1}{6}(\beta^3 - \alpha^3) + \frac{1}{4}(\beta^2 - \alpha^2) + \frac{1}{6}(\beta - \alpha)$ $y_2 = +\frac{1}{8}(\beta^4 - \alpha^4) - \frac{1}{3}(\beta^3 - \alpha^3) + \frac{2}{3}(\beta - \alpha)$ $y_3 = -\frac{1}{24}(\beta^4 - \alpha^4) + \frac{1}{6}(\beta^3 - \alpha^3) - \frac{1}{4}(\beta^2 - \alpha^2) + \frac{1}{6}(\beta - \alpha)$	$\frac{y_3 z^3 + y_2 z^2 + y_1 z + y_0}{(z-1)^3}$ $y_0 = \frac{1}{24}(\beta^4 - \alpha^4)$ $y_1 = -\frac{1}{8}(\beta^4 - \alpha^4) + \frac{1}{6}(\beta^3 - \alpha^3) + \frac{1}{4}(\beta^2 - \alpha^2) + \frac{1}{6}(\beta - \alpha)$ $y_2 = +\frac{1}{8}(\beta^4 - \alpha^4) - \frac{1}{3}(\beta^3 - \alpha^3) + \frac{2}{3}(\beta - \alpha)$ $y_3 = -\frac{1}{24}(\beta^4 - \alpha^4) + \frac{1}{6}(\beta^3 - \alpha^3) - \frac{1}{4}(\beta^2 - \alpha^2) + \frac{1}{6}(\beta - \alpha)$
$\frac{1}{s^kT^k}$	$\frac{1}{T^k k!}\frac{\partial^k}{\partial \lambda^k}\left(\frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z - e^{\lambda T}}\right)\Big\|_{\lambda=0}$	

The newly derived z-domain equivalent formulas can be compared with the formulas in [1] which both are illustrated in Table B.1. The results of this comparison indicate that y_1 in 2nd-order term and y_2 in 3rd-order

term are entirely different. The comparison can be done between the newly mentioned formulas and the ones presented in [22] which show y_1 in 3rd-order term are not the same. What is surprising is that even z-domain equivalent formulas in [22] and [1] are not identical and y_1 in 2nd-order term and y_1 and y_2 in 3rd-order term are completely different.

B.2 DT to CT Conversion:

In order to find the s-domain equivalent of the z-domain terms, Table B.1 is utilized. The 1st order z-domain term of (38) is converted to the s-domain which is expressed by (39) [1].

$$H_{1d}(z) = \frac{1}{z-1} \tag{38}$$

$$H_{1c}(s) = \frac{k_0}{s} \tag{39}$$

The z-domain equivalent of (39) is given by (40).

$$H_{1d}(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}\left(\left(\frac{k_0}{s}\right)\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s}\right)\Bigg|_{t=nT}\right\} = k_0\frac{\beta-\alpha}{F_s(z-1)} \tag{40}$$

The equation (40) must be equal to (38) to find the k_0 coefficient as follows:

$$k_0\frac{\beta-\alpha}{F_s(z-1)} = \frac{1}{z-1} \quad => \quad k_0 = \frac{F_s}{\beta-\alpha} \tag{41}$$

Where F_s represents the sampling frequency of the modulator. The 2nd order z-domain term of (42) has the s-domain term similar to what is expressed by (43) [1].

$$H_{2d}(z) = \frac{1}{(z-1)^2} \tag{42}$$

$$H_{2c}(s) = \frac{k_1 s + k_0}{s^2} = \frac{k_1}{s} + \frac{k_0}{s^2} \tag{43}$$

The z-domain equivalent of (43) is found once again by using Table B.1.

$$H_{2d}(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}\left(\left(\frac{k_1}{s}+\frac{k_0}{s^2}\right)\frac{e^{-\alpha Ts}-e^{-\beta Ts}}{s}\right)\Bigg|_{t=nT}\right\} \tag{44}$$

$$= \frac{k_1 T(\beta-\alpha)}{z-1} + \frac{k_0 T^2\left[\big(\beta(2-\beta)-\alpha(2-\alpha)\big)z+(\beta^2-\alpha^2)\right]}{2(z-1)^2}$$

The equation (44) must be equal to (42) in order to find the k_1 and k_0 coefficients as follows:

$$\frac{k_1 T(\beta-\alpha)}{z-1} + \frac{k_0 T^2\left[\big(\beta(2-\beta)-\alpha(2-\alpha)\big)z+(\beta^2-\alpha^2)\right]}{2(z-1)^2} = \frac{1}{(z-1)^2} \tag{41}$$

$$\Rightarrow \begin{cases} k_0 = \dfrac{{F_s}^2}{\beta-\alpha} \\ k_1 = \dfrac{F_2}{2}\dfrac{\alpha+\beta-2}{\beta-\alpha} \end{cases}$$

Similarly all the above-mentioned steps are performed again for the 3rd and 4th z-domain terms and their s-domain equivalents are listed in Table B.2 [1][22].

Table B.2: The DT-to-CT transformation for rectangular DAC waveforms [1].

z-domain	*s-domain equivalent for a rectangular DAC waveform*
$\frac{1}{z-1}$	$\frac{k_0}{s}$ $\quad k_0 = \frac{F_s}{\beta-\alpha}$
$\frac{1}{(z-1)^2}$	$\frac{k_1 s + k_0}{s^2}$ $\quad k_0 = \frac{{F_s}^2}{\beta-\alpha}$ $\quad k_1 = \frac{F_s}{2}\frac{\alpha+\beta-2}{\beta-\alpha}$
$\frac{1}{(z-1)^3}$	$\frac{k_2 s^2 + k_1 s + k_0}{s^3}$ $\quad k_0 = \frac{{F_s}^3}{\beta-\alpha}$ $\quad k_1 = \frac{{F_s}^2}{2}\frac{\alpha+\beta-3}{\beta-\alpha}$ $k_2 = \frac{F_s}{12}\frac{\beta(\beta-9)+\alpha(\alpha-9)+4\alpha\beta+12}{\beta-\alpha}$
$\frac{1}{(z-1)^4}$	$\frac{k_3 s^3 + k_2 s^2 + k_1 s + k_0}{s^4}$ $\quad k_0 = \frac{{F_s}^4}{\beta-\alpha}$ $\quad k_1 = \frac{{F_s}^3}{2}\frac{\alpha+\beta-4}{\beta-\alpha}$ $k_2 = \frac{{F_s}^2}{12}\frac{\beta(\beta-12)+\alpha(\alpha-12)+4\alpha\beta+22}{\beta-\alpha}$ $k_3 = \frac{F_s}{12}\frac{\beta^2(\alpha-2)+\alpha^2(\beta-2)+11(\alpha+\beta)-8\alpha\beta-12}{\beta-\alpha}$

Appendix C: Layout

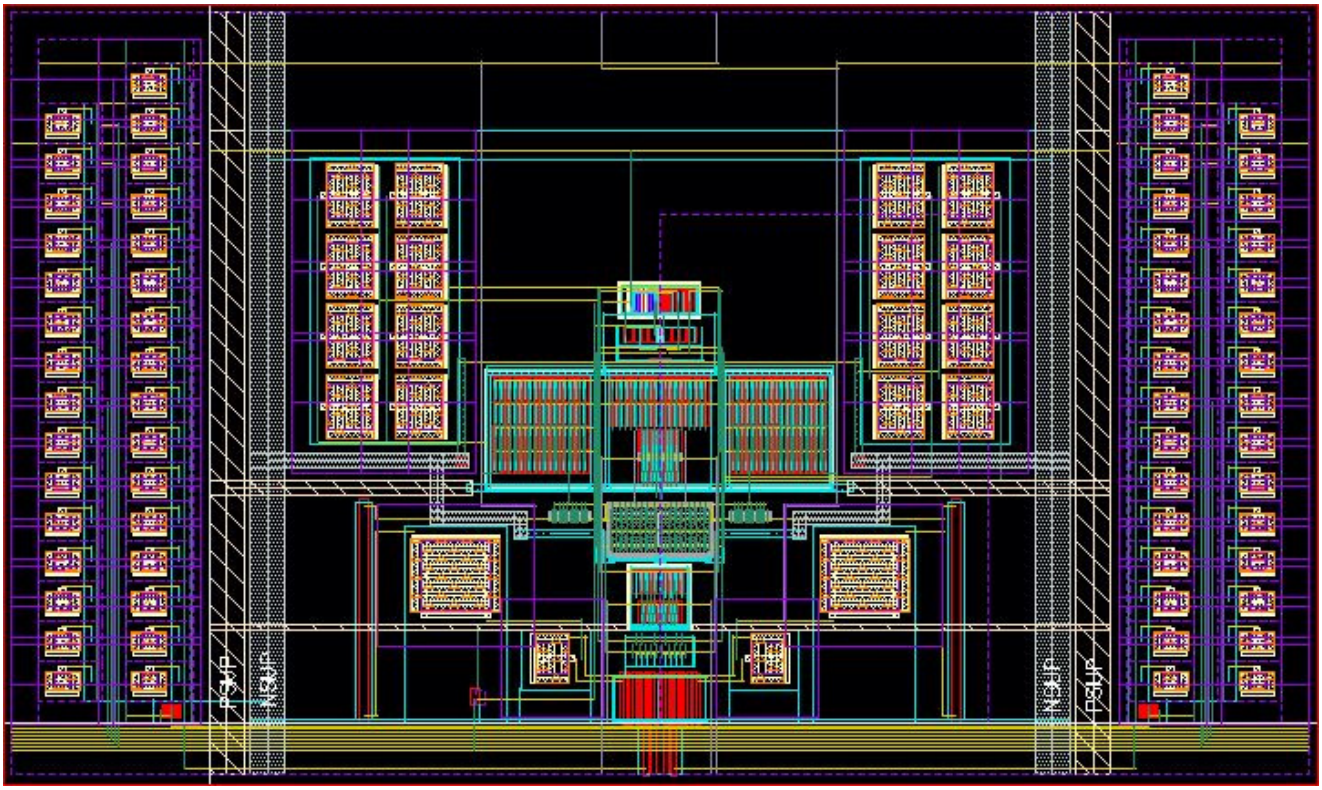


Figure C.1: The Layout of the first integrator.

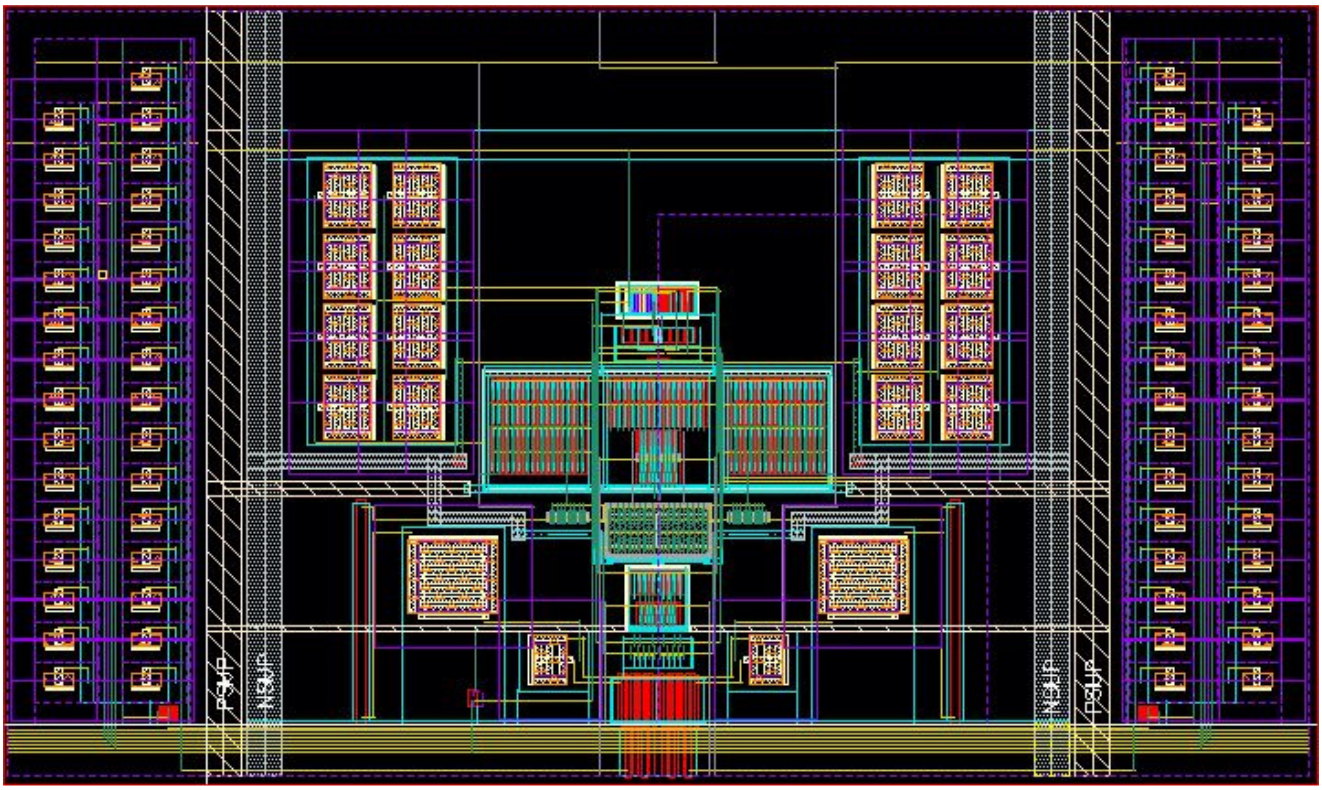


Figure C.2: The Layout of the second integrator.

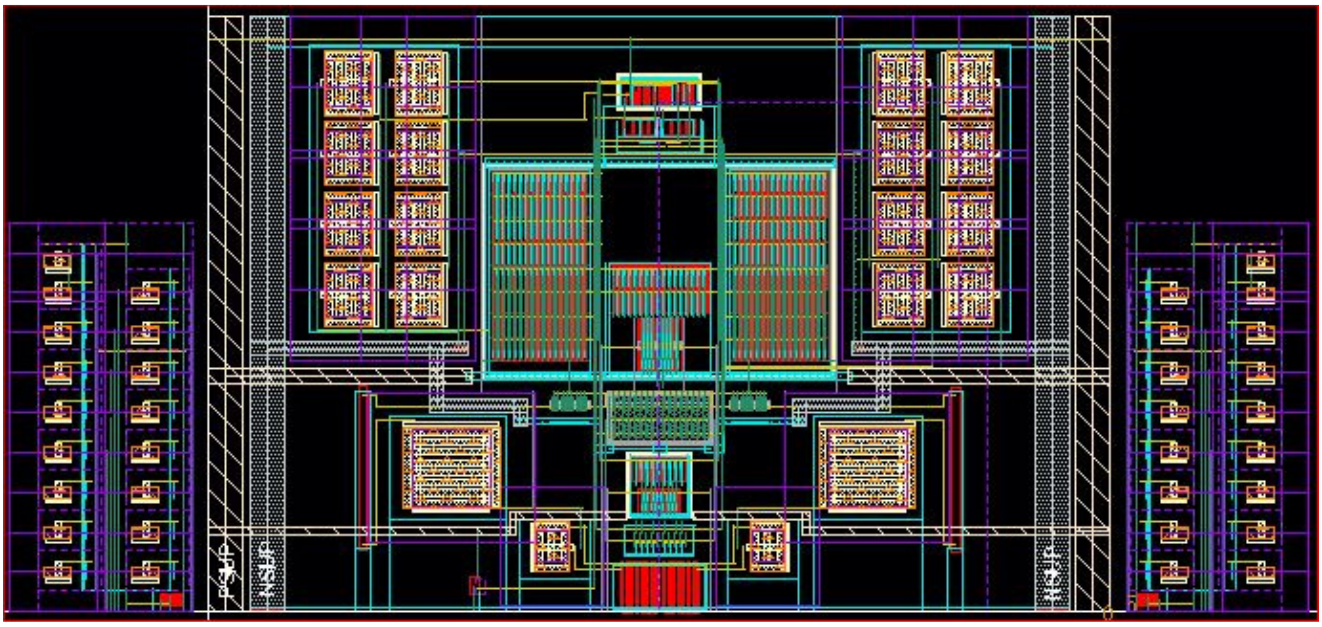


Figure C.3: The Layout of the third integrator.

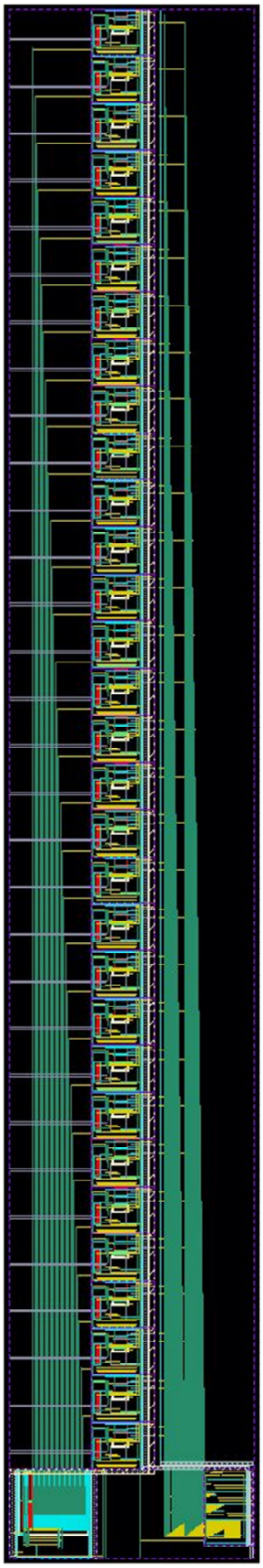


Figure C.4: The Layout of the ADC1.

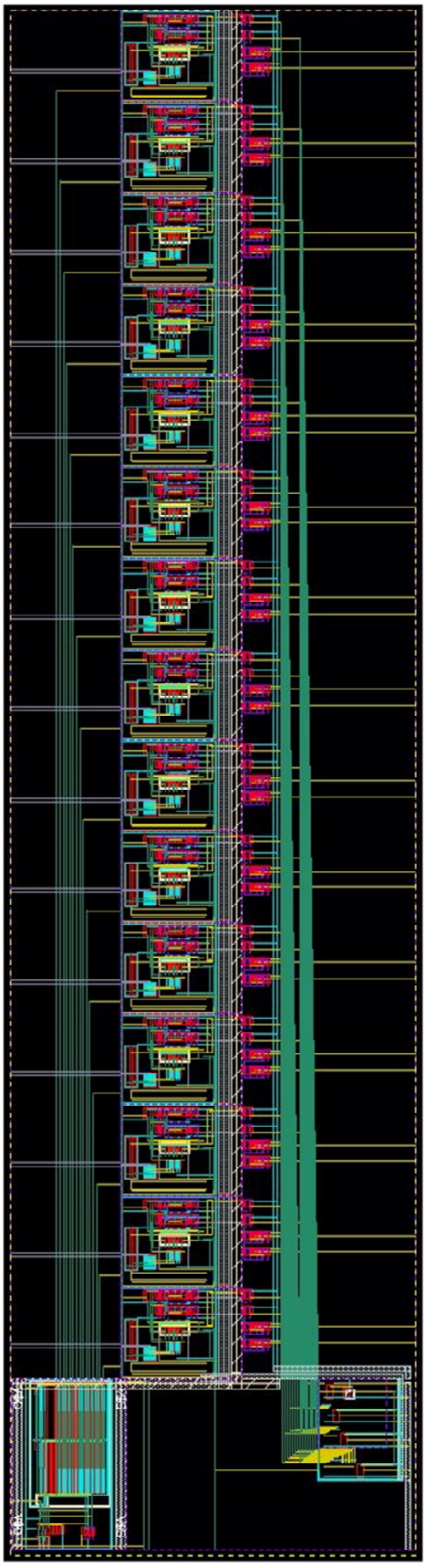


Figure C.5: The Layout of the ADC2.

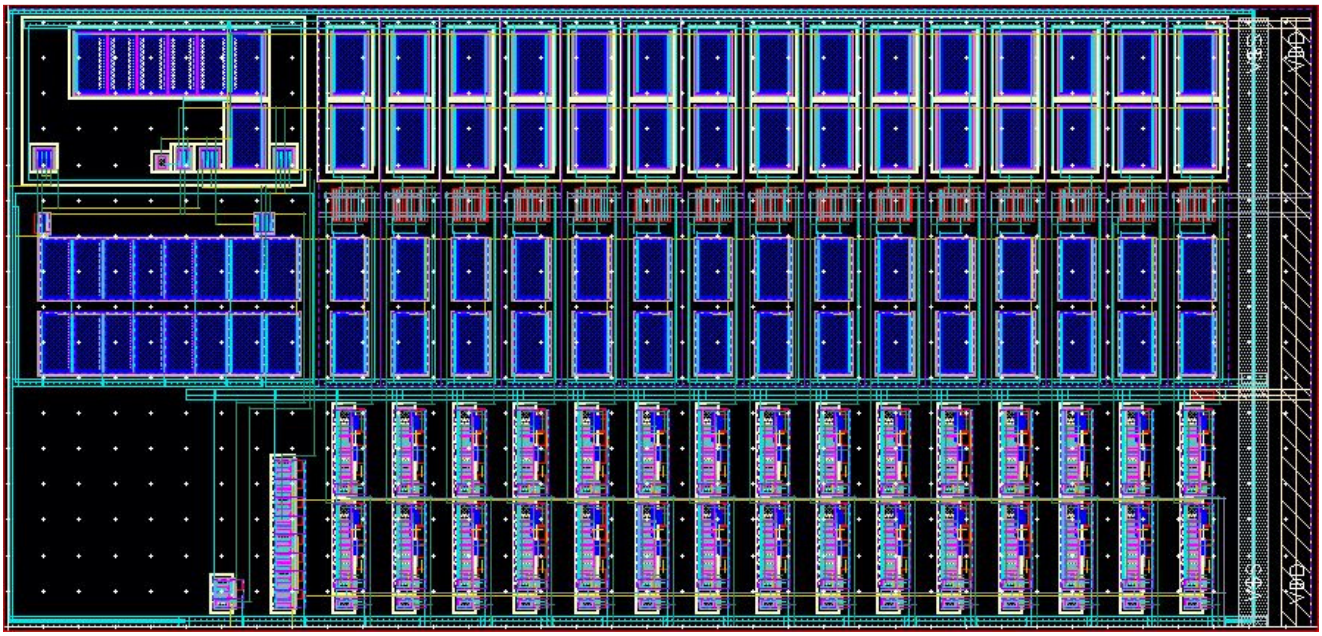


Figure C.6: The Layout of the DAC1.

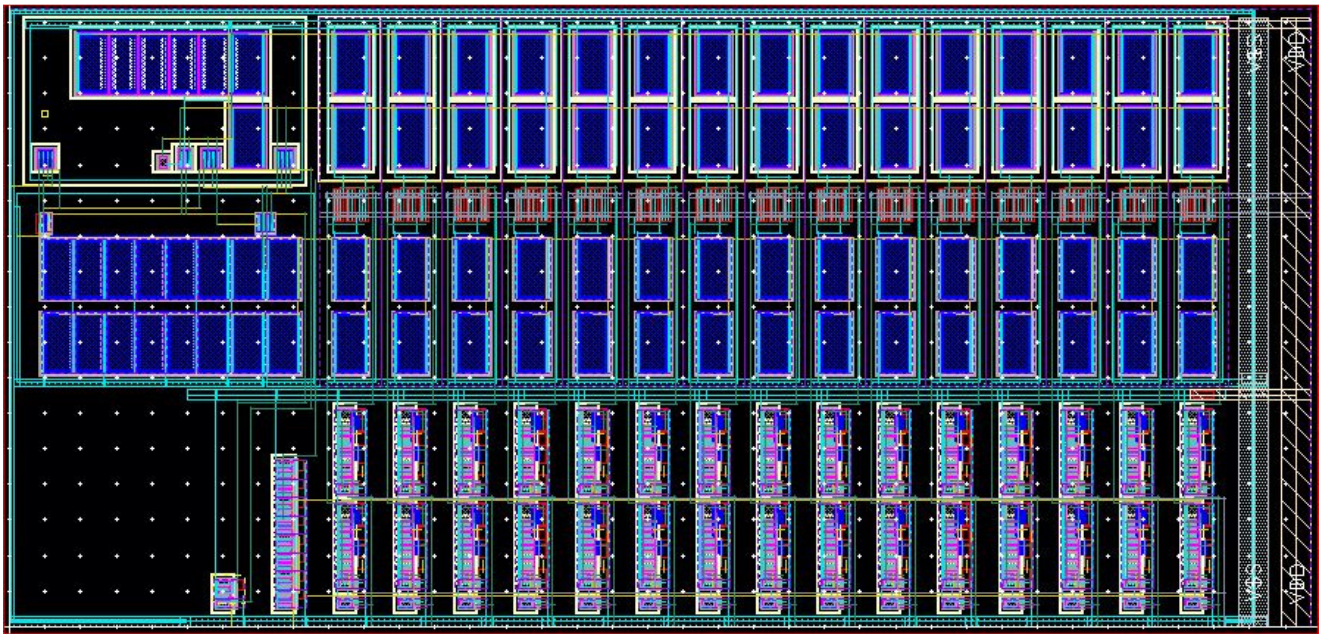


Figure C.7: The Layout of the DAC2.

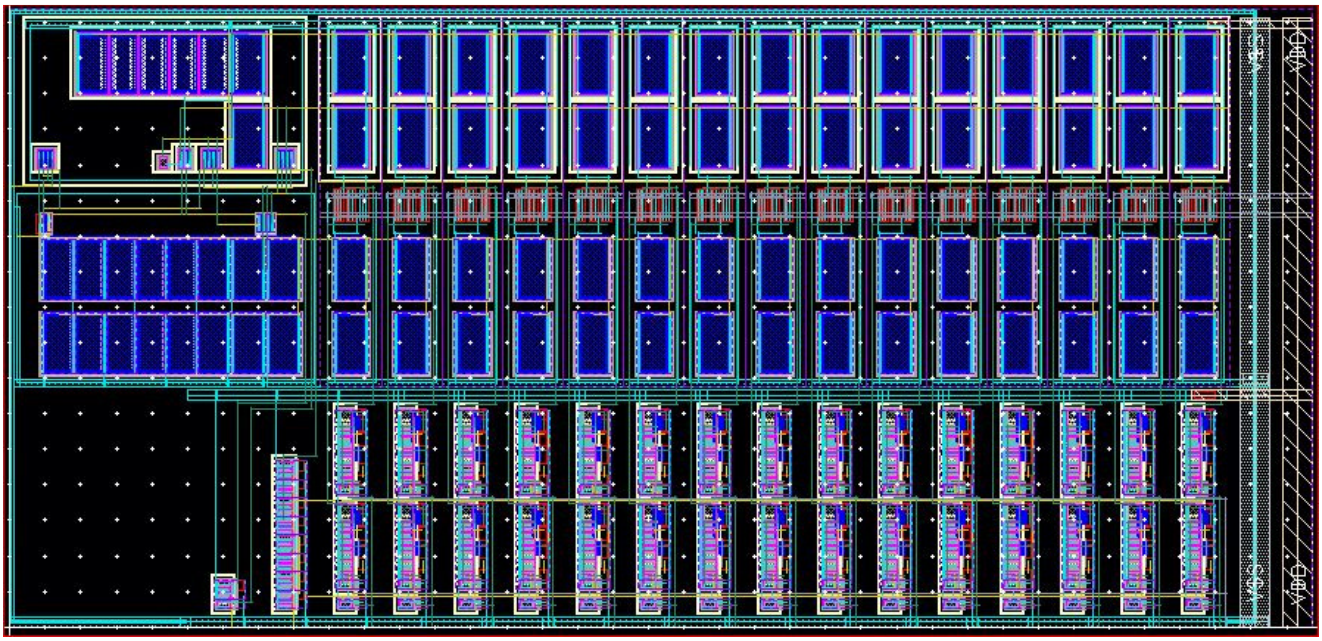


Figure C.8: The Layout of the DAC3.

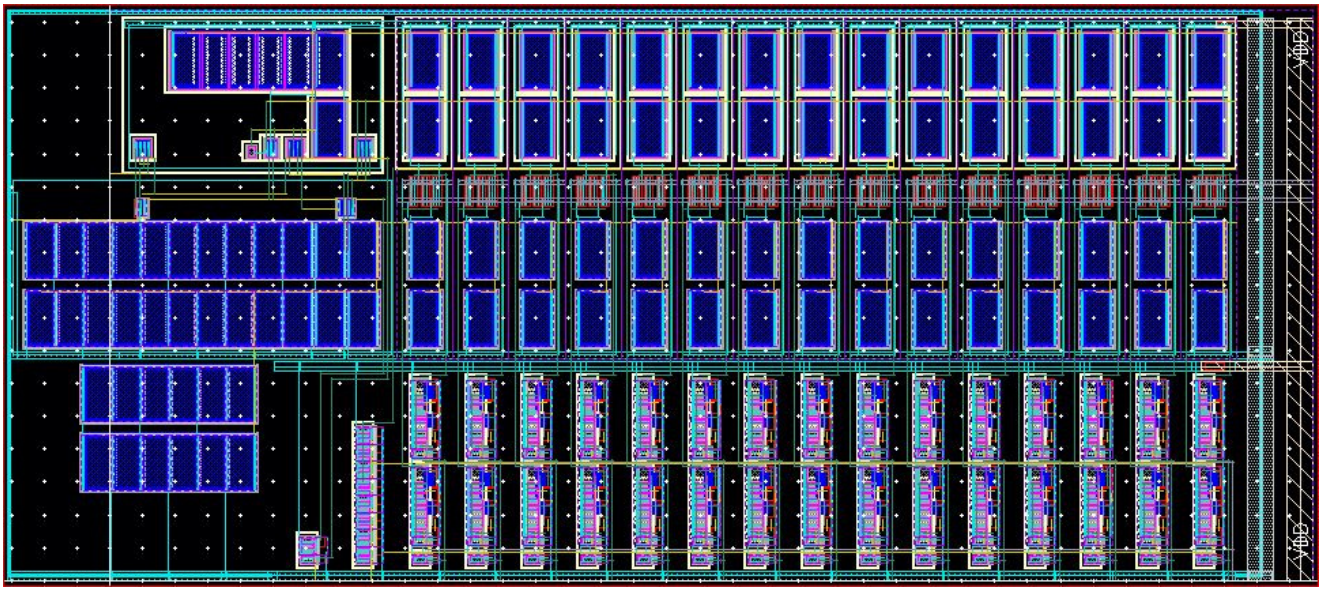


Figure C.9: The Layout of the DAC4.

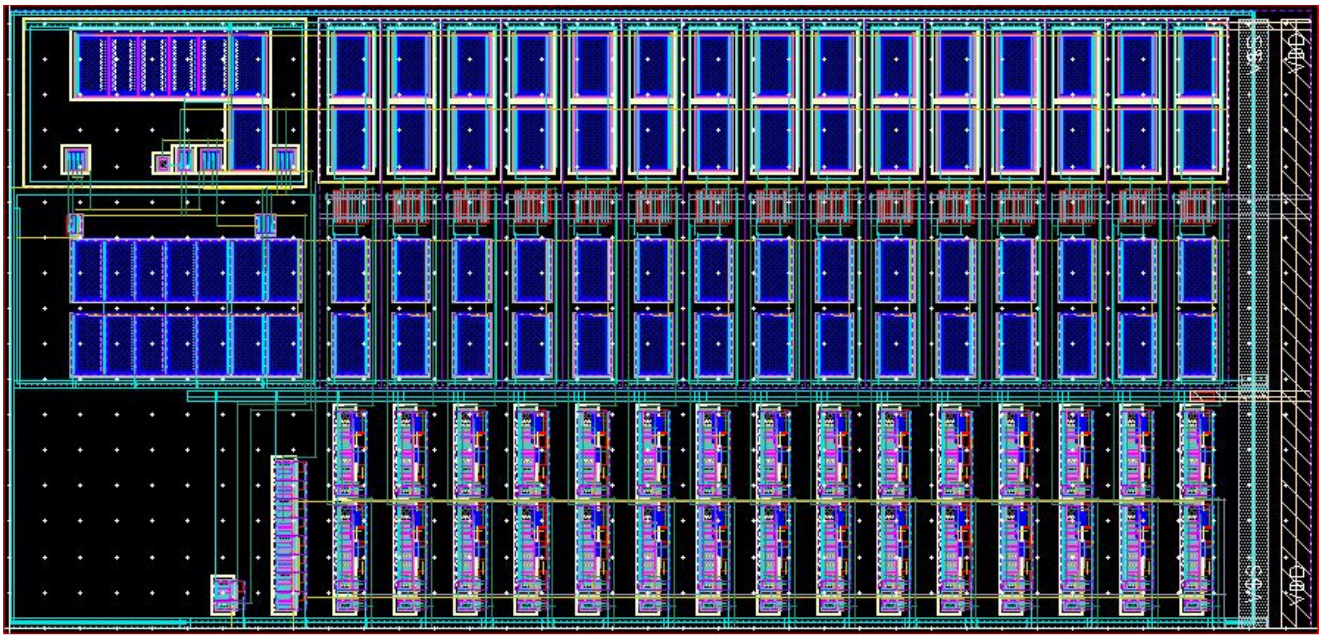


Figure C.10: The Layout of the DAC5.

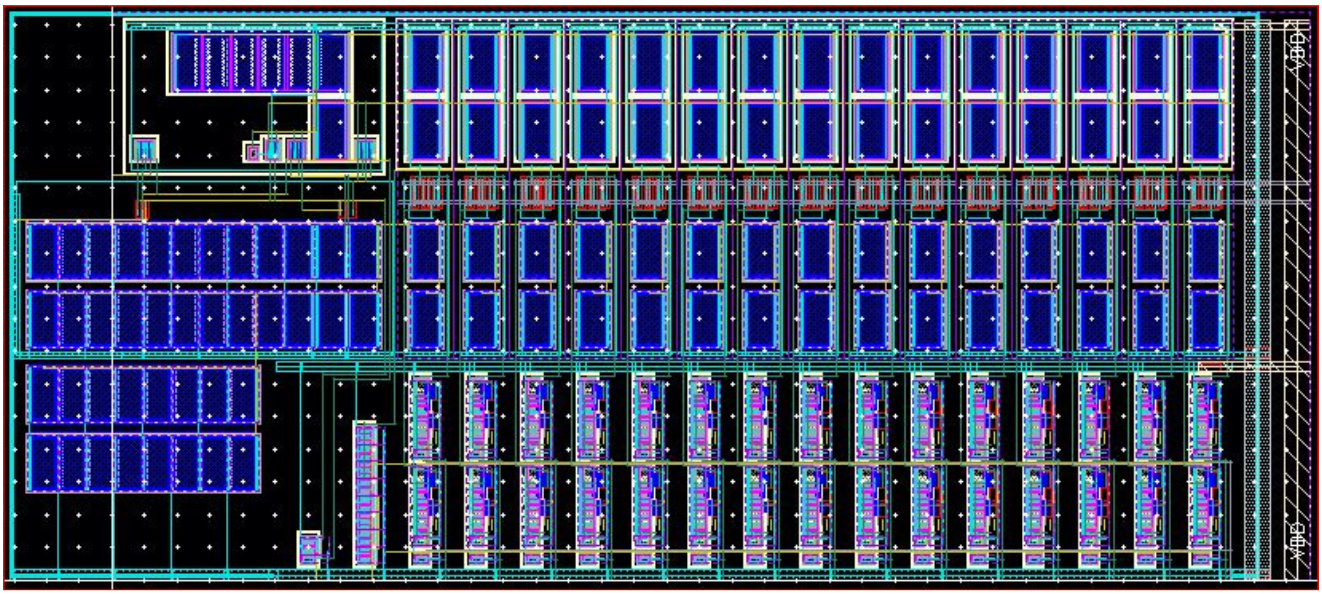


Figure C.11: The Layout of the DAC6.

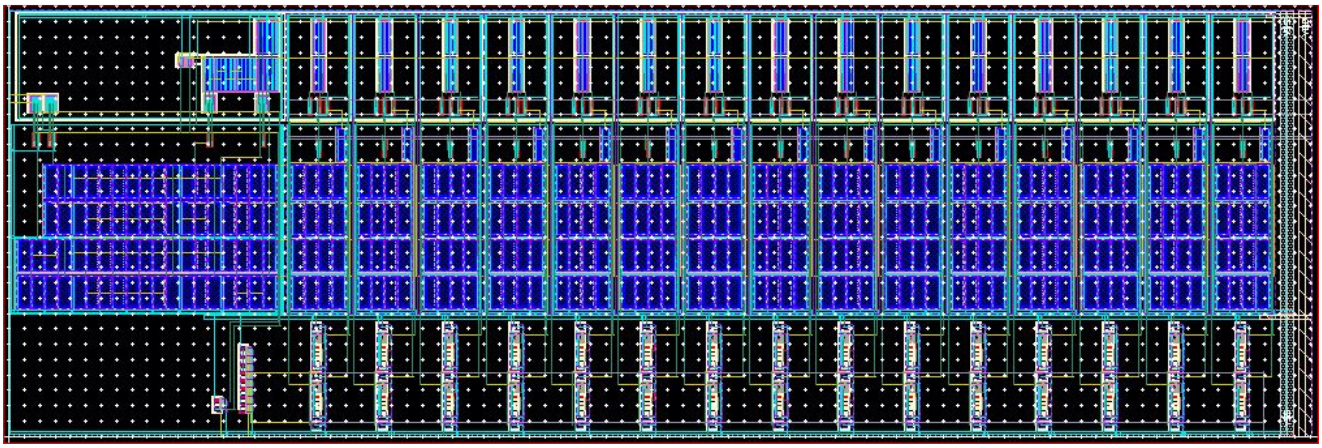


Figure C.12: The Layout of the DAC7.

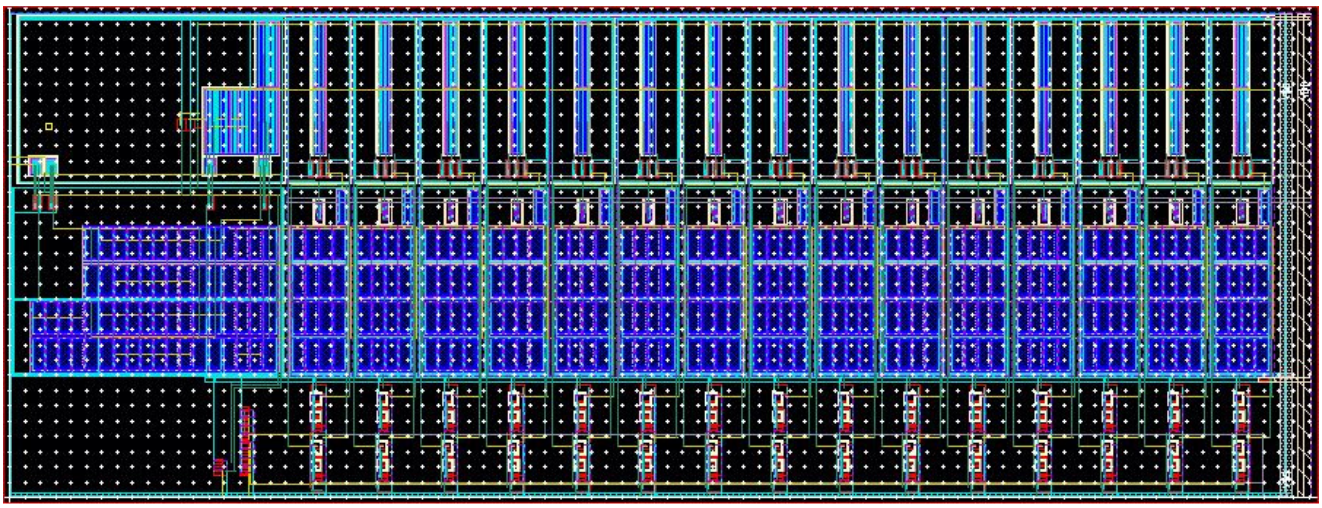


Figure C.13: The Layout of the DAC8.

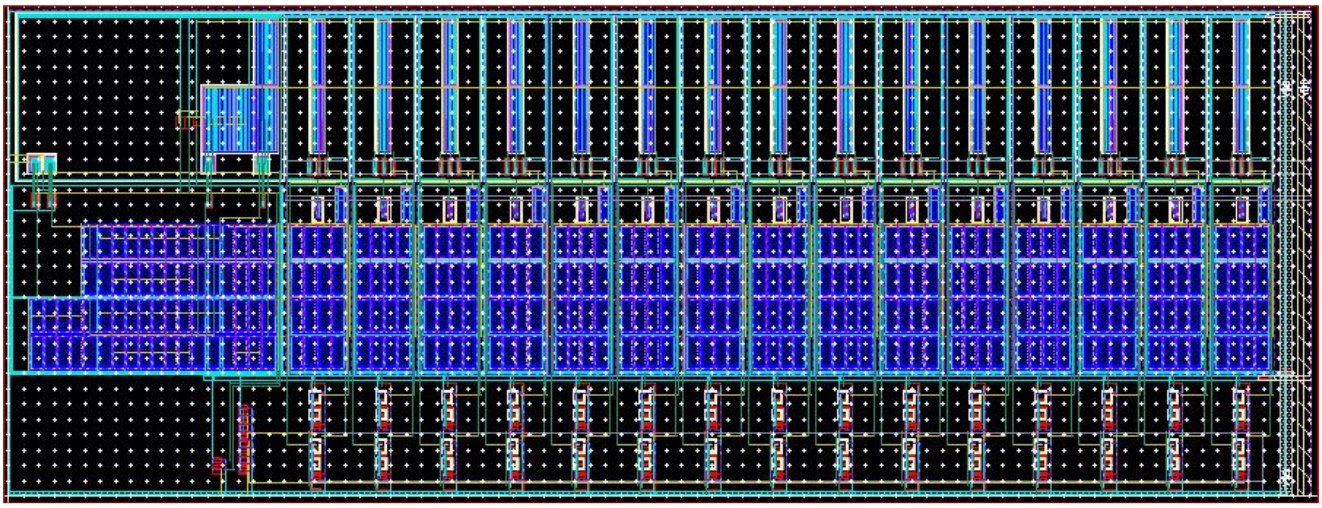


Figure C.14: The Layout of the DAC9.

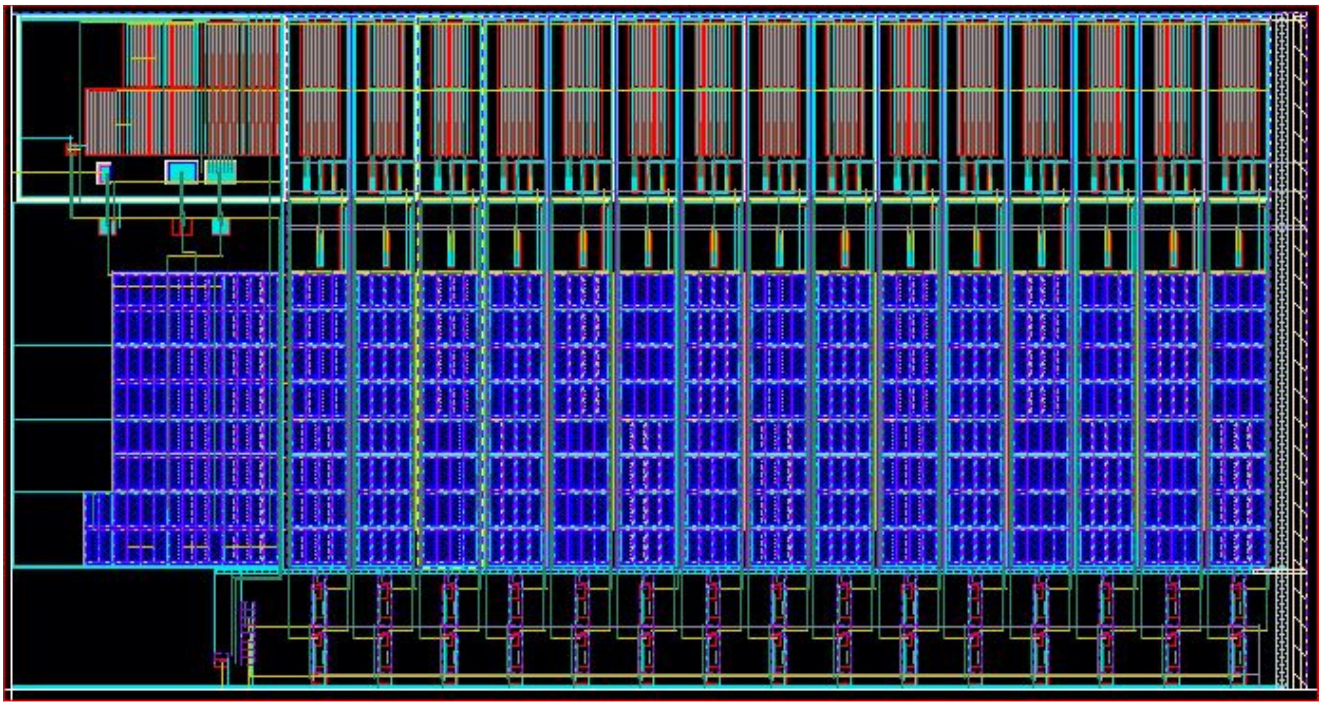


Figure C.15: The Layout of the DAC10.

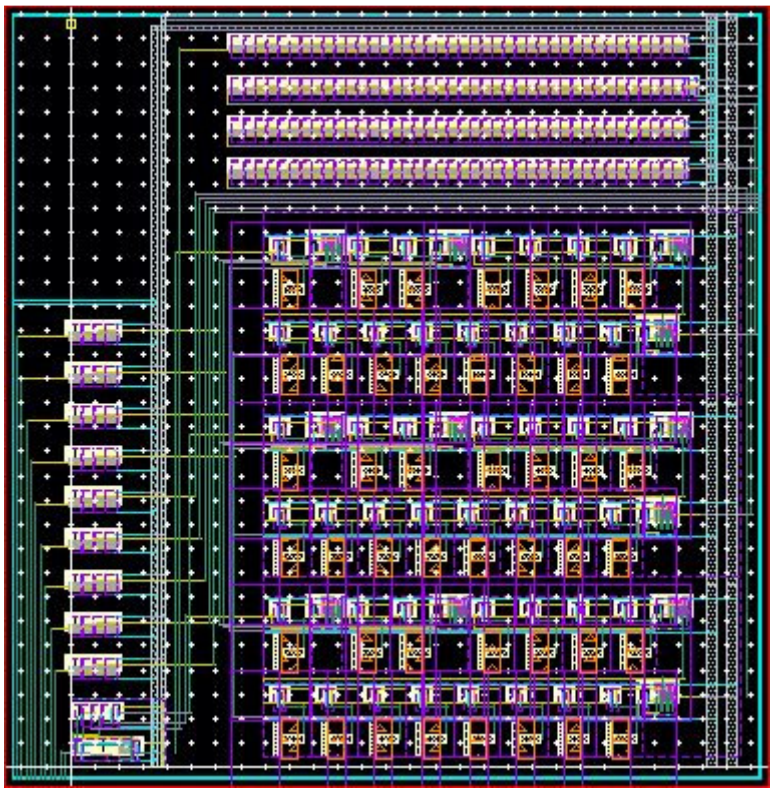


Figure C.16: The Layout of the clock generator and buffer.

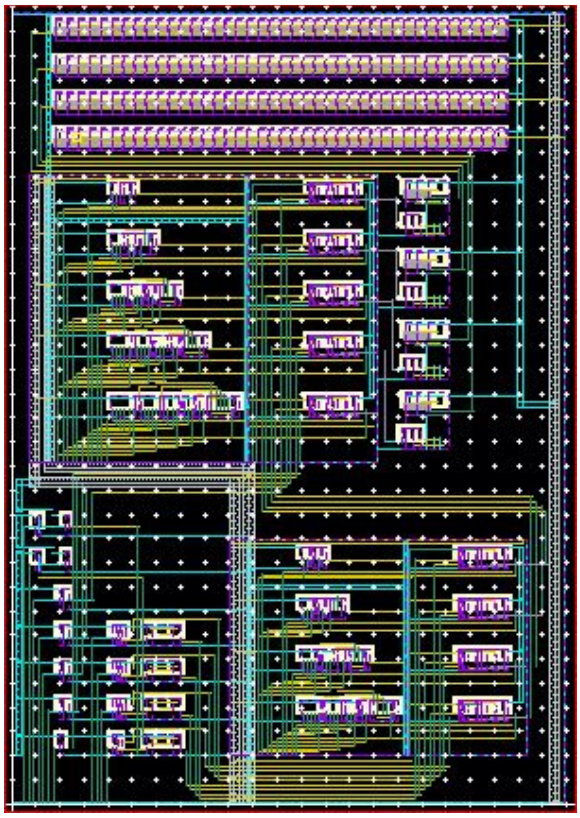


Figure C.17: The Layout of the digital block.

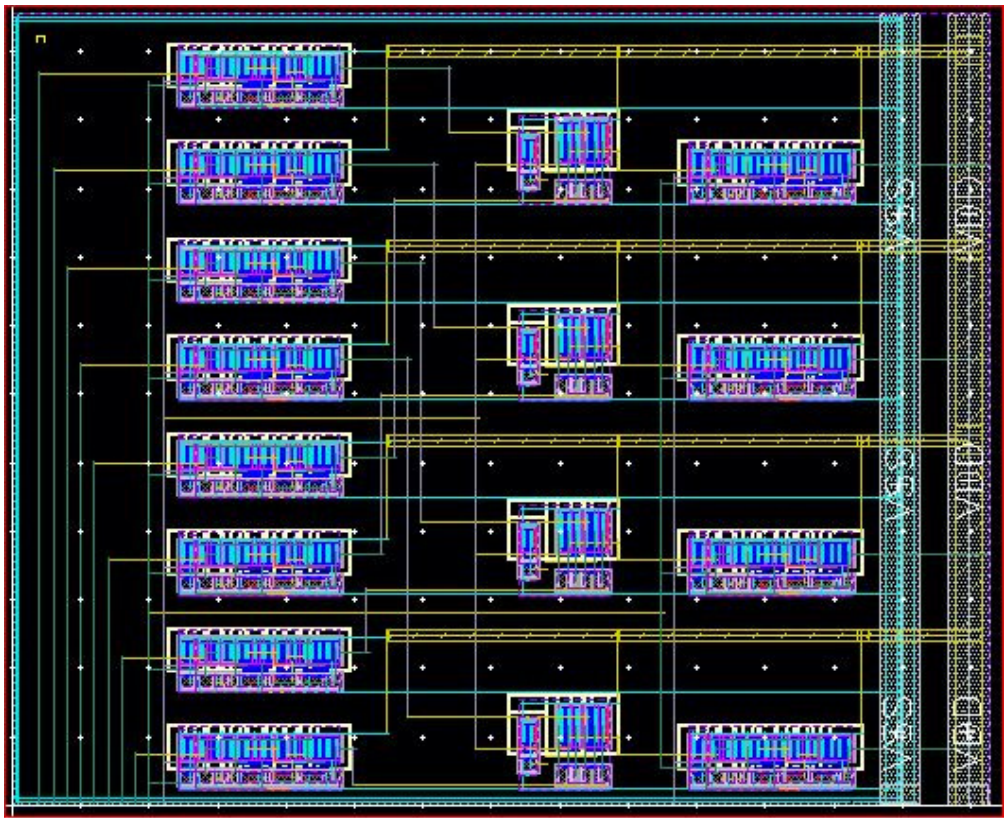


Figure C.18: The Layout of the multiplexer.

Appendix D: MATLAB Files and Simulink Models

The following MATLAB file is used to simulate the 3rd-order CTTI ΔΣ modulator. It calls a Simulink file which has been shown in Figure 4.1 and 4.2 and assigns all the modulator parameters into it then it plots the output spectrum and measures SNDR of the modulator.

```
clear all;
clc;
close all;
format long;

% H = synthesizeNTF(3,8,0,3.037855262,0);
% H = synthesizeChebyshevNTF(3,8,0,2.83321215,0);
% H = synthesizeChebyshevNTF(3,8,0,4,0);
% [num1,den1]=tfdata(H,'v');

num1=[1    -3     3    -1];
den1=[1  -0.999999999272257   0.527864044503167  -0.105572808885268];
c=den1(2)+3
b=(den1(3)+2*c-3)/c
a=(den1(4)+b*c-c+1)/(b*c)

c=2;

Fs=1;
OSR=16;
Fb=Fs/(2*OSR);
N=2^15;
Nb=floor((N*Fb)/Fs);
ain=0.7;
Ni=1001;
Fin=(Ni/(N))*Fs;
k=1;
g=3.9e-3;
B=0.125;
td_norm=0.5;
m1=1-td_norm;
m=m1;

fc1 = 1;
fc2 = 1;
fc3 = 1+a*(1-2*m);
fc4 = 1+a*(2-2*m);
fc5 = a*b*(2*m^2-m-(1/6))  +b*(1-2*m)+1;
fc6 = a*b*(2*m^2-3*m+(5/6))+b*(2-2*m)+1;
fc7 = a*b*c*(-(2/3)*m^3+(1/2)*m^2+(1/6)*m)+b*c*(m^2-m)+c*(1-m);
fc8 = a*b*c*(-(2/3)*m^3+(3/2)*m^2-(5/6)*m)+b*c*(m^2-2*m+1)+c*(1-m);
fc9 = a*b*c*(-(2/3)*m^3+(3/2)*m^2-(5/6)*m)+b*c*(m^2-2*m+1)+c*(1-m);
fc10= a*b*c*(-(2/3)*m^3+(5/2)*m^2-(17/6)*m+1)+b*c*(m^2-3*m+2)+c*(1-m);

fc=[fc1 fc2 fc3 fc4 fc5 fc6 fc7 fc8 fc9 fc10]
```

```
if td_norm==0
    td=0; % used in the delay block inside the simulink file
else
    td=1;
end;

sim('TI2CT3NRZ_original_scl_2');
L=length(y);
out=y(L-2*N:L);

[out,OUT] = myFFT(out,hann(2*N+1)',2*N+1,16,2*N);
snr    = calculateSNR1(OUT(3:2*Nb+1)')
q=dbv(OUT);
q=q-q(Ni+1);

figure(1)
f=0:10e6/(2*Nb):10e6;
semilogx(f,q(1:2*Nb+1))
legend('CTTI DS with ELD compensation') %,'my method DT','my method CT 1','my
method CT 2' )
xlabel('Frequency')
ylabel('output spectrum')

[max(abs(y1s)) max(abs(y2))]
```

```
function [x,X] = myFFT(x,Window,N,nlev,nfft)
if length(x)>N,
x      = x(end-N+1:end);
end
X      = fft(x.*Window',nfft)/(N*(nlev/2)/4);
```

```
% A 16-level quantizer with 15 comparators

function out = quan4bit(vi)

vref=1;
LSB=2*vref/16;

%inserting random offset
o2=zeros(1,15);

% Digitize input
if       vi>= +7*LSB+o2(15)                                , y=+7;
elseif   vi>= +6*LSB+o2(14) &  vi<  +7*LSB+o2(15)  , y=+6;
elseif   vi>= +5*LSB+o2(13) &  vi<  +6*LSB+o2(14)  , y=+5;
elseif   vi>= +4*LSB+o2(12) &  vi<  +5*LSB+o2(13)  , y=+4;
elseif   vi>= +3*LSB+o2(11) &  vi<  +4*LSB+o2(12)  , y=+3;
elseif   vi>= +2*LSB+o2(10) &  vi<  +3*LSB+o2(11)  , y=+2;
elseif   vi>= +1*LSB+o2(9)  &  vi<  +2*LSB+o2(10)  , y=+1;
elseif   vi>=  0*LSB+o2(8)  &  vi<  +1*LSB+o2(9)   , y= 0;
elseif   vi>= -1*LSB+o2(7)  &  vi<   0*LSB+o2(8)   , y=-1;
elseif   vi>= -2*LSB+o2(6)  &  vi<  -1*LSB+o2(7)   , y=-2;
elseif   vi>= -3*LSB+o2(5)  &  vi<  -2*LSB+o2(6)   , y=-3;
```

```
elseif   vi>= -4*LSB+o2(4)  &  vi<  -3*LSB+o2(5)   , y=-4;
elseif   vi>= -5*LSB+o2(3)  &  vi<  -4*LSB+o2(4)   , y=-5;
elseif   vi>= -6*LSB+o2(2)  &  vi<  -5*LSB+o2(3)   , y=-6;
elseif   vi>= -7*LSB+o2(1)  &  vi<  -6*LSB+o2(2)   , y=-7;
else     y=-8;
end;
out=y;
```

```
% A 32-level quantizer with 31 comparators

function out = quan5bit(vi)

vref=1;
LSB=2*vref/32;

%inserting random offset
o1=zeros(1,31);

% Digitize input
if       vi>= +15*LSB+o1(31)                          , y=+15;
elseif   vi>= +14*LSB+o1(30) &  vi< +15*LSB+o1(31)   , y=+14;
elseif   vi>= +13*LSB+o1(29) &  vi< +14*LSB+o1(30)   , y=+13;
elseif   vi>= +12*LSB+o1(28) &  vi< +13*LSB+o1(29)   , y=+12;
elseif   vi>= +11*LSB+o1(27) &  vi< +12*LSB+o1(28)   , y=+11;
elseif   vi>= +10*LSB+o1(26) &  vi< +11*LSB+o1(27)   , y=+10;
elseif   vi>= +9 *LSB+o1(25) &  vi< +10*LSB+o1(26)   , y=+9;
elseif   vi>= +8 *LSB+o1(24) &  vi< +9 *LSB+o1(25)   , y=+8;
elseif   vi>= +7 *LSB+o1(23) &  vi< +8 *LSB+o1(24)   , y=+7;
elseif   vi>= +6 *LSB+o1(22) &  vi< +7 *LSB+o1(23)   , y=+6;
elseif   vi>= +5 *LSB+o1(21) &  vi< +6 *LSB+o1(22)   , y=+5;
elseif   vi>= +4 *LSB+o1(20) &  vi< +5 *LSB+o1(21)   , y=+4;
elseif   vi>= +3 *LSB+o1(19) &  vi< +4 *LSB+o1(20)   , y=+3;
elseif   vi>= +2 *LSB+o1(18) &  vi< +3 *LSB+o1(19)   , y=+2;
elseif   vi>= +1 *LSB+o1(17) &  vi< +2 *LSB+o1(18)   , y=+1;
elseif   vi>=  0 *LSB+o1(16) &  vi< +1 *LSB+o1(17)   , y= 0;
elseif   vi>= -1 *LSB+o1(15) &  vi<  0 *LSB+o1(16)   , y=-1;
elseif   vi>= -2 *LSB+o1(14) &  vi< -1 *LSB+o1(15)   , y=-2;
elseif   vi>= -3 *LSB+o1(13) &  vi< -2 *LSB+o1(14)   , y=-3;
elseif   vi>= -4 *LSB+o1(12) &  vi< -3 *LSB+o1(13)   , y=-4;
elseif   vi>= -5 *LSB+o1(11) &  vi< -4 *LSB+o1(12)   , y=-5;
elseif   vi>= -6 *LSB+o1(10) &  vi< -5 *LSB+o1(11)   , y=-6;
elseif   vi>= -7 *LSB+o1(9)  &  vi< -6 *LSB+o1(10)   , y=-7;
elseif   vi>= -8 *LSB+o1(8)  &  vi< -7 *LSB+o1(9)    , y=-8;
elseif   vi>= -9 *LSB+o1(7)  &  vi< -8 *LSB+o1(8)    , y=-9;
elseif   vi>= -10*LSB+o1(6)  &  vi< -9 *LSB+o1(7)    , y=-10;
elseif   vi>= -11*LSB+o1(5)  &  vi< -10*LSB+o1(6)    , y=-11;
elseif   vi>= -12*LSB+o1(4)  &  vi< -11*LSB+o1(5)    , y=-12;
elseif   vi>= -13*LSB+o1(3)  &  vi< -12*LSB+o1(4)    , y=-13;
elseif   vi>= -14*LSB+o1(2)  &  vi< -13*LSB+o1(3)    , y=-14;
elseif   vi>= -15*LSB+o1(1)  &  vi< -14*LSB+o1(2)    , y=-15;
else     y=-16;
end;
out=y;
```

```
% A 16-level dac

function out = dac4bit(in)

vref=1;
LSB=2*vref/15;
out=(in+0.5)*LSB;
```

```
function [X] = dbv(x)

X=20*log10(abs(x));
```

```
function [snr] = calculateSNR1(X)

N=length(X);
q=abs(X);
[s,j]=max(q);
n=norm([q(1:j-4),q(j+4:N)]);
snr=20*log10(s/n);
```

REFERENCES

[1] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*. Berlin: Springer, 2006.

[2] Y. Zhang and A. Leuciuc," A 1.8V Continuous-Time Delta-Sigma Modulator with 2.5MHz Bandwidth," *IEEE MWSCAS,* pp. 140-143, 2002.

[3] A. Tabatabaei *et al.*, "A dual channel ΣΔ ADC with 40MHz aggregate signal bandwidth," *IEEE ISSCC, vol.1,* pp. 66–67, Feb. 2003.

[4] L. J. Breems *et al.*, "A cascaded continuous-time ΣΔ modulator with 67-dB dynamic range in 10MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2152–2160, Dec. 2004.

[5] P. Balmelli and Q. Huang, "A 25-MS/s 14-b 200mW ΣΔ modulator in 0.18- um CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2161–2169, Dec. 2004.

[6] S. Paton *et al.*,"A 70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11 Bits of resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1063, Jul. 2004.

[7] T. C. Caldwell and D. A. Johns," A Time-Interleaved Continuous-Time ΔΣ Modulator with 20-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits,* vol. 41, no. 7, pp. 1578-1588, July 2006.

[8] S. Ouzounov "A 1.2V 121-Mode CT ΣΔ Modulator for Wireless Receivers in 90nm CMOS" *IEEE ISSCC,* pp. 242–243, Feb. 2007.

[9] M. Z. Straayer "A 12-Bit, 10-MHz Bandwidth, Continuous-Time ΔΣ ADC with a 5-Bit, 950-MS/s VCO-Based Quantizer" *IEEE J. Solid-State Circuits*, vol.43, no.4*,* pp. 805-814 April *2008*.

[10] R. Schoofs "A Design-Optimized Continuous-Time Delta–Sigma ADC for WLAN Applications" *IEEE Trans. Circuits Syst. II*, vol. 54, no. 1, pp. 209–217, Jan. 2007.

[11] G. Mitteregger "A 20-mW 640-MHz CMOS Continuous-Time ΔΣ ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB" *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, Dec. 2006.

[12] J. Arias “A 32-mW 320-MHz Continuous-Time Complex Delta-Sigma ADC for Multi-Mode Wireless-LAN Receivers” *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 339–351, Feb. 2006.

[13] T. Wang, “Analysis and Design of a Continuous-Time Sigma-Delta Modulator with 20MHz Signal Bandwidth, 53.6dB Dynamic Range and 51.4dB SNDR” *IEEE International Symposium on Electronic Design, Test & Applications,* pp. 79-84, Jan. 2008.

[14] L. J. Breems, “A 56 mW Continuous-Time Quadrature Cascaded ΣΔ Modulator with 77dB DR in a Near Zero-IF 20 MHz Band” *IEEE J. Solid-State Circuits*, vol.42, no.12, pp. 2696-2705, Dec. 2007.

[15] M. Park and M. H. Perrott, “A 78dB SNDR 87mW 20MHz Bandwidth Continuous-Time ΣΔ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 um CMOS” *IEEE J. Solid-State Circuits*, vol.44, no.12, pp. 3344-3358, Dec. 2009.

[16] K. C. Hong and H. Chiueh, “A 36-mW Continuous-Time Sigma-Delta Modulator with 74db Dynamic Range and 10-MHz Bandwidth” *VLSI System on Chip IEEE Conference*, pp. 392-395, Sept. 2010.

[17] G. Jing, T. Mingqiang and L. Tao, “A 14-bit 5MHz continuous-time sigma-delta ADC” *Electron Devices and Solid State IEEE Conference*, Dec. 2010.

[18] H. Zare-Hosseini,” Continuous-Time Delta-Sigma Modulators with Immunity to Clock-Jitter,” *Ph.D. dissertation, ECS Dept., University of Westminster, London, UK*, 2008.

[19] S. D. Arco, D. Iannuzzi, E. Pagano and P. Tricoli, “Analysis of Active Filter Behaviour by Means of Modified Z-Transform Method” *IEE Proc.-Electr. Power Appl.,* vol. 152, no. 3, May 2005.

[20] E. I. Jury, Theory and Application of The z-Transform Method. *Robert E. Krieger Publishing Co., New York 1964*.

[21] S. Pavan, “Excess Loop Delay Compensation in Continuous-Time Delta-Sigma Modulators” *IEEE Trans. Circuits Syst. II,* vol. 55, no. 11, pp. 1119-1123, Nov. 1999.

[22] J. A. Cherry and W. M. Snelgrove, “Excess Loop Delay in Continuous-Time Delta-Sigma Modulators” *IEEE Trans. Circuits Syst. II,* vol. 46, no. 4, pp. 376-389, April 1999.

[23] P. Benabes, M. Keramat and R. Kielbasa, “A Methodology for Designing Continuous-Time Sigma-Delta Modulators” *European Design and Test IEEE Conference,* pp. 46-50, March 1997.

[24] R. Khoini-Poorfard, L. B. Lim and D. A. Johns,” Time-Interleaved Oversampling A/D Converters: Theory and Practice,” *IEEE Trans. Circuits Syst. II*, vol. 44, no. 8, pp. 634-645, Aug. 1997.

[25] A. Gharbiya, T. C. Caldwell and D. A. Johns,” High-Speed Oversampling Analog-To-Digital Converters,” *International Journal of High Speed Electronics and Systems,* pp. 1-21, 2005.

[26] M. Kozak and I. Kale, “Novel Topologies for Time-Interleaved Delta-Sigma Modulators,” *IEEE Trans. Circuits Syst. II*, *Analog Digit. Signal Process*, vol. 47, no. 7, pp. 639–654, Jul. 2000.

[27] K. S. Lee, Y. Choi and F. Maloberti,” Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator,” *IEEE ISCAS,* pp. 473-476, 2004.

[28] B. Xia, S. Yan and E. S. Sinencio,”An RC Time Constant Auto-Tuning Structure For High Linearity Continuous-Time Delta-Sigma Modulators and Active Filters,” *IEEE Trans. Circuits Syst. I*, vol. 54, no. 11, pp. 2179-2188, Nov. 2004.

[29] J. A. Cherry and W. M. Snelgrove, “Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.* , vol. 46, no. 6, pp. 661–676, Jun. 1999.

[30] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. Toronto: John Wiley & Sons, Inc., 1997.

[31] A. Gharbiya and D. A. Johns,” Combining Multipath and Single-Path Time-Interleaved Delta-Sigma Modulators,” *IEEE Trans. Circuits Syst. II*, vol. 55, no. 12, pp. 1224-1228, Dec. 2008.

[32] K. Lee, S. Kwon and F. Maloberti, ”A Power-Efficient Two-Channel Time-Interleaved ΔΣ Modulator for Broadband Applications,” *IEEE J. Solid-State Circuits,* vol.42, no.6, pp. 1206-1215, June 2007.

[33] K. Lee and F. Maloberti,” Time-Interleaved Sigma-Delta Modulator Using Output Prediction Scheme” *IEEE Trans. Circuits Syst. II*, vol. 51, no. 10, pp. 537-541, Oct. 2004.

[34] M. Kozak, M. Karaman, and I. Kale, “Efficient Architectures for Time-Interleaved Oversampling Delta-Sigma Converters,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 8, pp. 802–810, Aug. 2000.

[35] A. Gharbiya and D. A. Johns, ” On The Implementation of Input –Feedforward Delta-Sigma Modulator,” *IEEE Trans. Circuits Syst. II*, vol. 53, no. 6, pp. 453-457, June. 2006.

[36] R. Schreier and G. C. Temes*, Understanding Delta-Sigma Data Converters*. New York: Wiley-IEEE Press, 2004.

[37] H. T. Jensen and I. Galton,” A Reduced-Complexity Mismatch-Shaped DAC for Delta-Sigma Data Converters,” *IEEE ISCAS*, pp. 504-507, 1998.

[38] I. Kale, “Sigma-delta modulation and polyphase filtering – the key to high-fidelity data conversion and instrumentation”, invited paper for IMEKO TC4 Workshop “ADC Modeling”, Smolenice Castle, Slovakia Republic, pp.183-192, 7-9 May 1996.

[39] Crawley, P.J. and Roberts, G.W. “Designing Operational Transconductance Amplifiers for Low Voltage Operation,” *IEEE International Symposium on Circuits and Systems*, pp. 1455-1458, 1993.

[40] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P.G. Welbers, “Matching Properties of MOS Transistors,” *IEEE J. Solid State Circuits*, Vol. 24, no. 6, pp. 1433-1439, Oct. 1989.

[41] Jose Bastos, Augusto Marques, Michel Steyaert, and Willy Sansen, “A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC,” *IEEE J. Solid State Circuits*, Vol. 33, pp. 1959-1969, Dec. 1998.

[42] Jose Bastos, Michel Steyaert, and Willy Sansen, “A High Yield 12-bit 250-MS/s CMOS D/A Converter,” in *CICC*, pp. 431-434, 1996.

[43] S.Padoan, A.Boni, C.Morandi, F Venturi, “A novel coding schemes for the ROM of parallel ADCs, featuring reduced conversion noise in the case of single bubbles in the thermometer code”, IEEE International Conference on Circuits and Systems, vol. 2, pp. 271-274, Sep. 1998.

[44] V. Hiremath, “Design of Ultra High Speed Flash ADC, Low Power Folding and Interpolating ADC in CMOS 90nm Technology” Master Thesis, Visvesvaraya Technological University, India, 2005.

[45] H. Oguey and E. Vittoz, “CODYMOS frequency dividers achieve low power consumption and high frequency”, electronic Letters, vol.9, pp. 386-387, Aug. 1973.

[46] Trevor C. Caldwell, “Time-Interleaved Continuous-Time Delta-Sigma Modulators” Master Thesis, University of Toronto, Canada, 2004.

[47] X. Chen, “A Wideband Low-Power Continuous-Time Delta-Sigma Modulator for Next Generation Wireless Applications” PhD Thesis, Oregon State University, USA, 2007.

[48] X. Meng, Y. Zhang, T. He, P. Paayandehnia and G. C. Temes, “A noise-coupled time-interleaved delta-sigma modulator with shifted loop delays” IEEE ISCAS, pp. 2045-2048, 2015.

[49] C. Y. Lu, C. Y. Hsieh, H. L. Chen and J. S. Chiang, ” A high-resolution time-interleaved delta-sigma modulator with low oversampling” IEEE 12th International Symposium on Integrated Circuits, pp. 5-8, 2009.

[50] C. Han and N. Maghari, “Time-Interleaved Noise-Coupling Delta-Sigma Modulator Using Modified Noise-Shaped Integrating Quantizer” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, pp. 548-560, 2015.

[51] M. Y. Choi, H. D. Roh, M. J. Lee, S. Kwon, Y. H. Lee, H. J. Park and B. S. Kong, “Continuous-time ΔΣ modulator having time-interleaved switched-capacitor brief-return-to-zero DAC with first-order jitter noise shaping” Electronics Letters, pp. 910-911, 2016.

[52] I. Kalafat, M. Al-Janabi and I. Kale, “Design and evaluation of time-interleaved variable center-frequency sigma-delta modulators” IEEE 18th International Conference on Digital Signal Processing, pp.1-6, 2013.

[53] I. Kalafat, M. Al-Janabi and I. Kale, “Novel Time-Interleaved variable-center frequency Σ-Δ modulators-design, analysis and critical evaluation” IEEE I2MTC, pp. 480-483, 2013.

[54] M. A. Makarem, M. Dessouky, M. Tawfik and H. F. Ragaie, “Double-sampled time-interleaved delta-sigma modulators” IEEE 4th Internation Design and Test Workshop, pp. 1-4, 2009.

[55] H. Fakhoury, C. Jabbour, H. Khushk, V. T. Nguyen and P. Loumeau, " A 65nm CMOS EDGE/UMTS/WLAN tri-mode four-channel time-interleaved ΣΔ ADC" IEEE North-East Workshop on Circuits and Systems and TAISA Conference, pp. 1-4, 2009.

[56] X. Yang, G. Chen, J. Cheng and X. Xu, "A novel two-channel time-interleaved forth-order sigma-delta modulator topology" IEEE Asia Pacific Conference on Circuits and Systems, pp. 1152-1155, 2008.

[57] J. K. Cho and S. Woo, "A 6-mW, 70.1-dB SNDR, and 20-MHz BW Continuous-Time Sigma-Delta Modulator Using Low-Noise High-Linearity Feedback DAC" IEEE Trans. Very Large Scale Integr. (VLSI) Syst., pp. 1-14, 2017.

[58] C. H. Weng, Y. Y. Liu and T. H. Lin, "A 1-V 5-MHz Bandwidth 68.3-dB SNDR Continuous-Time Delta-Sigma Modulator With a Feedback-Assisted Quantizer" IEEE Trans. Circuits Syst. I, Reg. Papers, pp. 1-9, 2017.

[59] A. Edward, Q. Liu, C. B. Vidrios, M. Kinyua, E. G. Soenen, A. I. Karsilayan an J. S. Martines, "A 43-mW MASH 2-2 CT Sigma Delta Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40nm CMOS" IEEE J. Solid-State Circuits, pp. 448-459, 2017.

[60] A. Morgado, R. D. Rio and J. Rosa, "Design of a power-efficient widely-programmable Gm-LC band-pass sigma-delta modulator for SDR" IEEE ISCAS, pp. 53-56, 2016.

[61] P. L. Muntal, I. H. H. Jorgensen and E. Bruun, "A 10 MHz bandwidth continuous-time delta-sigma modulator for portable ultrasound scanners" IEEE NORCAS, pp. 1-5, 2016.

[62] S. Pavan, "Continuous-time ΔΣ modulators with dual switched capacitor resistor DACs" IEEE ISCAS, pp. 69-72, 2016.

[63] Y. H. Leow, H. Tang, Z. C. Sun and L. Siek, "A 1 V 103 dB 3rd-Order Audio Continuous-Time Delta Sigma ADC With Enhanced Noise Shaping in 65 nm CMOS" IEEE Solid-State Circuits, pp. 2625-2638, 2016

[64] A. Sukumaran and S. Pavan, "Design of Continuous-Time Modulators With Dual Switched-Capacitor Return-to-Zero DACs" IEEE Solid-State Circuits, pp.1619-1629, 2016.

[65] Q. Huang, Z. Teng, X. Tang, H. Lin and H. Wen, “Mass Measurement Method for the Electronic Balance Based on Continuous-Time Sigma-Delta Modulator” IEEE Trans. Instrum. Meas., pp. 1300-1309, 2016.

[66] K. Singh and S. Pavan, “A 14 Bit Dual Channel Incremental Continuous-Time Delta Sigma Modulator for Multiplexed Data Acquisition” IEEE 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), pp. 230-235, 2016.

[67] T. Kim, C. Han and N. Maghari, “A 7.2 mW 75.3 dB SNDR 10 MHz BW CT Delta-Sigma Modulator Using Gm-C-Based Noise-Shaped Quantizer and Digital Integrator” IEEE J. Solid-State Circuits, pp. 1840-1850, 2016.

[68] D. Basak, D. Li, Z. Fu, J. Wang, Z. Yang and K. P. Pun, “A fast three-level feedback technique in continuous-time delta-sigma modulators” IEEE EDSSC, pp. 149-152, 2016.

[69] J. Wagner, S. Reich, R. Ritter, J. Anders and M. Ortmanns, “Finite GBW in single OpAmp CT ΣΔ modulators” IEEE ICECS, pp. 468-471, 2016.

[70] C. H. Weng, T. A. Wei, E. Alpman, C. T. Fu and T. H. Lin, “A Continuous-Time Delta-Sigma Modulator Using ELD-Compensation-Embedded SAB and DWA-Inherent Time-Domain Quantizer” IEEE J. Solid-State Circuits, pp. 1235-1245, 2016.

[71] M. Webb and H. Tang, “A low-power low-complexity continuous-time Gm-C based Delta-Sigma modulator for wireless and instrumentation applications” IEEE International Workshop on Electromagnetics: Applications and Student Innovation Competition (iWEM), pp. 1-3, 2016.

[72] H. Chae and M. P. Flynn, “A 69 dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability” IEEE J. Solid-State Circuits, pp. 649-659, 2016.

[73] R. Ritter, J. G. Kauffman, J. Becker and M. Ortmanns, “A 10 MHz Bandwidth, 70 dB SNDR Continuous Time Delta-SigmaModulator With Digitally Improved Reconfigurable Blocker Rejection” IEEE J. Solid-State Circuits, pp. 660-670, 2016.

[74] C. Chu, J. Wanger, A. Marashli, J. Chi and M. Ortmanns, “A study on op-amp nonlinearity in a single-bit CT ΔΣ modulator employing GBW compensation” IEEE PRIME, pp. 1-4, 2016.

[75] A. Sanyal and N. Sun, ”Dynamic Element Matching Techniques for Static and Dynamic Errors in Continuous-Time Multi-Bit Modulators” IEEE Trans. Emerg. Topics Comput., pp. 598-611, 2015.

[76] R.T. Baird, and T.S. Fiez, ”A low oversampling ratio 14-b 500-kHz ΣΔ ADC with a self-calibrated multibit DAC” IEEE J. Solid-State Circuits, vol. 31, pp. 312–320, 1996.

[77] J. Nedved, J. Vanneuville, D. Gevaert and J. Sevenhans,”A transistor-only switched current sigma-delta A/D converter for a CMOS speech codec” IEEE J. Solid-State Circuits vol. 30, pp. 819–822 July 1995.

[78] L. Luh, J. Choma and J. Draper, ”A 50-MHz continuous-time switchedcurrent ΣΔ modulator” Proc. IEEE Int. Symp. Circuits Syst., pp. 579–582 1998.

[79] F. Gerfers , M. Ortmanns and Y. Manoli,”A 12-bit power efficient continuous-time ΣΔ modulator with 220 µW power consumption” Proc. Eur. Solid-State Circuits Conf., pp. 536–539 2001.

[80] E.J. van der Zwan and E.C. Dijkmans, ”A 0.2-mW CMOS ΣΔ modulator for speech coding with 80 dB dynamic range” IEEE J. Solid-State Circuits vol. 31 December 1996.

[81] J.F. Jensen, G. Raghavan, A.E. Cosand and R.H. Walden, “A 3.2-GHzsecond-order delta-sigma modulator implemented in InP HBT technology” IEEE J. Solid-State Circuits vol. 30, pp. 1119–1127 October 1995.

[82] K. Nguyen, “Practical dynamic element matching techniques for 3-level unit elements” IEEE CICC conference, July 2017.

[83] M. Neitola and T. Rahkonen, ”A Generalized Data-Weighted Averaging Algorithm” IEEE Trans. Circuits Syst. II, vol. 57, pp. 115-119, 2010.

[84] U. Yazkurt and G. Dundar, “Scaling Input Signal Swings of Overloaded Integrators in Resonator-Based Sigma-Delta Modulators” IEEE ICECS Conference, pp. 10-13, July 2006.

Design of a Delayless Feedback Path Free 2nd-order Two-Path Time-Interleaved Discrete-Time Delta-Sigma Modulator- a New Approach

Jafar Talebzadeh and Izzet Kale
Applied DSP & VLSI Research Group
Department of Engineering
University of Westminster London, W1W 6UW, UK
Emails: Jtalebzadeh@gmail.com & kalei@westminster.ac.uk

***Abstract*—this paper presents the design procedure for a 2nd_order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator from a conventional single-loop 2nd-order Discrete-Time (DT) ΔΣ modulator through the use of time domain equations and time-interleaving concepts [1]. The resulting modulator is free from the delayless feedback path and has only one set of integrators. The delayless feedback path issue in Time-Interleaved (TI) ΔΣ modulators is a critical restriction for the implementation of TI ΔΣ modulators and is effectively eliminated through the use of the approach proposed in this paper. The DTTI ΔΣ modulator requires only three op-amps and two quantizers both of which work concurrently, in comparison to the single-loop DT counterpart that also deploys two op-amps. For an OverSampling Ratio (OSR) of 16 and a clock frequency of 640MHz, our simulation results show a maximum Signal-to-Noise Ratio (SNR) for the DTTI ΔΣ modulator to be 70.5dB with an input bandwidth of 20MHz which has 15dB improvement in comparison to its single-loop, single-path DT counterpart.**

Keywords*— *Time-Interleaved, ΔΣ modulator, Signal-to-Noise Ratio.

I. INTRODUCTION

Recent trends in the portable communication industry demand both high resolution and low power Analog-to-Digital Converters (ADCs). These requirements can be met by utilizing ΔΣ modulators which perform analog-to-digital conversion for relatively low bandwidth signals. Both the OSR and the technology restrict the deployable signal bandwidth of ΔΣ modulators.

Recently wideband applications require the ADCs with larger signal bandwidth. In order to increase the signal bandwidth the modulator can deal with, a variety of methods can be used such as: using higher sampling frequency, increasing the order of the modulator and the number of quantizer bits. However, each of them has a price and is restricted by technology deployed. Using above mentioned methods to increase OSR make the design of the modulator more complicated and may cause stability problem which require to be dealt with carefully.

One efficient and attractive way to increase the OSR, is to consider the time-interleaving approach through which parallelism can be incorporated in ADCs in order to increase the effective sampling rate [1]-[8]. This approach is a practical solution that does not necessitate state of art technologies.

978-1-5090-3963-0/17/$31.00 ©2017 IEEE

However, using straightforward time-interleaving technique for ΔΣ modulators results in a bit improvement in SNR performance of the whole modulator. As shown in [1] and [2], the time-interleaving can be successfully applied to ΔΣ modulators. A TI ΔΣ modulator deploys M identical cross-coupled modulators working concurrently and each running at a sampling rate of F_s. The effective sampling rate is the same as a single-loop ΔΣ modulator which operates at a sampling frequency of MF_s.

One set of integrators is shared between two paths in order to save power dissipation, silicon area and to eliminate the instability arising from DC offset mismatch between indivisual integrator sets.

This paper is organized as follows. In section II, a 2nd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator is derived from a 2nd-order conventional DT ΔΣ modulator by deploying the time domain equations. In section III, the delayless feedback path problem is discussed and our proposed solution is presented in detail in this section. In section IV, MATLAB simulation results are presented. Finally, conclusions are given in section V.

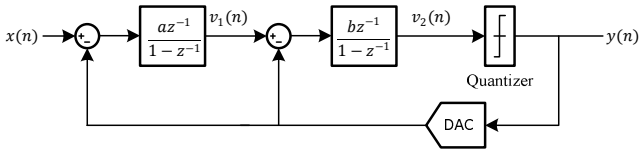


Figure 1: A 2nd-order conventional single-loop DT ΔΣ modulator.

II. DERIVATION OF TIME-INTERLEAVED ΔΣ MODULATOR

In order to derive a 2nd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator, the time-interleaving concept and the time domain equations of its conventional single-loop 2nd-order DT ΔΣ modulator counterpart as shown in Figure 1, are used [1]. The feedback loop of the DAC is assumed ideal and has unity transfer function ($H_{DAC}(z) = 1$). The time-domain equations defining the conventional single-loop 2nd-order DT ΔΣ modulator can be cast in the following way:

$$v_1(2n) = ax(n) \; - ay(n) + v_1(n-1) \quad (1)$$

$$v_2(2n) = bv_1(n) - by(n) + v_2(n-1) \quad (2)$$

$$y(n) \; = Q[v_2(n)] \quad (3)$$

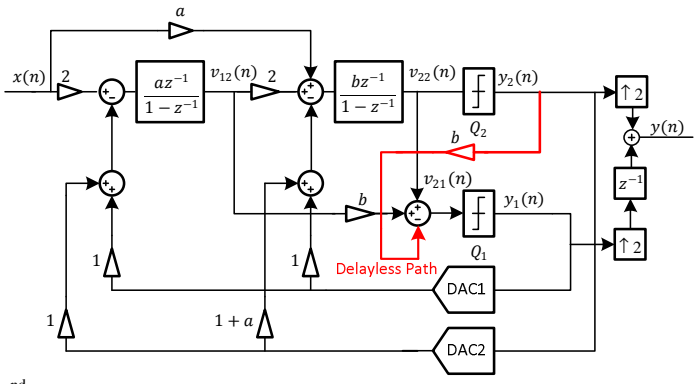


Figure 2: A two-path 2nd-order DTTI ΔΣ modulator with shared integrators and delayless feedback path highlighted.

Where $Q[.]$ represents the quantization function.

In order to derive the DTTI ΔΣ modulator, the time domain equations of the single-loop 2nd –order DT ΔΣ modulator are written for two consecutive time slots and are as (2n)th and (2n+1)th.

$$v_1(2n) = ax(2n-1) - ay(2n-1) + v_1(2n-1) \quad (4)$$
$$v_2(2n) = bx(2n-1) - by(2n-1) + v_2(2n-1) \quad (5)$$
$$y(2n) = Q[v_2(2n)] \quad (6)$$

and

$$v_1(2n+1) = ax(2n) - ay(2n) + v_1(2n) \quad (7)$$
$$v_2(2n+1) = bx(2n) - by(2n) + v_2(2n) \quad (8)$$
$$y(2n+1) = Q[v_2(2n+1)] \quad (9)$$

A fast demultiplexer is used to distribute the input signal $x(n)$ between the two paths/channels. The demultiplexer operates at twice the clock frequency of each channel [1]. The input $x(n)$ is relabeled as follows:

$$x_1(n) = x(2n), \; x_2(n) = x(2n-1) \quad (10)$$

Similarly, the other nodes of the modulator are relabelled:

$$v_{11}(n) = v_1(2n), \quad v_{12}(n) = v_1(2n-1) \quad (11)$$
$$v_{21}(n) = v_2(2n), \quad v_{22}(n) = v_2(2n-1) \quad (12)$$
$$y_1(n) = y(2n), \quad y_2(n) = y(2n-1) \quad (13)$$

To save power consumption and silicon area the input demultiplexer is removed and the input signal $x(n)$ is shared between two channels. Therefore equation (10) results in (14) as follows:

$$x_1(n) = x_2(n) = x(n) \quad (14)$$

The resulting equations are written as equations (15), (16), (17), (18) and (19) and the DTTI ΔΣ modulator shown in Figure 2 is derived directly from these equations [1]:

$$v_{12}(n) = 2ax(n-1) - ay_1(n-1) - ay_2(n-1) + v_{12}(n-1) \quad (15)$$
$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \quad (16)$$
$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \quad (17)$$
$$y_1(n) = Q[v_{21}(n)] \quad (18)$$
$$y_2(n) = Q[v_{22}(n)] \quad (19)$$

The dc offset mismatch of the two individual integrators set between channels in the DTTI ΔΣ modulator can cause instability which can be eliminated by sharing one set of integrators between the two channels [2]. A fast input demultiplexer which is a limiting factor for the performance of the DTTI ΔΣ modulators is necessary. However this input demultiplexer can be removed and the input signal simply shared between the two channels [5][6][10]. The Signal Transfer Function (STF) of the DTTI ΔΣ modulator exhibits some notches in its response at the following frequencies $0.5F_{clk}$, $1.5F_{clk}$, $2.5F_{clk}$, $3.5F_{clk}$, ... where F_{clk} is the clock frequency of the DTTI ΔΣ modulator resulting from the removal of the input demultiplexer. This modification and has no effect on the modulator's Noise Transfer Function (NTF) [5][6][10].

III. DELAYLESS FEEDBACK PATH ISSUE

The "delayless feedback path" problem makes the implementation of multi-path TI ΔΣ modulator impractical [4]. We have developed a new approach to circumvent this problem effectively with reduced complexity and the focus of this paper is on this approach. The root of the problem stems from equation (17) where $v_{21}(n)$ (the input of the quantizer Q1) is coupled directly to $y_2(n)$, dictating that the second quantizer (Q2) output has to connect to the input of quantizer (Q1) without any delay! We propose an approach based on an error correction technique to circumvent/eliminate this delayless feedback path. This is achieved by intentionally inducing an analog domain error by using the output of DAC2 as shown in Figure 3. The error is subsequently corrected to a great extent in the digital domain thereby circumventing/eliminating the delayless feedback path. A step by step mathematical analysis of the approach is exposed in the following lines to aid understanding. Furthermore a detailed event sequence diagram with the associated DAC outputs and the delay from the outputs of quantizers Q1 and Q2 that propagates through to the outputs of DAC1 and DAC2 as δ are shown in Figure 4. As a direct consequence it is clearly seen that the DAC2 output which is sampled at the nth time slot is

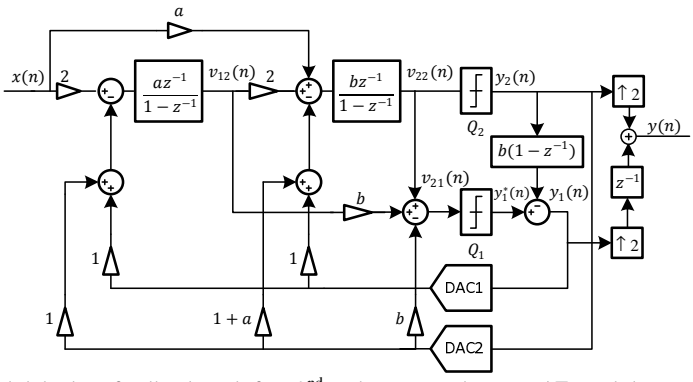


Figure 3: The proposed delayless feedback path free 2nd-order two-path DTTI ΔΣ modulator with shared integrators.

$y_2(n-1)$. However theory and the equations require that we should have $y_2(n)$. We can creatively overcome this problem by looking at the input and output of Q1, as depicted in Figure 2. The signal $v_{21}(n)$ is quantized through Q1 as follows:

$$y_1(n) = Q[v_{21}(n)] \tag{20}$$

By substituting (17) into (20) we arrive at equation (21):

$$y_1(n) = Q[bv_{12}(n) - by_2(n) + v_{22}(n)] \tag{21}$$

Equation (21) is rewritten by using the output of DAC2 in (22):

$$y_1(n) = Q[cv_{12}(n) - by_2(n-1) + v_{22}(n)] + by_2(n-1) - by_2(n) \tag{22}$$

We label the output of Q1 as $y_1^*(n)$ in (23):

$$y_1(n) = y_1^*(n) + by_2(n-1) - by_2(n) \tag{23}$$
$$error = b\Delta y = b(y_2(n) - y_2(n-1)) \tag{24}$$
$$Y_1(z) = Y_1^*(z) - b(1-z^{-1})Y_2(z) \tag{25}$$

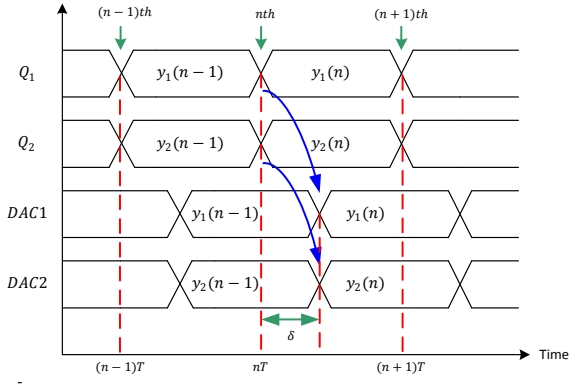


Figure 4: Sequence of events for the outputs of the quantizers and DACs for the DTTI.

Equation (23) illustrates $y_1^*(n)$ (the output of Q1) which contains the error depicted in equation (24) and as mentioned earlier needs to be corrected before applying it to the input of DAC1. The correction is performed in the digital domain by a first order differencer block $(1-z^{-1})$ as stipulated in (25). The first order differencer block only corrects the error in equation (23). It has no effect on targets and the signal or the quantization noise of our proposed 2nd-order two-path DTTI ΔΣ modulator which has shared integrators as shown in Figure 3. If the simple correction approach proposed above is not utilised the uncorrected error causes instability changing the modulator dynamics and increasing its order.

IV. SIMULATION RESULTS

A conventional single-loop 2nd-order single-path DT ΔΣ modulator with an OSR of 8 has been designed to operate with a clock frequency of 320MHz and a signal bandwidth of 20MHz and was modelled and simulated using SIMULINK. The modulator coefficients were chosen through the use of the sigma-delta toolbox [11] to be $a = 0.5$ and $b = 2.0$. The resulting 2nd-order two-path DTTI ΔΣ modulator has the same coefficients as the DT single-path, single-loop ΔΣ modulator as illustrated in Figure 3 with an OSR of 16 which operates from a clock frequency of 640MHz with a signal bandwidth of 20MHz. The single-loop, single-path 2nd order DT ΔΣ modulator DAC requires 4 bit resolution and as a consequence 15 comparators are chosen. The quantizer Q2 in DTTI ΔΣ modulator has 15 levels; however, the quantizer Q1 needs to have 31 levels due to the increase in the signal swing at the input of this quantizer. Therefore it will not lead to any SNR loss. After correcting the error as dictated by equation (13) in the digital domain, $y_1(n)$ will also need to be 4 bits in length.

The STF and NTF of the single-loop, single-path DT ΔΣ modulator of Figure 1 can be formulated as follows:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{26}$$
$$STF(z) = z^{-2} \tag{27}$$
$$NTF(z) = (1-z^{-1})^2 \tag{28}$$

Where $X(z)$ and $E(z)$ represents the z-transform of the input signal and quantization noise of the quantizer respectively. The STF and NTFs of the DTTI ΔΣ modulator of Figure 3 can be derived and formulated as follows:

$$Y(z) = Y_1(z^2)z^{-1} + Y_2(z^2) \tag{29}$$
$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) \tag{30}$$

$$STF(z) = z^{-2}(1 + z^{-1}) \quad (31)$$
$$NTF_1(z) = z^{-1}(1 - z^{-1})^2 \quad (32)$$
$$NTF_2(z) = (1 - z^{-1})^2 \quad (33)$$

Where $STF(z), NTF_1(z)$ and $NTF_2(z)$ represent the signal transfer function from $x(t)$ to $y(n)$, the noise transfer function from $e_1(n)$ (quantization noise of Q1) to $y(n)$ and the noise transfer function from $e_2(n)$ (quantization noise of Q2) to $y(n)$ respectively. The terms in z^2 in (21) show the effect of the up-samplers in the modulator. The term in $(1 + z^{-1})$ from the $STF(z)$ of the DTTI ΔΣ modulator shows the effect of removing the input demultiplexer of the DTTI ΔΣ modulator causing some notches in the STF as explained earlier on in the paper and as described in [5][6][10]. Figure 5 shows the NTFs of the DT and the DTTI ΔΣ modulator. As can be seen, NTF of the DTTI ΔΣ modulator shape the quantization noise more than the NTF of the DT ΔΣ modulator.

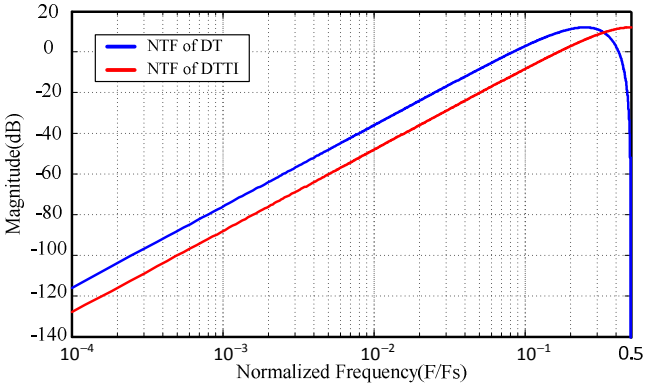


Figure 5: The NTFs of the DT and the DTTI ΔΣ modulator.

Figure 6 shows the comparison of the output spectra of the single-loop, single-path DT and the two-path DTTI ΔΣ modulators. As can be seen the two-path DTTI ΔΣ modulator output spectrum has more in-band noise shaping than its single-loop, single-path DT counterpart. The SNRs of the DT and the DTTI ΔΣ modulators for a single tone (sine) input signal having a frequency of 4.892MHz and an amplitude of -2dBFS with clock frequencies of 320MHz and 640MHz are 55.5dB and 70.5dB respectively. Therefore in this particular case, the SNR of the DTTI ΔΣ modulator shows a 15dB improvement in comparison to the DT one alone.

V. CONCLUSION

The design of a 2nd-order single-loop two-path DTTI ΔΣ modulator free from the delayless feedback path problem that can be extended to any-order multi-path DTTI ΔΣ modulator has been shown in this paper. The simulation results illustrate that the resulting DTTI ΔΣ modulator having an OSR of 16 and a clock frequency of 640MHz with a 20MHz signal bandwidth attains a maximum SNR of 70.5dB. This result suggests that the SNR is improved by 15dB in comparison to the maximum SNR of the conventional single-loop 2nd-order single-path DT ΔΣ modulator.

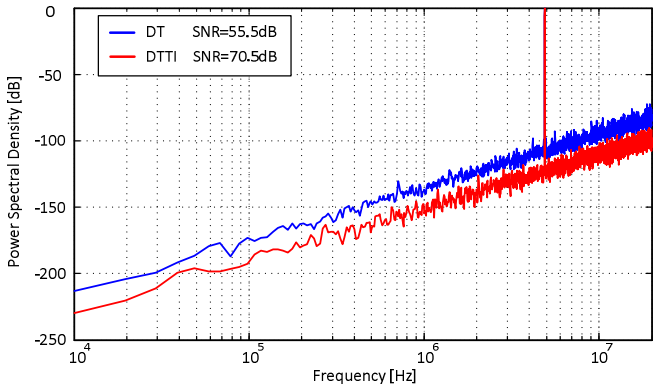


Figure 6: The output spectra of the conventional DT and the DTTI ΔΣ modulator for a 4.892MHz input sine signal with clock frequencies of 320MHz and 640MHz respectively.

REFERENCES

[1] M. Kozak and I. Kale, "Novel Topologies for Time-Interleaved Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 7, pp. 639–654, Jul. 2000.

[2] R. Khoini-Poorfard, L. B. Lim and D. A. Johns," Time-Interleaved Oversampling A/D Converters: Theory and Practice," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 8, pp. 634-645, Aug. 1997.

[3] T. C. Caldwell and D. A. Johns," A Time-Interleaved Continuous-Time ΔΣ Modulator with 20-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits,* vol. 41, no. 7, pp. 1578-1588, July 2006.

[4] K. S. Lee, Y. Choi and F. Maloberti," Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator," *IEEE ISCAS,* pp. 473-476, 2004.

[5] T. C. Caldwell," Time-Interleaved Continuous-Time Delta-Sigma Modulators," MSc Thesis, University of Toronto, Toronto, Ontario, Canada, 2004.

[6] A. Gharbiya and D. A. Johns," Combining Multipath and Single-Path Time-Interleaved Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 12, pp. 1224-1228, Dec. 2008.

[7] K. Lee, S. Kwon and F. Maloberti,"A Power-Efficient Two-Channel Time-Interleaved ΔΣ Modulator for Broadband Applications," *IEEE J. Solid-State Circuits,* vol.42, no.6, pp. 1206-1215, June 2007.

[8] K. Lee and F. Maloberti," Time-Interleaved Sigma-Delta Modulator Using Output Prediction Scheme" *IEEE Trans. Circuits Syst. II*, vol. 51, no. 10, pp. 537-541, Oct. 2004.

[9] J. Talebzadeh and I. Kale, "Delta-Sigma Modulator," UK Patent GB2524547, March 26, 2014.

[10] A. Gharbiya, T. C. Caldwell and D. A. Johns," High-Speed Oversampling Analog-To-Digital Converters," *International Journal of High Speed Electronics and Systems,* pp. 1-21, 2005.

[11] R. Schreier, "Delta Sigma Toolbox," Mathworks, 14 Jan 2000.

Design and Simulation of a 3rd-order Discrete-Time Time-Interleaved Delta-Sigma Modulator with Shared Integrators between Two Paths

Jafar Talebzadeh and Izzet Kale
Applied DSP & VLSI Research Group
Department of Engineering
University of Westminster London, W1W 6UW, UK
Emails: Jtalebzadeh@gmail.com & kalei@westminster.ac.uk

***Abstract*, this paper presents the design and simulation of a 3rd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator. By exploiting the concept of the time-interleaving techniques and time domain equations, a conventional 3rd-order Discrete-Time (DT) ΔΣ modulator is converted to a corresponding 3rd-order two-path DTTI counterpart. For the sake of saving power and silicon area, the integrators between the two paths of the DTTI ΔΣ modulator are shared. Using one set of integrators makes the DTTI ΔΣ modulator robust to path mismatch effects compared to the typical DTTI ΔΣ modulator which has individual integrators in all paths. A problem arises out of sharing integrators between paths which we call the delayless feedback problem. A solution for this problem is proposed in this paper and for an OverSampling Ratio (OSR) of 16 and a clock frequency of 320MHz, a maximum SNR of 76.5dB is obtained.**

***Keywords*: Discrete-Time, Time-Interleaved, ΔΣ modulator, Signal-to-Noise Ratio, OverSampling Ratio.**

I. INTRODUCTION

The ΔΣ modulators can achieve a very high resolution analog-to-digital conversion for low bandwidth applications by using oversampling and noise shaping techniques[1]. Recently, wideband applications require the ADCs with higher signal bandwidth. In order to increase the signal bandwidth of the modulator, a variety of methods can be used such as: using higher sampling frequency, increasing the order of the modulator and the number of quantizer bits.However, each of them has a price and is limited by technology [2].

One efficient appoach to increase the signal bandwidth is to use the time-interleaving technique [3] which increases the effective sampling frequency by paralleling more channels. This method is discussed in the next section.

II. TIME-INTERLEAVED (TI) ΔΣ MODULATORS

The well known procedure for the design of a ΔΣ modulator is based on choosing: the order and architecture of the ΔΣ modulator, the OSR and the number of bits for the quantizer. The time-interleaving technique can be successfully applied to ΔΣ modulators. However, the performance of the whole modulator is degraded due to channel mismatches. By paralleling M interconnected modulators that are working concurrently, the effective sampling rate and the OSR becomes M times the clock rate and the OSR of each modulator respectively [4],[5]. It should be noted that the required resolution can be obtained without increasing the order of the modulator or the number of bits for the quantizer and also without utilizing a state of the art technology.

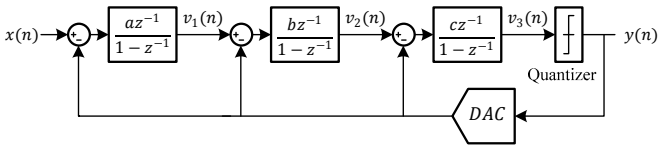


Figure 1: A 3rd-order conventional single-loop DT ΔΣ modulator.

A. DERIVATION OF THE TI ΔΣ MODULATOR

The 3rd-order DTTI ΔΣ modulator is derived directly from the time domain node equations of its conventional DT ΔΣ modulator as shown in Figure 1. It is assumed that the DAC in the feedback loop is ideal ($H_{DAC}(z) = 1$). The time domain equations of the modulator are written for two consecutive time slots as (2n)th and (2n+1)th as follows [6]:

$$v_1(2n) = ax(2n-1) - ay(2n-1) + v_1(2n-1) \quad (1.a)$$
$$v_2(2n) = bv_1(2n-1) - by(2n-1) + v_2(2n-1) \quad (1.b)$$
$$v_3(2n) = cv_2(2n-1) - cy(2n-1) + v_3(2n-1) \quad (1.c)$$
$$y(2n) = Q[v_3(2n)] \quad (1.d)$$

and

$$v_1(2n+1) = ax(2n) - ay(2n) + v_1(2n) \quad (2.a)$$
$$v_2(2n+1) = bv_1(2n) - by(2n) + v_2(2n) \quad (2.b)$$
$$v_3(2n+1) = cv_2(2n) - cy(2n) + v_3(2n) \quad (2.c)$$
$$y(2n+1) = Q[v_3(2n+1)] \quad (2.d)$$

where $Q[.]$ represents the quantization function. The input $x(n)$ is distributed between two channels through an input multiplexer which operates at twice the clock frequency of each channel. The input $x(n)$ is relabelled as follows:

$$x_1(n) = x(2n), \quad x_2(n) = x(2n-1) \quad (3)$$

978-1-5090-5963-8/17/$31.00 ©2017 IEEE

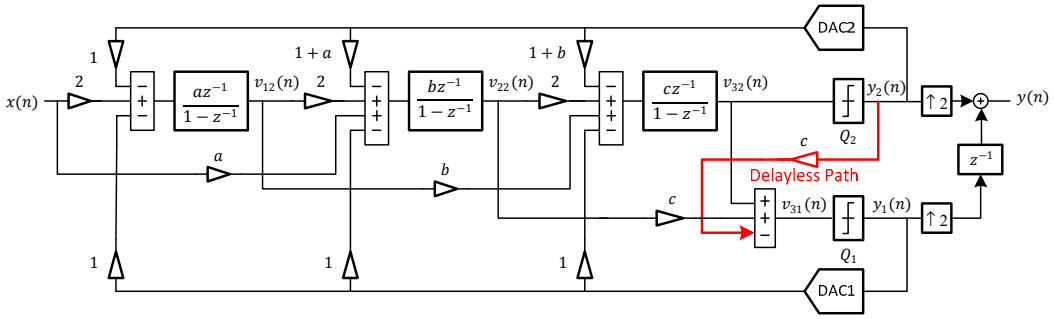


Figure 2: A 3rd-order DTTI ΔΣ modulator with shared integrators and delayless feedback path.

Similarly, the other nodes of the modulator are relabelled:

$$v_{11}(n) = v_1(2n), \quad v_{12}(n) = v_1(2n-1) \tag{4.a}$$
$$v_{21}(n) = v_2(2n), \quad v_{22}(n) = v_2(2n-1) \tag{4.b}$$
$$v_{31}(n) = v_3(2n), \quad v_{32}(n) = v_3(2n-1) \tag{4.c}$$
$$y_1(n) = y(2n), \quad y_2(n) = y(2n-1) \tag{4.d}$$

By sharing only one set of integrators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. Hence equation (3) results in (5) as follows:

$$x_1(n) = x_2(n) = x(n) \tag{5}$$

Equation sets (6) and (7) are derived by substituting equation set (4) and equation (5) into equation sets (1) and (2) respectively as follows:

$$v_{11}(n) = ax(n) - ay_2(n) + v_{12}(n) \tag{6.a}$$
$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \tag{6.b}$$
$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \tag{6.c}$$
$$y_1(n) = Q[v_{31}(n)] = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \tag{6.d}$$

and

$$v_{12}(n+1) = ax(n) - ay_1(n) + v_{11}(n) \tag{7.a}$$
$$v_{22}(n+1) = bv_{11}(n) - by_1(n) + v_{21}(n) \tag{7.b}$$
$$v_{32}(n+1) = cv_{21}(n) - cy_1(n) + v_{31}(n) \tag{7.c}$$
$$y_2(n+1) = Q[v_{32}(n+1)] \tag{7.d}$$

Equation set (7) can be rewritten as equation set (8):

$$v_{12}(n) = ax(n-1) - ay_1(n-1) + v_{11}(n-1) \tag{8.a}$$
$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \tag{8.b}$$
$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \tag{8.c}$$
$$y_2(n) = Q[v_{32}(n)] \tag{8.d}$$

Equation set (9) is derived by further substituting equation set (6) into equation set (8).

$$v_{12}(n) = 2ax(n-1) - ay_1(n-1) - ay_2(n-1) + v_{12}(n-1) \tag{9.a}$$
$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \tag{9.b}$$
$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - cy_1(n-1) - c(1+b)y_2(n-1) + v_{32}(n-1) \tag{9.c}$$

The 3rd-order DTTI ΔΣ modulator which is shown in Figure 2 is derived directly from the time domain equation set (6) and (9).

The motive behind sharing integrators is to eliminate the instability that can arise from the DC offset mismatch of the two individual integrator set based two channel interleaving case. The DTTI ΔΣ modulators need an input demultiplexer which samples the input signal at the highest clock frequency of the DTTI ΔΣ modulator and distributes it between channels. This fast demultiplexer is a limiting factor for the performance of the DTTI ΔΣ modulators. This architecture does not need an input demultiplexer and the input signal is shared between channels [3],[5]. Removing the input demultiplexer has no effect on the NTF of the DTTI ΔΣ modulator but it causes some notches in its Signal Transfer Function (STF) at the following frequencies $0.5F_{clk}$, $1.5F_{clk}$, $2.5F_{clk}$, $3.5F_{clk}$, … which is shown in Figure 5 where F_{clk} is the clock frequency of the DTTI ΔΣ modulator [5].

B. DELAYLESS FEEDBACK PATH PROBLEM IN TI ΔΣ MODULATORS

This is the issue that forms the focus of this paper which makes implementation of Time Interleaved (TI) ΔΣ modulators with shared integrators impractical and it is called the "*delayless feedback path problem*" that comes from equation (6.c) in which $v_{31}(n)$ (the input of quantizer Q1) is directly linked to $y_2(n)$. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay [7]. One method to eliminate the delayless path is to move this feedback to the digital domain instead of performing it in the analog domain [5]. The disadvantage of this method is that the first quantizer (Q1) requires more comparators than the number of the comparators in the second quantizer (Q2) [7]. The second method is to use a sample-and-hold in front of the first quantizer (Q1) and quantizing the signal when the output of DAC2 is ready [3]. This method needs a complicated timing generator, a sample-and-hold and also faster integrators. The third method which is our proposed method is based on substituting $v_{32}(n)$ for $y_2(n)$ in equation (6.c). This method increases the quantization noise of the quantizer Q2 at the output $y(n)$. To better understand how this works we shall perform a step by step

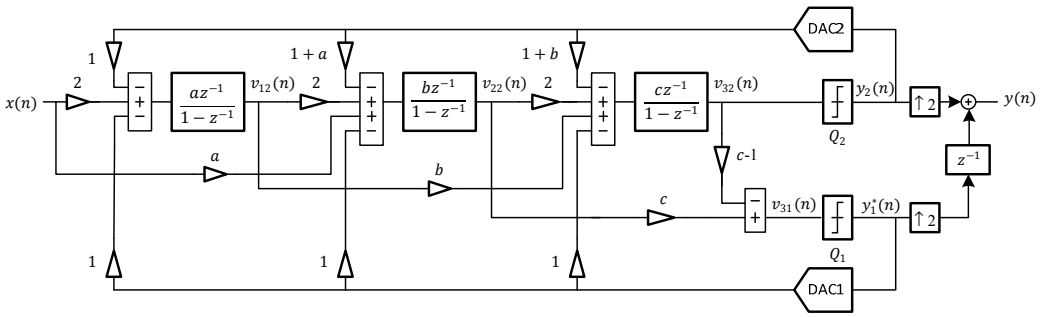


Figure 3: The proposed 3rd-order DTTI ΔΣ modulator with shared integrators and without delayless feedback path.

mathematical analysis of what happens. Quantizer Q1 and Q2 quantize the signal $v_{31}(n)$ and $v_{32}(n)$ as follows:

$$y_1(n) = Q[v_{31}(n)] = v_{31}(n) + e_1(n) \quad (10)$$
$$y_2(n) = Q[v_{32}(n)] = v_{32}(n) + e_2(n) \quad (11)$$

Where $e_1(n)$ and $e_2(n)$ represent the quantization noise of the quantizer Q1 and Q2 respectively. Equation (12) is derived by substituting (6.c) into (10):

$$y_1(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) + e_1(n) \quad (12)$$

Equation (13) is given by substituting $v_{32}(n)$ for $y_2(n)$ into equation (12). The output of Q1 is called $y_1^*(n)$ in (13):

$$y_1^*(n) = cv_{22}(n) - (c-1)v_{32}(n) + e_1(n) \quad (13)$$

$y_1^*(n)$ approximates $y_1(n)$ in the DTTI ΔΣ modulator. The error which is induced by this method is presented by equation (14). This error does not cause instability in the modulator but increases quantization noise of quantizer Q2 at the output $y(n)$ followed by degrading the SNR of the modulator.

$$error = y_1^*(n) - y_1(n) = cy_2(n) - cv_{32}(n) = ce_2(n) \quad (14)$$

The resulting 3rd-order DTTI ΔΣ modulator is shown in Figure 3. The Signal Transfer Function (STF) and Noise Transfer Function (NTF) can be obtained by determining the loop filters of the modulator. In this design, the DTTI ΔΣ modulator has six loop filters ($FF_1(z), FF_2(z), H_1(z), H_2(z), H_3(z)$ and $H_4(z)$) and can be determined with the help of the symbolic toolbox of MATLAB. These loop filters for the DTTI ΔΣ modulator are as depicted in Figure 4. The STF and NTFs can be formulated by performing the following algebraic analysis:

$$Y(z) = Y_1^*(z^2)z^{-1} + Y_2(z^2) \quad (15)$$
$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) \quad (16)$$
$$NTF_1(z) = \frac{H_3(z^2) + [1 - H_4(z^2)]z^{-1}}{[1 - H_1(z^2)][1 - H_4(z^2)] - H_2(z^2)H_3(z^2)} \quad (17)$$
$$NTF_2(z) = \frac{[1 - H_1(z^2)] + H_2(z^2)z^{-1}}{[1 - H_1(z^2)][1 - H_4(z^2)] - H_2(z^2)H_3(z^2)} \quad (18)$$
$$STF(z) = NTF_1(z)FF_1(z^2) + NTF_2(z)FF_2(z^2) \quad (19)$$

Where $STF(z), NTF_1(z)$ and $NTF_2(z)$ represent the signal transfer function from $x(n)$ to $y(n)$, the noise transfer function from $e_1(n)$ to $y(n)$ and the noise transfer function from $e_2(n)$ to $y(n)$ respectively. The z^2 terms show the effect of the up-samplers in the modulator.

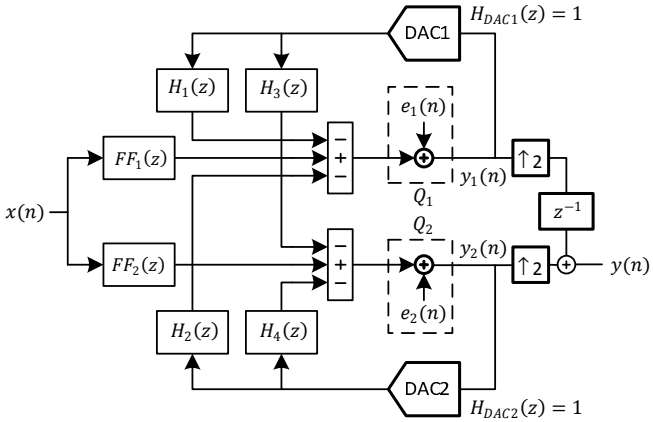


Figure 4: The block diagram of a DTTI ΔΣ modulator.

The conventional ΔΣ modulator is designed through the use of the delta-sigma toolbox from MATLAB to operate at 160MHz clock frequency and OSR of 16. The modulator coefficients are $\{a, b, c\} = \{0.333, 1, 3\}$. The STF and NTFs of the DTTI ΔΣ modulator are given by (20), (21) and (22).

$$STF(z) = z^{-3}(1 + z^{-1}) \quad (20)$$
$$NTF_1(z) = z^{-1}(1 - z^{-1})^3 \quad (21)$$
$$NTF_2(z) = (1 + z^{-1})(1 - z^{-1})^3 \quad (22)$$

Figure 5 compares the STFs of the DT and the DTTI ΔΣ modulator. STF of DT ΔΣ modulator is flat but STF of DTTI ΔΣ modulator has a notch at half sampling frequency resulting from $(1 + z^{-1})$ term in (20). Figure 6 shows the NTFs of the DT and the DTTI ΔΣ modulator. NTFs of the DTTI ΔΣ modulator shape the quantization noise more than the NTF of the DT ΔΣ modulator, however, $NTF_2(z)$ shapes noise less than $NTF_1(z)$ as a result of approximating $y_1(n)$ in (13).

III. SIMULATION RESULTS

The DT and the DTTI ΔΣ modulator have been simulated using the SIMULINK toolbox of MATLAB and all non-idealities such as finite dc gain, slew-rate and bandwidth of the opamps, the DAC mismatches and offsets of the quantizers have been modelled and their effects on the performance of the modulator have been investigated. The quantizers of the

DT and the DTTI ΔΣ modulator have 4bits of resolution in this design. The output spectra of the DT and the DTTI ΔΣ modulator for a 2.4462MHz input and clock frequencies of 160MHz and 320MHz respectively are plotted in Figure 7. The output spectra of the DTTI ΔΣ modulator is shaped more than the conventional DT ΔΣ modulator. The SNDRs of the conventional DT and the DTTI ΔΣ modulator are 64.5dB and 76.5dB respectively. Therefore in this particular case, the SNDRs of the DTTI ΔΣ modulators is improved by 11dB.

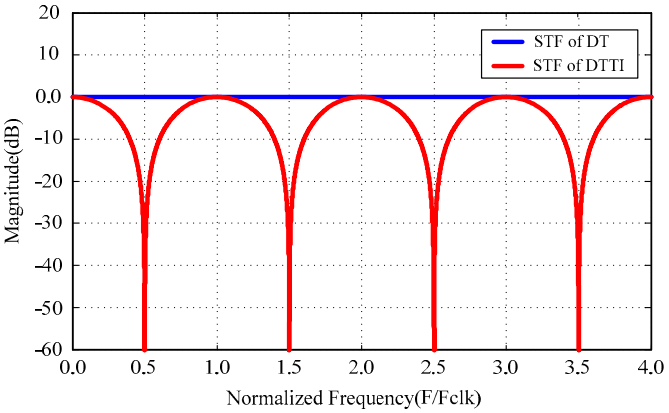


Figure 5: The STFs of the DT and the DTTI ΔΣ modulator.

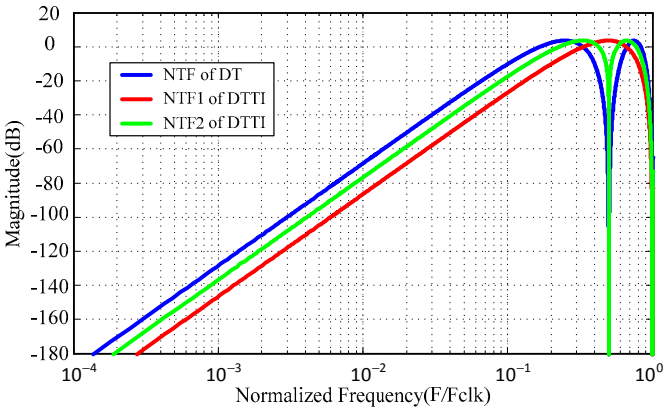


Figure 6: The NTFs of the DT and the DTTI ΔΣ modulator.

IV. CONCLUSION

In this paper a 3rd–order DTTI ΔΣ modulator with shared integrators between two-path and an OSR of 16 has been designed and simulated in the SIMULINK environment of MATLAB to operate at a sampling rate of 320MHz.. All practical non-idealities have been modelled and investigated. To resolve the delayless feedback path issue resulting from sharing integrators between paths, an approximation method has been proposed. The maximum SNDR obtained from the DTTI ΔΣ modulator is 76.5dB which shows an 11dB improvement in comparison with the standard single-loop single-path DT ΔΣ modulator.

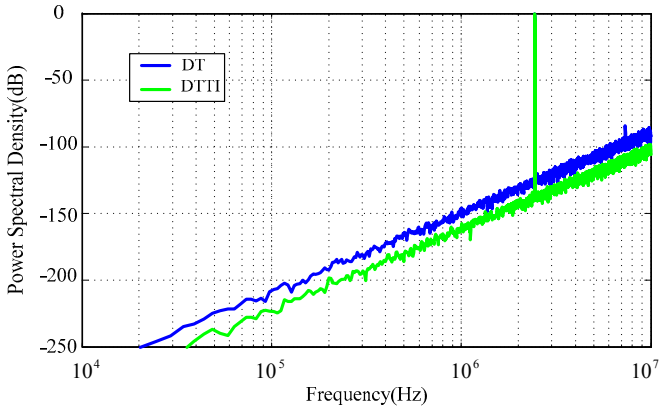


Figure 7: The output spectra of the DT and the DTTI ΔΣ modulator for a 2.4462MHz input with clock frequencies of 160MHz and 320MHz respectively.

V. REFERENCES

[1] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*. Berlin: Springer, 2006.

[2] D. Yang, F. F. Dai, W. N. S. Yin and R. C. Jaeger," Delta-Sigma Modulation for Direct Digital Frequency Synthesis," *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.,* vol. 17, no. 6, pp. 793-802, June 2009.

[3] T. C. Caldwell and D. A. Johns," A Time-Interleaved Continuous-Time ΔΣ Modulator with 20-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits,* vol. 41, no. 7, pp. 1578-1588, July 2006.

[4] R. Khoini-Poorfard, L. B. Lim and D. A. Johns," Time-Interleaved Oversampling A/D Converters: Theory and Practice," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 8, pp. 634-645, Aug. 1997.

[5] A. Gharbiya, T. C. Caldwell and D. A. Johns," High-Speed Oversampling Analog-To-Digital Converters," *International Journal of High Speed Electronics and Systems,* pp. 1-21, 2005.

[6] M. Kozak and I. Kale, "Novel Topologies for Time-Interleaved Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 7, pp. 639–654, Jul. 2000.

[7] Y. Zhang and A. Leuciuc," A 1.8V Continuous-Time Delta-Sigma Modulator with 2.5MHz Bandwidth," *IEEE MWSCAS,* pp. 140-143, 2002.

[8] K. S. Lee, Y. Choi and F. Maloberti," Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator," *IEEE ISCAS,* pp. 473-476, 2004.

[9] A. Gharbiya and D. A. Johns," Combining Multipath and Single-Path Time-Interleaved Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 12, pp. 1224-1228, Dec. 2008.

[10] B. Xia, S. Yan and E. S. Sinencio,"An RC Time Constant Auto-Tuning Structure For High Linearity Continuous-Time Delta-Sigma Modulators and Active Filters," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 11, pp. 2179-2188, Nov. 2004.

[11] K. Lee, S. Kwon and F. Maloberti,"A Power-Efficient Two-Channel Time-Interleaved ΔΣ Modulator for Broadband Applications," *IEEE J. Solid-State Circuits,* vol.42, no.6, pp. 1206-1215, June 2007.

[12] K. Lee and F. Maloberti," Time-Interleaved Sigma-Delta Modulator Using Output Prediction Scheme" *IEEE Trans. Circuits Syst. II*, vol. 51, no. 10, pp. 537-541, Oct. 2004.

[13] M. Kozak, M. Karaman, and I. Kale, "Efficient Architectures for Time-Interleaved Oversampling Delta-Sigma Converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 8, pp. 802–810, Aug. 2000.

[14] A. Gharbiya and D. A. Johns," On The Implementation of Input – Feedforward Delta-Sigma Modulator," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 6, pp. 453-457, June. 2006.

[15] T. C. Caldwell," Time-Interleaved Continuous-Time Delta-Sigma Modulators," MASc Thesis, University of Toronto, Toronto, Ontario, Canada, 2004.

A General Formula for Impulse-Invariant Transformation for Continuous-Time Delta-Sigma Modulators

Jafar Talebzadeh and Izzet Kale
Applied DSP and VLSI Research Group, Department of Electronic Systems,
University of Westminster, London, W1W 6UW, UK
Emails: Jtalebzadeh@gmail.com, kalei@westminster.ac.uk

Abstract, this paper presents a generalised new formula for impulse-invariant transformation which can be used to convert an nth-order Discrete-Time (DT) ΔΣ modulator to an nth-order equivalent Continuous-Time (CT) ΔΣ modulator. Impulse-invariant transformation formulas have been published in many open literature articles for s-domain to z-domain conversion and vice-versa. However, some of the published works contain omissions and oversights. To verify the newly derived formulas, very many designs of varying orders have been tested and a representative 4th-order single-loop DT ΔΣ modulator converted to an equivalent CT ΔΣ modulator through the new formulas are presented in this paper. The simulation results confirm that the CT ΔΣ modulator which has been derived by these formulas works in accordance with the initial DT specifications without any noticeable degradation in performance in comparison to its original DT ΔΣ modulator prototype.

Index Terms — Impulse-Invariant Transformation, Delta-Sigma Modulator, Continuous-Time, Discrete-Time.

I. INTRODUCTION

The ΔΣ modulators are widely used in audio applications and portable devices to achieve high resolution analog-to-digital conversion for relatively low-bandwidth signals by using the oversampling and the noise-shaping techniques. CT ΔΣ modulators have drawn a lot of attention from analog designers over the last decade due to their potential to operate at higher clock frequencies in comparison to their DT counterparts. Sampling requirements are relaxed in the CT ΔΣ modulators because the sampling is inside their loop and any sampling error is shaped by their Noise-Transfer Function (NTF). The CT ΔΣ modulators have an implicit anti-aliasing filter in their forward loop filter. However, CT ΔΣ modulators suffer from several drawbacks: excess loop delay, jitter sensitivity and RC time constant variations.

One way to convert a DT ΔΣ modulator to an equivalent CT ΔΣ modulator is through the use of the impulse-invariant transformation [1]-[6]. A DT ΔΣ modulator and a CT ΔΣ modulator are shown in Figure 1, and are said to be equivalent when their quantizer inputs are equal at the sampling instants.

$$q(n) = q_c(t)|_{t=nT} \quad \text{for all n} \tag{1}$$

Where $q(n)$ and $q(n)$ are the quantizer inputs of the DT and

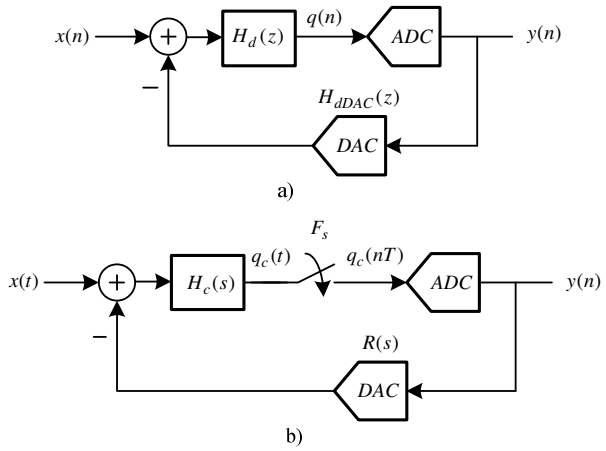


Figure 1: The block diagrams of a) The DT ΔΣ modulator and b) The CT ΔΣ modulator.

CT ΔΣ modulators and T is the clock period of the ΔΣ modulators. This condition would be fulfilled if the impulse responses of the open-loop filter of the CT and DT ΔΣ modulators were equal at the sampling times. As a result (1) translates directly into (2):

$$\mathcal{Z}^{-1}\{H_{dDAC}(z)H_d(z)\} = \mathcal{L}^{-1}\{R(s)H_c(s)\}\big|_{t=nT} \tag{2}$$

Because $H_{dDAC}(z) = 1$, equation (2) can be simplified to give (3):

$$\mathcal{Z}^{-1}\{H_d(z)\} = \mathcal{L}^{-1}\{H_{cDAC}(s)H_c(s)\}|_{t=nT} \tag{3}$$

The transformation in (3) is the well-known impulse-invariant transformation where $\mathcal{Z}^{-1}$, $\mathcal{L}^{-1}$, $R(s)$, $H_d(z)$ and $H_c(s)$ represent the inverse z-transform, the inverse Laplace transform, the CT DAC transfer function, the DT and the CT loop filters respectively [1],[4]. Depending on the output waveform of the CT DAC, there would be an exact mapping between the DT and the CT ΔΣ modulators. The popular feedback-DAC waveforms have rectangular shapes. The time and frequency (Laplace) domain responses of these waveforms are:

$$r_{(\alpha,\beta)}(t) = \begin{cases} 1, & \alpha T \le t \le \beta T, \quad 0 \le \alpha, \beta \le 1 \\ 0, & otherwise \end{cases} \tag{4}$$

$$R(s) = \frac{e^{-\alpha T s} - e^{-\beta T s}}{s} \tag{5}$$

978-1-5090-6508-0/17/$31.00 ©2017 IEEE

In the cases where $\beta > 1$ the DAC equation is divided into two parts as expressed by (6) and the z-domain equivalents of each part is calculated separately.

$$r_{(\alpha,\beta)}(t) = r_{(\alpha,1)}(t) + r_{(0,\beta)}(t-T) \tag{6}$$

This paper is organized as follows. To set the scene, in section II, the concept of the impulse-invariant transformation is reviewed and a general formula for s-domain to z-domain conversion for ΔΣ modulator applications is derived. In section III, simulation results of the 4th-order CT and DT ΔΣ modulators are both presented and discussed in detail. Finally, conclusions are given in section IV.

II. IMPULSE-INVARIANT TRANSFORMATION

In order to derive the equivalent z-domain transfer function of CT ΔΣ modulators with rectangular DAC waveforms, we shall start with the 1st order s-domain term. Equation (7) is derived by substituting (5) and the 1st order s-domain term into (3) as follows.

$$H_{1d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s^2}\right)\Big|_{t=nT}\} \tag{7}$$

An auxiliary variable λ is deployed to derive a general formula step by step. Equation (8) is equal to (7) when $\lambda = 0$ [7], [8]:

$$H_{1d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{(s-\lambda)^2}\right)\Big|_{t=nT}\}\Big|_{\lambda=0} = H_1(z)\Big|_{\lambda=0} \tag{8}$$

By using the Laplace transform properties, (8) leads to (9) where $u(t)$ represents a step function [7].

$$H_1(z) = \mathcal{Z}\left\{e^{\lambda t}(e^{-\alpha\lambda t}(t-\alpha T)u(t-\alpha T) - e^{-\beta\lambda t}(t-\beta T)u(t-\beta T))\Big|_{t=nT}\right\} \tag{9}$$

The continuous time variable t in (9) is replaced with nT in (10).

$$H_1(z) = \mathcal{Z}\left\{e^{\lambda nT}(e^{-\alpha\lambda T}(nT-\alpha T)u(nT-\alpha T) - e^{-\beta\lambda T}(nT-\beta T)u(nT-\beta T))\Big|_{t=nT}\right\} \tag{10}$$

The z-transform of (10) is expressed by (11) which results in (12) [7], [8].

$$H_1(z) = T\sum_{n=0}^{+\infty} e^{\lambda nT}(e^{-\alpha\lambda T}(n-\alpha) - e^{-\beta\lambda T}(n-\beta))z^{-n} \tag{11}$$

$$H_1(z) = T\left\{\frac{(1-\alpha)e^{(1-\alpha)\lambda T} - (1-\beta)e^{(1-\beta)\lambda T}}{(z-e^{\lambda T})} + \frac{e^{(2-\alpha)\lambda T} - e^{(2-\beta)\lambda T}}{(z-e^{\lambda T})^2}\right\} \tag{12}$$

It can be proved that (12) can be obtained by calculating the 1st derivative with respect to the variable λ of equation (13).

$$H_1(z) = \frac{\partial}{\partial\lambda}\left(\frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z - e^{\lambda T}}\right) \tag{13}$$

By substituting $\lambda = 0$ into (12) the z-domain equivalent of the 1st order s-domain term is expressed by (14).

$$H_{1d}(z) = T\left(\frac{\beta-\alpha}{z-1}\right) \tag{14}$$

The z-domain equivalent of the 2nd order s-domain term is derived by repeating all steps in the process mentioned above as follows.

$$H_{2d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s^3}\right)\Big|_{t=nT}\} \tag{15}$$

$$H_{2d}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{(s-\lambda)^3}\right)\Big|_{t=nT}\}\Big|_{\lambda=0} = H_2(z)\Big|_{\lambda=0} \tag{16}$$

$$H_2(z) = \mathcal{Z}\left\{e^{\lambda t}\left(\frac{e^{-\alpha\lambda t}}{2}(t-\alpha T)^2u(t-\alpha T) - \frac{e^{-\beta\lambda t}}{2}(t-\beta T)^2u(t-\beta T)\right)\Big|_{t=nT}\right\} \tag{17}$$

The z-transform of (17) is given by (18) which leads to (19) [7], [8].

$$H_2(z) = \frac{T^2}{2}\sum_{n=0}^{+\infty} e^{\lambda nT}(e^{-\alpha\lambda T}(n-\alpha)^2 - e^{-\beta\lambda T}(n-\beta)^2)z^{-n} \tag{18}$$

$$H_2(z) = \frac{T^2}{2}\left\{\frac{(1-\alpha)^2e^{(1-\alpha)\lambda T} - (1-\beta)^2e^{(1-\beta)\lambda T}}{(z-e^{\lambda T})} + \frac{(3-2\alpha)e^{(2-\alpha)\lambda T} - (3-2\beta)e^{(2-\beta)\lambda T}}{(z-e^{\lambda T})^2} + \frac{2e^{(3-\alpha)\lambda T} - 2e^{(3-\beta)\lambda T}}{(z-e^{\lambda T})^3}\right\} \tag{19}$$

The 2nd derivative of equation (20) with respect to the variable λ is equal to (19).

$$H_2(z) = \frac{1}{2}\frac{\partial^2}{\partial\lambda^2}\left(\frac{e^{(1-\alpha)\lambda T} - e^{(1-\beta)\lambda T}}{z - e^{\lambda T}}\right) \tag{20}$$

Substituting $\lambda = 0$ into (19) gives (21) which is the z-domain equivalent of the 2nd order s-domain term.

$$H_{2d}(z) = T^2\frac{[\beta(\beta-9) - \alpha(\alpha-9)]z + (\beta^2 - \alpha^2)}{2(z-1)^2} \tag{21}$$

Finally, the above-mentioned process is performed all over again for the 3rd and 4th order s-domain terms which are listed in Table I. To obtain the kth order s-domain term, the impulse-invariant transformation is written in (22).

$$H_{kd}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts} - e^{-\beta Ts}}{s^{k+1}}\right)\Big|_{t=nT}\} \tag{22}$$

Table I: The CT-to-DT transformation for rectangular DAC waveforms.

s-domain	z-domain equivalent for a rectangular DAC waveform	
	Proposed Formulas	Formulas in [4]
1	$[u(-\alpha T)-u(-\beta T)]+[u(T-\alpha T)-u(T-\beta T)]$	
$\frac{1}{sT}$	$\frac{y_0}{z-1}$ $y_0=\beta-\alpha$	$\frac{y_0}{z-1}$ $y_0=\beta-\alpha$
$\frac{1}{s^2T^2}$	$\frac{y_1z+y_0}{(z-1)^2}$ $y_0=\frac{1}{2}(\beta^2-\alpha^2)$ $y_1=\frac{1}{2}(\beta(2-\beta)-\alpha(2-\alpha))$	$\frac{y_1z+y_0}{(z-1)^2}$ $y_0=\frac{1}{2}(\beta^2-\alpha^2)$ $y_1=\frac{1}{2}(\beta(1-\beta)-\alpha(1-\alpha))$
$\frac{1}{s^3T^3}$	$\frac{y_2z^2+y_1z+y_0}{(z-1)^3}$ $y_0=\frac{1}{6}(\beta^3-\alpha^3)$ $y_1=-\frac{1}{3}(\beta^3-\alpha^3)+\frac{1}{2}(\beta^2-\alpha^2)+\frac{1}{2}(\beta-\alpha)$ $y_2=+\frac{1}{6}(\beta^3-\alpha^3)-\frac{1}{2}(\beta^2-\alpha^2)+\frac{1}{2}(\beta-\alpha)$	$\frac{y_2z^2+y_1z+y_0}{(z-1)^3}$ $y_0=\frac{1}{6}(\beta^3-\alpha^3)$ $y_1=-\frac{1}{3}(\beta^3-\alpha^3)+\frac{1}{2}(\beta^2-\alpha^2)+\frac{1}{2}(\beta-\alpha)$ $y_2=-\frac{1}{6}(\beta^3-\alpha^3)-\frac{1}{2}(\beta^2-\alpha^2)+\frac{1}{2}(\beta-\alpha)$
$\frac{1}{s^4T^4}$	$\frac{y_3z^3+y_2z^2+y_1z+y_0}{(z-1)^3}$ $y_0=\frac{1}{24}(\beta^4-\alpha^4)$ $y_1=-\frac{1}{8}(\beta^4-\alpha^4)+\frac{1}{6}(\beta^3-\alpha^3)+\frac{1}{4}(\beta^2-\alpha^2)+\frac{1}{6}(\beta-\alpha)$ $y_2=+\frac{1}{8}(\beta^4-\alpha^4)-\frac{1}{3}(\beta^3-\alpha^3)+\frac{2}{3}(\beta-\alpha)$ $y_3=-\frac{1}{24}(\beta^4-\alpha^4)+\frac{1}{6}(\beta^3-\alpha^3)-\frac{1}{4}(\beta^2-\alpha^2)+\frac{1}{6}(\beta-\alpha)$	$\frac{y_3z^3+y_2z^2+y_1z+y_0}{(z-1)^3}$ $y_0=\frac{1}{24}(\beta^4-\alpha^4)$ $y_1=-\frac{1}{8}(\beta^4-\alpha^4)+\frac{1}{6}(\beta^3-\alpha^3)+\frac{1}{4}(\beta^2-\alpha^2)+\frac{1}{6}(\beta-\alpha)$ $y_2=+\frac{1}{8}(\beta^4-\alpha^4)-\frac{1}{3}(\beta^3-\alpha^3)+\frac{2}{3}(\beta-\alpha)$ $y_3=-\frac{1}{24}(\beta^4-\alpha^4)+\frac{1}{6}(\beta^3-\alpha^3)-\frac{1}{4}(\beta^2-\alpha^2)+\frac{1}{6}(\beta-\alpha)$
$\frac{1}{s^kT^k}$	$\frac{1}{T^kk!}\frac{\partial^k}{\partial\lambda^k}\left(\frac{e^{(1-\alpha)\lambda T}-e^{(1-\beta)\lambda T}}{z-e^{\lambda T}}\right)\Big\|_{\lambda=0}$	

By utilizing the Laplace transform properties, (22) leads to (23) [9].

$$H_2(z)=\mathcal{Z}\left\{e^{\lambda t}\left(\frac{e^{-\alpha\lambda t}}{k!}(t-\alpha T)^k u(t-\alpha T)-\frac{e^{-\beta\lambda t}}{k!}(t-\beta T)^k u(t-\beta T)\right)\Big|_{t=nT}\right\} \quad (23)$$

The z-domain equivalent for the kth order s-domain function is expressed by (24) where k represents the order of the s-domain term.

$$H_{kd}(z)=\left(\frac{1}{k!}\frac{\partial^k}{\partial\lambda^k}\left(\frac{e^{(1-\alpha)\lambda T}-e^{(1-\beta)\lambda T}}{z-e^{\lambda T}}\right)\right)\Big|_{\lambda=0} \quad (24)$$

The z-domain equivalent for the 1st to 4th and the general kth order s-domain terms for a rectangular DAC waveform are presented in Table I.

One popular method to compensate the excess loop delay in CT ΔΣ modulators is to deploy negative feedback from the output of the DACs to the input of their quantizers as shown in Figure 2.b [1].

The z-domain equivalent of this feedback ($H_c(s)=1$) is developed and given by (26) as follows.

$$H_{0d}(z)=\mathcal{Z}\left\{\mathcal{L}^{-1}\left(\frac{e^{-\alpha Ts}-e^{-\beta Ts}}{s}\right)\Big|_{t=nT}\right\}=\sum_{n=0}^{+\infty}(u(nT-\alpha T)-u(nT-\beta T))z^{-n} \quad (25)$$

$$H_{0d}(z)=u(-\alpha T)-u(-\beta T)+(u(T-\alpha T)-u(T-\beta T))z^{-1} \quad (26)$$

One popular rectangular DAC waveform is the Non-Return-to-Zero (NRZ) one. The z-domain equivalent of the NRZ DAC with $\alpha=\tau_d$ and $\beta=1+\tau_d$ is calculated from (26) and is given by (27).

$$H_{0d}(z)=z^{-1} \quad (27)$$

The newly derived z-domain equivalent formulas can be compared with the formulas in [4] which both are illustrated in Table I. The results of this comparison indicate that y_1 in 2nd-order term and y_2 in 3rd-order term are entirely different. The comparison can be done between the newly mentioned formulas and the ones presented in [1] which show y_1 in 3rd-order term are not the same. What is surprising is that even z-domain equivalent formulas in [1] and [4] are not identical and y_1 in 2nd-order term and y_1 and y_2 in 3rd-order term are completely different.

III. SIMULATION RESULTS

To validate the newly derived formulas presented in Table I, a 4th-order DT ΔΣ modulator with an OverSampling Ratio (OSR) of 64 and 3-bit quantizer has been designed by using the Schreier toolbox and was then converted to its 4th-order CT ΔΣ modulator equivalent with a NonReturn-to-Zero (NRZ) DAC waveform by using DT-to-CT formulas described in Table I. The block diagrams of the 4th-order DT and CT ΔΣ modulator are shown in Figure 2. An extra feedback of f_{c0} is used to compensate the effect

of excess loop delay in the CT ΔΣ modulator. The coefficients of the DT ΔΣ modulator are given in (36).

$$\{a, b, c, d\} = \{0.1798, 0.4384, 0.8769, 2.0\} \quad (36)$$

By using Table I the coefficients of the equivalent 4th-order CT ΔΣ modulator with NRZ DAC and $\{\alpha, \beta\} = \{0.2, 1.2\}$ shown in Figure 2.b have been derived and presented in (37).

$$\{f_{c4}, f_{c3}, f_{c2}, f_{c1}, f_{c0}\} = \{1.6189, 1.2266, 0.5892, 0.1382, 0.3\} \quad (37)$$

Both modulators have been simulated by using the Mathworks SIMULINK environment and a sinusoidal input signal with amplitude of 0.7V and a frequency of 61.34 KHz is applied to both modulators in the simulation. The simulation results show that the SNR of the DT and CT ΔΣ modulators are about 130.37dB and 130.21dB respectively with a clock frequency of 80MHz and signal bandwidth of 625 KHz. The output spectra of the DT and CT ΔΣ modulators and their respective in-band noise are approximately the same as shown in Figure 3.

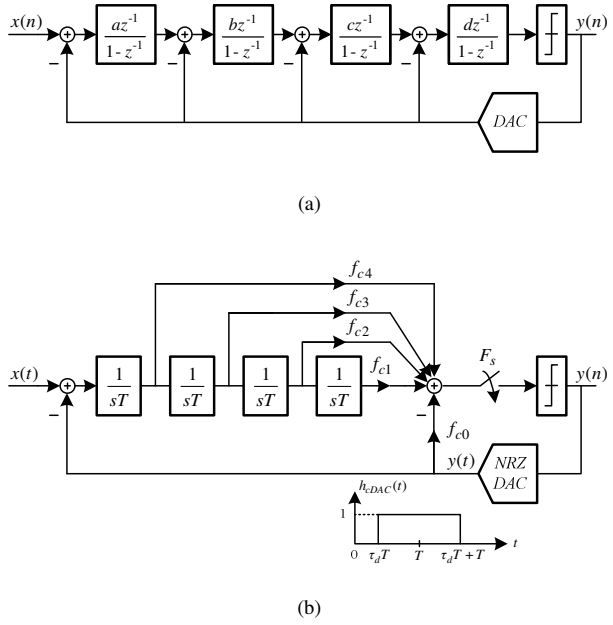


Figure 2: a) The block diagram of the fourth-order DT ΔΣ modulator and b) The block diagram of the fourth-order CT ΔΣ modulator.

IV. CONCLUSION

In this paper a general and novel formula for impulse invariant transformation is presented. The CT-to-DT conversion formulas for the 1st to 4th order terms are derived and listed in Table I. The 4th-order DT ΔΣ modulator and its 4th-orde CT modulator equivalent which is derived by these formulas both were simulated by using MATLAB. Similar simulation results for both modulators support the validity of the proposed formulas derived and described in this paper.

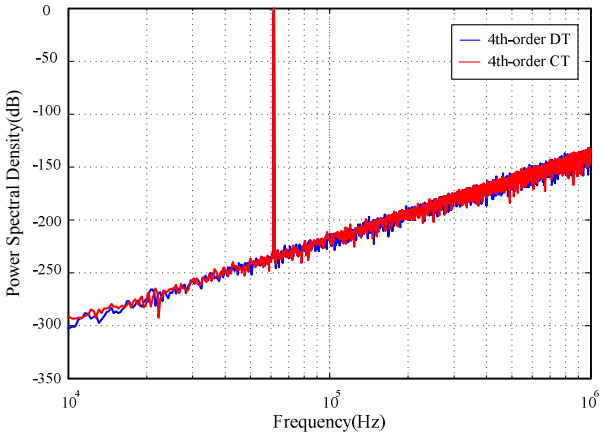


Figure 3: The output spectra of the fourth-order DT and CT ΔΣ modulators for a 61.34 KHz input with a clock frequency of 80MHz.

REFERENCES

[1] J. A. Cherry, and W. M. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 4, pp. 376-389, April 1999.

[2] M. Ortmanns, F. Gerfers, and Y. Manoli, "A Case Study on a 2-1-1 Cascaded Continuous-Time Sigma-Delta Modulators, "*IEEE Trans. Circuits Syst. I*, vol. 52, no. 8, pp. 1515-1525, Aug. 2005.

[3] H. Shamsi, O. Shoaei, "Continuous- Time Delta-Sigma Modulators with Arbitrary DAC Waveforms, "*IEEE ISCAS,* pp. 187-190, 2006.

[4] M. Ortmanns and F. Gerfers, "Continuous-Time Sigma-Delta A/D Conversion, "*Berlin: Springer*, 2006.

[5] T. Kim, C. Han and, N. Maghari, "A 7.2mW 75.3dB SNDR 10MHz BW CT Delta-Sigma Modulator Using GM-C Based Noise-Shaped Quantizer and Digital Integrator" *IEEE J. Solid-State Circuits,* vol. 51, no. 8, pp. 1840-1850, 2016.

[6] H. Chae, and M. P. Flynn, "A 69dB SNDR, 25MHz BW, 800 MS/s Continuous-Time Bandpass Delta Sigma Modulator Using Duty-Cycle-Controlled DAC for Low Power and Reconfigurability" *IEEE J. Solid-State Circuits,* vol. 51, no. 3, pp. 649-659, 2016.

[7] E. I. Jury, "Theory and Application of the z-Transform Method," *New York, Robert E. Krieger Publishing Co.,* 1973.

[8] P. P. G. Dyke, "An introduction to Laplace Transforms and Fourier Series," *Great Britain, Springer*, 2004

[9] Benabes, P., Keramat, M., Kielbasa, R., "A methodolgy for designing countinuous-time sigma-delta modulators" Analog. Int. Circuits Signal Process. 123(3), 189–200 June, 2000.

A 28mW 320MHz 3rd–Order Continuous-Time Time-Interleaved Delta-Sigma Modulator with 10MHz Bandwidth and 12 Bits of Resolution

Jafar Talebzadeh, Izzet Kale
Applied DSP & VLSI Research Group
Department of Engineering
University of Westminster London, W1W 6UW, UK
e-mails: Jtalebzadeh@gmail.com, kalei@westminster.ac.uk

***Abstract*—this paper presents a 3rd-order two-path Continuous-Time Time-Interleaved (CTTI) delta-sigma modulator which is implemented in standard 90nm CMOS technology. The architecture uses a novel method to solve the delayless feedback path issue arising from the sharing of integrators between paths. The clock frequency of the modulator is 320MHz but integrators, quantizers and DACs operate at 160MHz. The modulator achieves a dynamic range of 12 bits over a bandwidth of 10MHz and dissipates only 28mW of power from a 1.8-V supply.**

Keywords-time-interleaved; ΔΣ modulator; signal-to-noise ratio

I. INTRODUCTION

The rapid growth of the portable communication device markets such as audio systems and consumer electronics has led to an increasing demand for ADC designs with bandwidths up to 10-20MHz and medium resolutions of 10 to 12 bits [1]. In this paper we present an ADC which has potential to operate at high sampling rate with medium resolution.

The signal bandwidth ΔΣ modulators can deal with is narrow and restricted by the OverSampling Ratio (OSR) and technology deployed. The maximum achievable sampling rate in Discrete-Time (DT) ΔΣ modulator*s which are implemented using Switched-Capacitor (SC) techniques, is approximately 100-200MHz [1] but for Continuous-Time (CT)* ΔΣ modulator*s which are implemented through the use of active-RC or gm-c filters [2], a maximum sampling rate of 300-400MHz is indeed feasible [3].*

By using the time-interleaving technique and M interconnected parallel modulators that are working concurrently, the effective sampling rate and the OSR becomes M times the clock rate and the OSR of each modulator respectively [4],[5],[6]. It should be noted that the required resolution can be acquired without increasing the order of the modulator or the number of bits for the quantizer and also without utilizing a state of the art technology.

By using time-interleaving techniques and CT loop filters, a 3rd-order CTTI ΔΣ modulator *is designed. One set of integrators is shared between paths in order to save the power dissipation, silicon area and to eliminate the instability arising from DC offset mismatch of the two individual integrator sets based the two-channel interleaving case [5].*

This paper is organized as follows. In section II, a two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator *is derived from a 3rd-order conventional DT* ΔΣ modulator *using the time domain equations and then it is converted to a CTTI* ΔΣ modulator*. The delayless feedback path problem and our proposed solution are both discussed in detail in this section. In section III, MATLAB simulation results are presented. In section IV, circuit design of the modulator is discussed. Finally, conclusions are given in section V.*

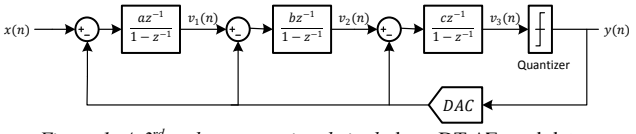


*Figure 1. A 3rd-order conventional single-*loop DT ΔΣ modulator.

II. DERIVATION OF TIME-INTERLEAVED ΔΣ MODULATOR

The 3rd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator is derived directly from the *time domain node equations of the* conventional DT ΔΣ *modulator as shown in Figure 1. The general method was described in detail in [7]. It is assumed that the DAC in the feedback loop is ideal ($H_{DAC}(z)=1$).The time domain equations of the modulator are written for two consecutive time slots as (2n)th and (2n+1)th and by sharing only one set of integrators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. Equation sets (1) and (2) are derived as follows:*

$$v_{11}(n) = ax(n) \quad - ay_2(n) + v_{12}(n) \qquad (1.a)$$
$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \qquad (1.b)$$
$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \qquad (1.c)$$
$$y_1(n) = Q[v_{31}(n)] = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \qquad (1.d)$$

and

$$v_{12}(n) = ax(n-1) \quad - ay_1(n-1) + v_{11}(n-1) \qquad (2.a)$$
$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \qquad (2.b)$$
$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \qquad (2.c)$$
$$y_2(n) = Q[v_{32}(n)] \qquad (2.d)$$

where $Q[.]$ represents the quantization function. Equation set (3) is derived by further substituting equation set (1) into equation set (2).

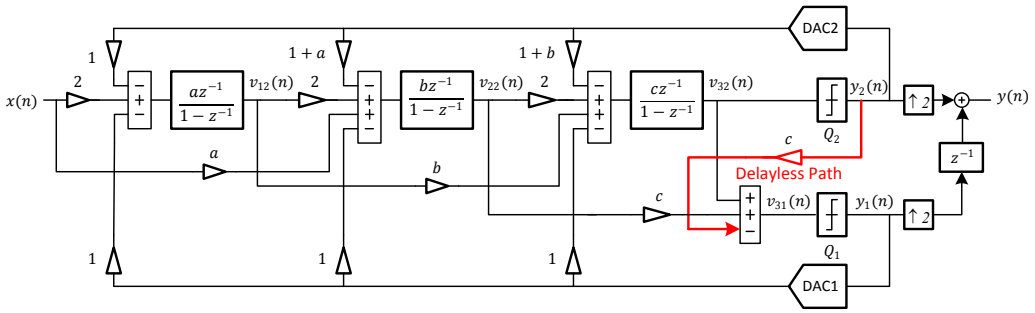


*Figure 2. A 3rd-order two-*path DTTI ΔΣ modulator *with shared integrators.*

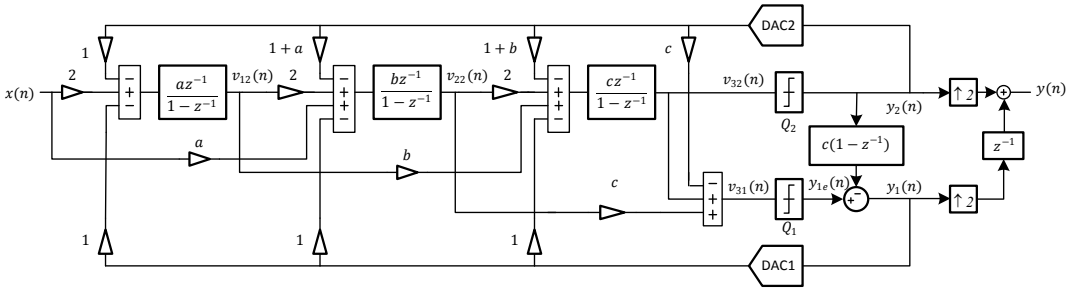


*Figure 3. The proposed 3rd-order two-*path DTTI ΔΣ modulator *with shared integrators.*

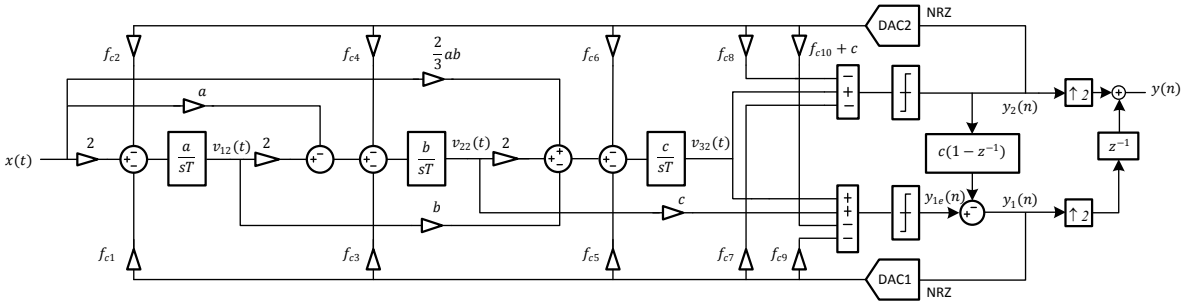


*Figure 4. The proposed 3rd-order two-*path CTTI ΔΣ modulator *with shared integrators.*

$$v_{12}(n) = 2ax(n-1) - ay_1(n-1) - ay_2(n-1) + v_{12}(n-1) \quad (3.a)$$

$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \quad (3.b)$$

$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - cy_1(n-1) - c(1+b)y_2(n-1) + v_{32}(n-1) \quad (3.c)$$

The DTTI ΔΣ modulator which is shown in Figure 2 is *derived directly from the time domain equation sets (1) and (3).*

A. Delayless Feedback Path Issue in TI ΔΣ Modulators

*In order to save power, silicon area and to eliminate the instability arising from DC offset mismatch of the individual integrator sets in multi-*path TI ΔΣ *modulators, one set of integrators is shared between paths but it causes a problem which is called the "delayless feedback path" problem. In* DTTI ΔΣ modulator which is shown in Figure 2 and *expressed by equation (1.c) in which* $v_{31}(n)$ *(the input of quantizer Q1) is directly linked to* $y_2(n)$*. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay [8]. The novel method proposed in this paper resolves this issue and is based on an error correction technique. We intentionally induce an error in the analog domain through the use of the output of DAC2 as shown in Figure 3. Quantizer Q1 quantizes the signal* $v_{31}(n)$ *as follows:*

$$y_1(n) = Q[v_{31}(n)] \quad (4)$$

Equation (5) is derived by substituting (1.c) into (4):

$$y_1(n) = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \quad (5)$$

The output of DAC2 is used in (6) and equation (5) is rewritten as:

$$y_1(n) = Q[cv_{22}(n) - cy_2(n-1) + v_{32}(n)] + cy_2(n-1) - cy_2(n) \quad (6)$$

The output of Q1 is called $y_{1e}(n)$ *in (7):*

$$y_1(n) = y_{1e}(n) + cy_2(n-1) - cy_2(n) \quad (7)$$

$$error = c\Delta y = c(y_2(n) - y_2(n-1)) \quad (8)$$

$$Y_1(z) = Y_{1e}(z) - c(1 - z^{-1})Y_2(z) \quad (9)$$

As stated in (7), $y_{1e}(n)$ (the output of Q1) requires to be corrected before it is applied to the input of DAC1; otherwise it causes instability in the modulator as it will change the modulators dynamics by increasing its order. A first order differencer block $(1 - z^{-1})$ is used to perform this correction as described in (9). The proposed 3rd-order two-path DTTI ΔΣ modulator *with shared integrator is shown in Figure 3.*

B. Derivation of CTTI ΔΣ Modulator

The CTTI ΔΣ modulator *equivalent of the DTTI* ΔΣ *modulator of Figure 3 can be obtained in three steps as follows: The first step is to determine the DT loop filters of the DTTI* ΔΣ modulator. *The second step is to convert the DT loop filters into equivalent CT loop filters by using the impulse-invariant transformation [1],[4],[6]. The third step is to convert the modulator into a 3rd order CTTI* ΔΣ modulator *as shown in Figure 4. Two DACs with Non-Retrun-To-Zero (NRZ) implementation and intentional delay of* $0.25T$ $(T = 1/160MHz)$ *have been used. To overcome the excess-loop delay issue, two additional feedback paths from the outputs of DAC1 and DAC2 to the inputs of each quantizer (Q1 and Q2) are used.*

III. MATLAB Simulation

The proposed CTTI ΔΣ modulator has been simulated *using the SIMULINK toolbox of MATLAB. All specifications of the* CTTI ΔΣ modulator *are as follows.*

$\{a, b, c\} = \{0.27639, 0.76393, 2.0\}$

$\{f_{c1}, f_{c3}, f_{c5}, f_{c7}, f_{c9}\} = \{1.0, 1.0, 0.9648, 0.6708, 1.3291\}$

$\{f_{c2}, f_{c4}, f_{c6}, f_{c8}, f_{c10}\} = \{1.0, 1.2764, 1.7287, 1.3291, 2.1986\}$

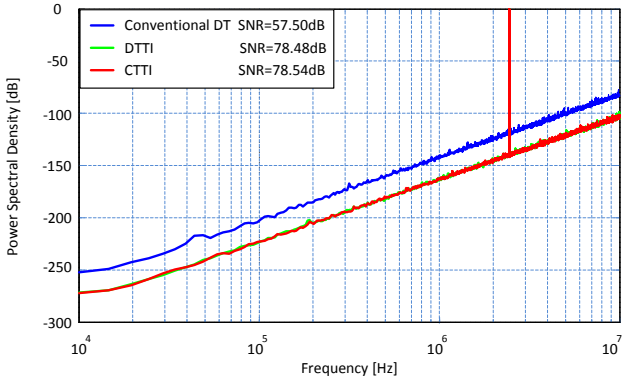


Figure 5. The output spectra of the conventional DT, the DTTI and the CTTI ΔΣ *modulator for a 2.4462MHz input with clock frequencies of 160MHz, 320MHz and 320MHz respectively.*

The output spectrum of this CTTI ΔΣ modulator is compared with the conventional DT and the DTTI ΔΣ *modulators in Figure 5. The output spectra of the DTTI and* CTTI ΔΣ modulators are the same and their in-*band noise are shaped more than the conv*entional DT ΔΣ modulator. The *SNDRs* of the conventional DT, the DTTI and CTTI ΔΣ *modulators are 57.50dB, 78.47dB and 78.54dB respectively. Therefore in this particular case, the SNDRs of the time-*interleaved ΔΣ modulators are *improved by 21dB. As can be seen in Figure 5, non-idealities have not been included in this comparison.*

IV. Circuit Design and Simulation

The modulator circuit has been designed using the 90nm CMOS TSMC technology with the supply voltage of 1.8-V. Figure 6 shows the block diagram of the 3rd-order two-path CTTI ΔΣ *modulator. The operating frequency of the two quantizers, DACs and all other blocks except for the output multiplexer is 160MHz but the output multiplexer operates at 320MHz. The OSR of the modulator is 16, allowing a maximum input signal bandwidth of 10MHz. The major circuit blocks of the modulator include three active-RC integrators, ten 4-bit current steering DACs, one 4-bit and one 5-bit flash ADC, two summation circuits, a clock generator, a biasing circuit, an output multiplexer and a digital error correction block $(1 - z^{-1})$.*

As can be seen in Figure 6, three active-RC integrators have been used and RC time constant varies up to 50% in CMOS technologies. A tuneable capacitor array will be used to tune up the RC time constant of the integrators and to compensate for process variations.

One popular opamp architecture is a two-stage Miller-compensation opamp which has been utilized for the first, second and third integrator and opamp4 and is shown in Figure 7. A PMOS input differential pair is used as the input stage for two reasons: First, the second pole is determined by the transconductance of the input transistors of the second stage and the NMOS transistor is faster than the PMOS one therefore the whole opamp will be more stable. Second, the input and output common mode voltage of the opamp is set to be 0.8V instead of VDD/2 (0.9V). The tail transistor in the first stage will have more VDS voltage and will not be pushed to triode region. The benefit of using PMOS transistors as input in the differential pair is low flicker noise, but in our wideband design, the flicker noise is of less concern.

This modulator requires two ADCs. The first ADC has 5bit resolution and 31 comparators and the second ADC has 4bit resolution and 15 comparators. As shown in Figure 8, each latched comparator is composed of a single preamplifier stage and a latch. The preamplifier is used to amplify the input signal and to minimize the input capacitance of the comparator. The preamplifier stage isolates the latch and the resistor ladder; therefore it reduces the kick-back noise seen in reference string during switching times of the comparator. The latch is used to compare the two amplified input signals comping from the preamplifier and to provide a digital rail-to-rail output signal.

The whole CTTI ΔΣ *modulator has been simulated with a $F_{in} = 1.005MHz$ input frequency, $1.6V_{pp}$ (-2dBFS) amplitude and 320MHz sampling rate across process corners and temperatures. Due to the excessive long simulation times, these circuit simulation results were obtained by using only 16384-point FFTs. Since the signal bandwidth is 10MHz, up to 512 frequency bins will be included in the calculation of*

the SNDR. The circuit-level simulations have been run to make sure that the modulator is stable across process corners and temperatures. The SNDR of the modulator obtained from circuit simulations in TT 27'C, FF 120'C and SS -40'C *are 75.3dB, 75.9dB and 74.5dB respectively.*

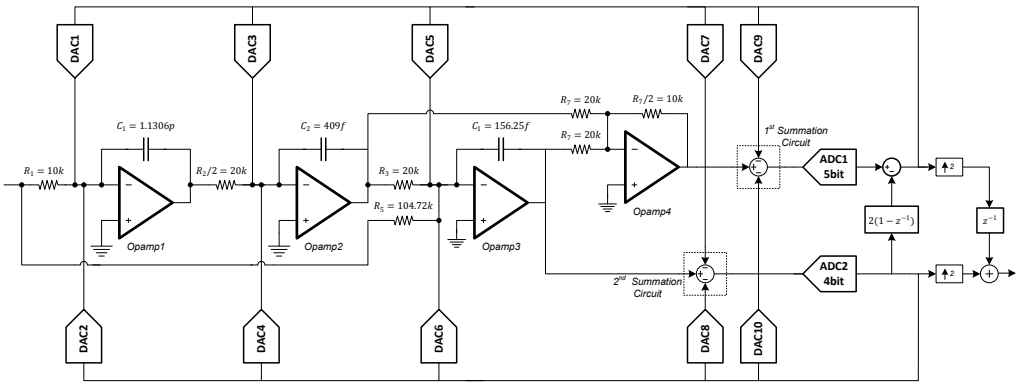
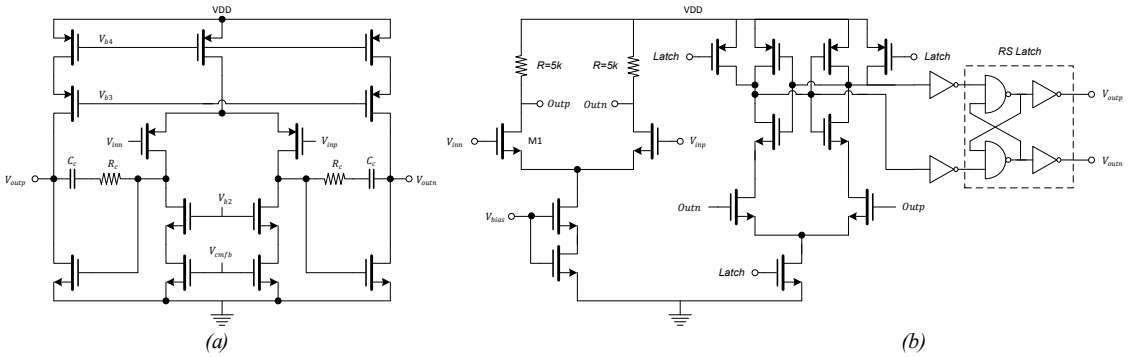


Figure 6. Block Diagram of the 3rd-order CTTI ΔΣ Modulator.



(a) (b)

Figure 7. Schematic of (a) opamp and (b) comparator of the 3rd-order CTTI ΔΣ Modulator.

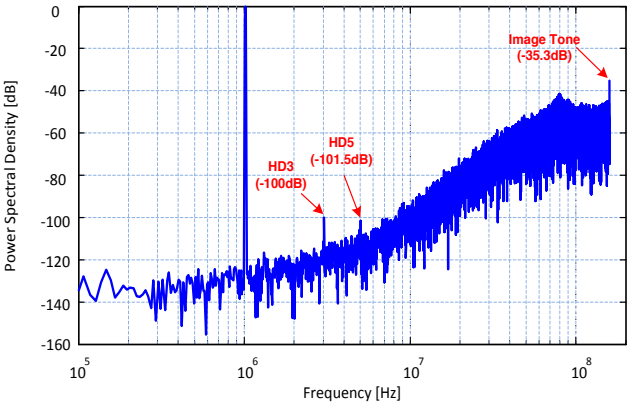


Figure 8. The output spectra of the CTTI ΔΣ modulator for a *1.005MHz input with clock frequencies of 320MHz simulated in TT corner and 27'C.*

The output spectrum obtained from the circuit simulation at TT corner and 27'C temperature is shown in Figure *8. From the output spectrum shown in Figure 8, it can be seen that big tones reside at around the half clock frequency (160MHz). Those tones are images and are created due to utilizing the time-interleaving technique in the modulator. Those tones are dangerous because they will fold the out-of-band noise into the band of interest and hence increase the in-band noise floor. The image tone located at* $0.5F_{clk} - F_{in}$ *has -35.3dB amplitude and should be attenuated enough in the decimation filter following this modulator.*

V. CONCLUSION

In this paper the design of a 3rd-order CTTI ΔΣ modulator with one set of integrators in 90nm CMOS technology has been presented. A novel method to resolve the delayless feedback path issue has been proposed [9]. The results obtained from the circuit simulation confirm that the theory behind the proposed method works very well without any degradation in the output performance.

REFERENCES

[1] *M. Ortmanns and F. Gerfers, Continuous-Time Sigma-Delta A/D Conversion. Berlin: Springer, 2006.*

[2] T. Kim, C. Han and N. Maghari, "A 7.2mW 75.3dB SNDR 10MHz *BW CT Delta-Sigma Modulator Using GM-C-Based Noise –Shaped* Quantizer and Digital Integrator" *IEEE J. Solid-State Circuits, vol. 51, no. 8, pp. 1840-1850, 2016.*

[3] X. Liu, M. Andersson, and L. Sundstom, "An 11mW continuous time *delta*-sigma modulator with 20MHz bandwidth in 65nm CMOS" *IEEE ISCAS pp. 2337-2340, 2014.*

[4] T. C. Caldwell and D. A. Johns," A Time-*Interleaved Continuous*-Time ΔΣ Modulator with 20-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits, vol. 41, no. 7, pp. 1578-1588, July 2006.*

[5] *R. Khoini*-Poorfard, L. B. Lim and D. A. Johns," Time-*Interleaved* Oversampling A/D Converters: Theory and Practice," *IEEE Trans. Circuits Syst. II, vol. 44, no. 8, pp. 634-645, Aug. 1997.*

[6] X. Meng, Y.Zhang, T. He and G.C. Temes,"A noise-*coupled time-interleaved delta*-sigma modulator with shifted loop delays" IEEE *ISCAS pp. 2045-2048, 2015.*

[7] M. Kozak and I. Kale, "Novel Topologies fo*r Time-Interleaved Delta*-Sigma Modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 47, no. 7, pp. 639–654, Jul. 2000.*

[8] K. S. Lee, Y. Choi and F. Maloberti," Domino Free 4-*Path Time-Interleaved Second Order Sigma*-Delta Modulator," *IEEE ISCAS, pp. 473-476, 2004.*

[9] J. Talebzadeh and I. Kale, "Delta-Sigma Modulator," UK Pa*tent GB2524547, March 26, 2014.*

A Novel Two-Channel Continuous-Time Time-Interleaved 3rd-order Sigma-Delta Modulator with Integrator-Sharing Topology

Jafar Talebzadeh, Izzet Kale
Applied DSP & VLSI Research Group, University of Westminster London, W1W 6UW, UK
Emails: Jtalebzadeh@gmail.com, kalei@westminster.ac.uk

Abstract: this paper presents a 3rd-order two-path Continuous-Time Time-Interleaved (CTTI) delta-sigma modulator which is implemented in standard 90nm CMOS technology. The architecture uses a novel method to resolve the delayless feedback path issue arising from the sharing of integrators between paths. The clock frequency of the modulator is 320MHz but integrators, quantizers and DACs operate at 160MHz. The modulator achieves a dynamic range of 12 bits over a bandwidth of 10MHz and dissipates only 28mW of power from a 1.8-V supply.

In order to derive the 3rd-order CTTI ΔΣ modulator, the 3rd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator is derived directly from the time domain node equations of the conventional DT ΔΣ modulator as shown in Figure 1. The time domain equations of the conventional DT ΔΣ modulator are written for two consecutive time slots as (2n)th and (2n+1)th and by sharing only one set of integrators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. The DTTI ΔΣ modulator which is shown in Figure 2 is derived directly from the time domain equation sets (1).

$$v_{12}(n) = 2ax(n-1) - ay_1(n-1) - ay_2(n-1) + v_{12}(n-1) \quad (1.a)$$
$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \quad (1.b)$$
$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - cy_1(n-1) - c(1+b)y_2(n-1) + v_{32}(n-1) \quad (1.c)$$
$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \quad (1.d)$$
$$y_1(n) = Q[v_{31}(n)] = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \quad (1.e)$$
$$y_2(n) = Q[v_{32}(n)] \quad (1.f)$$

In order to save power, silicon area and to eliminate the instability arising from DC offset mismatch of the individual integrator sets in multi-path TI ΔΣ modulators, one set of integrators is shared between paths but it causes a problem which is called the "*delayless feedback path*" problem. In DTTI ΔΣ modulator which is shown in Figure 2 and expressed by equation (1.d) in which $v_{31}(n)$ (the input of quantizer Q1) is directly linked to $y_2(n)$. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay. The novel method proposed in this paper resolves this issue and is based on an error correction technique. We intentionally induce an error in the analog domain through the use of the output of DAC2 which is $y_2(n-1)$ instead of $y_2(n)$ as shown in Figure 3. The output of DAC2 is used in (1.e) and equation (2) is rewritten as:

$$y_1(n) = Q[cv_{22}(n) - cy_2(n-1) + v_{32}(n)] + cy_2(n-1) - cy_2(n) \quad (2)$$

The output of Q1 is called $y_{1e}(n)$ in (3):

$$y_1(n) = y_{1e}(n) + cy_2(n-1) - cy_2(n) \quad (3)$$
$$error = c\Delta y = c(y_2(n) - y_2(n-1)) \quad (4)$$
$$Y_1(z) = Y_{1e}(z) - c(1-z^{-1})Y_2(z) \quad (5)$$

As stated in (3), $y_{1e}(n)$ (the output of Q1) requires to be corrected before it is applied to the input of DAC1 otherwise it causes instability in the modulator; A first order differencer block $(1-z^{-1})$ is used to perform this correction as described in (5). The proposed 3rd-order two-path DTTI ΔΣ modulator with shared integrator is shown in Figure 3.

The CTTI ΔΣ modulator equivalent of the DTTI ΔΣ modulator of Figure 3 can be obtained in three steps as follows: The first step is to determine the DT loop filters of the DTTI ΔΣ modulator. The second step is to convert the DT loop filters into equivalent CT loop filters by using the impulse-invariant transformation. The third step is to convert the modulator into a 3rd order CTTI ΔΣ modulator as shown in Figure 4. Two DACs with Non-Retrun-To-Zero (NRZ) implementation and intentional delay of $0.25T$ ($T = 1/160MHz$) have been used. To overcome the excess-loop delay issue, two additional feedback paths from the outputs of DAC1 and DAC2 to the inputs of each quantizer (Q1 and Q2) are used. The proposed CTTI ΔΣ modulator has been simulated using the SIMULINK toolbox of MATLAB. The output spectrum of this CTTI ΔΣ modulator is compared with the conventional DT and the DTTI ΔΣ modulators in Figure 5. The SNDRs of the conventional DT, the DTTI and CTTI ΔΣ modulators are 57.50dB, 78.47dB and 78.54dB respectively. Therefore in this particular case, the SNDRs of the time-interleaved ΔΣ modulators are improved by 21dB.

The modulator circuit has been designed using the 90nm CMOS TSMC technology with the supply voltage of 1.8-V. Figure 6 shows the block diagram of the 3rd-order two-path CTTI ΔΣ modulator. One popular opamp architecture is a two-stage Miller-compensation which has been utilized for the first, second and third integrator and opamp4 and is shown in Figure 7. This modulator requires two ADCs. The first ADC has 5bit resolution and 31 comparators and the second ADC has 4bit resolution and 15 comparators. As shown in Figure 8, each latched comparator is composed of a single preamplifier stage and a latch. The whole CTTI ΔΣ modulator has been simulated with a $F_{in} = 1.005MHz$ input frequency, $1.6V_{pp}$ (-2dBFS) amplitude and 320MHz sampling rate across process corners and temperatures. The output spectrum obtained from the circuit simulation at TT corner and 27'C temperature is shown in Figure 8. The results obtained from the circuit simulation confirm that the theory behind the proposed method works very well without any degradation in the output performance.

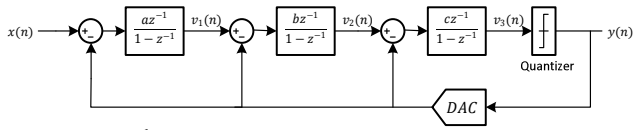


Figure 1. A 3rd-order conventional single-loop DT ΔΣ modulator.

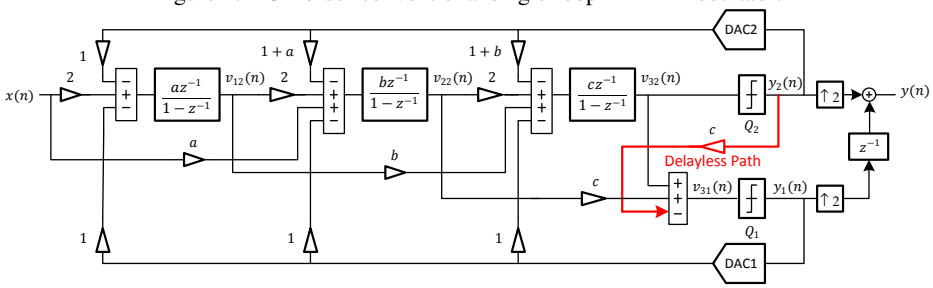


Figure 2. A 3rd-order two-path DTTI ΔΣ modulator with shared integrators.

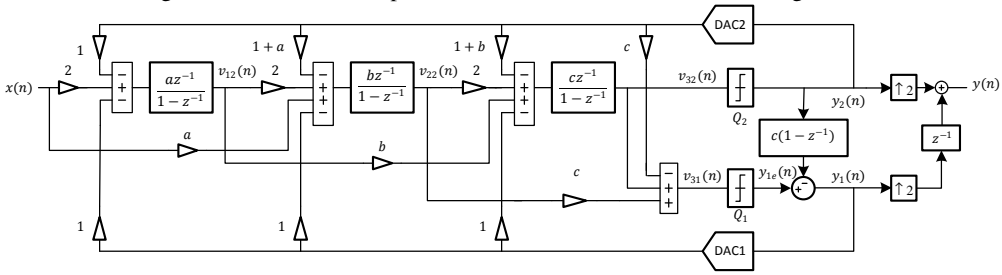


Figure 3. The proposed 3rd-order two-path DTTI ΔΣ modulator with shared integrators.

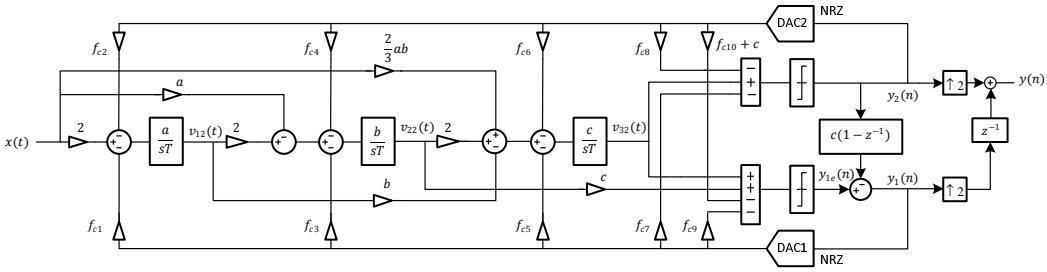


Figure 4. The proposed 3rd-order two-path CTTI ΔΣ modulator with shared integrators.

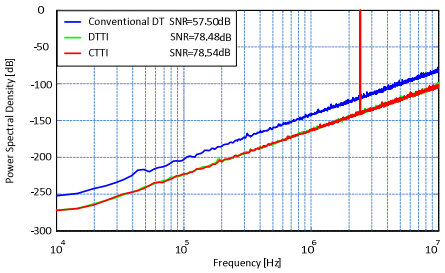


Figure 5. The output spectra of the conventional DT, the DTTI and the CTTI ΔΣ modulator for a 2.4462MHz input with clock frequencies

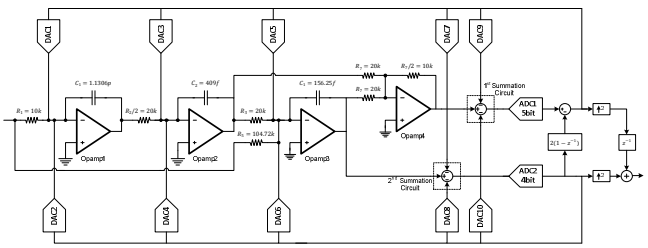


Figure 6. Block Diagram of the 3rd-order CTTI ΔΣ Modulator.

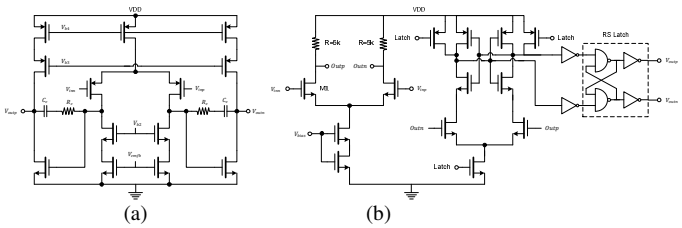


Figure 7. Schematic of (a) opamp and (b) comparator of the 3rd-order CTTI ΔΣ Modulator.

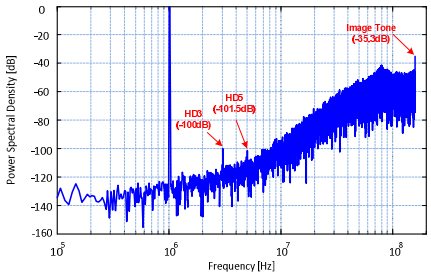


Figure 8. The output spectra of the CTTI ΔΣ modulator for a 1.005MHz input with clock frequencies of 320MHz simulated in TT corner and 27'C.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 October 2015 (01.10.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/144771 A1

(51) International Patent Classification:
H03M 3/00 (2006.01)

(21) International Application Number:
PCT/EP2015/056425

(22) International Filing Date:
25 March 2015 (25.03.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1405451.4 26 March 2014 (26.03.2014) GB

(71) Applicant: **UNIVERSITY OF WESTMINSTER** [GB/GB]; 309 Regent Street, London W1B 2UW (GB).

(72) Inventors: **KALE, Izzet**; 309 Regent Street, London W1B 2UW (GB). **TALEBZADEH, Jafar**; 309 Regent Street, London W1B 2UW (GB).

(74) Agent: **BAWDEN, Peter**; Bawden & Associates, 4 The Gatehouse, 2 High Street, Harpenden, Hertfordshire AL5 2TH (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

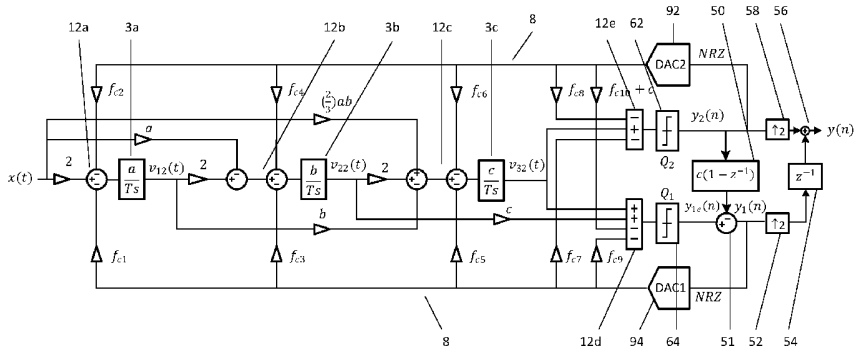
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: TIME INTERLEAVED DELTA SIGMA MODULATORS

Figure 7: A 3rd-order single-loop two path CTTI ΔΣ modulator.



(57) **Abstract**: In order to overcome the so-called delayless path problem, a time interleaved delta sigma modulator includes a plurality of paths for respective time interleaved data channels, said paths comprising a feed forward path arrangement, including first, second and third filter stages (3a, 3b, 3c), a first path including a first quantizer (Q1 64) being connected to a first feedback path (8) including a first DAC (94), a second path including a second quantizer (Q2 62) being connected to a second feedback path (8) including a DAC (92), and the output of the first DAC having a coupling (31) to the input of the second quantizer intentionally introducing errors in the analog domain, and the output of the first quantizer being coupled to the output of the second quantizer via a correction means performing a difference between the present time sample and the previous one and correcting the intentional errors introduced by said coupling (31).

WO 2015/144771 A1

TIME INTERLEAVED DELTA SIGMA MODULATORS

Field of the invention

This invention relates to Delta Sigma modulators.

Background of the invention

Delta Sigma (DS, or ΔΣ) modulators have applications in Analogue to Digital Converters (ADCs), Digital to Analogue Converters (DACs), Class D amplifiers, etc. They have become very popular converters for high-resolution applications because of their oversampling and noise shaping nature. These characteristics make them more robust to their components' nonlinearities and nonidealities. Indeed, by trading accuracy with speed, DS converters have become more attractive in the context of present CMOS technology evolution. The rapid growth of the portable communication device markets such as audio systems and consumer electronics has been led to an increasing demand for low power high resolution ADC designs over the last decade. The ΔΣ modulator can achieve a very high resolution analog-to-digital conversion for relatively low-bandwidth signals by using the oversampling and the noise shaping techniques. It is known that ΔΣ modulators do not require precise analog components and sharp cut-off frequencies for their analog anti-aliasing filters.

The noise-shaping loop filter of a ΔΣ modulator can be implemented as a single-loop Discrete-Time (DT) structure (Figure 1a) by using Switched-Capacitor (SC) circuits or as a single–loop Continuous-Time (CT) structure (Figure 1b) through active-RC or Gm-C filters. In Figures 1a and 1b, the reference numbers and symbols employed are applied throughout the remaining Figures to similar items. Referring to Figure 1a, a DT modulator accepts an input x(n), which is fed to a single loop comprising a feed-forward path 2 including a filter (accumulator) 4, which provides an output q(n) to an Analog to Digital Converter ADC 6 (quantizer), the output of the ADC providing the output y(n) of the modulator. The output of the modulator is fed in a feedback path 8, which includes a DAC 10, the output of the DAC being subtracted from the input signal in a combiner 12. Filter 4 is of a switched capacitor type, providing an accumulation function, and its transfer function is $H_d(z)$, where z is the z-transform for discrete time systems. The transfer function for DAC 10 is $H_{dDAC}(z)$. Switched Capacitor filter circuits of DT

structures are insensitive to clock jitter and the frequency response of the noise-shaping filter can be relatively accurately set by capacitor ratios.

For the purposes of the present specification, and in the context of ΔΣ modulation, the terms Analog to Digital Converter, ADC, and quantizer are regarded as having the same meaning.

Referring to Figure 1b, a CT ΔΣ modulator has an input signal x(t) applied to a single loop comprising a Continuous Time (CT) integrator filter 3 in its feed forward path 2, providing an output $q_c(t)$ followed by a sample and hold switch 5, providing an output $q_c(nT)$, which is fed to ADC (quantizer) 6. ADC 6 provides an output y(n), which is fed back in feedback path 8 via DAC 9 to combiner 12, where it is subtracted from the input signal x(t).

Filter 3 and DAC 9 in the feedback path 8 are represented by Laplacian transfer functions in the continuous time domain $H_c(s)$, $H_{cDAC}(s)$. Filter 3 provides an integration function. CT ΔΣ modulators benefit from operating at higher sampling frequencies in comparison to their DT counterparts. The errors of the sample-and-hold circuit are shaped by the loop filter and CT ΔΣ modulators have an implicit anti-aliasing filter in their forward signal path. However, CT ΔΣ modulators suffer from several drawbacks: excess loop delay, jitter sensitivity and RC time constant variations.

The signal bandwidth that ΔΣ modulators can deal with is narrow and is restricted by the OverSampling Ratio (OSR) and deployed technology. To increase the signal bandwidth the modulator can process, a variety of methods are used. The first one is to increase the order of the modulator. ΔΣ modulators commonly have a filter (accumulator or integrator) in the forward signal path. Inserting a second integrator in the feed forward path converts the modulator from first order to second order. The order may be increased at will, but at a price, where the stability problem needs to be dealt with very carefully.

The second is to increase the number of bits for the ADC/quantizer, which makes the modulator more complicated. The third is to increase the sampling frequency. However, the most serious disadvantage of the third method is the technology limitations.

A fourth method to increase bandwidth is to employ the time-interleaving (TI) technique. This is a known technique which is based on a concept of an array or plurality of ΔΣ modulators coupled in parallel to an input sampled

signal, each modulator providing a respective processing channel. The input samples are distributed cyclically to the modulator channels, one sample to the first modulator channel, the next sample to the second, etc., In this way, for M interconnected parallel modulators that are working concurrently, the effective sampling rate and the OSR become M times the clock rate and the OSR of each modulator respectively. It should be noted that the required resolution can be acquired without increasing the order of the modulator or the number of bits for the quantizer. Much work has been carried out to simplify the design of TI ΔΣ modulators, see M. Kozak, M. Karaman, and I. Kale, "Efficient Architectures for Time-Interleaved Oversampling Delta-Sigma Converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 8, pp. 802–810, Aug. 2000; M. Kozak and I. Kale, "Novel Topologies for Time-Interleaved Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 7, pp. 639–654, Jul. 2000. It has been demonstrated that a TI structure with a number of processing channels or paths may be simplified so that the paths are integrated in a single ΔΣ modulator structure. Each modulator path is routed to a respective ADC (quantizer), each ADC (quantizer) having a respective feedback path including a DAC. Hence for a Time Interleaved ΔΣ modulator, which will have at least two paths, there are at least two quantizers working in parallel, each with a respective feedback path including a DAC. This is more fully explained below.

As explained more fully below, a problem arises with time interleaved ΔΣ modulators, in that with two quantizers operating in parallel paths, there is necessarily a critical path, or so-called delayless path, between the output of one quantizer to the input of the other quantizer. Because of delays arising in paths of the modulators, this may prevent correct operation. One method to eliminate the delayless path problem is to move feedback to the digital domain instead of performing it in the analog domain: see K. S. Lee, Y. Choi and F. Maloberti," Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator," *IEEE ISCAS,* pp. 473-476, 2004 which discloses a four path discrete time TI modulator where, instead of directly generating the 4-consecutive modulator outputs for time slot n, n+1, n+2, n+3 for each of four quantizers, only the n-th time slot modulator output and three predictive terms are generated by the quantizers. The disadvantage of this method is that the

first quantizer requires more comparators than the number of the comparators in the second quantizer.

A second method is to use a sample-and-hold in front of the first quantizer and quantizing the signal when the output of the second DAC is ready [T. C. Caldwell and D. A. Johns," A Time-Interleaved Continuous-Time ΔΣ Modulator with 20-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits,* vol. 41, no. 7, pp. 1578-1588, July 2006.]. This method needs a complicated timing generator, a sample-and-hold and also faster integrators.

The problem therefore remains of overcoming the delayless path problem in a comparatively simple and efficient manner

Summary of the Invention

An embodiment of the invention is based on an error correction technique for overcoming the delayless path issue in time interleaved delta sigma modulators. An error is intentionally induced in the analog domain through the use of the output of one DAC in one feedback path from a first quantizer, which is applied to the input of a second quantizer associated with another feedback path and DAC. Although this output may relate to a previous time sample, the error thus created is then substantially corrected in the digital domain at the outputs of the quantizers, which may effectively eliminate the delayless feedback path.

Accordingly in one embodiment the invention provides a time interleaved delta sigma modulator including:

a plurality of paths for respective time interleaved data channels, which paths comprise a respective feed forward path arrangement including at least one filter stage, a first one of said paths including a first quantizer means being connected to a first feedback path including a first digital to analog conversion means, a second one of said paths including a second quantizer means being connected to a second feedback path including a second digital to analog conversion means, and

the output of the first digital to analog conversion means having a coupling to the input of the second quantizer means, and the output of the first quantizer being coupled to the output of the second quantizer means via a correction means for correcting errors introduced by said coupling.

The invention recognises that errors are created by delays causing timing misalignment, but because input signals vary relatively slowly in comparison to the clocking of the modulator, said coupling may provide the signal value from the first digital to analog conversion means (DAC) obtained at a previous clock interval. This will permit the second quantizer means to perform its quantisation operation. The error induced may then be corrected in the digital domain by means of an error correction circuit coupled between the outputs of the first and second quantizers means. Conveniently, said coupling is a direct coupling, not incorporating any delay or filtering circuits. Conveniently, the correction may be of the differencing form $(1-z^{-1})$, representing the difference between the present time sample, and the previous one.

The present invention is applicable to any number of channels/paths, two or more, in a time interleaved arrangement. Preferably the paths of the modulator share the same filter (integrator/ accumulator) stages in the feed forward arrangement. The invention is applicable to modulators having one or more modulator loops, although the invention is particularly applicable to a single loop arrangement in a time interleaved arrangement. Further the invention is applicable to both DT and CT modulators, although it is particularly useful with CT modulators, as will become clear below.

Brief Description of the Drawings

Preferred embodiments of the invention will now be described by way of example with reference to the accompanying drawings, wherein:

Figure 1 comprises Block diagrams of a) the known DT Single-Loop ΔΣ modulator and b) the known CT Single-Loop ΔΣ modulator r;

Figure 2 is a block diagram of a 3^{rd}-order single-loop DT ΔΣ modulator;

Figure 3 is a block diagram of a 3rd-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators;

Figure 4 is a waveform diagram showing the outputs of Q1, Q2, DAC1 and DAC2 of Figure 3;

Figure 5 is a block diagram of a first embodiment of the invention, comprising a 3rd-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators and digital correction network;

Figure 6 are block diagrams of a) a Single-Loop Two-Path DTTI ΔΣ modulator and b) a Single-Loop Two-Path CTTI ΔΣ modulator;

Figure 7 is a block diagram of a second embodiment of the invention comprising a 3rd-order Single-Loop Two-Path CTTI ΔΣ modulator with shared integrators;

Figure 8 shows the signal transfer functions of the 3rd-order Single-Loop Two-Path DTTI and the 3rd-order Single-Loop Two-Path CTTI ΔΣ modulators. of Figures 5 and 7;

Figure 9 shows noise transfer functions of the 3rd-order Single-Loop Two-Path CTTI ΔΣ modulator of Figure 7 and a 3rd-order Single-Loop Two-Path DTTI ΔΣ modulator;

Figure 10 is a block diagram of a third embodiment of the invention comprising a 4th-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators; and

Figure 11 is a block diagram of a fourth embodiment of the invention comprising a 3rd-order Single-Loop Four-Path DTTI ΔΣ modulator with shared accumulators.

Description of the Embodiments

CT ΔΣ modulators benefit from operating at higher sampling frequencies in comparison to their DT counterparts. The errors of the sample-and-hold circuit are shaped by the loop filter and the CT ΔΣ modulators have an implicit anti-aliasing filter in their forward signal path. However, CT ΔΣ modulators suffer from several drawbacks: excess loop delay, jitter sensitivity and RC time constant variations.

One way to convert a DT ΔΣ modulator to an equivalent CT ΔΣ modulator is the known impulse-invariant transformation [M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*. Berlin: Springer, 2006]. Another is the use of the modified z-transform. The impulse-invariant transformation is employed below. A DT ΔΣ modulator and a CT ΔΣ modulator are shown in Figure 1, and are said to be equivalent when their quantizer inputs are equal at the sampling instants.

$$q(n) = q_c(t)\big|_{t=nT} \quad (1)$$

The procedure for the design of a ΔΣ modulator is based on choosing: the order and architecture of the ΔΣ modulator, the OverSampling Ratio (OSR) and the number of bits for the quantizer. By using the time-interleaving technique and M interconnected parallel modulators that are working concurrently, the effective sampling rate and the OSR become M times the clock rate and the OSR of each modulator respectively; it should be noted with this technique the required resolution can be acquired without increasing the order of the modulator or the number of bits for the quantizer and also without utilizing a state of the art technology.

A 3rd-order single loop two path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator (below, Figure 3) may be derived from the time domain node equations of a conventional DT ΔΣ modulator, which is shown in Figure 2. In Figure 2, a first accumulator filter 4a obtains an input from combiner 12a, and has a transfer function $az^{-1}(1-z^{-1})^{-1}$, i.e.an accumulation function, with scaling a. Second and third accumulators 4b and 4c with respective transfer functions $bz^{-1}(1-z^{-1})^{-1}$, $cz^{-1}(1-z^{-1})^{-1}$ obtain inputs from respective combiners 12b, 12c. In this Figure, single step quantizer 6 represents the ADC. It is assumed that the DAC 10 in the feedback loop 8 is ideal ($H_{DAC}(z) = 1$). The time domain equations of the modulator are written for two consecutive time slots as (2n)th and (2n+1)th as follows:

$$v_1(2n) = ax(2n-1) - ay(2n-1) + v_1(2n-1) \quad (2.a)$$

$$v_2(2n) = bv_1(2n-1) - by(2n-1) + v_2(2n-1) \quad (2.b)$$

$$v_3(2n) = cv_2(2n-1) - cy(2n-1) + v_3(2n-1) \quad (2.c)$$

$$y(2n) = Q[v_3(2n)] \quad (2.d)$$

and

$$v_1(2n+1) = ax(2n) - ay(2n) + v_1(2n) \quad (3.a)$$

$$v_2(2n+1) = bv_1(2n) - by(2n) + v_2(2n) \quad (3.b)$$

$$v_3(2n+1) = cv_2(2n) - cy(2n) + v_3(2n) \quad (3.c)$$

$$y(2n+1) = Q[v_3(2n+1)] \quad (3.d)$$

where $Q[.]$ represents the quantization function. The input $x(n)$ is distributed between two channels through an input multiplexer which operates at twice the clock frequency of each channel. The input $x(n)$ is relabelled as follows:

$$x_1(n) = x(2n) \quad , \quad x_2(n) = x(2n-1) \quad (4)$$

Similarly, the other nodes of the modulator are relabelled:

$$v_{11}(n) = v_1(2n) \quad , \quad v_{12}(n) = v_1(2n-1) \quad (5.a)$$

$$v_{21}(n) = v_2(2n) \quad , \quad v_{22}(n) = v_2(2n-1) \quad (5.b)$$

$$v_{31}(n) = v_3(2n) \quad , \quad v_{32}(n) = v_3(2n-1) \quad (5.c)$$

$$y_1(n) = y(2n) \quad , \quad y_2(n) = y(2n-1) \quad (5.d)$$

By sharing only one set of accumulators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. Hence equation (4) results in (6) as follows:

$$x_1(n) = x_2(n) = x(n) \quad (6)$$

Equation sets (7) and (8) are derived by substituting equation set (5) and equation (6) into equation sets (2) and (3) respectively as follows:

$$v_{11}(n) = ax(n) - ay_2(n) + v_{12}(n) \quad (7.a)$$

$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \quad (7.b)$$

$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \quad (7.c)$$

and

$$v_{12}(n+1) = ax(n) - ay_1(n) + v_{11}(n) \quad (8.a)$$

$$v_{22}(n+1) = bv_{11}(n) - by_1(n) + v_{21}(n) \quad (8.b)$$

$$v_{32}(n+1) = cv_{21}(n) - cy_1(n) + v_{31}(n) \quad (8.c)$$

Equation set (8) can be rewritten as equation set (9):

$$v_{12}(n) = ax(n-1) - ay_1(n-1) + v_{11}(n-1) \quad (9.a)$$

$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \quad (9.b)$$

$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \quad (9.c)$$

Equation set (10) is derived by further substituting equation set (7) into equation set (8).

$$v_{12}(n) = 2ax(n-1) - a(y_1(n-1) + y_2(n-1)) + v_{12}(n-1) \quad (10.a)$$

$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \quad (10.b)$$

$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - cy_1(n-1) - c(1+b)y_2(n-1) + v_{32}(n-1) \quad (10.c)$$

The DTTI ΔΣ modulator which is shown in Figure 3 is derived directly from the time domain equation sets (7) and (10). The motive behind sharing one set of accumulator filters in a single feed forward path is to eliminate the instability that can arise due to the DC offset mismatch of the two individual accumulator set based two channel interleaving case. Known DTTI ΔΣ modulators need an input demultiplexer which samples the input signal at the highest clock frequency of the DTTI ΔΣ modulator and distributes it between channels. This fast demultiplexer is a limiting factor for the performance of the DTTI ΔΣ modulators. The architecture shown in Figure 3 does not need an input demultiplexer and the input signal is shared between channels. Removing the input demultiplexer has no effect on the NTF of the DTTI ΔΣ modulator but it causes some notches in its STF at the following frequencies $^{0.5F_{clk}}$, $^{1.5F_{clk}}$, $^{2.5F_{clk}}$, $^{3.5F_{clk}}$, ... which is shown in Figure 10 where $^{F_{clk}}$ is the clock frequency of the DTTI ΔΣ modulator.

Referring to the 3rd-order single-loop two-path DTTI ΔΣ modulator with shared accumulators Figure 3, the two paths comprise a feed forward path arrangement 2 having three accumulator filters 4a, 4b, 4c each with a respective transfer function $az^{-1}(1 - z^{-1})^{-1}$, $bz^{-1}(1 - z^{-1})^{-1,}$ $cz^{-1}(1 - z^{-1})^{-1}$, thus

providing a third order arrangement. Each accumulator is preceded by a respective signal combiner 12a, 12b, 12c. The input signal x(n) is fed to signal combiners 12a, 12b via respective scalers 2, a. The output of accumulator 4a, $v_{12}(n)$ is fed to combiners 12b, 12c via scalers 2, b. The output of accumulator 4b, $v_{22}(n)$ is fed to combiners 12c, 12d via respective scalers 2, c, and the output of accumulator 4c, $v_{32}(n)$ is fed direct to combiner 12d and quantizer Q2.

The output of accumulator 4c is fed direct to a second path quantizer (ADC) Q2 62, and, via signal combiner 12d, to the input of a first path quantizer (ADC) Q1 64. The output of Q2 62 is fed in a second feedback path 8 to DAC 102 and then to subtracting inputs of each signal combiner 12a - 12c, via scaling amplifiers 14, having respective values 1, 1+a, 1+b. The output of Q1 64 is fed in a first feedback path 8 to DAC 101 and then to subtracting inputs of each signal combiner 12a - 12c, via scaling amplifiers 16, having values 1. The output of Q2 62, $y_2(n)$, is fed in a Delayless Path 30 having a scaler c, to a summing input of combiner 12d. The output $y_1(n)$ is fed via a x2 scaler 32 and delay circuit 34, to a signal combiner 36, where it is combined with the output $y_2(n)$, scaled by 2 as at 38 to provide the output signal y(n).

As regards operation of the single path Time Interleaved modulator, it will be noted there is an analog adder 12d in front of quantizer Q1 and the input signal there generated is then applied to the quantizer Q1. In discrete time delta-sigma modulators, quantizers sample this input. As stated in the above formulas, v32(n) and v31(n) are the respective inputs of the second and first quantizers. v32(n) is the output of third accumulator 4c but v31(n) is: (v31(n)=c*v22(n)-c*y2(n)+v32(n)) (We will use an analog adder to generate v31(n) from v32(n), v22(n) and y2(n)). That means that v31(n) is generated by the outputs of the second and third accumulators 4b, 4c and also the output of the second quantizer Q2. The direct relation between v31(n) to y2(n) comprises the “delayless path”.

An issue which makes implementation of the single-path TI ΔΣ modulators impractical is this so-called “delayless feedback path” problem that comes from equation (7.c) above in which $v_{31}(n)$ (the input of quantizer Q1) is directly linked to $y_2(n)$. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay. One

method to eliminate the delayless path is to move this feedback to the digital domain instead of performing it in the analog domain [K. S. Lee, referenced above]. The disadvantage of this method is that the first quantizer (Q1) requires more comparators than the number of the comparators in the second quantizer (Q2) . Another second method is to use a sample-and-hold in front of the first quantizer (Q1) and quantizing the signal when the output of DAC2 is ready [T. C. Caldwell, referenced above]. This method needs a complicated timing generator, a sample-and-hold and also faster accumulators.

An embodiment of the invention, as shown in Figure 5, overcomes the delayless path issue by an error correction technique. We intentionally induce an error in the analog domain through the use of the output of DAC2 102 as shown in Figure 5. The error is substantially corrected in the digital domain which effectively eliminates the delayless feedback path.

To better understand how this works we shall perform a step by step analysis of what happens. A timing diagram as depicted in Figure 4 shows the delay from the outputs of quantizers Q1 and Q2 and their propagation through to the outputs of DAC1 and DAC2 as δ. As a result the output of DAC2 that is sampled at the nth time slot is $y_2(n-1)$ where we should have had $y_2(n)$. To overcome this inconsistency we look at the input and output of Q1, as depicted in Figure 4. Quantizer Q1 quantizes the signal $v_{31}(n)$ as follows:

$$y_1(n) = Q[v_{31}(n)] \quad (11)$$

Equation (12) is derived by substituting (7.c) into (11):

$$y_1(n) = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \quad (12)$$

The output of DAC2 is used in (13) and equation (12) is rewritten as:

$$y_1(n) = Q[cv_{22}(n) - cy_2(n-1) + v_{32}(n)] + cy_2(n-1) - cy_2(n) \quad (13)$$

The output of Q1 is called $y_{1e}(n)$ in (14):

$$y_1(n) = y_{1e}(n) + cy_2(n-1) - cy_2(n) \quad (14)$$

$$error = c\Delta y = c(y_2(n) - y_2(n-1)) \quad (15)$$

$$Y_1(z) = Y_{1e}(z) - c(1 - z^{-1})Y_2(z) \quad (16)$$

As appears from (14), $y_{1e}(n)$ (the output of Q1) needs to be corrected before it is applied to the input of DAC1; otherwise it causes instability in the modulator as it will change the modulators dynamics by increasing its order. A first order differencer block $(1-z^{-1})$ is used to perform this correction as described in (16). Equation (16) illustrates the point that Q1 is able to quantize its input without any additional circuit in the analog domain by merely using the output of DAC2. The differencer block $(1-z^{-1})$ only corrects the error in equation (14) and it has no effect on the quantization error or the signal.

The 3rd order single-loop two path DTTI ΔΣ modulator forming a first embodiment of the invention is shown in Figure 5. Referring to Figure 5, feed forward path arrangement comprises three accumulator filters 4a, 4b, 4c each with a respective transfer function $az^{-1}(1 - z^{-1})^{-1}$, $bz^{-1}(1 - z^{-1})^{-1}$, $cz^{-1}(1 - z^{-1})^{-1}$, thus providing a third order arrangement. Each accumulator is preceded by a respective signal combiner 12a, 12b, 12c. The input signal x(n) is fed to signal combiners 12a, 12b via scalers 2, a. The output of accumulator 4a, $v_{12}(n)$ is fed to combiners 12b, 12c via scalers 2, b. The output of accumulator 4b, $v_{22}(n)$ is fed to combiners 12c, 12d via scalers 2, c, and the output of accumulator 4c, $v_{32}(n)$ is fed direct to combiner 12d and quantizer Q2.

The output of accumulator 4c is fed direct to second path quantizer Q2 62, and, via signal combiner 12d, to the input of first path quantizer Q1 64. The output of Q2 is fed in a second feedback path 8 to DAC 102 and then to subtracting inputs of each signal combiner 12a-12d, via scaling amplifiers 14 having values1, 1+a, 1+b, and c. It will be noted there is a direct coupling 31 from the output of DAC 102 to the input of Q1 64. The output of Q1 is fed in a first feedback path 8 to DAC 101 and then to subtracting inputs of each signal combiner 12a-12c, via scaling amplifiers 1. The output of Q2, $y_2(n)$ is fed via an error correction circuit 50 having the transfer function $c(1-z^{-1})$ to a subtracting input of a signal combiner 51, where it is combined with the output of Q1, $y_{1e}(n)$,

to give output $y_1(n)$. The output $y_1(n)$ is fed via a x2 scaler 52 and delay circuit 54, to a signal combiner 56, were it is combined in combiner 56 with the output $y_2(n)$, scaled by 2 as at 58.

The significant advantages and disadvantages of the Lee paper, referenced above, the Caldwell paper, referenced above, and the present invention are summarized in the Table below:

Method	Comparator count for Q1	Comparator count for Q1	Advantage	Disadvantage
Lee	48	16	Additonal analog blocks not needed	More comparators for Q1 required
Caldwell	16	16	Fewer comparators	Sample/Hold, complex timing generator and fast integrators required
Invention	32	16	Additonal analog blocks not needed	More comparators required for Q1 than Caldwell

The signal swing at the input of quantizer Q1 is increased in the first and the present methods because scaling is not an option and it will lead to loss of Signal-to-Noise Ratio (SNR), the first and the present methods require 48 and 32 comparators for quantizer Q1 respectively, in comparison to the second method which requires 16 comparators as depicted in Table I.

The CTTI ΔΣ modulator equivalent of the DTTI ΔΣ modulator of Figure 5 can be obtained in three steps as follows: The first step is to determine the loop filters of the DTTI ΔΣ modulator. In this design, the DTTI ΔΣ modulator has six loop filters ($FF_{1d}(z)$, $FF_{2d}(z)$, $H_{1d}(z)$, $H_{2d}(z)$, $H_{3d}(z)$ and $H_{4d}(z)$) These loop filters for the DTTI ΔΣ modulator are as depicted in Figure 6(a). The second step is to convert the DT loop filters into equivalent CT loop filters by using the impulse-invariant transformation. The equivalent CTTI ΔΣ modulator is shown in Figure 6(b) where the DT loop filters of Figure 6(a) have been replaced with the equivalent CT loop filters $FF_{1c}(s)$, $FF_{2c}(s)$, $H_{1c}(s)$, $H_{2c}(s)$, $H_{3c}(s)$ and $H_{4c}(s)$.

The third step is to convert the modulator of Figure 6(b) into a 3rd order CTTI ΔΣ modulator as shown in Figure 7. To overcome the excess-loop delay issue, two additional feedback paths from the outputs of DAC1 and DAC2 to the inputs of each quantizer (Q1 and Q2) are used. The loop filters of the modulator as shown in Figure 7 can be found and matched to those in Figure 6(b) to determine the coefficients f_{1c}, f_{2c}, f_{3c}, f_{4c}, f_{5c}, f_{6c}, f_{7c}, f_{8c}, f_{9c} and f_{10c} in Figure 7.

Referring to the 3rd-order Single-Loop Two-Path CTTI ΔΣ modulator with shared integrators of Figure 7, three sets of integrator filters 3a, 3b, 3c, in a feed forward path arrangement have their inputs provided by signal combiners 12a, 12b, 12c, combiners 12b and 12c each comprising two combiners in series. Each integrator filter has a transfer function of the form 1/Ts, with respective scaling coefficients a, b, c. The input signal x(t) is fed to signal combiners 12a, 12b, 12c via scaling amplifiers having respective values 2, a, 2/3(ab). The output of integrator 3a, $v_{12}(t)$ is fed to combiners 12b, 12c via respective scaler amplifiers 2, b, the output of integrator 4b, $v_{22}(t)$ is fed to combiners 12c, 12d via scaling amplifiers 2, c, and the output of integrator 4c, $v_{32}(n)$ is fed direct to combiners 12d, 12e.

The output of integrator 3c is fed via signal combiner 12d to first path quantizer (ADC) Q1 64, and via signal combiner 12e to the input of second quantizer (ADC) Q2 62. The output of Q2 62 is fed in a second feedback path 8 to DAC 92 and then to subtracting inputs of each signal combiner 12a - 12e, via respective scaling amplifiers f_{c2}, f_{c4}, f_{c6}, f_{c10}, f_{c8}. It will be noted there is a direct coupling 31 from the output of DAC 92 to the input of Q1 64. The output of Q1 64, modified as at 51, is fed in a first feedback path 8 to DAC 94 and then to subtracting inputs of each signal combiner 12a - 12e, via scaling amplifiers f_{c1}, f_{34}, f_{c5}, f_{c9}, f_{c7}. The output of Q2, $y_2(n)$ is fed via an error correction circuit 50 having the transfer function $c(1-z^{-1})$ to a subtracting input of a signal combiner 51, where it is combined with the output of Q1, $y_{1e}(n)$, to give output $y_1(n)$. The output $y_1(n)$ is fed via a x2 scaler 52 and delay circuit 54, to a signal combiner 56, were it is combined in combiner 56 with the output $y_2(n)$, scaled by 2 as at 58 to give the final output y(n).

It will be noted that the outputs of DAC 92, 94 are each fed to each of quantizers Q1, Q2, via signal combiners 12d, 12e, to overcome excess loop delay.

The OSR of the overall modulator shown in Figure 7 from $x(t)$ to $y(n)$ is 16 and has been designed to operate at 320MHz clock frequency for a 10MHz signal bandwidth. The resolution of Q1 and Q2 are 5bits and 4bits respectively. After correcting the error as stated by equation (21) in the digital domain, $y_1(n)$ will be 4bits in length. Therefore, DAC1 and DAC2 both require 4bit DACs. To

simplify the design, generally, the coefficient c scaling the first order differencer $(1-z^{-1})$ in the digital domain should be chosen to be a number which is a power of two. This choice results in replacing the potentially complicated multiplier with a simple hard-wired shift.

The STFs of the DTTI and CTTI ΔΣ modulators are plotted in Figure 8. Since the $NTF_{1d}(z)$ and $NTF_{2d}(z)$ both have an identical amplitude, only the $NTF_{1d}(z)$ is plotted in Figure 9 and is compared to the NTF of the conventional DT ΔΣ modulator of Figure 4.

Referring now to Figure 10, which shows a third embodiment of the invention comprising a 4th-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators, similar parts to those of previous embodiments, in particular Figure 5, are denoted by the same reference numeral. In contrast to Figure 5, Figure 10 comprises a 4th order single-path DTTI ΔΣ modulator, having four accumulator filter stages 4a, 4b, 4c, 4f. Accumulator 4f has a transfer function $dz^{-1}(1 - z^{-1})^{-1}$, and has an input fed by combiner 12f, which receives a feedback signal from second path DAC 102, scaled by (1+c), a feedback signal from first path DAC 101, and the output from accumulator 4c, $v_{32}(n)$. The output of accumulator 4f, $v_{42}(n)$, is applied direct to the input of quantizer Q2 62, and to signal combiner 12g, where it is combined with the output $v_{32}(n)$, scaled by d, and by the feedback signal from DAC 102, scaled by d, to provide a resultant signal $v_{41}(n)$ to the input of quantizer Q1 64. The output of quantizer Q1 is combined at 51 with the output of Q2, digitally corrected in correction circuit 50d by a factor $d(1-z^{-1})$.

Referring now to Figure 11, which shows a fourth embodiment of the invention comprising a 3rd-order Single-Loop Four-Path DTTI ΔΣ modulator with shared accumulators, similar parts to those of previous embodiments, in particular Figure 5, are denoted by the same reference numeral. Figure 10 comprises a 3rd order four-path DTTI ΔΣ modulator, having three accumulator stages 4a, 4b, 4c in a feed forward path arrangement. Four quantizers of respective first, second, third and fourth paths are employed operating in parallel, Q1 64, Q2 62, Q3 66, Q4 68. Quantizer Q1 64 accepts an input from signal combiner 70, Quantizer Q2 62 accepts an input from signal combiner 72,

Quantizer Q3 66 accepts an input from signal combiner 74, and Quantizer Q4 68 accepts an input direct from accumulator 4c.

The output of quantizer Q4 68 is applied direct to signal combiner 56 via a x4 scaler, which provides the final output y(n), and to a fourth feedback path which include a DAC 104. The output of quantizer Q3 66 is applied to a signal combiner 71, and thence to a third feedback path which include a DAC 103. The output of quantizer Q2 62 is applied to a signal combiner 73, and thence to a second feedback path which include a DAC 102. The output of quantizer Q1 64 is applied to a signal combiner 75, and thence to a first feedback path which include a DAC 101.

The input signal x(n) is split into four parallel paths and is applied to combiners 12a, 12b, 12c, 12d, via respective scalers 4, 6a, 4ab, abc. The output of accumulator 4a, $v_{14}(n)$, is applied to combiners 12b, 72, 70 via respective scalers 4, bc, 3bc. The output of accumulator 4b, $v_{24}(n)$, is applied to combiners 12c, 74, 72, 70 via respective scalers 4, c, 2c, 3c. The output of accumulator 4c, $v_{34}(n)$, is applied directly to combiners 74, 72, 70.

The output of quantizer Q4 68 is applied to signal combiner 56, scaled by a factor of 4, and via digital correction circuit 80, to signal combiners 71, 73, 75, via respective scalers c, c(b+1), c(b(a+2) +1). The output of quantizer Q3 66 is applied to signal combiner 71, the output of 71 being scaled by a factor of 4, and applied to combiner 56 via a delay circuit z^{-1}. The output of 71 is also applied via digital correction circuit 82 to combiners 73, 75 via respective scalers c, c(b+1). The output of quantizer Q2 62 is applied to signal combiner 73, the output of 73 being scaled by a factor of 4, and applied to combiner 56 via two delay circuits z^{-1}. The output of 73 is also applied via digital correction circuit 84 to combiner 75 via respective scaler c. The output of quantizer Q1 64 is applied to signal combiner 75, the output of 75 being scaled by a factor of 4, and applied to combiner 56 via three delay circuits z^{-1}. The output of 73 is also applied via digital correction circuit 84 to combiner 75 via respective scaler c.

The feedback signal in the first path from DAC 101 is applied directly to combiners 12a, 12b, 12c. The feedback signal in the second path from DAC 102 is applied to combiners 12a, 12b, 12c, 70, via respective scalers (none), 1+a, 1+b, c. The feedback signal in the third path from DAC 103 is applied to combiners 12a, 12b, 12c, 70, 72 via respective scalers (none), 1+2a, 1+ab+2b,

c(b+1), c. The feedback signal in the fourth path from DAC 104 is applied to combiners 12a, 12b, 12c, 70, 72, 74 via respective scalers (none), 1+3a, 1+3ab+3b, c+2bc+abc, c(b+1), c. It will be noted there are direct couplings from the outputs of DACs 102 -104 to quantizers Q1-Q3.

In the single path modulator embodiments above, sharing the integrators/ accumulators between the input paths makes them robust to path mismatch effects compared to the typical Time-Interleaved (TI) modulators which have individual integrators in all paths. Practical issues like finite dc gain and bandwidth of the opamps, the DAC mismatches and offsets of the quantizers may not introduce any noticeable degradation in performance. For an OverSampling Ratio (OSR) of 16 and a clock frequency of 320MHz with all practical non-idealities the maximum SNDR of this modulator may be 78dB.

The present invention at least in embodiments provides a mechanism for resolving the delayless feedback path issue in TI ΔΣ modulators with reduced comparator count.

CLAIMS

1. A time interleaved delta sigma modulator including:

a plurality of paths for respective time interleaved data channels, said paths comprising a feed forward path arrangement, including at least one filter stage, a first one of said paths including a first quantizer means being connected to a first feedback path including a first digital to analog conversion means, a second one of said paths including a second quantizer means being connected to a second feedback path including a second digital to analog conversion means, and

the output of the first digital to analog conversion means having a coupling to the input of the second quantizer means, and the output of the first quantizer means being coupled to the output of the second quantizer means via a correction means for correcting errors introduced by said coupling.

2. A time interleaved sigma delta modulator, according to claim 1, wherein the modulator is a discrete time modulator.

3. A time interleaved sigma delta modulator, according to claim 2, wherein said feed forward path arrangement has at least first and second accumulator stages, and the output of the second stage is coupled to the input of the second quantizer means, and the outputs of both the first and second stages are coupled to the input of the first quantizer means.

4. A time interleaved sigma delta modulator, according to claim 2, wherein said feed forward path arrangement has at least first, second and third accumulator stages, wherein an input signal is fed to the first and second stages, an output from the first stage is fed to the second and third stages, an output from the second stage is fed to the third stage and said first quantizer means, and an output from the third stage is fed to said first quantizer means, and directly or via further accumulator stages to said second quantizer means.

5. A time interleaved sigma delta modulator, according to claim 3 or 4, wherein said feed forward path arrangement has at least first, second and third accumulator stages, wherein said first feedback path and said second feedback path are each coupled to each of said first, second and third accumulator stages.

6. A time interleaved sigma delta modulator, according to claim 1, wherein the modulator is a continuous time modulator.

7. A time interleaved sigma delta modulator, according to claim 6, wherein said feed forward path arrangement has at least first and second integrator stages, and the output of the second stage is coupled to the input of the second quantizer means, and the outputs of both the first and second stages are coupled to the input of the first quantizer means.

8. A time interleaved sigma delta modulator, according to claim 6, wherein said feed forward path arrangement has at least first, second and third integrator stages, wherein an input signal is fed to the first, second and third stages, an output from the first integrator stage is fed to the second stage and to the third stage, an output from the second integrator stage is fed to the third stage and said first quantizer means, and an output from the third integrator stage is fed to said first quantizer means, and directly or via further integrator stages to said second quantizer means.

9. A time interleaved sigma delta modulator, according to claim 7 or 8, wherein said feed forward path arrangement has at least first, second and third integrator stages, wherein said first feedback path and said second feedback path are each coupled to each of said first, second and third integrator stages.

10. A time interleaved sigma delta modulator, according to any of claims 7 to 9, wherein said first feedback path and said second feedback path are each coupled to each of the inputs of said first and second quantizer means.

11. A time interleaved sigma delta modulator, according to any preceding claim, wherein said correction means is a digital differencing circuit having a transfer function of the form $(1-z^{-1})$.

12. A time interleaved sigma delta modulator, according to claim 11, wherein a coefficient scaling said transfer function of the form $(1-z^{-1})$ comprises a number which is a power of two.

13. A time interleaved sigma delta modulator, according to any preceding claim, wherein the modulator has at least three paths with respective first, second and third quantizer means, said third quantizer means being connected to a third feedback path including a third digital to analog conversion means, the output of the third digital to analog conversion means

having a further coupling to the inputs of the first and second quantizer means, and the output of the third quantizer means being coupled to the outputs of the first and second quantizer means via respective further correction means for correcting errors introduced by said further coupling.

5

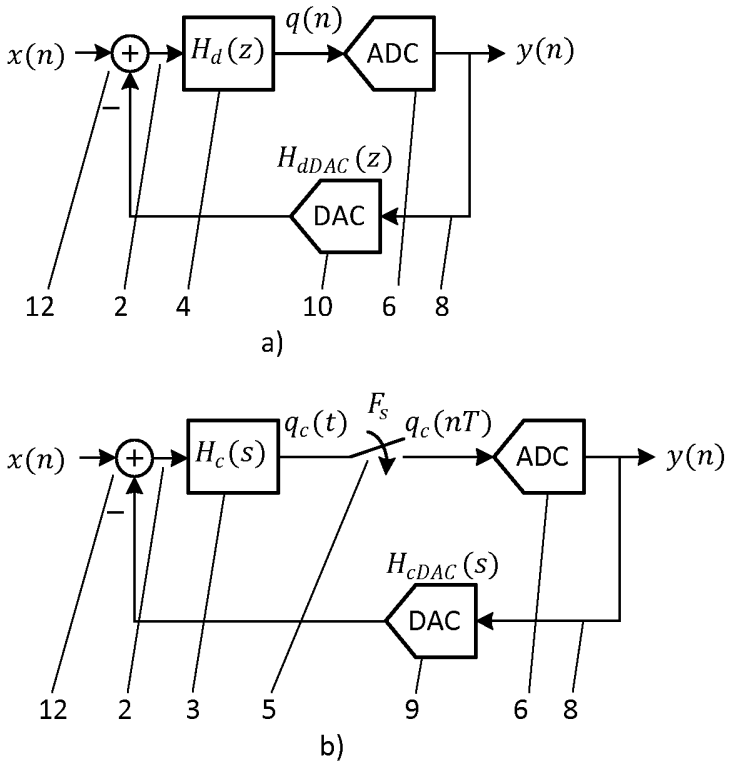


Figure 1: Block diagrams of a) The DT ΔΣ modulator and b) The CT ΔΣ modulator.

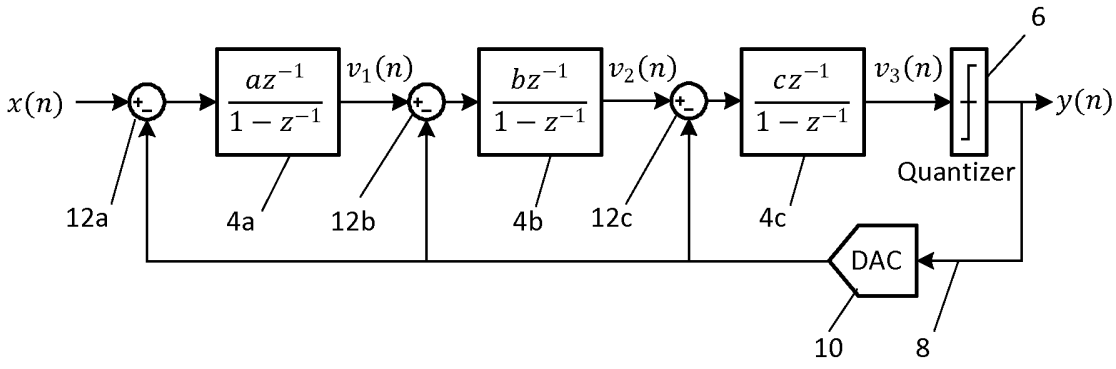


Figure 2: Block diagram of a 3rd-order single-loop DT ΔΣ modulator.

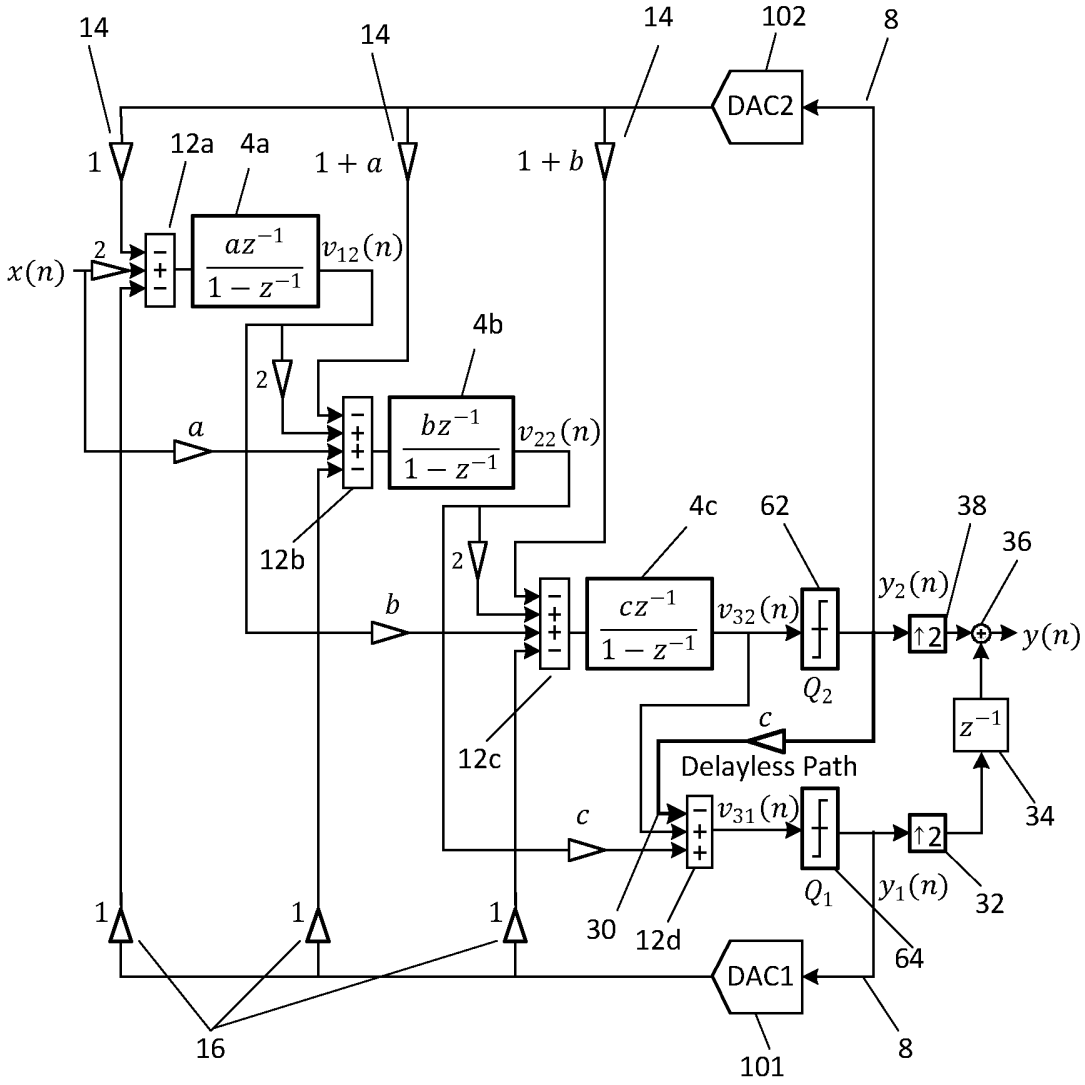


Figure 3: A 3rd-order single-loop two path DTTI ΔΣ modulator.

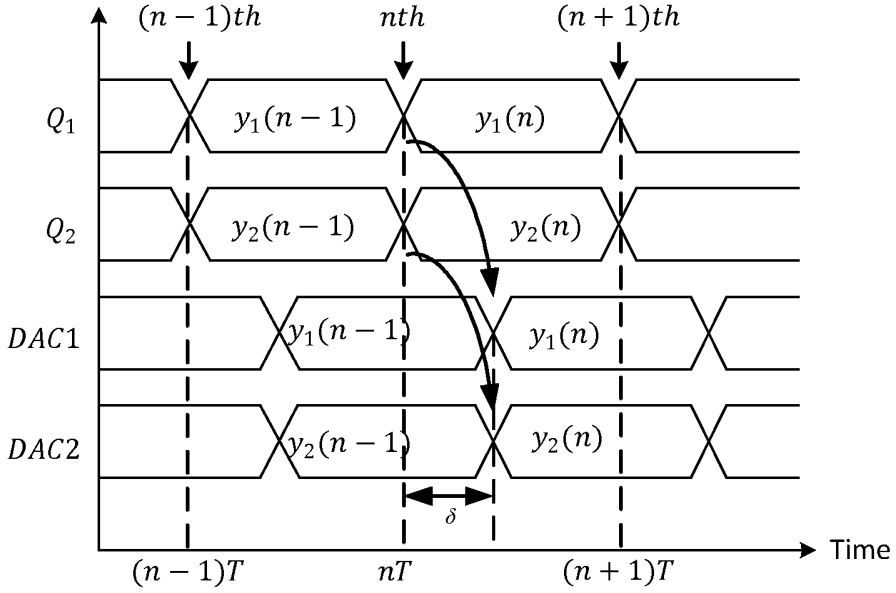


Figure 4: The outputs of Q1, Q2, DAC1 and DAC2.

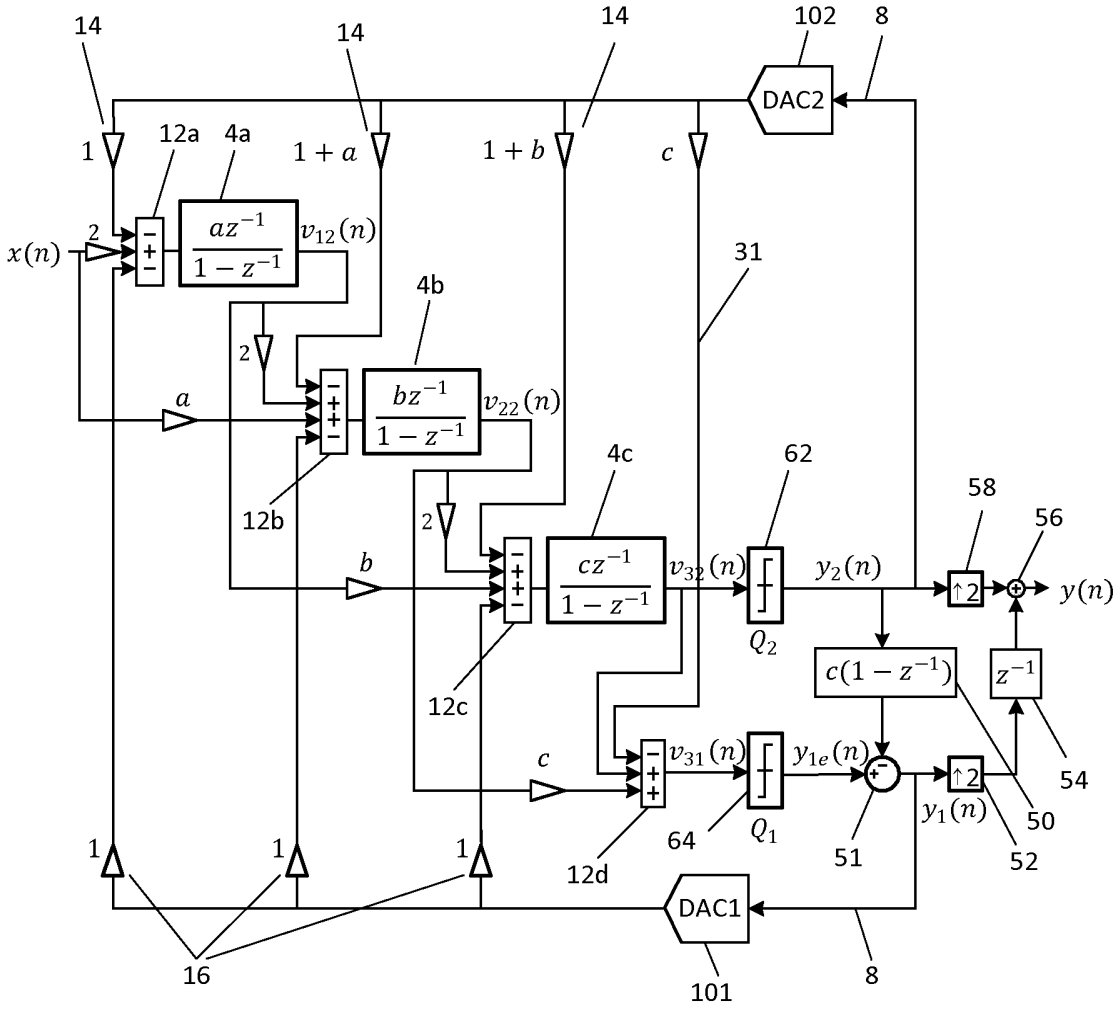


Figure 5: A 3rd-order single-loop two path DTTI ΔΣ modulator

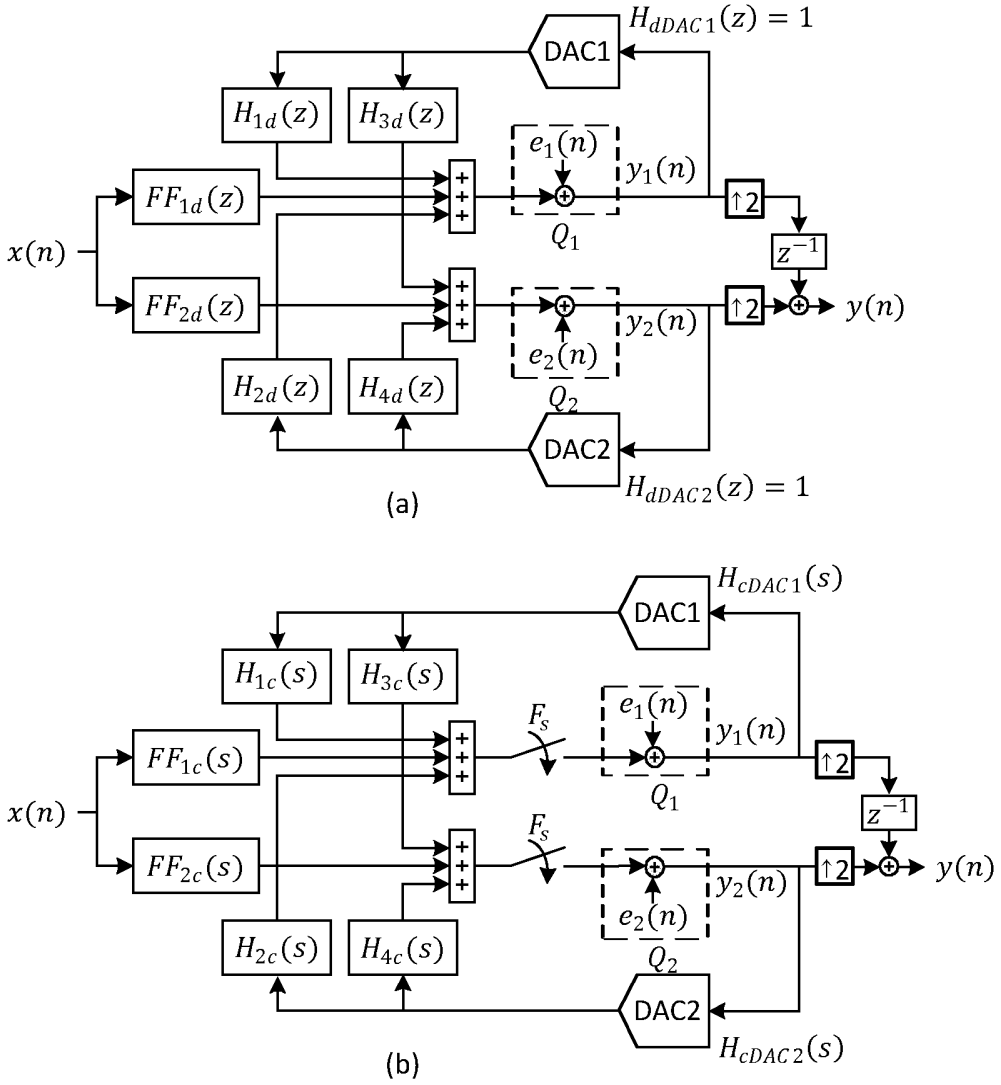


Figure 6: Block diagrams of a) a DTTI ΔΣ modulator and b) a CTTI ΔΣ modulator.

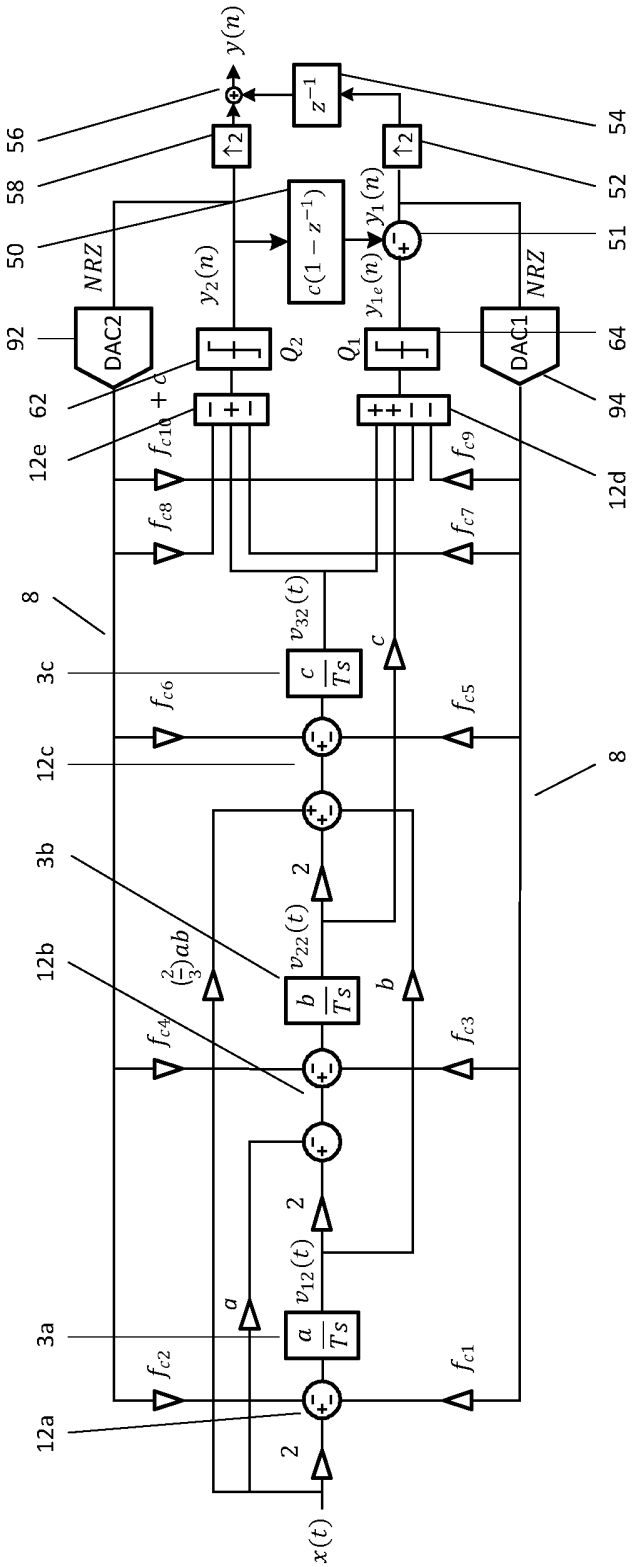


Figure 7: A 3rd-order single-loop two path CTTI ΔΣ modulator.

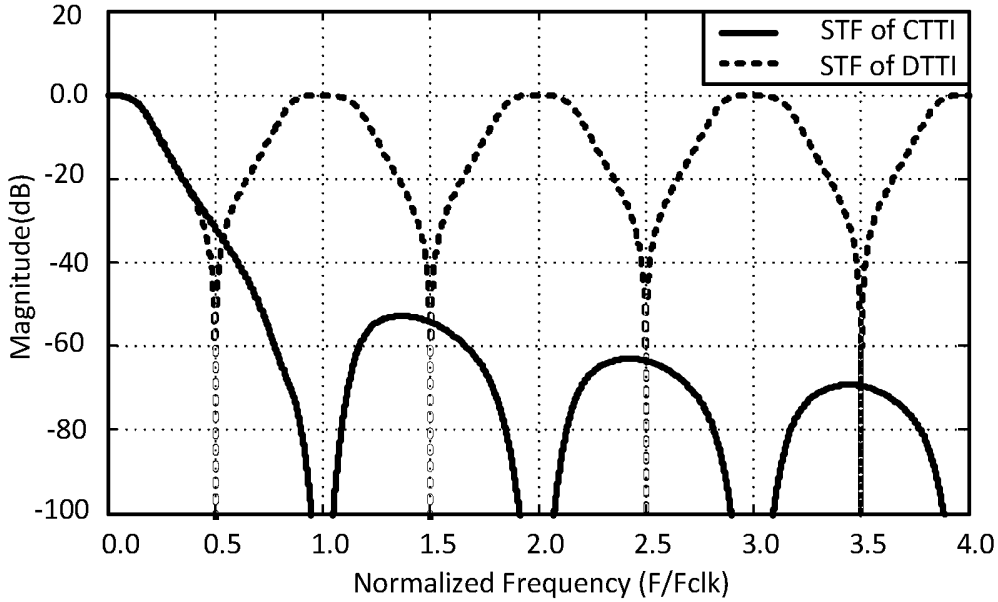


Figure 8: Signal transfer functions of DTTI and CTTI ΔΣ modulators.

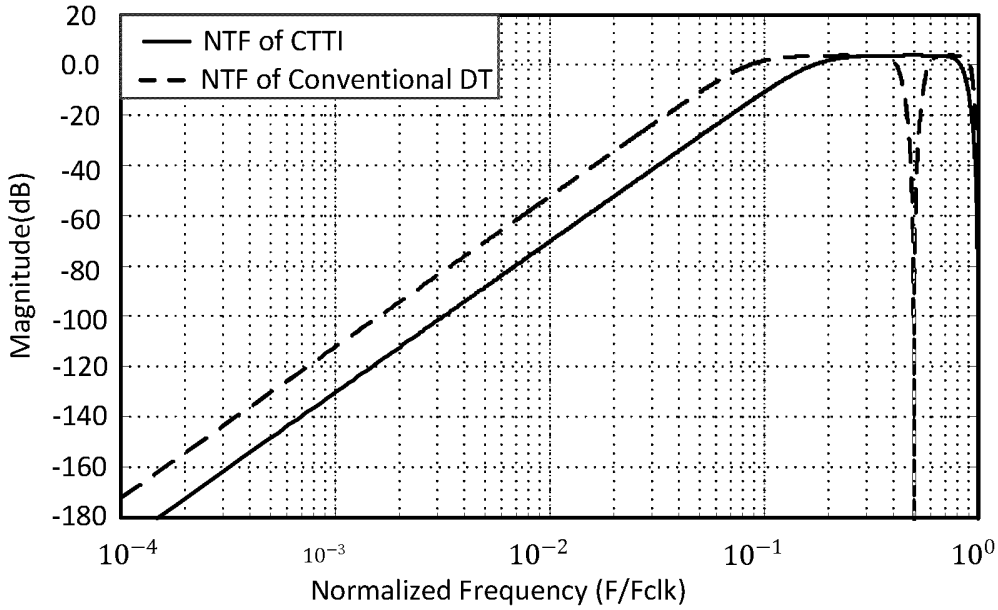


Figure 9: Noise transfer functions of the CTTI and the DT ΔΣ modulators.

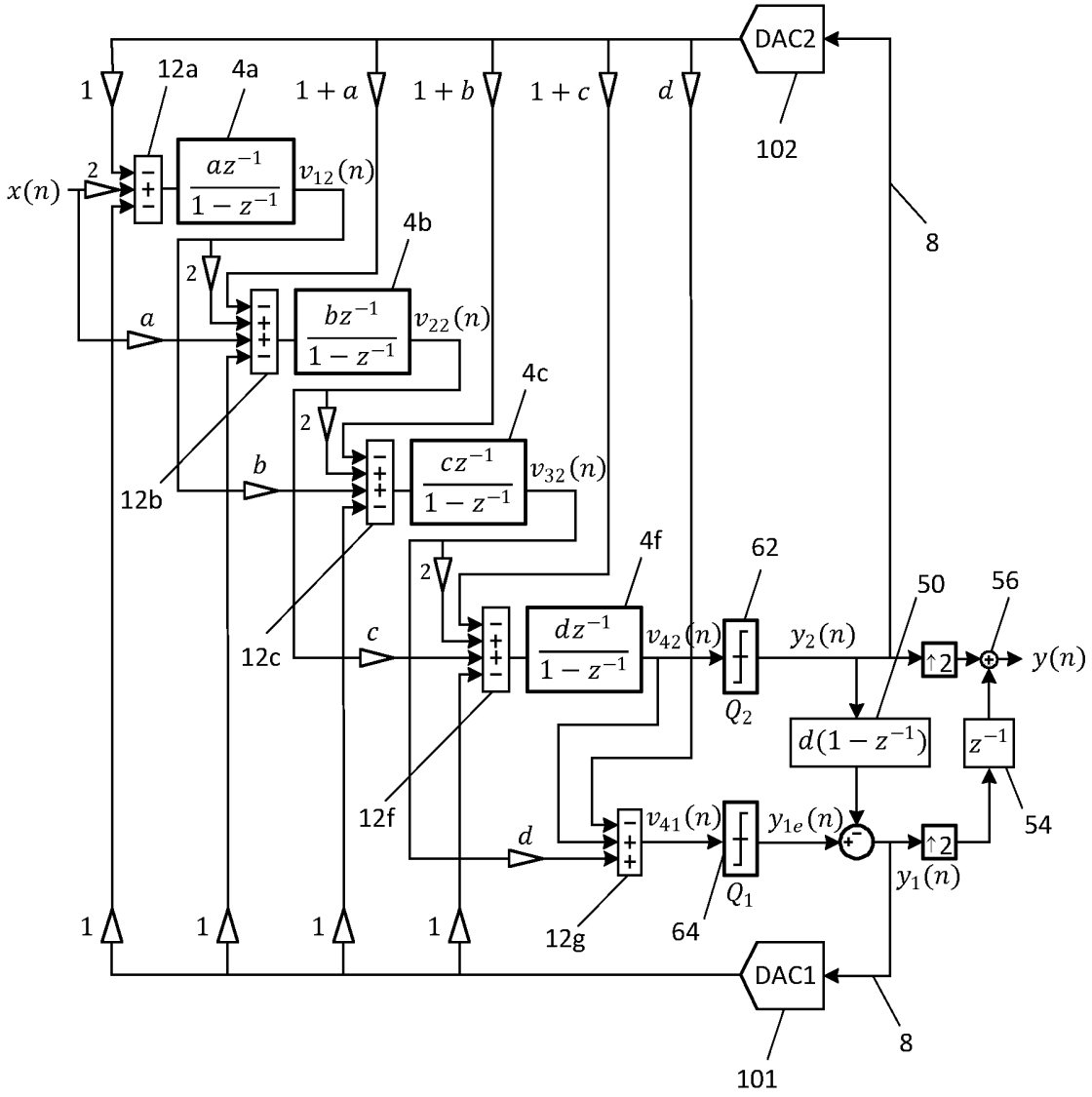


Figure 10: A 4th-Order Two-Path Discrete-Time Time-Interleaved Delta Sigma Modulator

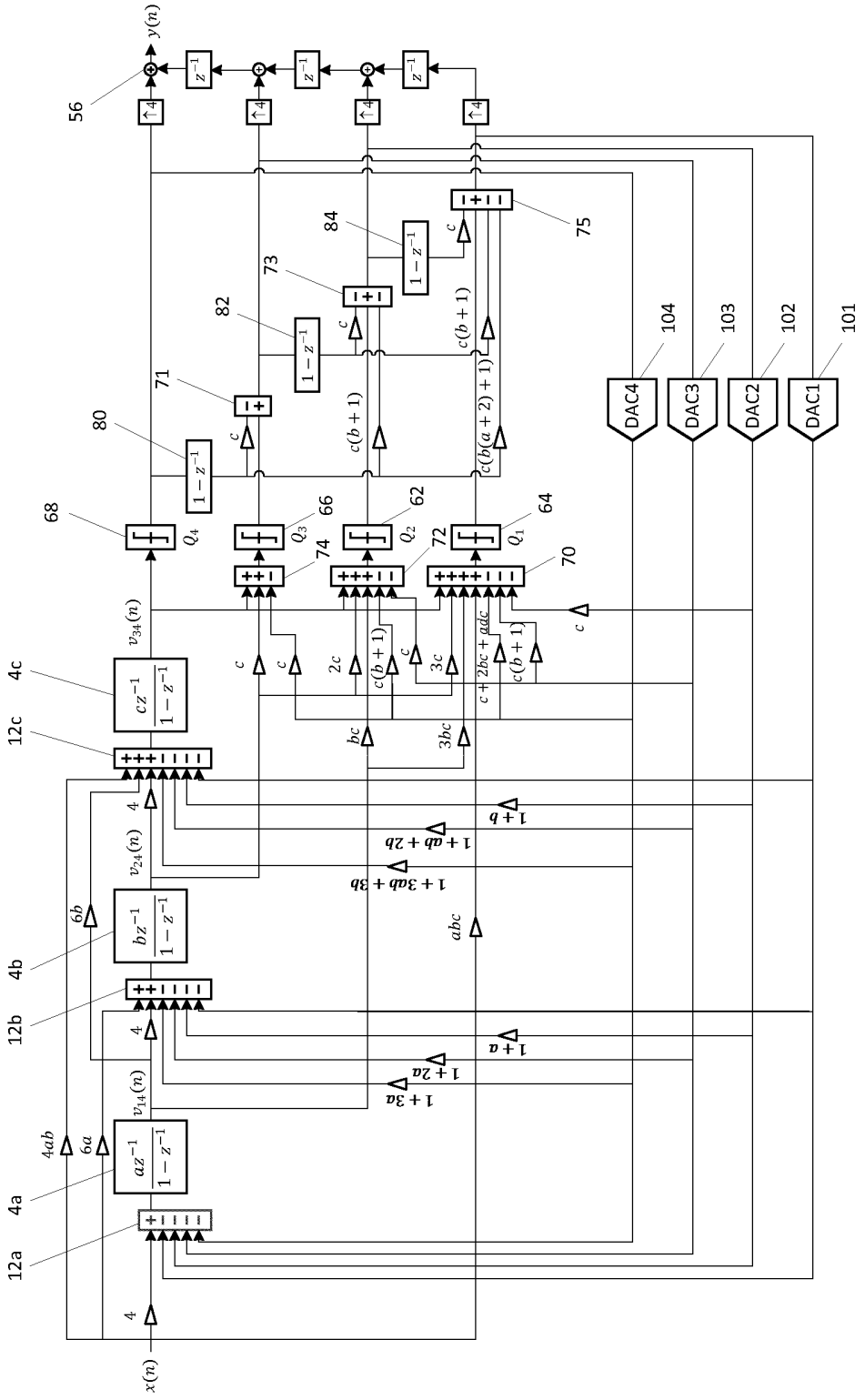


Figure 11: A 3rd-Order four-Path Discrete-Time Time-Interleaved Delta Sigma Modulator.

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/056425

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M3/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KYE-SHIN LEE ET AL: "Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator", ANALOG INTEGRATED CIRCUITS AND SIGNAL PROCESSING, KLUWER ACADEMIC PUBLISHERS, BO, vol. 43, no. 3, 1 June 2005 (2005-06-01), pages 225-235, XP019204021, ISSN: 1573-1979, DOI: 10.1007/S10470-005-1604-3 cited in the application the whole document ----- -/--	1-13

[X] Further documents are listed in the continuation of Box C.

[ ] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 June 2015	02/07/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Galardi, Leonardo

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/056425

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CALDWELL T C ET AL: "A time-interleaved continuous-time /spl Delta//spl Sigma/ modulator with 20MHz signal bandwidth", SOLID-STATE CIRCUITS CONFERENCE, 2005. ESSCIRC 2005. PROCEEDINGS OF THE 31ST EUROPEAN, IEEE, PISCATAWAY, NJ, USA, 12 September 2005 (2005-09-12), pages 447-450, XP010854998, DOI: 10.1109/ESSCIR.2005.1541656 ISBN: 978-0-7803-9205-2 cited in the application the whole document -----	1-13