UNIVERSITY OF LIVERPOOL

THE DESIGN AND DEVELOPMENT OF AN ORGANIC COMPARATOR FOR USE IN LOW COST SMART SENSOR SYSTEMS

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ABSTRACT

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This thesis chiefly examines ways of increasing the frequency response of circuits through using organic materials with high charge carrier mobility values as well as by reducing the overlap parasitic capacitances in thin film transistors (TFTs) by developing and optimizing of a self-aligned gap (SAG) fabrication process. The organic materials studied in this work include: Polytriarylamine (PTAA), Poly 3-hexylthiophene (P3HT), Poly [2, 5-bis (3-hexadecylthiophen-2-yl) thieno [3, 2-b] thiophene] (PBTTT-C16) and Indacenodithiophene-co-benzothiadiazole (IDTBT-C16). The electrical characterisation of the above-mentioned polymers are carried out using Schottky diodes, OTFTs and saturated-load inverters. The analysis of these devices is done with the aid of appropriate organic models developed in this work, which assume an exponential approximation to the tail of the Gaussian Density of States (DOS). Key material parameters of the disordered models i.e. the Meyer Neldel energy (*MNE*), the characteristic temperature of the DOS (T_C), the mobility prefactor (K) and the degree of disorder (m) are subsequently utilised in the design of organic circuits in Cadence design software.

A temperature study of PBTTT-C16 and IDTBT-C16 polymers is carried out using vertical Schottky diode with the aim of investigating the conduction mechanisms present in the films. The values of T_0, T_C and *MNE* of the PBTTT-C16 diode, obtained from the forward characteristics, are found to be 707.5 K, 523.6 K and 45 meV respectively and the values of the IDTBT-C16 diode are found to be

343.6 K, 382.7 K and 33.0 meV respectively. The acceptor density value, N_A, of the PBTTT-C16 diode is obtained from the semi-logarithmic plot of J_R versus $V_R^{1/4}$ and found to be 1.59×10^{22} m^{-3}. The activation energy, E_A, values of the PBTTT-C16 and IDTBT-C16 devices are 126 meV and 339 meV respectively, with the higher E_A value obtained for the IDTBT-C16 polymer being because of the large intermolecular π-stacking distances present in the polymer.

A SAG process that utilizes a bi-layer photoresist structure to create an undercut is developed. The size of the undercut formed from the process is found to vary inversely with the soft bake temperature and time. Utilizing the various gap sizes formed from the process, lateral PTAA diodes are fabricated and characterized accordingly. With the gap size increasing from 0.05 µm to 2 µm, the forward current density values decreases inversely from 15.86 Am^{-2} to 0.31 Am^{-2} due to an increase in the series resistance of the devices. Similarly, the conduction mechanism in the devices is found to be more limited by contact resistance effects as the gap size decreases. In addition, the N_A values obtained from the devices ranges from 2.33×10^{20} m^{-3} to 1.76×10^{21} m^{-3}. Interestingly enough, CV measurements and SILVACO simulations of these devices show that the modulation of the depletion layer in devices with a lateral topology is chiefly dependent on the electrode spacing and area of the active layer rather than the film thickness as is typically observed in vertical diodes.

The parameters of a PBTTT-C16 self-aligned transistor with an aspect ratio of 50 are utilized in the design and modelling of organic circuits within this work. The device has a sub-threshold swing of −1.8 V/decade, an on/off

ratio of 4.26×10^{2}, a saturation field effect mobility value, μ_{fe} of $0.74\ cm^{2}\ V^{-1}\ s^{-1}$ and a threshold voltage, V_T of −1.5 V. Utilizing the disordered model developed in this work, the values of *m*, *K*, T_C and *MNE* are 0.57, $2.15\times10^{-16}\ AV^{-m}$, 473 K and 41 meV respectively. These parameters are subsequently used in Cadence design software to create a compatible OTFT model for subsequent design of an organic comparator. The comparator has a maximum gain of 45.62 dB and operates at a 300 Hz frequency. A PBTTT-C16 saturated load inverter with a gain of 12.4 dB and an average propagation delay of 3.4 ms is also fabricated using the Cadence mask designs developed for the SAG process. A study of the effect of varying the width of the driver transistor of the inverters as well as the use of materials with lower mobility values is also investigated. The challenges of the SAG process are also highlighted with possible methods to circumvent and in some cases eliminate them presented as well.

Dedicated

to

My Loving Family

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ABBREVIATIONS

α-NPD	*N*,*N*^{I}-diphenyl-*N*, *N*^{I}-bis (1-naphthyl)-1, 10-biphenyl–4,4^{II}-diamine
AC	Alternating Current
ADC	Analogue to Digital Converter
AFM	Atomic Force Microscope
Al	Aluminium
Al_20_3	Aluminium oxide
Au	Gold
C_{60}	Buckminsterfullerene
CDM	Correlated Disorder Model
CMOS	Complementary Metal-Oxide Semiconductor
CV	Capacitance-Voltage
Cr	Chromium
DAC	Digital to Analogue Converter
DC	Direct Current
DFT	Discrete Fourier Transform
DOS	Density of States
EGDM	Extended Gaussian Disorder Model
GDM	Gaussian Disorder Model
HOMO	Highest Occupied Molecular Orbital
IDTBT-C16	Indacenodithiophene-co-benzothiadiazole
IP	Ionization Potential
IV	Current-voltage
J-V	Current density-voltage
KPFM	Kelvin-Probe Force Microscopy
LOR	Lift-off resist
LUMO	Lowest Unoccupied Molecular Orbital

MEE	Multiexcitation entropy
MIM	Metal Insulator Metal
MNE	Meyer Neldel Energy
MNR	Meyer Neldel Rule
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTR	Multiple trap and release
NMOS	*N*-type Metal-Oxide-Semiconductor
OC_1C_{10}-PPV	Poly (2-methoxy-5-(3', 7'-dimethyloctyloxy)-p-phenylene vinylene)
OFET	Organic Field Effect Transistor
OLED	Organic Light Emitting Diode
OSC	Organic semiconductor
OTFT	Organic thin-film transistor
P3HT	Poly 3-hexylthiophene
PBTTT-C16	Poly[2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene]
PFBT	Pentafluorobenzenethiol
PMOS	*P*-type Metal-Oxide-Semiconductor
PTAA	Polytriarylamine
RFID	Radio Frequency Identification Tag
SAG	Self-aligned gap
SAM	Self-assembled monolayer
SCLC	Space charge limited current
Si	Silicon
SiC	Silicon Carbide
TCAD	Technology computer-aided design
TE	Transport Energy
UML	Universal Mobility Law
UV	Ultra-violet

VASE	Variable angle spectroscopic ellipsometry
VRH	Variable range hopping
ZnO	Zinc oxide

SYMBOLS

A	*Area (m^2)*
A^*	*Richardson constant ($A\ cm^{-2}\ K^{-2}$)*
B_C	*The critical number for the onset of percolation*
C	*Capacitance (F)*
C_{dep}	*Capacitance of the depletion region (F)*
C_{OX}	*Oxide capacitance (F)*
D_{ij}	*Distance between two hopping states (m)*
D_n, D_p	*Diffusion coefficient for electrons, holes (m^2s^{-1})*
E	*Energy (eV)*
E_a	*Activation energy (eV)*
E_b	*Mean energy (eV)*
E_{Bar}	*Energy of the top of the barrier (eV)*
E_C	*Energy of the conduction band edge (eV)*
E_F	*Extrinsic Fermi level (eV)*
E_g	*Energy band gap (eV)*
E_i	*Intrinsic Fermi level (eV)*
E_t	*Energy of the trap states (eV)*
E_T	*Transport energy level (eV)*
E_V	*Energy of the valence band edge (eV)*
E_{vac}	*Energy at vacuum level (eV)*
F	*Electric field strength (Vm^{-1})*
$\overline{F}_{Bn}$	*Mean value of the barrier height (eV)*
F_{max}	*Maximum electric field (Vm^{-1})*
F	*Frequency (Hz)*
$f_i\ (T)$	*Probability that site i (located at R_i and with an energy i) will be occupied*
$F(E)$	*Fermi Dirac distribution function*
G_{ij}	*Intersite conductance (AV^{-1})*
g_d	*Channel conductance (AV^{-1})*
g_m	*Transconductance (AV^{-1})*
H	*Planck's constant (Js)*
$\hbar$	*Reduced Planck's constant (Js)*
I	*Current (A)*
$I_{Diffussion}$	*Diffusive current (A)*
I_{Drift}	*Drift current (A)*
J	*Current density (Am^{-2})*
J_0	*Saturation current density (Am^{-2})*
K	*Boltzmann's constant (eV/K)*
kT/q	*Thermal voltage at 300K*
kT_C	*MNE (eV)*
K	*Prefactor in the Universal Mobility Law ($cm^{-2}V^{-1}s^{-1}$)*

l_{gap}	*Distance between two electrodes (m)*
L	*Grain size (m)*
L	*Length (m)*
L_{Debye}	*Debye length (m)*
M	*Exponent in the Universal Mobility Law dependent on T_C and the material*
m^*	*Effective carrier mass (kg)*
$N'(E)$	*Effective DOS at energy level, E (cm^{-3})*
$N'(0)$	*The rate of change of density of traps with energy (cm^{-3})*
n, n_{free}	*Electron concentration (cm^{-3})*
n_i	*Intrinsic electron concentration (cm^{-3})*
N_A	*acceptor electron concentration (cm^{-3})*
N_{SC}	*Density of space-charge per unit volume per hole volt (cm^{-3})*
N_{SS}	*Density of surface states per unit area per hole volt (cm^{-3})*
N_T	*DOS at the transport energy (cm^{-3})*
N_t	*Density of trap states (cm^{-3})*
N_0	*DOS at energy (cm^{-3})*
N_V	*Effective DOS in the valence band (cm^{-3})*
p_f	*Free hole concentration (cm^{-3})*
p_i	*Intrinsic hole concentration (cm^{-3})*
p_t	*Trap carrier (hole) concentration (cm^{-3})*
Q_{dep}	*Charge in depletion region (C)*
Q_{fixed}/Q_{ox}	*Fixed oxide charge (C)*
Q_s	*Magnitude of charge at the interface of the oxide and semiconductor (C)*
Q_{it}	*Interface trap charges (C)*
Q	*Electronic charge (C)*
qV_{bi}	*Built-in potential (eV)*
$Q\chi$	*Electron affinity (eV)*
R_C	*Contact resistance (Ω)*
Rs	*Series resistance (Ω)*
S	*Sub-threshold swing (V/decade)*
T	*Generic thickness (m)*
	Time (s)
T	*Absolute temperature (K)*
T_0	*Characteristic temperature associated with the distribution of carriers (K)*
T_C	*Characteristic temperature associated with the exponential density of states distribution (K)*
t_{eff}	*Effective thickness (m)*
t_{osc}	*Thickness of the organic semiconductor layer thickness (m)*
t_{ox}	*Dielectric thickness (m)*
$\bar{v}$	*the electron mean velocity ($m \cdot s^{-1}$)*
V	*Voltage (V)*
V_{app}	*Applied voltage (V)*

V_{bi}	*Built-in voltage (V)*
V_{bulk}	*Voltage across the bulk of the semiconductor (V)*
υ_D	*Effective diffusion velocity (ms^{-1})*
υ_R	*Effective surface recombination velocity (ms^{-1})*
V_D	*Drain voltage (V)*
V_G	*Gate voltage (V)*
V_T	*Threshold voltage (V)*
W, w	*Generic width (m)*
W_{dep}	*Width of the depletion region (m)*
W_{ij}	*Transition rate from an occupied site (i) to an unoccupied site (j)*
W_{max}	*Maximum depletion region width (m)*
X	*Generic thickness/ distance (m)*
x_p	*Semiconductor thickness (m)*
x_{max}	*Distance from the metal/semiconductor interface at $\Delta\phi_B$ (m)*
Y_{00}	*Constant prefactor*
A	*Inverse localization length (m)*
Δ	*Fraction of localized states occupied by the carrier*
ε_0	*Permittivity of free space*
E	*Relative dielectric constant*
ε_s	*Dielectric constant of the oxide*
ε_{ox}	*Static dielectric constant of the semiconductor*
ε_∞	*High frequency permittivity of the semiconductor*
Θ	*Ratio of the free carriers to the total carriers*
H	*Ideality factor*
μ	*Mobility ($m^2V^{-1}s^{-1}$)*
μ_0	*Mobility prefactor ($m^2V^{-1}s^{-1}$)*
μ_{eff}	*Effective mobility ($m^2V^{-1}s^{-1}$)*
μ_{fe}	*Field-effect mobility ($m^2V^{-1}s^{-1}$)*
μ_m	*Measured mobility ($m^2V^{-1}s^{-1}$)*
P	*Resistivity (Ωm)*
Σ	*Conductivity ($\Omega^{-1}m^{-1}$)*
	Variance of the width of the DOS
σ_F	*Standard deviation of the barrier height (eV)*
σ_W	*Width of a Gaussian function (eV)*
σ_0	*Conductivity prefactor ($\Omega^{-1}m^{-1}$)*
N	*Frequency of the carriers (s^{-1})*
ν_0	*Attempt-to-Hop frequency (s^{-1})*
λ_i	*The decay rate of the excited charge at site i*
Ψ	*Potential needed to induce satisfactory accumulation or inversion of carriers (V)*
X	*Electron affinity (eV)*
Φ	*Electrostatic potential (V)*
ϕ_B	*Metal-semiconductor barrier height (V)*

$\Delta\phi_B$	*Metal-semiconductor barrier lowering (V)*
ϕ_m	*Metal work function (V)*
ϕ_s	*Semiconductor work function (V)*

CHAPTER 1

Introduction

This chapter gives a short summary of organic materials and their use in applications for the microelectronics industry. A literature survey of the current state of the art organic analogue circuits is also outlined. The key challenges facing the realisation of organic materials in circuit applications are also highlighted. Lastly, the thesis organisation, experimental characterisation techniques and the contributions from this thesis are presented.

1.1 INTRODUCTION TO ORGANIC SEMICONDUCTORS AND ORGANIC CIRCUIT TECHNOLOGY

The field of organic electronics has grown immensely since the discovery of the electrical conductivity of carbon-based materials made by Chiang et al [1]. Whilst most electronic applications utilize silicon and its derivatives in the semiconductor industry, organic materials offer a specific set of advantages particularly useful in applications that require mechanical flexibility along with large area integration at an affordable cost. These benefits include amongst others the ease of device fabrication, as they do not require high vacuum and high temperature conditions for processing, mechanical flexibility, lightness and solution processing capability, which enables the possibility of large-scale mass production through processes such as roll-to, roll printing. The above-mentioned features are well suited for applications such as flexible displays, RFID tags and integrated smart sensor systems.

Presently, there have been quite a number of advancements in the development of organic digital circuitry such as RFID tags [2-5], shift registers [6-8] and microprocessors [9,10]. Analogue circuitry, on the other hand, is still in its early stages because of issues facing organic electronics, which will be mentioned briefly. In spite of this, there has still been reasonable progress in the design of organic analogue circuits such as the development of analogue to digital converters (ADC) [11-15], comparators [11,12,16-21] and operational [12,19,20] and differential amplifiers [22-24]. Nonetheless, to realise more fully functional integrated mixed signal circuits, more research into analogue circuit designs is needed.

One of the major challenges of organic materials is the poor intrinsic charge carrier mobility values, which results in low transconductance values and low intrinsic transistor gains. In addition to this, most designs use large parameters for the specifications of the channel width and length of the transistor with the aim of increasing the driving capability of devices. This results in large overlap parasitic capacitances thereby inherently limiting the speed of operation of the devices. Subsequently, a lot of research work has been undertaken to improve the mobility of organic materials with reported values of about 10 cm^2/V s for *p*-type organic semiconductors [25] and 0.76 cm^2/Vs [26] for *n*-type organic semiconductors respectively. However, most organic materials with high mobility values greater than 10 cm^2/Vs are typically crystalline organic semiconductors, which are usually deposited via thermal evaporation, which negates the pitch for solution processing as an alternative fabrication methodology for organic semiconductors. In addition, the lower mobility values of the few,

available *n*-type organic semiconductors make it difficult for the realisation of CMOS circuits. The development of organic CMOS circuits is equally challenging because of the added complexity of fabricating two different polymers on the substrate without affecting the functionality of either of the two. Similarly, the need for different metal layers for the power supply rails further complicates the fabrication process. This thereby restricts most analogue engineers to designing circuits using only *p*-type transistors further limiting the options of the different device topologies to be used. Currently most mature state of the art organic analogue designs employ *p*-type only topologies in comparison to a CMOS type as shown in *Table 1.1* below.

Table 1. 1: *A summary of the current state of the art analogue organic circuits in literature. Most of the analogue circuit topologies use p-type only transistors due to the few number of stable n-type transistors and the lack of robust, repeatable complementary fabrication processes.*

Type of Circuit	**Circuit type**	**Power Supply (V)**	**References**
ADC	CMOS	10	H. T. Pham, T. V. Nguyen, L. Pham-Nguyen, H. Sakai, and T. T. Dao [11].
	PMOS	15	H. Marien, M. S. J. Steyaert, E. v. Veenendaal and P. Heremans [12].
	PMOS	20	D. Raiteri, P. v. Lieshout, A. v. Roermund and E. Cantatore [13].
	CMOS	3	W. Xiong, U. Zschieschang, H. Klauk, and B. Murmann [14].
	CMOS	40	S. Abdinia *et al* [15].
Comparator	PMOS	20	H. Marien, M. Steyaert, N. v. Aerle, and P. Heremans [16].
	PMOS	20	D. Raiteri, F. Torricelli, P. v. Lieshout, A. H. M. v. Roermund, and E. Cantatore [17].
	PMOS	10	M. Torres-Miranda, A. Petritz, A. Fian, C. Prietl, H. Gold, H. Aboushady, Y. Bonnassieux and B. Stadlober [18].
	CMOS	50	G. Maiellaro, E. Ragonese, A. Castorina, S. Jacob, M. Benwadih, R. Coppard, E. Cantatore and G. Palmisano [19].
	PMOS	5	I. Nausieda, K. K. Ryu, D. D. He, A. I. Akinwande, V. Bulovic and C. G. Sodini [20].
	CMOS	40	S. Abdinia *et al* [21].
	PMOS	15	H. Marien, M. S. J. Steyaert, E. v. Veenendaal and P. Heremans [12].
Operational amplifier	PMOS	15	H. Marien, M. S. J. Steyaert, E. v. Veenendaal and P. Heremans [12].
	PMOS	5	I. Nausieda, K. K. Ryu, D. D. He, A. I. Akinwande, V. Bulovic and C. G. Sodini [20].
	CMOS	50	G. Maiellaro, E. Ragonese, A. Castorina, S. Jacob, M. Benwadih, R. Coppard, E. Cantatore and G. Palmisano [19].
Differential amplifier	CMOS	40	M. Guerin, A. Daami, S. Jacob, E. Bergeret, E. Benevent, P. Pannier and R. Coppard [22].
	PMOS	40	J. Chang, X. Zhang, T. Ge and J. Zhou [23].
	PMOS	40	N. Gay and W. J. Fischer [24].

An additional issue of organic based circuits is the low dielectric capacitance values and hence high threshold voltage values obtained because of using polymer dielectrics with

low dielectric constants or in other cases using inorganic dielectrics such as silicon dioxide with equally low dielectric constant values. Alternatively, the use of high k-dielectrics that can be grown or processed with low temperatures have been researched into in literature [27] as well as in this thesis. Opting to use higher k-dielectrics also helps reduce the power supply rail values needed for organic circuits thereby reducing the overall power dissipated from the circuits [28]. It is evident from *Table 1.1* that even to date most of the state of the art organic circuits operate at relatively high power supply voltages.

TFT parameters such as the mobility and threshold voltage values are unstable because of environmental factors such as water vapour and oxygen doping effects, which thereby pose another major challenge in the design of organic circuits. Such variations typically result in mismatching of devices across a substrate and as such, affecting the overall circuit performance. Robust organic circuit designs are thereby needed in order to withstand/ cope with such variations. Organic material designs can be made less susceptible to oxygen doping effects by reducing the HOMO level of materials [29]. In addition, encapsulation of the devices [30,31] reduces susceptibility to oxygen and water vapour effects. The latter option is however not within the scope of study in this thesis.

The first aim of this thesis is to create compact organic models within Cadence circuit design software. This is achieved by modifying pre-existing Silicon PSpice DC model parameters to take into account the larger power law factor typically observed in disordered organic devices.

The second aim is to increase the frequency response of organic circuits, specifically the speed and the bandwidth, by primarily developing a fabrication process that reduces the overlap parasitic capacitances within the circuits. It is well known that the overlap capacitance between the source/drain contacts and the gate dielectric accounts for a large percentage of the load capacitance in organic circuits therefore adopting a self-aligned transistor process would ideally improve the frequency response of the circuit as well as the reproducibility of the circuit performance. Interestingly enough, to the best of our knowledge, there is insufficient literature on the fabrication of organic analogue circuits using a self-aligned process. In fact, in the previous table, Torres-Miranda et al [18] only recently adopted a self-aligned fabrication process to address the frequency response of organic analogue circuits, obtaining an organic comparator having a clock frequency of 10 kHz and an operational amplifier with a gain-bandwidth (GBW) of 3 kHz using only *p*-type transistors. In this work, a *p*-type saturated-load

circuit topology is likewise adopted for the performance analysis of the self-aligned circuits as it has been shown to be robust in withstanding variations of Thin Film Transistor (TFT) parameters.

Lastly, high mobility solution-based organic materials are adopted for fabrication of the circuits to improve the frequency response of the circuits. In addition to this, the mobility of the organic semiconductor is enhanced by modifying the interface of the dielectric and the semiconductor by reducing the surface energy and roughness of the dielectric layer through annealing of the dielectric layer as well as through surface treatments such as oxygen plasma, UV ozone radiation and using self-assembled monolayers (SAM). Annealing of the dielectric is known to reduce the surface energy of the dielectric and also to improve the electrical performance of devices through reduction in the water vapour content between the dielectric/organic semiconductor interface [32]. Moreover, with the reduction in the surface energy of the dielectric, the polymer layer would subsequently have a better morphology, which thereby enhances the mobility of the semiconductor and hence improves the frequency response of the organic devices and circuits.

1.2 ORGANISATION OF THE THESIS

The following section gives a brief overview of the details of each chapter found within this thesis.

Chapter 2 begins by describing the equivalent band structure of organic semiconductors utilising the Hückel Molecular Orbital theory. A literature survey of the charge transport models developed for disordered organic semiconductors is also presented. Moreover, the impact of the Meyer Neldel Energy (*MNE*) within the framework of charge transport in disordered organic materials is investigated. The *MNE* is widely believed to be associated with the width of the Gaussian DOS distribution and thereby provides a means of assessing the degree of disorder within a material. An analytical model for charge transport is presented in this thesis assuming the aforementioned sentiments. In the model, the dependency of the effective mobility on carrier concentration, normally referred to as the Universal Mobility Law (UML), is established. By incorporating the developed mobility model, expressions for the current density in organic Schottky diodes and OTFTs are also modelled. These disordered

models form the basis for the modelling, designing and development of organic circuits used in this work.

Chapter 3 is primarily concerned with the study of the charge transport mechanisms of solution based, high charge carrier mobility, thiophene polymers. The investigation is carried out with the aid of the temperature variation of the current-density voltage characteristics of two vertical Schottky diodes having indacenothiophene–benzothiadiazole (IDTBT-C16) and poly [2, 5-bis (3-hexadecylthiophen-2-yl) thieno [3, 2-b] thiophene] (PBTTT-C16) polymers as the active layer. The activation energy, which is a significant parameter in understanding and establishing the mechanism of charge transport in conjugated polymers, is also obtained from the Arrhenius plots of the forward current density taken at relatively high temperatures. Additionally, the quantitative modelling of the forward and reverse characteristics of the two Schottky diodes is also carried out using the disordered Schottky model developed in chapter 2.

Chapter 4 deals chiefly with the development and optimisation of a self-aligned gap (SAG) process, which is later used for the fabrication of lateral organic devices and circuits on the same substrate. The optimisation of the process is carried out via optical characterisation studies as well as electrical scaling studies utilising Polytriarylamine (PTAA) lateral Schottky diodes. Based on the optimised process, PBTTT-C16 OTFTs are realised and the electrical characteristics are fitted to the disordered OTFT model derived in chapter 2. Key material parameters obtained from the fittings are compared to and validated with those obtained from the electrical characterisation of the Schottky diodes made using the same material given in Chapter 3.

Chapter 5 deals with the incorporation of the disordered organic models developed in chapter 2 into a commonly used circuit design software, Cadence, for later use in the aid of designing organic devices and circuits. This is realised through modification of the in-built silicon models. By employing the modified models, various analogue and digital circuit blocks are designed using only *p*-type transistors. The results of the fabricated circuits are discussed and compared to the simulated designs. Furthermore, challenges of the SAG process are also presented with possible suggestions for future works.

Chapter 6 gives a conclusion of the work carried out in this thesis as well as the key challenges. Recommendations for future works are also explored in this chapter.

1.3 EXPERIMENTAL TECHNIQUES/CHARACTERISATION

The fabrication of the organic devices (i.e. lateral/vertical diodes and OTFTs) and circuits is carried out in clean ambient conditions and in the presence of yellow light. Given that the fabrication techniques vary depending on the type of device/circuit being made, more details on the fabrication steps will be provided in the relevant sections of the thesis. On the other hand, the main characterisation techniques carried out in this thesis (i.e. electrical and optical characterisation) are described in this section.

The electrical characterisation carried out in this work includes direct current (*DC*), current-voltage (*IV*), capacitance-voltage (*CV*), frequency and transient measurements. The *DC* and *IV* characterisation of the circuits and devices is performed using a PC controlled Agilent B1500A semiconductor parameter analyser. Temperature studies of the *IV* measurements of vertical Schottky diodes are also carried out using a B1500A semiconductor parameter analyser connected to a Keithley 615 electrometer and 230 Voltmeter. Each of the samples is secured onto a holder, which is then placed into a liquid nitrogen cryostat under a vacuum pressure of 0.1 mbar. *CV* measurements of lateral diodes is carried out using an E4980A precision LCR meter. The samples are secured onto the sample stage of the measurement rig using a vacuum chuck to cancel out any environmental disturbance. Alternating current (*AC*) and transient measurements of circuits are done using a set-up equipment consisting of an Agilent 33320A signal waveform generator and two power supply units connected to the circuit under test. The input signal comprised of a 15 V peak to peak step signal with varying values of frequency and the output is measured using an Agilent 54621D oscilloscope.

The characterisation of the gap sizes obtained from the self-aligned process is done using a Veeco CP-II Atomic Force Microscope (AFM). One can obtain the three dimensional profile of a sample using this technique as it measures a sample in the horizontal X-Y plane and the vertical Z dimension. To avoid damaging of the samples, all characterisation is done in non-contact imaging mode. Imaging in non-contact mode may sometimes result in obtaining a lower image resolution [33]. Unlike contact AFM mode, non-contact AFM mode has a tip that hovers at a distance of around 50 to 150 Angstroms above the surface of the sample [34]. Attractive forces such as Van der Waals forces and electrostatic forces acting between the cantilever tip and the sample are detected and topographic images are produced as a result of scanning the tip of the cantilever directly above the sample surface. In non-contact AFM imaging, the attractive forces from the surface are much weaker than those used in contact

mode. A small oscillation signal is thereby applied to the cantilever tip so that AC detection methods can be used to measure the amplitude, phase and/or the frequency response of the force gradients from the sample in order to detect the small forces between the tip and sample surface.

To achieve a high resolution image in non-contact mode, one needs to measure the force gradients from the Van der Waals forces which normally extend a few nanometres from the sample. Nonetheless, obtaining a high resolution image may sometimes be difficult particularly when imaging hydrophilic surfaces which can have a water layer that is significantly thicker than the range of the Van der Waals forces being investigated. In such a case, imaging of the "actual" surface might possbily be futile as the effective range of forces are beyond that which the oscillating probe hovers. Similarly, when a low oscillation amplitude is applied to the sample, the resolution of the image can be degraded as a result of the tip of the sample being unable to dislodge easily from the layer of water. It is adviseable therefore to perform AFM characterisation in an ultra-high vacuum environment in order to avoid having the water layer on the sample. A surface treatment of the samples prior to characterisation in conjunction with application of the appropriate oscillation signal is recommended if characterising in ambient air conditions.

Finally yet importantly, a J. A. Woollam M2000UI variable angle spectroscopic ellipsometry (*VASE*) kit is used to determine the thickness of the organic films used in this thesis. When light is reflected or transmitted from a material structure, there is a change in the polarization of the light, which is measured by the ellipsometry kit. The change is typically characterized by an amplitude ratio, Ψ, and a phase difference, Δ, as described using Fresnel's reflection and transmission equations [35]. The measured data varies depending on the thickness and optical properties of the materials. Upon measuring, one makes a comparison of the measured data to a user-defined model in order to estimate the thickness of the semiconductor. Given that the samples are characterised on silicon wafers, the first step in building the model is to extract the thickness of the native oxide layer on the wafer by utilising a Cauchy layer [36] as defined in the software. Having built a model for the first layer, a general oscillator layer is then used to estimate the thickness of the semiconductor layer using a regression analysis. The VASE software uses a Mean Squared Error (*MSE*) estimator to compute the difference between the measured data and the calculated data from the model. Good fits are assumed to be obtained when the MSE value is below 10.

1.4 CONTRIBUTIONS

The work carried out in this thesis has the following contributions:

- A model showing the dependency of mobility on carrier concentration is presented. Based on the model, disordered models for the current transport in organic Schottky diodes and TFTs are developed and subsequently used for modelling and designing of organic circuits.

- An analysis of the DC characteristics of vertical Schottky diodes based on PBTTT-C16 and IDTBT-C16 polymers is done. Utilising the organic Schottky diode model, key parameters such as the characteristic temperature associated with the distribution of carriers T_0, characteristic temperature associated with the intrinsic density of states T_C, and the Meyer Neldel Energy *(MNE)* are extracted. The respective values for the PBTTT-C16 diode are 707.5 K, 523.6 K and 45 meV and for the IDTBT-C16 diode, they are 343.6 K, 382.7 K and 33.0 meV respectively.

- Forward characteristics of vertical PBTTT-C16 Schottky diodes display a kink possibly due to resonant tunnelling. Nonetheless, a good fit is obtained for the semi-logarithmic plot of J_R versus $V_R^{¼}$ resulting in an acceptor density of 1.59×10^{22} m^{-3}.

- The semi-logarithmic plot of J_R versus $V_R^{¼}$ of the vertical IDTBT-C16 Schottky diode has poor fits.

- For the PBTTT-C16 Schottky diode, parameters such as the forward and reverse *J-V* characteristics, the effective mobility and the carrier concentration increases with increasing temperature. The same observation is made for the IDTBT-C16 Schottky diode with the exception of the reverse *J-V* characteristics, which did not have any visible temperature dependency.

- The activation energy, E_A of PBTTT-C16 and IDTBT-C16 is extracted from the Arrhenius plots of the forward current density against 1000/*T* and is found to be 126 meV and 339 meV respectively.

- The turn on voltage of the IDTBT-C16 Schottky diode shifted toward more negative values with reduction in temperature.

- A self-aligned gap (SAG) fabrication process is developed and consequently used for fabrication of organic devices and circuits.

- Optimisation of the SAG fabrication process is demonstrated through variation of the soft bake parameters of the photoresist; a reduction in the soft bake parameters results in an increase of the undercut size formed by the process.

- The forward current density values of lateral PTAA Schottky diodes increases with a decrease in the inter electrode distance due to the reduction in the series resistance of the devices.

- A 12.6 % film thickness variation of lateral PTAA Schottky diodes resulted in a variation of the reverse current density values with values ranging from 2.78×10^{-3} Am^{-2} to $8.89\times10^{-3}Am^{-2}$.

- The current conduction mechanism of lateral PTAA Schottky diodes with an inter electrode spacing of less than 1 μm is dominated by space charge effects whereas those with gap sizes greater than 1 μm have a current transport mechanism dominated more by the bulk resistivity of the film rather than the contact resistances.

- Kinks/roll over effects in the reverse characteristics of lateral PTAA Schottky diodes with gap sizes less than 1 μm are observed and attributed to overlapping of the zero-biased depletion layer of the Ohmic contact with the expanding depletion layer width of the reverse-biased Schottky contact.

- The modulation of the depletion width in lateral PTAA Schottky diodes is dictated by the field across the gap and the area of the active layer.

- Isolation of the active area of lateral PTAA Schottky diodes through photolithography patterning results in an increase in forward and reverse characteristics, due to the unintentional doping of the active layer by the chemical solvents.

- The saturation field-effect mobility, μ_{fe}, threshold voltage, V_T and on/off ratio of PBTTT-C16 transistors are approximately 0.74 $cm^2V^{-1}s^{-1}$, −1.5 V and 4.26×10^2 respectively. Using the disordered TFT model, the material parameters: *m*, *K* and MNE *are* 0.57, 2.15×10^{-16} AV^{-m} and 41 meV respectively.

- Good fits of the output and transfer characteristics of the PBTTT-C16 transistor to the disordered TFT model are obtained particularly for gate-source voltage values lower than −8 V.

- Device instability of PBTTT-C16 transistors is due to the occurrence of residual mobile dopant ions in the film.

- An OTFT model is realised in Cadence design software by modifying pre-existing silicon transistor parameters within the software. The model displays adequate fits to experimental data at higher drain bias with marginally poor fits at lower drain bias associated with contact resistance effects.

- An organic comparator circuit comprising of a preamplifier, latch and self-biased output stage is simulated using the new OTFT model. It has a gain of 45.62 dB and operating frequency of 300 Hz.

- Unpatterned PBTTT-C16 saturated-load inverters are realised using the SAG process. The gain of the various inverters ranges from 1.8 dB to 15.3 dB depending on the aspect ratio of the devices. The operating frequencies of these inverters also ranges from 242.7 Hz to 538.8 Hz.

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CHAPTER 2

Charge Transport Properties of Organic Semiconductors and its application in Organic devices

A brief overview of the equivalent band structure formed within organic semiconductors is presented. This is followed by a review of the theories used to describe the charge transport mechanism within disordered organic materials. The impact of the Meyer Neldel Rule in understanding the charge transport is also explored. An analytical model used to describe the dependency of the effective mobility on carrier concentration is subsequently presented. Finally, based on the effective mobility model, new equations for organic Schottky diodes and thin-film transistors are presented.

2.1 INTRODUCTION

Organic devices and circuits are gradually making their way into the consumer market; thereby effective use of these materials in integrated circuit applications necessitates the need to understand the mechanism governing charge transport within them, for effective modelling and designing of circuits.

This chapter begins by briefly discussing the formation of band structures similar to the conduction and valence bands in inorganic semiconductors, using the Hückel Molecular Orbital theory [1]. Subsequently, the Density of States (DOS) function is described by means of a Gaussian or Exponential distribution. Discussions are also presented on the significance of the Meyer Neldel Energy (MNE) [2] in organic materials. It is commonly associated with the width of the DOS, σ, [3], which could be of practical importance as it provides a means of assessing the degree of energetic disorder within organic materials [4,5] as evidenced by experimental works carried out using Buckminsterfullerene(C_{60})-based Organic Thin Film Transistor (OTFT) devices [5,6] and pentacene-based OTFTs [3]. However, the microscopic origin of the rule is not yet fully understood as will be discussed in later sections. Charge transport models based either on the polaron model [7] or the disorder formalism [8] are presented. The charge transport mechanism in this work is described using the latter model specifically utilising the Variable Range Hopping (VRH) mechanism [9]. By incorporating the VRH mechanism, an analytical model for the effective mobility is expressed in order to explain the charge mobility dependency on carrier concentration as typically observed in disordered materials. This empirical relationship between the carrier mobility and the acceptor (donor) concentration is commonly referred to as the Universal Mobility Law (UML) [10].

More information on the material properties of conjugated polymers can be obtained using simple two-terminal devices such as Schottky diodes, and therefore the relevant theory will be briefly discussed in this chapter. This includes the current transport mechanisms such as the thermionic and diffusion mechanism, Schottky effect and space charge limited current (SCLC) properties. Typically, the equations used in the aforementioned mechanisms are described using a fixed mobility term, and thus are not entirely applicable in describing accurately the current transport mechanisms of the organic materials used in this work. Consequently, different current expressions that incorporate the mobility dependency on carrier concentration (UML) are expounded on. From these revised equations, key parameters

such as the characteristic temperature associated with the distribution of carriers (T_0), the characteristic temperature associated with the DOS (T_C), the MNE and mobility prefactor, K can be obtained.

Lastly, the fundamental theory of the inorganic thin-film transistor is presented, and applied in understanding the operation of the OTFT. Using a similar approach as above i.e. dependency of the mobility on carrier concentration, which describes the VRH model, appropriate drain current expressions of the disordered OTFTs are presented, in terms of the same key parameters as the Schottky diode. Subsequently, the parameter values for different devices with the same active semiconductor can be compared. Similarly, the parameter values of other disordered semiconductors can also be examined and compared where appropriate. This will allow building of libraries of appropriate device models and parameters, which is important for designing organic circuits.

2.2 MATERIAL PROPERTIES AND CHARGE TRANSPORT IN ORGANIC SEMICONDUCTORS

2.2.1 ELECTRONIC STRUCTURE IN ORGANIC SEMICONDCUTORS

The key building blocks of organic semiconductors i.e. molecular crystals and polymeric films, are monomers (molecular sub units), which primarily consist of covalently bonded carbon (C) and hydrogen (H) atoms. Strong σ and σ* bonds are formed from either constructive or destructive overlapping of hybridised atomic orbitals between carbon and its neighbouring carbon/hydrogen atom. The molecular backbone and subsequently the structural properties are based on these bonds. Likewise, the unhybridised p_z orbitals of adjacent carbon atoms overlap constructively or destructively to form π and π* bonds respectively. Electronic properties are associated with these bonds due to their weaker bonding energy with respect to the σ and σ* bonds. The bonding orbitals (π) result in discrete energy levels consisting of the Highest Occupied Molecular Orbital (HOMO), whereas the antibonding orbitals (π*) yield the Lowest Unoccupied Molecular Orbital (LUMO). The hybridised orbitals lie within 120^o from each other and form stronger bonds with other atoms whilst the unhybridised orbitals lie on the perpendicular plane. *Figure 2. 1 (a)* depicts the above-mentioned bonding between adjacent carbon atoms labelled here as C_1 and C_2 respectively with the resultant energy structure shown in *(b)*.

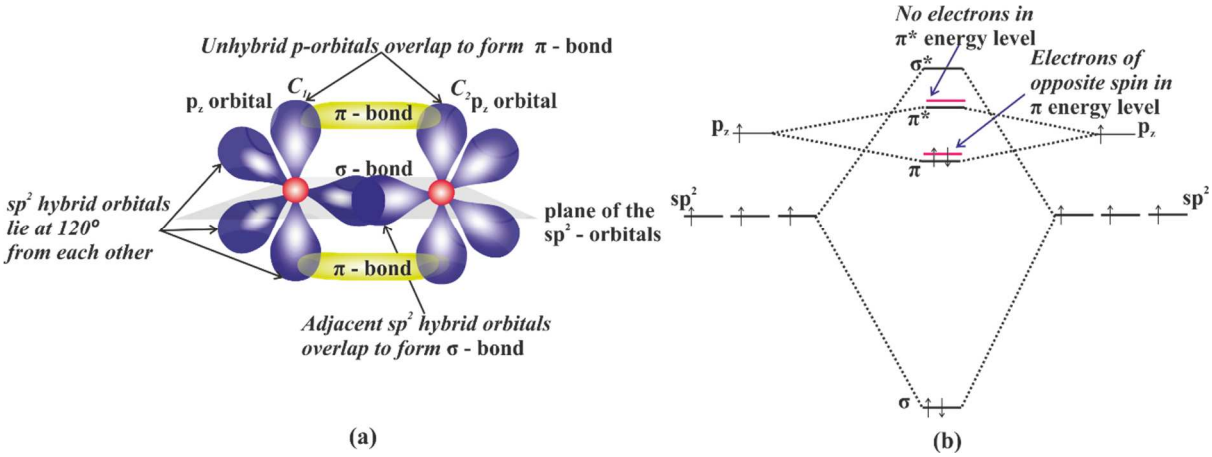

Figure 2. 1: Illustration of the bonding between two adjacent carbon atoms, C_1 and C_2 (a) and the equivalent energy structure (b). The hybridised orbitals lie within 120^o from each other whilst the unhybridised orbitals lie on the perpendicular plane.

Within a chain, as in polymeric films, or within small molecules, the molecular orbitals of repeating adjacent monomer units are coupled with a weak π-electron overlap. This linking results in the interaction and delocalisation of neighbouring HOMO and LUMO levels across the system. Consequently, the equivalent valence and conduction bands are formed as described in the Hückel Molecular Orbital Theory [1]. The band gap (E_g) of the semiconductor is thus taken to be the difference between the resultant HOMO and LUMO energy levels.

In the ground state, the HOMO level is filled with electrons whereas the LUMO energy level is devoid of electrons. Promotion of an electron from the HOMO level to the LUMO level, for instance through light absorption, can result in the formation of a neutral excited state. Similarly, other charged excited states can be formed through the addition or removal of one or more electrons to the molecule either electrochemically or chemically. This results in shifting of the orbitals relative to the vacuum level. The structural geometry of the molecule is changed as well due to alteration of the electrons within the σ-bonds. The coupling of the charge with the energy of the altered structural geometry results in the formation of a polaron. Furthermore, the addition of one or two electrons to the LUMO results in a negative polaron and bipolaron respectively, whereas the removal of one or two electrons from the HOMO results in a positive polaron and bipolaron respectively.

2.2.2 DENSITY OF STATES FUNCTIONS

The shape of the DOS function in disordered organic semiconductors is commonly believed to be Gaussian as made popular in the Gaussian Disorder Model (GDM) [8]. In his work, Bässler stipulates that this is the case as evidenced by the shape of the energy spectrum of an organic material that, in effect, determines opto-electronic properties up to and including the charge transport properties of organic semiconductors. The Gaussian distribution expression takes the form below:

$$g(E) = \frac{N_t}{\sigma\sqrt{2\pi}} \exp\left(-\frac{E^2}{2\sigma^2}\right) \qquad 2.1$$

where N_t is the total concentration of the localised states, σ is the variance of the width of the DOS and E is the energy of the localised states.

Conversely, Vissenberg and Matters [11] derived an expression for the field effect mobility of transistors, assuming an exponential DOS of the form given by *equation 2.2* below:

$$g(E) = \frac{N_t}{kT_C} \exp\left(\frac{E}{kT_C}\right) \quad (-\infty < E \leq 0,\ T < T_C) \qquad 2.2$$

where k is Boltzmann's constant, T is absolute temperature and T_C is the characteristic temperature associated with the exponential DOS distribution.

The use of the exponential DOS is justified by Tanase *et al.*, [12,13] who assert that the conduction properties, at low carrier densities and temperature, are determined by the tail of the Gaussian distribution which, for a given energy range, accurately takes an exponential form as demonstrated in *Figure 2. 2*.

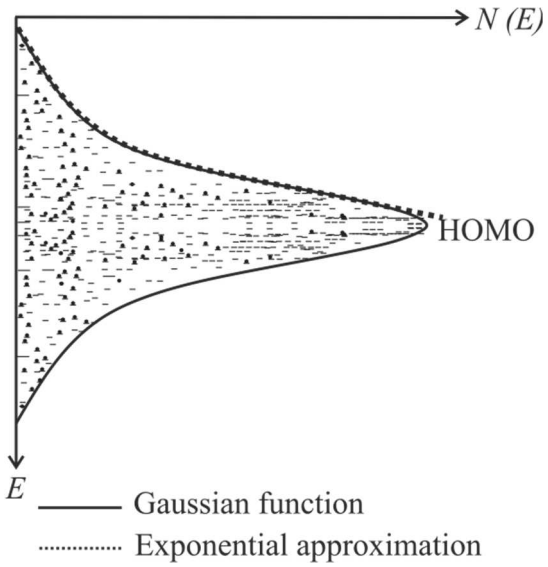

Figure 2. 2: Illustration of the Gaussian DOS distribution and the exponential approximation at the tail of the Gaussian for a given energy range.

On the other hand, recent studies by Oelerich *et al.*, [14] state that the equation for the exponential DOS should ideally take the form of:

$$g(E) = \frac{N_t}{Q} \exp\left[\left(-\frac{|E|}{\sigma}\right)^p\right] \quad (p \geq 1) \qquad 2.3$$

Here,

$$Q = \sigma \cdot \Gamma\left(p^{-1} + 1\right)$$

where p is an arbitrary power factor associated with the exponential DOS.

Values of $p > 1.8$ are used in the fitting of the experimental data of poly (2-methoxy-5-(3', 7'-dimethyloctyloxy)-p-phenylene vinylene) (OC_1C_{10}-PPV) and poly-3-hexylthiophene (P3HT). Evidently, for $p = 1$, *equation 2. 3* resembles that of *equation 2.2*, which can be termed as the "pure" exponential DOS whereas for $p = 2$, *equation 2. 3* resembles the bottom half of the Gaussian DOS spectrum.

Direct measurement of the DOS is carried out using electrochemically doped OC_1C_{10}-PPV [15] and is found to follow an exponential form, however, dopants have a tendency of changing the shape of the DOS [16,17] therefore casting doubts on the validity of the results/measurement technique. Accordingly, measurements of the DOS using a technique

based on Kelvin-Probe Force Microscopy (KPFM) on both doped and undoped *N*,*N*^{I}-diphenyl-*N*, *N*^{I}-bis (1-naphthyl)-1, 10-biphenyl-4,4^{II}-diamine (α-NPD) based TFTs [18] are carried out. Results from the undoped α-NPD sample show a Gaussian distribution with an exponential-like tail dependency. On the doped sample, the DOS broadens and has additional discrete peaks induced. The broadening of the DOS is associated with trapped charges at the interface of the dielectric and in other cases due to potential fluctuations as a result of internal dipoles [19].

To summarise, the shape of the DOS in disordered organic semiconductors may be either a Gaussian or an exponential form and is dictated by the amount of residual dopants present in the film as well as the device used to characterise the measurement.

2.2.3 CHARGE TRANSPORT IN ORGANIC SEMICONDUCTORS

There is a general agreement that the charge transport in organic semiconductors occurs as a result of thermally assisted hopping between localized states, whereby the probability of hopping from an occupied site *i* to an unoccupied one *j* is described using the general equation below [16]:

$$\frac{\partial}{\partial t} f_i(t) = -\sum_{j \neq i} W_{ji} f(t)[1 - f_i(t)] + \sum_{j \neq 1} W_{ij} f_j(t)[1 - f_i(t)] - \lambda_i f_i(t) \qquad 2.4$$

where $f_i(T)$ is the probability that site *i* (located at R_i and with an energy *i*) has a charge at a given time *t*, W_{ij} is the transition rate from the occupied site *(i)* to the unoccupied site *(j)* and λ_i is the decay rate of the excited charge at site *i.*

The transition rate in this equation usually takes two forms whereby hopping is either a single phonon or a multiphonon process. The first form, commonly referred to as Miller-Abrahams jump rate model [20], assumes the former, and results in a transition rate equation given by:

$$W_{ij} = \nu_0 \exp\left(-2\frac{R_{ij}}{\alpha}\right)\exp\left(-\frac{\left|E_j - E_i\right| + \left|E_j - E_i\right|}{2kT}\right) \qquad 2.5$$

where ν_0 is the attempt-to-hop frequency, R_{ij} is the intersite distance, α is the inverse of the localisation length, E_j is the energy at the unoccupied site and E_i is the energy at the occupied site.

In the VRH model, Mott and Davis [9] extend the above model by further analysing the distances over which the carriers can hop, suggesting that carriers may hop with a low activation energy over longer distances as well as hop with a high activation energy over small distances.

Alternatively, the Marcus jump rate model [19] as shown in *equation 2. 6*, takes account of polaron formation, and its resultant effects on charge transport. It is based on studies of electron transfer reactions by Marcus [21, 22].

$$W_{ij} = W_0 \exp\left(-\frac{E_a^{pol}}{kT}\right)\exp\left(-\frac{\left(E_j - E_i\right)}{2kT} - \frac{\left(E_j - E_i\right)^2}{16kTE_a^{pol}}\right) \qquad 2.6$$

Here,

$$E_a^{pol} = \frac{E_b}{2}$$

$$W_0 = \frac{J_0^2}{\hbar}\sqrt{\frac{\pi}{4E_a^{pol}kT}}\exp\left(-2\frac{R_{ij}}{\alpha}\right)$$

where E_b is the polaron binding energy, E_a^{pol} is the polaron activation energy, J_0 is the prefactor in the transfer integral and $\hbar$ is the Dirac constant/reduced Planck constant.

Subsequently, numerous debates on the charge transport mechanism based on either a dominant polaronic transport or a dominant non-polaronic transport (disordered transport) have arisen and are further discussed below.

♦ **Polaron-based transport**

Electron-phonon interactions usually result in the deformation of the matrix of an organic semiconductor as shown in *Figure 2. 3*, assuming a polythiophene chain. A polaron is usually formed as a result of the charge coupling with its matrix distortion energy as explained in *section 2.2.1* of this chapter. Polaronic motion is characterised by polarons hopping between neighbouring sites. In the "small polaron" transport model developed by Holstein [7], a polaron is described as small when its size is comparable to the spacing within the matrix. Emin [23] characterised the hopping nature of the small polarons as being adiabatic, which is the case when the lifetime of a predecessor and successor site is equal in energy and larger than the carrier transit time.

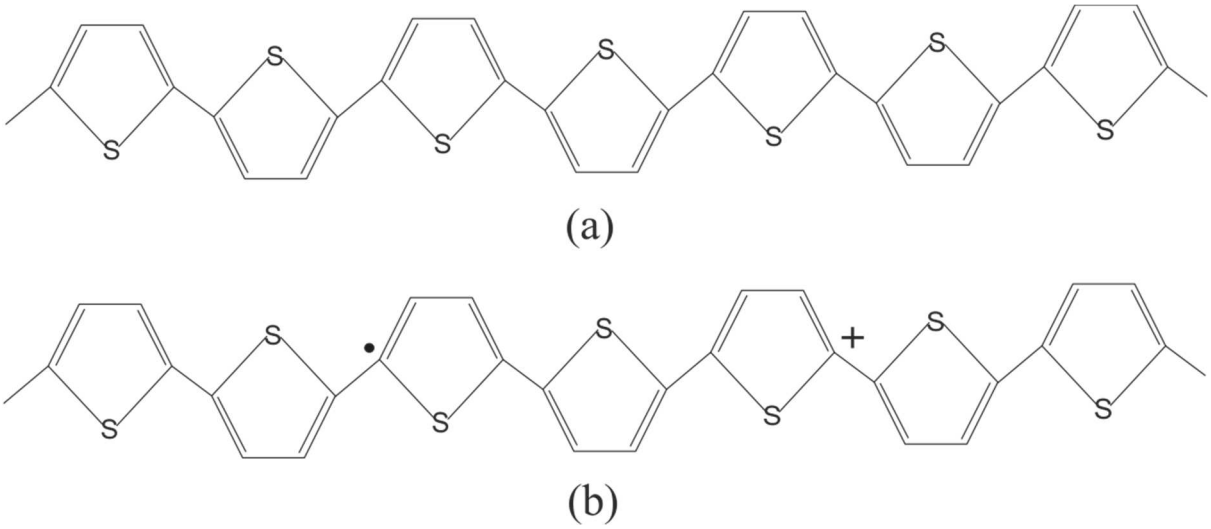

Figure 2. 3: (a) Chemical structure of a polythiophene. (b) Change in the chemical structure of polythiophene after a polaron is formed.

Waragai et al have carried out experimental studies on the temperature and field effects of pure polaron motion on carrier transport in organic semiconductors [24, 25]. However, for charge carrier mobility values to fit the small polaron model, impractical parameters would be needed for the polaron binding energy and the transfer integral described in the Marcus jump rate model. Furthermore, the model developed by Waragai et al fails to account for the change

in transport regimes of FETs from a nondispersive one to a dispersive one upon reduction of temperature [26].

On the other hand, studies have shown that temperature dependent carrier mobility expressions can be explained by a combination of both polaronic and disordered effects [27, 28]. The Correlated Disorder Model (CDM) resolves the above-mentioned limitations cited for the pure polaron model where it states that small-polaron transport takes place in occurrence with correlated energetic disorder for polaron carriers that have a polaron binding energy ranging from 50-500 meV and a transfer integral of 1-20 meV. In such a case, the zero-field effect mobility is given by [27]:

$$\mu(T) \propto \exp\left(-\frac{E_b}{2kT}\right)\exp\left[\left(-A\left(\frac{\sigma}{kT}\right)^2\right)\right] \qquad 2.7$$

where the arbitrary coefficient, *A*, usually extrapolated from experimental data, has been shown to be dependent on the ratio of the polaron binding energy to the width of the DOS i.e. E_b/σ.

Fishchuk *et al.*, [29, 30] carried out further work on the carrier concentration dependency on mobility using the disordered model and CDM. For values where E_b is large such that $E_b/\sigma \geq 3$, i.e. when the polaron effects are more pronounced, the mobility showed a weaker dependency on the concentration of carriers, which is explained to be due to the fact that polaron activation energy is not dependent on the concentration of the polarons unlike in disorder-based models where the mobility is greatly dependent on carrier concentration as will be discussed in the next section.

♦ Disorder-based transport

Most of the disorder hopping models in organic semiconductors are based on the work carried out by Bassler [8]. In his work, the model, termed the Gaussian Disorder Model (GDM), describes the hopping transport using Monte Carlo simulations. In the model, a non-Arrhenius-like temperature, *T*, dependency on hopping mobility and a Poole-Frenkel-type [31] behaviour for constant field, ξ is obtained as given in *equations 2. 8* and *2. 9* below:

$$\log(\mu) \propto 1/T^2 \qquad 2.8$$

$$\log(\mu) \propto \xi^{1/2} \qquad 2.9$$

The model however fails to account for the vast differences in values obtained for the field-effect hole mobilites in field-effect transistors (FETs) and hole mobilities of diodes made using the same material as the active layer. The differences in the two values is because of failing to account for the dependency of the charger carrier mobility on carrier concentration. The aforementioned problem is thereby resolved by taking into account the mobility dependency on carrier concentration [12,13,32] as is commonly done presently resulting in similar mobility values being obtained from different device topologies made with the same material. The modified models result in Arrhenius-like temperature dependent mobility expressions with varying mobility prefactor values depending on the averaging procedure used for the hopping sites. In the Extended Gaussian Disorder Model (EGDM) [32], the procedural method used averages all the sites using the Miller-Abraham expression given by *equation 2. 5*, whereas in [12, 13] a percolation approach is used. The resultant field-effect mobility for EGDM is as given in *equation 2. 10*. In both cases, as will be discussed briefly, the dependency of carrier concentration, *p,* on mobility has remarkable similarities in spite using different methods for averaging the hopping sites.

$$\mu(T,p) = \frac{a^2 \nu_0 q}{\sigma} c_1 \exp\left[-c_2 \hat{\sigma}^2\right] \exp\left[\frac{1}{2}\left(\hat{\sigma}^2 - \hat{\sigma}\right)\left(2pa^3\right)^{\delta}\right] \qquad 2.10$$

Here,

$$\delta \equiv 2\frac{\ln\left(\hat{\sigma}^2 - \hat{\sigma}\right) - \ln(\ln 4)}{\hat{\sigma}^2}, \quad \hat{\sigma}^2 \equiv \frac{\sigma}{kT}$$

where a is the localisation length and c_1 and c_2 are arbitrary constants with values as follows: $c_1 = 1.8\times10^{-9}$ and $c_2 = 0.42$.

Alternatively, the percolation approach is introduced by Ambegoakar *et al.,* [33] and utilised by Vissenberg and Matters [11] to derive a carrier concentration dependent mobility model, assuming an exponential DOS. In the percolation model, the system is regarded as a network of interconnected resistors with an intersite conductance, G_{ij}, given by:

$$G_{ij} = G_0 \exp\left(-s_{ij}\right) \qquad 2.\ 11$$

Here,

$$s_{ij} = 2\alpha R_{ij} + \frac{\left|E_i - E_j\right| + \left|E_j - E_F\right| + \left|E_i - E_j\right|}{2kT}$$

where E_F is the Fermi-level and G_0 is a prefactor.

The total conductivity of the system is then obtained using the percolation theory. Theoretically, it is assumed that hopping between sites with decreasing s_{ij} is unimportant. Following this, the conductance value initially remains almost constant, until a critical value s_c, where it then drops strongly. This parameter, s_c determines the inception of percolation i.e. the formation of the first infinite clusters and the subsequent clusters to follow whereby a larger cluster is formed for smaller values of s_{ij}. At s_c, the clusters are interconnected via a number of bonds referred to as B_c. Subsequently, the conductivity of this system is proportional to the critical conductance as given below:

$$\sigma(\delta, T) = \sigma_0 \left(\frac{\pi N_T \delta (T_C/T)^3}{(2\alpha)^3 B_c \Gamma\left(1 - T/T_C\right)\Gamma\left(1 + T/T_C\right)} \right)^{\frac{T_C}{T}} \qquad 2.\ 12$$

Here,

$$B_c \approx \pi \left(\frac{T_C}{2\alpha T}\right)^3 N_t \exp\left(\frac{E_F + s_c kT}{kT_C}\right)$$

$$\Gamma(z) = \int_0^\infty dy \exp(-y) y^{z-1}$$

where δ is the fraction of states occupied.

Equation 2. 12 shows that the conductivity value (related to the field-effect mobility as in *equation 2. 13*) exhibits a strong dependency on carrier concentration as well as an Arrhenius-like temperature dependence.

$$\mu_{FE}(p) = \frac{\sigma_0}{q}\left(\frac{(T_C/T)^4 \sin(\pi T/T_C)}{(2\alpha)^3 B_c}\right)^{T_C/T} p^{T_C/T-1} \qquad 2.\ 13$$

where σ_0 is the conductivity prefactor, B_C is the critical number for the onset of percolation and p is the hole concentration.

Similarly, other authors have derived the field-effect mobility utilising the percolation theory, however, it is assumed that in this case the hopping is dependent on the average of the infinite cluster sites that provide percolation [34,35], unlike in the aforementioned model and in [16,36] where all the hopping sites are averaged. It is shown by Nenashev *et al.*, [37] that regardless of the analytical approach used, the resultant mobility expression typically takes the form below:

$$\mu = A\frac{\nu_0 e}{n\sigma a}\left[B\frac{p}{8}\left(\frac{a\sigma}{kT}\right)^3\right]^{\sigma/kT} \qquad 2.\ 14$$

where a is the localisation length and A and B are the analytical prefactors attributed to the different analytical approaches used in which case they are dependent on either σ/kT or are arbitrary numerical constants.

The multi-trapping and release model (MTR) [38], commonly used to describe charge transport in inorganic amorphous materials, has also been adopted extensively in organic semiconductors [34, 39-42]. The mobility edge in the former is substituted in the latter with a slightly temperature-dependent energy level referred to as the "transport energy "(TE) level, E_T. In the model, the mobility is strongly dependent on the successive hopping of free carriers between states situated near E_T. Carriers located below E_T are essentially trapped in deep lying states. Upon thermal excitation, charges are released from the traps to the transport level as shown in *Figure 2. 4* below. The mobility μ term in this system shows an Arrhenius-like temperature dependency given by [39]:

$$u = \frac{q\bar{v}l}{8kT}\exp\left(-\frac{E_b}{kT}\right) \qquad 2.\ 15$$

where q is electronic charge, $\bar{v}$ is the electron mean velocity, l is the grain size and E_b is the mean energy.

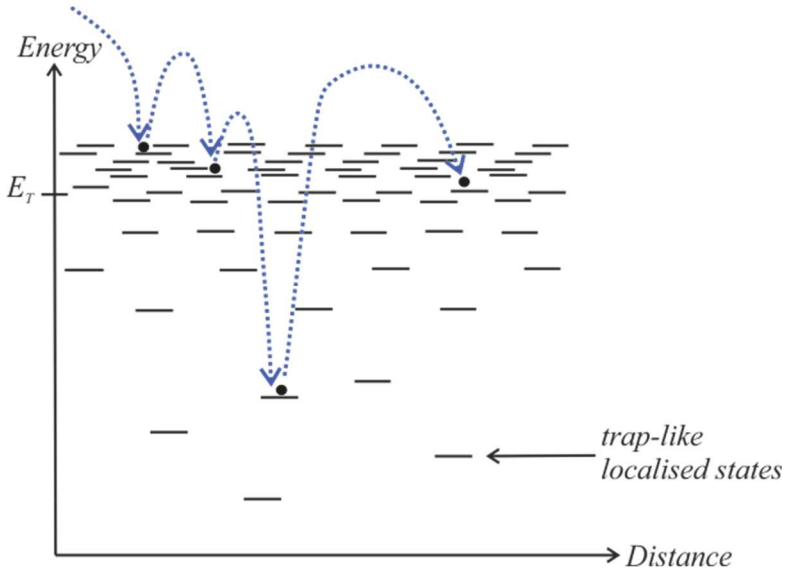

Figure 2. 4: Illustration of the Multi-trap and release model. Filled circles represent charge carriers introduced through thermal excitation or injection.

♦ Impact of Meyer Neldel Rule in Charge transport

The Meyer Neldel Rule (MNR) has commonly been used to describe the relationship between enthalpy and entropy of a chemical reaction [2]. It states that in a process, Y, that has been thermally activated, an exponentially increasing activation energy, E_a, is partly compensated by an increasing prefactor, Y_0 as in the relationship:

$$Y = Y_0 \exp-\left(\frac{E_a}{kT}\right) \qquad 2.\ 16$$

Here,

$$Y_0 = Y_{00} \exp\left(\frac{E_a}{kT_C}\right)$$

where Y_{00} is a constant prefactor and kT_C is the MNE.

In semiconductor physics, the MNR has been observed in FETs, which essentially have conductivity and mobility expressions with an associated temperature dependency. Nonetheless, there are numerous debates on the origin of this effect and its physical interpretation in the context of organic semiconductors as will be discussed shortly. Studies of the MNR and its effect on charge transport in inorganic transistors made using amorphous silicon have been carried out in [43-45]. Charge transport in this material is explained by means of the MTR model, assuming an exponential DOS, whereby thermally activated carriers hop from the Fermi level to the mobility edge. In this case, the authors claim that the statistical shifting of the Fermi level with temperature accounts for the mobility expressions obeying the MNR whereby the MNE given in *equation 2. 16*, is then believed to be equivalent to the width of the DOS [45].

On the other hand, studies of the MNR in organic semiconductors have slight modifications to their explanations, specifically, in the context of the hopping carriers that contribute to conduction. Briefly, hopping is associated with the distribution of occupied sites in the whole DOS not simply at the Fermi level, and in other cases, the equivalent transport energy level, much like the inorganic counterparts, is assumed. There have been numerous debates on the origin of MNR and its physical interpretation in the context of organic semiconductors. Some arguments suggest that, in organic semiconductors, the MNR is in fact not observed but it is instead an "*apparent*" compensation effect [4] as experimentally illustrated by the works of Fischuk *et al.*, [4] and Meijer *et al.*, [46]. In the former work, the temperature dependency of mobility with varying carrier concentrations displays the MNR effect however; the effect is not observed when the width of the DOS is varied directly, which essentially contradicts the MNR. It is expected that upon varying the activation energy (which is achieved either by varying the width of the DOS or by increasing the carrier concentration upon application of an external field), there will be an accompanying partial prefactor as well. This suggests that there is not, as yet, any correlation between the prefactor of the mobility term and the attempt-to-hop frequency, which determines the transition rate of carriers.

On the contrary, Yelon *et al.*, [47] argue instead that the observation of the MNR is due to polaronic transport described by multiphonon processes [48]. In their model, termed multiexcitation entropy, *MEE*, a number of activation paths increases exponentially because of multiphonon excitation, which results in an exponentially increasing prefactor with increasing activation energy.

The previous section already highlighted the limitations of a purely polaronic transport model, therefore favouring the superposition of disordered and polaronic transport. Most organic FETs exhibit a dominant disordered transport mechanism whereas others exhibit a largely disordered transport mechanism coupled with minor polaronic effects such that $E_b/\sigma \leq 3$. A recent study by Fishchuk *et al.*, [3] shows that in a system which combines disordered and small/moderate polaron effects, the MNR compensation effect is not significantly altered. Furthermore, it concludes that in a dominant disordered system, which has a temperature-dependent mobility, the MNE is determined by the shape of the DOS, the polaron binding energy as well as the partial filling of the DOS due to field-effect.

♦ The Universal Mobility Law and its application to charge transport in organic semiconductors

The charge-carrier mobility model used in this thesis assumes a Gaussian DOS with an exponential approximation at the band tail, as given by *equation 2.2*. Mott's VRH mechanism is used to explain the carrier transport mechanism; however, the model in this work does not use its transition rate expression to derive an expression for the effective mobility. As described earlier, the carrier concentration dependent mobility has a comparable dependency irrespective of the hopping mechanism used, assuming a disordered transport system. A Fermi-Dirac (F-D) distribution function [49] as given in *equation 2. 17* , is used in determining the probability of carrier occupation within the DOS.

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)} \qquad 2.\ 17$$

The conduction processes are assumed to take place within the vicinity of the Fermi level, E_F, which is commonly believed to lie within the tail of the Gaussian DOS. Assuming a *p*-type semiconductor, hopping takes place close to E_F due to the combined effect of an exponentially falling carrier occupancy defined by the distribution function (below E_F) and the high number of energy states located a few kT below E_F i.e. at the transport energy level, E_T [41,42].

To obtain an expression for the free carrier concentration, it is assumed that carriers above the E_F do not contribute to conduction as depicted in *Figure 2. 5*. This assumption is made because there is a small number of unoccupied sites for carriers to hop to and in any case, the sites are much further apart and at higher energy levels making them virtually immobile. In this case, the probability of occupation above E_F is assumed equal to one, and the carrier concentration probability below E_F can be replaced with the Maxwell Boltzmann Distribution $f(E)$ function given by:

$$f(E) = \begin{cases} \exp\left(-\dfrac{E_F - E}{kT}\right) & \text{if } E < E_F \\ 1 & \text{if } E \geq E_F \end{cases} \qquad 2.\ 18$$

An increase in carrier concentration upon application of field therefore results in occupation of the lower energy levels, below E_F and near E_T, where hopping is enhanced due to smaller hopping distances, thereby increasing the carrier mobility. The carriers in this area hop with an activation energy, E_A from E_F to E_T. Despite the fact that there are more states at lower energy levels, i.e. below E_T, the carrier concentration is lower therefore resulting in no conduction past this point.

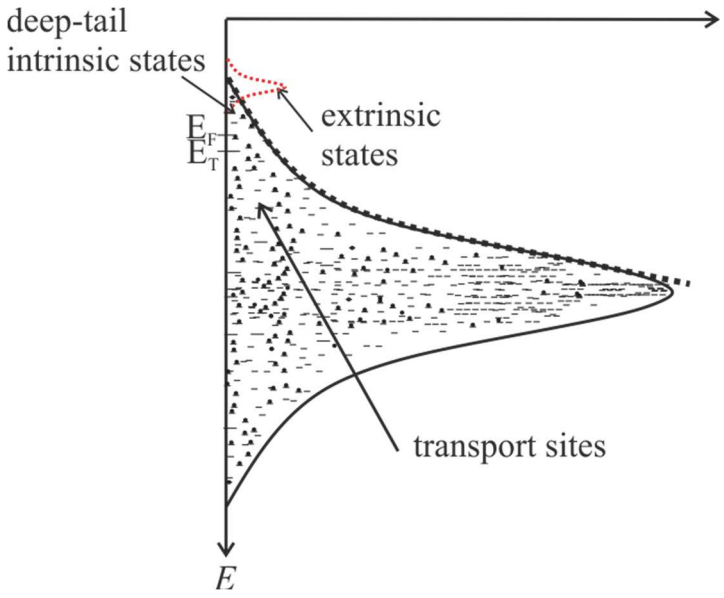

Figure 2. 5: Illustration of an exponential approximation to the tail of the Gaussian DOS distribution for the lower energy range, where charge transport in organic devices typically takes place. Charge carriers above E_F are trapped and do not contribute to conduction. At lower energies, close to E_F, an increase in carrier concentration results in an increase in mobility due to the enhanced hopping rates.

Assuming a *p*-type semiconductor, the free carrier concentration *p*, can therefore be obtained from integrating *equation 2. 19* as shown below (Full derivation is provided in Appendix A).

$$p = \int_{-\infty}^{E_F} N'(E) f(E) dE \qquad 2.\ 19$$

$$p = N'(0) kT_0 \exp\left[-\frac{E_F}{kT_C} \right] \qquad 2.\ 20$$

Here [50],

$$\frac{1}{T_0} = \frac{1}{T} - \frac{1}{T_C} \qquad 2.\ 21$$

where *N' (E)* is the effective density of states, *N' (0)* is the rate of change of density of traps with energy and T_0 is the characteristic temperature associated with the distribution of carriers

A single mobility term is typically used to describe the carrier mobility in inorganic crystalline semiconductors. However, as has been previously discussed, the DOS distribution in disordered materials follows either an exponential or Gaussian shape with change in energy such that carriers at different energy levels are likely to experience different hopping rates thereby resulting in a mobility value that is not fixed hence the term effective mobility, $\mu_{eff.}$ Although the device physics in the two materials vary greatly, it is still plausible to describe the movement of carriers in disordered materials by the use of an effective mobility term, which is akin to the conventional mobility term but has a stronger dependency on the carrier concentration. The significance of μ_{eff} in disordered materials can be better appreciated by comparing the current density of a disordered system, $J_{Disordered}$, with the current density of an ordered, crystalline system, $J_{Ordered}$, as given by *equations 2. 22* and *2. 23* respectively:

$$J_{Ordered} = N_V \exp\left(-\frac{E_F - E_V}{kT}\right) q u_m F \qquad 2.\ 22$$

$$J_{Disordered} = N'(0) kT_0 \exp\left(\frac{E_F}{kT_C}\right) q u_{eff} F \qquad 2.\ 23$$

where N_V is the effective DOS at the edge of the valence band, E_V and μ_m is the measured mobility.

Upon comparison, it is assumed that a disordered system is in contact with an ordered system in the manner shown in *Figure 2. 6*, whereby current flow, band-bending and trapped charges at the interface are assumed absent. Furthermore, it is assumed that the disordered system has an energy level, referred to as the effective transport energy level (E_T) which is equal in energy to E_V in the ordered system.

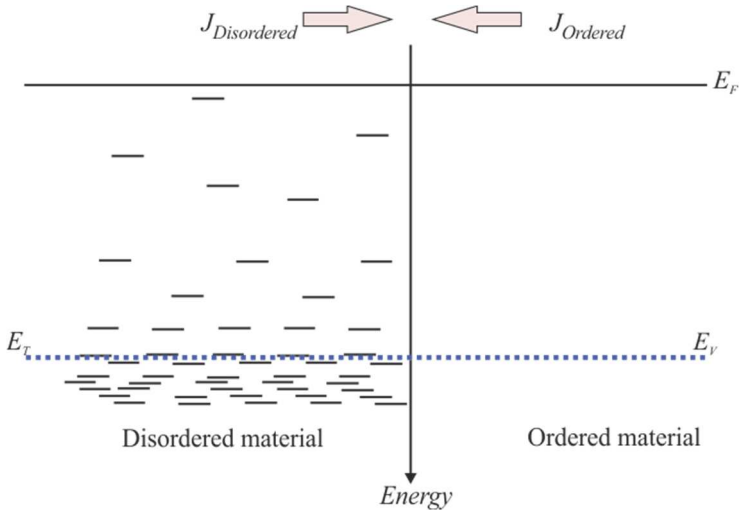

Figure 2. 6: Illustration of a disordered system in contact with an ordered system under thermal equilibrium, for a p-type semiconductor. Band bending and trapped charges are assumed absent.

When in thermal equilibrium, the carrier flux is equal on both sides and the effective mobility of a conjugated polymer can be expressed in terms of the measured mobility [51] as shown below (full details are provided in Appendix B):

$$\mu_{eff} = Kp^m \qquad 2.\ 24$$

Here,

$$m = \frac{T_C}{T} - 1 \qquad 2.\ 25$$

$$K = \mu_m \frac{N_V}{\left[N'(0)kT_0\right]^{T_C/T}} \exp\left(-\frac{E_V}{kT}\right) \qquad 2.\ 26$$

Equation 2. 24 shows a power dependency, *m* of the mobility on carrier concentration, *p* as observed in the UML [10], with an additional mobility pre-factor, *K*. The same observation of the effective mobility dependency on carrier concentration has been made on doped disordered organic semiconductors [51]. It follows from *equations 2. 24* and *2. 25* that the effective mobility in organic semiconductors is affected by the degree of disorder and temperature such that the electrical conductivity reduces with the increase in disorder.

Conversely, an increase temperature i.e. increase in the thermal energy of carriers results in an increase the effective mobility.

The bulk of this thesis utilises organic Schottky diodes and OTFTs in the characterisation of the materials, thus, understanding the underlying theory of such devices and subsequently developing and utilising appropriate models incorporating the newly developed effective mobility term is essential and is presented in the ensuing sections.

2.3 FUNDAMENTAL THEORY OF SCHOTTKY DIODES AND THIN-FILM TRANSISTORS (TFTs)

2.3.1 METAL/SEMICONDUCTOR CONTACTS – SCHOTTKY DIODES

When a semiconductor with no surface states [52-54] comes into contact with a metal, the Fermi levels align to reach thermal equilibrium. For a *p*-type semiconductor, if the metal has a lower work function, W_M than its own, carriers move from the metal contact into the semiconductor resulting in the formation of a potential barrier V_{bi}, and a depletion layer of width W, consisting of uncompensated acceptor ions. The resultant potential barrier restricts the flow of carriers from the metal into the semiconductor leading to subsequent rectification behaviour at the Schottky contact.

Upon application of a negative voltage on the Schottky contact (i.e. forward bias), the potential barrier at the interface is reduced, resulting in reduction of the depletion region, and thus allowing majority carriers (holes) to easily move from the semiconductor across the interface. In contrast, application of a positive voltage (i.e. reverse bias), enhances the potential barrier and widens the depletion region thereby impeding the movement of holes across the interface. In the latter case, the current is therefore due to the flow of carriers from the adjacent metal contact. *Figure 2. 7* below shows the energy band diagrams of a metal and *p*-type semiconductor, with varying application of external bias.

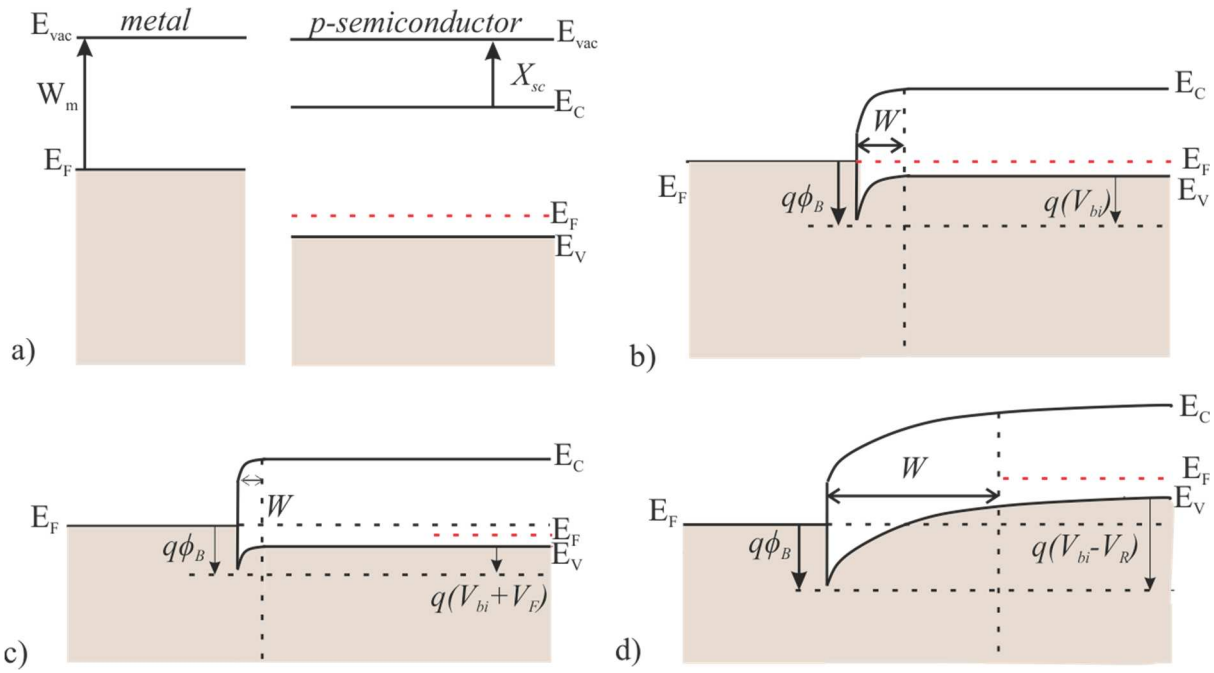

Figure 2. 7: Energy band diagram of metal-semiconductor junctions with a p-type semiconductor (a-d)); where (a) is before the metal and semiconductor make contact (b) when the junction is in thermal equilibrium without any application of bias (c) on application of a forward bias and (d) on application of a reverse bias.

For a semiconductor with a large density of surface states [55], the situation is different, such that a space charge region already exists on the semiconductor side prior to contact formation. Further to this, surface traps are occupied up to the quasi-Fermi level, such that upon metal contact formation, carriers moving from the semiconductor into the metal are trapped in the surface states resulting in minimal movement of the quasi-Fermi level as illustrated in *Figure 2. 8*. Consequently, the surface depletion layer is essentially similar to the unchanged space charge region. Subsequent band bending will occur at the bare semiconductor surface such that the barrier height will be independent of the metal function.

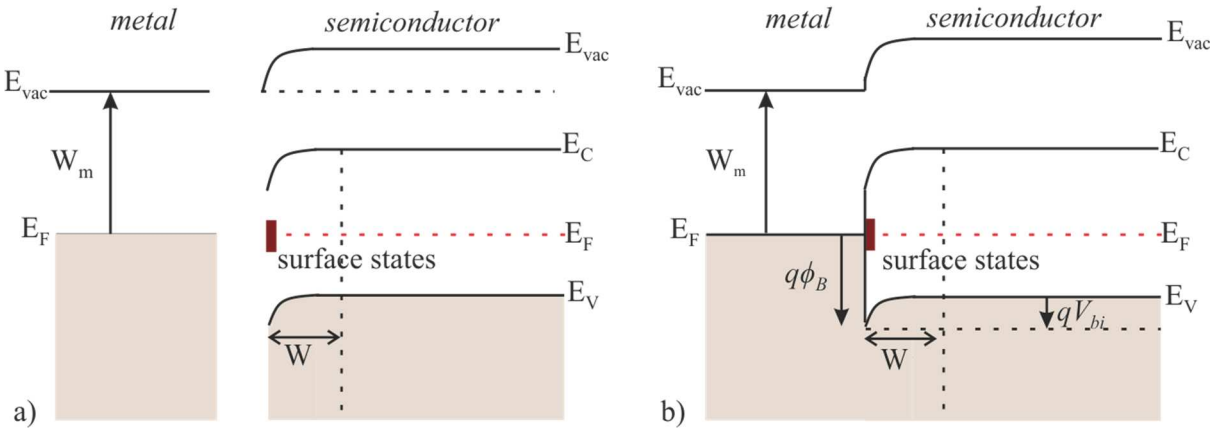

Figure 2. 8: Energy band diagram of a p-type metal-semiconductor junction that is characterised by surface states at the interface of the metal and semiconductor: a) before contact formation and b) after contact formation.

As indicated earlier, assuming the absence of surface states, an application of forward bias results in the reduction of the potential barrier, thereby allowing movement of holes into the metal. For a low forward bias, the associated current density in inorganic semiconductors is given by *equation 2. 27* [56], whereby the exponential dependency of the current density, *J*, is related to the exponential distribution of carriers.

$$J = J_0\left[\exp\left(\frac{qV_{app}}{\eta kT}\right)-1\right] \qquad 2.\ 27$$

where J_0 is the saturation current density, q is the electronic charge, V_{app} is the applied voltage, η is the ideality factor, k is Boltzmann's constant and T is the absolute temperature

The value of J_0 in *equation 2. 27*, depends on the conduction mechanism present in the material. More often than not, the transport process of carriers above the barrier can be explained by either a diffusion process [57, 58] or a thermionic process [59] or a combination of both [60]. In a diffusion process, typically associated with semiconductors with a low mobility, thermal equilibrium is established upon metal contact formation such that E_F of the metal matches with that of the semiconductor. The flow of current is consequently dictated by drift and diffusion processes across the depletion layer. The saturation current density in this case takes the form [56]:

$$J_{D0} = qN_V v_D \exp\left(-\frac{q\phi_B}{kT}\right) \approx qN_V \mu F_{\max} \exp\left(-\frac{q\phi_B}{kT}\right) \quad 2.28$$

where N_V is the effective DOS in the valence band, v_D is the effective diffusion velocity, ϕ_B is the barrier height, μ is the carrier mobility and F_{max} is the maximum electric field, neglecting image force effect.

On the other hand, in a thermionic emission process (applicable to semiconductors with high mobility), current is limited by the amount of carriers with energy high enough to overcome the potential barrier and move into the metal contact. The saturation current density in this case is given by the equation below [56]:

$$J_{TE0} = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \quad 2.29$$

A^* is the Richardson constant and ϕ_B is the barrier height

When both of the aforementioned processes are present in the material, the saturation current density takes the form [56]:

$$J_0 = q\left(\frac{v_R}{1+v_R/v_D}\right) N_V \exp\left(-\frac{q\phi_B}{kT}\right) \quad 2.30$$

Here,

$$v_R = A^* T^2 / qN_V$$

where v_R is the effective surface recombination velocity.

For highly doped semiconductors, carriers may tunnel through the thin potential barrier at higher electric fields. The field-emission current [61] for this situation is given by:

$$J_0 = \frac{q^3 F_{\max}^2}{16\pi^2 \hbar \phi_B} \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar F_{\max}} \right] \qquad 2.\ 31$$

where $\hbar$ is Plank's constant and m^* is the carrier effective mass.

The previously mentioned equations i.e. *2. 27* to *2. 31* are not suitable for explaining the current transport mechanisms in the organic materials used in this work. Consequently, different current expressions that incorporate the carrier mobility dependency (UML) are used for the characterisation of the forward current density in the low-voltage regime. In organic semiconductors, the exponential rise in the current obtained at low voltages is associated with the exponential rise in the carrier occupancy with energy as dictated by the Maxwell Boltzmann approximation at the tail of the Exponential DOS distribution. The forward current density in this case takes the form given in *equation 2. 32* [51]. The full derivation of the equation is provided in Appendix C.

$$J \propto \exp\left(\frac{qV_{app}}{kT_0} \right) \qquad 2.\ 32$$

where T_0 is the characteristic temperature associated with the distribution of carriers.

The ideality factor, η of the organic Schottky diode is related to T_0 using the relation given in *equation 2. 33*.

$$T_0 = \eta T \qquad 2.\ 33$$

At higher forward bias, the current density of an inorganic diode typically deviates from its exponential form such that most of the voltage drops across the neutral region of the film. Deviation from an Ohmic conduction to a space charge limited current (SCLC) conduction occurs when an accumulation layer of a non-uniformly distributed layer of excess charge from the injected carriers exists. In the presence of a potential barrier at the injecting metal/semiconductor interface, the current density may be characterised by the properties of the adjourning contact or a combination of both the space charge effects and contact effects.

The current density in this case is dependent on the applied voltage to a power *a* as in *equation 2. 34*:

$$J \propto \left(V_{app}\right)^{a} \qquad 2.\ 34$$

A double logarithmic plot of the forward current density yields the value of *a*, such that a value of *a*~1 suggests that the current density is dictated by the resistivity of the film and is essentially given by Ohm's law as in *equation 2. 35*:

$$J = pq\mu \frac{V_{app}}{x} \qquad 2.\ 35$$

where *p* is the carrier concentration and *x* is the material thickness.

For $a \geq 2$, the current density is thought to be limited by the space charge effects in the material. For an inorganic material with a single set of shallow traps [62], the SCLC current density [62-64] is commonly expressed as in *equation 2. 36*.

$$J = \left(\frac{9}{8}\right)\varepsilon_0\varepsilon_r\mu\theta\left(\frac{V_{app}^2}{x^3}\right) \qquad 2.\ 36$$

Here,

$$\theta = \frac{p_f}{p_f + p_t} \approx \frac{N_V}{N_T}\exp\left[-\frac{\left(E_T - E_V\right)}{kT}\right] \qquad 2.\ 37$$

where ε_0 is the permittivity of free space, ε_r is the relative dielectric constant of the material, θ is the ratio of the free carrier concentration, p_f to the total carrier concentraion, p_t is the trap carrier concentration, N_T is the DOS at the transport energy level E_T, and E_V is the valence band edge.

The application of *equation 2. 36* assumes a constant mobility term, which as has been mentioned extensively is not the case for organic semiconductors thereby prompting the need for an expression for the SCLC in organic semiconductors. The term θ, commonly found in the SCLC expression, is the ratio of free injected carriers to the total injected carriers whereby in inorganic semiconductors, the trapped carries are associated with extrinsic energy levels found

between the Fermi level and the valence band energy level [62]. On the other hand, in the organic model used in this work, θ is treated differently such that both the free and trapped carriers are associated with the intrinsic energy levels found within the DOS of the material. With this definition in mind, the modified expression for θ takes the form given by *equation 2. 38* and the SCLC expression for the disordered material is given by *equation 2. 39* (full details of the derivation are given in Appendix D). The slope of the double logarithmic plot of *equation 2. 39* yields the degree of disorder *m* and subsequently T_C. In addition, the mobility prefactor, *K* can be obtained from the intercept.

$$\theta = \frac{T_0}{T_0 + T_C} = \frac{T}{T_C} \qquad 2.\ 38$$

$$J = \frac{K}{q^m}\left(\frac{\varepsilon_0 \varepsilon_r \theta(m+1)}{m+2}\right)^{m+1}\left(\frac{2m+3}{m+2}\right)^{m+2}\frac{V_{app}^{m+2}}{x^{2m+3}} \qquad 2.\ 39$$

Alternatively, the application of a reverse bias increases the potential barrier at the interface of the Schottky contact and the semiconductor, as well as expansion in the depletion width. In the presence of image-force barrier lowering and applied field [56], the reverse current density, J_R, takes the form given in *equation 2. 40* (the full derivation is provided in Appendix E).

$$J_R = J_0 \exp\left[\frac{q}{kT}\left(\frac{q^3 N_A}{8\pi^2 \varepsilon_0^3 \varepsilon_r \varepsilon_\infty^2}\left(V_{app} - V_{bi} - \frac{kT}{q}\right)\right)^{1/4}\right] \qquad 2.\ 40$$

where N_A is the acceptor density, ε_∞ is the high-frequency permittivity of the semiconductor, and V_{bi} is the built-in potential.

By plotting the semi-logarithmic plot of J_R versus $Vapp^{1/4}$, the values of N_A and V_{bi} can be extrapolated from the slope and intercept respectively as will be done in chapters 3 and 4. The extraction of N_A from the plot is done under the assumption of the applicability of an abrupt

depletion edge approximation whereby the carrier concentration is assumed to sharply increase at the edge of the depletion layer having a width, *W*, given by *equation 2. 41*.

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_A}\left(V_{app} - V_{bi} - \frac{kT}{q}\right)} \qquad 2.\ 41$$

However, the carrier concentration increases gradually at the edge of the depletion region by a Debye length, L_{Debye} that is given by:

$$L_{Debye} = \sqrt{\frac{\varepsilon_0\varepsilon_r kT_C}{q^2 N_A}} \qquad 2.\ 42$$

Therefore, the approximation is assumed valid in organic semiconductors when the depletion width is much larger than the Debye length.

2.3.2 THEORY OF TFTs

A thin-film transistor (TFT) is a type of field-effect transistor consisting of three terminals (gate, source and drain). It regulates the current on somewhat similar basic principles as that of the Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). The main differences in the two devices is the thinner active layer found in TFTs, differences in the material properties and the differences in the modes of conduction. The source and drain contacts in TFTs are typically made using Ohmic contacts, whereas in MOSFET devices they are usually made of either *p*-type or *n*-type doped regions thereby forming *p*-*n* junctions with the semiconductor bulk. The off state current in MOSFETs is controlled by the depletion region occurring at the *p*-*n* junctions formed at the bulk/contact interface [56] whereas in TFTs it is characterised by the bulk resistivity of the organic film [65].On the other hand, in the on state, *p*-type TFTs operate in accumulation mode whereby the majority carriers (holes), accumulate at the interface of the dielectric and semiconductor upon application of a negative gate bias whereas for MOSFETs, the on state is dictated by an inversion layer of minority carriers formed at the dielectric/semiconductor interface.

The very first expressions derived for the drain current in TFTs was introduced by Borkan and Weimer [66]. Assuming a conventional *p*-type inorganic TFT, upon application of a positive gate bias i.e. $V_G > 0$, positive charges get induced on the gate contact thereby resulting in depletion of majority carriers at the interface of the gate and the semiconductor as depicted in *Figure 2. 9 a).*When a small negative bias is applied at the drain contact, holes migrate towards the drain contact thereby resulting in current flow as in *Figure 2. 9 b).* This current is mainly dependent on the bulk conductivity σ_p of the semiconductor and corresponds to the leakage current/off-state current of the transistor due to lack of formation of a channel. The drain current, I_D in this regime takes the form given by *equation 2. 43*.

$$I_D = \sigma_p x_p V_D \frac{W}{L} \qquad 2.\ 43$$

where x_p is the thickness of the semiconductor, V_D is the drain voltage; W and L are the channel width and channel length respectively.

When the polarity of the gate voltage is reversed i.e. $V_G < 0$, negative charges are induced on the gate contact thereby resulting in accumulation of holes at the gate/semiconductor interface. Holes begin to accumulate at the drain end with the application of a negative drain bias i.e. $V_D < V_G < 0$, as depicted in *Figure 2. 9 c).* With further application of a negative gate bias, more holes accumulate between the source and drain contacts as shown in *Figure 2. 9 d).* This results in an increase in the drain current, which corresponds to an on-state regime where the linear drain current I_{Dlin}, [65] takes the form of:

$$I_{Dlin} = \beta\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \qquad 2.\ 44$$

Here,

$$\beta = \mu C_{ox} W/L$$

$$V_T = \frac{(Q_s - Q_f)}{C_{ox}} + \psi$$

where μ is the field-effect mobility, V_T is the threshold voltage, C_{ox} is the oxide capacitance, Q_s is the amount of the charge at the interface of the dielectric and semiconductor, Q_f is the

fixed charge occurring in the dielectric and ψ is the potential needed to induce satisfactory accumulation or inversion of carriers depending on the type of transistor.

By plotting I_D versus V_G (i.e. the transfer characteristics), the transconductance, g_m given by *equation 2. 45* can be obtained from the slope. Consequently, the linear field-effect mobility, μ_{lin} can be extrapolated from the linear regime.

$$g_m = \frac{\partial I_D}{\partial V_G} = \mu_{lin} C_{ox} W/L (V_D) \qquad 2.\ 45$$

Furthermore, from the plot of I_D versus V_D (i.e. the output characteristics), the channel conductance g_d given by *equation 2. 46* can be obtained from the slope in the linear regime as well.

$$g_d = \frac{\partial I_D}{\partial V_D} = \mu_{lin} C_{ox} W/L (V_G - V_T) \qquad 2.\ 46$$

In conventional inorganic TFTs, V_T corresponds to the gate potential required for the onset of conduction or in other words, it defines the onset of a drift mechanism from a diffusion one. On the other hand, as OTFT devices operate in drift mechanism even at low operational voltages, V_T instead corresponds to the amount of gate bias for which substantial charge carriers are accumulated at the dielectric/semiconductor interface in comparison to the bulk of the semiconductor thereby turning on the transistor. The region below V_T is commonly referred to as the subthreshold region. Consequently, the subthreshold swing, S is a parameter used to typically define the amount of change of gate voltage required to turn the transistor off and on. By definition, it is the V_G needed to increase the drain current by one decade and it takes the form [67] below:

$$S = \frac{\partial V_{GS}}{\partial(\log I_D)} = \frac{\partial V_{GS} \ln 10}{\partial(\ln I_D)} = \frac{kT}{q} \ln 10 \cdot \left[1 + \frac{q t_{ox}}{\varepsilon_{ox}} \left(\sqrt{\varepsilon_r N_{sc}} + q N_{ss} \right) \right] \qquad 2.\ 47$$

where t_{ox} is the dielectric thickness, N_{SC} is the density of space-charge per unit volume per hole volt and N_{SS} is the density of surface states per unit area per hole volt.

It follows from *equation 2. 47,* that the subthreshold swing in inorganic TFTs is dependent on the dielectric thickness and density of surface states. For low power consumption and high speed in circuits, smaller values of *S* are desirable.

Upon further increasing the gate voltage i.e. $V_G - V_T = V_D$, pinch-off condition takes place, such that the field from the source towards the drain terminal gradually drops down and the drain current begins to saturate due to fewer carriers present at the drain terminal as in *Figure 2. 9 d).* Increasing the drain voltage i.e. $V_D < V_G - V_T$, results in changing the direction of the vertical field at the gate/semiconductor interface thereby reducing further the number of carriers at the drain end such that there is no channel present at the edge of the drain contact, leaving the drain current to remain nearly constant and independent of applied drain bias. The saturation current, I_{Dsat}, ignoring channel length modulation is therefore given by:

$$I_{Dsat} = \beta \frac{(V_G - V_T)^2}{2} \qquad 2.\ 48$$

In addition, the saturation field-effect mobility, μ_{sat} takes the form:

$$g_m = \mu_{sat} C_{ox} W/L (V_G - V_T) = \left(2\mu_{sat} C_{ox} W/L I_D\right)^{0.5} \qquad 2.\ 49$$

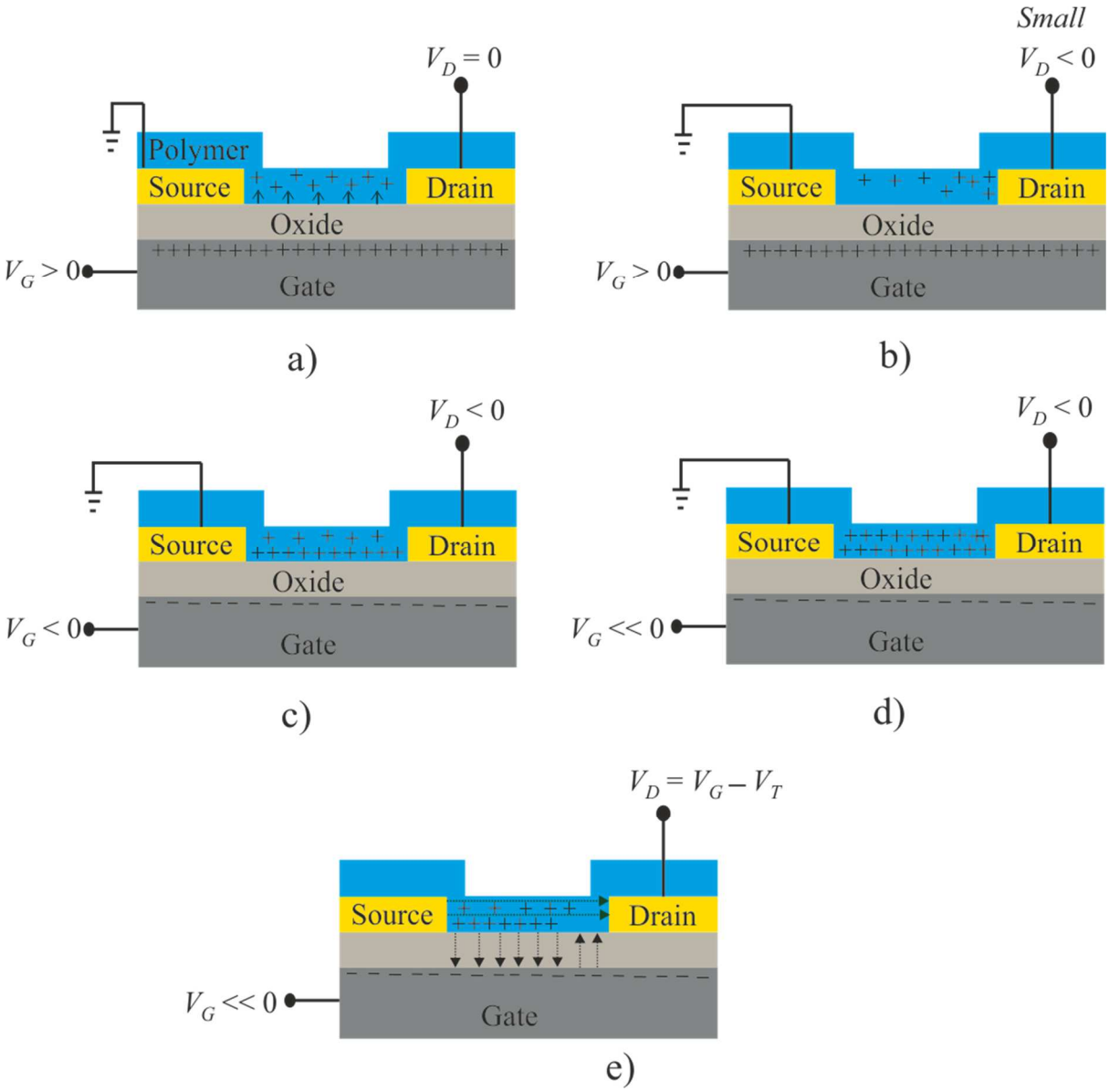

Figure 2. 9: Basic theory of the operation of a TFT: a) Holes accumulate at the surface of the semiconductor with application of V_G. b) Holes move toward the drain with application of small V_D. c) Accumulation of holes at the oxide and semiconductor interface with negative V_G. d) Increased accumulation of holes in the channel with injection of carriers at the drain. e) No carriers at the drain end when $V_D=V_G-V_T$ resulting in pinch off.

To analyse the OTFT results in this thesis, an appropriate model that takes into account the carrier-dependent mobility, as predicted by the UML, is developed just as it is done for the Schottky diodes before. The expressions for the linear OTFT drain current and saturation drain current used in this work are given by *equation 2. 50* and *equation 2. 51* respectively. The full details of the derivation of the equations are provided in Appendix F.

$$I_{lin} = \frac{W}{L}\frac{KC_0^{2m+1}}{(2m+1)(2m+2)(2\varepsilon_0\varepsilon_r kT_C)^m}\times\left[(V_G - V_T)^{2m+2} - (V_G - V_T - V_D)^{2m+2}\right] \quad 2.\ 50$$

$$I_{sat} = \frac{W}{L}\frac{KC_0^{2m+1}}{(2m+1)(2m+2)(2\varepsilon_0\varepsilon_r kT_C)^m}\left[(V_G - V_T)^{2m+2}\right] \quad 2.\ 51$$

By differentiating and taking the logarithm of *equation 2. 51* as shown in *equation 2. 52*, the material parameters *m* and *K* can be obtained evaluated. The values of such material parameters will be extracted and compared to those obtained from Schottky measurements taken for the same *p*-type semiconductor, as discussed in chapters 3 and 4.

$$\log\left(\frac{dI_{sat}}{dV_G}\right) = \log\left(\frac{WKC_0^{2m+1}}{L(2m+1)(2k\varepsilon_0\varepsilon_r kT_C)^m}\right) + (2m+1)\log(V_G - V_T) \quad 2.\ 52$$

An expression for the effective mobility, μ_{eff} can be obtained by equating the disordered saturation current expression (*equation 2. 51*) to the square-law MOSFET saturation current, *equation 2. 48*, resulting in:

$$\mu_{eff} = \frac{KC_0^{2m}}{(2m+1)(2m+2)(2k\varepsilon_0\varepsilon_r kT_C)^m}(V_G - V_T)^{2m} \quad 2.\ 53$$

2.4 CONCLUSIONS

This chapter gave a brief overview of the physics of conjugated polymers. The band structure in these materials is explained using the Hückel Molecular Orbital Theory where the LUMO and HOMO energy levels are analogous to the conduction and valence band energy levels in inorganic semiconductors.

In organic materials, the number of states per energy interval at a given energy level can be explained using a DOS function, which follows either a Gaussian distribution or an Exponential distribution. Evidence for both types of DOS has been shown in literature; however, the amount of residual dopant ions present in the film as well as the type of device used for making the test measurements may have an impact on the shape. Nonetheless, in this

work, an exponential approximation to the tail of the Gaussian DOS is assumed as the curves at the lower energy ranges of the Gaussian DOS corresponds accurately with the Exponential DOS which is the range in which decisive charge transport in OTFTs and Schottky diodes takes place.

Charge transport in organic materials generally takes place through thermal activation of carriers between localised states. It is shown that the charge transport can be explained by a superposition of polaronic and disordered effects whereby a disordered charge transport is said to be dominant when the polaron binding energy values are small in comparison to the width of the DOS. In such a case, the effective mobility shows a strong dependency on carrier concentration as described by the UML whereas in a pronounced polaronic transport regime, the mobility shows a weaker dependency on carrier concentration because the polaron activation energy is independent of the concentration of the polarons.

The basis of the MNE and its physical understanding in the framework of organic semiconductors is also discussed. The MNR has been observed in experiments where the carrier concentration is varied, however, in some experiments, the same dependency is not observed when the width of the DOS is directly varied, thereby contradicting the MNR in organic semiconductors and leading other authors to suggest that the MNR is instead an apparent compensation effect related to charge transport rather than the DOS. The so-called compensation effect is recently observed in organic materials having a dominant disordered system, such that in this case, the MNE is found to be determined by the partial filling of the DOS due to field-effect as well as the shape of the DOS and the polaron binding energy. Evidently, the debate on the significance of the MNE in organic materials is not settled yet, however, in this work, the MNE has been assumed to be related to the width of the exponential DOS.

An analytical model for the expression of the effective mobility is also described in this work. It is derived by making a comparison of a disordered system in contact with an ordered system whereby movement of carriers can be described by means of a charge transport level similar to the valence band in a crystalline semiconductor. The model shows a carrier concentration dependency on mobility similar to UML and similar to the expressions obtained using a percolation theory approach. Utilising the new expression for the effective mobility, disordered models for the current transport in Schottky diodes and TFTs are developed as well

resulting in additional material parameters such as *MNE, K* and *m*. These parameters can be used instead for designing circuits, as they are material constants, which are independent of the carrier density unlike the effective mobility term. Furthermore, the experimental values obtained from Schottky and TFT devices can be used in future as a characterisation and validation tool for a given material as will be done in Chapters 3 and 4 of this thesis.

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CHAPTER 3

A Comparative Study of the Charge Transport Properties of Thiophene-Based Polymers made using Schottky Diodes

This chapter discusses the charge transport study of two thiophene-based polymers: indacenothiophene–benzothiadiazole (IDTBT-C16) and
poly [2, 5-bis (3-hexadecylthiophen-2-yl) thieno [3, 2-b] thiophene] (PBTTT-C16) which were provided by Prof. M. Heeney from Imperial College London. The study is investigated with the aid of temperature variation of the current-density voltage characteristics of vertical Schottky diodes, made using these materials. The activation energy is evaluated using Arrhenius plots of the forward current density measurements taken at relatively high temperatures. Forward and reverse current density characteristics of the devices are also discussed.

3.1 INTRODUCTION

Research into material design strategies of solution-based semiconducting polymers has led to a substantial increase in the achievable field-effect mobility values of conjugated polymers, whereby values ≥ 1 cm^2/Vs [1-3] have been reported. Among these organic semiconductors, some of the highest charge carrier mobility values have been obtained from thiophene based polymers containing alkyl side chains. Such high mobility values have been attributed to their highly ordered two-dimensional (2D) structural motif. The polymer family series of poly [2, 5-bis (3-hexadecylthiophen-2-yl) thieno [3, 2-b] thiophene] (PBTTT) [4], has emerged as a prime example of the correlation of a high charge carrier mobility to a highly ordered 2D structural motif. The as-mentioned motif has long been believed to facilitate charge transport along the polymer chain (intramolecular hopping) as well as between adjacent chains (intermolecular hopping) through π-π stacking. The PBTTT film is typically characterised by individual monomer units, lying along the monomer backbone in a coplanar manner, thereby facilitating a tilted, face to face arrangement of the adjacent polymer backbone [5,6] as represented in *Figure 3. 1 a).* The latter arrangement results in an extended, laterally ordered structure typically referred to as a π-stacked lamella backbone [7]. The polymer film is ordered further through interdigitating of the alkyl side chains via thermal annealing facilitating a closer π-π stacking motif as shown in *Figure 3. 1 b).*

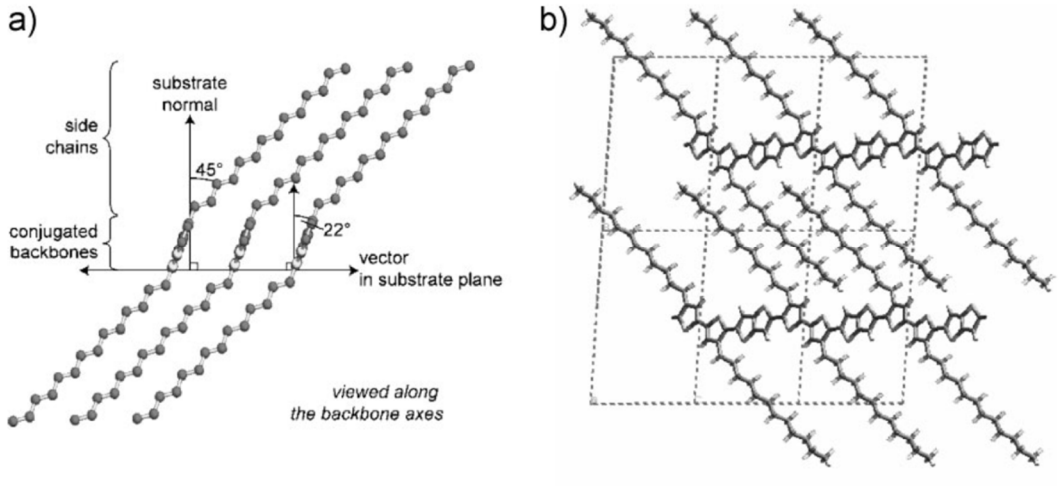

Figure 3. 1: (a) Coplanar arrangement of the individual PBTTT monomer units lying along a monomer backbone. (b) Structure of the interdigitated alkyl side chains resulting in closer π-π stacking. Image taken from [8].

On the other hand, the latest advancements in research have seen the birth of conjugated polymers made with interchanging donor-acceptor backbone configurations [8-10] that exhibit significantly higher values of mobility (1-10 cm^2/Vs) despite lacking long-range order, unlike the previously mentioned thiophene polymers. This is attributed to the backbone rigidity found within the copolymers. For instance, indacenothiophene–benzothiadiazole (IDTBT-C16) copolymer has been shown to have mobility values exceeding 1 cm^2/Vs due to its "near-torsion-free" backbone and its planar conformation whilst in solid form [11,12]. In such materials, the charge transport is believed to be controlled by conduction along the disorder-free backbone with minimal intermolecular hopping thereby resulting in the observed higher charge-carrier mobility values [12]. The above observation highlights the fact that further research work is needed in order to get a better understanding of the underlying phenomena/structural features that facilitate charge transport in conjugated polymers, thus resulting in higher charge carrier mobility values. In other words, further insight into the charge transport mechanism in conjugated polymers is necessary for future design strategies of organic semiconductors.

In this chapter, a charge transport study is carried out with the aid of temperature measurements of the current density-voltage *J-V* characteristics of vertical Schottky diodes, made using high charge carrier mobility polymers: IDTBT-C16 and PBTTT-C16 respectively. *Figure 3. 2* shows the chemical structure of the two polymers.

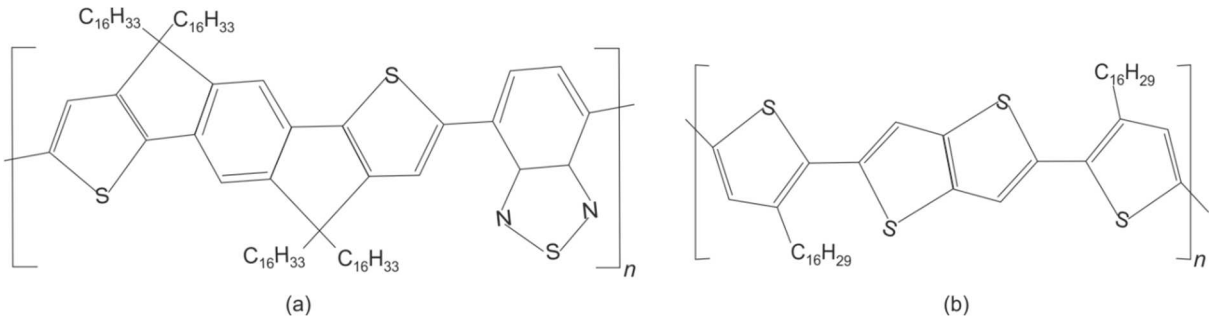

Figure 3. 2: Structure of (a) Indacenothiophene–benzothiadiazole (IDTBT-C16) copolymer and (b) Poly [2, 5-bis (3-hexadecylthiophen-2-yl) thieno [3, 2-b] thiophene] (PBTTT-C16) polymer.

Whilst the vertical diode topology is used for characterisation in this chapter, the lateral diode topology is also fabricated and used for electrical characterisation in the subsequent chapter; therefore, the differences of the two topologies will be briefly discussed here. The vertical organic Schottky diode structure normally consists of an organic semiconductor inserted between the Ohmic and Schottky contacts. The processing steps for this device include the thermal deposition of the contacts and the polymer deposition of the semiconductor achieved either by drop casting, spin coating or printing from solution. Film thicknesses ranging from a few hundred nanometres to around 10 μm can be obtained as a result depending on the deposition process. The film thickness and morphology of the organic semiconductor in vertical diodes is vital as it defines the electric field strength, with thinner films being the preferable option for yielding high forward current density values. On the other hand, thicker and uniform films are also desirable as they reduce short-circuiting effects between the metal contacts although at the cost of an increase in the reverse current density values thereby resulting in poor rectification properties of the device. A good balance/trade-off between the two characteristics would therefore be needed in order to achieve optimal device performance with this topology.

In lateral diode structures, both of the contacts are thermally deposited onto the substrate whist the semiconductor is typically deposited via spin coating onto the top of the contacts. Depending on the solution concentration and the spin speeds used, relatively uniform films of a few hundred nanometres are formed as a result. Unlike vertical diodes, the inter-electrode distance between the contacts determines the electric field strength with very small gap sizes (<1 μm) being the preferred option for intensifying the field. However, this is quite difficult to achieve using conventional photolithography processes because of the low resolution of the equipment. The lateral diode topology is a desirable topology as it enables the realization of diode integration in circuits, which would otherwise be complex and more expensive to implement with vertical diodes. However, it is more difficult to chemically modify the interface of the Ohmic contact and the semiconductor without simultaneously altering the properties of the Schottky contacts as well particularly when using devices with small feature sizes.

Using the organic Schottky diode model developed in chapter 2, the forward current density at high applied bias, with changes in temperature, can be used to extract the activation energy, E_A, of the materials under study. As mentioned in the previous chapter, charge transport

in conjugated polymers is attained through the thermal hopping of carriers from an occupied site to an unoccupied site. The thermal hopping of carriers is characterised by an activation energy. The activation energy signifies the energy difference between the trapped carriers and the mobile states, which is a significant parameter in understanding and establishing the mechanism of charge transport in conjugated polymers. In addition to studying the charge transporting nature of such materials, the forward and reverse current density characteristics of the Schottky diodes are also analysed using the organic Schottky diode model, and where applicable, the limitations of the models are highlighted.

3.2 FABRICATION OF VERTICAL IDTBT-C16 AND PBTTT-C16 SCHOTTKY DIODES

The structure of the vertical diode used in this work is as represented in *Figure 3. 3*.

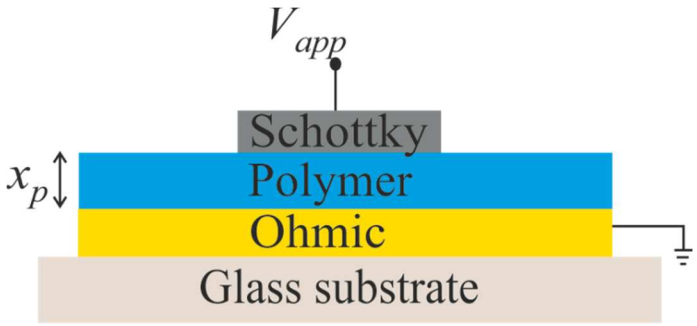

Figure 3. 3: Structure of the vertical Schottky diode, with aluminium and gold as the Schottky and Ohmic contacts respectively. The polymer (IDTBT-C16 or PBTTT-C16) with a thickness x_p, is sandwiched between the contacts.

A 100 nm gold layer purchased from Alfa Aesar, UK is thermally evaporated onto two pre-cleaned glass slides ordered from Corning Incorporated, USA. To reduce the work function of the gold contacts in order to make an Ohmic contact with the organic semiconductor layer, samples are immersed in a 0.5 mM solution of pentafluorobenzenethiol (PFBT) and propanol, for 10 minutes, followed by a thorough rinse in propanol. The PFBT molecules are believed to bind to the metal surface thereby inducing the formation of strong surface dipoles that shift the vacuum level. This shift results in a reduction of the work function of the metal and consequently a reduction in the barrier height at the interface of the metal contact and the

semiconductor [13,14].The aforementioned chemicals i.e. PFBT and propanol, are respectively acquired from Sigma-Aldrich Company Ltd, UK and Fisher Scientific Ltd, UK.

For the first sample, 10 mg/ml of IDTBT-C16 polymer is dissolved in chlorobenzene, followed by drop casting and annealing of the sample at 100 °C for 30 minutes in ambient conditions. For the second sample, a PBTTT-C16 solution is formed by dissolving 10 mg/ml of PBTTT-C16 polymer in hot (100 °C) dichlorobenzene, and leaving it to stir on a magnetic stirrer hot plate for about three hours. While still hot, the solution is drop cast and annealed at 180 °C for 10 minutes, followed by a slow cooling down step at 5 °C/minute, through the liquid-crystalline mesophase region of the polymer. The ordering and π-packing morphology of PBTTT-C16 is widely known to be influenced by temperature, such that annealing the film in its mesophase, results in melting of the alkyl side-chains belonging to the polymer, which when left to slowly cool results into an ordered and well-interdigitated π-stacking structure [4]. Such deposition processes of both polymers results in thick films x_p, of typically 1 to 1.5 µm. Both polymers are obtained from Imperial College London, UK whereas the chlorobenzene and dichlorobenzene chemicals used to make the polymer solutions are bought from Sigma-Aldrich Company Ltd, UK. To reduce the oxidative effects brought on during processing, both samples are left in vacuum overnight. On the following day, an aluminium wire purchased from Testbourne Ltd, UK is thermally evaporated via a shadow mask onto the samples resulting in the formation of 100 nm thick aluminium dots that act as the Schottky contact to the polymers. This is believed to be the case given that the injection barrier between the Al layer and the respective polymer layers is significantly larger than the injection barrier formed between the Au layer and the polymer layers.

The differences between a Schottky contact and an Ohmic contact are briefly highlighted in the following section. A Schottky contact is attained when a metal comes into contact with a semiconductor such that a high resistance, potential barrier is formed at the interface as a result of the difference in work functions of the two materials [15]. The barrier formed from the Schottky contact limits the flow of carriers between the two materials as discussed in *section 2.3* of Chapter 2. To obtain a Schottky contact with an organic *p*-type semiconductor, a potential barrier is formed when the semiconductor is aligned with a metal having a work function lower than its HOMO level. In the absence of surface states occurring within the semiconductor, when the two materials come into contact, electrons move from the metal into the semiconductor to reach thermal equilibrium. A potential barrier consisting of

uncompensated acceptor ions is subsequently formed on the polymer side as a result. With the Fermi levels of the two materials aligned at thermal equilibrium, energy band-bending occurs at the interface and a barrier to hole transport is formed. With the application of a bias, the potential barrier can be reduced thereby facilitating current transport across the barrier. The theoretical band diagram of a Schottky contact to a *p*-type semiconductor is as illustrated in *Figure 3. 4*.

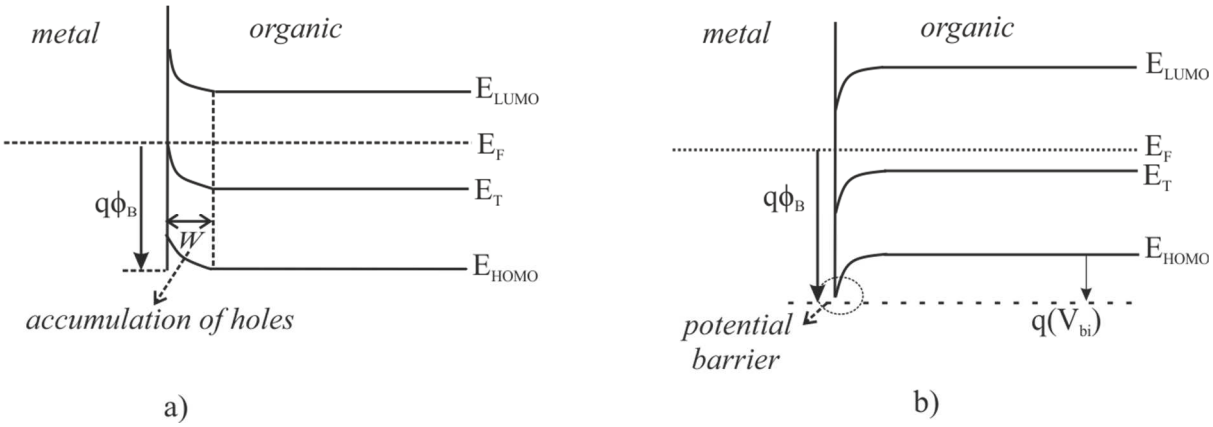

Figure 3. 4: (a) The theoretical band diagram of a p-type semiconductor in contact with an Ohmic metal contact at thermal equilibrium. The accumulation layer width, W, depends on the intrinsic carrier concentration of the polymer. (b) The theoretical band diagram of a p-type semiconductor in contact with a Schottky metal at thermal equilibrium. The built-in potential and energy barrier form because of the differences in the work functions of the two materials.

Unlike the Schottky contact, an ideal Ohmic contact is a contact where no potential barrier is formed at the metal/semiconductor interface thereby resulting in the free movement of carriers between the two materials. Nonetheless, the term 'Ohmic contact' is often times used to define low resistance contacts i.e. contacts that have negligible resistance in comparison to the resistance associated with the bulk of the semiconductor that it is in contact with [16].

To obtain an Ohmic contact with an organic *p*-type semiconductor, an accumulation layer is formed when the semiconductor is in contact with a metal having a higher work function than the HOMO level of the semiconductor. The resultant energy band bending due to the work function difference between the two materials attracts holes to accumulate at the

interface thereby giving rise to a small contact resistance associated with the accumulation layer as demonstrated in *Figure 3. 4.* The free carrier concentration of the semiconductor determines the width of the accumulation layer, *W*. With the application of a suitable bias, the hole density increases resulting in the reduction of the width of the accumulation layer and thus allowing passage of carriers with relative ease from the metal into the semiconductor and vice versa.

Current-voltage characterisation of the devices is performed in ambient conditions using a HP4145B semiconductor parameter analyser. Variable temperature characterisation is carried out at a pressure of 0.1 mbar, whereby the sample is cooled using a liquid nitrogen cryostat and heated using an electric heater.

3.3 PBTTT-C16 SCHOTTKY DIODE

3.3.1 CURRENT DENSITY-VOLTAGE CHARACTERISTICS OF PBTTT-C16 SCHOTTKY DIODE

The current density-voltage (*J-V*) characteristics of the PBTTT-C16 diode measured at room temperature and in ambient conditions are as shown in *Figure 3.5*. The diode has a rectification ratio of 8.1×10^2. As mentioned earlier, the polymer solution is drop-cast, which results in thicker films thus reducing the probability of short circuiting/punching through the top contact during probing of the samples. However, such thick films could also result in lower rectification ratios due to the larger bulk resistance of the polymer, which is in series with the potential barrier [17]. Moreover, chemical oxidative doping of polymers has been shown to occur when the ionisation potential (HOMO energy level) of the polymer is around or higher than −4.9 eV relative to the vacuum energy level (i.e. closer to the vacuum energy level) [18]. The theoretical value of the HOMO level of PBTTT-C16 polymer is −5.1 eV [4], which is quite close to the threshold limit, thereby making it susceptible to the aforementioned effect with time. The latter effect results in higher reverse and off current density values of the measured Schottky diode and OTFTs respectively.

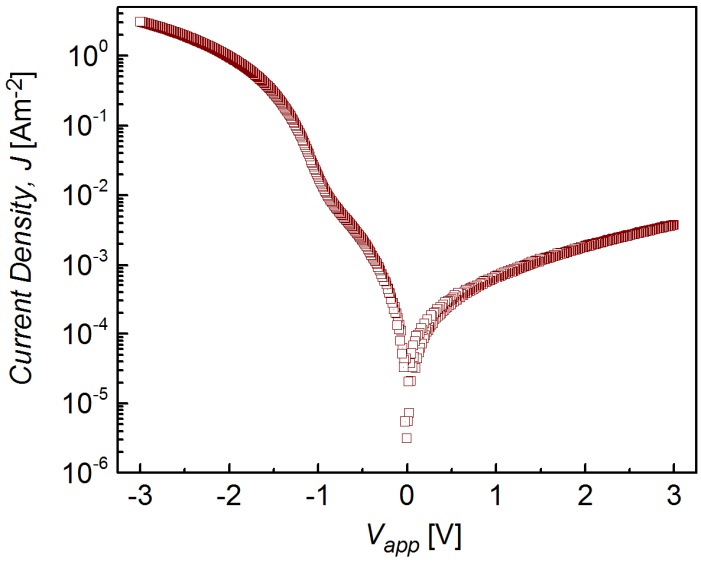

Figure 3.5: Semi-logarithmic plot of the current density-voltage characteristics of PBTTT-C16 Schottky diode. The voltage is applied to the Schottky contact with respect to the Ohmic contact.

Upon application of a forward bias, the current density increases exponentially due to an increase in carrier concentration, reflective of the exponential increase of the density of states distribution with energy as described in chapter 2. The characteristic temperature associated with the distribution of carriers, T_0, can be extrapolated from the slope of the forward current density given by *equation 2. 32*. The value of T_0 is found to be 708 K, and using the relation in *equation 2. 21*, the characteristic temperature associated with the intrinsic DOS, T_C, is found to be 524 K. This corresponds to a Meyer-Neldel Energy (*MNE)* of 45 meV, which is in close agreement to values obtained from field-effect Seebeck measurements [19] made using the same material. The microstructure of this material, as previously mentioned, is strongly controlled via thermal annealing, as the polymer is a liquid-crystalline mesophase polymer. Therefore, annealing the sample above its liquid-crystalline phase and allowing the sample to cool slowly should result in formation of large ordered crystalline domains i.e. the morphology of the polymer is dictated by thermal annealing. Based on the Seebeck measurements outlined by Venkateshvaran *et al.*, the width of the DOS of the material when in a crystalline state is 30 meV, whereas when it is disordered it is 48 meV [19]; thereby the extracted *MNE* in this work suggests that the fabricated material in this diode is likely to be in a disordered state with small semi-crystalline regions.

Furthermore, the forward current density plot displays a visible kink at around −1 V. The cause of the kink in the forward *J-V* characteristics is believed to be as a result of resonant

tunnelling [20]. By varying the potential bias applied to the electrodes, the Fermi levels of the electrodes can be moved relative to the energy levels of the molecules thereby making it possible to bring the Fermi energy levels of the contacts in resonance with the LUMO or HOMO energy level of the molecule. In this case, when both the Ohmic and Schottky contact have a zero applied bias, there is negligible resonant tunnelling current observed. Upon applying a negative bias on the Schottky contact, whilst keeping the Ohmic contact grounded, an exponential increase in the forward current density is observed, as expected, until a maximum in peak current flowing between the two electrodes via the polymer molecules is reached at around a voltage bias of −0.8 V as observed in *Figure 3.5*. It is at this point where it is believed that the Fermi level of the Al contact aligns with the HOMO level of the polymer resulting in the occurrence of resonant tunnelling [21]. The current slightly decreases or "dips" thereafter as a result of the reduction of the coupling of the molecules to the electrodes. With further application of a negative bias, the forward current density values continue to increase as a result of the increase in carrier concentration.

Other studies have attributed the observed kink effect to be as a result of conformational changes in the molecules [22] which generally results in the creation of relatively narrow features in the density of states of the polymer. With the application of a bias voltage, the energy levels of the semiconductor may move as a result of the change in the electrostatic potential distribution in the molecular system. At certain voltage values, adjacent segments of the energy levels match whereas at other values they mismatch [23,24]. The coupling of matched segments would be expected to be stronger than the coupling of the mismatched segments thereby resulting in variations of the coupling strength between the molecules and the electrodes with applied bias and hence could account for the peak and dip in the current that is observed in the current-voltage characteristics.

Utilising *equation 2. 33*, the value of η is found to be 2.3. In inorganic semiconductors, η values greater than 1 are associated with spatial barrier height variations at the interface of the metal and semiconductor, which are a result of a non-uniform doping of the semiconductor layer [25,26], dopant crowding effects [27], a combination of dissimilar metallic phases resulting in varying degrees of the interface metallurgy [28], high interface state density due to local strain [29], or due to an interfacial oxide layer. To account for the aforementioned

inhomogeneity, Werner and Gutler [30] proposed a model, using a Gaussian distribution function where the barrier height, F_{Bn}^{j}, is given by,

$$F_{Bn}^{j} = \overline{F}_{Bn} - \frac{\sigma_F^2}{2kT} \qquad 3.\ 1$$

where $\overline{F}_{Bn}$ is the mean value of the barrier height and σ_F is the standard deviation of the barrier height.

Conversely, in organic semiconductors, η has been shown to be related to the degree of energetic disorder σ [31-33] or T_C depending on the shape of the density of states chosen i.e. either a Gaussian or an exponential shape respectively. The effective ideality factor n_f, has therefore been correlated to the Gaussian density of states [34] using *equation 3. 2* below,

$$n_f = \frac{\eta}{1 + k/2} \qquad 3.\ 2$$

Here,

$$k = 0.73 - 1.17 \cdot \overline{\sigma} \cdot \exp\left(-\frac{\overline{\sigma}}{1.65}\right)$$

where $\overline{\sigma}$ is the variance of the width of the DOS.

Equation 3. 2 shows that an increase in σ or T_C results in an increase in the ideality factor. Furthermore, η is expected to have a charge density dependency/voltage dependency as evidenced by Roichman and Tessler whereby an increase in the relative charge density resulted in higher ideality factor values [34]. The high value obtained for η (2.3) could therefore be related to the intrinsic width of the DOS of the material as well as a result of barrier inhomogeneity at the interface of the Schottky metal and the polymer.

To investigate further on the conduction mechanism of the PBTT-C16 Schottky diode, a double logarithmic plot of the forward characteristics is plotted in *Figure 3.6*. Based on SCLC theory discussed in chapter 2, at very low applied forward bias, the field due to the injected carriers is mostly in the region occurring close to the injecting electrode and is negligible across most of the film thereby leading to an Ohmic dependency within a voltage range of 0 V to −0.5 V.

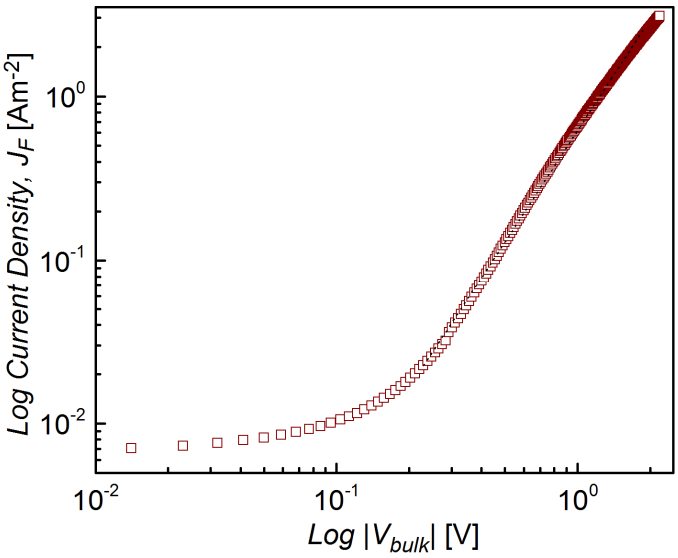

Figure 3.6: Double-logarithmic plot of the forward characteristics versus bulk voltage of the PBTTT-C16 Schottky diode.

The current density dependency on voltage deviates from an Ohmic one (given that that slope of the graph in *Figure 3.6* has a value of approximately 1.0 at lower forward bias) to a space charge limited one (slope of about 2.75 obtained) upon application of higher forward bias due to accumulation of a non-uniformly distributed layer of excess charge from the injected carriers. As the Fermi level is widely believed to lie within the tail of the Gaussian DOS, it follows that the quasi-Fermi level already intersects the intrinsic deep-tail sites thereby implying that the SCLC dependency would be described by the exponentially filling intrinsic trap distribution occurring at the tail. Chemical defects may manifest as a discrete/exponential distribution of extrinsic traps occurring near the tail of the Gaussian DOS as illustrated in *Figure 3.7* while the conduction sites are located further down in energy towards the centre of the Gaussian DOS.

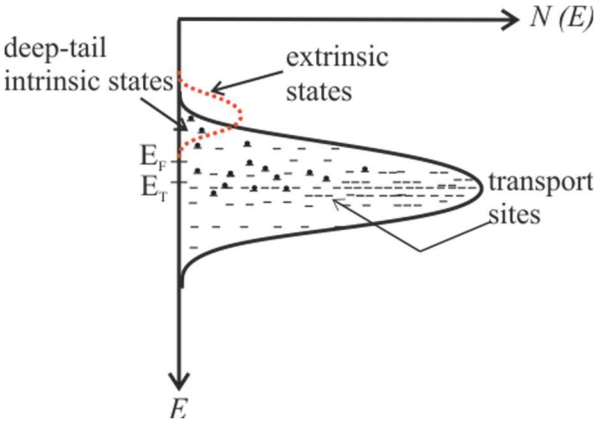

Figure 3.7: Model of the trapped states whereby intrinsic trap states occur deep in the tail of the Gaussian DOS and the extrinsic states due to chemical or structural defects occur near the tail. The conduction sites occur at lower energy levels below the Fermi level for a p-type semiconductor.

At higher forward bias and with increase in carrier concentration, according to Pauli's exclusion principle, the very few states occurring at higher energy levels (above and near the Fermi level) i.e. the trap sites, will be filled with carriers [35]. Carriers below the Fermi level will be filled once the rest of the higher energy levels are almost full. At this point, as there are fewer unoccupied sites above the Fermi level, the number of free carriers will increase at a much higher rate in comparison to the trapped carriers. The rest of the current density on further application of forward bias would be mainly due to hopping of free carriers at lower energy levels as the effect of trapped carriers is considered negligible. From the double-logarithmic plot of the forward current density versus applied voltage, the value of K is obtained and substituted into *equation 2. 39*, thereby yielding an effective mobility of 0.13 cm^2/Vs. The field-effect mobility values of this material have been reported to range between 0.1-1 cm^2/Vs. The possible reason for the variation could be attributed to the morphology of the polymer, which as indicated before is dependent on the processing conditions [36-38].

The reverse current density, J_R also increases with the application of a reverse bias, V_R thereby suggesting the possibility of barrier lowering, $\Delta\phi_B$, given by *equation 2. 40* in chapter 2. The straight-line fit of the semi-logarithmic plot of J_R versus $V_R^{1/4}$ as shown in *Figure 3.8*, confirms the applicability of the barrier lowering phenomena. The value of the acceptor density N_A, extrapolated from the slope of the graph is found to be approximately 1.6×10^{22} m^{-3} assuming an abrupt depletion edge approximation. The latter is assumed valid in organic

semiconductors when the depletion width is much larger than the Debye length. Given the N_A value obtained, the ratio of W/L_{Debye} is found to be 14 implying that the approximation is applicable.

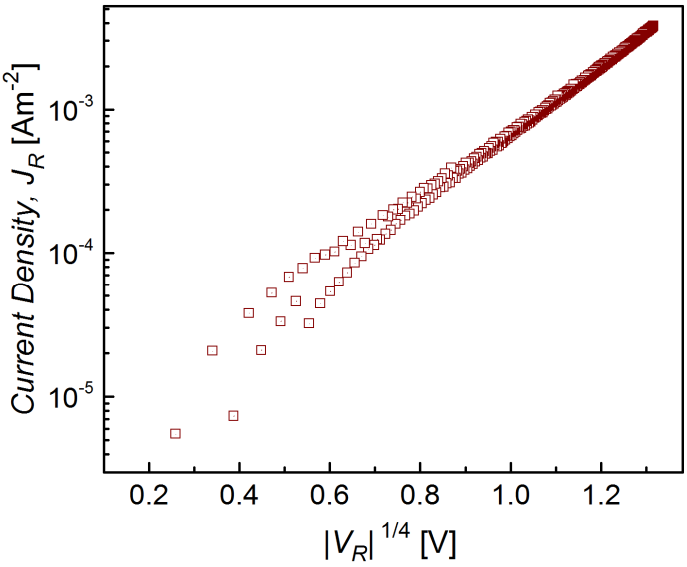

Figure 3.8: Reverse current density against $|V_R|^{¼}$ for the PBTTT-C16 Schottky diode. The deviation of the linearity at lower applied voltages is due to the (V_{bi}-V_R-kT/q) term.

The value of the saturation current density is extrapolated from the intercept of *Figure 3.8* and substituted into *equation 2. 29* to extrapolate the barrier height of the Al/PBTTT-C16 Schottky diode, which is found to be 0.92 eV. The theoretical barrier height is 0.8 eV. The differences in the values obtained could be associated with the kink observed in the graph, which perhaps results in erroneous values of the saturation current density.

3.3.2 TEMPERATURE-DEPENDENCE OF PBTTT-C16 SCHOTTKY DIODE

In order to understand the charge transport properties of PBTTT-C16 polymer, current density-voltage measurements are carried out at temperatures of 140 K to 320 K as shown in *Figure 3. 9.*

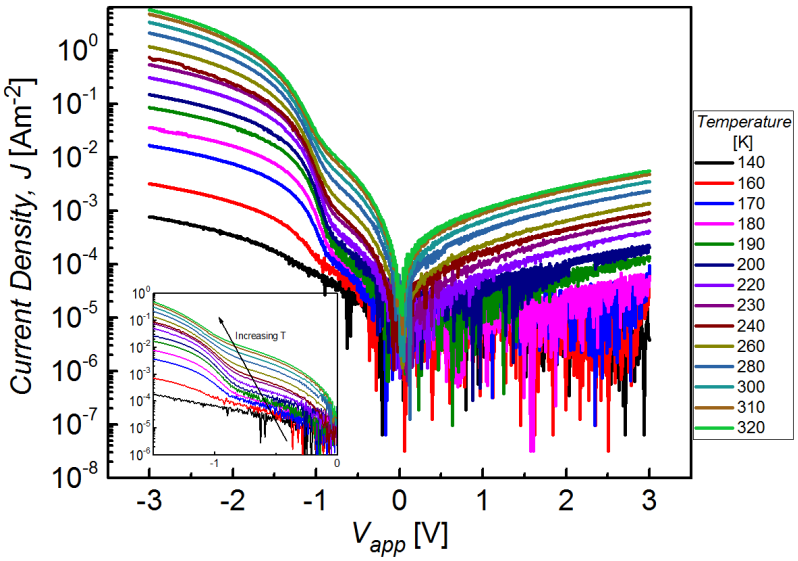

Figure 3. 9: Semi-logarithmic plot of current density-voltage characteristics of PBTTT-C16 Schottky diode measured at a temperature range between 140 K and 320 K. The voltage is applied onto the Schottky contact while the Ohmic contact is grounded.

With the decrease in temperature from 320 K to 140 K, the forward current density is reduced by three orders of magnitude, whereas the reverse current density is reduced by two orders. The reduction in the latter with temperature can be attributed to an increase in barrier height brought on by shifting of the quasi Fermi-level to lower energy levels with falling temperature.

Figure 3. 9 (inset) shows the linear fits to the semi-logarithmic plots of J_R versus $V_R^{¼}$ for temperatures ranging from 190 K to 320 K. Such agreements confirm the applicability of the barrier lowering phenomena within the specified temperature range. For temperatures of less than 190 K, the measured reverse current density is found to be very noisy thereby raising doubts regarding the accuracy of fitting of the data to the above plot. Values of N_A extrapolated from the slope in *Figure 3.10*, appears to increase slightly from 5.87×10^{21} m^{-3} to 1.81×10^{22} m^{-3}, as the temperature increases from 190 K to 320 K . Such a decrease in acceptor density with decrease in temperature is thought to be associated with the reduction of deionised dopants, resulting in "freeze-out conditions" [39] where the acceptor states recombine with their charge carriers as the temperature drops, akin to inorganic extrinsic semiconductors.

Consequently, the free carrier density within this temperature range is assumed to be approximately equal to the acceptor density N_A [40].

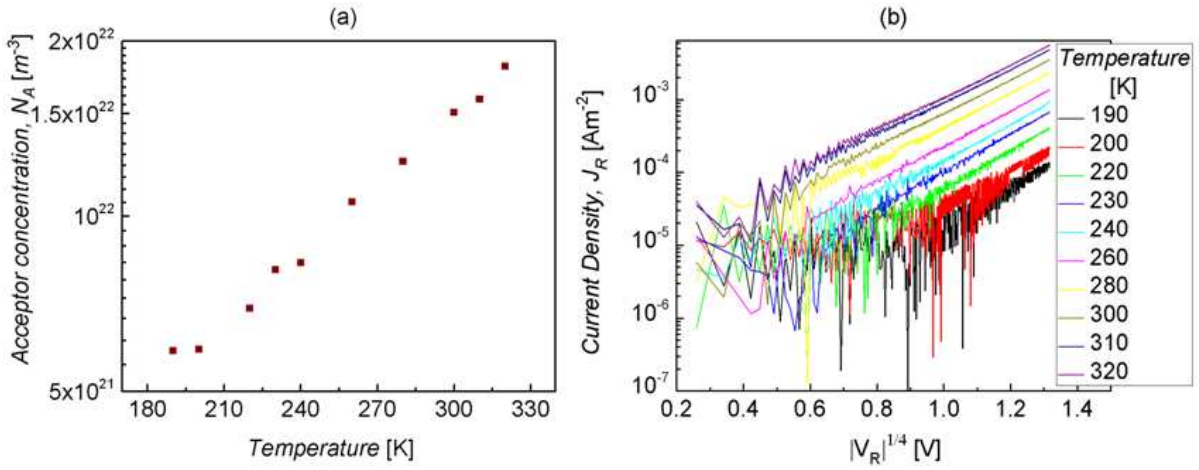

Figure 3.10: (a) Variation of the acceptor concentration N_A, with varying temperature. The values of N_A are extracted from the semi-logarithmic plot of the slope of the reverse current density with $|V_R|^{¼}$ as shown in (b).

The ratio of W/L_{Debye} varies slightly from 13 to 18 as the temperature increases; nonetheless, the large ratio indicates that the abrupt depletion width approximation is applicable. Moreover, respective values of the depletion width and Debye length are found to increase inversely with decrease in temperature, as depicted in *Figure 3.11*. Such a trend could be accounted for by the partially occupied acceptor states at lower temperatures that result in reduction in carrier concentration coupled with shifting of the quasi-Fermi level. This subsequently leads to increasing of the depletion region width as well as the Debye length.

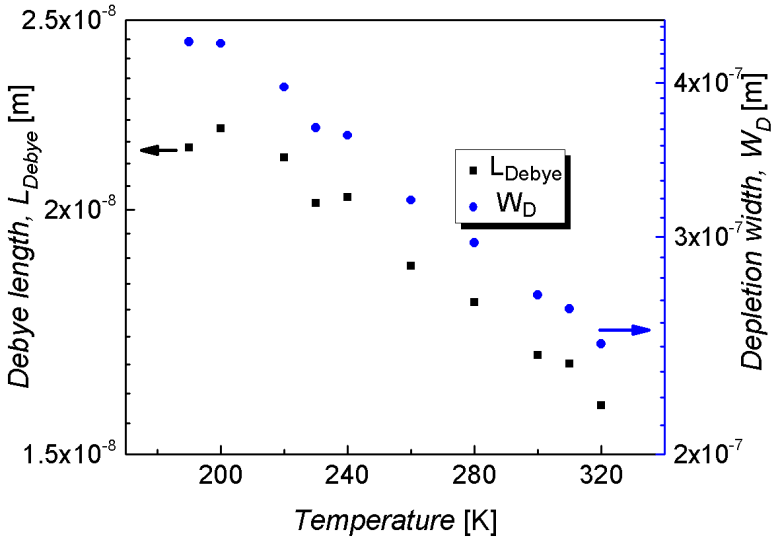

Figure 3.11: Logarithmic plot of the depletion width, W and Debye length, L_{Debye} with varying temperature from 190 K to 320 K.

The increase in the forward current density of organic Schottky diodes is because of an increase in the effective mobility brought on by an exponential increase in the carrier concentration. It is clear from the previous section that the carrier concentration, *p* (assumed to be approximately equal to the acceptor density N_A within the given temperature range of 190 K to 320 K) remains nearly constant in spite of an increasing forward current density. The derived carrier concentration given by *equation 2. 20* implies that the carrier concentration is dependent on the position of the Fermi level, E_F as well as the characteristic temperature associated with the distribution of carriers, T_0. Subsequently, with a drop in temperature, the quasi-Fermi level shifts to lower energy levels and the carriers rearrange with varying temperature, as the Fermi-Dirac distribution function is temperature-dependent. Although rearranging of the Fermi-Dirac statistics leads to more carriers being distributed towards higher energy levels, the likelihood of carriers hopping to adjacent sites is still restricted by the large distances between the occupied and unoccupied states. In chapter 2, it is highlighted that the charge transport in organic semiconductors typically occurs due to the thermally activated hopping of carriers from an occupied site to an unoccupied one. Consequently, the few carriers that are assumed to contribute to conduction (located below the E_F) will have much lower thermal energy to hop from site to site with decreasing temperature thereby reducing the forward current density. An increase in the thermal energy of the carriers would consequently increase the effective mobility and subsequently the forward current density. From the double-logarithmic plot of the forward current density versus applied voltage, the values of the

mobility prefactor, K, are obtained from the intercept of each temperature value and substituted into *equation 2. 24*, thereby yielding values of the effective mobility as plotted in *Figure 3.12*.

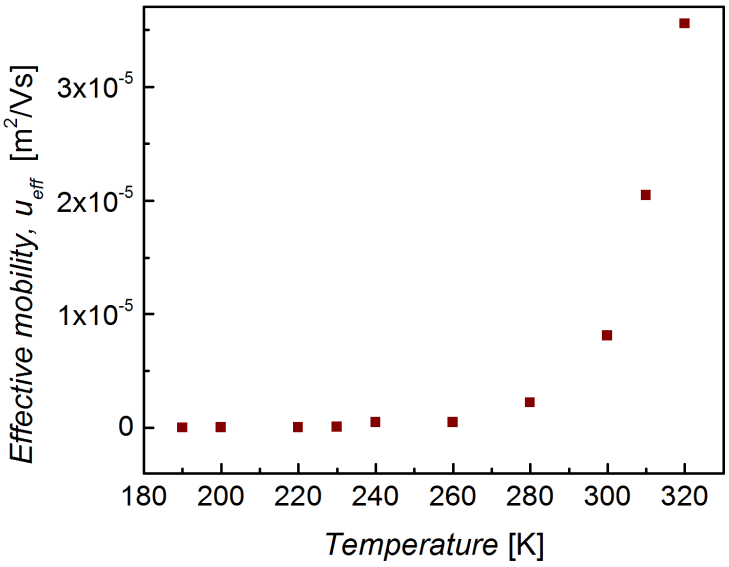

Figure 3.12: Variation of the effective mobility with temperature.

It is commonly believed that hopping within either the Gaussian or Exponential DOS is characterised by carriers being thermally activated by a given activation energy E_A [41,42], from the trapped sites to the transport energy level E_T. To extrapolate E_A, an Arrhenius plot of the forward current density at higher bias against 1000/T is plotted as shown in *Figure 3.13*. The value from the slope corresponds to 126 meV. This activation energy is comparable to the activation energy (125 meV) obtained for the same material in a FET device [43].

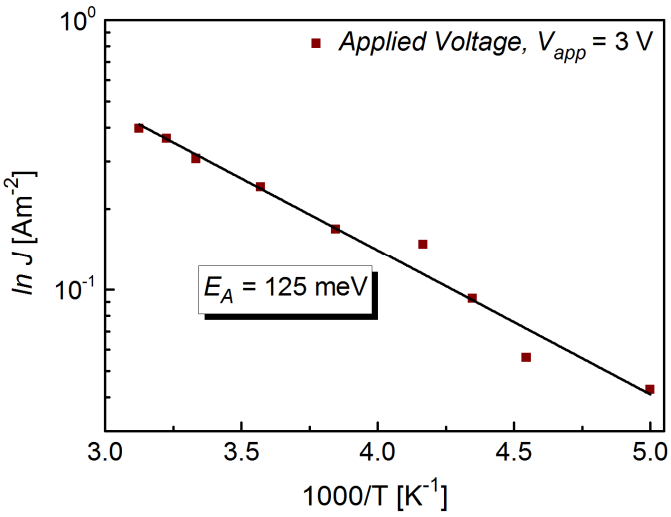

Figure 3.13: Arrhenius plot of the forward current density against 1000/T for PBTTT-C16. An activation energy of 126 meV is extrapolated from the slope.

Furthermore, the ideality factor η is also extrapolated from the exponential region of the forward current density as described in *section 3.3.1*. From *Figure 3. 14*, it follows that η increases with decrease in temperature, implying that the interface of the Schottky contact and the semiconductor is altered with varying temperature. Assuming the DOS remains unchanged with temperature, the temperature-dependent carrier distribution would decrease below E_F with the decrease in temperature. Carriers would initially fill up higher energy levels, and then proceed to fill the remaining lower energy levels. It is likely that the broadening and narrowing of the carrier distribution function with variation in temperature in conjunction with the irregular distances seen by carriers approaching the metal interface may very well influence the potential distribution at the interface. Thereby, carriers may take alternative routes to cross into the metal contact resulting in a similar situation as having lateral barrier inhomogeneity and consequently result in variation of the η with temperature. Moreover, as charge transport of carriers into the metal is temperature dependent, carriers at lower temperatures are more likely to take the route with lower energy corresponding to the large η observed at lower temperature.

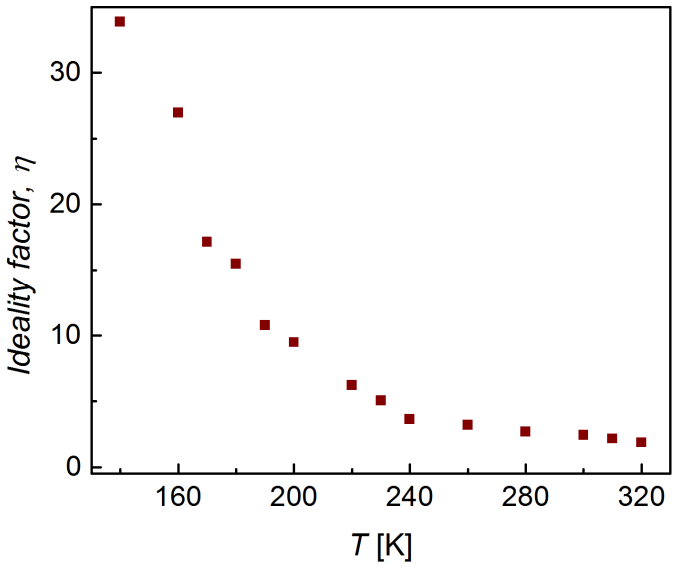

Figure 3. 14: Variation of the ideality factor with temperature for PBTTT-C16 Schottky diode.

3.4 IDT-BT SCHOTTKY DIODE

3.4.1 CURRENT DENSITY-VOLTAGE CHARACTERISTICS OF IDTBT-C16 SCHOTTKY DIODE

Similar to the previous section, the current-voltage measurements of IDTBT-C16 Schottky diode are also characterised as shown in *Figure 3.15*. The diode yields a rectification ratio of approximately 2.2×10^4. The value of the forward current density is about one order of magnitude lower than the PBTTT-C16 diode discussed in *section 3.3.1*. Such a variation is thought to be due to the differences in potential barriers, associated with the energy offset between the work function of the gold contact (−4.9 eV) and the HOMO level of PBTTT-C16 (−5.1 eV) and IDTBT-C16 (−5.4 eV) [11] respectively. In addition, the large turn-on voltage of −1 V observed in the latter device, could be attributed to the large built-in potential between the work function of the Schottky contact (−4.3 eV) and the HOMO of the IDTBT-C16, which corresponds to a theoretical value of 1.1 V. The reverse current density of the latter is also relatively lower in comparison to PBTTT-C16, possibly due to the higher level of dopants retained in the PBTTT-C16 film. Moreover, due to its lower lying HOMO level, IDTBT-C16 is more electrochemically stable to oxidative doping effects thereby resulting in lower values for the reverse current density.

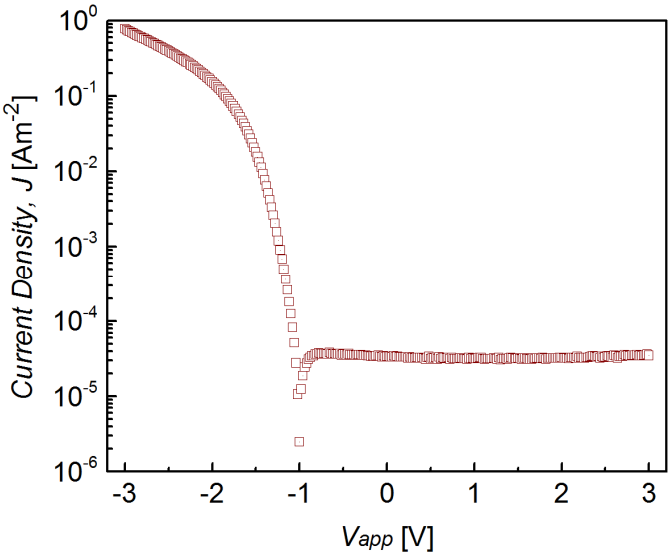

Figure 3.15: Semi-logarithmic plot of current density-voltage characteristics of IDTBT-C16 Schottky diode. The voltage is applied to the Schottky contact while the Ohmic contact is grounded.

The values of T_0 and subsequently η are extrapolated from the slope of the exponential region of the forward characteristics and found to be approximately 343 K and 1.14 respectively. The low value of η suggests that the interface of the metal and semiconductor has fewer traps. The double logarithmic plot of the forward characteristics is used in order to ascertain the nature of the conduction mechanism in this material. A value of 2.28 is obtained from the slope of the plot, indicative of SCLC mechanism. Moreover, the material parameter, *m*, is also obtained from the slope corresponding to a value of 0.28. Using the relation given by *equations 2. 25* and *2. 16*, values of T_C and the corresponding *MNE* are found to be approximately 383 K and 33 meV respectively. The aforementioned values are in agreement with both DFT calculations and optical absorption measurements made using photo-thermal deflection spectroscopy of the same film when in a disordered/amorphous state [19]. Moreover, the lower value of T_C in comparison to the PBTTT-C16 polymer indicates that the polymer has a lower degree of energetic disorder in spite lacking long-range order. The low energetic disorder is reportedly due to the resilience/rigidity of the polymer backbone to side-chain disorder [19]. Interestingly enough, the ideality factor obtained for the IDTBT-C16 polymer (1.14) is also lower than the PBTTT-C16 polymer (2.3). It was mentioned previously in *section 3.3* that the ideality factor in organic semiconductors has been suggested to be directly correlated to the degree of energetic disorder as indicated using the relation given by

equation 3. 2, which as we have observed in this section, the IDTBT-C16 polymer has a lower T_C value (523.6 K) than PBTTT-C16 polymer resulting in a lower ideality factor value as well.

With the application of a reverse bias, the current density is found to essentially remain the same, implying that the Schottky barrier is practically unchanged. To assess the aforementioned statement, the semi-logarithmic plot of J_R versus $V_R^{¼}$ is drawn and yields a poor line fitting to the data as demonstrated in *Figure 3.16*.

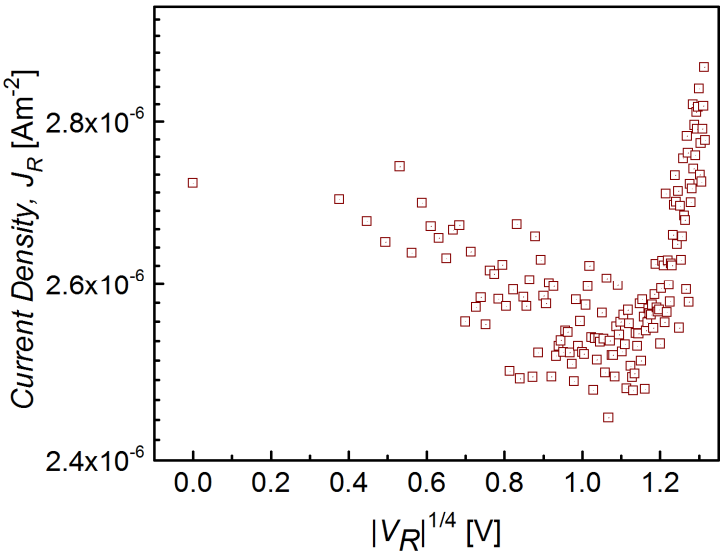

Figure 3.16: Reverse current density J_R against $|V_R|^{¼}$ of IDTBT-C16 Schottky diode.

The acceptor density N_A extracted from the slope at voltage values greater than 1.1 V is 3.6 × 10^{18} m^{-3}, corresponding to a depletion width W of 18.0 µm that surpasses the film thickness (1.2 µm). This abnormality together with the limited fitting of the plot seems to question the applicability of the Schottky theory to this diode. Some authors have made similar observations using vertical diodes made from a single rubrene crystal [44] and pentacene [45] respectively. They argued that based on the low values obtained for the acceptor density (similar to the ones obtained in this work), the device lacks an expanding depletion layer. Given that the film is already fully depleted at zero bias and given that the reverse current characteristics are independent of voltage bias, the diodes should therefore instead be characterised as pure capacitors rather than Schottky diodes.

On the other hand, the constant reverse current density could also be due to the occurrence of traps within the semiconductor, which would result in pinning of the quasi Fermi level [46,47]. In such a case, the application of the reverse bias would force the release of holes

from the trap states. In so doing, the Schottky barrier lowering effect is limited and as such, a relatively constant current density is produced across the barrier. To get a better understanding of the nature of the device i.e. manifestation of traps or lack thereof, a temperature study is also carried out on the current density voltage measurements of the polymer as outlined in the next section.

3.4.2 TEMPERATURE DEPENDENCE OF IDTBT-C16 SCHOTTKY DIODE

Figure 3. 17 shows the current-voltage characteristics of the IDTBT-C16 Schottky diode measured from 150 K to 300 K. The rectification ratios obtained increases proportionally from 3.6 to 2.2×10^4 with increasing temperature owing to the steady increase of the forward current density with increasing temperature. The forward current density increases by four orders of magnitude from 150 K to 300 K, because of carriers having a higher thermal energy to hop from occupied sites to unoccupied ones essentially increasing the effective mobility of the carriers and consequently the forward current density. The reverse current density, on the other hand, did not have a specific trend with variation in temperature; it instead remained fairly constant with final values ranging between 5.62×10^{-7} A/m^2 and 2.78×10^{-6} A/m^2 at an applied bias of 3 V for the given temperature range. In addition, the acceptor density could not be obtained from the reverse characteristics, particularly for reverse current density values below 300 K, as they do not follow the ¼ power law for Schottky theory.

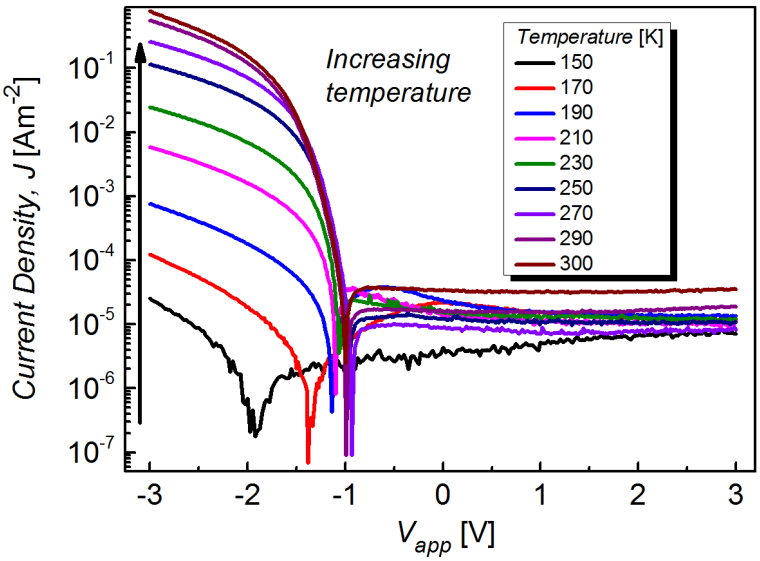

Figure 3. 17: Semi-logarithmic plot of the current density-voltage characteristics of IDTBT-C16 Schottky diode measured for a given temperature range between 150 K and 300 K.

It is also observed that with the decrease in temperature, the turn-on voltage shifts towards more negative voltage values as in *Figure 3. 18*. The reason for the observed change can be associated with dipoles [48] occurring at the interface of the metal and semiconductor as well as external trap states brought on during film deposition and/or diffusion of the metal contact into the organic layer during thermal evaporation [49]. On lowering the temperature of the device, the interface dipoles are predisposed to being frozen thereby resulting in the trapping of carriers. In addition, the surface states that could be brought on during thermal evaporation result in a space charge layer/interfacial layer at the interface. Due to the occurrence of the aforementioned carriers, the majority of the external bias is primarily used to neutralize the trapped charges to turn on the device, thereby explaining the observed voltage offset.

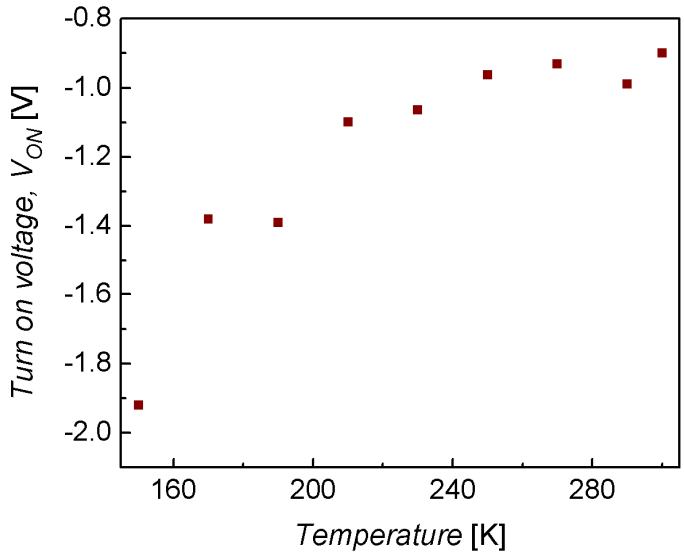

Figure 3. 18: Variation of the turn-on voltage, V_{ON} with temperature for IDBT-C16 Schottky diode.

The ideality factor in the IDTBT-C16 diode also increases with decreasing temperature as demonstrated in *Figure 3. 19*, much like the PBTTT-C16 diode studied in the previous section, owing to inhomogeneity at the metal/semiconductor interface. The IDTBT-C16 diode however shows a lower temperature variation of the ideality factor values perhaps because the width of the energetic distribution of carriers as well as the DOS is smaller in comparison thereby reducing the amount of alternative routes that carriers may choose to take to cross over the potential barrier. In addition, the kink in the *J-V* characteristics of the PBTTT-C16 diode increases the number of potential barriers seen by carriers thereby affecting the ideality factor values too.

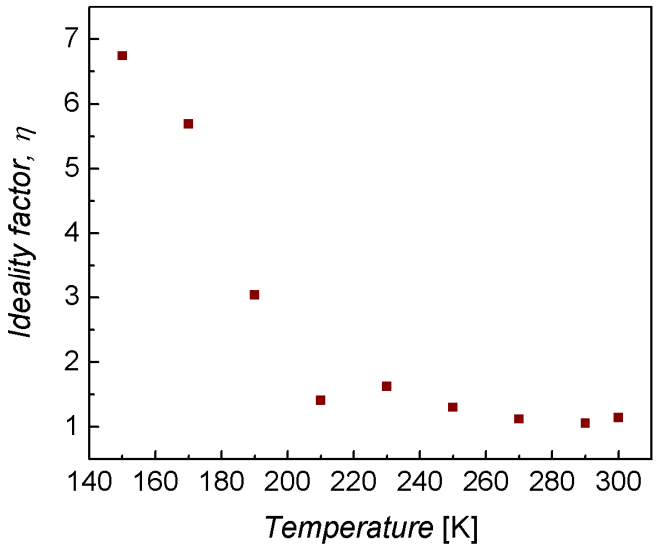

Figure 3. 19: Variation of the ideality factor with temperature for IDTBT-C16 Schottky diode.

The material parameter *m* and subsequently, T_C and *MNE* are extrapolated from the forward current density at higher applied voltages, specifically from the slope of the logarithmic plot of the current density versus the bulk voltage using the relation given by *equation 2. 39* in chapter 2. Based on the extrapolation, the *MNE* is found to decrease with temperature for a limited temperature range as in *Figure 3. 20*. As mentioned in chapter 2, the *MNE* is widely assumed to be related to the width of the DOS, σ, or the characteristic temperature associated with the DOS, T_C depending on the choice of the shape of the DOS. The same assumption is made in the organic models used to analyse the data in this work. Physically, it is hard to envision why T_C and subsequently *MNE would* vary with changes in temperature. Subsequently, the perceived variation in *MNE in* this work could be attributed to the modification of the Au/IDTBT-C16 interface as the temperature varies. Although the Au back contact is modified to facilitate better injection of carriers into the polymer layer, the offset in the energy levels of the two materials (0.5 eV at zero bias) with variation in temperature results in an increase in the barrier height as well as widening of the space charge region associated with the contact.

The space charge limited current in this case is thereby dictated by the properties of the Au/IDTBT-C16 interface. The latter phenomena subsequently affects the width of the neutral region as well thereby affecting the voltage dependency of the space charge limited current as evidenced by the different values obtained from the slope leading to a variation of T_C and *MNE* . The organic model adopted in this work does not account for the changing

interface of the back metal and active layer, which could greatly impact the boundary conditions of the SCLC and hence the *MNE* dependency with temperature.

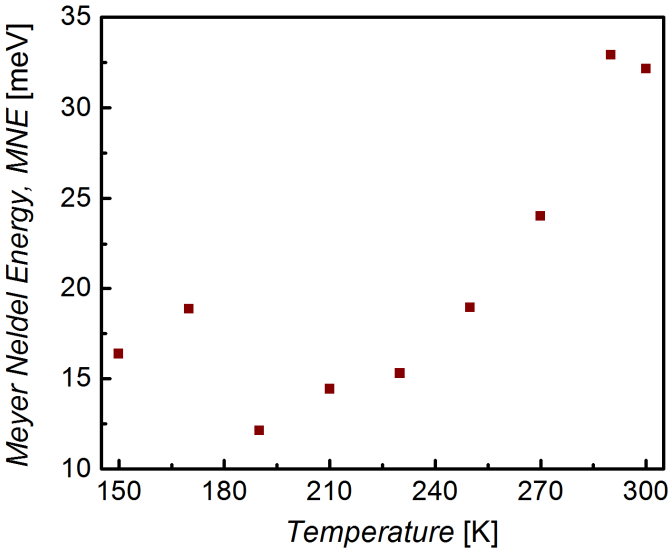

Figure 3. 20: Variation of the Meyer Neldel Energy (MNE) extracted from the slope of the forward current density versus the bulk voltage taken at higher voltage values with temperature. (Slopes of greater than 2 are obtained corresponding to the presence of space charge effects with changes in temperature).

Similar to *section 3.3.2*, the activation energy E_A is extrapolated from the Arrhenius plot of the forward current density versus 1000/*T*, as shown in *Figure 3.21*. The value of E_A extracted from the slope is found to be approximately 339 meV. In comparison however, a much lower E_A of 61 meV [50] has been reported, measured using OTFTs, using the same material. Possible reason for such large variation could be attributed to the morphological structure of the polymer film, as well as the configuration of the device from which the measurement is taken. In their work, Zhang *et al.*, [50] indicate that the reason for the low activation energy and consequently high mobility obtained from IDTBT-C16 is attributed to the charge transport, which is predominantly quasi one-dimensional (1D), where charge carriers move along the polymer chain backbone i.e. intramolecular hopping, with minimal intermolecular hopping (hopping between adjacent chains). The transport in IDTBT-C16 is thought to be particularly favourable to intramolecular hopping in lateral-type devices such as OTFTs due to its rigid, disorder/torsion free backbone and its planar conformation. In other words, the few traps occurring along the polymer chain of the IDTBT-C16 film favours the

horizontal movement of charge carriers in devices whose transport is dictated by lateral field thereby resulting in lower activation energy as observed by Zhang *et al*. [50].

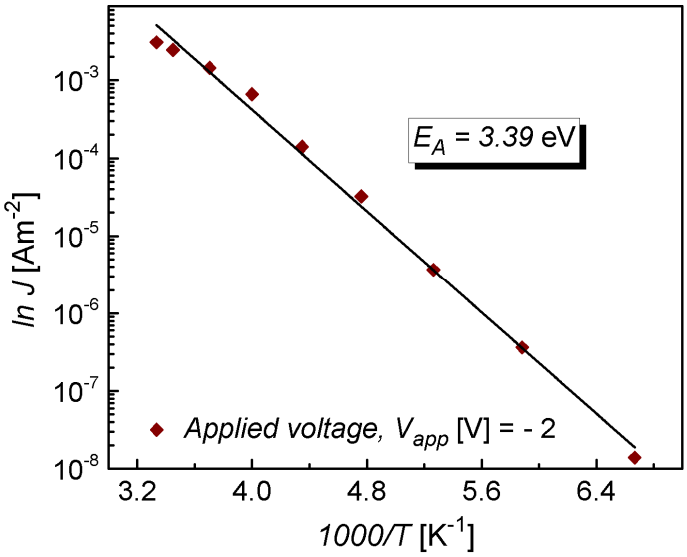

Figure 3.21: Arrhenius temperature plot of the forward current density against 1000/T of IDTBT-C16 Schottky diode. The activation energy is extrapolated from the slope and found to be 3.39 eV as shown inset.

On the other hand, the charge transport study in this work is carried out using a vertical diode whereby the vertical field dictates the operation of the device. In such a case, it is more likely that the transfer rate occurring between adjacent chains limits the charge transport rather than intramolecular hopping. It is well known that the molecular ordering of IDTBT-C16 is poor, displaying a face-on backbone orientation and huge π stacking distances (4.1 Å) [12]; ideally, characteristics that do not favour bulk charge transport. It is therefore argued in this work that the high activation energy is associated with the poor hole coupling between adjacent chains, owing to the large π-stacking distance. In essence, because of the large distances occurring between polymer chains, carriers are virtually immobile; thereby they are essentially trapped and would require a larger activation energy to facilitate hopping from one chain to another (intermolecular hopping). It has also been shown in literature that charge transport can be enhanced by improving intermolecular hopping through reduction of the π-stacking distance [51,52], particularly in polythiophenes, further corroborating the above argument. Moreover, the latter holds true when comparing the lower activation energy (126 meV) obtained for the PBTTT-C16 polymer studied in *section 3.3.2.* In comparison to IDTBT-C16, the PBTTT-C16 polymer has better hole coupling interactions due to its well-ordered domains, closer π-packing

distance and interdigitating of its side chains with adjacent chains [51], characteristics synonymous with efficient 2D transport i.e. along the polymer chain and between adjacent polymer chains. Interestingly, the activation energy obtained from PBTTT-C16 OTFTs, coincides with the value obtained from vertical PBTTT-C16 Schottky diodes; perhaps suggesting that intermolecular and intramolecular hopping may play an equal role in charge transport of polymers having the 2D structural motif synonymous with this material or that the motif results in a nearly equal number of traps in field pathways that are perpendicular and/or parallel to the direction of applied field.

The results obtained in this section give a new insight into the role of the structural properties of conjugated polymers in charge transport. The morphological structure of PBTTT-C16 favours 2D charge transport particularly useful in vertical-type devices. In such cases, charge transport is limited by the intermolecular hopping rate, which is characterised by the π-π stacking, accompanied with occasional hopping along the polymer chain. Conversely, the poorly ordered structure of the IDTBT-C16 polymer, specifically the π-π packing, does not favour charge transport in vertical-type devices, nonetheless, its rigid polymer backbone favours charge transport in lateral type devices as already shown in literature. An important implication of these findings is that future design strategies may not necessarily focus on improving long range order to obtain high mobility values but would instead make polymers tailored to specific device topologies having either/both a high charge carrier mobility as well as a lack of long-range order if need be. In addition, in applications where 2D charge transport is the dominant transport mechanism, a structural trade-off would be needed when designing polymers with regards to intermolecular and intramolecular hopping rate mechanisms.

3.5 CONCLUSIONS

A temperature dependency of the current-voltage characteristics of vertical Schottky diodes made using poly PBTTT-C16 and IDTBT-C16 polymers are carried out to characterise the charge transport mechanisms present in these films.

At room temperature, the forward current density of both devices increases exponentially with applied forward bias, due to an exponential increase in carrier concentration. The forward current density of the PBTTT-C16 diode is found to be one order

of magnitude higher than the IDTBT-C16 diode, due to its smaller potential barrier with the gold (Ohmic) contact (i.e. 0.2 eV for PBTTT-C16 diode and 0.5 eV for IDTBT-C16 diode), thus enabling easier injection of carriers. Using the forward characteristics and the associated Schottky diode model, the following parameters i.e. the characteristic temperature associated with the distribution of carriers T_0, characteristic temperature associated with the intrinsic DOS T_C and *MNE* of the PBTTT-C16 are found to be approximately 707.5 K, 523.6 K and 45 meV. Conversely, for IDTBT-C16, the extracted values are found to be 343.6 K, 382.7 K and 33 meV respectively. The lower values of T_C and *MNE* of the IDTBT-C16 indicate that the polymer has a lower degree of energetic disorder in spite lacking long-range order. The lower degree of energetic disorder also results in a lower ideality factor η of 1.1 in comparison to the former, which has η of 2.3.

Furthermore, PBTTT-C16 Schottky diode has higher reverse current density values, which is attributed to the presence of residual dopant ions in the film as well as its high HOMO energy level of −5.1 eV, which makes it more predisposed to oxygen doping effects. The current density of the same device also increases with application of reverse bias whilst for the IDTBT-C16 diode; it remained constant probably due to Fermi-level pinning due to the presence of trap-states. The acceptor density N_A, obtained from the semi-logarithmic plot of J_R versus $V_R^{¼}$ of both materials are found to be approximately 3.59×10^{18} m^{-3} and 1.59×10^{22} m^{-3} respectively. The barrier height is obtained from the intercept of the plot of J_R versus $V_R^{¼}$ and is found to be 0.92 eV, which exceeds the theoretical barrier height by 0.12 eV. The difference in the value obtained is associated with the extraction of an erroneous value of the saturation current density, which is used in the calculation of the barrier height.

From temperature measurements of the current-voltage characteristics, it is observed that the reverse current density of the PBTTT-C16 Schottky diode increases steadily with temperature, however, for IDTBT-C16, no visible temperature dependency is observed, in effect making it hard to assess the acceptor density profile as well as the effective mobility. For the PBTTT-C16 device, the values of N_A are found to increase slightly between 5.87×10^{21} m^{-3} to 1.81×10^{22} m^{-3} as the temperature increases from 190 K to 320 K.

Additionally, the forward current density of both devices showed a steady increase with increase in temperature, because of carriers having a higher thermal energy to hop from occupied sites to unoccupied ones. For the IDTBT-C16 device, the turn-on voltage displayed

a noticeable temperature dependency whereby it shifted towards more negative values with fall in temperature. This effect is associated with the occurrence of trapped charges at the interface of the Schottky metal and the semiconductor. The *MNE* obtained from the forward current density of the device at higher applied bias showed an increase from 12 meV to 33 meV between a limited temperature range of 190 K to 290 K. This apparent observation is attributed to the modification of the Au/IDTBT-C16 interface with temperature, as well as a variation of the width of the neutral region with temperature. In addition, the ideality factor η increases from 1.14 to 6.74 as the temperature decreases from 300 K to 150 K. The effect is associated with the presence of a potential barrier at the interface whereby carriers opt to take alternative routes to cross over the metal/semiconductor interface. On the other hand, the PBTTT-C16 diode has a much larger temperature dependency on η, such that values of 33.9 to 1.9 are obtained within a temperature range from 140 K to 320 K. The kink in the *J-V* characteristics of the PBTTT-C16 diode increases the amount of potential barriers seen by carriers thereby greatly affecting the ideality factor. The larger values have also been shown to be due to having a larger degree of energetic disorder relative to the IDTBT-C16 diode.

Finally, the activation energy E_A of the two devices is extracted from the Arrhenius plots of the forward current density against 1000/*T*. For PBTTT-C16, the value of E_A is 126 meV, which is in agreement with those obtained from OTFT measurements, made with the same material. For IDTBT-C16 Schottky diode, a higher value of E_A of 339 meV is obtained, compared to the values obtained from OTFT measurements. Such larger values have been attributed to the poor polymer chain interaction of the material because of its large π-stacking distance. On the other hand, the PBTTT-C16 polymer has a lower E_A because of the interdigitating of its side chains with adjacent chains and its smaller π-packing distance thereby facilitating 2D transport along the polymer chain and between adjacent polymer chains. Future design strategies would therefore need to take into account the end-user application to create appropriate polymer motifs whilst retaining high charge carrier mobility values.

3.6 REFERENCES

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CHAPTER 4

Development and optimisation of a self-aligned gap process for organic lateral devices

An overview of the fabrication process in the development of a self-aligned gap (SAG) is initially discussed in this chapter. The SAG process is subsequently utilised in the fabrication of lateral devices including the organic Schottky diode and organic thin-film transistor (OTFT). Optimisation of the process is also discussed, with the aid of electrical studies of lateral PTAA Schottky diodes. Subsequently, using the optimised process, OTFTs are fabricated, and the electrical characteristics are fitted to the disordered model derived in chapter 2.

4.1 INTRODUCTION

The field of Organic Electronics has grown progressively over the decades from research on single devices such as Schottky diodes and thin-film transistors to functional blocks such as RFID tags and sensors. However, the performance of these circuits with respect to switching speeds, operation voltages and power consumption could be enhanced. The speed of operation of a circuit scales inversely with the square of the channel length and charge carrier mobility. Therefore, to enhance circuit performance from a switching speed perspective, the charge carrier mobility needs to be increases and the channel length reduced. Unlike inorganic semiconductors, the mobility term in organic semiconductors is not fixed i.e. it varies strongly with the carrier concentration, as discussed in chapter 2; therefore, it cannot be used as a scaling parameter for increasing the operational speed of a transistor. Alternatively, using materials with specific values of K and T_C, which result in higher effective mobility values, may be used instead as a scaling parameter.

Although scaling down the channel length of the transistor results in higher operational speeds, it would be more realistic to use slightly larger feature sizes in order to achieve desirable specifications within certain applications due to the low mobility values of organic semiconductors. In addition, most target applications of organic semiconductors are for use in large-scale area applications. Recent research groups are however opting to reduce the channel length by adopting vertical OTFT design topologies [1-3] whereby, akin to vertical diodes discussed in chapter 3, the channel length is defined by the thickness of the organic semiconductor layer unlike in lateral OTFTs and diodes where it is generally defined by the resolution of the photolithography process. These designs have better switching speeds and superior DC performance.

On the other hand, the switching speed of a transistor has a direct correlation to the frequency response and subsequently the power delay product of a circuit. The transition frequency, f_t, as shown in *equation 4. 1* is ordinarily used as a figure of merit for the frequency response of a circuit.

$$f_t = \frac{g_m}{2\pi(C_{GD}+C_{GS})} \qquad 4.1$$

where g_m is the transconductance of a transistor, C_{GD} is the gate-to-drain capacitance and C_{GS} is the gate-to-source capacitance.

From *equation 4. 1*, it follows therefore that a reduction in the Miller (overlap) capacitances as well as the minimisation of the crossover structures and active layer area, results in a better frequency response and hence faster switching speeds of a circuit. In this chapter, a self-aligned gap (SAG) process is introduced, which allows the minimisation of such parasitic capacitances. In addition to reducing the overlap capacitance, the versatility of the process allows the development of different lateral devices (i.e. Schottky diodes and thin-film transistors) on the same substrate and at the same time. The SAG process is firstly developed and subsequently optimised in the fabrication of lateral Schottky diodes as discussed in *section 4.2*. Having optimised the process, a scaling study is carried out using the lateral diode, with a low-mobility amorphous polymer, Polytriarylamine (PTAA), as the active layer. PTAA is used as the active layer in this initial study since it is more stable in ambient conditions and forms reasonably uniform films, thus making it a suitable material for performing scaling and limitation studies of conjugated and amorphous polymers for subsequent use in modelling of circuits [4-6]. Furthermore, due to its amorphous nature, there is no need for additional processing steps that could affect the semiconductor post-deposition; for instance, annealing to change the film structure and morphology as needed for the liquid-crystalline mesophase polymers such as PBTTT-C16 that is studied in chapter 3. Moreover, the effect of isolating the active region of the PTAA film, to reduce the area of the active layer, is also explored.

Using the optimised SAG process, organic thin-film transistors (OTFTs) are also developed in *section 4.3*, with PBTTT-C16, as the active layer. This polymer is chosen as it has a higher mobility and hence appropriate for use in subsequent circuit studies, as described in chapter 5. From the electrical characteristics of the PBTTT-C16 OTFTs, values of key material parameters such as *m* and *K* are extracted, and subsequently utilised in fitting the experimental data to the disordered equations, developed in chapter 2.

4.2 THE STUDY OF A SELF-ALIGNED PROCESS USING SCHOTTKY DIODES

4.2.1 FABRICATION METHODOLOGY

The structure of the lateral Schottky diode used in the development and optimisation of the self-aligned gap (SAG) process is as shown in *Figure 4. 1*. It consists of Ohmic and Schottky contacts made of aluminium (Al) and gold (Au) contacts respectively and PTAA as the active layer.

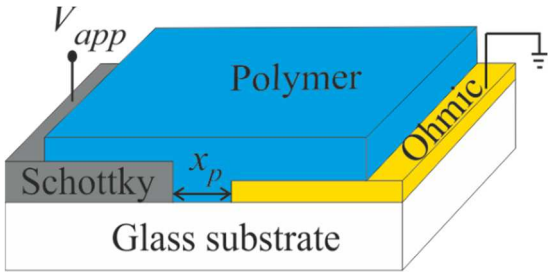

Figure 4. 1: Structure of the lateral Schottky diode with aluminium and gold as the Schottky and Ohmic contacts respectively. The electric field is intensified with smaller inter-electrode spacing defined by the gap, x_p. The width of the Ohmic and Schottky contact is 1mm and the area of the patterned active layer is estimated to be around 0.3μm^2 (i.e. 300 μm by 1 mm polymer coverage).

The steps involved in the SAG fabrication process of the lateral diodes are as described below. The summary of the process steps is also shown in *Figure 4. 2*.

1. *Substrate cleaning*

   - All the devices are fabricated on Corning glass slides. To remove contaminants such as dusts and oils, the slides are cleaned in an ultrasonic bath containing industrial cleaning agent, Decon 90, obtained from Fisher Scientific Ltd, UK. Samples are then rinsed using deionised water and dried using a nitrogen gun. The aforementioned process is then repeated sequentially using acetone and propanol solvents that are both purchased from Fisher Scientific Ltd, UK. The samples are left to dry in a hot box for about 30 minutes and subsequently cleaned using a UV ozone cleaner, to remove any residual organic contaminants.

2. *Aluminium (Schottky contact) patterning and gap formation*:

- A 200 nm thick Al layer is thermally evaporated onto the pre-cleaned glass substrates at a rate of 4 Å/s at a pressure of 1.96×10^{-7} mTorr, as shown in *Figure 4. 2 (a)*.
- A lift-off resist layer (LOR 3A), which is obtained from A-Gas Electronic Materials, UK, is spun onto the aluminium film, at 3000 revolutions per minute (rpm) for 45 seconds, followed by soft baking of the samples on a hotplate. The soft bake parameters, specifically the baking time and temperature, are varied appropriately, to obtain different undercut sizes of the LOR layer. Samples are then allowed to cool on a glass slab prior to commencing the next step.
- A positive image resist layer (HPR 504), which is procured from FUJIFILM Electronic Materials (Europe) N.V., Belgium, is spun on the LOR 3A coated samples at 3000 rpm for 45 seconds, followed by soft baking of the samples at 110 °C for 90 seconds on a hotplate.
- The resist-coated samples are then exposed to ultra-violet (UV) light through a chromium-coated mask containing the aluminium layer pattern/layout, as shown in *Figure 4. 2 (b)*. The layout of the mask used to make the lateral devices is as shown in *Figure 4. 3*.
- The exposed samples are then developed in HPRD 429 developer solution for 45 seconds. The developer is bought from FUJIFILM Electronic Materials (Europe) N.V., Belgium. The samples are then rinsed in deionised water and dried with a nitrogen gun followed by hard baking of the imaging resist at 125 °C for 300 seconds on a hot plate, as demonstrated in *Figure 4. 2 (c)*. The latter step is essential to create a larger difference of the dissolution rates of the imaging resist and the LOR resist. Omission of this step results in improper formation of an undercut, which subsequently leads to short circuits. The samples are then developed again for 60 seconds, followed by a thorough rinse off and drying using a nitrogen gun.
- The samples are hard baked at 140 °C for 120 seconds to harden the imaging resist, to make it resilient to aluminium etchant, which is used to define the resultant Schottky contact as shown in *Figure 4. 2 (d)*. The above-mentioned etchant is ordered from MicroChemicals GmbH, Germany.

- The next step involved the thermal evaporation of a 5 nm chromium layer at a rate of 1 Å/s, followed by thermal evaporation of a 50 nm gold layer at a rate of 3 Å/s as shown in *Figure 4. 2 (e)*.
- After evaporation, the samples are immersed in a beaker of 80 °C heated Microstrip 2001 solution (photoresist remover), in order to lift-off the resist resulting in the formation of a gap between the Al and Au contacts as in *Figure 4. 2 (f)*. The photoresist remover solution is acquired from FUJIFILM Electronic Materials (Europe) N.V., Belgium. The samples are then rinsed thoroughly in deionised water, dried with a nitrogen gun and cleaned using UV-radiation remove residual resist contaminants.

3. Gold (Ohmic contact) patterning:

- A positive image resist (HPR 504) is spun on the glass samples at 3000 rpm for 45 seconds followed by soft baking of the samples at 110 °C for 90 seconds on a hotplate.
- The resist-coated samples are exposed to UV light using a mask aligner followed by developing in HPRD 429 developer for 45 seconds as detailed in *Figure 4. 2 (g)* and *Figure 4. 2 (h)* respectively. The samples are rinsed in deionised water and dried with a nitrogen gun then the imaging resist is hard baked at 140 °C for 120 seconds on a hot plate. The next step involves the wet chemical etching of the chromium and gold layers respectively using gold and chromium etchant obtained from MicroChemicals GmbH, Germany and Sigma-Aldrich Company Ltd, UK, respectively. Once etched, the Ohmic contact is thereby defined as outlined in *Figure 4. 2 (i)*. The photoresist is successively removed as detailed in the last part of *section 2* and demonstrated in *Figure 4. 2 (j)*.

4. Polymer deposition as in Figure 4. 2 (k).

Having defined the Ohmic and Schottky contacts, the polymer is deposited, following the steps below.

- Unpatterned - represents a polymer layer that is not isolated using photolithography patterning.

  A PTAA solution (1% wt. of toluene) is spin coated onto the samples at various spin-speeds (500 rpm to 1500 rpm) depending on the desired film thickness followed by thermal annealing at 100 °C for 600 seconds. These samples are left

under vacuum overnight, prior to electrical characterisation. This is done to reduce the oxygen doping effects experienced during processing and is believed to result in more stable electrical characteristics from the devices. The PTAA powder and toluene chemical is obtained from Sigma-Aldrich Company Ltd, UK and VWR International Ltd, UK respectively. PTAA polymer is used as is it was purchased i.e. no further fractionation was carried out.

- Patterned - represents a polymer layer that has been isolated using photolithography patterning.

  For the patterned samples, the polymer is deposited as described in the last section, followed by spinning of OSCoR 4000 negative photoresist solution at 1000 rpm for 60 seconds. A post-application bake of the samples is then carried out at 105 °C for 90 seconds on a hotplate.

  The resist-coated samples are exposed to UV light using a mask aligner followed by a post exposure bake at 105 °C for 90 seconds on a hotplate. Samples are subsequently developed in Developer 103 solution for 180 seconds followed by a wet chemical etching of the polymer in 1, 2, 3, 4-tetrahydronaphthalene (tetralin) solution. Lastly, the samples are placed in Stripper 700 solution for 300 seconds to remove the photoresist, and left overnight under vacuum prior to electrical characterisation. The chemicals used to pattern the semiconductor layer i.e. OSCoR 4000 negative photoresist, Developer 103 solution and Stripper 700 solution, were collectively obtained from Orthogonal Incorporated, USA whereas tetralin was purchased from VWR International Ltd, UK.

All fabrication and characterisation of the Schottky diodes (i.e. optical and electrical), are carried out in clean ambient conditions and in the presence of yellow light. A HP4155B semiconductor parameter analyser and an E4980A precision LCR meter are utilised for the current-voltage (I-V) and capacitance-voltage (C-V) measurements respectively. The measurements of the gap sizes are obtained using a Veeco CP-II Atomic Force Microscope (AFM), whereas the thickness mapping and uniformity is characterised using an M-2000 Ellipsometer.

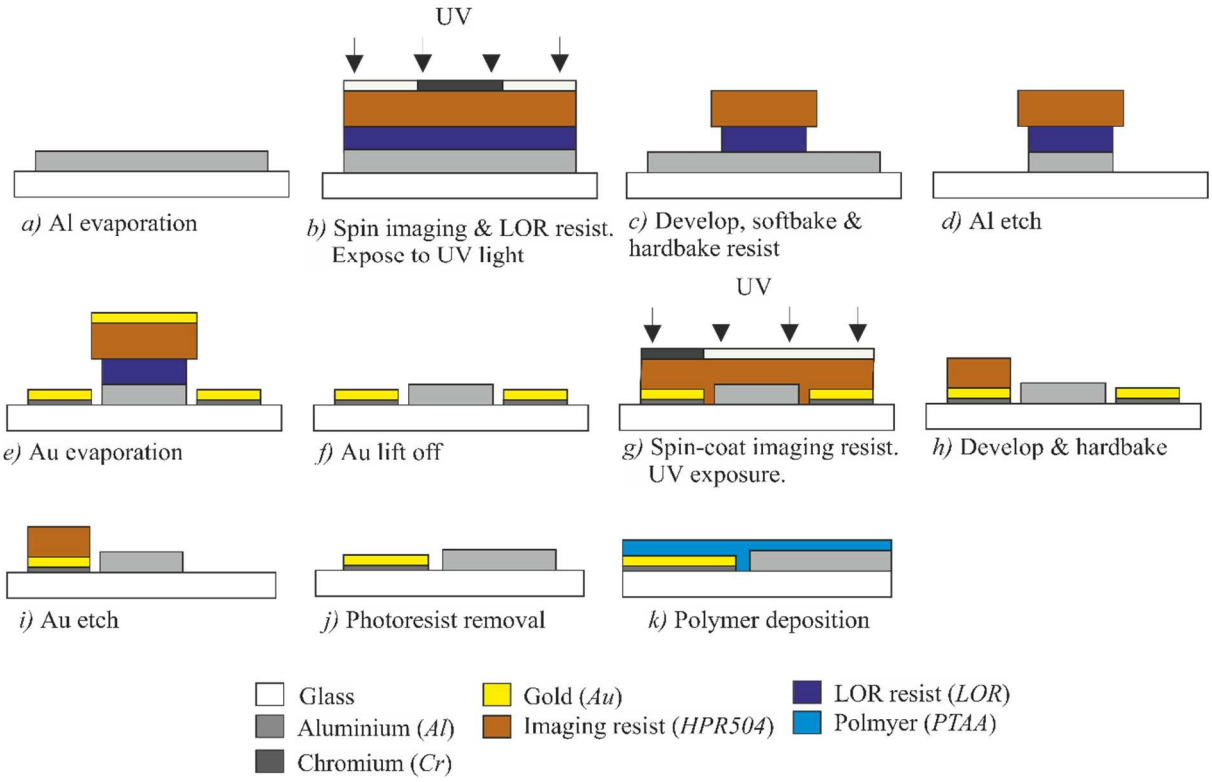

Figure 4. 2: Overview of the fabrication of a lateral Schottky diode made using a SAG fabrication processes.

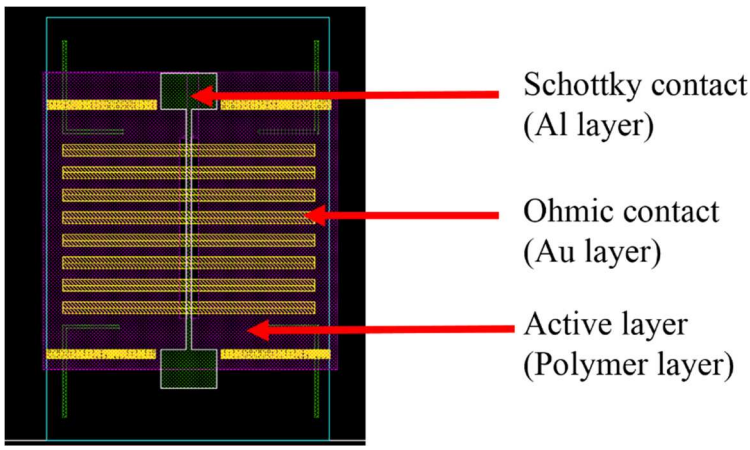

Figure 4. 3: Mask layout design of the lateral Schottky diode used in the characterisation of the SAG fabrication processes.

4.2.2 CHARACTERISATION OF THE UNDERCUT

As highlighted earlier, the soft bake process facilitates a more accurate and reproducible control of the undercut, when using a bilayer photoresist lift-off process. To obtain different gap sizes, a parametric study of the soft bake processes i.e. the soft bake temperature and time is carried out. There are ten samples fabricated in total. With the first five samples, the soft bake temperature is varied from 150 °C to 190 °C, with a constant soft bake time of 225 seconds, whereas with the remaining five samples, the soft bake time is varied from 120 seconds to 600 seconds with a constant soft bake temperature of 170 °C. The resultant undercuts (gap sizes) are measured using an Atomic Force Microscope (AFM) in non-contact mode to prevent any damages on the surfaces, as they are later used in the making and characterisation of lateral Schottky diodes.

From the measurements, it is evident that the dissolution rate, hence the undercut size, decreases with an increase in both the soft bake temperature and time, as illustrated in *Figure 4. 4* and *Figure 4. 5* . It is well-known that soft-baking of a photoresist is characterised mainly by, the evaporation and diffusion of the photoresist solvent, and densification of the polymer resist [7]. The rate at which the solvent diffuses and evaporates into the atmosphere is inversely proportional to the soft bake parameters, such that low soft bake times and temperatures result in more retention of residual solvents in the resist film [8]. The higher solvent concentration left in the film leads to a larger free volume of the solvent [9,10], which facilitates faster diffusion of the developer solution into the resist film, and in so doing creates a higher dissolution rate [7,11-13]. On the other hand, high soft bake times and temperatures result in rapid loss of the photoresist solvent thereby reducing the free volume of the solvent. This, coupled with annealing of the photoresist [7], enhances the polymer matrix within the film such that with the increased polymer-polymer packing density, the mobility of penetrant molecules gets reduced thereby resulting in a lower dissolution rate and hence smaller gap sizes are formed.

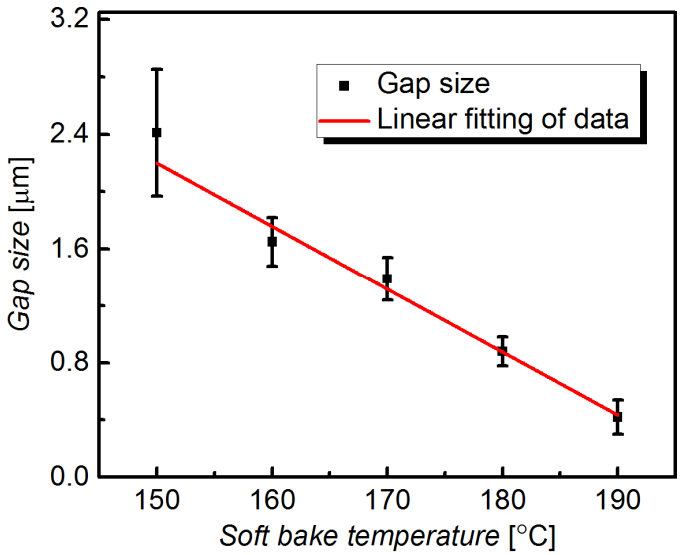

Figure 4. 4: Variation of the gap size with respect to the soft bake temperature for a soft bake time of 225 seconds.

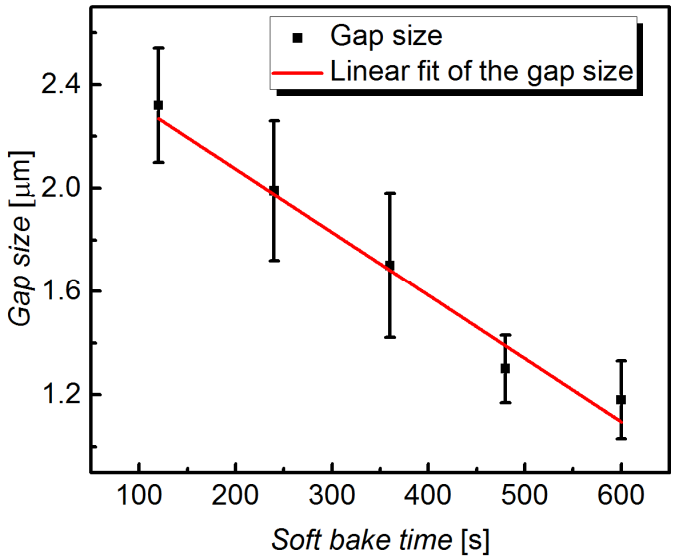

Figure 4. 5: Variation of the gap size with respect to the soft bake time for a soft bake temperature of 170 °C.

The experimental data is collected from 16 devices per sample, for each soft bake temperature and time, and is collated to give the data as represented by the standard deviation (SD) error bars in *Figure 4. 4* and *Figure 4. 5*. On comparison of the slopes for both plots, it is evident that the undercut rate is more dependent on the soft bake temperature than the soft bake time. However, the soft bake time is found to yield more variation in the gap sizes, compared to the soft bake temperature as illustrated by the error bars within the plots. The variation of the gap sizes across different samples from the same processing batch (i.e. processed at the same

time) is believed to be due to uneven distribution of light intensity/exposure dose across the substrate during photolithography patterning as well as non-uniform thickness spread of the photoresist film on the substrates. Moreover, although all the samples are processed together and at the same time, involuntary factors such as inadequate/excess agitation while developing of the samples and the varying reaction times when removing samples from the developer solution may influence the spread in variations across samples.

One notable difference in the two figures is the different range of gap sizes obtained for samples having the same soft bake temperature and soft bake time but processed at different times i.e. different processing batches. In this case for instance the two samples having the same soft bake time (225 seconds) and temperature (170 °C) notably have a different range of gap sizes obtained. The reason for the differences in the gap sizes obtained for the two plots is believed to be as a result of differences in the rate of the solvent evolution in the film during the soft baking process. This difference is brought on by different transfer rates occurring at the interface of the resist film and air [14,15]. During the soft bake process, the bottom of the resist film will have nearly the same temperature as the hot plate whilst the top of the film will presumably have a lower temperature that is dependent on the convective flow pattern and the surrounding clean room air conditions i.e humidity content, air flow and exhaust flow. This temperature gradient in the film results in a solvent vapour pressure gradient as well, which sequentially brings on a diffusion coefficient gradient during the development stage of the film. The latter parameter affects the content of the solvent in the film, which as was previously mentioned, influences the rate at which the resist gets developed and thereby, by default, the gap size as well.

In short, if films have different temperature gradients, in spite having the same film thickness, the same soft bake time and the same soft bake temperature, then the evaporation rate of the film and hence the gap sizes obtained, will have some variation. Therefore, in future, one needs to take proper control of the exhaust and airflow pattern in order to achieve repeatable and reproducible results. One possible way to reduce such differencs would be to perhaps cover the samples with a petri dish while soft baking the resist film. In addition to this, placing the soft baked samples on a hot plate having significantly lower temperature values whilst covering it with a petri dish in order to control the cooling down rate of the photoresist post baking would be adviseable.

The obtained plots provide a blueprint for future tailoring of subsequent fabrication processes to obtain specific gap sizes. For instance, in order to obtain smaller gaps of 50 nm, a soft bake temperature and time of 190 °C and 300 seconds would be required. *Figure 4. 6* below shows a sample of the AFM images of the different gap sizes obtained by varying the soft bake temperature.

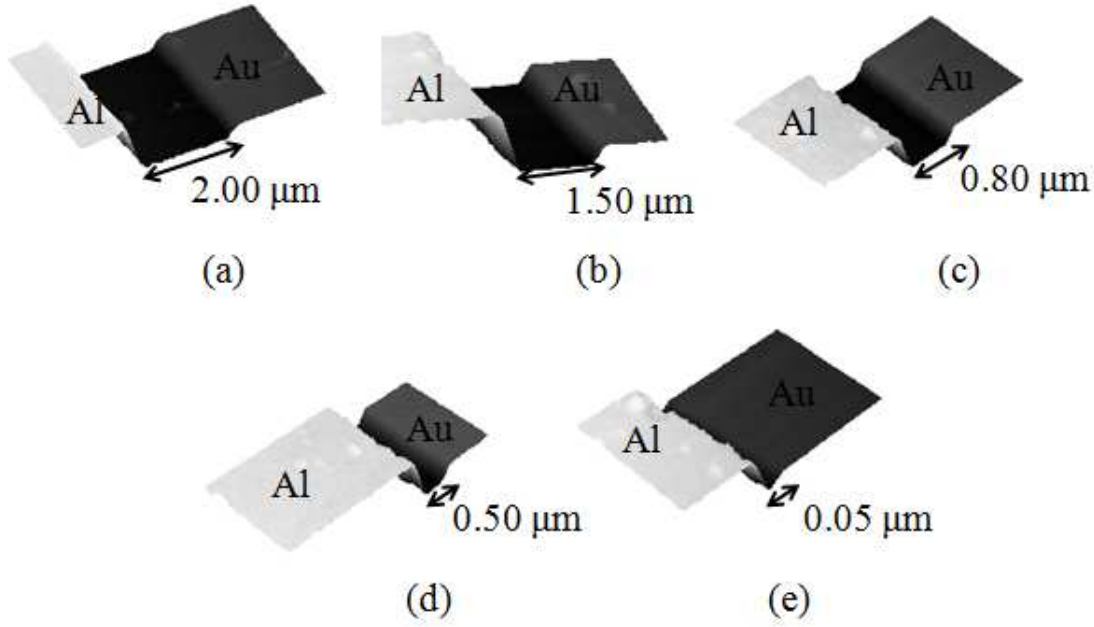

Figure 4. 6: AFM images of the different gap sizes obtained by varying the soft bake temperature from 150 °C to 190 °C. The inter-electrode spacing between the Ohmic (Au) and Schottky (Al) contacts are as indicated by the arrow.

4.2.3 CURRENT-VOLTAGE CHARACTERISTICS OF THE PTAA SCHOTTKY DIODES

The current density-voltage characteristics of the aforementioned gap sizes are also analysed using a semiconductor parameter analyser and are plotted in *Figure 4. 7.*

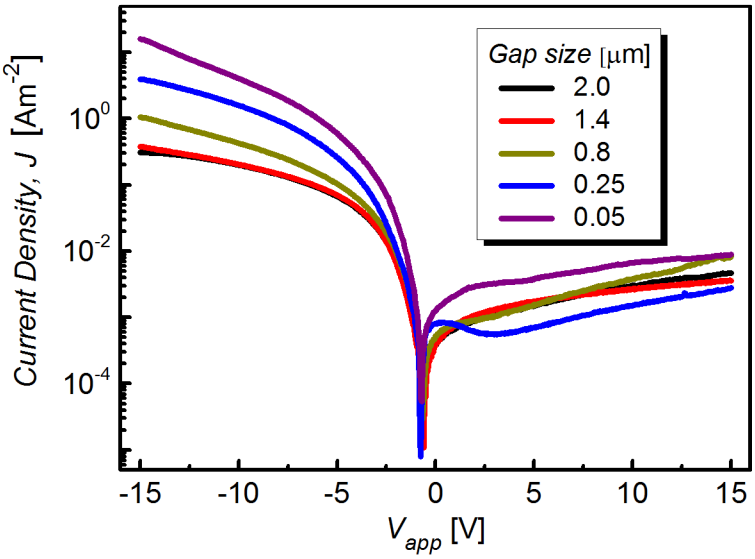

Figure 4. 7: Current density-voltage characteristics of spin coated lateral PTAA Schottky diodes with different gap sizes. Measurements are taken at a step voltage of 50 mV.

The forward current density decreases, by approximately one order of magnitude, from 15.86 Am^{-2} to 0.31 Am^{-2}, with increase in the gap size, from 0.05 µm to 2 µm respectively. This effect is thought to be associated with the reduction of the series resistance as the gap size reduces, which is demonstrated from the extrapolation of the series resistance done using Cheung and Cheung functions [16]. In their work, Cheung and Cheung stipulate that the series resistance of a Schottky diode can be obtained using the following function,

$$\frac{d(V)}{d(\ln J)} = RA_{eff}J + \frac{\eta}{\beta} \qquad 4.2$$

Here,

$$\beta = \frac{q}{kT}$$

where R is the series resistance, A_{eff} is the effective area, η is the ideality factor, J is the current density and V is the applied bias.

From the above equation, the series resistance can be obtained from the slope of the plot of *d* (*V*)/*d* (ln *J*) against *J*. Consequently, the series resistance is obtained from the plots in *Figure 4. 8* and found to vary from 3.00 MΩ to 0.09 MΩ with reduction in gap sizes as summarised in *table 4.1*.

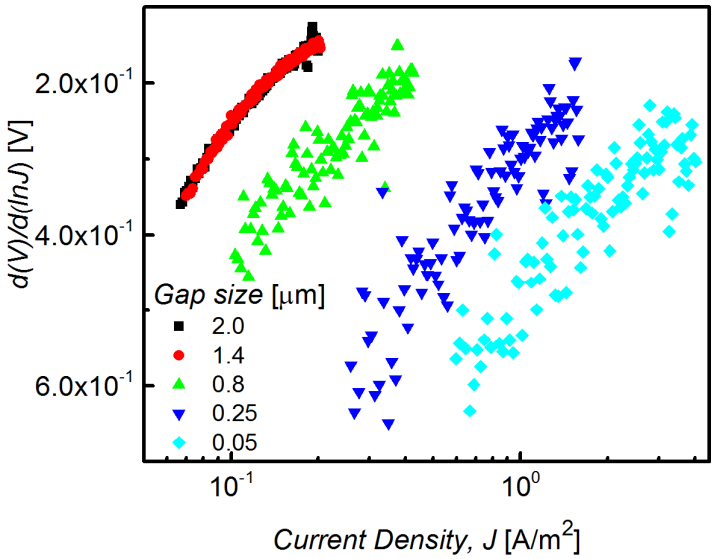

Figure 4. 8: Plot of d (V)/d (ln J) against J for the PTAA lateral Schottky diodes with gap sizes ranging from 0.05 µm to 2 µm.

Furthermore, other key parameter values such as T_C, and consequentially *MNE* are also extrapolated using the relations given by *equations 2. 32, 2. 21* and *2. 16* respectively. They are found to vary slightly with changes in gap size, which, for material parameters are expected to be constant. The reason for this variation is not fully understood, however, given that value of T_C is calculated using relation given by *equation 2. 21,* it therefore follows that variations or erroneous values in the extraction of T_0 will inadvertently affect the values obtained for T_C as well. Interestingly enough, the respective values corresponding to the smaller gap sizes as in Table 4.1, resemble almost directly those attained for vertical Schottky diodes made with the same material (i.e. T_C = 361 K and *MNE* = 32 meV) [17]. The values of T_0 and subsequently η are also obtained from *equations 2. 32* and *2. 33* and are found to vary with different gap sizes as shown in Table 4.1. The variation is believed to be attributed to the anomalous distribution of the extrinsic carriers, possibly brought on by formation of a non-ideal barrier at the interface during fabrication processes [18-20] and/or pronounced contact resistance effects, between the metal and semiconductor. On another note, the ideality factor shows a direct trend

with the gap size such that it gets smaller with a reduction in gap size, possibly due to reduction in the series resistance.

Table 4. 1: Summary of the parameters extracted from the exponential region of the lateral PTAA Schottky diodes.

Soft bake temperature (°C)	**Gap size (µm)**	**Rectification ratio**	**T_0 (K)**	**T_c (K)**	**MNE (meV)**	**η**	***Rs (MΩ)***
150	2.00	5.6×10^{1}	1853	358	31	6.2	3.00
160	1.40	9.3×10^{1}	1787	361	31	6.0	2.01
180	0.80	1.1×10^{2}	1788	360	31	6.0	1.43
190	0.25	1.2×10^{3}	1158	405	35	3.9	0.34
190_optimised	0.05	1.5×10^{3}	913	447	39	3.0	0.09

The nature of the current conduction mechanism is investigated from the slope of the plot of the current density taken at lower forward bias. At voltage values lower than −7.5 V, the conduction mechanism for some of the devices deviates to that of a space charge limited conduction (SCLC), as a result of the values obtained from the slopes i.e. > 2. From the plot of log (J_F) against log (V_F), the values of the slope, *a*, following *equation 2. 34* are extrapolated for each diode, with varying gap sizes, and represented in *Figure 4. 9*. It can be seen that *a* increases from 1.25 to 3.5, with reduction in gap size.

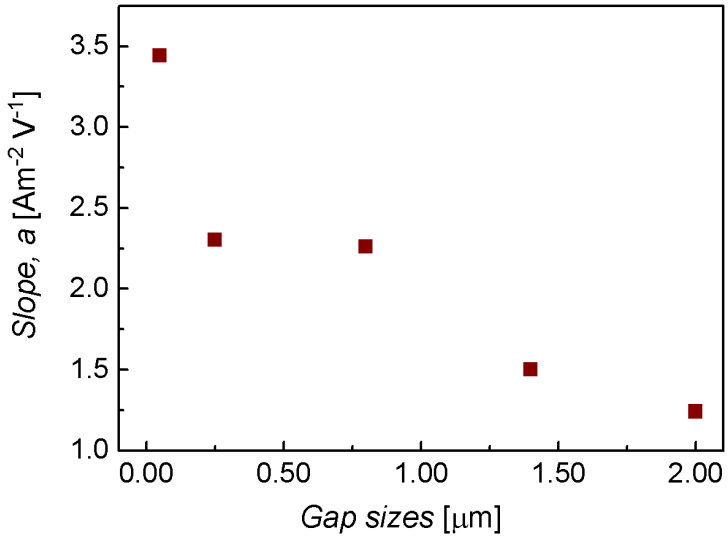

Figure 4. 9: Quadratic variation of the slope a, with changes in gap sizes. The slope is calculated from current-voltage characteristics in the neutral region.

Conventionally, the theory of SCLC assumes that the injecting electrode makes an Ohmic contact with the semiconductor such that it has an unlimited amount of charge carriers available for injection into the semiconductor and diffusion currents are assumed to be negligible as they are only deemed important in the regions close to the injecting electrode [21-23]. Based on the abovementioned assumptions, the properties of the injecting contact are usually ignored. It therefore follows that as long as there is no voltage drop across the injecting contact, the current at low applied voltages will initially be Ohmic but with further increase in the applied voltage, a space charge region is formed within the semiconductor that essentially screens the injecting contact from the associated field thereby forming a space charge limited current.

In the case of the Au contact on PTAA, the theoretical value of ϕ_m is −4.9 eV and ϕ_p is −5.2 eV respectively [24-26], therefore in thermal equilibrium, the theoretical work function difference of the two materials is 0.3 eV. In this work the Au contact is assumed to be Ohmic by functionalizing of the work function of the electrode by chemically treating it with pentafluorobenzenethiol (PFBT) self-assembled monolayer [27,28]. The chemical treatment entails immersing the substrates in a PFBT solution such that the PFBT molecules bind to the metal surface thereby inducing the formation of strong surface dipoles that shift the vacuum level. This shift results in a reduction in the work function of the metal and consequently a reduction of the barrier height at the interface of the metal and semiconductor [29]. However, previous studies of vertical diodes made within the group have however shown a lack of significant change to electrical measurements done with devices modified with PFBT [30]. Furthermore, it is likely that modification of contacts especially those occurring on the same plane may cause other effects that are not yet understood yet. Assuming that the modification of the Au contact is unsuccessful, it would therefore mean that the properties of the Au contact would affect the SCLC current observed at higher fields. The difference in work functions of the Au/PTAA interface would result in the formation of a depletion layer. This depletion layer is assumed to remain constant given that the Au contact is grounded whereas the depletion layer occurring at the Schottky/OSC interface reduces and decreases with application of a forward and reverse bias respectively. Due to the low acceptor density of PTAA, as will be discussed in the ensuing section, it is likely that the width of the depletion layer, associated with the injecting Au contact, is comparable to the width of the electrode separation (i.e. ideally for smaller gap sizes in the range of 50 nm to 300 nm). Thus in such cases, the extent of the

depletion layer associated with this contact may be more pronounced. In other words, as the electrode separation decreases, the gap resistance also decreases, and thus the current transport becomes dominated by the contact effects rather than by the bulk resistance of the film [31]. This is in agreement with the quadratic variation of the slope with reduction of the gap sizes, specifically for the diodes with gap sizes of less than 1 μm, which suggests the prevalence of SCLC mechanism. Conversely, as the gap resistance increases, the properties of the Au contact become less pronounced, and thus current is controlled by the bulk resistivity of the semiconductor. This is especially evident in devices where the gap sizes are larger than a micron, and the slope is nearly unity (1), which in such cases, obeys Ohm's law as indicated from the obtained values of the slope.

For the case of the reverse current density, there is a slight variation in the values that is independent of the gap sizes, whereby the reverse current density ranges from 2.78×10^{-3} Am^{-2} to $8.89\times10^{-3}Am^{-2}$, indicative of the varying film thickness uniformity, across different samples in spite using the same polymer solution and the same spin-coating parameters. To confirm this, thickness mapping measurements using a "Z-shaped pattern" are carried out on a 2×2 cm^2 substrate at three angles (i.e. 65°, 70° and 75°) using an M-2000 Ellipsometer. The film thickness of the deposited polymer is found to vary across the sample as shown in *Figure 4. 10* by approximately 12.6 %, thus possibly accounting for the discrepancies in the values of the reverse current density for the various gap sizes.

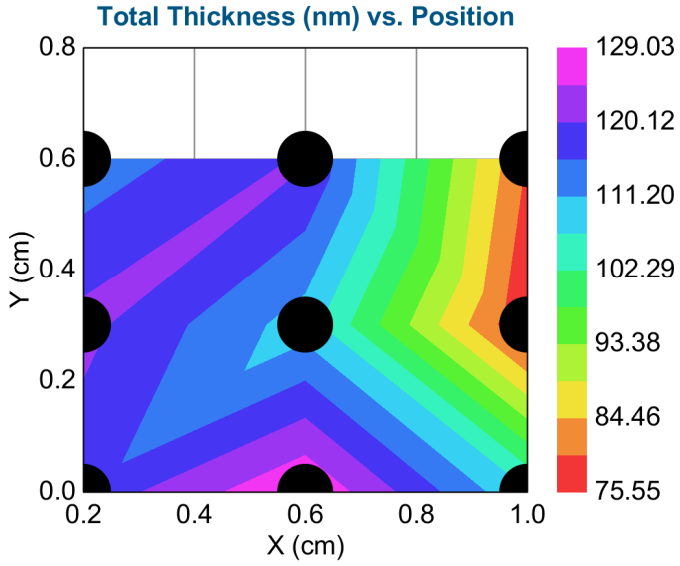

Figure 4. 10: Ellipsometry characterisation of the variation of the film thickness of the PTAA polymer across a sample for a spin speed of 1000 rpm.

Furthermore, the acceptor density N_A of the lateral PTAA devices is also extracted from the reverse characteristics as shown in *Figure 4. 11*. The acceptor density determined from the slopes of the plots of log_e (J_R) against $V_R^{¼}$ varied by one order of magnitude, from approximately 2.33×10^{20} m^{-3} to 1.76×10^{21} m^{-3}.

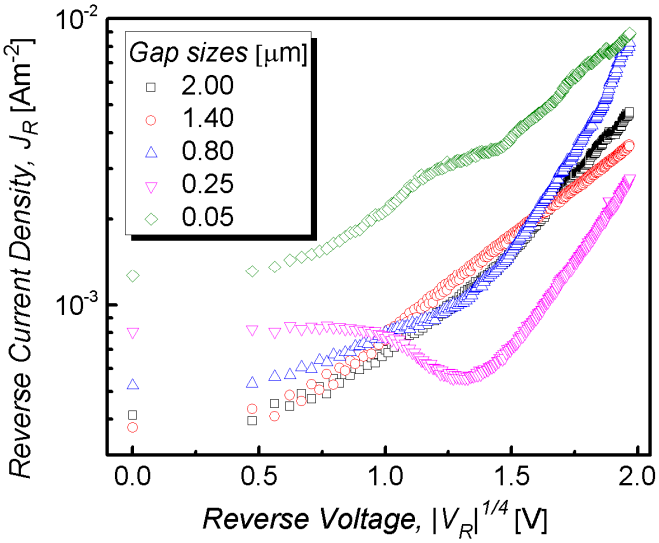

Figure 4. 11: Variation of the reverse current density against voltage, of the lateral PTAA diodes with different gap sizes.

The reason for the variation in acceptor density is due to the varying film thicknesses and possibly because of the variation of the area of active layer. Thicker films have higher reverse currents due to a higher number of residual mobile dopants occurring in the film. Furthermore, ambient oxygen can also act as an unintentional dopant in organic semiconductors [32]. The N_A values obtained correspond to a depletion width ranging from 4.8 µm to 1.3 µm, which essentially exceeds the organic film thickness of approximately 110 nm. The reverse current density in Schottky diodes is typically controlled by the modulation of the depletion layer width, W occurring at the Schottky contact. Usually it is presumed that in thermal equilibrium, the depletion width is smaller than the thickness of the active layer or simply the film is partially depleted before application of a reverse bias [33]. In such cases, on application of a reverse bias, the depletion width widens with an associated reduction in the depletion capacitance. Recent studies in pure materials such as rubrene [34], show a constant reverse bias capacitance due to the low dopant concentration in the material, such that at thermal equilibrium, the material is already fully depleted and thus the reverse

characteristics do not follow the quarter power law, typically associated with Schottky devices. Given that the values obtained for N_A correspond to a depletion width that exceeds the organic film thickness, much like the case of the rubrene diodes, it would be expected that the reverse current and capacitance would have remained constant upon application of a reverse bias. The aforementioned case does not seem applicable to the lateral diodes studied in this work as they show a visible increase in current values as well as a reduction in the depletion capacitance with the application of a reverse bias as shown in *Figure 4. 7* and *Figure 4. 12*.

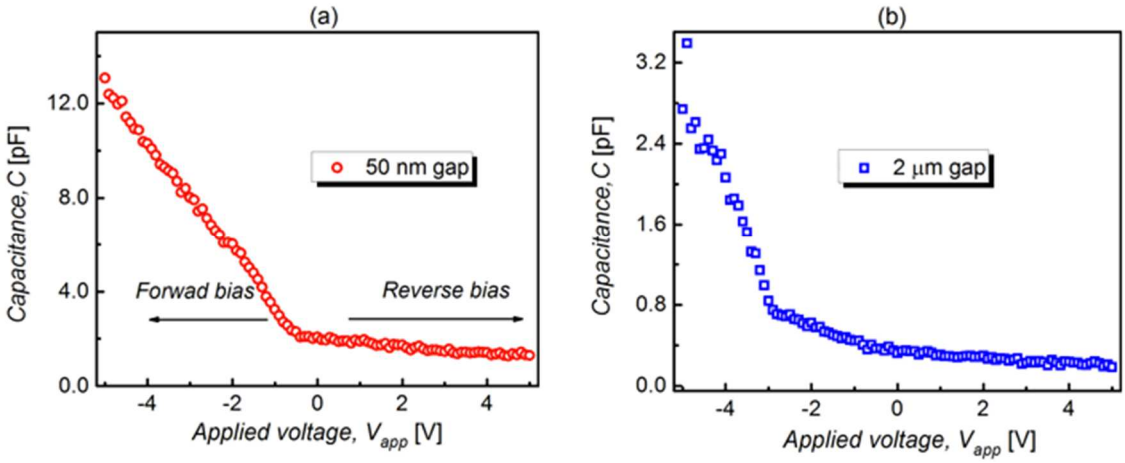

Figure 4. 12: The capacitance voltage characteristics of two PTAA lateral Schottky diodes with a gap size of 50 nm (a) and 2 µm (b) respectively. The 100 Hz frequency of the small AC signal applied is held at 50 mV whilst the DC voltage is swept from –5 V to +5 V.

To further understand the thickness dependency effect on the depletion width, a much thicker film is drop-cast onto the substrate that has the largest gap size (2.0 µm) thereby resulting in a film thickness of 1 µm. The acceptor density obtained from this sample (1 µm thick) is 3.25×10^{21} m^{-3}, corresponding to a depletion width of 1.3 µm, exceeding the thickness of the semiconductor active layer as well. The acceptor density obtained from this same sample but with a film thickness of 110 nm thick is 1.32×10^{21} m^{-3}, corresponding to a depletion width of 2.0 µm, exceeding the thickness of the semiconductor active layer as well. The latter shows that the depletion width extends past the width of the active layer irrespective of the thickness of the film for a sample with the same gap size. A summary of the extracted acceptor density values and the associated depletion widths, *W* is shown in *Table 4.2*.

Table 4. 2: Summary of the parameters extracted from the reverse current characteristics of the lateral Schottky diodes.

Soft bake temperature (°C)	**Gap size (µm)**	**Thickness of active layer (nm)**	N_A **(m^{-3})**	W_{max} **(µm)**
150	2.00	110	1.32×10^{21}	2.0
150	2.00	1000	3.25×10^{21}	1.3
160	1.40	110	1.76×10^{21}	1.7
180	0.80	110	3.01×10^{20}	4.2
190	0.25	110	1.46×10^{21}	1.9
190_optimised	0.05	110	2.33×10^{20}	4.8

In order to get a better understanding of the experimental results of the reverse characteristics, a numerical simulation is carried out using ATLAS from Silvaco. It is a well-known technology computer-aided design (TCAD) simulator, which ideally computes a set of physical equations from a device structure that is defined by the user within a two-dimensional (2-D) mesh/grid. The typical data that the user defines are device size specifications/structure, material parameters specification, mesh definition and various models for calculation of the data. From these, the possible outputs obtained include 2-D numerical solutions as well as current-voltage characteristics at specified bias conditions and contour maps detailing current distribution and electrostatic distribution such as potential, field and charge distribution.

For the numerical simulation study, two lateral structures are designed to represent the largest and smallest gap sizes i.e. 2 µm and 50 nm respectively. The simulation parameters used to define the structure and the related material properties are as outlined in *Table 4. 3*.

Table 4. 3: Physical parameters for numerical simulation in Silvaco software.

Parameter	**Value**
Dielectric constant, ε_r	3.6
Ionization potential (HOMO)	−5.2 eV
Acceptor concentration, N_A	1×10^{21} m^{-3}
Electron affinity, χ (LUMO)	−2.15 eV
Schottky (anode) work function	−4.38 eV
Ohmic (cathode) work function	−4.9 eV
Bandgap of polymer, E_g	2.95
Effective DOS	10^{20} cm^{-3}
Semiconductor thickness	110 nm

Figure 4. 13 and *Figure 4. 14* show the simulated 2-D contour map for the hole distribution inside the PTAA film of the 2 µm and 50 nm gap diode at different reverse biases,

applied on the Schottky contact. *Figure 4. 13 (a)* shows the hole distribution at thermal equilibrium, wherein such a case, the zero-bias depletion width can be approximated theoretically using the *equation 2. 41* in chapter 2. Assuming an acceptor density of 1×10^{21} m^{-3} for homogeneity in simulations, at thermal equilibrium, the zero-bias depletion width coincides with the depletion width of 250 nm, suggesting that irrespective of the gap size, the depletion width at zero bias already exceeds the film thickness. Interestingly enough, from the numerical simulations of both gap sizes (2 µm and 50nm) the latter statement is only the case for the film thickness directly on top of the Schottky contact and extends equally laterally for the same distance. In other words, for the lateral devices, the modulation of the depletion width is dictated by the lateral field across the gap rather than the film thickness. This accounts for the nearly similar depletion widths observed for the thicker and thinner samples. Given that the width extent of the polymer covering the devices is 300 µm, it is plausible to obtain depletion widths that extend towards 4 µm and above as observed in the experimental results and as evidenced from the numerical simulations plots. Notably, with increasing reverse bias voltage, the depletion width extends across the gap and continues to extend above the Ohmic contact and across it too due to the low acceptor density of PTAA.

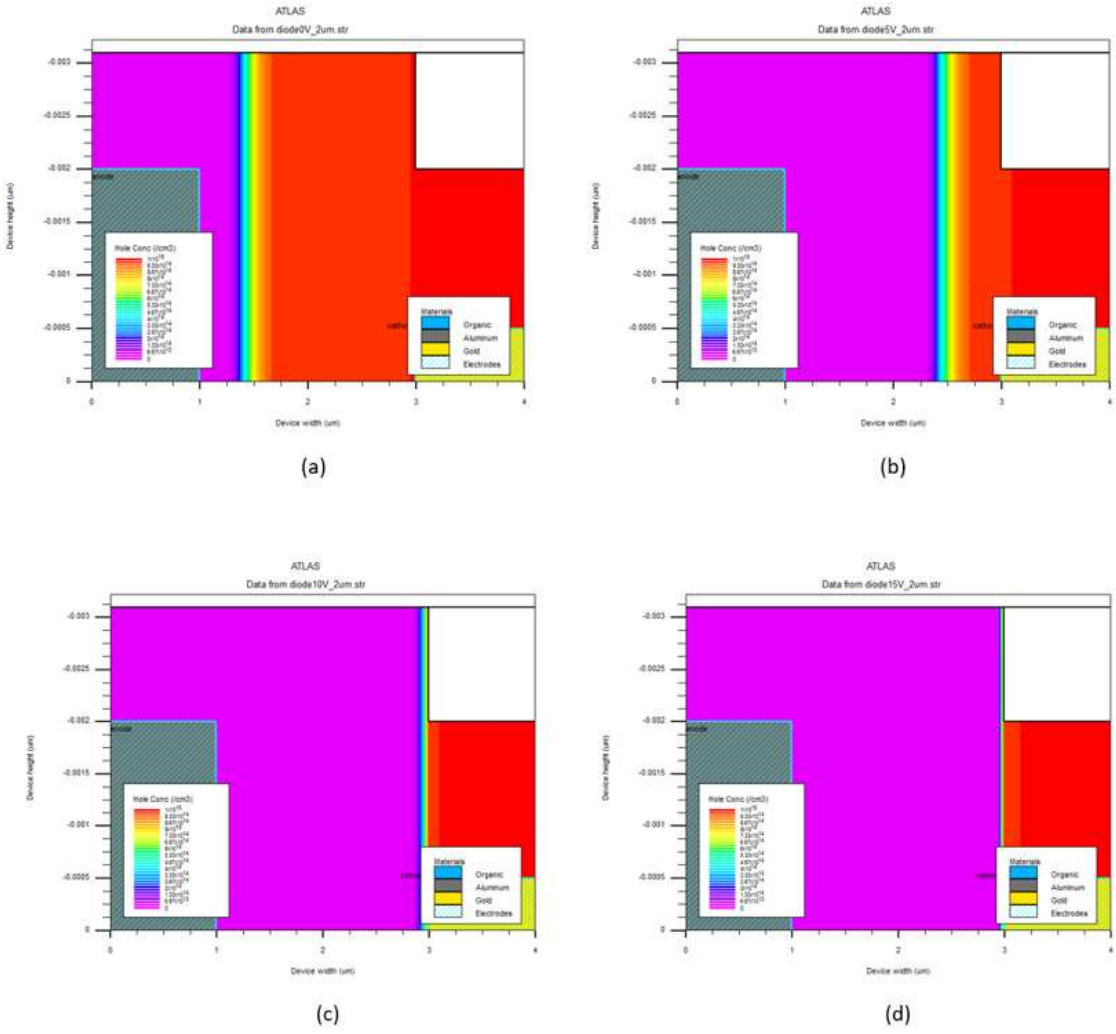

Figure 4. 13: Variation of the hole distribution with application of different reverse bias voltages for the 2 µm lateral diode: (a) 0 V, (b) 5 V, (c) 10 V and (d) 15 V.

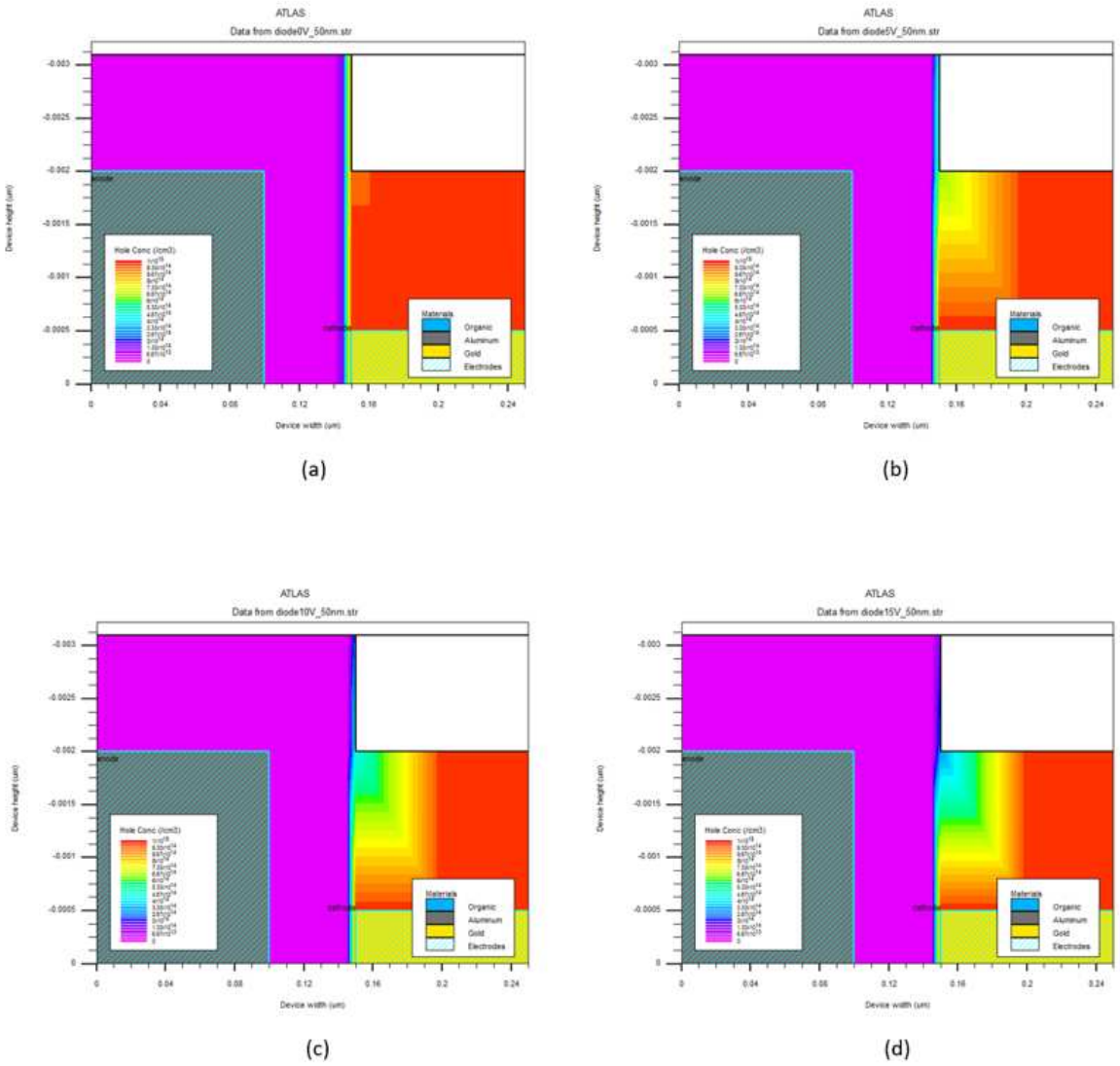

Figure 4. 14: Variation of the hole distribution with application of different reverse bias voltages for the 0.05 µm lateral diode: (a) 0 V, (b) 5 V, (c) 10 V and (d) 15 V.

Additionally, an interesting observation of the reverse characteristics is the kink/roll-over effect seen in the smaller gap sizes for example, with 50 nm and 250 nm, as can be seen in *Figure 4. 7.* This kink/roll-over effect in the reverse characteristics is believed to be because of a small hole-injection barrier occurring at the Au contact. As previously mentioned, there is a depletion layer present at the Au contact because of the difference in work functions of the Au/PTAA material. This layer remains constant given that the Au contact is grounded, however the depletion layer at the Al/PTAA interface keeps widening because of the application of a reverse bias. It is therefore likely that the depletion layer width associated with the Schottky contact overlaps with the depletion layer width of the Au contact. This is believed to be the

case for the devices having smaller gap sizes (typically <300 nm) as the depletion widths for these devices are comparable to or in some cases larger than the gap size. It is assumed that the larger gap sizes lack the kink because the two depletion layers associated with the adjacent contacts do not overlap/interact thereby the reverse characteristics remain unaffected in this case. *Figure 4. 15* below depicts the aforementioned statements.

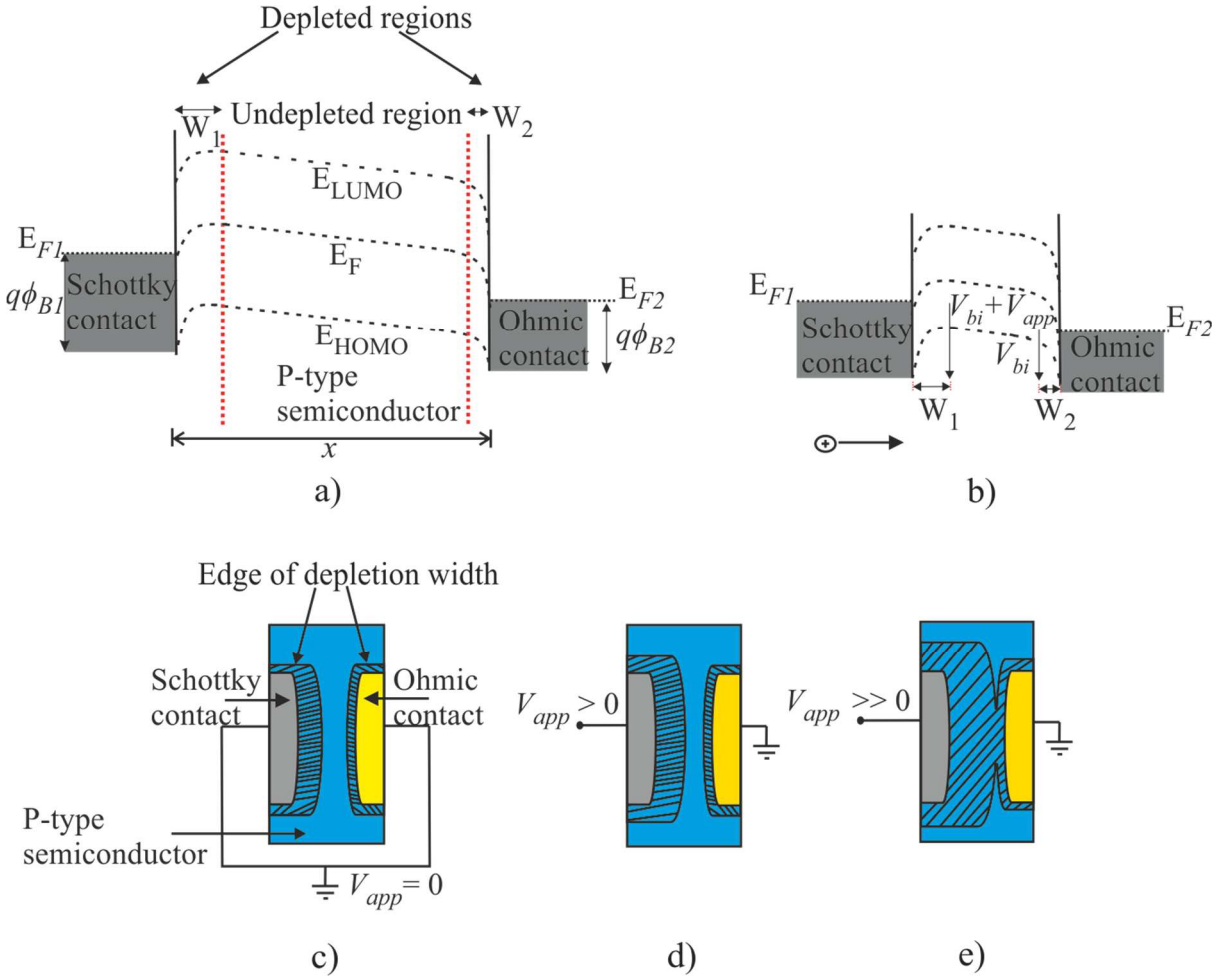

Figure 4. 15: Theoretical band diagram of the 2 µm gap and <300 nm gap lateral devices in thermal equilibrium, without the application of a bias voltage. At zero bias, the depletion layers of the adjacent contacts are not interacting as shown in (a) to (c). Upon application of a bias voltage onto the Schottky contact, the depletion width of the Schottky contact extends towards the depletion width of the Ohmic contact (d). With further increase in the voltage, the two depletion widths overlap (e) resulting in the kink in the reverse characteristics for the devices with gap sizes < 300 nm. The overlap is not observed in the 2 µm device because of the large inter-electrode distance.

4.2.4 PATTERNING SURVEY OF THE CURRENT-VOLTAGE CHARACTERISTICS OF PTAA SCHOTTKY DIODES

The isolation of the active layer through patterning usually results in reduction in cross talk between adjacent devices and subsequently an overall reduction of the leakage currents. Polymer patterning using orthogonal solvents has been achieved through either lift-off [35-37] of the polymer or via dry plasma etching [38]. In this section, polymer patterning is carried out via wet etching using 1, 2, 3, 4-tetrahydronaphthalene solvent. Due to its hazardous nature, several other studies of the dissolution kinetics of polymer films using supercritical carbon dioxide as an alternative to organic solvents such as tetrahydronaphthalene are underway although they are still in their infancy stages [39,40].

Figure 4. 16 and *Figure 4. 17* show the forward and reverse currents of gap sizes measured from lateral Schottky diodes, with patterned and unpatterned PTAA layers. It can be observed that upon patterning, the reverse currents for most of the samples increase, which is not as expected. Interestingly enough, however, the sample having a soft bake temperature of 160 °C notably had much lower reverse current values for the patterned batch compared to the unpatterned batch. The reason for these findings is not fully understood however, one could speculate that the findings could be changes in the morphology of the PTAA during the etching stage. Dissolution of a polymer film is thought to be governed by two mechanisms: solvent diffusion into the polymer network and chain disentanglement of the polymer [41-43]. These take place in three stages i.e. diffusion of the solvent molecules into the polymer film, plasticization and relaxation of polymer chains initiated by solvent molecules thereby creating a solvent-swollen gel layer and lastly reduction of the gel layer thickness due to desorption of the polymer chains into the solvent. It is proposed that perhaps the first two stages of etching took place but the third did not i.e. desorption of polymer chains into the solvent after formation of the solvent-swollen gel layer. The solvent-swollen gel layer that contains semi-detangled polymer chains and trapped solvent molecules could act as chemical dopants to the active layer thereby increasing its bulk conductivity and subsequently leading to the observed higher forward and reverse currents.

On the other hand, the current spreads for both forward and reverse characteristics are significantly reduced in most of the samples. Further to this, the forward currents of the patterned samples scaled inversely to the higher soft bake temperatures (i.e. smaller gaps)

similar to the observation made in the previous section. The reverse current on the other hand did not show any correlation to the gap size as expected, given that the reverse current values are chiefly dictated by the film thickness.

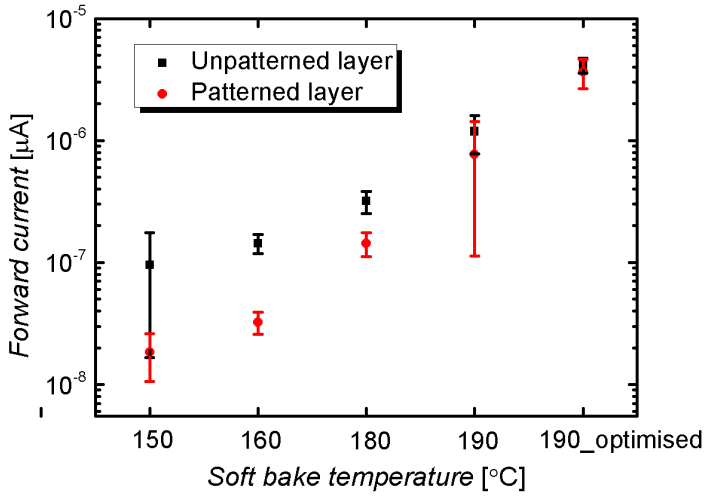

Figure 4. 16: Variation of the forward currents of the lateral diodes, for both patterned and unpatterned samples, with varying gap sizes achieved by varying the soft bake temperature. The first four samples i.e. 150 °C, 160 °C, 180 °C and 190 °C are processed with the same soft bake time of 225 seconds whereas the 190_optimised sample denotes a sample processed with a soft bake temperature and time of 190 °C and 45 seconds respectively.

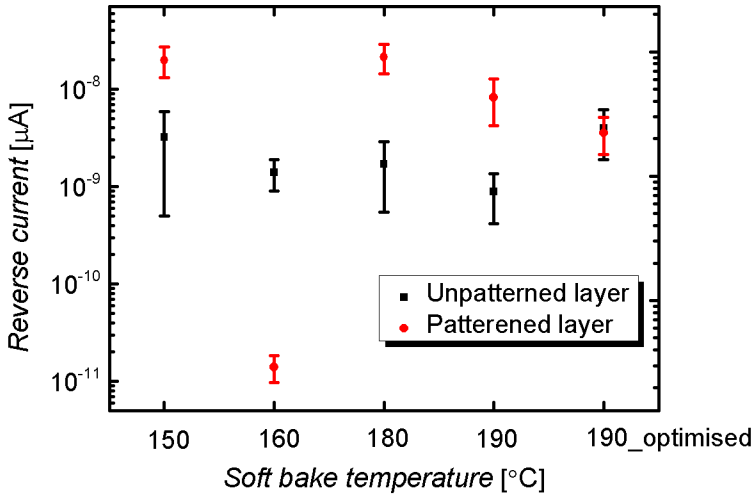

Figure 4. 17: Variation of the reverse currents of the lateral diodes with varying gap sizes for both patterned and unpatterned samples.

4.3 SELF-ALIGNED THIN-FILM TRANSISTOR WITH PBTTT-C16

4.3.1 FABRICATION METHODOLOGY

The structure of the planar self-aligned thin-film transistor (TFT) used in this work is as shown in *Figure 4. 18*. The source and drain contacts comprise of gold (Au) electrodes, whilst the gate contact consisted of aluminium (Al) electrode. The gate oxide constitutes of aqueous anodised aluminium oxide (Al_2O_3) and the *p*-type semiconductor is PBTTT-C16. PBTTT-C16 is utilised for both TFT and circuit characterisation in subsequent sections due to its high mobility relative to the previously studied polymer, PTAA.

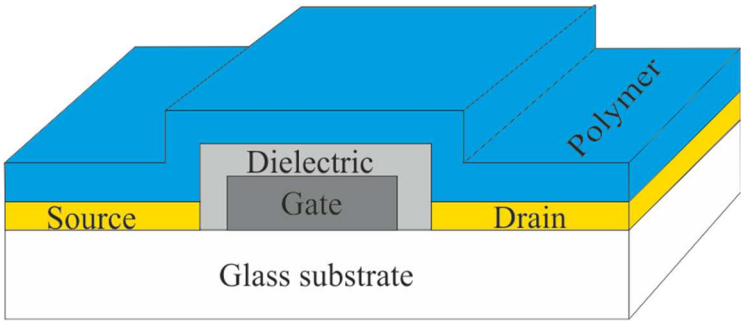

Figure 4. 18: Structure of the planar, PBTTT-C16 TFT, with Al_2O_3 gate dielectric and gold source and drain contacts.

The procedures involved in the development of the self-aligned PBTTT-C16 are described next. The processing steps involved in defining the source, drain and gate contacts (steps 1 to 3), are as discussed in *section 4.2.1* of the lateral diode section and demonstrated in *Figure 4. 19 (a) to (k)*.

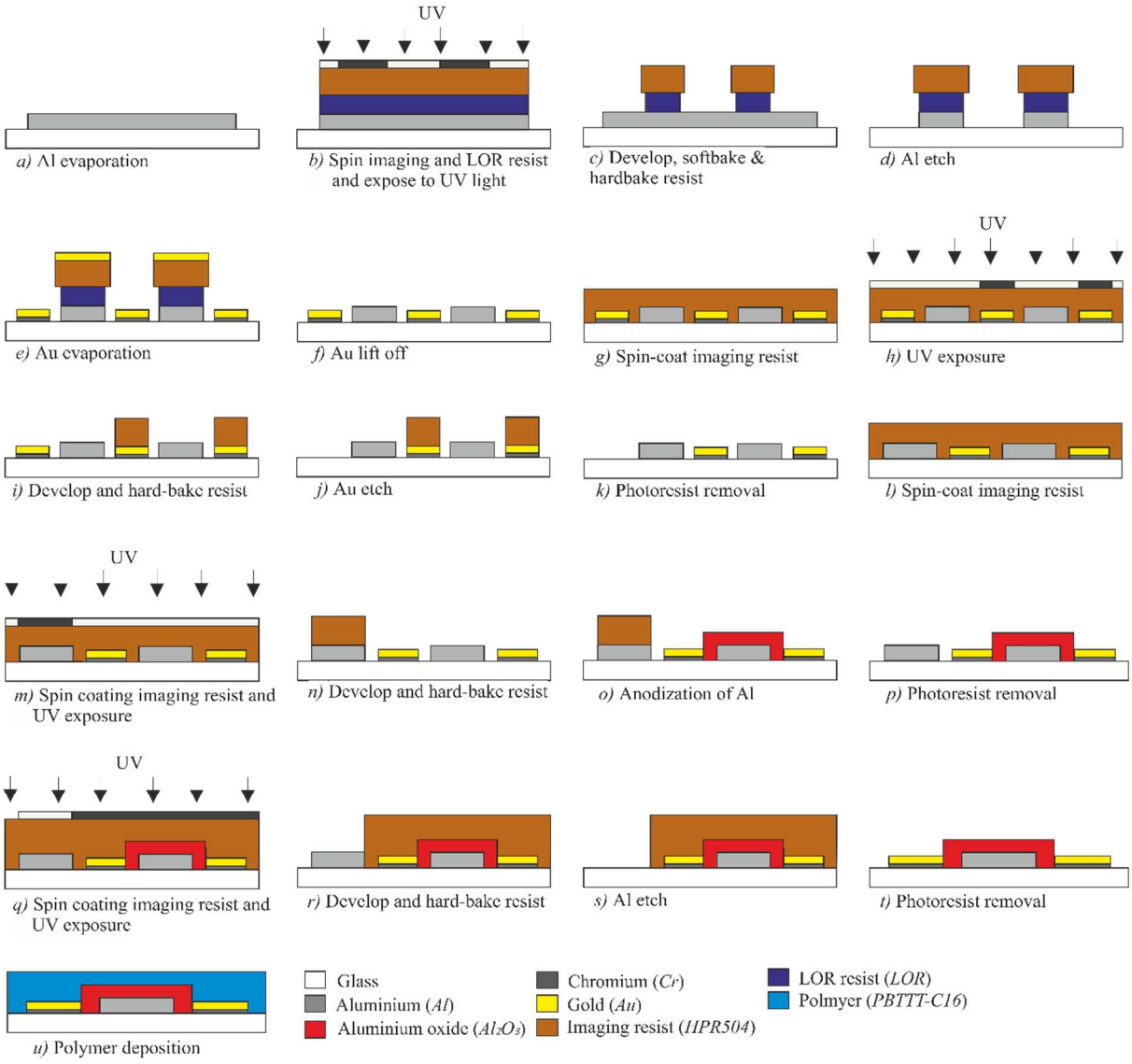

Figure 4. 19: Overview of the fabrication of a bottom gate planar p-type OTFT made using a self-aligned fabrication processes.

To achieve an undercut of 50 nm, a soft bake temperature and time of 190 °C and 300 seconds is used for step 2. The aforementioned size is used to reduce the series resistance of the TFT and accommodate an oxide film thickness of 50 nm to achieve high oxide capacitance, C_{ox} and consequently result in low threshold voltage values, V_T. In this section, a brief overview/explanation of the formation of the gate oxide as well as polymer deposition is discussed.

1. *Glass cleaning*: Same process as described for "glass cleaning" in *section 4.2.1*.

2. *Gate contact patterning and gap formation:* Akin to "Al patterning and gap formation" in *section 4.2.1.*
3. *Source/Drain formation:* Similar process to "Au patterning" in *section 4.2.1.*
4. *Gate oxide formation:*

A constant voltage method is used for aqueous anodization of aluminium as it is believed to result in the formation of oxide films without voids [44]. With this process, the resultant thickness of the oxide generally depends on the magnitude of the applied voltage. Details on the anodization process are given below:

- A positive image resist (HPR 504) is spun on the pre-patterned source, drain and gate contacts on the glass samples at 3000 rpm for 45 seconds followed by soft baking of the samples at 110 °C for 90 seconds on a hotplate, as demonstrated in *Figure 4. 19 (l).*
- The resist-coated samples are exposed to UV light using a mask aligner followed by developing in HPRD 429 developer for 45 seconds as illustrated in *Figure 4. 19 (m).* The mask used to make the OTFT devices is demonstrated in *section 5.3* of Chapter 5, however a sample layout of the SAG TFT found in this mask is as shown in *Figure 4. 20.*

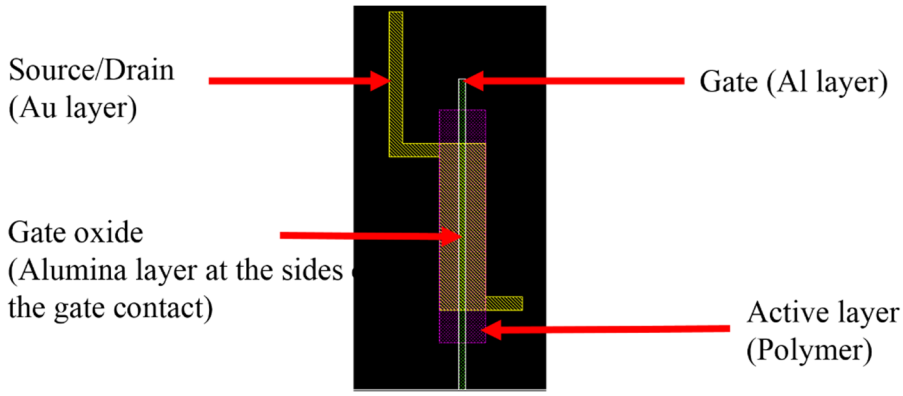

Figure 4. 20: Sample layout of a SAG TFT fabricated in this work having a channel width and length of 500 µm and 20 µm respectively.

The samples are then rinsed in deionised water and dried with a nitrogen gun. The imaging resist is then hard baked at 140 °C for 120 seconds on a hot plate, as shown in *Figure 4. 19 (n),* to make the photoresist resilient to chemical attacks by the electrolyte

solution used for anodization. The samples are then setup for anodization as illustrated in *Figure 4. 21*, with the aluminium layer used as the anode and a platinum foil as the cathode, immersed in an electrolyte solution of 0.001 M citric acid solution. The citric acid is bought in powder form from Merck Chemicals Ltd, UK before making the solution using deionized water. A constant voltage of 30 V is applied across the anode and cathode, and left to anodize for about half an hour, to obtain a 50 nm thick dielectric as demonstrated in *Figure 4. 19 (o)*. *Figure 4. 22* shows a relationship between the applied voltage and the thickness of the oxide grown as well as the breakdown voltage, as attained previously within the group [45]. After anodization, the samples are rinsed thoroughly in deionised water, followed by drying with a nitrogen gun and annealed in nitrogen at 100 °C for two hours. Subsequently, the resist is removed by submerging the samples in a beaker of 80 °C pre-heated micro-stripper solution for about an hour followed by a thorough rinse in deionised water and drying using a nitrogen gun as shown in *Figure 4. 19 (p).*

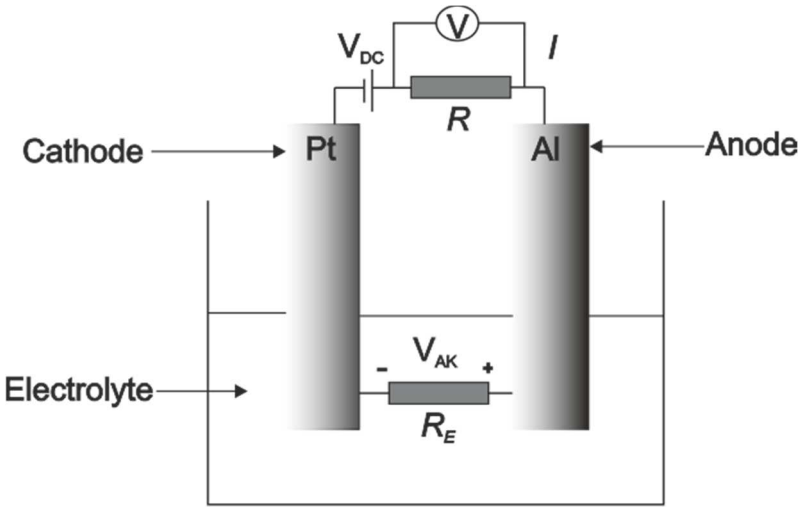

Figure 4. 21: Setup for aqueous anodization of aluminium using a constant voltage method. The anode and cathode consists of the pre-patterned Aluminium layer and a platinum foil respectively, and the electrolyte is a 0.001 M citric acid solution.

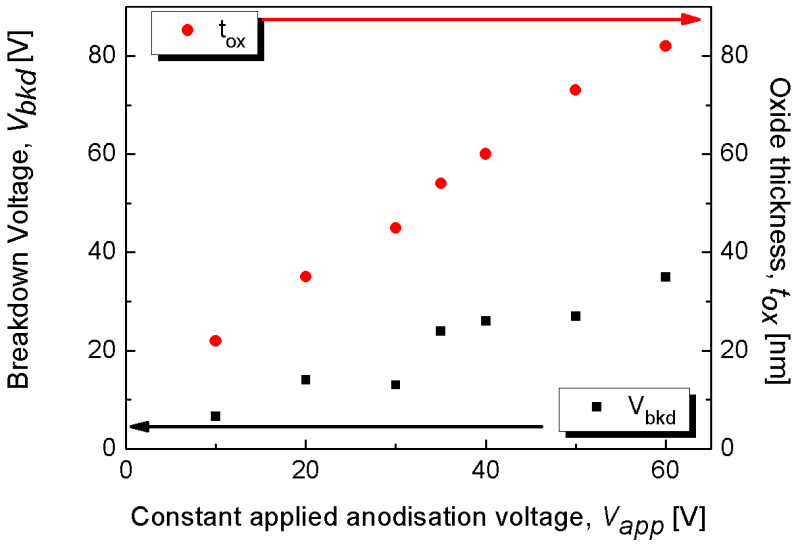

Figure 4. 22: Variation of the oxide film thickness and breakdown voltage with the constant applied voltage. Adapted from [45].

5. Al etch

In this process step, the unwanted aluminium areas are etched, which essentially defines the areas of aluminium that can be removed after oxide growth. These areas are only required to supply electrical current to specific areas of the devices/circuit for anodization to occur. Details on the etching process are given below:

- A positive image resist (HPR 504) is spun on the glass samples at 3000 rpm for 45 seconds followed by soft baking of the samples at 110 °C for 90 seconds on a hotplate as in *Figure 4. 19 (q)*.
- The resist-coated samples are exposed to UV light using a mask aligner followed by developing in HPRD 429 developer for 45 seconds as demonstrated in *Figure 4. 19 (r)*. The samples are rinsed in deionised water and dried with a nitrogen gun then the imaging resist is hard baked at 140 °C for 120 seconds on a hot plate. The next step involves the wet chemical etching of the aluminium layer as shown in *Figure 4. 19 (s)*. The resist is subsequently removed as detailed in part 2 of *section 4.2.1* and as demonstrated in *Figure 4. 19 (t).*

6. Polymer deposition: PBTTT-C16.

In this process, the PBTTT-C16 polymer is deposited via spin coating. Attempts to isolate the active layer through patterning are futile. Details on the polymer deposition process are outlined below and as shown in *Figure 4. 19 (u)*:

- The substrates are briefly exposed to oxygen plasma, followed by the formation of a self-assembled monolayer by immersing the samples in 2-propanol solution of 5 mM n-octadecylphosphonic acid (ODPA). ODPA chemical is procured from Alfa Aesar, UK prior to making the aforementioned solution using propanol. After 16 hours [46], the samples are rinsed thoroughly in 2-propanol, dried with a nitrogen gun and baked on a hot plate for 300 seconds at 60 °C. This step is understood to change the surface properties of the dielectric from hydrophilic to hydrophobic, thereby improving polymer adhesion onto the substrates [47,48] and subsequently molecular ordering of the polymer on the substrates. The semiconductor solution is formed by dissolving 10 mg/ml of PBTTT-C16 solution in hot (100 °C) 1 ml of dichlorobenzene. The solution is left to mix thoroughly with a magnetic stirrer, on a hot plate, for three hours. While still hot, the solution is then spun on the samples at 1000 rpm for 45 seconds, which results in a film thickness of about 70 nm. The films are subsequently annealed at 180 °C for 10 minutes followed by slow cooling at approximately 5 °C/minute, through the liquid-crystal mesophase region. The samples are left in vacuum overnight prior to electrical characterisation using a HP4155B semiconductor parameter analyser.

4.3.2 OUTPUT CHARACTERISTICS OF THE PBTTT-C16 TFT

Figure 4. 23 shows the output characteristics of the PBTTT-C16 TFT with a channel length of 20 µm and channel width of 1000 µm. As expected, the drain current increases with drain voltage for a given gate voltage bias. The slight curvature in each of the output characteristics at a small drain-to-source voltage, V_{DS}, is indicative of the presence of contact resistance effects, associated with the difference in the work function between Au and PBTTT-C16 layer (about 0.2 eV difference). In addition, the metal resistance of the Au layer also contributes to the contact resistance effect. Although the samples are dipped in PFBT solution to lower the potential barrier, additional surface treatments are done to the interface of the dielectric and the organic semiconductor as mentioned in the sixth fabrication step in *section 4.3.1*. Briefly, a plasma treatment and SAM treatment using ODPA is done to smoothen the dielectric/OSC interface and to reduce interface-trapping effects that are particularly prevalent in bottom gate-bottom contact and planar TFT structures. It is well known that the contact resistance is greatly determined by the electronic structure of the materials, chemical bonds as well as the geometrical structure (edges) and surface morphology of the interface [49]. Consequently, the difference in the surface morphology and edges of the contacts relative to the semiconductor plays a vital role for efficient injection of carriers at the metal/semiconductor interface. Moreover, it has been shown that higher contact resistances arise due to strong orbital hybridisation and a lack of chemical bonding thereby the aforementioned SAM modifications of the dielectric may chemically alter the potential barrier and consequently the interface of the Ohmic contacts and the semiconductor [50,51] resulting in the parasitic contact effects seen in the characteristics.

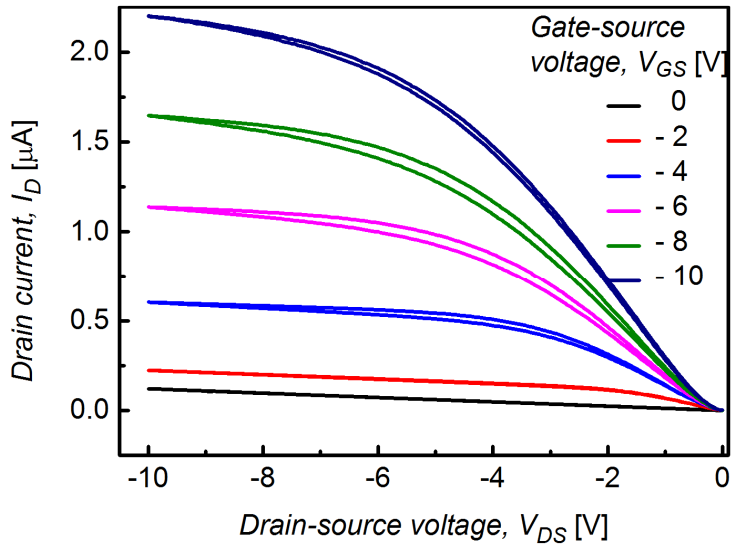

Figure 4. 23: Output characteristics of the self-aligned PBTTT-C16 TFT. The thickness of the active layer and aluminium oxide is 65 nm and 50 nm respectively. The aspect ratio of the TFT is 50 (W/L=1000 µm/20 µm).

It is expected that with further increase in drain voltage, the current saturates after pinch-off condition because of carrier depletion at the drain end. The lack of saturation of the drain current in this device may be because of the presence of residual impurities/dopants which result in an increase in hole concentration and thereby bulk conductivity at the drain terminal.

4.3.3 TRANSFER CHARACTERISTICS OF THE PBTTT-C16 TFT

Figure 4. 24 shows the corresponding transfer characteristics of the PBTTT-C16 TFT. The gate voltage is swept from −10 V to +10 V and vice-versa at a fixed drain voltage of −10 V. In the off state i.e. on application of a positive gate bias ($V_{GS} > V_T$), it can be seen that the drain current remains nearly constant. The current in this case is associated with the bulk conductivity of the film. When the gate voltage bias is reversed, and with application of a negative drain bias, holes are injected through the drain terminal thereby resulting in a sharp increase of the drain current as observed in the plot. In this sub-threshold regime, the drain current increases exponentially due to the exponential increase in the carrier concentration, attributed to the exponential increase of the DOS. With further increase in gate bias, more carriers are accumulated at the semiconductor/dielectric interface thereby resulting in an increase in the drain current until it finally saturates.

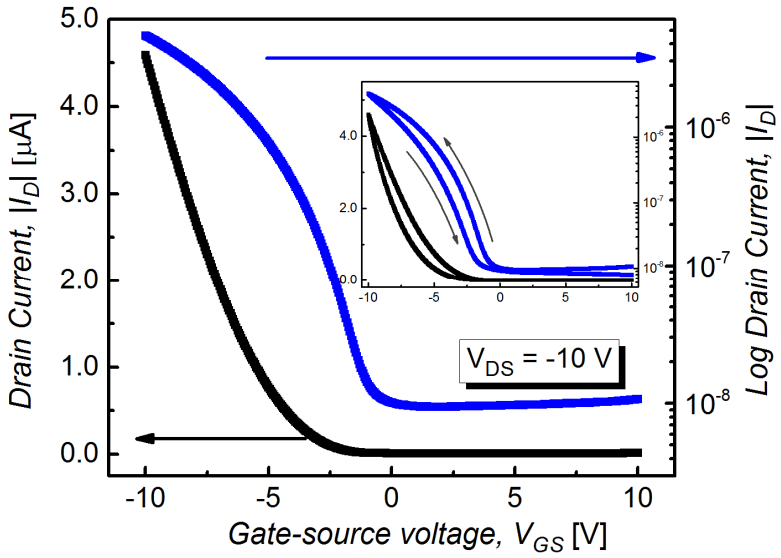

Figure 4. 24: Linear and sub-threshold plots of spin-coated SAG PBTTT-C16 TFT swept from V_{GS} of +10 V to −10 V at a V_{DS} of −10 V. Inset: forward and reverse sweeps of the transfer characteristics. The thickness of the active layer and aluminium oxide dielectric is 65 nm and 50 nm respectively. The aspect ratio of the TFT is 50 (W/L=1000 µm/20 µm).

The on/off ratio of the transistor is found to be about 4.26×10^2. Higher on/off ratios of 10^4 have been reported for this material [52]. The low on/off ratio observed in this work is possibly attributed to the ambient effects i.e. light and oxygen, which unintentionally dope the active layer thereby resulting in higher acceptor density values and bulk conductivity values consequently causing higher off currents. Another reason for the low on/off ratio could be related to the film thickness. The on/off ratio depends on the film thickness using the relation below [53].

$$\frac{I_{on}}{I_{off}} = \frac{\mu}{\sigma}\frac{C_{ox}^2}{qN_A x_p^2}V_D^2 \qquad 4.3$$

where I_{on} and I_{off} are the on and off currents, μ is the mobility term, σ is the conductivity, q is the electronic charge, N_A is the acceptor density, x_p is the polymer thickness, C_{ox} is the oxide capacitance and V_D is the drain bias.

A sub-threshold swing of −1.8 V/decade is obtained from the inverse of the slope in *Figure 4. 24*, within the voltage range of −1 V and −2.5 V. Smaller values of the subthreshold swing are desirable in order to have fast switching speeds in circuits and thereby less power consumption. The saturation field-effect mobility, μ_{fe} and threshold voltage, V_T are also

extrapolated from the plot of $I_D^{0.5}$ versus V_G and are found to be 0.74 $cm^2V^{-1}s^{-1}$ and −1.5 V respectively. The low value of the threshold is attributed to the use of a high-k dielectric, Al_2O_3, with a dielectric constant of approximately 10. The saturation field-effect mobility of this polymer has been found to vary from around 0.1 $cm^2V^{-1}s^{-1}$ to as high as 1 $cm^2V^{-1}s^{-1}$ depending on the device structure and method of deposition of the polymer [54,55]. It should be noted that the field-effect mobility extracted here is simply a figure of merit as it is obtained using the square-law dependency for drain current i.e. following the standard MOSFET equation as given by *equation 2. 48*, which is not entirely applicable to organic TFTs. However, more appropriate material constants such as *K* and *m* expressed in the disordered model derived in chapter 2 are extrapolated from the characteristics as detailed in the ensuing sections.

The material constants, *m* and *K*, are obtained from the plot of $log\ (dI_{sat}/dV_G)$ against $log\ (V_G')$ as shown in *Figure 4. 25*. The respective values are found to be approximately 0.57 and 2.15×10^{-16} AV^{-m} which corresponds to T_C and *MNE* of 473 K and 41 meV respectively. These values are lower than those extracted from the vertical Schottky diode measurements found in chapter 3 most likely due to the evident contact resistance effects observed in the output characteristics of the TFTs.

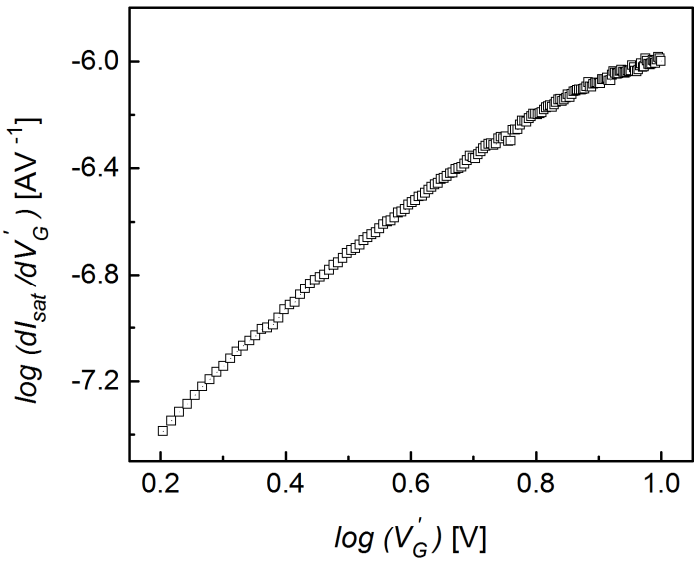

Figure 4. 25: Plot of log (dI_{sat}/V_G') against log (V_G') for PBTTT-C16 SAG TFT measured at V_{DS} = −10 V.

Using the previously derived parameters values of *m*, *K* and T_C, the dependence of the effective mobility with change in gate voltage is extracted using *equation 2. 53* and plotted as in *Figure 4. 26*. From the plot, it can be seen that the effective mobility varies with the applied bias such that, it increases with applied gate voltage due to the increase in carrier concentration injected in the channel as explained by the UML and the VRH mechanism, described in chapter 2.

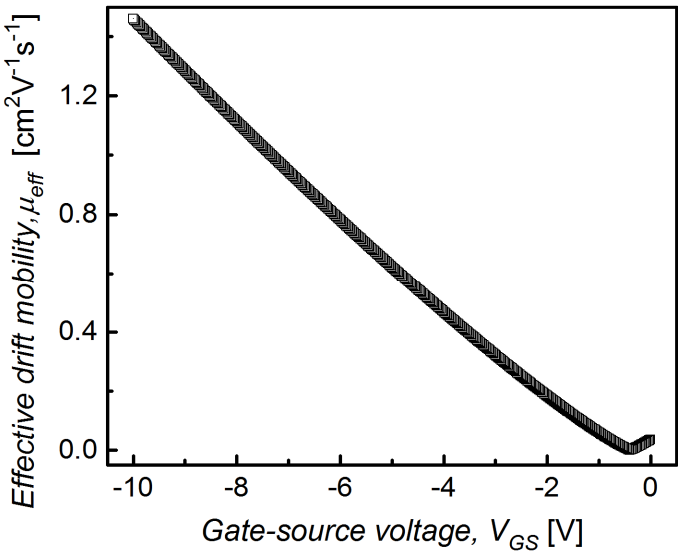

Figure 4. 26: Variation of the effective mobility of the PBTTT-C16 SAG TFT, with changes in the applied gate voltage.

Utilising the above mentioned parameters, a fitting of the disordered equations (*equations 2. 50* and *2. 51*) is also made to the experimental data using MATHCAD software. The fit in *Figure 4. 27*, shows good agreement for values higher than −8 V, but a slight deviation from −8 V to −10 V. This could be due to contact resistance effects which are not accounted for when fitting of the experimental data to the disordered model.

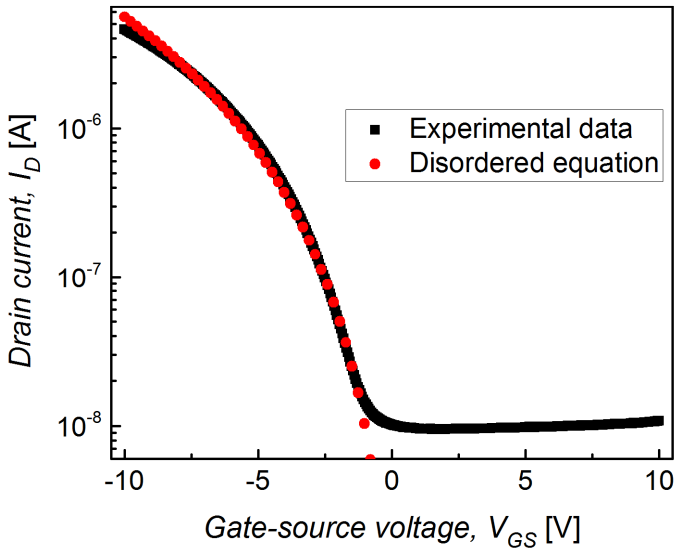

Figure 4. 27: Transfer characteristics using the disordered equation (red dots), fitted to the experimental data (black squares) of PBTTT-C16 TFT of W/L=50, oxide thickness of 50 nm and applied drain voltage, V_{DS} = −10 V.

To study the stability of the TFT, repeated forward and reverse sweeps (−10 V to +10 V and vice-versa) are carried out on the transfer characteristics, as shown in the inset of *Figure 4. 24*. The off-current changes slightly from 7.7 nA to 10.8 nA possibly due to the unintentional doping effect of oxygen and light as mentioned in the previous sections. Due to this effect, the conductivity of the polymer film increases thereby increasing the value of the drain current for positive gate voltage values.

An additional feature is the hysteresis formation when the direction of the gate voltage sweep is reversed. This results in a change in the threshold voltage of −1.5 V to −2.2 V, when the sweep is from −10 V to +10 V (forward sweep) and +10 V to −10V (reverse sweep) respectively. Typically, for an ideal TFT, the I_D-V_{GS} characteristics and subsequently the threshold voltages are identical regardless of the sweeping direction. Such instability could be because of oxide charge or residual dopant ions occurring in the oxide and semiconductor. Oxide charges usually include fixed charges, mobile ions and trapped charges [56,57]. The presence of fixed charges in the oxide ordinarily manifests itself in the form of a lateral shift of the I_D-V_{GS} characteristics relative to the polarity of the induced charges. In other words, it does not form a hysteresis effect thereby it is doubtful that the fixed charges resulted in the transfer characteristics obtained. In addition, mobile ions within the oxide would result in a clockwise hysteresis I_D-V_{GS} characteristic rather than anticlockwise as observed in this work.

Alternatively, anticlockwise hysteresis has been associated with traps occurring at the interface of the semiconductor and the dielectric. These traps are thought to result from morphological defects of the polymer film, surface polarity and roughness of the dielectric [57] and occurrence of small adsorbed molecules [58,59] such as oxygen (O_2), water (H_2O) and hydroxyl molecules (OH)) at the interface. The net charge density of traps that subsequently forms results in a built-in-field that modifies the threshold voltage thereby causing hysteresis between the forward and reverse sweeps. Modification of the dielectric interface using a SAM layer, as carried out in this work, mitigates but does not completely eliminate the degree of hysteresis [60]. Nonetheless, by the same token, the component molecules of the SAM layer has a built-in dipole field that changes the surface potential of the metal/semiconductor interface akin to applying a negative gate voltage [61]. Altering the magnitude of the built-in-field results in changes of the threshold voltage and subsequently the formation of an anticlockwise hysteresis occurs.

Additionally, the anticlockwise hysteresis could be associated with the presence of mobile residual dopants/impurities in the semiconductor film [44] due to the use of a solution-based fabrication process for the formation of the oxide and semiconductor layer. The anticlockwise hysteresis suggests that the charge of the mobile ions in the semiconductor is negative; therefore, for a forward gate voltage sweep i.e. from −10 V to +10 V, the mobile ions firstly deplete from the surface and then accumulate possibly forming a thin layer of mobile ions. On reversing the sweep, the opposite occurs thus resulting in the hysteresis effect because of the charge drifting with application of gate voltage. In essence, any surface charge occurring at the interface of the metal/semiconductor and/or mobile ions located in the semiconductor inherently results in hysteresis of the transfer curves in so doing influencing both the threshold and turn-on voltage as observed in this work.

4.4 CONCLUSIONS

A SAG fabrication process that utilises a bi-layer photoresist consisting of an imaging resist layer and a sacrificial lift-off resist layer is presented in this chapter. By varying the soft bake temperature and time, a parametric study of the undercut size formed by the process is carried out. The undercut size is found to increase with decreasing soft bake parameters due to

a higher retention of residual solvents within the film, which eases diffusion of the developer solution into the resist film resulting in faster dissolution rates and hence undercut sizes. Moreover, the undercut size is found to have a larger dependency on the soft bake temperature parameter than the soft bake time.

A scaling study of the undercut size formed by the self-aligned process is carried out using five lateral Schottky diodes with varying gap sizes, ranging from 0.05 µm to 2 µm. The organic semiconductor used for this study is PTAA, with gold and aluminium metal as the Ohmic and Schottky contacts respectively. The forward current density is found to decrease, by approximately one order of magnitude (from 15.86 Am^{-2} to 0.31 Am^{-2}), as the gap size increases from 0.05 µm to 2 µm, which is thought to be due to the overall reduction in the series resistance of the devices. Moreover, the ideality factor is found to vary directly with the gap size, from 5.0 to 2.2 possibly due to reduction in the series resistance, which essentially affects the potential barrier at the metal/semiconductor interface. The derived values of T_0 also varies with the gap sizes from 913 K to 1853 K; the variation is associated with the anomalous distribution of extrinsic carriers brought on by fabrication processes. The characteristic temperature of the traps, T_C also ranges from 671 K to 1503 K. It would however be expected to remain constant as it is a material parameter, defining the distribution of the traps/states. The reason for this divergence is still not yet understood but it is speculated to be because of the variation of the T_0 values, which thereby affects the values, obtained for T_C as well.

The nature of the current conduction mechanism of the PTAA diodes is also investigated from the logarithmic plot of the current density versus the forward bias taken at the higher voltage regime. At lower voltage values, the conduction mechanism started off as being Ohmic however at higher voltage values, the conduction mechanism for the devices with gap sizes lower than 1 µm deviated to that of a SCLC, as observed from the values obtained from the slope (> 2.0).This is due to the fact that as the electrode separation decreases, the gap resistance also decreases, and thus the current transport becomes dominated by the properties of the Au contact rather than by the bulk resistivity of the film.

The reverse current density values obtained from the same devices ranged from 2.78×10^{-3} Am^{-2} to 8.89×10^{-3} Am^{-2} since the spin-coated film is non-uniform with variation in thickness of about 12.6 % observed across the substrate, as measured through Ellipsometry measurements. Devices having gap sizes less than 300 nm, are found to have kinks/roll-over

effects in the reverse characteristics. This phenomenon is thought to be due to the depletion layer width overlapping with the depletion layer of the Au contact, as the gap size is comparable and/or smaller to the width of the expanding depletion layer of the reverse-biased Schottky contact. This is particularly possible for pure materials such as PTAA, which has a lower acceptor density. The acceptor density is extrapolated from the plot of $log_e (J_R)$ against $V_R^{¼}$, assuming the applicability of the abrupt depletion region approximation. The acceptor density obtained from the slopes of the plots varied by one order of magnitude ranging from approximately 2.33×10^{20} m^{-3} to 1.76×10^{21} m^{-3}, corresponding to a depletion width ranging from 4.8 µm to 1.3 µm, which effectively exceeds the thickness of the organic PTAA film, 110 nm, even in the absence of an external bias. The variation in the acceptor density values is attributed to the variation of the thickness of the active layer and thus the amount of residual dopant within the film. Further characterisation studies of the charge distribution within the lateral devices carried out using SILVACO software reveals that unlike vertical Schottky diodes, the modulation of the depletion width in lateral Schottky diodes is dictated by the lateral field across the gap and the active layer area rather than the film thickness.

A study on the reduction of the area of PTAA active region is also carried out by patterning the previously mentioned lateral diodes using orthogonal solvents. With the exception of the reverse characteristics of the 1.40 µm device, the values of the forward and reverse currents increases after patterning, which is not as expected. Such findings are thought to be associated with the unintentional doping of the active layer by the chemical solvents used in the patterning thus resulting in higher bulk conductivity values and consequently higher forward and reverse currents. Nonetheless, the forward and reverse current spreads are significantly reduced after patterning, suggesting the reduction of cross talk across the substrate. Further research into alternative patterning techniques/chemicals for this material would therefore need to be explored.

A planar PBTTT-C16 TFT is also fabricated using the optimised SAG process. The TFT comprises of anodised aluminium oxide as the gate dielectric, gold as the source and drain contacts, and aluminium for the gate contact. The aspect ratio of the device is 50 with a dielectric film thickness of about 50 nm and an active layer with a thickness of 65 nm. The output characteristics show a slight curvature for low drain voltage values because of contact resistance effects at the interface of the contacts and the polymer layer. In addition, the output

characteristics display poor pinch-off conditions due to the presence of residual impurities from solution processing.

The sub-threshold characteristics of the same transistor measured at a drain bias of −10 V has a sub-threshold swing of −1.8 V/decade and an on/off ratio of 4.26×10^{2}. The low on/off ratio is associated with oxygen in the air having a doping effect on the polymer thereby increasing the bulk conductivity of the film and hence the off-currents. Fabricating and characterising in a glovebox environment, filled with inert air and with low humidity content can lead to better off-currents and ratios. The saturation field-effect mobility, μ_{fe}, and threshold voltage, V_T, extrapolated from the plot of $I_D^{0.5}$ versus V_G, are found to be approximately 0.74 $cm^2V^{-1}s^{-1}$ and −1.5 V respectively, which agree to those reported in the literature. The lower threshold values attained is attributed to the higher k-dielectric Al_2O_3 used for the gate oxide. The stability of the PBTTT-C16 TFT is investigated by applying forward and reverse sweeps of the gate voltage i.e. from −10 V to +10 V and vice-versa. The results revealed an anticlockwise hysteresis, which shows an increase in off current from 7.7 nA to 10.8 nA and a change in the threshold voltage from −1.5 V to −2.2 V respectively. These changes are thought to be due to the combined effects of unintentional doping effects of oxygen molecules in the atmosphere as well as the migration of the residual dopants/impurities in the semiconductor film retained during fabrication of the devices.

Finally, the disordered model equation developed in chapter 2, is used in further analysing the SAG PBTTT-C16 TFT. Material constants such as *m* and *K* are extrapolated from the intercept and slope of log (dI_{sat}/dV_G') against log (V_G'), and are found to be approximately 0.57 and 2.15×10^{-16} AV^{-m} respectively. This value for *m* leads to a T_C and *MNE* of 473 K and 41 meV respectively. Using these values, the theoretical TFT data is compared to the experimental transfer characteristics using MATHCAD software. Good fits are obtained particularly for voltage values higher than −8 V. However, at lower voltage values, a slight deviation is observed which is attributed to contact resistance effects.

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CHAPTER 5

Design, development and characterisation of organic circuits using a Self-Aligned Gap process

In this chapter, the disordered models demonstrated in chapter 2 are used for designing mixed analogue and digital circuits in Cadence circuit design software. The designed circuits are fabricated using the SAG process developed in chapter 4 and subsequently characterised in ambient conditions. Limitations of the SAG fabrication processes are also discussed in this chapter with possible solutions to fabrication complications presented as well.

5.1 INTRODUCTION

The advancement of the design of organic analogue and mixed signal circuits is increasing in spite of the challenges discussed in Chapter 1.Whilst using CMOS-type technology [1-5] for the design of circuits is advantageous, its realisation in organic technology is fraught by key challenges such as the intrinsic low charge carrier mobility values of both *p*- and *n*- type transistors, the lack of a vast number of air-stable *n*-type organic semiconductors as well as the added complexity of device fabrication of both *p*- and *n*- type semiconductors on the same substrate. The aforementioned issues have thereby resulted in a large number of the current state of the art organic circuits being limited to mostly *p*-type configurations.

The load transistor of *p*-type organic circuits can be implemented using a number of topologies, whereby the most popular ones include: a resistor load [6], a pseudo CMOS load configuration [7,8], a diode-connected/saturated load [9], a zero-V_{GS} load [10-12] and a bootstrapped load [13, 14]. The advantages and disadvantages of these topologies can be understood by comparing their attributes using a simple circuit such as an inverter/amplifier. *Figure 5. 1* below shows inverter configurations using the above-mentioned topologies.

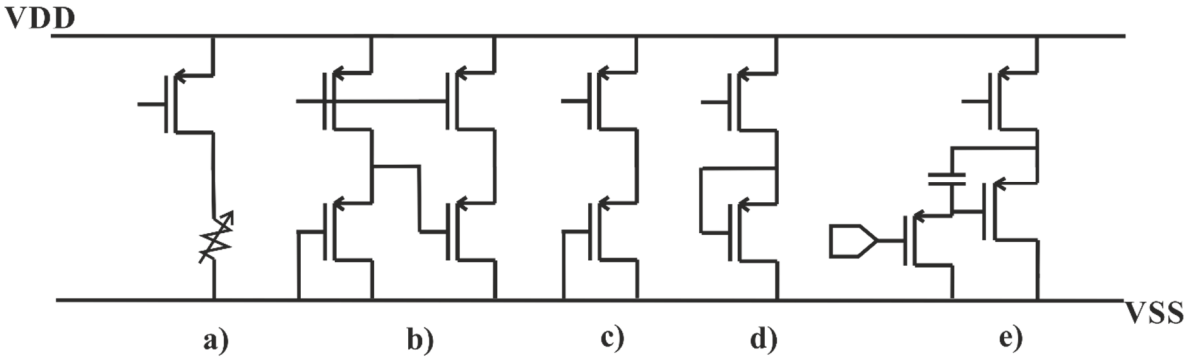

Figure 5. 1: Different inverter topologies using only p-type transistors. From a) to e) the inverter configurations are a resistor load topology, a pseudo CMOS load topology, a saturated load topology, a zero-V_{GS} topology and a bootstrapped topology respectively.

A resistor load configuration, as shown in *Figure 5. 1 (a),* is usually not employed in circuits due to the large area needed for their implementation [15] and their unreliability due to threshold voltage variations. Another approach in organic circuit designs is the pseudo-CMOS design, which consists of two inverters that have their inputs connected to each other, and the output of the first stage is connected to the output of the second stage as shown in *Figure 5. 1(b).* This topology offers good dynamic characteristics and realistic gain values

however at the cost of an increase in the number of transistors resulting in an increase in the circuit area. It also requires a higher power supply for proper functionality resulting in increase in power dissipation [16].

Alternatively, a zero-V_{GS} load configuration consists of a load transistor that has its gate and source connections connected to each other, as shown in *Figure 5. 1(c)*. The output resistance in this case is high resulting in large gain values, however, the impedance of this topology is highly susceptible to threshold voltage variations which subsequently leads to poor matching of devices [15]. Mismatching of devices would in turn prove unfavourable for proper functionality of analogue circuits such as differential amplifiers and operational amplifiers.

On the other hand, a saturated load configuration, which consists of a load transistor that has its drain and gate connected to each other, as shown in *Figure 5. 1(d)*, has a high gate overdrive voltage and is more reliable with regards to threshold-voltage sensitivity in comparison to the zero-V_{GS} load topology [17]. In spite of this advantage, the former has a low gain due to it small output impedance value; however, several techniques can be employed to boost the gain. A circuit that combines the two attributes of the aforementioned topologies i.e. high gain and sufficient reliability, is the bootstrapped load configuration shown in *Figure 5. 1(e)*. It consists of a capacitor connected between the source and gate of the load transistor and a switch connected between the gate and the power supply. In spite of its high gain and good reliability when compared to the zero-V_{GS} topology, the latter may suffer from instability issues as a result of having both a zero and a pole at lower frequencies [15]. Whilst the zero-V_{GS} and the bootstrapped load offer higher gain, a diode load topology is instead adopted for circuit designs in this work to ensure stability and reliability. To circumvent the challenge of low gain associated with this topology, a cascading configuration and cross-coupled inverter topology with positive feedback are some of the methods implemented in the design of analogue circuits in this work to enhance the gain.

The circuit designs in this work are executed in Cadence design software as demonstrated in section 5.2 of this chapter. The disordered TFT model from chapter 2 and the TFT parameters extracted from chapter 4 are used for the circuit designs. Utilising the optimised SAG fabrication process from chapter 4, circuits are fabricated and subsequently analysed in section 5.3. The challenges encountered with the SAG process are discussed and the possible solutions to them are presented in section 5.3.

5.2 MODELLING AND DESIGNING OF ORGANIC CIRCUITS IN CADENCE SOFTWARE

5.2.1 CADENCE DESIGN MODEL

As the field of organic electronics is relatively new, barely any circuit simulating software contain built-in organic models to aid in the design of circuits. Currently, most models used in organic circuit designs are modified models of either silicon based MOSFETs or inorganic TFTs. In this work, the former approach is used with subsequent organic models being created in Cadence circuit simulator (V.5.10). The key parameters that have been modified and adapted for the organic model include the power factor of the drain current, the threshold voltage, the off current value, the dielectric thickness, the contact resistance and the mobility term. The modified model thereby consists of a *p*-type, silicon transistor connected to a voltage controlled current source (VCCS) as shown in *Figure 5. 2* below.

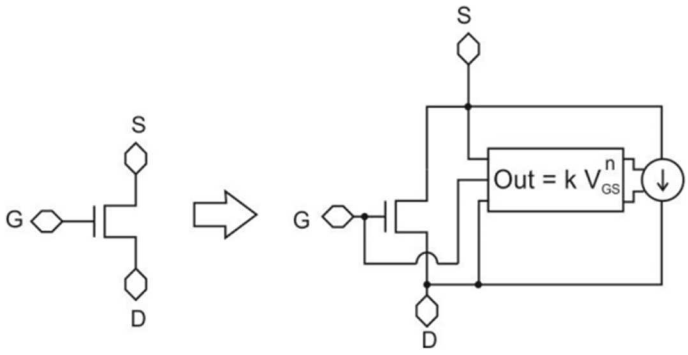

Figure 5. 2: OTFT model consisting of a modified silicon p-type transistor. The new model consists of a VCCS that modifies the drain current expressions of the conventional transistor using a Verilog code.

The purpose of the VCCS is to modify the power factor of the MOSFET linear and saturation current equations to account for the increase in power factor given by *m* (quantifies the degree of energetic disorder) as is commonly observed in the organic TFT current expressions as shown in *equations 2. 50* and *2. 51* . This is executed using a Verilog code, further details of the code can be found in Appendix G. The values of *m* and *K* used for the code are obtained from those extracted from the plot of log (dI_{sat}/dV_G) against log (V_G') of the PBTTT-C16 transistor i.e. *Figure 4. 25* found in chapter 4.

In addition to the Verilog code, the built-in PSpice parameters of the silicon transistor are modified accordingly to reflect the organic transistor parameters. The source and drain contact resistances, R_S and R_D, are modelled using the relation:

$$R_C = \frac{R_{sh}}{W} \qquad 5.1$$

where R_C is the contact resistance, R_{sh} is the sheet resistance and W is the channel width of the transistor.

Gold (Au) metal is used for the source and drain contacts thereby, assuming transistors with channel widths ranging from 8 mm to 90 µm, the estimated values modelled for the contact resistances also range from 300 kΩ to 2.68 Ω.

To set the value of the oxide thickness, an equivalent oxide thickness, t_{OTFT} is found by equating the oxide capacitance, C_{ox}, of a silicon oxide dielectric (SiO_2) to that of the aluminium oxide dielectric (Al_2O_3) used in this work as detailed in *equations 5. 2* and *5. 3* below:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox\_Al_2O_3}}{t_{ox\_Al_2O_3}} = \frac{\varepsilon_0 \varepsilon_{ox\_SiO_2}}{t_{ox\_SiO_2}} \qquad 5.2$$

Making $t_{ox\_SiO_2}$ the subject term,

$$t_{ox\_SiO_2} = t_{OTFT} = \left(\frac{\varepsilon_{ox\_SiO_2}}{\varepsilon_{ox\_Al_2O_3}} \right) t_{ox\_Al_2O_3} \qquad 5.3$$

where $t_{ox\_SiO_2}$ and $\varepsilon_{ox\_SiO_2}$ are the thickness and the permittivity of silicon oxide and $t_{ox\_Al_2O_3}$ and $\varepsilon_{ox\_Al_2O_3}$ are the thickness and the permittivity of aluminium oxide.

Assuming $\varepsilon_{ox\_SiO_2} = 3.9$, $t_{ox\_Al_2O_3} = 50$ nm and $\varepsilon_{ox\_Al_2O_3} = 10$, the value of t_{OTFT} used in the Cadence simulations is therefore set to 19.5 nm.

An effective mobility expression is derived in chapter 2 to account for the mobility dependency on carrier concentration as observed in OTFTs. This is subsequently used for analysis in chapter 4. Given that in silicon equations a single mobility term is used, the average of the effective mobility obtained in chapter 4 is used in the PSpice parameters although it is important to note that the OTFT mobility prefactor value, K, is modelled in the Verilog code. The chosen value for the effective mobility term, μ_0, is 0.1 $cm^2V^{-1}S^{-1}$, which is slightly lower than the average effective mobility. The lower value is chosen for circuit simulations to account for the expected decline in mobility values seen across the substrates when fabricating circuits because of additional processing steps as well as fabricating in ambient conditions.

Lastly, the values of the threshold voltage, V_T and the off current, I_{off} are found from the values extrapolated from the plot of $I_D^{0.5}$ versus V_G and the transfer characteristics plot respectively, as discussed in chapter 4. The values used are, respectively, −1.5 V and 7.7 nA. *Table 5. 1* below gives a summary of the parameters used in the Cadence OTFT model.

Table 5. 1: Summary of the parameters used in the Cadence OTFT model

Parameter	Value	Unit
m	0.57	-
K	2.15×10^{-16}	AV^{-m}
R_C	300×10^3 - 2.68	Ω
t_{ox}	19.5	Nm
μ_0	0.1	cm^2/Vs
V_T	−1.5	V
I_{off}	7.7×10^{-9}	A

Utilising the parameters listed in the previous table, the experimental transfer characteristics of the PBTTT-C16 transistor given in *Figure 4. 24* are compared to the plot of the transfer characteristics of the Cadence OTFT model as shown in *Figure 5. 3* below:

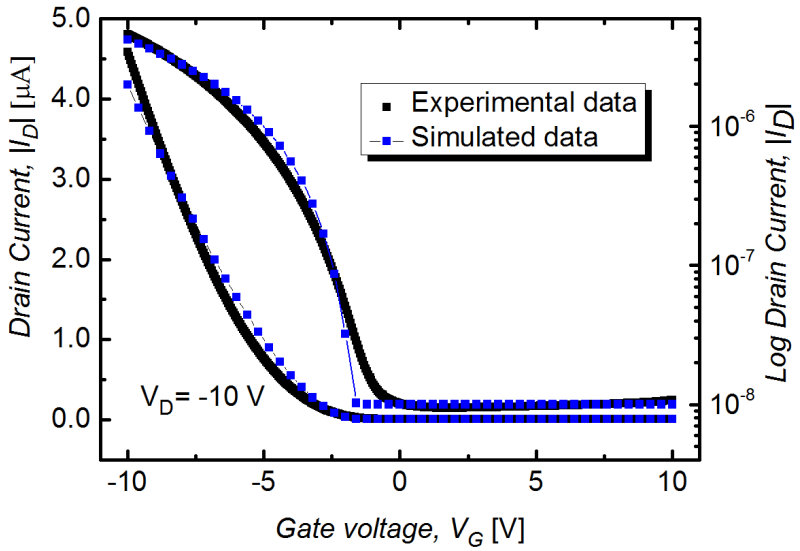

Figure 5. 3: Linear and sub-threshold graphs of the measured and simulated SAG PBTTT-C16 TFT swept from V_G of +10 V to −10 V at a V_{DS} of −10 V. The thickness of the active layer and aluminium oxide dielectric is 65 nm and 50 nm respectively. The aspect ratio of the TFT is 50 (W/L=1000 μm/20 μm).

From *Figure 5. 3*, it is evident that better fits are obtained for gate voltage values less than

−5 V). This is thought to be because of contact resistance effects. Although the contact resistance is included in the PSpice parameters of the silicon transistor, it is believed that better fits to the drain current will be obtained if the contact resistance is modelled into the Verilog code as well.

5.2.2 DESIGN AND SIMULATION OF AN ORGANIC COMPARATOR

♦ **Theory and design of the Organic Comparators**

A comparator is an essential building block of analogue-to-digital converters (ADC), which form an integral part of mixed signal applications such as in smart sensor systems. The conversion of an analogue signal to a digital signal is preferable as digitized signals are less susceptible to spurious signals encountered during routing. A comparator computes the difference between two analogue input signals, V_{inp} and V_{inn}, and produces a digital voltage value, V_{OL} and V_{OH}, which corresponds to a logic 0 and logic 1 respectively. V_{inp}, V_{inn}, V_{OL} and V_{OH} is the positive input voltage, the negative input voltage, the maximum output voltage and the minimum output voltage respectively. *Figure 5. 4* below shows the symbol of a comparator and the ideal transfer curve of a comparator having an infinite gain.

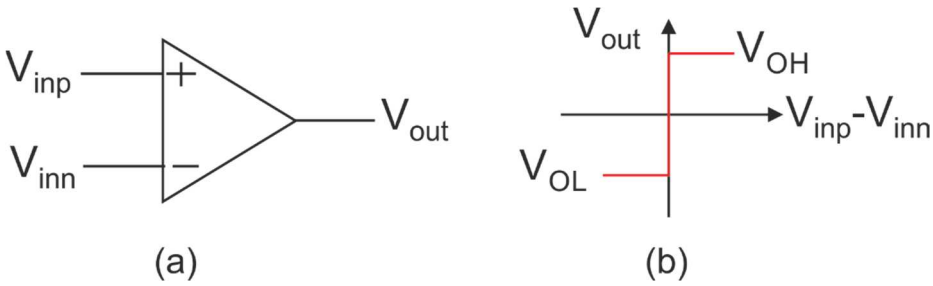

Figure 5. 4: (a) Symbol of a comparator circuit and (b) the ideal transfer curve of a comparator.

A comparator can easily be implemented using a simple amplifier circuit having a moderately high gain, although, more often than not, analogue circuit designers do not chose this option given that the slew rate of an amplifier is limited. Typically, the propagation delay time and subsequently the speed of a comparator changes as a function of the magnitude of the input signal, therefore it follows that to obtain a smaller delay time, a larger input would be needed. In other words, to obtain a fast working comparator, a steady, linear rise in current/voltage would be required, which cannot be achieved using a single amplifier circuit.

This effect can typically be attained using a latch circuit as shown in *Figure 5. 5*, it consists of two cross-coupled inverters.

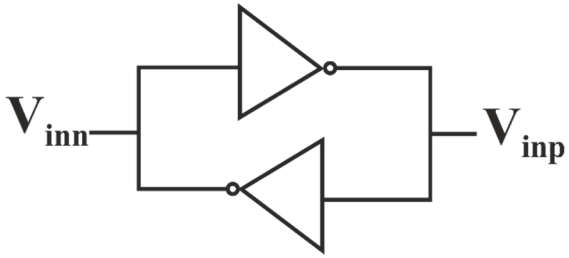

Figure 5. 5: Schematic of a latch consisting of two inverters connected back-to-back in a positive feedback topology.

The aforementioned topology achieves an output voltage that increases exponentially towards the power supply rails, with time, as demonstrated in *equation 5. 4*:

$$\Delta V = \Delta V_0 e^{t/\tau} \qquad 5.\ 4$$

Here,

$$\Delta V = V_{inp} - V_{inn}$$

$$\tau = \frac{C_L}{g_m}$$

where g_m is the transconductance of the inverter driver, C_L is the capacitance at the node of V_{inp} and V_{inn}, ΔV_0 is the initial voltage difference between V_{inp} and V_{inn}, t is the transient time and τ is the time constant.

It therefore follows from *equation 5. 4* that larger values of ΔV_0 result in shorter propagation delays and as such a faster time in reaching the required value of ΔV. In this thesis, comparators consisting of a preamplifier, a latch and a self-biased output stage are designed in Cadence design software using the OTFT model discussed in the previous section. The incorporation of a preamplifier stage before the latch stage is desirable given that it amplifies the difference of the input signals before being fed into the latch which as has been shown is necessary for achieving shorter propagation delay times and hence higher speed. Additionally, this amplification is essential in diminishing any offset brought on by the latch. Given that the gain of a differential amplifier with a single saturated load transistor is relatively small, the preamplifier is designed with saturated cascode load transistors as shown in *Figure 5. 6*. The layout of the same schematic is found in *Figure 5. 7*. A current source consisting of saturated load transistors connected in series is used to bias the differential amplifier via transistor M9

and V_{bias}. The output impedance of the cascaded topology is greater than that of a single saturated load transistor thereby resulting in a higher gain value although this comes at the cost of a reduction of the allowable output voltage swing given that the maximum and minimum output voltage values are dependent on the aspect ratios of the load and driver transistors. The number of cascade load transistors is limited to three since a further increase in the number reduces the output swing without giving considerably larger gain values. The gain in this case takes the form below:

$$|A_V| = \beta_{M1}(V_{GS} - V_T)R_{total} \qquad 5.5$$

where A_v is the differential amplifier gain, β_{M1} is the process transconductance parameter of the driver transistor, *M1*, V_{GS} is the gate to source voltage, V_T is the threshold voltage and R_{total} is the equivalent resistance of the cascaded load transistors i.e. *M4* to *M8*.

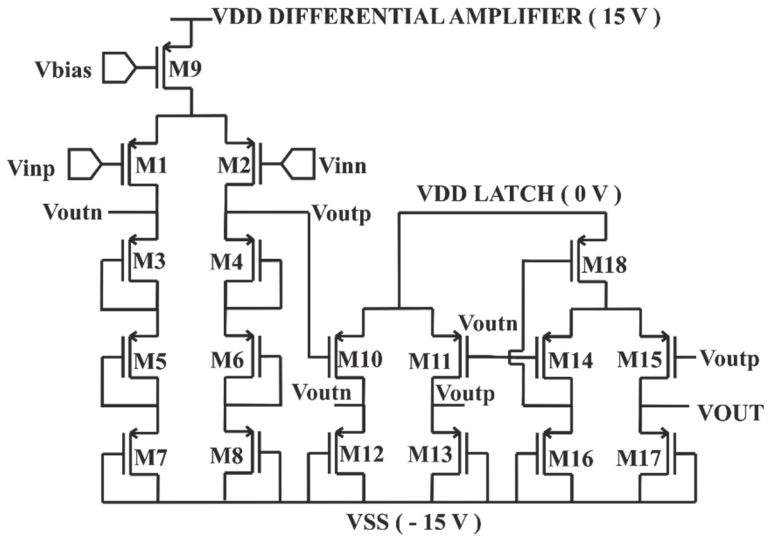

Figure 5. 6: Schematic of the comparator design having a preamplifier consisting of a cascaded differential amplifier, a latch stage consisting of a single set of cross-coupled saturated load inverters and a self-biased differential amplifier for the output stage.

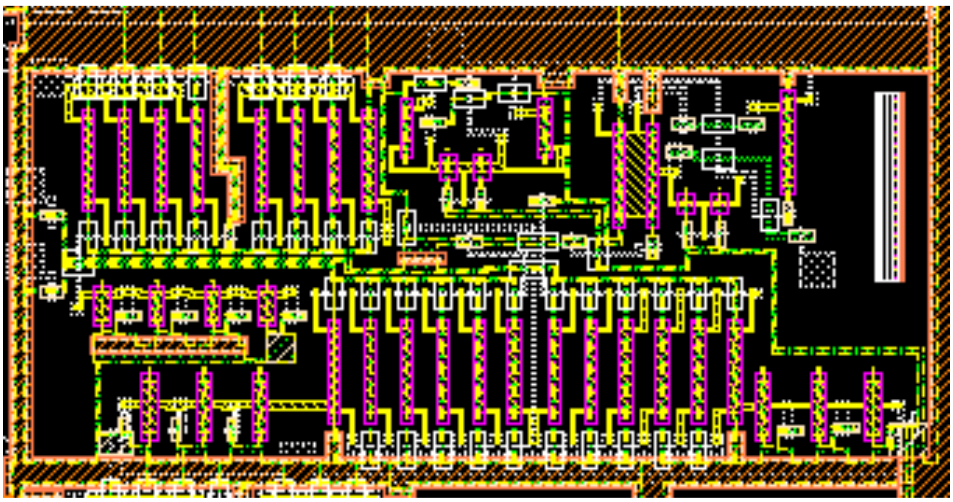

Figure 5. 7: Layout of the schematic in Figure 5. 6 as designed in Cadence design software. Details of the Design Rule Check (DRC) layout rules and the mask containing the layout of the circuit can be found in Appendix H and I respectively.

The latch in this design consists of saturated load inverters which are always operating in regenerative mode given that the comparator is synchronous i.e. clocks are not utilized in the designs. The latch and the output stage also has a lower supply rail value of 15 V to safeguard the transistors in the subsequent sections from breaking down. An additional stage consisting of a self-biased difference amplifier is connected to the outputs of the latch, given that the latch would be insufficient in driving successive stages that may have large output capacitances. Furthermore, this stage adds more gain to the circuit and converts the two output signals from the latch into a single output.

♦ **Simulations of the Organic Comparators**

The DC and transient response of the comparator circuit are done using two different values of the threshold voltage i.e. –1.5 V and –2.5 V, to account for the variation of the V_T values as observed in the PBTTT-C16 transistors fabricated in chapter 4. A DC sweep of – 9 V to +9 V is applied at the V_{inp} of the M1 driver transistor whereas the V_{inn} of the M2 driver transistor is grounded. The values of V_{OL} and V_{OH} obtained from the transfer curve, shown in *Figure 5. 8 (a)* having a V_T of –1.5 V, are –0.6 V and –7.7 V whereas the values of V_{OL} and V_{OH} obtained from the transfer curve having a V_T of –2.5 V are –0.6 V and –6.7 V. This observation is made due to the result of a reduction in the overdrive voltage of the devices having a V_T of –2.5 V, which subsequently leads to a reduction in the current driving capability of the circuit as well as the output voltage swing. Furthermore, the reduced output voltage

swing observed in this comparator is believed to be a result of the high values of V_T and I_{off} currents used in the OTFT model. As it is mentioned before, the high off currents and subsequently low aspect ratios obtained from the PBTTT-C16 transistor in chapter 4 is a result the susceptibility of the polymer to oxygen doping effects. Therefore, the disordered model has to consider this. On the other hand, previous simulations of the same circuit, made using a polycrystalline model with significantly lower off current and threshold voltage values display a much wider output voltage swing with reported V_{OL} and V_{OH} values of – 1.2 V and – 13.9 V respectively [18].

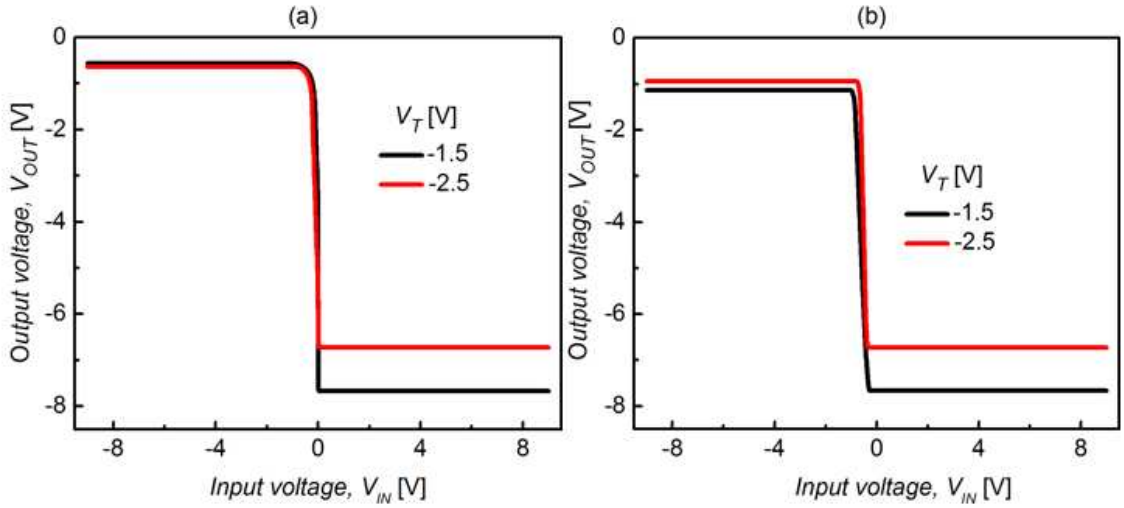

Figure 5. 8: Transfer curves of the output voltage of the comparator connected to a (a) latch stage and (b) one without the latch stage connected. The positive terminal is swept from –9 V to +9 V while the negative terminal is grounded.

In addition, DC gains of 45.62 dB and 35.40 dB are obtained for circuit simulations having a V_T of –1.5 V and –2.5 V respectively. The values of the input offset voltages obtained for the same circuits corresponded to 0.1 V for both circuits. Offsets are expected especially in this design topology given that a saturated load inverter is used for the latch. The Voltage Transfer Curves (VTC) of this type of inverter is usually asymmetric, because of using only *p*-type transistors. The VTC characteristics of this type of inverter will be discussed further in the subsequent sections. Reduction in the offset is attempted by varying the aspect ratio of the inverters in the latch to ensure that the trip point of the inverters coincides with the switching point of the differential amplifier. It is also believed that the contribution made by the latch offset to the overall comparator offset is reduced by the gain of the amplifier. In addition, appropriate aspect ratios of the output stage are chosen to reduce the offsets given that the input

offset is a combination of the offset of the preamplifier, the latch and the output stage as shown in *equation 5. 6*:

$$V_{offset,total} = V_{offset,preamp} + \frac{V_{offset,latch}}{A_V} + \frac{V_{offset,output}}{A_{Vlatch} \cdot A_V} \qquad 5.\ 6$$

where $V_{offset,\ total}$ is the total offset, $V_{offset,\ preamp}$ is the offset of the preamplifier, $V_{offset,\ latch}$ is the latch offset, A_{Vlatch} is the gain of the latch stage and $V_{offset,\ output}$ is the offset of the output stage.

The impact of the latch stage on the output characteristics of the comparator can also be appreciated from the plot in *Figure 5. 8 (b)* which shows the transfer curves of the comparator without the latch. From the graph, the gain values obtained from the comparator without the latch stage is 22.63 dB and 27.31 dB for a V_T of – 1.5 V and – 2.5 V respectively, which is much lower than the values obtained for the latched comparator mentioned in the previous section, further corroborating the added benefit of the latch.

For the transient response simulations, a ± 1 V pulse waveform with a period of 1 ms and rise/fall times of 0.1 ms is applied at V_{inp} whereas V_{inn} remained grounded. The outputs obtained are detailed in *Figure 5. 9*. Propagation delay values of 3.28 ms and 3.4 ms are obtained for the V_T of – 1.5 V and the V_T of – 2.5 V respectively, corresponding to operational frequencies of about 300 Hz. The resolution of the comparator is also found to be 0.1 V and 0.3 V for the V_T of – 1.5 V and the V_T of – 2.5 V respectively.

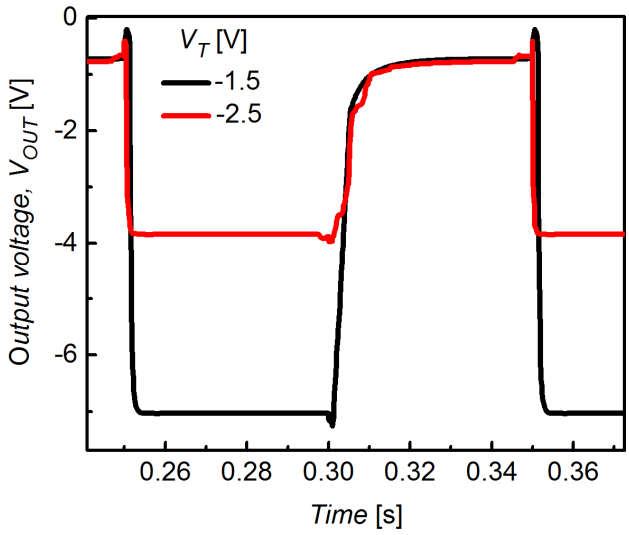

Figure 5. 9: Transient response of the comparator with an input pulse of ± 1 V, period of 0.1 ms and rise/fall times of 0.01 ms. The input is applied to the input voltage (on the positive terminal) while the negative terminal is grounded.

A circuit containing two additional inverters in the latch stage, as shown in *Figure 5. 10* is also designed.

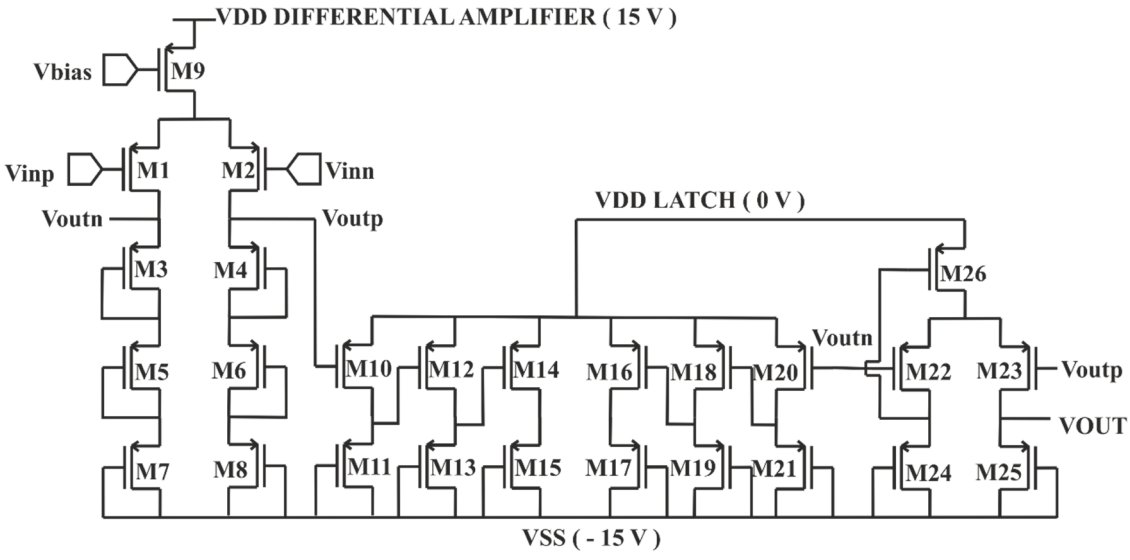

Figure 5. 10: Schematic design of the comparator circuit having two additional inverters at the latch stage.

Similar to the previous sections, the DC and transient analysis are investigated as shown in *Figure 5. 11*. The minimum and maximum output voltage of this design is found to be –3.9 V and –7.7 V for a V_T of –1.5 V. The input offset voltage and the open loop DC gains are

found to be –0.2 V and 11.6 dB respectively. The overall reduction in gain in comparison to the previous design is attributed to the reduction in the output voltage swing given that the gain is proportional to the output voltage range. The propagation delay and resolution of the second circuit design is 13.0 ms and 0.5 V. The overall delay of this comparator increases because of the additional propagation delay associated with the inverter stages added to the latch. *Table 5. 2* shows a summary of the DC and transient characteristics of the two comparator circuits whereas *Table 5. 3* shows a summary of the values of the device parameters.

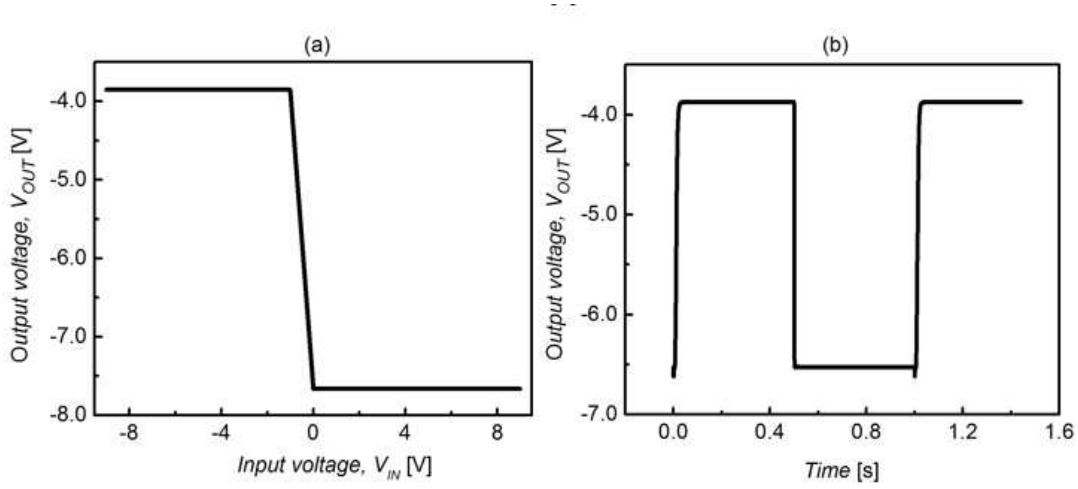

Figure 5. 11: (a) Transfer curves of the output voltage of the comparator having two additional inverters at the latch stage. The positive terminal is swept from –9 V to +9 V while the negative terminal is grounded. (b) Transient response of the same inverter. The input pulse has a magnitude of ±1 V, period of 1 s and rise/fall times of 1 ms. The input is applied to the input voltage (on the positive terminal) while the negative terminal is grounded.

Table 5. 2: Summary of the DC and transient properties of the two comparators designed in this thesis.

Comparator schematic	*Figure 5.6*		*Figure 5.6*		*Figure 5.10*	
Threshold voltage (V)	– 1.5		– 2.5		– 1.5	
Current consumption (nA)	861.7		726.0		861.7	
Supply rails (V)	± 15		± 15		± 15	
Input offset voltage (mV)	10.0		10.0		– 212.0	
DC Output voltage swing (V)	V_{OL}	– 0.6	V_{OL}	– 0.6	V_{OL}	– 3.9
	V_{OH}	– 7.7	V_{OH}	– 6.7	V_{OH}	– 7.7
DC Gain (dB)	45.6		35.4		11.6	
Resolution (V)	0.1		0.3		0.5	
Propagation delay (ms)	3.28		3.4		13.0	
Operational frequency (Hz)	294.1		304.9		76.9	

Table 5. 3: Summary of the device dimensions of the comparators designed in this work.

Comparator schematic	*Figure 5.6*		*Figure 5.10*	
Current source	Width of transistors (µm)	300		300
Current mirror	Width of M9 (mm)	4		4
Pre amplifier stage	Driver width (mm)	6		8
	Load width (µm)	550		650
Latch stage	Aspect ratios (S)	750/90	S_1	200/20
			S_2	300/60
			S_3	450/100
Output stage	Driver width (mm)	1		1
	Load width (µm)	50		5
	Width of M18/M26 (mm)	1		1
*Channel length (*µm)	20		20	

5.3 CHARACTERISATION OF SAG ORGANIC CIRCUITS

5.3.1 FABRICATION METHODOLOGY

Figure 5. 12 below shows a structure of a circuit block typically made using the planar SAG process. The source and drain contacts comprise of gold (Au) electrodes, whilst the gate contact consists of aluminium (Al) electrode. The gate oxide constitutes of aqueous anodised aluminium oxide (Al_2O_3) and the *p*-type semiconductor is PBTTT-C16. P3HT polymer is also used occasionally for comparison purposes.

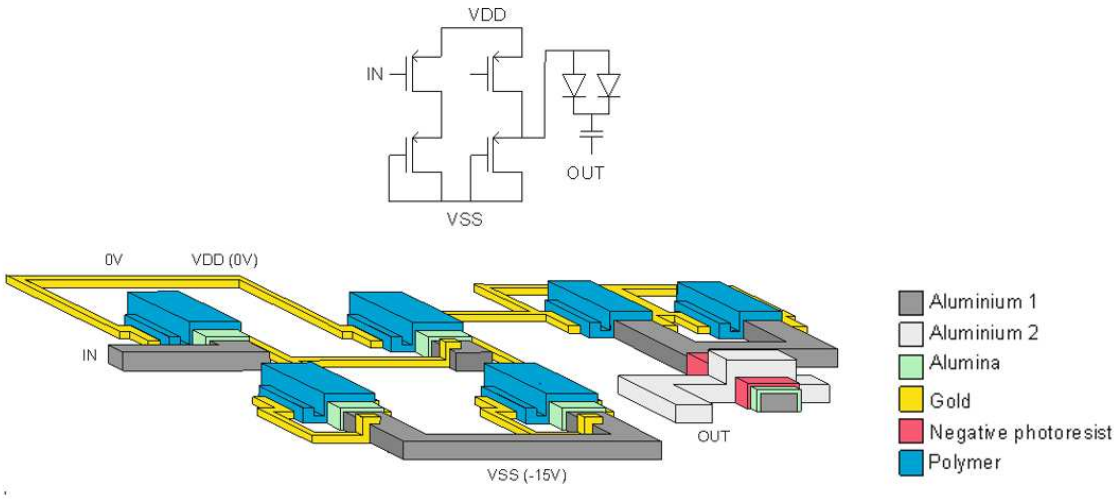

Figure 5. 12: Structure of prospective circuit blocks and lateral devices processed on the same substrate, at the same time using the SAG fabrication process.

The procedures involved in the development of the SAG circuit are explained further in the following section and demonstrated graphically in *Figure 5. 13*. The processing steps

involved in defining the source, drain, gate contacts and gate oxide (steps 1 to 5), are as discussed in *section 4.2.1* and *4.3.1* of the lateral diode section and self-aligned TFT section respectively as outlined in chapter 4. In this section, a brief overview of the formation of the crossover structures as well as the formation of the top metal contact for interlayer connections is presented.

1. *Glass cleaning*: Same process as described for "glass cleaning" in *section 4.2.1*
2. *Gate contact patterning and gap formation:* Similar to "Al patterning and gap formation" in *section 4.2.1*
3. *Source/Drain formation:* Akin to "Au patterning" in *section 4.2.1*
4. *Dielectric growth:* Exact process as "Gate oxide formation" in *section 4.3.1*
5. *Al etch:* Same process as described for "Al etch" in *section 4.3.1*
6. *SU8 crossover.*

This mask layer defines the areas where crossover structures are produced.

- A negative image resist (SU8 2000.5) obtained from A-Gas Electronic Materials, UK, is spun on the circuit samples at 3000 rpm for 30 seconds, followed by a post application bake (PAB) for 90 seconds at 110 °C on a hotplate as shown in *Figure 5. 13 (u).*
- The resist-coated samples are then exposed to ultra-violet (UV) light through a chromium-coated mask containing the crossover pattern layout as demonstrated in *Figure 5. 13 (v).*
- The exposed samples are subsequently baked at 110 °C for 120 seconds and left to cool down to room temperature on a glass slab for about an hour.
- The cooled samples are developed in Ethylene carbonate (EC) solvent for 60 seconds. EC solvent is a negative photoresist developer solution, which is procured from A-Gas Electronic Materials, UK. The samples are later rinsed thoroughly in propanol for a further 60 seconds and later dried with a nitrogen gun.
- The samples are cured at increasing temperatures of 70 °C, 100 °C, 130 °C, and 160 °C for 5 minutes with a 10 minute interval between each curing step as shown in *Figure 5. 13 (w).* The last step consists of a further curing step at 210 °C for 30 minutes to ensure proper adhesion of the cured crossover structures onto the sample. Failure to cure at the specified elevated temperature results in peeling off the SU8 layer as will be demonstrated in *section 5.3.2.*

7. Aluminium (2) contact formation.

This layer defines areas where contact between gold (source/drain) and (gate) aluminium is required as well as completing crossover structures.

- A positive image resist (HPR 504) is spun on the samples at 3000 rpm for 45 seconds, followed by soft baking of the samples at 110 °C for 90 seconds on a hotplate as in *Figure 5. 13 (x).*
- The resist-coated samples are then exposed to ultra-violet (UV) light through a chromium-coated mask containing the aluminium layer pattern/layout as shown in *Figure 5. 13 (y).*
- The exposed samples are then developed in HPRD 429 developer for 45 seconds. The samples are then rinsed in deionised water and dried with a nitrogen gun as demonstrated in *Figure 5. 13 (z).*
- The samples are left in an oven set at 100 °C for 30 minutes to evaporate any residual water droplets on the samples. A light oxygen plasma treatment for 30 seconds at an RF power of 15 watts is subsequently performed on the samples to roughen the samples to ensure the subsequent Aluminium layer sticks well to the sample.
- A 100 nm thick Al layer is thermally evaporated onto the samples at a rate of 4 Å/s at a pressure of 1.96×10^{-7} mTorr as shown in *Figure 5. 13 (a.a).*
- After evaporation, the samples are immersed in a beaker of 80 °C heated micro-stripper solution (photo resist remover), in order to lift-off the resist as well as the unwanted Al layer as indicated in *Figure 5. 13 (a.b).* The samples are rinsed thoroughly in deionised water, dried with a nitrogen gun and cleaned using UV-radiation to remove residual resist contaminants in preparation for polymer deposition in the next step.

8. Polymer deposition: In this section, two different polymers are used to define the active area as demonstrated in the following steps.

- PBTTT-C16 polymer - Same process as described for "Polymer deposition of PBTTT-C16" in *section 4.3.1* and as demonstrated in *Figure 5. 13 (a.c).*

- Poly 3-hexylthiophene (P3HT) polymer– Used for characterising and comparing the mobility and speed performance of the inverters relative to the devices and circuits made using PBTTT-C16.

  Prior to deposition of the P3HT polymer, the substrates are briefly exposed to oxygen plasma, followed by the formation of a self-assembled monolayer (SAM) using hexamethyldisilazane (HMDS) purchased from Alfa Aesar. The SAM layer is formed by spin coating the HMDS solution at a 3000 rpm for 45 seconds onto the sample followed by annealing on a hotplate at 70 °C for 300 seconds. This improves the adhesion of the polymer onto the sample thereby enhancing molecular ordering of the polymer on the samples. P3HT obtained from Ossila Limited, UK is then dissolved in hot (100°C) toluene solvent. The solution is left to mix thoroughly with a magnetic stirrer, on a hot plate, for three hours. While still hot, the solution is then spun on the samples at 1000 rpm for 45 seconds, which results in a film thickness of about 70 nm. The films are subsequently annealed at 110 °C for 10 minutes. The samples are left in vacuum overnight prior to electrical characterisation.

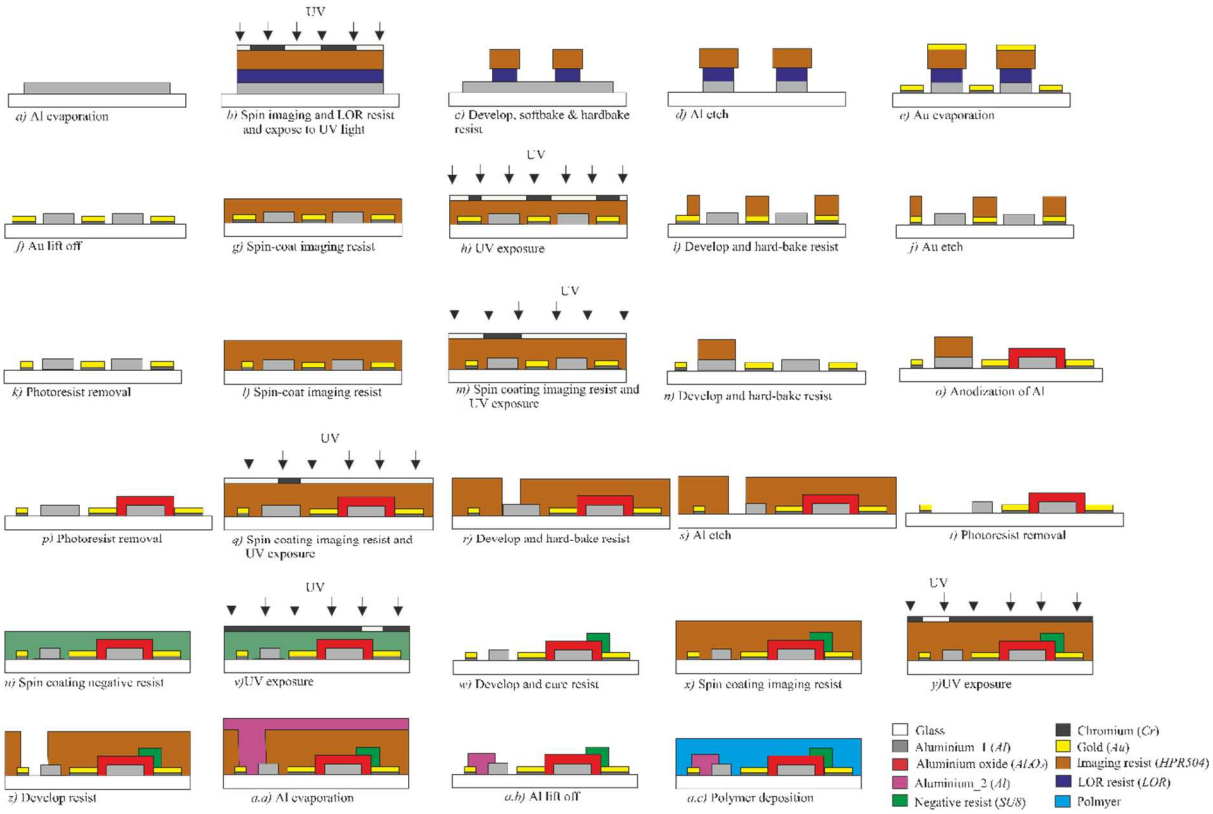

Figure 5. 13: Summary of the SAG fabrication process.

5.3.2 RESULTS AND ANALYSIS

The fabrication of SAG circuits using the processes outlined in the previous section is carried out and the results will be elaborated further in the following section. The design and modelling of the circuit is done using Cadence Virtuoso software as mentioned in *section 5.2.1* whereas the DC characterisation of the circuits is carried using a Keithley semiconductor system in dark, ambient conditions. Alternating current (*AC*) and transient measurements of circuits are executed using a set-up equipment consisting of an Agilent 33220A signal waveform generator connected to a Falco Systems Model WMA01 high voltage amplifier and two power supply units connected to the circuit under test. The input signal comprises of a 15 V peak to peak step signal with varying values of frequency whereas the output is measured using an Agilent 54621D oscilloscope. The output is connected to the oscilloscope via a buffer amplifier to reduce loading effects from the oscilloscope.

♦ **Analysis of circuits made using the SAG process**

Nonetheless, a saturated *p*-type load inverter is successfully fabricated and analysed. Given the simplicity of the inverter topology, it is imperative for any future fabrication design prospects to at least demonstrate a working inverter as the initial step to realising organic integrated circuits. On the other hand, the realisation of the organic comparators designed in *section 5.2.1* is futile because of the challenges faced with the SAG process that will be discussed in the succeeding section. In this section, the saturated *p*-type inverters are characterised. The operation of a *p*-type saturated load inverter can be described as follows: when the driver transistor is off, the output of the inverter is a logic level_1 and is determined by the leakage current of the continuously on load transistor. In this case, the high output voltage takes the form given in *equation 5. 7* below:

$$V_{OH} \cong V_{SS} - V_{T\_L} \qquad 5.\ 7$$

where V_{OH} is the high output voltage, which corresponds to a logic level 1, VSS, is the power rail and V_{T_L} is the threshold voltage of the load transistor.

Conversely, when both the driver and load transistor are on, logic level_0 is registered. The output voltage in this case is determined by the aspect ratios, W/L of the driver and load transistor as illustrated using *equation 5. 8* below:

$$V_{OL} \cong (V_{SS} - V_T) - \frac{V_{SS} - V_T}{\sqrt{1 + (\beta_L / \beta_D)}} \qquad 5.8$$

where V_{OL} is the low output voltage, which corresponds to a logic level 0, VT, is the threshold voltage, which is assumed equal for both of the transistors, and β_L and β_D are the transconductance parameters of the load and driver transistor.

The Voltage Transfer Curve (VTC) graph of a saturated load inverter made using the SAG process is as shown in *Figure 5. 14*.

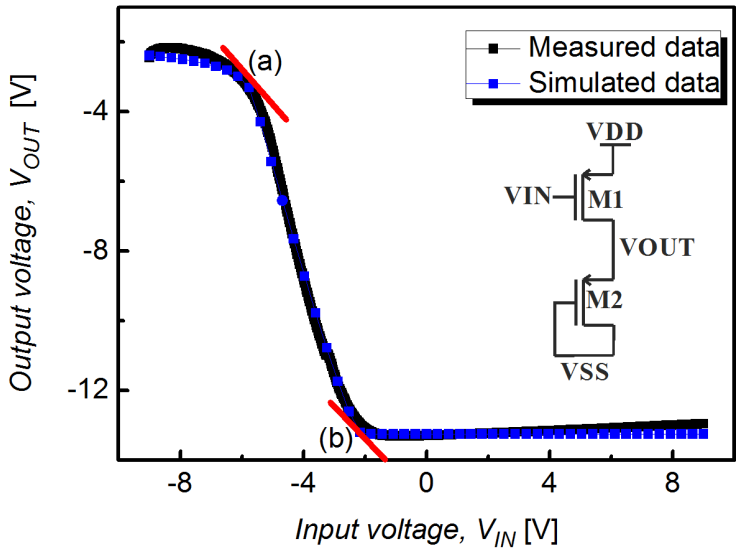

Figure 5. 14: The measured and simulated Voltage Transfer Characteristics of a saturated load inverter (inset) made using PBTTT-C16 polymer. The values of V_{DD} and V_{SS} are 0 and −15 V whereas the input voltage is swept from −9 V to +9 V. The channel length, L = 20 µm, is the same for all the transistors whereas the width of the driver (W_D) and the width of the load (W_L) are 500 µm and 90 µm respectively.

The experimental values of V_{OL} and V_{OH} values are found to be −2.2V and −13.3 V respectively whereas the simulated values are −2.18 V and −13.25 V respectively. The gain of the inverter is obtained from the derivative of the VTC plot and is found to be 12.4 dB, which is slightly higher than the simulated gain, which has a value of 10 dB. The lower gain for the simulated inverter could be because of underestimating the transconductance values of the transistors. To

get a better understanding of the effect of the transconductance values on the gain of the inverter, the theoretical gain of the OTFT is derived as shown in the ensuing sections. The small-signal DC gain, A_V, of an organic saturated load inverter takes the form:

$$A_V = -g_{M1} R_{load} \qquad 5.\ 9$$

Here,

$$R_{load} = \left(\frac{1}{g_{M2}}\right) \| r_{01} \| r_{02} \qquad 5.\ 10$$

$$A_V = -g_{M1}\left[\left(\frac{1}{g_{M2}}\right) \| r_{01} \| r_{02}\right] \cong -\frac{g_{M1}}{g_{M2}} \qquad 5.\ 11$$

where g_{M1} and g_{M2} is the small-signal transconductance of the driver and load OTFTs (M1 & M2), R_{load} is the total load resistance, r_{01} and r_{02} are the output resistances of the driver and load transistor (M2) respectively.

The expression for g_{M1} below can be found by finding the derivative of the saturation drain source current given by equation *2. 51*:

$$g_M = \frac{\partial I_{DS}}{\partial V_G} = \frac{K \cdot W \cdot C_{ox}^{2m+1} \left(V_{GS} - V_T\right)^{2m+1}}{L \cdot (2m+1) \cdot \left(2\varepsilon_0 \varepsilon_r T_C k\right)^m} \qquad 5.\ 12$$

Given that the channel length of the driver and load transistors are the same in this work and assuming that the process parameters of the two are equal, the small-signal DC gain finally takes the form:

$$\frac{g_{M1}}{g_{M2}} = \frac{W_{M1} \cdot \left(V_{GS} - V_{T\_M1}\right)^{2m+1}}{W_{M2} \cdot \left(V_{GS} - V_{T\_M2}\right)^{2m+1}} \cong \frac{W_{M1}}{W_{M2}} \qquad 5.\ 13$$

Equation 5. 13 suggests that the gain is determined by the device dimensions, the degree of disorder of the polymer and the overdrive voltage thereby for higher gain values, larger aspect ratios and larger overdrive voltages would be needed. Increasing the gain by these means

would however result in limiting of the allowable output voltage swing thereby providing unfavourable dynamic response characteristics of the inverter.

An inverter is also typically characterised by its noise margins, which essentially describes the tolerance level of the inverters to spurious signals occurring at the input before its operation becomes corrupted/incorrect [19]. Generally, positive noise margins are required for proper functionality of an inverter. The noise margin high, NM_H and noise margin low NM_L are typically described using the equations below:

$$NM_H = V_{OH} - V_{IH} \qquad 5.14$$

$$NM_L = V_{IL} - V_{OL} \qquad 5.15$$

where V_{OH} is the high output voltage when the input voltage is equal to zero/V_{DD}, V_{OL} is the low output voltage when the input voltage is equal to V_{SS} and V_{IH} and V_{IL} are the high input voltage and the low input voltage extracted from the VTC of the inverter where the gradient of the curve is equal to −1 V/V.

In an ideal inverter, NM_H and NM_L are typically equal to $V_{SS}/2$ respectively; thereby the sum total of the two can never exceed the power supply rails. The NM_H and NM_L of the aforementioned inverter is found to be 7.2 V and 0.05 V respectively which means that in an example of a worst-case situation, a low output from the inverter may not be sufficient to drive subsequent inverter stages connected to this inverter leading to a degraded dynamic response. The poor noise margins are attributed to the asymmetry of the VTC of the *p*-type only technology employed in this work. The use of a large driver width relative to the load in order to obtain higher gain margins contributes to the aforementioned characteristics. Furthermore, the asymmetry is also associated with the switching point of the inverter, which is dependent on the ratio of the threshold voltage of the driver and load transistors. By incorporating a level shifter [20] at the front of the saturated load inverter, the switching point and VTC can be centred and the noise margins can be improved. However, this comes at the expense of an increase in circuit complexity due to the need for an extra power supply, increase in the circuit area and lastly significant power dissipation owing to the large amount of current flowing in the branch of the level-shifter.

Another means authors have tried to improve the asymmetry of the VTC characteristics is by using a dual-gate enhanced logic [21] which essentially entails using a top-gate bias, V_{bg}, on the driver transistor to vary the threshold voltage of the pull up transistor. Using this technology, slightly improved noise margins have been recorded for saturated load inverters, although using two sources of power [22]. Unfortunately, V_{bg} values greater than the power supply are required to achieve symmetry thereby resulting in a larger power consumption. Moreover, the overdrive of the pull up TFT is reduced thereby resulting in slower pull-up times.

Variations in the threshold voltage and mobility values of the transistors of the same inverter can affect the noise margin of an inverter as well. A patterned growth of the active layer [23] can however mitigate the spreads in variations. In this work, it is believed that the use of a polymer with a good structural 2D motif such as PBTTT-C16 reduces the variations. As mentioned in chapter 3, the PBTTT-C16 polymer is well ordered because of interdigitating of its alkyl side chains via thermal annealing which facilitates a closer π-π stacking motif. To further enhance charge transport, it is more advantageous to use a flow coating technique [24] to align the nano fibrils of the polymer along the channel length of the transistors as demonstrated by work carried out by DeLongchamp et al., using the same polymer.

Table 5. 4 below gives a literature summary of the dynamic response characteristics of inverters made using the same polymer with different load topologies i.e. saturated load topology [25], CMOS topology [26-28] and resistive load topology [29].With the exception of [28-29], most of the published devices as well as the inverter in this work, operate at high power supply rail values i.e. > 5 V so as to compensate for the semiconductor mobility. The inverter in this work has a moderate gain on 12.4 dB whilst other authors have gain values ranging from 16 dB to 32.5 dB. It is not easy to use the gain as a figure of merit in quantifying the performance of this inverter relative to the others given that the gain is affected by the aspect ratios of the driver and load transistors as demonstrated in *equation 5. 13*. In addition, out of all the five published inverters, only Baklar et al., gives the dimensions of the transistors used in making the saturated load inverter. The aspect ratios of the driver and the load transistor are 20 mm/20 µm and 2 mm/5 µm respectively, which visibly translates to a higher gain value in comparison to the inverter made in this work. On the other hand, the noise margin values would give a reasonable measure of the quality of robustness of the inverters to spurious signals. Luzio et al., report NM_H and NM_L values that are 28 % of the power supply rail whereas the inverter in this work has NM_H and NM_L values that are 48 % and 0.3 % of the power supply

rail values. The latter inverter has a better noise tolerance for high voltage values but a very poor tolerance for the lower voltage values. The unbalanced noise margin values arise because of the asymmetry of the VTC of the *p*-type only technology, which are because of using large driver width to obtain high gain values.

Table 5. 4: A comparison of the dynamic parameters of inverters made using PBTTT-C16 polymer.

Circuit topology	**Power supply (V)**	**NM_H (V)**	**NM_L (V)**	**Gain (dB)**	**References**
Saturated load	40			16	M. Baklar, P. H. Wobkenberg, D. Sparrowe, M. Goncalves, I. McCulloch, M. Heeney, T. Anthopoulos and N. Stingelin [25].
CMOS	50			12	W. Huang, J. C. Markwart, A. L. Briseno and R. C. Hayward [26].
CMOS	20			32.5	Y. Hu, C. Warwick, A. Sou, L. Jiang and H. Sirringhaus [27].
CMOS	5	1.4	1.4	1.5	A. Luzio, F. G. Ferré, F. D. Fonzo and M. Caironi [28].
Resistive load	5			2	Y.-Y. Noh, N. Zhao, M. Caironi and H. Sirringhaus [29].
This work	15	7.2	0.05	12.4	

The transient analysis of the same inverter is also carried out and the plots of the result are as shown in *Figure 5. 15*. An input pulse with a frequency of 1 Hz is preferred for the extraction of the relevant transient parameters given that the output response of the inverter becomes less stable and attenuates with increase in the input frequency as demonstrated in *Figure 5. 15 (a)* to *(d)*. As can be seen, the V_{OH} signal drops from −13.25 V to −7.16 V with an increase in frequency from 1 Hz to 100 Hz. Similarly, V_{OL} also drops from −1.72 V to −2.95 V with the same increment of frequency.

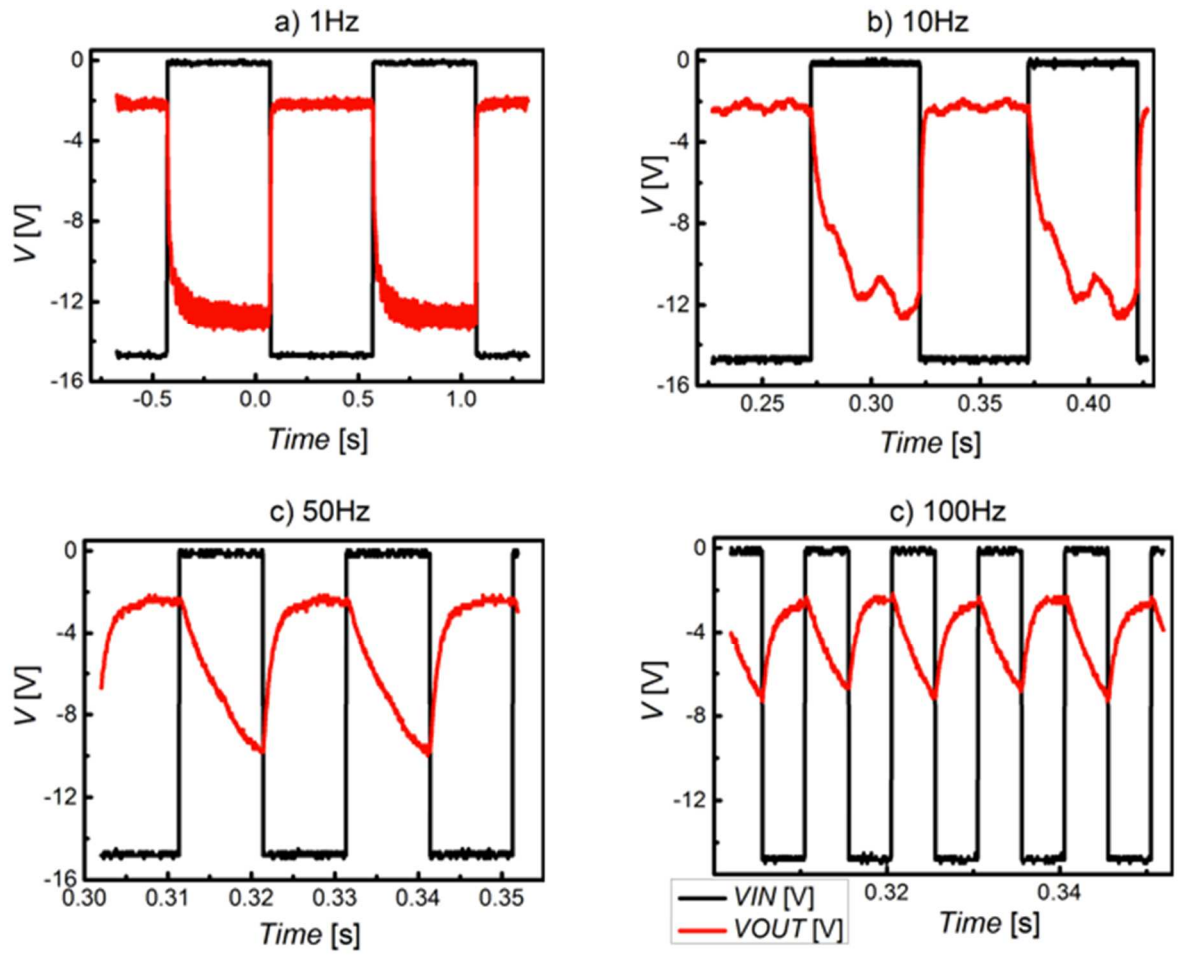

Figure 5. 15: Transient response of a saturated load inverter with PBTTT-C16 polymer as the active layer. The frequency of the step pulse applied at the input terminal is varied from 1 Hz to 100 Hz as shown in the figure from a) to d). The magnitude of the step pulse is 15 V.

The fall time i.e. the time it takes for the output response to drop from 90% to 10% of the logic 1 level, is found to be 5.1 ms. The fall time in this circuit topology is determined by the time required to discharge the load capacitance as demonstrated in *Figure 5.16*. The current available to the capacitive load during this time is supplied from the driver transistor, although the load device uses some of it up. To make a comparison of the experimental values obtained for the fall time to the ones obtained from the simulated results, a value for the load capacitance would need to be estimated. The load capacitance for the fall time is estimated in the following section using the schematic shown in *Figure 5.16*.

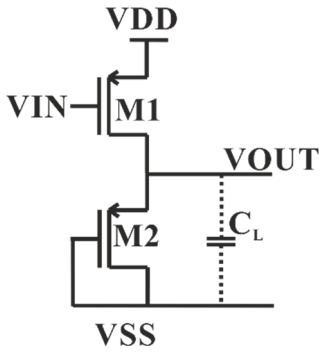

Figure 5. 16: Structure of the saturated load inverter circuit used for the estimation of the load capacitance.

As the input of the driver goes from logic 0 to 1 i.e. (0 to −15 V), the output goes from high to low. The load capacitance that is associated with the fall time comprises of the gate to drain charge, C_{GD}, of the driver transistor (M1), the gate to source capacitance, C_{GS}, of the transistor in the next stage (M3), the C_{GS} of the saturated load transistor (M2) and the capacitance associated with the buffer amplifier, C_{buffer}. The equations for these capacitances are as shown below:

$$C_{GD\_M1\_linear} = 2\left(C_{ox} \cdot LD \cdot W_D\right) + \left(1/2\right) C_{ox} \cdot L \cdot W_D \qquad 5.\ 16$$

$$C_{GD\_M1\_sat} = C_{ox} \cdot LD \cdot W_D \qquad 5.\ 17$$

$$C_{GS\_M2} = C_{ox} \cdot LD \cdot W_L + \left(2/3\right) C_{ox} \cdot L \cdot W_L \qquad 5.\ 18$$

$$C_{GS\_M3} = C_{ox} \cdot LD \cdot W_D + \left(1/2\right) C_{ox} \cdot L \cdot W_D \qquad 5.\ 19$$

where $C_{GD\_M1\_linear}$ consists of the gate to drain capacitance of the driver transistor, M1, in the linear regime and the associated Miller capacitance due to the input switching from low to high and the output switching from high to low, $C_{GD\_M1\_sat}$ is the gate to drain capacitance of the driver transistor, M1 in the saturation regime, C_{GS_M2} is the gate to source capacitance of the M2 transistor, C_{GS_M3} is the gate to source capacitance of the driver transistor in the next stage, M3, LD is the overlap length of the source/drain contacts over the gate contacts, W_D is the

driver width of M1 and M3 assuming W_{M1}=W_{M3}= W_D, W_L is the width of the M2 transistor and L is the channel length which is the same for all the transistors.

Given that a SAG process is used to make the inverters, it is therefore assumed that LD is equal to zero. Therefore, the total load capacitance of the fall time, C_f is given by *equations 5. 20* and *5. 21* where C_{f_lin} is when the M1 driver transistor is in the linear regime and C_{f_sat} is when the M1 driver is saturated.

$$C_{f\_lin} = C_{ox}W_D L + \frac{2}{3}C_{ox}W_L L + C_{buffer} \qquad 5.\ 20$$

$$C_{f\_sat} = \frac{1}{2}C_{ox}W_D L + \frac{2}{3}C_{ox}W_L L + C_{buffer} \qquad 5.\ 21$$

By including the value for C_{buffer}, the values of C_{f_lin} and C_{f_sat} are found to be 159 pF and 151 pf which corresponds to a simulated fall time value of 1 ms which is close enough to the experimental value obtained of 5.1 ms. The higher experimental fall time is a result of the decline in the effective mobility of the circuit given that the circuits are characterised in air rather than in a nitrogen-filled glove box. The transient response of the simulated data is shown in *Figure 5. 17* below.

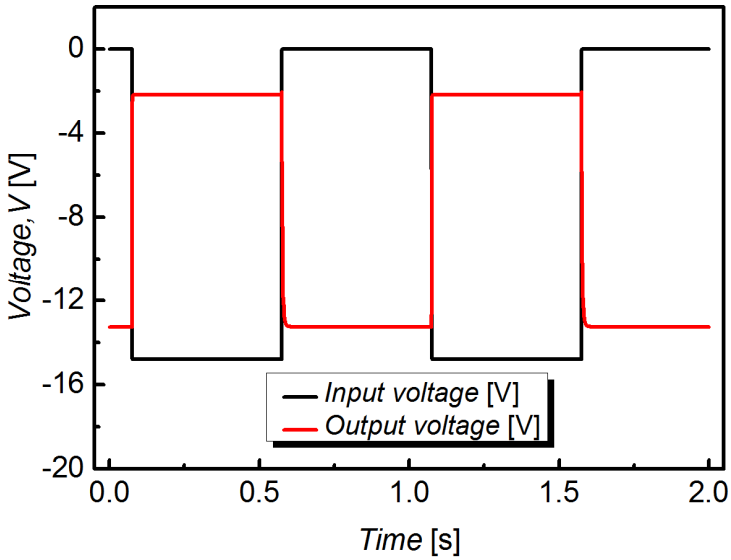

Figure 5. 17: The simulated transient response of a saturated load inverter. A 1 Hz step pulse with a magnitude of 15 V is applied at the input terminal.

Similarly, the rise time i.e. the time it takes for the output response to increase from 10% to 90% of the logic 1 level, is found to be 19.9 ms. The rise time is determined by the rate at which the saturated load transistor sinks all of the current from the driver transistor. In other words, the driver can be seen as a constant current source for the load transistor to charge the capacitive load. Given that the aspect ratio of the load device is smaller than the driver transistor, the rise time would be expected to be greater than the fall time as observed from the experimental results.

An estimation of the load capacitance can be derived for the rise time. The load capacitance for the rise time comprises of the C_{GD} of the M1 driver transistor as given in *equation 5. 17*, the associated Miller capacitance due to the input switching from high to low and the output switching from low to high, the C_{GS} of M2 as given in equation *5. 16* and C_{buffer}.

The total load capacitance associated with the rise time, $C_{r,}$ can therefore be found from the sum total of the aforementioned values. The theoretical value of C_r is 162.8 pF, which is slightly larger than the capacitance for the fall time. The simulated rise time value is found to be 4.2 ms, which is also close enough to the experimental value. The average propagation delay, t_p, of the measured inverter is found to be 3.4 ms corresponding to an operational frequency of 292 Hz. Similarly, the t_p of the simulated inverter is found to be 0.6 ms corresponding to an operational frequency of 1670 Hz; the higher average propagation delay obtained from the measured inverter is because of a decline in the effective mobility of the devices as they are measured in ambient conditions. Another possible explanation for the difference in the operational frequency could be because of underestimating the channel length of the device in device simulations. In the simulated device, a fixed channel length of 20 µm is set however, in the making of the actual device, a variation in the undercut size could occur as discussed extensively in *section 4.2.1* of chapter 4, which subsequently results in variation of the channel length values. In this case, it is plausible that a larger channel length is fabricated thereby resulting in a reduction in the speed of the inverter circuit. A summary of the experimental and simulated inverter characteristics is given in *Table 5. 5* below.

Table 5. 5: Summary of the DC and transient properties of the experimental and simulated inverters made using PBTTT-C16 polymer.

Parameters	**Experimental Values**	**Simulated Values**
Power supply (V)	15	15
Gain (dB)	12.4	10
DC: V_{OL} (V)	- 2.2	- 2.3
DC: V_{OH} (V)	- 13.3	- 13.25
Transient: V_{OL} (V)	- 1.7	- 2.18
Transient: V_{OH} (V)	- 13.4	- 13.25
t_r (ms)	19.9	4.2
t_f (ms)	5.1	1.0
t_p (ms)	3.4	0.6
Operational frequency (Hz)	292	1670

It is important to note that the estimation of the load capacitance in this work did not take into account the junction capacitance found between the source and the gate contact. Typically, when a TFT is on, the source terminal is grounded while the drain terminal is forward biased. A depletion layer therefore exists under the source contact due to the difference in the work function of the metal and the semiconductor (0.2 eV) as has been discussed extensively in the last three chapters. For a saturated load inverter, the gate to drain bias is kept constant; hence, the barrier height of the junction is kept constant. However, by fluctuating the gate to source potential in the load device, the amount of charge entering the transistor fluctuates and so does the potential barrier. Subsequently, there is a fluctuating charge on the source contact side, which is effectively mirrored by fluctuating charge on the gate as well thereby resulting in additional charge on the gate to source capacitance.

The effect of varying the driver width of the inverter is also investigated using three inverters with the following driver widths: 800 µm, 710 µm and 300 µm. The graph of the forward and reverse sweeps of the VTC are shown in *Figure 5. 18*. As the width of the driver device increases from 300 µm to 800 µm, the DC gain of the forward sweep increases as well from 4.7 dB to 15.3 dB as it is proportional to the transconductance of the driver transistor. Similarly, the V_{OL} value decreases from −1.3 V to −4.4 V with the decrease in driver width as expected, given that V_{OL} is determined by the aspect ratio of the driver and load width as demonstrated in *equation 5. 8*. On the other hand, the V_{OH} value remains fairly constant at −13.6 V and −13.5 V for the 710 µm and 300 µm device whereas for the 800 µm device, the

value is slightly higher at −12.3 V. The reason for this could be that the V_{T_L} of the 800 µm inverter is slightly higher than the V_{T_L} of the other inverters, resulting in a reduction of the output voltage swing. Another important observation is that the switching point of this inverter is more negative than the other inverters, which contradicts the theoretical expectation, whereby it would be expected that as the driver width increases, the switching point would also shift towards more positive values thereby compromising the noise margins and dynamic range of the inverter. This observation seems to corroborate the fact that the threshold voltage is different in the load device of the inverter having a W_D of 800 µm. This seems plausible given that variations in the film thickness of the oxide on different parts of the substrates could occur during the growth of the dielectric thereby resulting in different threshold voltage values.

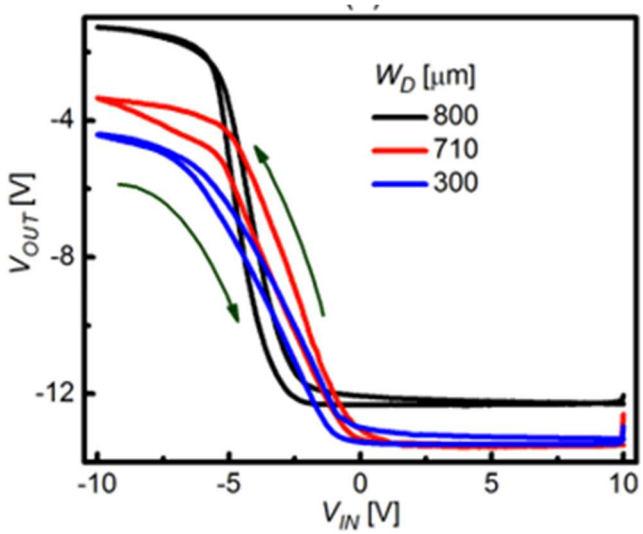

Figure 5. 18: The VTC of a saturated load inverter with PBTTT-C16 polymer as the active layer. The value of the driver widths is 800 µm, 710 µm and 300 µm whereas the width and length of the load and the driver transistors are kept constant at 90 µm and 20 µm respectively. The values of V_{DD} and V_{SS} are 0 and –15 V whereas the input voltage for the DC response is swept from −9 V to +9 V and vice versa.

Table 5.6 over leaf gives a summary of the DC and transient properties of the previously mentioned inverters.

Table 5. 6: Summary of the DC properties of inverters made with different driver widths made using PBTTT-C16 polymer.

	Width of driver (µm)		
	800	710	300
Forward DC sweep			
V_{OL} *(V)*	−1.3	−3.4	−4.4
V_{OH} *(V)*	−12.3	−13.6	−13.5
DC gain (dB)	15.3	11.1	4.7
Reverse DC sweep			
V_{OL} *(V)*	−1.3	−3.4	−4.4
V_{OH} *(V)*	−12.3	−13.5	−13.3
DC gain (dB)	12.7	6.6	1.8

The DC and transient response of the inverter studied in *Figure 5. 14* is carried out using a thiophene-based polymer, P3HT that is known to have a lower mobility value than PBTTT-C16 polymer. The aspect ratio and topology of the SAG TFT used in characterisation of the PBTTT-C16 polymer in chapter 4, is adopted for characterisation of the P3HT polymer. The output and transfer characteristics of the SAG P3HT TFT are shown in *Figure 5. 19*. The on/off ratio of the transistor is found to be about 1.6×10^2. The saturation field-effect mobility, μ_{fe} and threshold voltage, V_T are also extrapolated from the plot of $I_D^{0.5}$ versus V_G and are found to be 0.01 $cm^2V^{-1}s^{-1}$ and 2.5 V respectively.

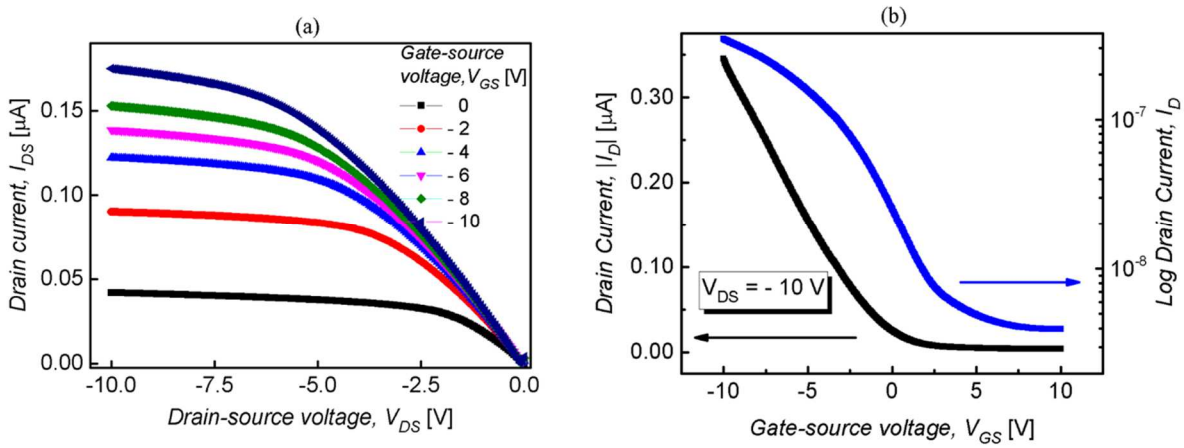

Figure 5. 19: Linear and sub-threshold plots of spin-coated SAG P3HT TFT swept from V_{GS} of +10 V to −10 V at a V_{DS} of −10 V. The thickness of the active layer and aluminium oxide dielectric is 70 nm and 50 nm respectively. The aspect ratio of the TFT is 50 (W/L=1000 µm/20 µm).

The graph of the VTC and the transient response of the P3HT inverter are as shown in *Figure 5. 20*. From the VTC curve the values obtained for the gain, V_{OH} and V_{OL} are 5.6 dB, −13.7 V and − 2.9 V respectively. The lower gain obtained is associated with the lower transconductance value of the transistors due to reduction in the mobility of the active layer. Furthermore, the use of different SAM layers (i.e. ODPA and HMDS for the PBTTT-C16 and the P3HT devices respectively) to modify the interface of the dielectric and OSC may affect the electrical conductivity of the individual transistors, which subsequently affects the driving capability of the inverter circuits. Whilst using the same SAM layer for characterisation of the two polymers would have been ideal, it was difficult to obtain a uniform spin-coated P3HT layer sticking onto the sample that has ODPA therefore HMDS SAM layer is chosen instead. In other words, the polymer adhesion of P3HT on ODPA-treated samples is poor in comparison to that of the adhesion of P3HT on HMDS-treated samples. However, a study of the electrical performance effect of SAM layers on plasma-treated alumina-based OTFTs shows that samples having silane based SAMs have substantially higher leakage currents and significant threshold variation in comparison to samples having an ODPA SAM layer [30]. This is corroborated with XPS data, which shows the surface coverage of the ODPA SAM on the plasma-treated alumina having a greater packing density compared to the silane based SAM on the same surface. In such a case, it is likely that the molecular ordering of PBTTT-C16 on ODPA is better than that of P3HT on HMDS, which translates to better charge transport.

The rise and fall times of the P3HT circuit inverter is 250 ms and 70 ms respectively. The average propagation delay is 38.4 ms, which relates to an operational frequency of 26.1 Hz, which is one order of magnitude lower than the value obtained for the PBTTT-C16 polymer, further highlighting the advantage of using materials with higher charge carrier mobility values to increase the speed of circuits.

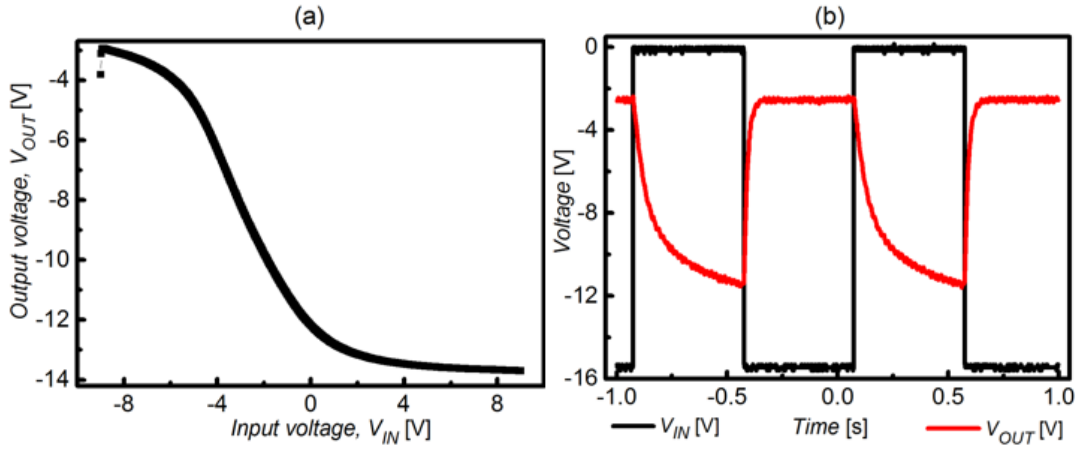

Figure 5. 20: The VTC (a) and transient response (b) of a saturated load inverter with P3HT polymer as the active layer. The values of V_{DD} and V_{SS} are 0 and −15 V whereas the input voltage for the DC response is swept from –9 V to +9 V. For the transient response, the frequency of the step pulse applied at the input terminal is 1 Hz. The magnitude of the step pulse is 15 V.

♦ **Challenges of the SAG process**

Although simple circuits such as inverters are fabricated using the SAG process, there are a number of key challenges that are encountered in the realisation of the circuits. Some of the challenges are fixed in this thesis whereas others are simply mitigated as discussed in the subsequent sections.

The first major challenge in the SAG process is encountered in the second processing step, which is essentially patterning of the gate contact and formation of the gap using the bi-layer photoresist (i.e. the LOR resist and the imaging resist). Initially, the fabrication of the circuit would fail due to failure in the formation of the gap. As it is mentioned in *section 4.2.1* of chapter 4, the formation of the gap is dictated by the soft bake process parameters. In the SAG process, it is necessary to develop the bilayer photoresist twice with a hard baking step in between the two developing times to create a difference in the dissolution rates of the two resists for proper formation of an undercut/gap, otherwise, the gold and aluminium metal contact will remain intact. If the gold and the aluminium metal layer remain in contact, when one proceeds to the next processing step i.e. growth of the dielectric, the gold layer will peel off as shown in *Figure 5. 21*. The two ways to mitigate this is by ensuring there is always a gap formed between the Au and Al contact and also reducing the channel widths of the transistors to <1000 µm or alternatively using a finger-type topology to spread out the area of the widths.

Increasing the gap size would not be a viable option, as it would result in larger channel resistances, which subsequently leads to reduction in the driving capability of the devices as observed in chapter 4. Further research into alternative ways of achieving the self-aligned gap would therefore be needed.

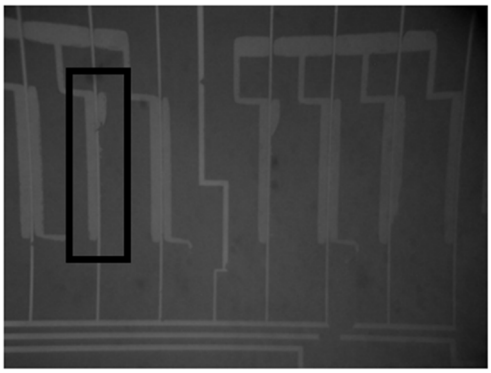

Figure 5. 21: Section of a circuit block made using the SAG process with the gold layer peeling off during the anodisation process due to lack of a gap between the gold and aluminium metal contacts.

The second challenge in fabricating of the circuit is in the third processing step, which is basically the formation of the source, and drain contacts made from gold metal. In *section 4.2.1* of chapter 4, it is mentioned that gold etchant is used for etching the unwanted gold metal contacts. However, while the unwanted gold metal is etched, parts of the underlying aluminium are etched as well even when the sample is exposed to the gold etchant for as little as 10 seconds. This is detrimental to subsequent processing steps as it is imperative that all of the underlying aluminium layer stays intact as it is used in the next step for anodisation of the gate contact; if this step is not achieved, there will be no dielectric and hence no viable transistors. *Figure 5. 22* below shows an example of a sample dipped in gold etchant for 5 seconds, with parts of the aluminium rails etched away.

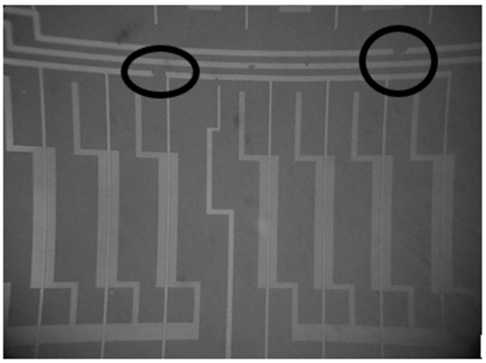

Figure 5. 22: Circuit section in the SAG process whereby part of the aluminium layer gets etched away by gold etchant when forming the source and drain contacts which are made from gold metal layer.

Some of the methods used in reducing the effect of the gold etchant on the aluminium layer are: using a thicker photoresist layer to protect/cover the aluminium layer, diluting of the gold etchant with deionised water to reduce the etching rate of the etchant on the aluminium layer and evaporating a thick enough aluminium layer to ensure some aluminium layer remains even after dipping in gold etch. Using a different etchant to the one used in this thesis would also be futile because aluminium metal reacts with most chemicals therefore it is decided that the best method in resolving the issue is to first grow the aluminium oxide layer and then pattern the source and drain contacts due to the fact that aluminium oxide is more resilient to gold etch than aluminium. However, in future it would be advisable to altogether use different materials for the gate contact and dielectric or alternatively a different method of dielectric formation.

The third challenge faced in the SAG process is the peeling of the crossover structures made from SU8 negative photoresist as shown in *Figure 5. 23 (a).* As mentioned in *section 5.3* of this chapter, the SU8 layer serves the purpose of allowing similar metal layers to crossover each other without connecting to avoid the formation of short circuits; therefore, peeling of the SU8 layer would result in improper functioning of circuits. The cause of the peel is due to insufficient curing of the negative photoresist, which therefore makes it susceptible to dissolving in any photoresist remover in subsequent steps. To eliminate this issue, one needs to cure the resist at an elevated temperature of about 210 °C for 30 min to ensure proper polymer crosslinking thereby making it resilient to remover solution. *Figure 5. 23 (b)* shows part of a circuit fabricated with the aforementioned conditions. The colourless SU8 structures remain intact even after being left in remover solution for an hour.

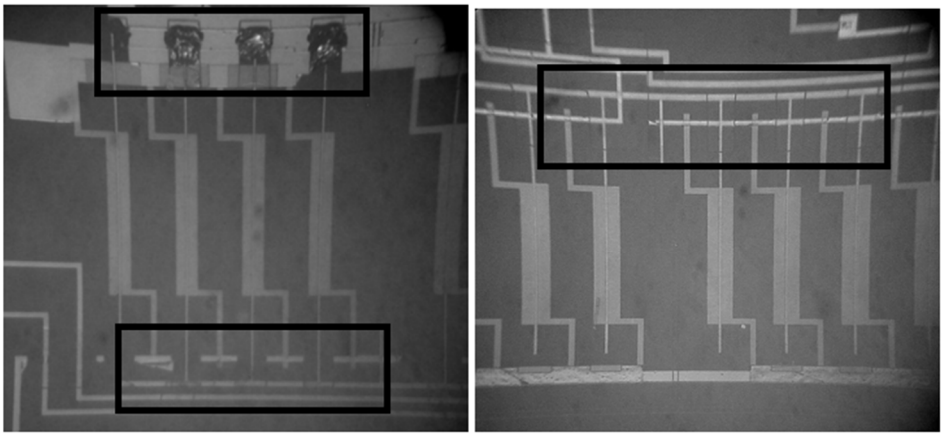

Figure 5. 23: (a) Part of the SU8 negative resist peeling off from a circuit block when dissolved in remover solution because of insufficient curing of the SU8 resist during processing. (b) A sample circuit block with SU8 resist layer remaining intact after being exposed to remover solution; the layer is cured at an elevated temperature and time of 210 °C and 30 min respectively.

The last challenge faced in the SAG process is to do with the lift off the aluminium layer in the last stage prior to deposition of the polymer layer. Parts of the aluminium layer would remain on the substrate, which would be problematic, especially if the remaining parts overlapped connections of transistors that are otherwise meant to not be connected. *Figure 5. 24 (a)* gives an example of parts of the aluminium layer retained on the substrate although fortunately enough not forming unwanted connections as opposed to *(b)* where clearly patterned structures of the second aluminium layer are retained and the unwanted bits are lifted off. The unwanted remains are thought to be a result of residual resist/contaminants from the previous patterning steps, which could therefore be removed with a gentle plasma/UV ozone treatment as is done for the circuit in *Figure 5. 24 (b).* It is not advisable to use ultrasonic agitation while lifting off for fear of losing the layers that are supposed to remain on the sample.

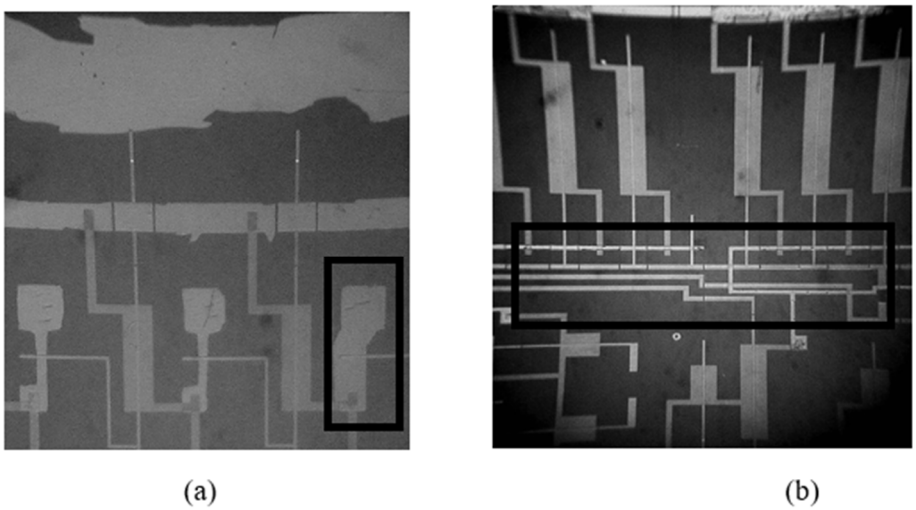

Figure 5. 24: (a) A circuit section made using the SAG process where parts of the unwanted aluminium layer remain on the substrate after lift-off. (b) A different circuit showing better aluminium lift off because of cleaning the substrate using UV ozone prior to aluminium deposition to remove unwanted contaminants on the surface.

5.4 CONCLUSIONS

An OTFT model is designed in this chapter for later use in the design and modelling of mixed analogue and digital signal circuits. The model modifies pre-existing silicon transistors within the Cadence design software environment and utilizes key parameters from the disordered models developed in Chapter 2 for circuit simulation. The fit of the Cadence OTFT model to the experimental data displayed slightly poor fits for lower gate bias believed to be because of contact resistance effects.

A comparator circuit consisting of a preamplifier, latch and a self-biased amplifier for the output stage is designed using the Cadence OTFT model. The amplifier has a gain of 45.62 dB and 35.40 dB assuming a threshold voltage of −1.5 V and −2.5 V respectively. A perceived decrease in the threshold voltage value of the comparator is seen to result in a decrease in the output voltage swing of the comparator. The operational frequency of the comparator is found to be around 300 Hz. The addition of two inverter stages into the latch section of the comparator results in a drop in the gain from 45.62 dB to 11.63 dB and an increase in the propagation delay of the inverter from 3.4 ms to 13.1 ms.

The fabrication of the designed circuits is carried out using the SAG process developed in chapter 4. A PBTTT-C16 saturated load inverter is successfully fabricated and is found to

have a gain of 12.4 dB and an average propagation delay of 3.4 ms. The performance of the same inverter is compared to one with the same dimensions but different polymer, namely, P3HT. The later inverter has a gain, V_{OH} and V_{OL} of 5.6 dB, −13.7 V and −2.9 V respectively and a propagation delay of 38.4 ms, highlighting the improved characteristics of gain and speed from using a polymer with a higher charge carrier mobility such as PBTTT-C16. Similarly, inverters with different driver widths of 800 µm, 710 µm and 300 µm are fabricated using the same polymer. The value of V_{OL} and the gain is found to increase from −4.4 V to −1.3 V and from 4.7 dB to 15.3 dB respectively with increase in the driver width as both the output level and the gain are directly proportional to the driver width. The value of V_{OH} is also found to be higher (−12.3 V) for the device with a driver width of 800 µm suggesting that the threshold voltage is probably different to the other devices as a result of processing variations.

The challenges faced in the fabrication of the circuits using the SAG process are also highlighted. The problems include peeling of the Au layer during anodisation of the Al layer, etching of the Al layer whilst simultaneously etching the unwanted Au layer, peeling of the crossover structures and insufficient lift off the second Al layer. The issue of the crossover structure and unwanted etching of the Al layer is solved by ensuring sufficient curing of the SU8 layer and ensuring the dielectric is formed before formation of the source and drain contacts respectively. However, solutions offered for the remaining problems are found to merely reduce the extent of the issues thereby enabling one to make some circuit blocks although replicability of the process would prove challenging as is experienced in the undertaking of this thesis.

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CHAPTER 6

Conclusions and Recommendations for Future work

A summary of the key conclusions of this thesis is outlined. In addition, recommendations for potential experimental work to be carried out in future are presented.

6.1 CONCLUSIONS

In organic materials, charge transport is believed to take place through thermal activation of carriers between localised states, which are typically expressed using an exponential, or Gaussian distribution. In this thesis, an exponential approximation to the tail of the Gaussian DOS distribution is used in the formulation of analytical models. One of these models includes an expression for the effective mobility, which is developed by making a direct comparison of a disordered system to an ordered one such that carrier movement is described by a charge transport energy level akin to the valence energy band level in an ordered system. By equating the current flux of these systems, a mobility expression with a dependency on carrier concentration is developed. Subsequently, disordered models are developed for the current expressions of Schottky diodes and OTFTs with the subsequent introduction of material parameters: *MNE, K* and *m.* These parameters are later used in the modelling and design of organic circuits in this thesis.

The forward *J-V* characteristics of PBTTT-C16 and IDTBT-C16 vertical diodes increases exponentially with application of a forward bias because of an exponential increase in carrier concentration. PBTTT-C16 diode has a higher forward current value than IDTBT-C16 diode, which is believed to be associated with the smaller potential barrier, formed with the gold contact. The use of an Ohmic contact with a higher work function or modifying the potential barrier between IDTBT-C16 and the Ohmic contact by using a SAM layer would therefore be preferable for easier injection of carriers. From the exponential region of the forward characteristics, the values of T_0, T_C and *MNE* of the PBTTT-C16 diode are found to be 707.5 K, 523.6 K and 45 meV and that of the IDTBT-C16 diode are found to be 343.6 K, 382.7 K and 33.0 meV respectively, indicating that the latter has a lower degree of energetic disorder. Similarly, the ideality factor values obtained for PBTTT-C16 and IDTBT-C16 Schottky diodes are 2.3 and 1.1 respectively.

The PBTTT-C16 Schottky diode displayed higher reverse current density values than IDTBT-C16 because of its high HOMO energy level value, which essentially makes it susceptible to oxygen doping effects. Good fits are obtained from the semi-logarithmic plot of J_R versus $V_R^{¼}$ of the PBTTT-C16 diode resulting in an acceptor density value of 1.59×10^{22} m^{-3}. On the other hand, poor fits of the same plot are obtained for the IDTBT C16

diode, which could be because of Fermi-level pinning within the diode. The activation energy values for the PBTTT-C16 and IDTBT-C16 devices are found to be 126 meV and 339 meV respectively. The larger value obtained for the latter is believed to be associated with the large π-stacking distance between neighbouring polymer chains making them essentially trapped carriers.

A SAG fabrication process is developed and characterised in this work through electrical and optical measurements. Studies of the undercut size/gap formed by the process are made by varying the soft bake temperature and time whereby increasing both of the aforementioned parameters resulted in smaller gap sizes. Subsequent scaling studies of lateral PTAA diodes with gap sizes ranging from 0.05 µm to 2 µm revealed an inverse correlation of the gap size with the forward current density (from 15.86 Am^{-2} to 0.31 Am^{-2} respectively). The ideality factor obtained from these devices increases from 2.2 to 5.0 with increase in the gap size, which is believed to be associated with the increase in the series resistance. The value of T_C varied from 671 K to 1503 K for the same devices; the reason for this is not fully understood, as it would be expected that it would remain constant given that T_C is a material constant parameter that defines the distribution of the DOS. The current conduction mechanism of these devices is also shown to be dominated by contact resistance effects as the electrode spacing reduced. From the plot of $log_e (J_R)$ against $V_R^{0.25}$, the acceptor density values obtained from these devices varied between 2.33×10^{20} m^{-3} to 1.76×10^{21} m^{-3} corresponding to depletion width values of about 4.8 µm to 1.3 µm, which is much wider than the film thickness of 110 nm. CV measurements and SILVACO simulations also revealed that the modulation of the depletion width of the PTAA lateral diodes is in fact dependent on the gap size of the devices as well as the area of the active layer. The patterning of the active layer using orthogonal solvents resulted in an overall reduction of the spread of the forward and reverse current values in these devices, however, an increase in both of the forward and reverse currents is also noted and is believed to be associated with the unintentional doping of the active layer by the chemical solvents used in the patterning process.

A PBTTT-C16 transistor with an aspect ratio of 50 is also fabricated using the SAG process. The device has a sub-threshold swing of −1.8 V/decade and an on/off ratio of 4.26×10^2. From the plot of $I_D^{0.5}$ versus V_G, the values of μ_{fe} and $V_{T\ are}$ found to be 0.74 $cm^2V^{-1}s^{-1}$ and −1.5 V respectively. Forward and reverse sweeps of the electrical

characteristics showed instability in the device with the threshold voltage and the off current changing from −1.5 V to −2.2 V and from 7.7 nA to 10.8 nA respectively. The aforementioned instability is associated with migration of residual dopants within the film. Utilising the disordered model, the material constants *m* and *K*, are obtained from the intercept and slope of log (dI_{sat}/dV_G) against log (V_G') and are found to be 0.57 and 2.15×10^{-16} AV^{-m} respectively corresponding to a T_C and *MNE* of 473 K and 41 meV respectively.

An OTFT model is created in Cadence design software such that key parameters found in the model files i.e. t_{ox}, I_{off}, $\mu_{fe,}$ and V_T are edited to reflect the values obtained from the experimental data. In addition, a Verilog code containing OTFT parameters specifically, *m* and *K* are also incorporated into the model to reflect the higher power dependency of the drain current as typically observed in disordered transistors. The fitting of the experimental data to the Cadence model showed inadequate fits for the lower drain voltage values because of contact resistance effects. Utilizing this new model, a comparator circuit containing three stages, namely: a preamplifier, latch and self-biased amplifier for the output stage is designed. To account for the threshold instability observed in the PBTTT-C16 device, the comparator is simulated using two values of threshold voltage i.e. −1.5 V and −2.2 V resulting in a gain value of 45.62 dB and 35.40 dB respectively. The comparator operates at a frequency of about 300 Hz. The addition of two inverter stages into the latch stage of the comparator resulted in a gain of 11.63 dB and an increase in the propagation delay by one order of magnitude.

The fabrication of circuits using the SAG process is a bit challenging to execute. The challenges faced in realising the circuits included among others: failure in forming of a gap between the aluminium and gold layers, unintentional etching of parts of the aluminium layer while patterning the gold layer, peeling of the crossover structures and poor lift off of the last metal layer which is also made of aluminium. Whilst the third challenge is completely eradicated, the rest are simply mitigated thereby resulting in lack of a full proof, reliable and repeatable fabrication process. In spite of these challenges, saturated-load inverter circuits are realised using this SAG process. A PBTTT-C16 saturated-load inverter with a gain of 12.4 dB and an average propagation delay of 3.4 ms is fabricated. Similarly, the same inverter is made using P3HT polymer, which is known to have a lower mobility than the latter polymer. The inverter has a gain of 5.6 dB and an average propagation delay of 38.4 ms. In addition, PBTTT-C16 inverters with driver widths of 800 µm, 710 µm and 300 µm are fabricated. The

experimental gain and V_{OL} value of these inverters is found to be proportional to the driver width as would be expected.

To conclude, this work confirms that the mobility of organic semiconductors has a strong dependency on carrier concentration. In addition to this, the π-stacking distance between neighbouring polymer chains is a critical parameter determining carrier transport in vertical devices, such that, having a small π-stacking distance reduces the thermal activation energy needed for intermolecular hopping thereby enhancing charge transport. Lateral devices and circuits can also be realised using a SAG process. The feature sizes obtained from this process are optimised by varying the soft bake parameters of the lift-off resist layer whereby to obtain small feature sizes, the soft bake temperature and time are reduced. Another interesting conclusion drawn from this work is that contact resistance effects dominate current conduction in lateral diode topologies particularly as the electrode spacing is reduced. Moreover, the interelectrode spacing and the active layer area of the latter device topology determines the modulation of the depletion width when the device is either forward or reverse biased. Lastly, orthogonal solvents used for patterning of PTAA polymer unintentionally dopes the polymer resulting in an apparent increase of its electrical conductivity.

6.2 RECOMMENDATIONS

The field of organic electronics has unquestionably advanced over the years from the conception of simple devices to the realisation of simple and a number of advanced circuit blocks. In spite of this, there are a couple of challenges needed to be overcome in order to fully realise the numerous potential opportunities that this field has to offer.

A number of charge transport models have been developed in the field of organics with a couple favouring an exponential DOS over a Gaussian DOS and vice versa. In this thesis, the former is chosen and is subsequently used in developing an expression for the effective mobility. Interestingly enough, the model demonstrated in this work showed a dependency of the effective mobility on carrier concentration, akin to the UML. The model did not incorporate the conduction mechanism of carriers yet arrived at the same dependency as other models published in literature i.e. percolation theory approach and Variable Range Hopping (VRH) mechanism, just to name a few. This observation is still not yet understood and as such, the

importance of the hopping mechanism and its correlation or lack thereof to the mobility expression needs to be studied further.

A key challenge in the modelling of organic circuits is the instability of organic devices as a result of drifting of residual mobile ions within the polymer film and oxygen doping effects upon exposure to ambient conditions. This effect makes it particularly challenging to model circuits given the change in key operating parameters of the device, for instance, the threshold voltage. Although recent advancements in designing organic materials involves increasing the HOMO energy level to reduce the oxygen doping effects, more rigorous efforts are needed to ensure longer shelf-lives and proper functionality of the intended circuits in the future. Encapsulation of devices could be one way of realising this.

The mobility of solution-based organic materials is still relatively low in comparison to inorganic materials such as silicon. One major way of increasing the mobility value is by tweaking the morphological structure of the organic material as is shown with the two different thiophene polymers studied in this thesis, however, as is noted, the structure of the device also effects the perceived operating efficiency of the organic material with some topologies favouring 2D charge type transport dictated by intermolecular and intramolecular hopping mechanisms whereas others favour the 1D transport along the polymer chain. Therefore, in future, material scientists would need to tailor the morphology of the polymers according to the end-user application to provide better electrical characteristics.

Surface treatments of the interface between the Ohmic contact and the organic semiconductor as well as at the interface of the organic semiconductor and the dielectric are sometimes necessary to improve the electrical characteristics of the end devices, however, this is particularly challenging to execute in devices such as bottom gate, bottom contact devices or in planar devices such as those studied in this work as carrying out both treatments in such topologies inherently degrades one of the interfaces thereby resulting in poor electrical performance to some degree. Future research into simultaneously treating both interfaces without compromising the performance of the other would be beneficial.

In this thesis, models for the forward current density in organic Schottky diodes and in OTFTs are developed. Several of the organic Schottky diodes showed good fittings to the plot of J_R vs $V_R^{¼}$, with the acceptor density values obtained from the slope of these plots. Although

the experimental data fits well with the conventional theory of Schottky diodes, it is still not yet understood why it is so given that the conventional theory fails to include/account for the conduction process of the organic semiconductors.

Isolating of the active layer through patterning either via lift off or wet/dry etching is typically done to reduce cross talk between devices on a substrate/wafer. However, one challenge with patterning of organic devices is the insufficient number of orthogonal solvents available in the microelectronics industry. In addition, the few that are available in some way or another end up having a doping effect on the organic layer in spite of them being orthogonal to the organic material. Moreover, presently, some polymers studied in this work e.g. P3HT and PBTTT-C16 cannot be patterned efficiently with the aforementioned chemicals as they end up coagulating upon exposure to the orthogonal solvents; the reason for this is still not yet understood and would need to be investigated further.

Lastly, alternative methods in realising a self-aligned fabrication process would also be an interesting research topic given the numerous implications of the process i.e. faster switching speeds as well as improving the bandwidth of circuits through the reduction of overlap parasitic capacitances.

APPENDICES

Appendix A: Expression for the free carrier concentration in a *p*-type Disordered Organic Semiconductor

The Density of States (DOS) can be expressed using a Gaussian distribution, with an exponential approximation at the band tail, as assumed in this work, which is given by *equation A. 1*:

$$N'(E) = N'(0)\exp\left(-\frac{E}{kT_C}\right) \qquad A.\ 1$$

where $N'(0)$ is the rate of change of the density of traps at energy E=0, E is the energy of the localized states, k is Boltzmann's constant and T_C is the characteristic temperature associated with the exponential DOS.

For energies below the Fermi level E_F, the carrier distribution can be expressed by approximating the Fermi-Dirac statistics to a Maxwell Boltzmann function, as represented by *equation A. 2*:

$$f(E) = \exp\left(-\frac{E_F - E}{kT}\right) \qquad A.\ 2$$

where T is the absolute temperature.

Subsequently, the free carrier concentration, p, is found by integrating *equation A. 1* and *equation A. 2* as shown below, assuming that the hopping events that contribute to conduction occur below E_F.

$$p = \int_{-\infty}^{E_F} N'(E) f(E) dE \qquad A.\ 3$$

$$p = \int_{-\infty}^{E_F} N'(0)\exp\left(-\frac{E}{kT_C}\right)\exp\left(-\frac{E_F - E}{kT}\right)dE \qquad A.\ 4$$

Or simply,

$$p = \int_{-\infty}^{E_F} N'(0)\exp\left(-\frac{E}{kT_C}\right)\exp\left(\frac{E}{kT}\right)\exp\left(-\frac{E_F}{kT}\right)dE \qquad A.\ 5$$

Equation A. 5 can further be simplified using the relation given by *equation A. 6* ,

$$\frac{1}{T_0} = \frac{1}{T} - \frac{1}{T_C} \qquad A.\ 6$$

where T_0 is the characteristic temperature associated with the distribution of carriers.

Thus resulting in:

$$p = N'(0)\exp\left(-\frac{E_F}{kT}\right)\int_{-\infty}^{E_F}\exp\left(\frac{E}{kT_0}\right)dE \qquad A.\ 7$$

Upon integrating *equation A. 7*, the final expression for the free hole carrier concentration takes the form:

$$p = N'(0)kT_0\exp\left(-\frac{E_F}{kT_C}\right) \qquad A.\ 8$$

Appendix B: Expression for the effective mobility in terms of carrier concentration

The effective mobility, $\mu_{eff,}$ can be found by making a direct comparison of the current densities of a disordered system, $J_{Disordered}$ to that of an ordered (crystalline) system, $J_{Ordered}$, as given by *equations B. 1* and *B. 2* respectively:

$$J_{Disordered} = N'(0)kT_0 \exp\left(-\frac{E_F}{kT_C}\right) q\mu_{eff} F \qquad B.\ 1$$

$$J_{Ordered} = N_V \exp\left(-\frac{E_F - E_V}{kT}\right) q\mu_m F \qquad B.\ 2$$

where N_V is the effective DOS at the edge of the valence band, E_V, E_F is the Fermi level, k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge, F is the applied electric field, μ_m is the measured mobility, $N'(0)$ is the rate of change of the density of traps at energy $E = 0$, T_0 is the characteristic temperature associated with the distribution of carriers and T_C is the characteristic temperature associated with the DOS.

Subsequently, at equilibrium, μ_{eff} takes the form below:

$$\mu_{eff} = \mu_m \frac{N_V}{N'(0)kT_0} \exp\left(-\frac{E_F - E_V}{kT}\right) \exp\left(\frac{E_F}{kT_C}\right) \qquad B.\ 3$$

Upon simplification of *equation B. 3* using the relation given by *equation B. 4*, the effective mobility takes the form given in *equation B. 5*,

$$\exp\left(-\frac{E_F}{kT}\right) = \exp\left(-\frac{E_F}{kT_C}\right)^{T_C/T} \qquad B.\ 4$$

$$\mu_{eff} = \mu_m \frac{N_V}{N'(0)kT_0} \exp\left(\frac{E_V}{kT}\right) \exp\left(\frac{E_F}{kT_C}\right)^{(T_C/T)-1} \qquad B.\ 5$$

To express the effective mobility in terms of the free carrier concentration (p) and temperature, the expression for the free carrier concentration, given by *equation B. 6*, is rearranged accordingly as shown in *equation B. 7*,

$$p = N'(0)kT_0 \exp\left(-\frac{E_F}{kT_C}\right) \qquad B.\ 6$$

$$\left[\frac{p}{N'(0)kT_0}\right]^{(T_C/T)-1} = \left[\exp\left(\frac{E_F}{kT_C}\right)\right]^{(T_C/T)-1} \qquad B.\ 7$$

By substituting for *equation B. 7* in *B. 5*, the expression for the dependency of the effective mobility on carrier concentration and temperature takes the form given in *equation B. 8*,

$$\mu_{eff} = \mu_m \frac{N_V}{\left(N'(0)kT_0\right)^{(T_C/T)}} \exp\left(\frac{E_V}{kT_C}\right) p^{(T_C/T)-1} \qquad B.\ 8$$

where,

$$K = \mu_m \frac{N_V}{\left(N'(0)kT_0\right)^{(T_C/T)}} \exp\left(\frac{E_V}{kT_C}\right) \qquad B.\ 9$$

$$m = \frac{T_C}{T} - 1 \qquad B.\ 10$$

K can simplify be referred to as the mobility prefactor and *m* is the power factor correlating the mobility to the carrier concentration whose value is dependent on the degree of energetic disorder, dictated by the values of T_C.

Appendix C: Expression for the Forward Current Density of an Organic diode at Low Applied Bias

On application of a forward bias, the current density initially increases exponentially because of an increase in the carrier concentration, which is typically described by an exponential DOS distribution with energy given by the Maxwell Boltzmann approximation to the Fermi-Dirac statistics.

Assuming that all the carriers that contribute to conduction occur below the Fermi level, E_F, an expression for the free carrier concentration involved in current conduction in an organic Schottky diode thereby takes the form given by *equation C. 1*:

$$p = \int_{-\infty}^{E_F} N'(0)\exp\left(-\frac{E}{kT_C}\right)\exp\left(-\frac{E_F - E}{kT}\right)dE \qquad C.\ 1$$

where *N' (0)* is the rate of change of the density of traps at energy E=0, E is the energy of the localized states, T_C is the characteristic temperature representing the exponential DOS, k is Boltzmann's constant and T is the absolute temperature.

By assuming a flat quasi Fermi-level, the forward current density of an organic diode with respect to the applied voltage, V_{app}, can be obtained. Upon application of a negative voltage bias, the energy barrier between the Schottky and organic semiconductor is reduced significantly thereby facilitating the movement of carriers (holes) across the interface into the adjourning metal contact. An exponential increase in the forward current density is observed because of the increase in carrier concentration brought on by the application of an external bias. By integrating from the top of the energy barrier, E_B, to infinity, the resultant current density can be obtained as shown in *equation C. 2*:

$$J \propto \int_{-\infty}^{-E_B+qV_{app}} N'(0)\exp\left(-\frac{E}{kT_C}\right)\exp\left(-\frac{E_F - E}{kT}\right)dE \qquad C.\ 2$$

Rearranging above by substituting with the relation, $\frac{1}{T_0} = \frac{1}{T} - \frac{1}{T_C}$ gives:

$$J \propto \int_{-\infty}^{-E_B+qV_{app}} N'(0)\exp\left(-\frac{E}{kT_C}\right)\exp\left(-\frac{E_F}{kT}\right)\exp\left(\frac{E}{kT}\right)dE$$

$$J \propto \int_{-\infty}^{-E_B+qV_{app}} N'(0)\exp\left(-\frac{E_F}{kT}\right)\exp\left(\frac{E}{kT_0}\right)dE \qquad C.\ 3$$

where T_0 is the characteristic temperature representing the exponential distribution of carriers.

On further rearranging *equation C. 3*, we obtain an expression for the forward current density at low bias as shown in *equation C. 4*,

$$J \propto N'(0)\exp\left(-\frac{E_F}{kT}\right)\int_{-\infty}^{-E_B+qV_{app}} \exp\left(\frac{E}{kT_0}\right)dE$$

$$J \propto N'(0)kT_0\exp\left(-\frac{E_F}{kT}\right)\exp\left(-\frac{E_B}{kT_0}\right)\exp\left(\frac{qV_{app}}{kT_0}\right) \qquad C.\ 4$$

Equation C. 4 can be expressed in a much simpler form as in *equation C. 5*:

$$J \propto \exp\left(\frac{qV_{app}}{kT_0}\right) \qquad C.\ 5$$

Appendix D: Expression for the Forward Space Charge Limited Current (SCLC) Density of an Organic diode at Higher Applied Bias

The drift current density, *J*, associated with the SCLC takes the form:

$$J = p_f q \mu_{eff} F \qquad D.\ 1$$

where p_f is the free carrier concentration, q is the electronic charge, μ_{eff} is the effective mobility and F is the applied electric field.

Taking into account the carrier-dependent effective mobility, the expression for the current density is thereby rewritten as follows:

$$J = qKp_f^{\,m+1}F \qquad D.\ 2$$

Here,

$$\mu_{eff} = Kp^{\,m}$$

where K is the mobility prefactor and m is a material constant

In a material with a single set of shallow traps, the factor θ as given by *equation D. 3* gives the ratio of the free carrier concentration to the total injected carrier concentration.

$$\theta = \frac{p_f}{p_f + p_t} \qquad D.\ 3$$

where p_f is the concentration of the free carriers and p_t is the concentration of the trapped carriers.

In deriving a model for the SCLC in disordered semiconductors, it is assumed that the trapped and free carriers are associated with the intrinsic energy levels found within the exponential DOS of the material such that, in a *p*-type semiconductor, the trapped and free carriers occur above and below the Fermi level, E_F, respectively. The probability of the carrier occupancy within the DOS is hereby explained using the Maxwell Boltzmann statics given by *equation D. 4*:

$$f(E)=\begin{cases} \exp\left(-\dfrac{E_F-E}{kT}\right) & \text{if } E < E_F \\ 1 & \text{if } E \geq E_F \end{cases} \qquad D.\ 4$$

where E is the energy of the localised states, k is Boltzmann's constant and T is the absolute temperature.

The concentration of the trapped carriers, p_t, occurring above E_F is therefore given by:

$$p_t = N'(0)kT_C \exp\left(-\frac{E_F}{kT_C}\right) \qquad D.\ 5$$

where $N'(0)$ is the rate of change of the density of traps at energy E=0 and T_C is the characteristic temperature associated with the exponential DOS.

On the other hand, the concentration of the free carriers, p_f, occurring below E_F is given by:

$$p_f = N'(0)kT_0 \exp\left(-\frac{E_F}{kT_C}\right) \qquad D.\ 6$$

By inserting the expressions for the free carriers and trapped carriers in *equation D. 3*, θ is given as:

$$\theta = \frac{N'(0)kT_0 \exp\left(-\dfrac{E_F}{kT_C}\right)}{N'(0)kT_0 \exp\left(-\dfrac{E_F}{kT_C}\right) + N'(0)kT_C \exp\left(-\dfrac{E_F}{kT_C}\right)} \qquad D.\ 7$$

On rearranging and simplifying the above and using the relation $\frac{1}{T_0}=\frac{1}{T}-\frac{1}{T_C}$, θ for the disordered SCLC takes the form:

$$\theta = \frac{T_0}{T_0+T_C} = \frac{T}{T_C} \qquad D.\ 8$$

where T_0 is the distribution of carriers.

By expressing p_f in terms of θ and using Poisson's equation, the expression for the concentration of free carriers, p_f can be derived as shown below:

$$\frac{dF(x)}{dx} = -\frac{q(p_f + p_t)}{\varepsilon_0 \varepsilon_r} = -\frac{qp_f}{\varepsilon_0 \varepsilon_r \theta} \qquad D.\ 9$$

where ε_0 is the permittivity of free space and ε_r is the relative permittivity of the semiconductor

Substituing the above expression for p_f into *equation D. 2* we obtain:

$$\frac{dF(x)}{dx} = -\frac{qp_f}{\varepsilon_0 \varepsilon_r \theta}\left(\frac{J}{qKF}\right)^{\frac{1}{m+1}} \qquad D.\ 10$$

By integrating *equation D. 10* above with respect to the interelectrode distance, *x*, the electric field takes the form:

$$F = \left[\frac{q}{\varepsilon_0 \varepsilon_r \theta}\left(\frac{m+2}{m+1}\right)\right]^{\frac{m+1}{m+2}}\left(\frac{J}{qK}\right)^{\frac{1}{m+2}} x^{\frac{m+1}{m+2}} \qquad D.\ 11$$

The electric field is substituted for into *equation D. 11* above using the relation $F = -dV/dx$ and the correlation of varying potential (i.e. application of a voltage, V_{app}) with inter-electrode spacing *x* is obtained as shown in *equation D. 12:*

$$V_{app} = \left(\frac{J}{qK}\right)^{\frac{1}{m+2}}\left(\frac{q(m+2)}{\varepsilon_0 \varepsilon_r \theta(m+1)}\right)^{\frac{m+1}{m+2}} x^{\frac{2m+3}{m+2}}\frac{m+2}{2m+3} \qquad D.\ 12$$

Rearranging *equation D. 12* above to make the current density, *J* the subject of the equation, the SCLC current density expression for organic materials is obtained:

$$J = \frac{K}{q^m}\left[\frac{\varepsilon_0 \varepsilon_r \theta(m+1)}{m+2}\right]^{m+1}\left(\frac{2m+3}{m+2}\right)^{m+2}\frac{V_{app}^{m+2}}{x^{2m+3}} \qquad D.\ 13$$

Appendix E: Expression for $\Delta\phi_B$ in Schottky diodes

The sum total of the potential energy of carriers, E_T, as a function of a distance x, is given by the sum of the image force energy, E_{IF} and the applied electric field energy, E_{EF}, as depicted in *Figure E. 1 such* that:

$$E_T = E_{IF} + E_{EF} \qquad E.\ 1$$

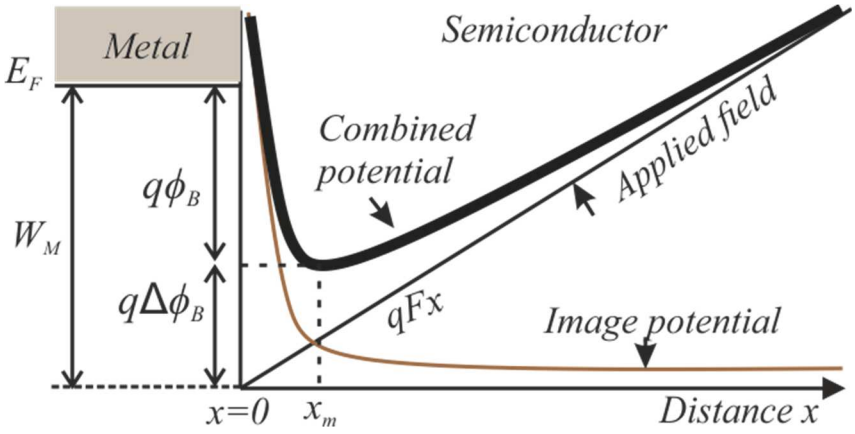

Figure E. 1: Sum total of the potential energy of holes (thick black line) due to the combined effect of image force and applied field.

The image force, F_{IF}, is associated with a hole charge carrier found at a distance x from the metal/semiconductor interface as depicted in *Figure E. 2* and expressed as:

$$F_{IF} = \frac{q^2}{4\pi\varepsilon_0\varepsilon_\infty\left(2x^2\right)} = -\frac{q^2}{16\pi\varepsilon_0\varepsilon_\infty x^2} \qquad E.\ 2$$

where q is the electronic charge, ε_o is the permittivity of free space and ε_∞ is the high-frequency permittivity of the semiconductor.

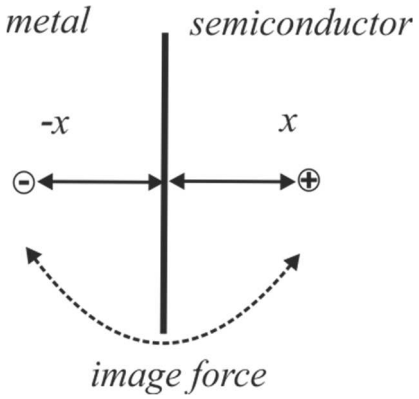

Figure E. 2: Image force effect at the interface of a p-type semiconductor and a Schottky metal contact.

The image force energy is solved for by integrating from x to ∞ as indicated below*:*

$$E_{IF} = \frac{q^2}{16\pi\varepsilon_0\varepsilon_\infty}\int_{\infty}^{x}\frac{1}{x^2}dx = \frac{q^2}{16\pi\varepsilon_0\varepsilon_\infty x} \qquad E.\ 3$$

The energy due to the external field, F takes the form:

$$E_{EF} = qxF \qquad E.\ 4$$

Substituting *equations E. 2* and *E. 4*, into *equation E. 1* results in:

$$E_T = \frac{q^2}{16\pi\varepsilon_0\varepsilon_\infty x} + qxF \qquad E.\ 5$$

The distance at which the barrier reaches its maximum value, given by x_m, is obtained when $dE_T/dx = 0$ as shown in *equation E. 6*:

$$\frac{dE_T}{dx} = \frac{d}{dx}\left(\frac{q^2}{16\pi\varepsilon_0\varepsilon_\infty x_m} + qx_mF\right) = 0 \qquad E.\ 6$$

Here *equation E. 6* can be further simplified to:

$$0 = -\frac{q^2}{16\pi\varepsilon_0\varepsilon_\infty x_m^2} + qF$$

Rearranging the above equation results in an expression for x_m given by *equation E. 7*:

$$x_m = \sqrt{\frac{q}{16\pi\varepsilon_0\varepsilon_\infty F}} \qquad E.\ 7$$

Substituting for x_m from *equation E. 7* into *equation E. 5*, the magnitude of the barrier lowering, $\Delta\phi_B$ takes the form:

$$\Delta\phi_B = x_m F + \sqrt{\frac{q}{16\pi\varepsilon_0\varepsilon_\infty x_m}} = 2x_m F \qquad E.\ 8$$

The electric field associated with the depletion layer found at the interface of the metal and semiconductor is determined by the distribution of acceptor ions. *Equation E. 9* shows the potential variation with the distance associated with the distribution of acceptor ions.

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon_0\varepsilon_r} \qquad E.\ 9$$

where ε_r is the relative permittivity of the material.

An expression of the electric field can thereby be achieved by solving for the Poisson's equation given in *equation E. 9* resulting in *equation E. 10*:

$$F = -\frac{dV}{dx} = \frac{qN_A W}{\varepsilon_0\varepsilon_r} \qquad E.\ 10$$

where W is the depletion width associated with the distribution of acceptor ions.

W is obtained by integrating *equation E. 10* from the surface of the semiconductor to the edge of the depletion layer resulting in:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_A}\left(V_{bi} - V_{app}\right)} \qquad E.\ 11$$

where V_{app} is the applied voltage and V_{bi} is the built-in potential.

Substituting *equation E. 11* (using the maximum depletion width given by x_m) in *E. 10* gives an expression for the field in terms of V_{app} and N_A as:

$$F = \sqrt{\frac{2qN_A}{\varepsilon_0\varepsilon_r}\left(V_{bi} - V_{app}\right)} \qquad E.\ 12$$

Combining the expressions for x_m and F given by *equations E. 11* and *E. 12* and inserting them into *equation E. 8*, the final expression for $\Delta\phi_B$ becomes:

$$\Delta\varphi_B = \left[\frac{q}{16\pi\varepsilon_0\varepsilon_\infty}\right]^{1/2}\left[\frac{2qN_A}{\varepsilon_0\varepsilon_r}\left(V_{bi} - V_{app}\right)\right]^{1/4} = \left[\frac{q^3N_A}{8\pi^2\varepsilon_0^3\varepsilon_r\varepsilon_\infty^2}\left(V_{bi} - V_{app}\right)\right]^{1/4} \qquad E.\ 13$$

Appendix F: Disordered model for an Organic Thin-Film Transistor (OTFT)

The expressions for the linear and saturation drain currents of OTFTs is derived using a gradual channel approximation assuming a planar *p*-type transistor working in accumulation regime as shown in *Figure F. 1*.

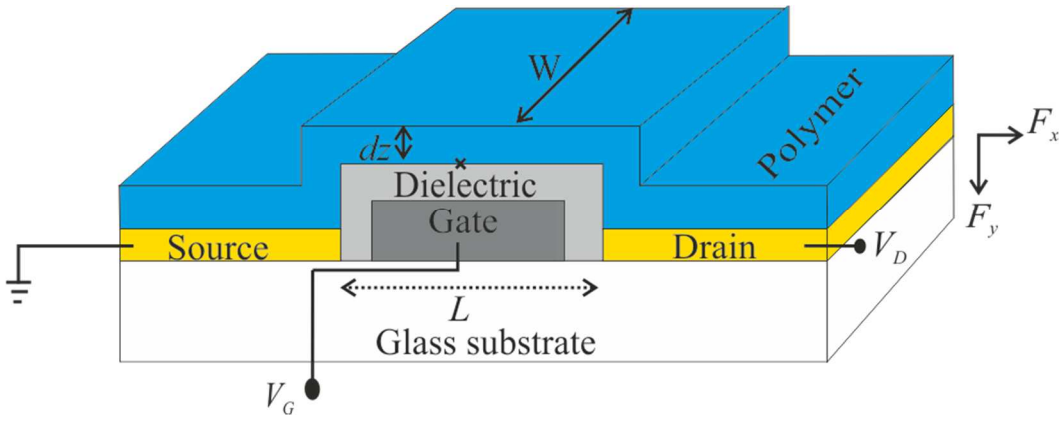

Figure F. 1: Structure of a planar self-aligned gap (SAG) p-type OTFT with gold source and drain contacts.

Upon applying a negative gate bias, V_G, charges accumulate at the semiconductor/ dielectric interface. The aforementioned induced charge, Q_S, takes the form:

$$Q_s = pq\ \mathrm{dz} = -C_{ox}\left(V_G - V_x\right) \qquad F.\ 1$$

where q is the electronic charge, p is the free hole concentration, dz is the thickness of the accumulation layer, C_{ox} is the dielectric capacitance per unit area and V_x is the voltage induced in the channel.

On application of a negative drain bias, V_D, a drift current density, J, flows between the source and drain contacts and is given by:

$$J = pqu_{eff}F_x \qquad F.\ 2$$

where F_x is the lateral field between the source and drain, in the x direction and μ_{eff} is the effective mobility.

By incorporating the Universal Mobility Law (UML) given by *equation F. 3* into *equation F. 2*, the expression for the current density takes the form shown in *equation F. 4*,

$$\mu_{eff} = Kp^{m} \qquad F.\ 3$$

$$J = qKp^{m+1}F_x \qquad F.\ 4$$

where *K* is the mobility prefactor and *m* is a material parameter.

Taking into account the variation of the free hole concentration with the surface potential, ϕ, *equation F. 4* becomes:

$$J = qKp_i^{m+1}\left[\exp\left(\frac{q\phi}{kT_C}\right)\right]^{m+1}F_x \qquad F.\ 5$$

Here,

$$p = p_i \exp\left(\frac{q\phi}{kT_C}\right)$$

where p_i is the intrinsic hole concentration, k is Boltzmann's constant and T_C is the characteristic temperature associated with the exponential DOS.

With a channel width, *W*, the current density can be expressed in terms of the current, *I*, as shown in *equation F. 6* :

$$I = (W\ \mathrm{dz})qKp_i^{m+1}\left[\exp\left(\frac{q\phi}{kT_C}\right)\right]^{m+1}F_x \qquad F.\ 6$$

Utilising Poisson's equation, the accumulation layer thickness, *dz*, can be expressed as:

$$\mathrm{dz} = \pm\frac{d\varphi}{F_y} \cong \pm\frac{d\varphi}{\sqrt{-(2qp_i/\varepsilon_0\varepsilon_r)(kT_C/q)\exp(q\varphi/kT_C)}} \qquad F.\ 7$$

where F_y is the vertical field, *y*, in the accumulated layer, ε_0 is the permittivity of free space and ε_r is the relative permittivity of the semiconductor.

Replacing for *dz* in *equation F. 6* with *equation F. 7*, the current expression becomes:

$$I = \pm qWKp_i^{(m+(1/2))} \sqrt{\frac{\varepsilon_0 \varepsilon_r}{2kT_C}} \times F_x \left[\exp\left(\frac{q\varphi}{kT_C} \right) \right]^{(m+(1/2))} \mathrm{d}\varphi \qquad F.\ 8$$

Upon integration of *equation F. 8* between *0* and ϕ_s (i.e. the maximum surface potential), the current takes the form given in *equation F. 9*:

$$I = \pm qWKp_i^{(m+(1/2))} \sqrt{\frac{\varepsilon_0 \varepsilon_r}{2kT_C}} F_x \int_0^{\varphi_s} \exp\left(\frac{q\left(m+(1/2)\right)\varphi}{kT_C} \right) \mathrm{d}\varphi$$

$$I = \pm WKp_i^{(m+(1/2))} \frac{\sqrt{2kT_C \varepsilon_0 \varepsilon_r}}{(2m+1)} \exp\left(\frac{q\left(m+(1/2)\right)\varphi_s}{kT_C} \right) F_x \qquad F.\ 9$$

Using *equation F. 1* and applying Gauss' law, the surface potential can be substituted with the applied voltages such that:

$$\varepsilon_0 \varepsilon_r F_y = C_{ox}\left(V_G - V_x\right) \qquad F.\ 10$$

Replacing for the vertical field, *Fy*, using *equation F. 7*, *equation F. 10* above becomes:

$$\varepsilon_0 \varepsilon_r \sqrt{\frac{2qp_i}{\varepsilon_0 \varepsilon_r} \frac{kT_C}{q} \exp\left(\frac{q\varphi}{kT_C} \right)} = C_{ox}\left(V_G - V_x\right) \qquad F.\ 11$$

Rearranging *equation F. 11* above and replacing into *equation F. 9*, the current then takes the form given in *equation F. 12*:

$$\exp\left(\frac{q\left(m+\left(1/2\right)\right)\varphi_s}{kT_C}\right)=\frac{C_{ox}^{2m+1}\left(V_G-V_x\right)^{2m+1}}{\left(2p_i\varepsilon_0\varepsilon_r kT_C\right)^{(m+(1/2))}}$$

$$I=\pm WKp_i^{(m+(1/2))}\frac{\sqrt{2kT_C\varepsilon_0\varepsilon_r}}{\left(2m+1\right)}\frac{C_{ox}^{2m+1}\left(V_G-V_x\right)^{2m+1}}{\left(2n_i\varepsilon_0\varepsilon_s kT_C\right)^{(m+(1/2))}}\ F_x \qquad \textit{F. 12}$$

Simplifying *equation F. 12*, replacing for the lateral field, $F_x = dV_x/dx$, and integrating across the accumulated channel length, L, the drain current then becomes:

$$I\int_0^L \mathrm{d}x=\pm\frac{KWC_{ox}^{2m+1}}{\left(2m+1\right)\left(2\varepsilon_0\varepsilon_r kT_C\right)^m}\int_0^{V_D}\left(V_G-V_x\right)^{2m+1}\ \mathrm{d}V_x$$

$$I=\pm\frac{W}{L}\frac{KC_{ox}^{2m+1}}{\left(2m+1\right)\left(2m+2\right)\left(2\varepsilon_0\varepsilon_r kT_C\right)^m}\times\left[V_G^{2m+2}-\left(V_G-V_D\right)^{2m+2}\right] \qquad \textit{F. 13}$$

Lastly, by adding the threshold voltage effects, V_T, the linear drain current, I_{lin}, and saturation drain current, I_{sat}, expressions are given by *equation F. 14* and *equation F. 15* respectively:

$$I_{lin}=\frac{W}{L}\frac{KC_{ox}^{2m+1}}{\left(2m+1\right)\left(2m+2\right)\left(2\varepsilon_0\varepsilon_r kT_C\right)^m}\times\left[\left(V_G-V_T\right)^{2m+2}-\left(V_G-V_T-V_D\right)^{2m+2}\right] \qquad \textit{F. 14}$$

$$I_{sat}=\frac{W}{L}\frac{KC_{ox}^{2m+1}}{\left(2m+1\right)\left(2m+2\right)\left(2\varepsilon_0\varepsilon_r kT_C\right)^m}\left[\left(V_G-V_T\right)^{2m+2}\right] \qquad \textit{F. 15}$$

Appendix G: Verilog Code for OTFT model

```
// VerilogA for organic_vccs, org_vgsexp, veriloga

`include "constants.vams"
`include "disciplines.vams"

module org_vgsexp(vg, vs, vd, outvgs, outgnd);

input vg ,vs, vd;
output outvgs, outgnd;
electrical vg, vs, vd;
electrical outvgs, outgnd;

parameter real m=0.57 from (0:inf);
parameter real K= 2.15*pow(10,-16)from (0:inf);
parameter real vthdrift=-1.5 from (-1*inf:inf);
parameter real wkd=2000*pow(10,-6) from (0:inf);
parameter real lkd=20*pow(10,-6) from (0:inf);

real vgst, vds, ids, vdint, vsint, Cox, Eo, Epoly, kBOLTZ, TC,
const, REVERSE;
analog
begin
     @(initial_step)
     begin
          Eo = 8.85 * pow(10,-12);
          Cox = 1.2* pow(10,-4);
          Epoly = 3;
          kBOLTZ = 1.38*pow(10,-23);
          TC = 473;
          if (V(vd) > V(vs)) begin
               vdint = V(vs);
               vsint = V(vd);
               REVERSE = -1;
          end
          else begin
               vdint=V(vd);
               vsint=V(vs);
               REVERSE = 1;
          end
          vds = (vdint - vsint) * -1;
          vgst = (V(vg)- vsint- vthdrift)*-1;
          const =(wkd*K*pow(Cox,(2*m
+1)))/(pow(2*Eo*Epoly*kBOLTZ*TC,m)*lkd);
          if ((vgst-vthdrift ) < 0)
               const = 0;
          else
               if (vgst < vds)
```

```
                    ids = const*(pow(vgst,(2*m +2)))/((2*m
+1)*(2*m +2));
               else
                    ids = const*(pow(vgst,(2*m +2))-pow((vgst-
vds),(2*m +2)))/((2*m +1)*(2*m +2));
     end

     if (REVERSE == 1)
     begin
          V(outvgs) <+ ids;
          V(outgnd) <+ 0;
     end
     else
     begin
          V(outvgs) <+ 0;
          V(outgnd) <+ ids;
     end


end
endmodule
```

Appendix H: DRC rules for the Self-Aligned Gap (SAG) process

Drawn layer numbers	***Mask Layer Name***	***Purpose of Layer***
1	ALU1	Defines the initial aluminium layer for OTFTs and diodes. It also allows formation of the self-aligned gap for all devices in the circuit.
2	ALU2	Defines areas where contact between gold and aluminium layers is required as well as completing crossover structures.
3	AU	Defines the chromium/gold features for each OTFT and diode.
4	SU8CO	Defines the areas where crossover structures are produced in order to avoid connections between the Al1 and Al2 layers.
5	ETCH	Defines the areas of aluminum that can be removed after oxide growth. These areas are only required to supply electrical current to specific areas to the circuit for gate dielectric growth to occur.
6	ISOLETCH	Defines the organic semiconductor isolation features for every device in the circuit.
7	GATECON	Protects areas of the aluminium where clean contact is required to the gate. Areas not protected by this layer will be anodized (the gate dielectric will be grown.

Design Layer Rules

Drawn layer 1: ALU1

1.1	Min. width	λ
1.2	Min. spacing	λ
1.3	Min. enclosure by Gatecon	λ
1.4	Min. spacing to Etch	2λ
1.5	Min. spacing to Au	2λ
1.6	Min. spacing Alu1 (no SU8) to Alu2 (unrelated)	3λ
1.7	Min. spacing to Isoletch (unrelated)	2λ
1.8	Alu1 overlap of Isoletch	2λ
1.9	Min. enclosure by Alu2 in Alu2 direction	2λ
1.10	Min. enclosure by Alu2 in perpendicular direction	2λ
1.11	Min. cover by SU8 on Alu1/Alu2 crossover in Alu2 direction	2λ
1.12	Min. cover by SU8 on Alu1/Alu2 crossover in perpendicular direction	4λ
1.13	Min. enclosure by SU8	2λ
1.14	Isoletch overlap for TFT width	2λ
1.15	Min. spacing of Isoletch to Alu1/Gatecon	3λ

Drawn layer 2: ALU2

2.1	Min. width	λ

2.2	Min. spacing	λ
2.3	Overlap contact size of Alu2 to Au	λ
2.4	Overlap of Alu2 on Au to make contact	λ
2.5	Min. spacing to Alu1/Gatecon	λ
2.6	Min. spacing to Alu1 with Gatecon	3λ
2.7	Min. spacing to SU8	4λ
2.8	Min. spacing to Isoletch (unrelated)	4λ
2.9	Min. spacing to Au (unrelated)	2λ

Drawn layer 3: AU

3.1	Min. width	λ
3.2	Min. spacing	λ
3.3	Min. spacing to Gatecon	λ
3.4	Min. spacing to Alu2	3λ
3.5	Min. spacing to Alu2-SU8 spacing	2λ
3.6	Overlap by Isoletch	3λ
3.7	Min. spacing to Isoletch	3λ
3.8	Min. spacing to Alu2 contact edge	3λ

Drawn layer 4: SU8CO

4.1	Min. width	3λ
4.2	Min. spacing to Alu2 for gate contact	3λ
4.3	Min. spacing to Au	2λ
4.4	Min. spacing to Isoletch	2λ
4.5	Min. spacing to Gatecon (unrelated)	3λ
4.6	Enclosure of Gatecon	2λ
4.7	Min. spacing to Alu1/Au contact edge	3λ
4.8	Min. spacing to Alu2/Alu1 cross over	3λ
4.9	Overlap of Gatecon with Alu1	3λ

Drawn layer 5: ETCH

5.1	Min. width	λ
5.2	Min. spacing to Alu1	2λ
5.3	Min. spacing to Au	2λ
5.4	Min. spacing	λ
5.5	Min. spacing to Gatecon	3λ
5.6	Min enclosure of Gatecon	λ
5.7	Min. enclosure of Alu1	2λ

Drawn layer 6: ISOLETCH

6.1	Min. spacing	λ

Drawn layer 7: GATECON

7.1	Min. width	3λ
7.2	Min. spacing	λ

7.3	Min. spacing to Alu1	2λ
7.4	Min. spacing to Etch	λ
7.5	Min. spacing to Au	λ
7.6	Min. enclosure by Etch	λ
7.7	Min. enclosure of Alu1	2λ

Drawn layer 8: CONTACT

8.1	Min. spacing between Alu2/Alu1 contact	3λ
8.2	Min. spacing between Alu2/Au contact	3λ
8.3	Gatecon overlap of Alu1/Alu2	4λ

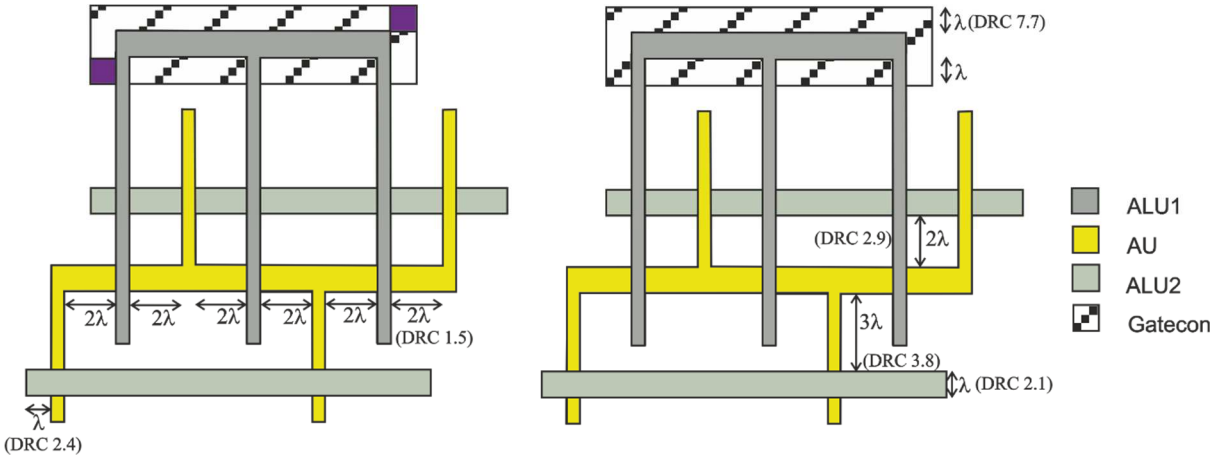

Figure H. 1: Explanation of the DRC rules.

Appendix I: Mask layout of the circuit designs

The layout of the circuits and devices designed in this work is as shown in *Figure I. 1(a)* .The depiction of the mask layout is also shown in *Figure I. 1(b)* with numerical figures used to correspond to the respective circuits and devices as detailed below:

1) A comparator with a latch stage comprising of three sets of inverter stages.
2) Vertical SU8 capacitors.
3) A comparator with a latch stage consisting of a single inverter set.
4) A differential amplifier with a cascading load configuration.
5) A 9-stage ring oscillator.
6) A number of TFTs with varying channel length sizes used for characterising the contact resistances.
7) A differential amplifier with a saturated load transistor.
8) A 5-stage ring oscillator.
9) Test bench for overlap capacitance.
10) Test bench for current mirror.
11) Inverter buffer.
12) Test bench for current source.
13) Diode characterisation with different widths for the Ohmic contact.

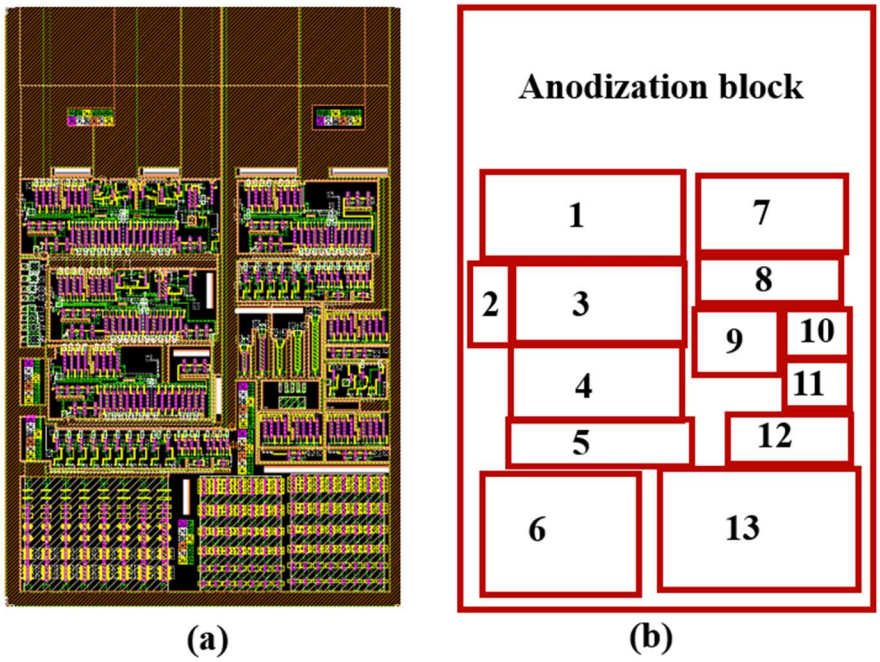

Figure I. 1: Figure (a) showing the layout of the circuits designed in Cadence software and (b) a depiction of the mask layout designs.

Appendix J: Conference and Journal papers

Journal papers

[1] R. W. Wanjau and M. Raja, "*Development and optimisation of a self-aligned gap process for organic lateral Schottky diodes*," (In preparation for submission to Organic electronics journal).

Conference proceedings

[1] R. W. Wanjau, M. Raja and B. Choubey, *IEEE Sensors 2017*, Glasgow, U.K. (2017).
[2] R. W. Wanjau, D. Donaghy and M. Raja, *11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME 2015)*, Glasgow, U.K. (2015).