Growth, Dielectric Properties, and Reliability of High-*k* Thin Films Grown on Si and Ge Substrates

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Abstract

With the continuous physical size down scaling of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), silicon (Si) based MOS devices have reached their limits. To further decrease the minimum feature size of devices, high-*k* materials (with dielectric constants larger than that of silicon dioxide (SiO_2), 3.9) have been employed to replace the SiO_2 gate dielectric. However, there are higher densities of traps in high-*k* dielectrics than in the near trap free SiO_2. Therefore, it is important to comprehensively investigate the defects and electron trapping/de-trapping properties of the oxides. Also, germanium (Ge) has emerged as a promising channel material to be used in high-speed metal-oxide-semiconductor (MOS) devices, mainly due to its high carrier mobility compared with that of silicon. However, due to the poor interface quality between the Ge substrate and gate dielectrics, it is difficult to fabricate high-performance germanium based devices. Therefore, an effective passivation method for the germanium substrate is a critical issue to be addressed to allow the fabrication of high quality Ge MOSFETs.

To solve the above problems, the study of high-*k* materials and the passivation of germanium substrates was carried out in this research. In the first part of this work, lanthanide zirconium oxides ($LaZrO_x$) were deposited on Si substrates using atomic layer deposition (ALD). The pulse capacitance-voltage (CV) technique, which can allow the completion of the CV sweep in several hundreds of microseconds, was employed to investigate oxide traps in the $LaZrO_x$. The results indicate that: (1) more

traps are observed in the $LaZrO_x$ when compared with measurements using the conventional CV characterization method; (2) the time-dependent trapping/de-trapping is influenced by edge times, pulse widths and peak to peak voltages (V_{PP}) of the gate voltage pulses applied. Also, an anomalous behavior in the pulse CV curves, in which the relative positions of the forward and reverse CV traces are opposite to those obtained from the conventional measurements, was observed. A model relating to interface dipoles formed at the high-*k*/SiO_x is proposed to explain this behavior. Formation of interface dipoles is caused by the oxygen atom density difference between the high-*k* materials and native oxides. In addition, a hump appears in the forward pulse CV traces. This is explained by the current displacement due to the pn junction formed between the substrate and inversion layer during the pulse CV measurement.

Secondly, hafnium titanate oxides ($Ti_xHf_{1-x}O_2$) with different concentrations of titanium oxide were deposited on p-type germanium substrates by ALD. X-ray Photoelectron Spectroscopy (XPS) was used to analyze the interface quality and chemical structure. The current-voltage (IV) and capacitance-voltage (CV) characteristics were measured using an Aglient B1500A semiconductor analyzer. The results indicate that GeO_x and germinate are formed at the high-*k*/Ge interface and the interface quality deteriorates severely. Also, an increased leakage current is obtained when the HfO_2 content in the $Ti_xHf_{1-x}O_2$ is increased. A relatively large leakage current density (~10^{-3} A/cm^2) is partially attributed to the deterioration of the interface between Ge and $Ti_xHf_{1-x}O_2$ caused by the oxidation source from HfO_2. The small band gap of

the TiO_2 also contributes to the observed leakage current. The CV characteristics show almost no hysteresis between the forward and reverse CV traces, which indicates low trap density in the oxide. Since deterioration of the interface quality was observed, an in-situ ZnO interfacial layer was deposited in the ALD system to passivate the germanium substrate. However, a larger distortion of the as-deposited sample was observed. Although the post deposition annealing (PDA) has a positive effect on the CV curves, there is an increase in frequency dispersion and the leakage current after PDA. Therefore, the ZnO interfacial layer is not an effective passivation layer for the germanium substrate. In addition, GeO is formed due to the reaction and GeO desorption from the gate oxide/Ge interface occurs, which also leads to the deterioration of the device performance.

In the final part of this work, to circumvent the problems explored above, 0.1 mol/L propanethiol solution in 2-propanol, 0.1 mol/L octanethiol solution in 2-propanol, and 20% $(NH_4)_2S$ solution in DI water were used to passivate the n-type germanium substrates before HfO_2 dielectric thin films were deposited by ALD. The results show that an increase in the dielectric constant and a reduction in leakage current are obtained for the samples with chemical treatments. The sample passivated by octanethiol solution has the largest dielectric constant. The lowest leakage current density is observed for the sample passivated by $(NH_4)_2S$ solution followed by the one passivated by octanethiol solution. In addition, effects of a TiN cap layer on the formation and suppression of GeO were investigated. It was found that the formation of GeO and

desorption of the GeO form gate oxides/Ge interface are suppressed by the cap layer. As a result, an increase in dielectric constant from 8.2 to 13.5 and a lower leakage current density for a negatively applied voltage are obtained. Therefore, the passivation of the substrates by octanethiol or $(NH_4)_2S$ solutions followed by the TiN cap layer is a useful technique for Ge based devices.

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List of Symbols

Symbol	Definition
A	amplification factor
C	capacitance
C_{ox}	oxide capacitance
N	number of the measurement in the determination of R_{rms}
N_{ot}	oxide trap density
Q	charge of interface dipole per unit area
Q_{dep}	depletion charge per unit area
Q_{it}	equivalent charge of interface state per unit area
Q_{ot}	equivalent charge in the oxide
R	resistance
R_{rms}	root-mean-square roughness
T	thickness of the dielectric oxide
V_{FB}	flat-band voltage
V_g	bias voltage applied to a metal gate
ΔV_g	voltage shift of CV traces
V_{PP}	peak to peak voltage
W_f	loop width of forward pulse CV relative to that of conventional CV
W_r	loop width of reverse pulse CV relative to that of conventional CV

d_1	the dipole separation in conventional CV measurement
d_2	the dipole separation of forward sweep under pulse measurements
d_3	the dipole separation of reverse sweep under pulse measurements
i_{ac}	AC current through a capacitor
i_C	current through a capacitor
i_R	current through a resistor
i_{total}	total current through a device
k	dielectric constant
q	elemental charge
t	time
$t_{high\text{-}k}$	thickness of high-*k* thin film
v_{CH1}	voltage signal of channel 1 of an oscilloscope
v_{CH2}	voltage signal of channel 2 of an oscilloscope
v_{ac}	AC voltage applied on a capacitor
$\bar{z}$	average height in the determination of R_{rms}
z_n	measured height in the determination of R_{rms}
ε_{SiO_2}	dielectric constant of silicon dioxide
$\varepsilon_{high\text{-}k}$	dielectric constant of high-*k* thin film
ε_{ox}	dielectric constant of an oxide
$\emptyset_F$	The potential between fermi level and intrinsic fermi level
θ	angle between the dipole and interface

List of Abbreviations and Acronyms

Term	Initial Components of the Terms
Al	Aluminum
ALD	Atomic Layer Deposition
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
a-Si:H	Hydrogenated Amorphous Silicon
CET	Capacitance Equivalent Thickness
C-f	Capacitance-frequency
CMOS	Complementary Metal Oxide Semiconductor
CV	Capacitance-Voltage
Dy	Dysprosium
DI water	Deionized Water
DUT	Device Under Test
ΔE_c	Conduction Band Offset
ΔE_v	Valance Band Offset
E_g	Bandgap
EOT	Equivalent Oxide Thickness
Er	Erbium
FG	Forming Gas

GaAs	Gallium Arsenide
Gd	Gadolinium
Ge	Germanium
GeO_2	Germanium Dioxide
GeO_x	Germanium OSxide
GeOI	Germanium on Insulator
HBr	Hydrobromic Acid
HCl	Hydrogen Chloride
HF	Hydrofluoric Acid
HI	Hydrolodic Acid
H_2	Hydrogen
H_2S	Hydrogen Sulfide
Hf	Hafnium
HfO_2	Hafnium Oxide
$HfSiO_4$	Hafnium Silicate
HSA	Hemispherical Analyzer
InP	Indium Phosphide
InSb	Indium Antimonide
ITRS	International Technology Roadmap for Semiconductors
IV	Current-Voltage
La	Lanthanum

La_2O_3	Lanthanum Oxide
$LaZrO_x$	Lanthanide Zirconium Oxide
MNT	Micro and Nano Technology
MO	Metal-Organic
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N_2	Nitrogen
NS	$(NH_4)_2S$
OH	Hydroxyl
OT	Octanethiol
PDA	Post Deposition Annealing
PECVD	Plasma Enhanced Chemical Vapor Deposition
PMA	Post Metal Annealing
PT	Propanethiol
RTA	Rapid Thermal Annealing
SAED	Selected Area Electron Diffraction
Si	Silicon
Si_3N_4	Silicon Nitride
SiO_2	Silicon Dioxide
$SrTiO_3$	Strontium Titanate
TEM	Transmission Electron Microscope

Ta_2O_5	Tantalum Oxide
$Ti_xHf_{1-x}O_2$	Hafnium Titanate oxide
TiN	Titanium Nitride
TiO_2	Titanium Dioxides
UHV	Ultra-High Vacuum
VT	voltage-time
WT	Without Treatment
XRD	X-ray Diffraction
XPS	X-ray Photoelectron Spectroscopy
Y_2O_3	Yttrium Oxide
ZnO	Zinc Oxide
ZrO_2	Zirconium Oxide
$ZrSiO_4$	Zirconium Silicates

Chapter 1: Introduction and Background Information

1.1 Research Background

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are the key components of an integrated circuit (IC) and the structure of a MOSFET is shown in Figure 1.1. The device consists of a drain, a source, a gate, a gate oxide layer and a channel region beneath the gate oxide. Usually, the drain and source are the heavily doped p-type silicon (Si) if the n-type Si wafer is used as substrate or vice versa. Dielectric materials, such as silicon dioxide (SiO_2) and hafnium dioxide (HfO_2), have been used as gate oxide layers. The gate was made of poly-silicon in the early age of the IC though it is generally made of metal in modern times.

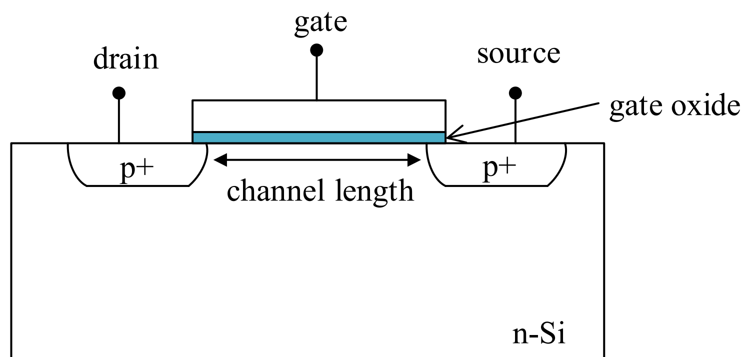

Figure 1.1 The structure of a MOSFET.

From Figure 1.1, it can be seen that two diodes are formed by the drain/substrate and source/substrate positioned connected back-to back when no gate voltage is applied. If a negative voltage is applied to the gate terminal (PMOS in this example), an inversion layer will be formed in the channel region and a current is able to flow between the

drain and source terminals. The voltage required to turn on the MOSFET is called the threshold voltage, V_t. It can be expressed as

$$V_t = V_{FB} + 2\emptyset_F - \frac{Q_{dep}}{C_{ox}} - \frac{Q_{ot} + Q_{it}}{C_{ox}} \tag{1.1}$$

In Formula (1.1), V_{FB} is the flat-band voltage, controlled by the gate material and substrate material used. $\emptyset_F$ is related to the doping concentration of the substrate material. Q_{dep} is the depletion charge per unit area and determined by the substrate material and body bias. The terms, Q_{ot} and Q_{it} are related to the traps in the oxide and the interface between the oxide and substrate. In this research, the traps formed by the interaction of the materials used to manufacture the device will be investigated. As such a MOS capacitor structure, shown in Figure 1.2, will be used as it simplifies the manufacturing process, whilst providing all of the same material interfaces which can be tested for traps in a similar manner to the MOS transistor. Therefore, in the research, a MOS capacitor (shown in Figure 1.2) is a sufficient structure to investigate the performance of a device and the trapping/de-trapping behavior of the charges in the gate oxides.

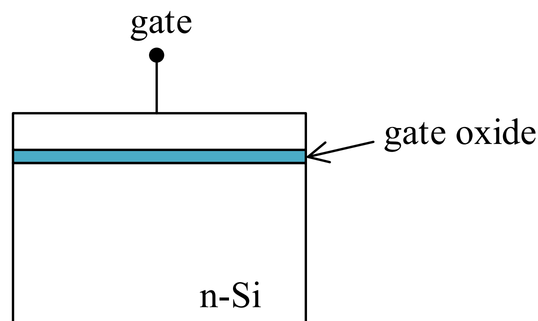

Figure 1.2 The structure of MOS capacitor.

In order to integrate more MOSFETs within the unit area of a chip, over the years since its inception, the size of the MOSFET has been continuously scaled down. The process technology developed from 10 μm in the middle of the 20th century to state-of-the-art processes for 14 nm nowadays. It is believed that miniaturization of the device size will continue to drive the development of IC technology. However, the traditional SiO_2 dielectric based devices have reached their physical limitations due to the material properties of the oxide. When the thickness of the SiO_2 gate dielectric decreases below 1.2 nm, electron tunneling effects and leakage current (>10 A/cm^2) become serious obstacles in relation to device operation and power consumption [1, 2]. To further decrease the size of devices, high-*k* materials, materials with dielectric constants larger than that of SiO_2, 3.9, have been employed to replace the SiO_2 gate dielectrics. For example, in 2007, MOSFET technology substituted the SiO_2 for a hafnium-based high-*k* material [3]. With the introduction of high-*k* materials, a smaller equivalent oxide thickness (EOT) is obtained from a greater physical thickness compared to that of the SiO_2 gate dielectric [4]. A small EOT is desired in order to scale down the size of devices and the large physical thickness is required to ensure a small leakage current. As reported by Nadimi, the leakage current densities for hafnium oxide (HfO_2) and SiO_2 decrease by 0.31 decade/Å and 0.49 decade/Å, respectively, with the increase of oxide thickness [5]. The formula for calculation of EOT is shown in Formula (1.2).

$$\mathrm{EOT} = \frac{\mathrm{t}_{\mathrm{high}-k} \cdot \varepsilon_{\mathrm{SiO_2}}}{\varepsilon_{\mathrm{high}-k}}, \tag{1.2}$$

where $t_{high\text{-}k}$ is the thickness of the high-k material, $\varepsilon_{high\text{-}k}$ is the relative permittivity of the high-k material and ε_{SiO_2} is the relative permittivity of SiO_2, 3.9.

Formula (1.2) shows that through the employment of high-k materials, gate dielectrics with a small EOT can be obtained without causing an increase in gate leakage current, which is one of the most significant issues related to device operation and power consumption [6-10]. A number of high-k materials, HfO_2, ZrO_2, Y_2O_3, and their silicates, have been widely studied due to their relatively high dielectric constants [11, 12]. In addition to increasing the dielectric constant of the gate oxide, it is also desired to have a larger band gap and band offset to that of the substrate material. If the conduction band offset (ΔE_c) from the substrate material for the gate oxide is much less than 1.0 eV, it will likely to preclude its use, since electron transport, either by thermal emission or tunneling, will lead to unacceptably high leakage currents [13]. As the ΔE_c for a number of potential ternary gate dielectrics have not been reported previously, the closest and most readily attainable indicator of the band offset is considered to be the dielectric band gap (E_g). Usually, a large E_g corresponds to a large ΔE_c. In addition, the higher the dielectric constant the dielectric material has, the narrower the band gap it will have. Therefore, a tradeoff between the two factors should be considered when the potential dielectric material is selected. The electrical properties of some widely studied high-k materials are listed in Table 1-1.

From Table 1-1, the reported dielectric constants of the binary oxides with acceptable band gaps are not high enough (to scale down to EOT$<$0.5 nm), and hence would not allow further scaling of the MOSFETs [20, 21]. In order to overcome this problem, a number of trials have been carried out to further increase the permittivity of these dielectrics. For example, zirconium oxide (ZrO_2) exhibits a wide range of crystal phases

each with a different dielectric constant, in theory, ranging from 16 for the monoclinic phase to 47 for the metastable tetragonal phase [22].

Table 1-1 Electrical properties of high-*k* dielectrics [14-19]

Dielectric Materials	Dielectric Constant	Band Gap (eV)
Si_3N_4	7.1	5.3
Al_2O_3	8.5	6.7
HfO_2	21	4.7
Ta_2O_5	26	4.4
ZrO_2	29	5.8
Y_2O_3	15	6.0
TiO_2	60	3.2
$SrTiO_3$	120	1.8
$HfSiO_4$	11	6.5

Some researchers have indicated that ZrO_2 with metastable tetragonal and cubic phases, with higher *k*-values, can be stabilized by adding small amounts of rare earth elements (such as lanthanum (La), Gadolinium (Gd), Dysprosium (Dy), Erbium (Er), *etc.*) [23-27]. Lightly lanthanum doped zirconium oxide is considered to be one potential candidate that could be used to reduce EOT and hence allow scaling of the transistor size. However, a significant dielectric relaxation accompanies the increase in dielectric constant for lanthanide zirconium oxide ($LaZrO_x$) [28]. Generally, the dielectric relaxation represents the frequency dispersion of the dielectric material. In detail, the capacitance of the MOS capacitor will decrease with an increase in measurement frequency. This phenomenon is partially caused by extrinsic factors, such as series resistance, parasitic effects, lossy interfacial layers, leakage currents, and surface roughness of dielectric layers [29]. However, in the case of $LaZrO_x$, the intrinsic factors are the main cause for the dielectric

relaxation. Three intrinsic causes for the dielectric relaxation are: 1) ion movement of interstitial La^+ or Zr^+ ions in the metal-oxide lattice [30]; 2) the combination of unbound metal ions with electron traps, generating dipole moments and inducing dielectric relaxation [31]; and 3) decrease in crystal grain size, causing an increase in the dielectric relaxation due to increased stresses [32, 33].

Besides doping with rare earth elements, another possible way of increasing the dielectric constant of the dielectrics is to mix the oxide with other dielectric materials of a higher relative permittivity, such as titanium oxide (TiO_2, which has $k\approx60$). The high dielectric constant of the TiO_2 originates from the soft phonons of titanium, and it increases the overall dielectric constant of the gate oxide [34-36]. Despite the increase in dielectric constant of the dielectric material through mixing it with TiO_2, the small band gap of TiO_2 [37] will result in a large leakage current, this remains an issue to be considered [34]. Therefore, although the ternary oxides may be a solution to further reducing the EOT and hence scaling down the size of the transistor, more research needs to be carried out to address the accompanied problems and a great amount of attention has been attracted from both industrial and academic researchers [6, 30, 34, 36, 37].

Although EOT can be reduced by employing high-*k* materials, the quality of the high-*k* material is typically inferior to that of the conventional SiO_2 based gate dielectrics. High-*k* dielectrics exhibit a significant number of defects which have been proven to result in the instability of devices, such as threshold voltage instability [38-42]. Also, most of the charge traps in the bulk of the material are difficult to detect or probe using traditional CV/IV techniques due to the charge loss over the long time scales taken for the measurements [43, 44]. With regard to the photo IV technique, it is used to assess the spatial distribution of charges [45, 46], but the measurement is too slow to characterize defects near the interface because of fast de-trapping [47, 48].

Therefore, in order to investigate the effect of charge trapping/de-trapping by the defects and provide possible explanations for the phenomena caused by the defects, a number of fast measurement techniques, such as the charge injection and sensing technique [49], the pulse IV technique [50-53] and the pulse CV technique [54-56] have been developed. Over the course of this study, a pulse CV method, able to complete the CV sweep in several hundreds of micro seconds, was developed. The detailed working principle and mechanism of this measurement system will be discussed in Sections 2.3 and 3.1. Using this powerful method, more trapped charges can be detected in comparison to conventional methods. This improvement is attributed to the fast characterization of the pulse CV technique resulting in less de-trapping when compared with conventional methods, therefore, more traps can be measured. In addition, the time-dependent trapping/de-trapping of the traps can be traced by changing the edge time, width and peak to peak voltage (V_{PP}) of the pulse applied.

As the transistor size becomes small enough (EOT<0.5 nm), the operation speed of a transistor is dominated by the injection velocity at the source region of a MOSFET rather than the saturation velocity [57, 58]. The injection velocity is the velocity of positively and negatively directed fluxes and is proportional to the mobility of the semiconductor material. Therefore, high-mobility channel materials offer one of possible option towards improving the performance of future nanoelectronic devices. The electrical properties of several potential channel materials are compared with Si at 300 K in Table 1-2 [58-60].

From the parameters in Table 1-2, germanium is seen to be a semiconductor material of great potential for the fabrication of MOSFETs. Firstly, both the electron and hole bulk motilities of Ge are higher than those of Si [58] and can also be enhanced by strain [61]. The smaller bandgap, E_g, of Ge compared to that of Si allows the supply voltage to be

further reduced despite a significant increase in leakage current and reverse current density of a pn junction [62-64].

Table 1-2 Electrical properties of potential channel materials for future nanoelectronics.

	Ge	Si	GaAs	InSb	InP
Bandgap (eV)	0.66	1.12	1.42	0.17	1.35
Electron affinity (eV)	4.05	4.0	4.07	4.59	4.38
Hole mobility ($cm^2V^{-1}s^{-1}$)	1900	450	400	1250	150
Electron mobility ($cm^2V^{-1}s^{-1}$)	3900	1500	8500	80000	4600
Lattice constant (nm)	0.565	0.543	0.565	0.648	0.587
Dielectric constant	16	11.9	13.1	17.7	12.4
Melting points (°C)	937	1412	1240	527	1060

Moreover, the process technology is compatible with the Si CMOS process technology. Therefore, Ge is considered to be one of the most promising channel materials for the future of nanoelectronics. However, due to the instability of germanium native oxides and the poor interface quality between germanium substrates and dielectric oxides [65, 66], selection of a suitable passivation technique presents a major technical hurdle to overcome before Ge can be used to make high-performance MOSFET devices. Generally, except for the interface quality of SiO_2 on Si, the oxide layer (including native oxide) is insufficient to passivate the surface of semiconductor substrates [59]. With regard to the deterioration of the germanium interface, it has been widely conjectured to be attributed to the formation of GeO_x at the interface between the Ge substrate and the deposited dielectric thin film [67, 68]. In addition, a typical reaction for a GeO_2/Ge interface as shown by Formula (1.3), will lead to the reduction of GeO_2 and generation of volatile GeO [69, 70]. GeO desorption from the gate oxide/Ge interface and diffusion across the thin film will also deteriorate the quality of dielectric thin films.

$$GeO_2 + Ge \rightarrow 2GeO \quad (1.3)$$

Proof of this phenomenon has been supported by inspecting the thickness of the GeO_2 layer deposited on Ge and SiO_2/Si substrates in published research [68]. The deterioration caused by the reaction between the GeO_2 layer and Ge substrate will lead to a large hysteresis (of around 1.5 V) in the measured CV curves as observed for the Ge/GeO_2 gate stacked MOS capacitor [67]. The hysteresis (also called loop width) is defined as the voltage shift between the reverse and forward CV traces. A detailed description of this phenomenon will be presented in Section 2.4.

The dielectric constant of the Ge oxide can be as low as 7, which limits the potential scaling of the MOS device. Therefore, the removal of Ge oxides from the Ge substrate prior to the deposition of a high-*k* thin film is a necessary step in achieving an EOT below 0.5 nm as required in the International Technology Roadmap for Semiconductors (ITRS) [71]. One effective method of decreasing the amount of Ge oxide is through the application of an acid pretreatment, using for example halogen acid (HF, HCl, HBr, and HI) [59, 72]. In addition, oxidizing the insoluble GeO_x into soluble GeO_2 using oxidizing agents, such as O_2, O_3, and H_2O_2, has also been attempted for removal of the oxide. However, it should be emphasized that a certain amount of Ge oxide still remains due to inefficient acid treatment and the re-oxidation process during the transfer of samples. The residual germanium oxide will diffuse into the high-*k* film and deteriorate the quality of the device. Therefore, a cap layer technique has been proposed to suppress the desorption of the GeO from the gate oxide/Ge interface to the high-*k* oxides. An Si cap has been attempted in previous research, in which CV characteristics with less distortion were observed compared with that without the cap layer [75]. In the research work, a GeO_2 dielectric layer was deposited on a Ge substrate. The reaction described

by Formula (1.3) occurred and GeO at the interface between the dielectric layer and substrate was formed. When the Si cap layer was placed on top of the GeO_2 thin film, it is considered that it blocks the diffusion of the GeO to the air and, therefore, the chemical potential of the GeO inside the film is increased. The reaction rate of GeO_2 at the interface, as described by Formula (1.3), decreases due to the equilibrium of the reaction. The mechanism is considered to suppress the formation of GeO [68].

Besides the cap layer technique, a number of other techniques have also been proposed to directly passivate the germanium surface after the removal of GeO to improve the electrical performance of the devices. These passivation techniques include NH_3 treatment [76], surface nitridation [77-81], SiH_4 treatment [82], AlN_x passivation [83, 84], sulfur treatment [85-87], aluminum oxide passivation [21], high-quality GeO_2 passivation [88, 89].

In addition to the unwanted desorption of GeO due to the reaction of the GeO_2 and substrate, the relatively low dielectric constant of GeO_2 is also a fatal problem preventing further scaling of the MOS device. High-*k* material offers is a possible solution to this problem. However, for high-*k* materials deposited on Ge substrates, there are two main requirements: obtaining a small EOT (<0.5 nm) and a thermally stable property with the substrate (used as passivation layer or dielectric layer). Unfortunately, one of the most promising high-*k* materials tried on Si substrates, HfO_2, is unsuitable for direct application onto a Ge substrate, since as reported by Van Elshocht [78] and Xie [90], the diffusion of Ge into the HfO_2 layer leads to poor electrical properties, unless a good interfacial layer or suitable passivation technique is used. So, stabilization of a high-*k*/Ge interface is a key issue for the fabrication of Ge MOS devices.

Detailed working principles of an effective passivation method for the Ge surface and the corresponding mechanism remain open questions. The criteria for selecting a high-*k* gate insulator to realize a good interface with the Ge substrate should be: (1) readily intermixable with interfacial Ge oxide only at the interface and a germinate with less defects is formed; and (2) an amorphous thin film is formed, which can restrict Ge diffusion into the high-*k* film and hence GeO desorption through the high-*k* thin film. However, in most cases, the native oxide cannot be completely removed and intermixing cannot be avoided during the deposition of dielectrics (or during subsequent treatments, such as post-deposition annealing (PDA)). An excess incorporation of Ge into the high-*k* layer quickly deteriorates electrical characteristics, such as forming an increase in hysteresis in the CV characteristics and mobility degradation [91]. In future research and industrial application, a variety of high-*k* materials will be applied. Criteria defined based on results and physical analysis will be helpful in the selection of the high-*k* dielectrics in the application of Ge substrate MOS devices.

In reality, there is comparatively less economic Ge than Si available and hence less production of bulk Ge wafers. Ge channels integrated on other substrates as thin surface layers, such as Ge-on-Insulator (GOI) [92-94], Ge-on-Si [95, 96], are considered to be some of the potential solutions to improving future device performance. SiGe substrates may also be a realistic option for obtaining relatively high mobility [97, 98].

1.2 Outline of Work

The SiO_2 based device has reached its physical limit due to the rapid scaling of MOSFETs. In order to continue the scaling of MOSFETs, high-*k* oxides have been employed as gate oxides. However, the larger number of defects in high-*k* oxides

compared with those in SiO_2 leads to the instability of such MOS devices. A fundamental understanding of the traps in new dielectric materials is a critical issue. A high-*k* material, $LaZrO_x$, was deposited on n-type silicon substrate and the corresponding MOS capacitor was fabricated. A pulse CV system was developed and employed to investigate the charge trapping/de-trapping behavior in the oxide. The pulse CV system is capable of completing the CV sweep in several hundreds of microseconds allowing more traps to be detected compared with conventional CV measurement systems. In addition, when the pulse CV measurements were performed on MOS capacitors with non-stoichiometric oxides native to the substrates, an anomalous behavior in the CV curves was observed. In order to explain this anomalous phenomenon in the CV curves, a hypothesis that successfully explains most of the abnormal features was proposed. Furthermore, the effects of deposition and annealing conditions on the pulse CV behavior were also explored. Additionally, a hump in the weak inversion region of the forward pulse CV trace was also observed and a corresponding explanation for this was provided.

Due to the higher carrier mobility of germanium, it has emerged as a promising candidate for the channel material in high-speed MOSFET devices [99, 100]. However, the unstable native oxide and the poor interface quality between the germanium substrate and dielectric oxide make it difficult to be applied in the fabrication of a MOSFET. Also, there is a debate on the impact of GeO_x on the device performance. Therefore, research into the physical and electrical properties of $Ti_xHf_{1-x}O_2$ on germanium substrates was carried out. X-ray Photoelectron Spectroscopy (XPS) was used to investigate interfacial quality and chemical structure. The Agilent B1500A semiconductor device analyzer was used to measure the gate leakage current and CV characteristics. The correlation between the gate leakage current and interface quality

of the samples is studied. In addition, an in-situ ZnO interfacial layer in atomic layer deposition (ALD) was attempted to passivate the substrate and the effects of PDA were also explored.

An effective passivation technique for germanium surfaces is known to be a significant hurdle to overcome before Ge can be used to make high-performance MOS devices, due to the poor interface quality between high-*k*/Ge materials as described in Section 1.1. The deterioration of the germanium interface is widely believed to be due to the reaction of the dielectric oxides and germanium substrates and diffusion of GeO formed during the reaction. Therefore, two techniques were attempted to suppress the deterioration of germanium interface quality. Firstly, previous research outputs have reported that the introduction of sulfur in the GeO_x can result in a superior Ge gate stack. Therefore, wet chemical treatments with both organic and inorganic solutions were performed on the germanium substrates to form a sulfur monolayer. Secondly, a TiN cap layer was deposited on the high-*k* oxide to suppress the formation of volatile GeO, which would otherwise degrade the quality of the dielectric thin film.

1.3 Aims and Objectives

This research aims to fabricate Ge MOS capacitors with high-*k* dielectric materials using an effective passivation method, which is important for the application of Ge MOS devices. This will make a contribution to the development of ICs with germanium wafers. The following three objectives will be realized in achieving the aims of the thesis:

I. To deposit high-*k* dielectric thin films on Si substrates using ALD and to investigate the oxide traps in the dielectrics, including the number of traps and time-dependent trapping/de-trapping behavior of the charges, using a developed pulse CV system.

Explanations for the behaviors in the pulse CV traces are to be provided.

II. To deposit high-*k* thin films on Ge substrates and analyze the interface quality and chemical structure and their relationships to the CV/IV characteristics. To passivate the Ge substrate and investigate the CV/IV characteristics of the MOS capacitors with an in-situ passivation method.

III. To analyze the effect of different wet chemical treatments on germanium substrates and investigate the impact of a cap layer on electrical properties of Ge MOS capacitors, including dielectric constant, frequency dispersion and leakage current. Models related to the observed phenomenon are to be proposed.

1.4 Original Contribution

I. A current probe was replaced by an amplifier connected to an oscilloscope in the developed pulse CV system. The system is more cost-effective and can be updated more easily when compared to the current probe. In addition, for the pulse CV characteristics, the relative positions of forward and reverse CV traces are opposite to those obtained from conventional measurements. A model related to interface dipoles was proposed to explain the anomalous behavior.

II. There is a debate on the role and effect of the GeO_x and germinate at the high-*k*/Ge interface and no solid conclusion has been determined. In this research, the formation of GeO_x and germinate at the interface between Ge substrates and $Ti_xHf_{1-x}O_2$ gate oxides was observed and a severe deterioration of the interface

quality was detected by using XPS. The deterioration of the interface between Ge and $Ti_xHf_{1-x}O_2$ is caused by the oxidation source from HfO_2, which leads to an increase in leakage current.

III. Propanethiol solution and octanethiol solutions were used to passivate the n-type germanium substrates for the first time. The results show that all the passivated samples have a larger dielectric constant and lower leakage current density when compared with the control sample. In addition, the TiN cap layer was employed to suppress the formation of volatile GeO, which was considered to deteriorate the quality of the gate oxides. As a result, the dielectric constant of the oxide layer increases from 8.2 to 13.5 and a lower leakage current density is obtained when a negative voltage is applied. Compared with the Si cap layer, no additional processes, such as ex-situ plasma enhanced chemical vapor deposition (PECVD), are required for the TiN cap layer.

1.5 Published works

Journal Articles

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[1] **Qifeng Lu**, Yifei Mu, Yinchao Zhao, Ce Zhou Zhao, Sang Lam, Yuxiao Fang, Li Yang, Chun Zhao, Steve Taylor and Paul R. Chalker, *Effect of Surface Passivation and Post-Metal Annealing on Electrical Performance of Ge MOS Devices with HfO_2 Gate Dielectric*, 17: 526 – 530, ***IEEE Transactions on Device and Materials Reliability*** (2017).

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Conference Papers

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[1] **Qifeng Lu**, Sang Lam, Yifei Mu, Ce Zhou Zhao, Yinchao Zhao, Yuxiao Fang, Li Yang, Steve Taylor and Paul R. Chalker, *Atomic Layer Deposition of HfO_2 Gate Dielectric with Surface Treatments and Post-metallization Annealing for Germanium MOSFETs,* ***The 17th IEEE International Conference on Nanotechnology,*** 25-27 Jul 2017, Pittsburgh, USA.

[2] Yanfei Qi, Yuxiao Fang, Chun Zhao, **Qifeng Lu,** Chenguang Liu and Ce Zhou Zhao, *Influence of HfAlO Composition on Resistance Ratio of RRAM with Ti electrode,* ***The 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits****,* 4-7 Jul 2017, Chengdu, China.

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Books

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Patents

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[1] **Qifeng Lu**, Jingjin Wu, Ce Zhou Zhao, *A surface passivation method for Ge MOS device with ALD deposited high-k dielectrics*. No. CN 205177850 U.

1.6 Chapter Outline

In Chapter 1, the background information, including the structure of the device, the advantage of the high-*k* materials, the updated CV characterization technique and the challenges faced by the Ge MOS devices, were presented. The aims and objectives of this thesis and the main contributions are also covered in this chapter.

In Chapter 2, ALD is described together with the working mechanism. The E-beam evaporator used for the deposition of metal gates is introduced briefly. The fabrication processes and a summary of the samples used in this research are shown in Section 2.1. The physical and electrical characterization techniques are presented in Sections 2.2 and 2.3. The related technical terms used in following discussions are introduced in Section 2.4 in order to provide some background theory.

In Chapter 3, a pulse CV system which has been developed was employed to explore the CV behavior of MOS capacitors with $LaZrO_x$ gate oxides. The behavior of charge trapping/de-trapped was investigated and discussed in detail. An abnormal CV behavior was observed when the pulse CV technique was applied to MOS capacitors with some high-*k* dielectrics. In addition, a hump in the weak inversion region of the forward pulse CV trace was also observed. The corresponding models used to explain these phenomenon were proposed. The description and explanation for these two behaviors are presented in Section 3.3.

In Chapter 4, $Ti_xHf_{1-x}O_2$ thin films, with different concentrations of titanium oxides, were deposited on p-type Ge substrates. XPS was employed to analyze the interface

quality and chemical structure. The results are presented in Section 4.1. Due to the deterioration of the interface for direct application of high-*k* materials on Ge substrates, in-situ ZnO thin films were used as the interfacial layer between the high-*k*/Ge interface. The effect of PDA on the device performance was also investigated. The results and discussions are presented in Section 4.2

In Chapter 5, propanethiol and octanethiol solutions were used to passivate the Ge substrates in Section 5.1. Also, forming gas (FG, 10% H_2 and 90% N_2) annealing was performed and better interface quality and smaller delta loop width under long-time stress were obtained when the samples were annealed in a FG environment. Furthermore, since the diffusion of GeO into the high-*k* thin films is considered to be one of the factors resulting in the deterioration of the device performance, a TiN cap layer was fabricated to suppress the formation of violate GeO in Section 5.2. As a result, a higher dielectric constant and a lower leakage current density for negatively applied voltages were obtained.

In Chapter 6, conclusions for the corresponding objectives are provided in each section. Also, future research directions in which to continue the research are discussed.

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Chapter 2: Methodology and Experimental Processes

The thickness of the dielectric oxide is only on the order of several nanometers in the MOSFETs nowadays, therefore, a deposition technique, which can control the thin film thickness precisely and uniformly, is required. In this chapter, ALD, which is able to control the thin film thickness at the monolayer level, is used to deposit high-*k* gate dielectrics. It is described together with its working mechanism. The precursors and corresponding oxidation source employed to deposit the high-*k* thin films are listed. The E-beam evaporator, a PVD system, is introduced briefly which was used in this work to deposit the metal gates for the MOS capacitors. All of the fabrication procedures used to manufacture the samples produced will be provided in detail. The techniques used to characterize the physical and electrical properties of the thin films are presented in Sections 2.2 and 2.3.

2.1 Background Theory and Sample Preparation

With the scaling down of the device size, the thickness of the dielectric oxide is now only on the order of several nanometers [1]. A dielectric deposition method, which can deposit contamination-free thin films with precise and uniform-controlled thickness, is required in future IC fabrication. ALD is one of the most attractive solutions and it was employed to deposit the high-*k* dielectrics in this research work. ALD is a useful technique to deposit ultrathin films with excellent uniform and conformal structure because of its sequential and self-limiting surface reaction. The thickness of the thin film can be controlled at the monolayer level. Usually, the ALD process is a binary

reaction sequence where a surface exchange reaction between the chemisorbed metal-containing precursor and the oxidant source occurs to form a binary compound thin film. The reaction sequence is shown in Figure 2.1. Firstly, a precursor in its vapor phase is initially injected into the processing chamber at a pressure of 10 Pa followed by a purge to remove the unreacted precursors from the chamber. Then, the oxidant source is introduced into the chamber to react with the absorbed metal-organic precursor followed by a purge to remove the unreacted precursors and byproduct. Although ALD deposition is a self-limiting and surface-controlled process theoretically, unfortunately, most commonly used precursors for oxide growth do not exhibit a perfectly self-limiting process. Also, the relatively high concentration of residual impurities originating from the alkane of the precursors and byproducts is unfavorable for gate dielectrics. Therefore, the deposition rate and the quality of the thin films are dependent on the deposition temperature and the choice of the precursor.

In this research, two ALD systems were used, the Micro and Nano Technology (MNT), Wuxi, China or OpAL™, Oxford, UK. The selected metal-organic (MO) precursors used to deposit the high-*k* thin films are listed in Table 2-1. Since commercial ALD systems and precursors were employed, the deposition conditions, including deposition temperatures, precursor temperatures, pulse time of the precursor, purge time etc., were set based on the manuals provided by the manufacturers.

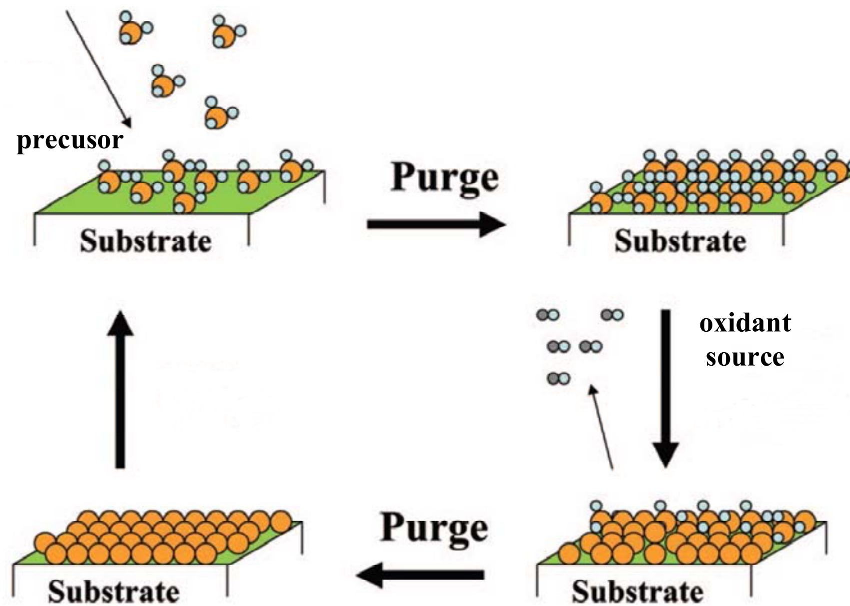

Figure 2.1 Schematic representation of reaction sequence in ALD deposition [2].

Table 2-1 MO precursor and corresponding oxidation source for ALD deposition.

Dielectrics	MO precusor	Oxidation Source
La_2O_3	$(^iPrCp)_3La$	DI water
ZrO_2	$Zr(NMe_2)_4$	DI water
TiO_2	$Ti(O\text{-}^iPr)_4$	DI water
TiO_2	$Ti(NMe_2)_4$	DI water
HfO_2	$Hf(NMe_2)_4$	DI water
Al_2O_3	TMAl	DI water

For the deposition of the metal gates, an E-beam evaporation system from Technol Co., Beijing, China, was employed. E-beam evaporation deposition is a form of physical vapor deposition. A target material is bombarded with an electron beam generated by a tungsten filament. The kinetic energy of the electrons is converted into thermal energy once the electrons strike the target. As the target heats up, the target material will begin to melt or sublimate. Under high vacuum conditions, the target

material will be transformed into its gaseous phase and it can be used to coat surfaces. In this work, aluminum (Al) and titanium nitride (TiN) target materials were used to deposit the metal contacts.

In this thesis, several samples were prepared. Firstly, $LaZrO_x$ thin films were deposited on n-type silicon wafers by ALD. From the published research, there are expected to be a number of traps, in different energy levels, in $LaZrO_x$ thin films [3]. These samples were used to investigate the charge trapping and de-trapping behavior in oxides using the pulse CV techniques developed, results can be found in Sections 3.1 and 3.2. During the measurement, pulse voltages with different edge times, pulse widths and V_{PP}'s were applied to the gate terminal to investigate the time-dependent behavior of the traps. The detailed procedure for the preparation of the samples is described in the following.

The $LaZrO_x$ thin films were deposited on n-type Si (111) wafers with resistivity of 1–10 Ω·cm by ALD at 300 °C using $Zr(NMe_2)_4$ and $(^{i}PrCp)_3La$ as precursors. Deionized (DI) water was used as the oxidant source. The cycle ratio of zirconium oxide to lanthanum oxide was 9:1 and a total number of 200 ALD cycles were performed. After deposition of the gate dielectric, aluminum electrode contacts with a diameter of 0.3 mm were deposited by E-beam evaporation.

In Section 3.3, ZrO_2 thin films were deposited on n-Si (100) wafers with 150 ALD cycles at 150 °C, 200 °C, and 250 °C using 130 °C $Zr(NMe_2)_4$ as precursors. HfO_2 thin films were deposited on the same type of substrates with 150 ALD cycles at 200 °C

using 120 °C $Hf(NMe_2)_4$ as precursors. Aluminum gate contacts with a diameter of 0.3 mm were deposited by E-beam evaporation to form MOS capacitors. Each ZrO_2 sample was cut into three pieces, two of which were annealed in nitrogen and FG environments, respectively, for 30 minutes at 350 °C. The samples were labeled "as-deposited", "N_2", and "FG".

In Section 4.1, $Ti_xHf_{1-x}O_2$ thin films, with thicknesses of 5 nm, 10 nm and 15 nm, were deposited on p-type germanium wafers to investigate the interface quality between the high-*k* oxide and germanium substrates using XPS. XPS is a surface sensitive technique, so the interface was probed by using a 5 nm thickness thin film. The change of chemical structure was discussed by the comparison of the XPS results from samples with different thicknesses. The IV and CV characteristics of the samples were measured using an Agilent B1500A semiconductor device analyzer. For the deposition of $Ti_xHf_{1-x}O_2$, firstly, the ALD growth rates of TiO_2 and HfO_2 were tested individually. 40 °C titanium isopropoxide and 100 °C $Hf(NMe_2)_4$ were used as the ALD precursors. All depositions were performed at a substrate temperature of 300 °C using the ALD system from Oxford Instruments OpAL™, Oxford, UK. From the thickness measured by ellipsometer, the estimated deposition rates for TiO_2 and HfO_2 were approximately 0.203 Å/cycle and 0.166 Å/cycle, respectively. Based on the growth rates, the cycle ratio of TiO_2 to HfO_2 was evaluated to obtain the required $Ti_xHf_{1-x}O_2$ dielectric oxides, with x being 1, 0.9, 0.25, and 0, in terms of thickness. According to the cycle ratio and deposition rates, the total cycles were designed to deposit the thin films with thicknesses of 5 nm, 10 nm and 15 nm on p-type Ge wafers with an Al_2O_3 passivation layer

(~0.3 nm). XPS was used to characterize the interface quality and thin film structure of high-*k* dielectrics deposited on Ge wafers. Aluminum gate electrodes with a diameter of 0.3 mm were deposited by E-beam evaporation to form the MOS capacitors.

In addition, in order to investigate the effect of the in-situ ZnO passivation layer and PDA on $Ti_xHf_{1-x}O_2$ thin films in Section 4.2, three samples of $Ti_{0.1}Hf_{0.9}O_2$ were deposited at 200 °C on n-Ge substrates by ALD using 50 °C $Ti(NMe_2)_4$ and 120 °C $Hf(NMe_2)_4$. Two of the samples received PDA in a nitrogen environment for 30 seconds at 450 °C and 550 °C, respectively. The IV and CV characteristics of the samples were measured using an Agilent B1500A semiconductor device analyzer. In regards to the fabrication process, all of the n-Ge substrate were cleaned ultrasonically in acetone and isopropanol followed by 20% $(NH_4)_2S$ solution treatment at 75 °C for 15 minutes before the deposition of high-*k* dielectrics. Thin films with a cycle ratio of TiO_2 to HfO_2 being 1:9 and 100 ALD cycles were deposited. After the deposition of the $Ti_{0.1}Hf_{0.9}O_2$ thin films, two samples received PDA in a nitrogen environment for 30 seconds at 450 °C and 550 °C, respectively. Aluminum gate electrodes with a diameter of 0.3 mm were deposited by E-beam evaporation to form MOS capacitors.

In Section 5.1, in order to investigate the effect of the passivation method, MOS capacitors with germanium substrates with different passivation techniques were prepared. In addition, the annealing of the samples in FG was carried out to explore the influence of FG annealing. For the fabrication of the samples, firstly, wet chemical treatments were used to passivate the substrates before the deposition of the HfO_2 dielectrics. From previous research [4], the propanethiol and octanethiol treatments

have significant effects on preventing surface oxidation for nanowires. Therefore, germanium wafer pieces were immersed into propanethiol solution (0.1 mol/L in 2-propanol) and octanethiol solution (0.1 mol/L in 2-propanol) for 24 hours to form the -HS passivation layer and labeled PT and OT, respectively. To prevent substantial evaporation of the solution during exposure, the container holding the samples was sealed with Parafilm. After the passivation layer was formed, the Ge substrates were cleaned in 2-propanol and blow-dried with N_2 [4]. Another substrate was dipped in a 20% $(NH_4)_2S$ solution in water for 15 minutes at 75 °C (labelled NS) and dried under an N_2 flow. This sample was used as a comparison for those treated by organic solutions. The sample without any treatment, labeled WT, was the control sample. After chemical treatments, the samples were immediately transferred into the ALD reactor, where 150 ALD cycles were used to deposit the HfO_2 thin films. Aluminum electrode contacts with a diameter of 0.3 mm were deposited by E-beam evaporation. Each sample was cut into two pieces, one of which was annealed in FG at 350 °C for 30 minutes and the effect of annealing in FG on device performance was explored. All of the electrical characteristics, including IV and CV curves, were measured using an Agilent B1500A semiconductor device analyzer.

In order to investigate the effect of using a TiN cap on the electrical properties of MOS capacitors with HfO_2 thin films on n-Ge (100), samples with Al and Al/TiN gate electrodes with a diameter 0.3 mm were fabricated in Section 5.2. IV and CV curves were measured using an Agilent B1500A semiconductor device analyzer. For surface passivation techniques and deposition conditions of the thin films, they were the same

as the conditions for the sample deposited in Section 5.1 except for the ALD cycle number (100 cycles in Section 5.2).

To show the purposes of designation and the samples used in this research clearly, the information is listed in Table 2-2 and Table 2-3.

Table 2-2 Purpose for the design of the samples.

Section	Purpose
3.1	Application of the pulse CV system
3.2	Investigation of charge trap/de-trapping in the oxides
3.3	Exploration of the anomalous CV behavior caused by the interface diploes, including the effect of deposition and annealing condition on the CV behaviors
4.1	Investigation of interface quality and change of chemical structure between the high-*k* oxide and germanium substrates
4.2	Investigation of effect of the in-situ ZnO passivation layer and PDA on CV and IV characteristics
5.1	Study on the effect of the passivation method and FG annealing on the physical and electrical properties of the samples
5.2	Study on effect of TiN cap layer on the electrical properties of MOS capacitors

Table 2-3 Summary of the samples used in this research.

Section	Substrate	Passivation	Dielectric Oxide	Thickness (nm)	Metal Gate	PDA	*PMA
3.1	n-Si	no	$LaZrO_x$	22	Al	no	no
3.2	n-Si	no	$LaZrO_x$	22	Al	no	no
3.3	n-Si	no	ZrO_2	20	Al	no	no
	n-Si	no	ZrO_2	20	Al	no	FG
	n-Si	no	ZrO_2	20	Al	no	N_2
	n-Si	no	HfO_2	19	Al	no	no
	n-Si	no	HfO_2	19	Al	no	FG
	n-Si	no	HfO_2	19	Al	no	N_2
4.1	p-Ge	0.3 nm Al_2O_3	$Ti_xHf_{1-x}O_2$ (x=1, 0.9, 0.25, 0)	5	Al	no	no
	p-Ge	0.3 nm Al_2O_3	$Ti_xHf_{1-x}O_2$ (x=1, 0.9, 0.25, 0)	10	Al	no	no
	p-Ge	0.3 nm Al_2O_3	$Ti_xHf_{1-x}O_2$ (x=1, 0.9, 0.25, 0)	15	Al	no	no
4.2	n-Ge	$(NH_4)_2S$	$Ti_{0.1}Hf_{0.9}O_2$	13.5	Al	no	no
	n-Ge	$(NH_4)_2S$	$Ti_{0.1}Hf_{0.9}O_2$	13.5	Al	450 ℃ in N_2	no
	n-Ge	$(NH_4)_2S$	$Ti_{0.1}Hf_{0.9}O_2$	13.5	Al	550 ℃ in N_2	no
5.1	n-Ge	no	HfO_2	20	Al	no	no
	n-Ge	$(NH_4)_2S$	HfO_2	20	Al	no	no
	n-Ge	PT	HfO_2	20	Al	no	no
	n-Ge	OT	HfO_2	20	Al	no	no
	n-Ge	no	HfO_2	20	Al	no	FG
	n-Ge	$(NH_4)_2S$	HfO_2	20	Al	no	FG
	n-Ge	PT	HfO_2	20	Al	no	FG
	n-Ge	OT	HfO_2	20	Al	no	FG
5.2	n-Ge	$(NH_4)_2S$	HfO_2	12.9	Al	no	no
	n-Ge	$(NH_4)_2S$	HfO_2	12.9	Al	no	no

* For post-metal annealing (PMA), FG and N_2 represent annealing in FG and N_2 environments, respectively, for 30 minutes at 350 ℃

2.2 Physical Characterization

The physical properties of high-*k* thin films were studied using X-ray Photoelectron Spectroscopy (XPS), X-ray diffraction (XRD), and atomic force microscopy (AFM).

The atomic composition and chemical structure of the samples were investigated by XPS. XPS measurements were carried out in an Ultra-High Vacuum (UHV) system consisting of an Al *K*α X-ray (1486.6 eV) source and a PSP vacuum systems 5-channel HSA electron energy analyzer. Due to the carbon impurity in the samples, the C 1*s* peak in the spectra at 284.6 eV was used to calibrate any charging effects during measurements [5]. The experimental XPS spectra were fitted using a Gaussian-Lorentzian line shape doublet to account for the spin-orbit splitting, using the CASAXPS fitting package.

XRD was used to study the crystallization state of the high-*k* thin films using a Bruker diffractometer (Bruker, Karlsruhe, Germany) with a Cu Kα radiation source was also used to carry out the XRD.

An atomic force microscope (AFM, Bruker, Karlsruhe, Germany) was used to examine the surface roughness of the samples. The surface roughness of the samples is quantitatively determined by the root-mean-squared roughness (R_{rms}), defined as:

$$R_{rms} = \sqrt{\frac{\sum_{n=1}^{N}(z_n - \bar{z})^2}{N}}, \tag{2.1}$$

where z_n is the measured height, $\bar{z}$ is the average height of the sample and N is the number of measurements.

2.3 Electrical Characterization

Electrical properties of the samples were characterized using the conventional CV method, pulse CV technique, and IV measurement. All of the measurements were carried out based on the MOS structure. A detailed discussion of the MOS structure has been presented in Section 1.1. The conventional CV method was carried out using an Agilent 4284A LCR Meter (Agilent, Santa Clara, CA, USA) controlled by computer via a GPIB module and a probe station. The MOS capacitors were probed on the probe station's platform and the CV characteristics were measured by the Agilent 4284A LCR Meter as shown Figure 2.2.

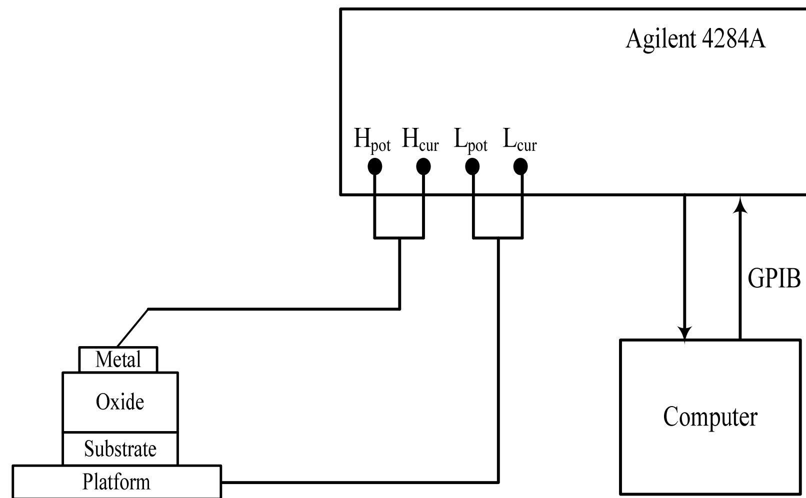

Figure 2.2 Conventional CV measurement system of MOS capacitors using Agilent 4284A LCR Meter.

As shown in Figure 2.2, the MOS capacitor consists of a metal contact, an oxide dielectric layer, and a semiconductor substrate. When the capacitance of the device is measured by conventional method, a small AC voltage with a variation rate of dv_{ac}/dt is applied and the corresponding current (i_{ac}) flowing through the MOS capacitor is

measured. The differential capacitance (C) of the MOS capacitor is determined by

$$C = \frac{i_{\mathrm{ac}}}{\mathrm{d}v_{\mathrm{ac}}/\mathrm{d}t} \tag{2.2}$$

For an Agilent 4284A precision LCR meter, two measurement models can be selected, parallel model and series model. The corresponding schematic representations for the two models are shown in Figure 2.3. For the MOS capacitors measured in this work, the resistance (R) is high (>1 MΩ) and so the parallel mode is selected.

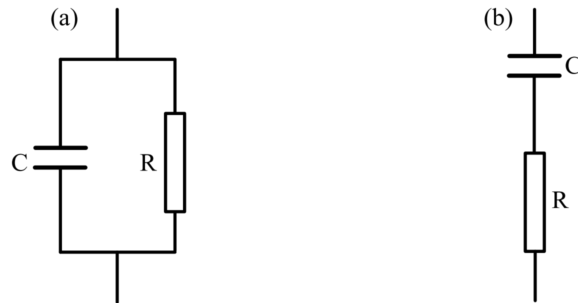

Figure 2.3 Schematic representation for (a) parallel and (b) series model.

The pulse CV technique developed in this research uses a function generator (RIGOL DG3061A), a current amplifier (Keithley 428) and an oscilloscope (RIGOL DC1302CA). The system structure chart is shown in Figure 2.4 [6]. Compared with other pulse CV systems, the current probe is replaced by an oscilloscope and a current amplifier [6, 7]. Pulse signals with higher speed can be used, only limited by the bandwidth of the oscilloscope. Also, the system is cost-effective and can be updated easily. In the measurement of the CV traces, the function generator is used to apply a pulse voltage (v_{g}) to the device under test (DUT) and is monitored on channel 1 (v_{CH1}) of the oscilloscope. The induced current through the device (i_{total}) is fed into the current amplifier and amplified by the amplification factor A. Selection of the amplification

factor is dependent on the capacitance, induced current and the oscilloscope used. Channel 2 (v_{CH2}) of the oscilloscope is used to monitor the output voltage of the amplifier. Usually, the resistance of a MOS capacitor with high-*k* thin film is larger than 1 MΩ, therefore, the MOS capacitor is modelled as a capacitor (*C*) connected with a resistor (*R*) in parallel. The current through the capacitor and resistor are denoted i_C and i_R, respectively. The capacitance of the MOS capacitor can then be determined by [4]:

$$i_{\mathrm{total}}(t) = \frac{v_{\mathrm{CH2}}(\mathrm{t})}{\mathrm{A}} = i_{\mathrm{C}}(\mathrm{t}) + i_{\mathrm{R}}(\mathrm{t}) = C \cdot \frac{\mathrm{d}v_{\mathrm{g}}(\mathrm{t})}{\mathrm{d}t} + \frac{v_{\mathrm{g}}(t)}{R} \quad (2.3)$$

$$v_{\mathrm{CH2}} = \mathrm{A} \cdot \mathrm{C} \cdot \frac{\mathrm{d}v_{\mathrm{g}}}{\mathrm{d}t} + \mathrm{A} \cdot \frac{v_{\mathrm{g}}}{R} \quad (2.4)$$

If the resistance, *R*, is large enough (>1 MΩ), Formula (2.4) can be simplified to,

$$v_{\mathrm{CH2}} = \mathrm{A} \cdot C \cdot \frac{\mathrm{d}v_{\mathrm{g}}}{\mathrm{d}t} \quad (2.5)$$

Thus, the capacitance, *C*, can be evaluated from Formula (2.5).

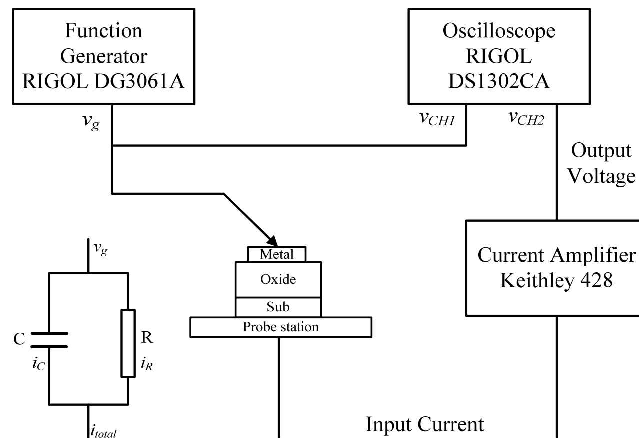

Figure 2.4 The pulse CV measurement system structure chart [4].

IV measurements were carried out using a Keithley 487 pico-ampere meter or an Agilent B1500A semiconductor device analyzer. From the IV characteristics, the gate leakage current is obtained.

2.4 Basic Terms and Definitions

Tunneling

The scaling down of the MOS device requires a decrease in gate oxide thickness, however the gate leakage current is dominated by the tunneling current if conventional SiO_2 gate dielectrics are used. The direct tunneling and Fowler-Nordheim tunneling shown in Figure 2.5 are the main tunneling mechanisms in MOS devices. The difference between the two mechanisms is the dielectric thickness (*T*). When the oxide thickness is smaller than 3 nm, direct tunneling is the dominant conduction mechanism, which leads to a large gate leakage current.

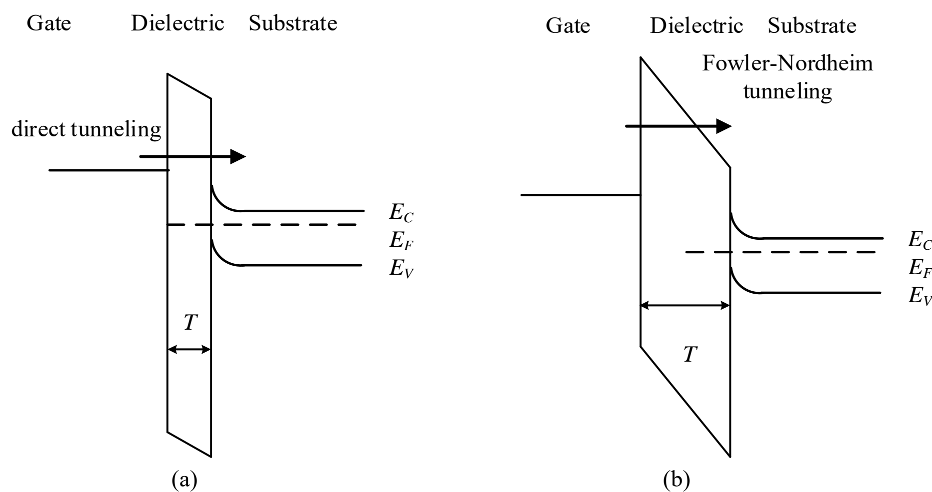

Figure 2.5 Energy band diagrams of direction tunneling and Fowler-Nordheim tunneling.

Gate Leakage Current

The gate leakage current is measured by IV sweep using a pico-ampere meter with an internal voltage source. The increase in leakage current leads to more power consumption and heat generation. Therefore, a small leakage current density is desired. The maximum tolerable gate leakage density is 1 A/cm^2 at a supply voltage of 1 V

[8] .When SiO_2 is replaced by high-*k* material, the tunneling current is not the main cause for the gate leakage current, because the smaller EOT (defined in Formula (1.1)) can be obtained with a larger physical thickness using high-*k* materials. Trap-assisted leakage current becomes the dominant contributor to the gate leakage current, due to the large number of traps ($>10^{12}$ /cm^2) in high-*k* dielectrics.

CV Characteristics

A typical high-frequency CV characteristic for a PMOS capacitor (n-type substrate) is shown in Figure 2.6. CV traces for two different frequencies (f1<<f2) are included. The inversion region, depletion region and accumulation region are denoted in Figure 2.6. A number of characteristics can be extracted from the CV traces, such as interface state and trap density. This study focuses on hysteresis and frequency dispersion. The CV curves were measured using an Agilent 4284 LCR Meter and a developed pulse CV system.

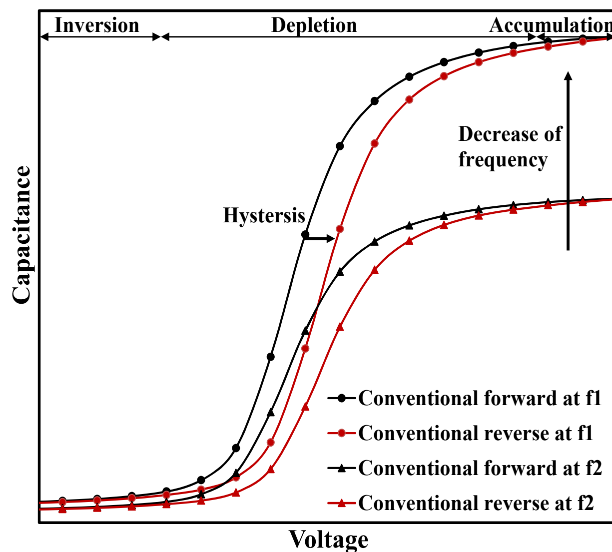

Figure 2.6 Typical CV characteristics of a MOS capacitor.

Hysteresis

Hysteresis, also termed loop width, is the voltage shift between the reverse CV trace and the forward one indicated by a black arrow in Figure 2.6. The hysteresis of the CV curves is attributed to the trapping and de-trapping of charges. When the positive charges are trapped in the oxides during the CV sweep, a negative shift is obtained. Similarly, when electrons are trapped, a positive shift of the CV curve is obtained. In addition, interface dipoles also have an effect on hysteresis, which will be discussed in detail in Section 3.3. Quantitatively, the voltage shift (ΔV_{g}) can be express as:

$$\Delta V_{\mathrm{g}} = -\frac{\Delta N_{ot}}{\mathrm{q} \cdot \mathrm{C_{ox}}}, \tag{2.6}$$

where ΔN_{ot} is the change of oxide traps per unit area, q is the elemental charge and C_{ox} is the oxide capacitance per unit area.

Therefore, for a perfect dielectric material, such as SiO_2 on silicon, there are almost no traps in the oxide and so no hysteresis will be observed during the CV sweep.

Frequency Dispersion

Frequency dispersion is represented by the dielectric relaxation of the dielectric material. The capacitance of the MOS device decreases with an increase in measurement frequency as shown in Figure 2.6. This phenomenon can be caused by both intrinsic and extrinsic factors. Intrinsic factors are causes related with micro structures within the material, such as ion movement in the metal-oxide lattice, generation of dipole momentum due to unbound metal ions with electron traps, or increased stresses due to a decrease in crystal grain size. Extrinsic factors include series

resistance, parasitic effect, lossy interfacial layer, leakage current and surface roughness.

2.5 Summary

In conclusion, a technique for high-*k* thin film deposition, ALD, and a PVD system used for the deposition of metal contacts, E-beam evaporator, were introduced. ALD can control the thickness of thin films theoretically at the monolayer level. The procedures for the fabrication of the samples were described in detail. In addition, the physical and electrical characterization systems used in this research were presented in Sections 2.2 and 2.3 and the discussion was focused on the pulse CV system. Finally, the descriptions on basic terms and definitions were provided in Section 2.4.

2.6 Reference

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Chapter 3: Characterization of High-*k* Oxides on Silicon Substrates

With the scaling down of the physical size of the MOSFET, the thickness of the SiO_2 dielectric layer needed is on the order of the nanometer. A major challenge associated with this is gate leakage current which becomes unacceptably large [1]. In order to overcome this problem, high-*k* dielectrics have been employed to replace SiO_2 gate dielectrics. However, it has been reported there are significantly more charge traps in high-*k* material than in SiO_2 [2]. To characterize the number of traps accurately and to comprehensively investigate the trapping/de-trapping behavior, a pulse CV system has been developed to explore the CV behavior of $LaZrO_x$ thin films deposited on Si in this research. The application of the pulse CV technique and characterization of the traps are presented in Section 3.1 and 3.2 respectively. In addition, the pulse CV measurements were performed on MOS capacitors with non-stoichiometric oxides native to the substrate. Either ZrO_2 or HfO_2 deposited on an n-type silicon substrate was used as the gate oxide. During the measurements, pulse voltages with different edge times, pulse widths and V_{PP}'s were applied to the gate terminal to investigate their effects on the pulse CV measurement behavior. Also, the samples were annealed in a nitrogen and FG environment to explore the effect of PMA on device performance. The results and discussions are covered in Section 3.3.

3.1 Application of Pulse CV Technique

Before employing the pulse CV system to characterize the MOS capacitors with high-*k* dielectrics, the measurement system was evaluated using SiO_2 based standard MOS capacitors. Figure 3.1 (a) shows the voltage-time (VT) data from both channel 1 and channel 2 of the oscilloscope [1]. Using Formula (2.5), the relationship between capacitance and applied voltage can be determined; the result of this is illustrated in Figure 3.1 (b). In addition, a conventional CV measurement using the Agilent 4284A is also shown for comparison with that from the pulse CV technique. From observation of the CV curves in Figure 3.1 (b), the pulse CV and conventional CV techniques show the same trends and there is no clear shift between forward and reverse characteristics in either the pulse CV or conventional CV tests. This result is consistent with the fact that there are not a significant number of traps located in the oxide layer of the thermal SiO_2 MOS capacitor. Therefore, it can be concluded that the pulse CV system developed here is suitable for the CV characterization of MOS capacitors with high-*k* dielectrics.

3.2 Characterization of MOS Capacitors with $LaZrO_x$ dielectrics

For a MOS capacitor with $LaZrO_x$ dielectric, Figure 3.2 (a) shows the input voltage to the device and the output signal of the current amplifier using the pulse CV technique. The pulse CV characteristics shown in Figure 3.2 (b) are extracted from the results in Figure 3.2 (a) using Formula (2.5). The hysteresis, ΔV_g, is denoted in Figure 3.2 (b). In regards to the hump in the forward CV trace, it will be fully discussed in Section 3.3.

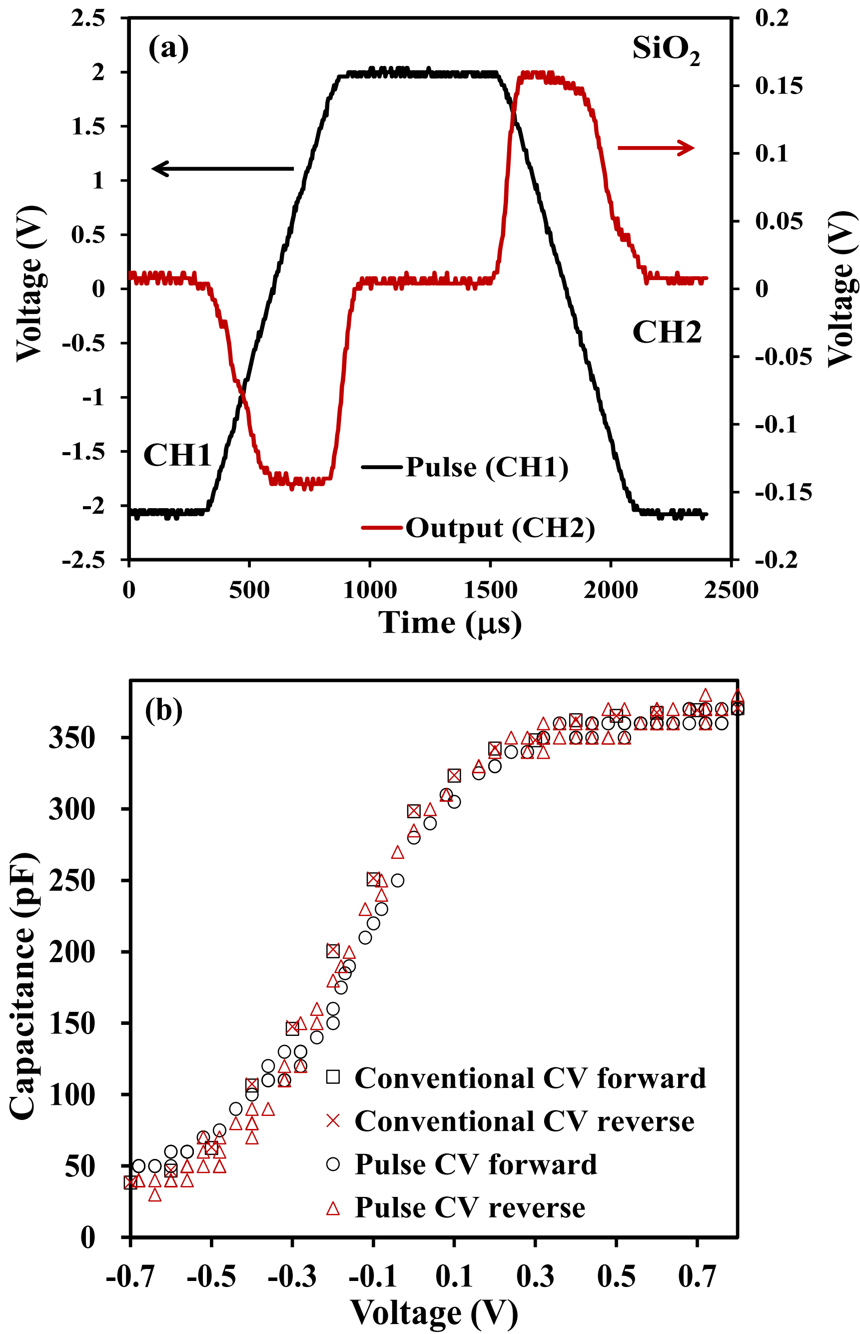


Figure 3.1 (a) Relationship between applied voltage and time for the voltage signal applied to the MOS capacitor and output voltage of the amplifier; (b) Relationship between capacitance and voltage calculated using Formula (2.5) for the SiO_2 MOS sample.

Figure 3.3 illustrates measurements obtained from conventional CV tests for the $LaZrO_x$ dielectric MOS capacitor. Comparing Figure 3.2 (b) and Figure 3.3, a clear hysteresis can be seen between the pulse CV curves (forward and reverse traces), while there is almost no hysteresis in the conventional CV test.

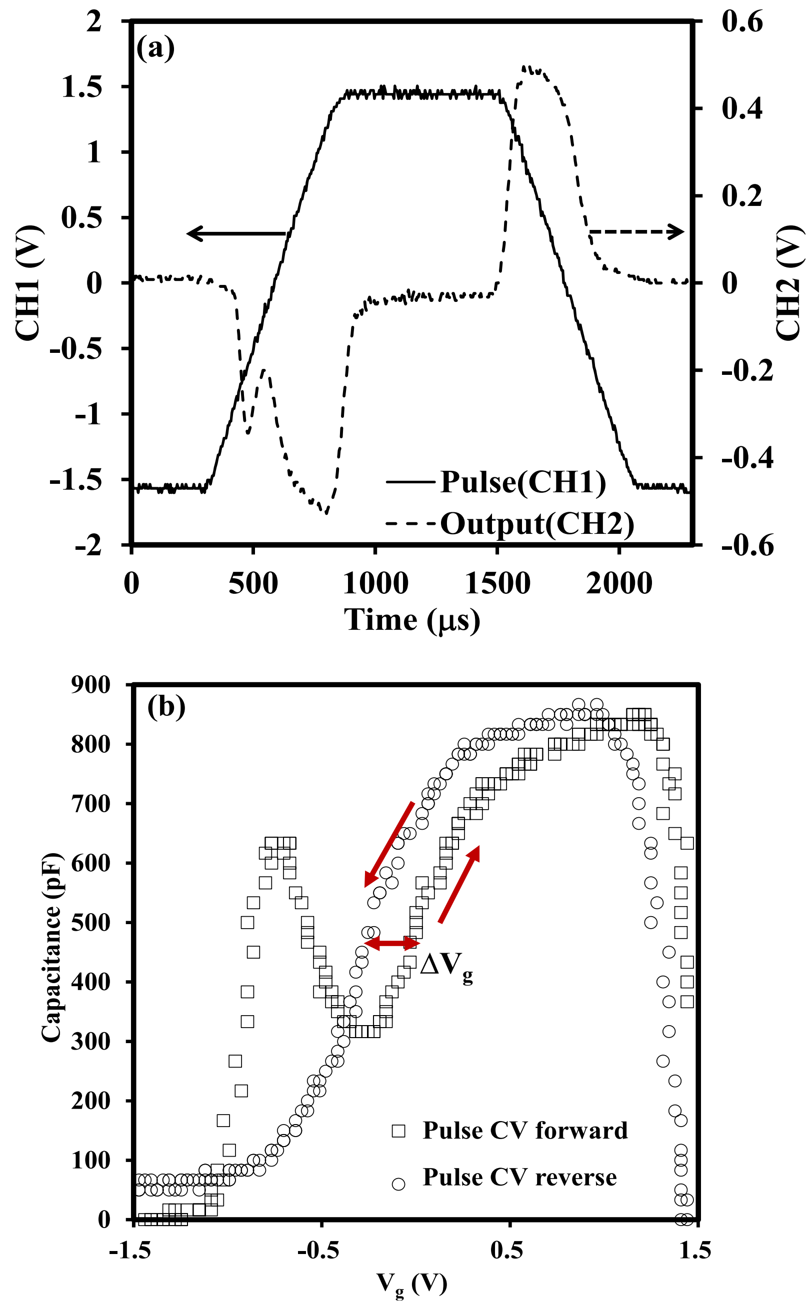


Figure 3.2 (a) Relationship between applied voltage and time for the voltage signal applied to the MOS capacitor (CH1) and output voltage of the amplifier (CH2); (b) Relationship between capacitance and voltage calculated using Formula (2.5) for the MOS capacitor with $LaZrO_x$ dielectric.

This behavior indicates that all of the trapped charges in the oxide are de-trapped or recovered and so no charge is detected in the conventional CV measurement. The de-trapping time is usually on the order of microseconds, while it takes several seconds

for the conventional CV measurement process [3]. Therefore, from Formula (2.6), no hysteresis will be observed since no trapped charges remain for the duration of the test. The hysteresis is revealed by the rapid characterization used by the pulse CV technique, on the order of several hundreds of micro seconds. It is clear that the traps have not recovered completely before the end of the measurement. Therefore, the pulse CV technique can reveal the trap density in the oxide layer more accurately. In other words, the conventional method underestimates the trap density in the oxide. The influence of test time on changes of ΔV_g (shown in Figure 3.2 (b)) will be fully discussed later.

The shift of the CV curves in Figure 3.2 (b) is attributed to charge trapping/de-trapping in the oxide [4, 5]. In this case, the charges existing in the oxide probably belonged to as-grown fixed positive charges (oxygen vacancies) with high energy levels or probably were trapped-in as-grown electron traps in the high-*k* oxide. When the gate was applied with a positive bias voltage ($V_g>0$), electrons were de-trapped from the as-grown electron traps to the metal gate through tunneling and the net positive charges in the oxide led to the CV curves shifting negatively. Similarly, if a negative voltage ($V_g<0$) was applied on the metal side, the as-grown positive charges would be compensated by electrons from the metal gate and trapped in the as-grown electron traps. Thus, a positive shift of the CV curves was observed due to the electrons trapped in the oxides [6-9].

Indicated in the inset of Figure 3.4 (a), edge time, is a critical parameter for the characterization of traps in the oxide and detailed discussions are now presented. During the measurement, the rising edge applied to the gate provides a measurement

before any stress is applied, then, the falling edge of the pulse provides the other measurement after stress.

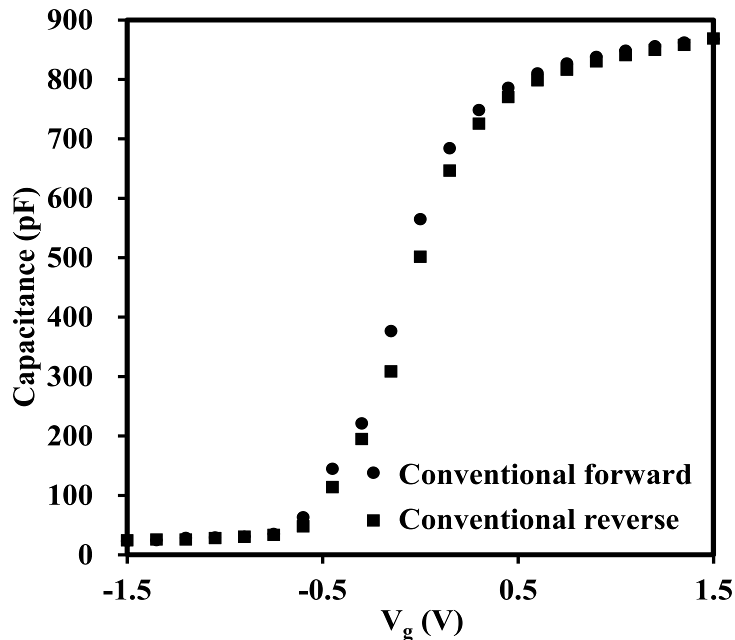


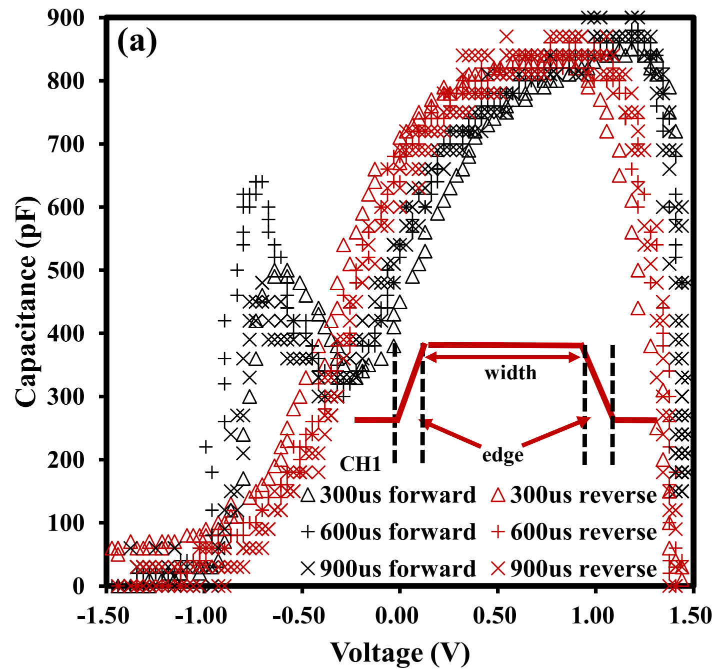
Figure 3.3 Conventional CV characteristics measured by Agilent 4284A for the sample with the thickness of about 22 nm.

The applied stress time is determined by the width of the pulse. If the stress of a pulse induces charge trapping in oxides, there will be a hysteresis between the forward and reverse CV curves as shown in Figure 3.2 (a). In addition, the change in the edge time leads to a change in total test time. If a longer test time is used by increasing the edge time, more trapped charges will be recovered and a lower trap density detected, as shown in Figure 3.4. Pulse CV traces shown in Figure 3.4 (a) were measured for edge times of 300 μs, 600 μs and 900 μs for a fixed pulse width of 800 μs. As the edge time is increased to a relatively large value, or relatively long test time (several seconds), the pulse CV technique is considered to be the same as the conventional CV test carried out using an LCR meter. This hypothesis is consistent with the results shown in

Figure 3.4 (a) and (b). Figure 3.4 (b) shows that the detected trap density, N_{ot}, reduces from 2.48×10^{12} cm^{-2} for an edge time of 300 μs to 0.7×10^{12} cm^{-2} for an edge time of 900 μs. The N_{ot} is calculated by Formula (3.1), assuming these traps are located at the silicon substrate and dielectric oxide interface:

$$N_{ot}=\Delta V_g\times C_{ox}/q, \qquad (3.1)$$

The above analysis implies that the trapped electrons/holes are recovered with an increase of the measurement time, in turn, leading to the partial reduction of trapped charges. Figure 3.4 (b) graphically summarizes the relationship between trap density and pulse edge time for a high-*k* material ($LaZrO_x$) and a SiO_2 dielectric MOS capacitor measured by pulse technique. For the SiO_2 gate dielectric, it is known that there are no as-grown electron traps in the oxide and no hysteresis is observed whatever the edge time is [1]. Thus, the SiO_2 sample was used as a reference in this experiment. By adjusting the edge time, the time-dependent trapping/de-trapping characteristic was detected correspondingly. For the high-*k* material in this research, detected N_{ot} reduces with an increase in edge time as shown in Figure 3.4 (b). Due to the limitations of the function generator (RIGOL DG3061A), the longest edge time is 900 micro seconds. However, from the trend of N_{ot}, it can be estimated that if the edge time is long enough, say, one second, the trap density measured by pulse CV technique will be equal to that of the conventional CV test as shown in Figure 3.3. The dashed line in Figure 3.4 (b) indicates the estimated behavior of N_{ot} with increasing edge time.



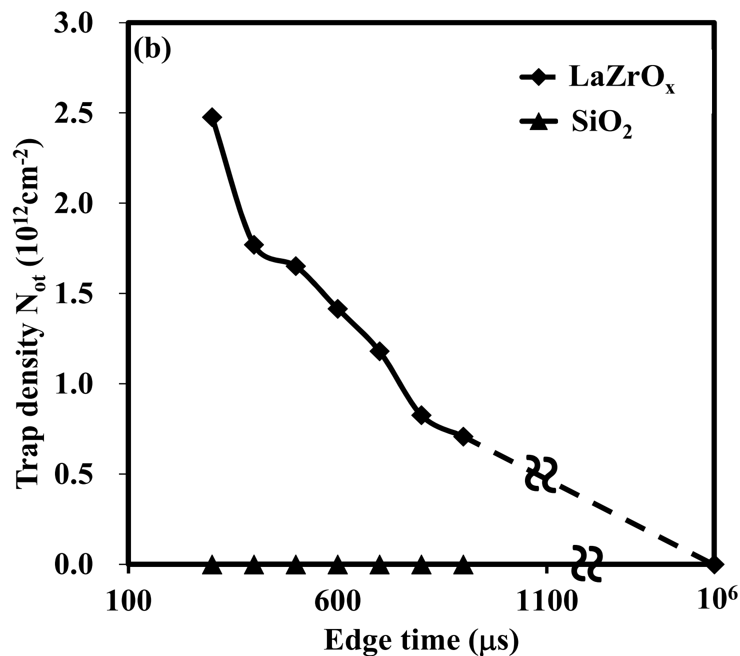


Figure 3.4 (a) Capacitance versus gate voltage with various edge time for $LaZrO_x$; (b) Variation of N_{ot} versus edge time for $LaZrO_x$ and SiO_2.

It can also be concluded that the recovery of trapped electrons/holes is sensitive to the measurement time from the change of N_{ot} with the variation in total test time. To be precise, a shorter test time gives a larger N_{ot}. Therefore, time-dependent trapping/de-trapping should be probed using a short edge time for pulse CV

measurements, which is able to access shallower traps (traps at a high energy levels within the oxide), at least for the timescale considered here. While for the longer edge times, the transient shift of the N_{ot} is attributed to slow electron trapping/de-trapping.

Following the examination of edge time, the focus now moves to look at the influence of the stress time on the detected trap density. The stress time (pulse width) is indicated in the inset of Figure 3.5. The pulse width is defined as the interval between the 90% points of the peak voltage. Figure 3.5 shows that charges trapped in the oxide are highly dependent on the stress time with N_{ot}'s of 4.14×10^{12} cm^{-2}, 3.17×10^{12} cm^{-2}, 2.48×10^{12} cm^{-2} for stress times of 4500 μs, 2500 μs and 800 μs, respectively, with the edge time set at 300 μs. The longer the pulse width, or stress time, the larger the electron fluency supplying the charge into traps in the oxide, this in turn, leads to more trapped charges. Also, the figure shows that the recovery of N_{ot} with edge time for the three curves share similar trends regardless of the initial charges trapped in the oxide. This result also implies that the de-trapping process is highly dependent on the test time.

Finally, pulses of various V_{PP} were applied to the gate of the MOS capacitors to investigate the effect of V_{PP} on charge trapping. Figure 3.6 shows the relationship between the detected trap density and edge time under different V_{PP} conditions. It shows that for larger V_{PP} (4 V), larger N_{ot} (3.58×10^{12} cm^{-2}) is observed for a given pulse edge time because the traps in deeper energy levels in the oxide are also detected due to the higher voltage. Interestingly, when V_{PP}=4 V, the detected trap density is saturated for a small pulse edge time, 400 μs in this case, which means that all of the traps at the corresponding energy level are fully probed provided that the pulse edge time is below

400 μs at this voltage level. From this behavior, it can also be inferred that an equilibrium between trapping and de-trapping is achieved for a short pulse edge time of less than 400 μs.

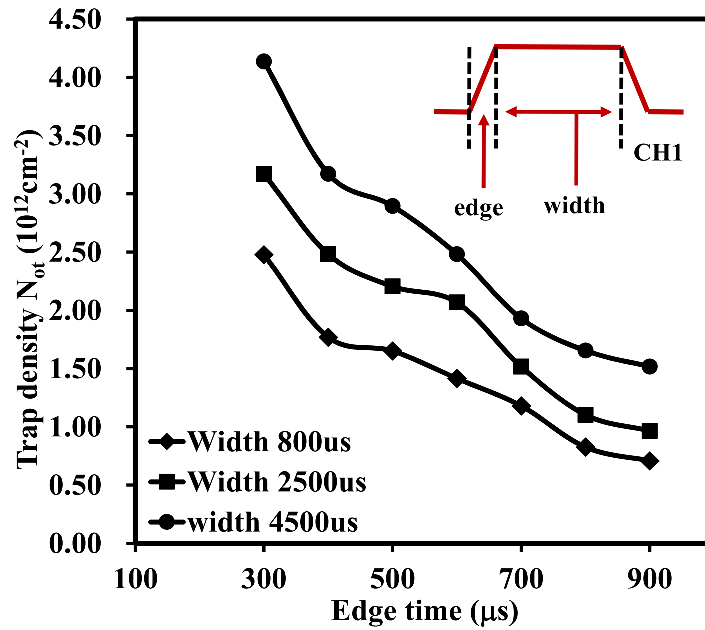


Figure 3.5 Variation of N_{ot} versus edge time with different stress time for $LaZrO_x$.

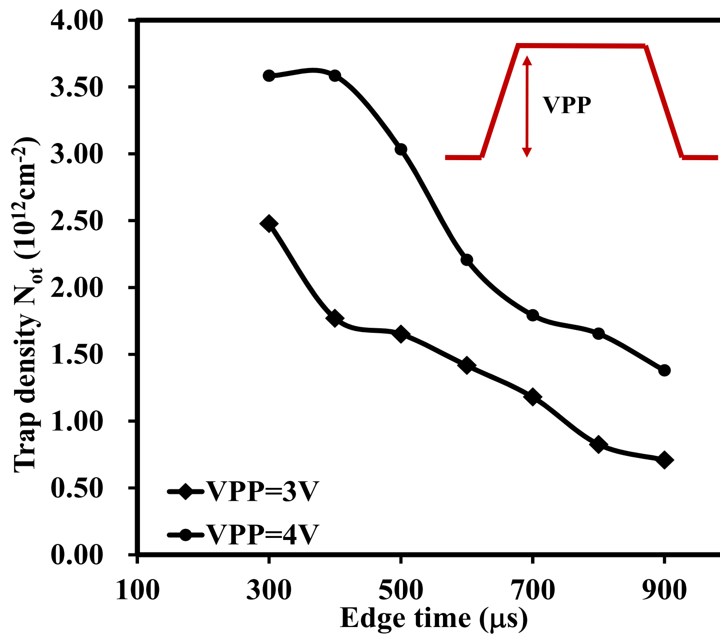


Figure 3.6 Relationship between N_{ot} and edge time with various V_{PP} for $LaZrO_x$ dielectric MOS capacitors.

3.3 Anomalous Hysteresis in Capacitance-Voltage Traces

It has been shown that the pulse CV technique enables the completion of electrical characterization, and is therefore a powerful tool for use in the accurate characterization of traps. However, abnormal CV behavior is observed when the pulse CV technique is applied to some MOS capacitors with high-*k* dielectrics, especially for a device with a relatively thick non-stoichiometric native oxide [10, 11]. Opposite relative positions of the forward and reverse traces are observed for the pulse CV curves compared with those from the LCR meter. The CV traces of the MOS capacitors with ZrO_2 and HfO_2 dielectrics are presented in Figure 3.7 (a) and (b), respectively. The Agilent 4284A (labeled conventional CV) and the developed pulse CV system (labeled pulse CV) were used to extract the CV characteristics. The detailed working principle of the test systems have already been discussed in Sections 2.3 and 3.1. In this experiment, a small pulse width of 800 μs (determined by the pulse generator) was chosen to minimize charge trapping due to an applied pulse voltage stress [12, 13]. The extraction of the CV characteristics is achieved through application of Formula (2.5) with an edge time of 400 μs and a pulse width of 800 μs for the pulse CV technique. The thicknesses of the dielectrics are 20 nm and 19 nm for ZrO_2 and HfO_2, respectively, with each a corresponding equivalent oxide thickness (EOT) of about 5.3 and 9.3 nm. The V_{PP} for the ZrO_2 dielectric sample is 3 V, while it is 4 V for the HfO_2 sample. For both samples, positive shifts in the reverse traces of conventional CV were observed with respect to the forward one, while the shift became negative in the results extracted from the pulse technique. The shift directions are indicated by the arrows in both figures. In the

following discussions, the positive (or negative) shift of the reverse trace with respect to the forward one is referred to as the positive (or negative) loop width for convenience. In regards to the positive loop width observed in the conventional CV traces for both samples, this is attributed to the trapping and de-trapping of charges [14]. When the MOS capacitor is biased in its inversion region (negative voltage for PMOS in this research), holes are captured by the traps in the oxides, which leads to a negative shift during the forward sweep. Similarly, when the device is biased in its accumulation region (positive voltage for PMOS in this research), electrons are trapped and a positive shift of the CV curve is obtained [15], [16].

However, this mechanism cannot consistently explain the shift in conventional CV and pulse CV, since an opposite shift direction was observed. To explain this phenomenon, a model relating to the response of interface dipoles has been proposed, as shown in Figure 3.8 [15]. The orientations of the dipoles should be randomly directed in reality, however, they are assumed to be perpendicular to the high-*k*/SiO_x interface (ZrO_2/SiO_x interface in Figure 3.8 as an example) for simplicity in this discussion since only a qualitative result is presented [15]. Figure 3.8 shows the separation of the dipoles during the pulse CV ((b) and (c)) and conventional CV (a) measurements. In the following discussions, dipole separations in conventional CV measurement, pulse CV measurements of rising and falling edge are by d_1, d_2 and d_3, respectively. The relaxation time for orientation polarization is usually on a time scale of microseconds depending on the materials [17]. Therefore, in the conventional measurement, due to the low sweeping speed (more than 30 microseconds per step), the dipoles have enough

relaxation time and exactly follow the change of the oxide field induced by the DC bias.

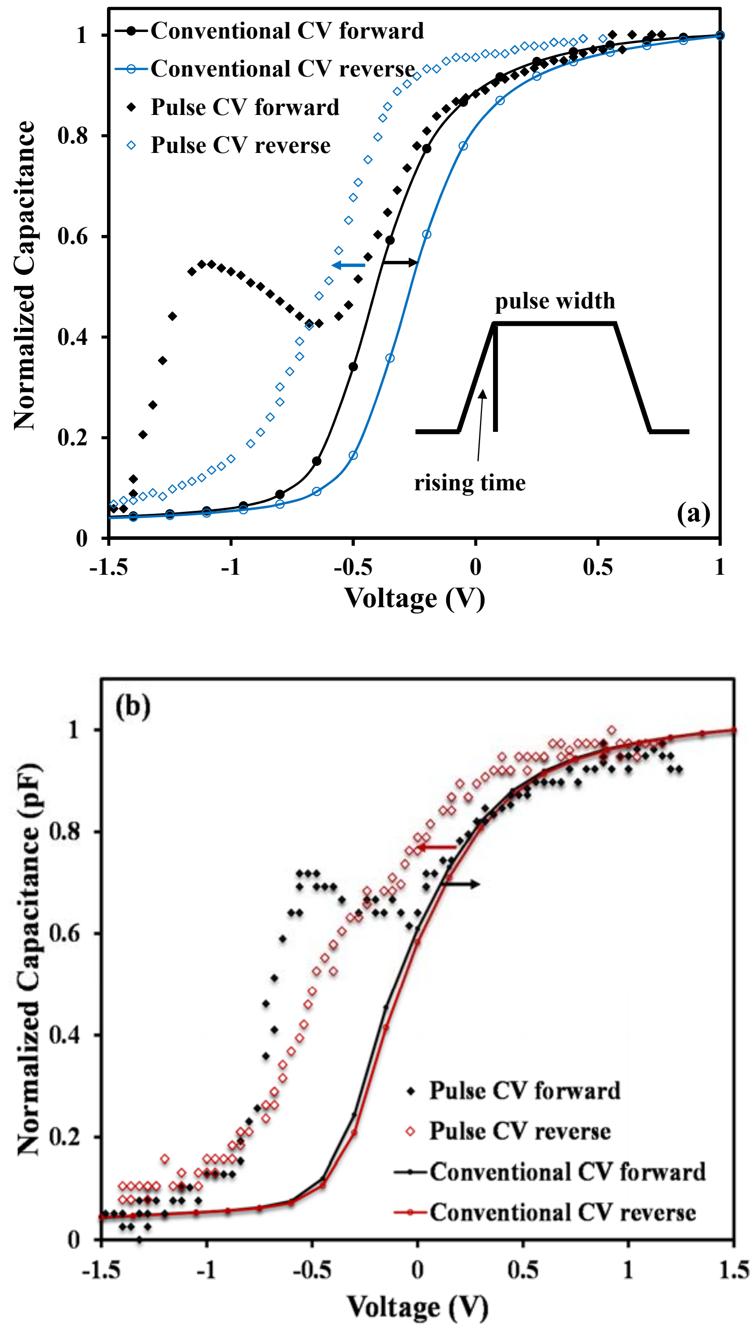


Figure 3.7 CV characteristics measured by an Agilent 4284A LCR meter and a pulse CV system for (a) ZrO_2 and (b) HfO_2 dielectric MOS capacitors.

Therefore, there is no change of dipole separation in forward and reverse sweep during the measurement (Figure 3.8 (a)). However, in the pulse CV measurement (sweeping from negative to positive), the electric field across the capacitor stretches the dipoles,

$d_2>d_1$, (Figure 3.8 (b)) at the negative bias. Then, when a fast voltage pulse sweeps from negative to positive, the dipole separation remains unchanged due to the lag in dipole response. Consequently, a positive shift of the forward trace is observed because the negative ends of the dipoles are closer to, and the positive ends are further from, the Si/SiO_x interface compared with the case in the conventional measurement. A similar mechanism is operative (Figure 3.8 (c)) when a pulse voltage sweeps from positive to negative, $d_3<d_1$, and a negative shift of the reverse trace is observed consequently. In fact, it should be noted that a lag in interface dipole response also exists in the conventional CV measurement because of the high frequency (1 MHz) AC signal. However, the hysteresis in the conventional CV curves is mainly attributed to charge trapping in oxides due to the DC bias rather than the interface dipole effect because the amplitude of the AC signal (~50 mV) is very small compared with a significant variation in gate pulse voltage (2500 mV for ZrO_2 and 3000 mV for HfO_2) within a short time interval (~ several hundred μs) [15]. Thus, the effect of the interface dipoles can be ignored in the analysis of conventional CV measurements.

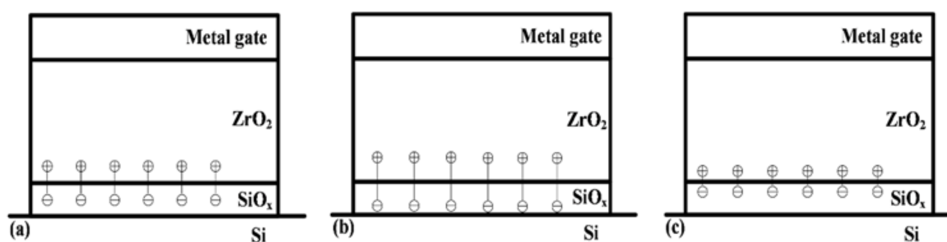


Figure 3.8 The separation of interface dipoles for the as-deposited sample (a) during conventional measurement, under pulse voltage sweep (b) from negative to positive and (c) from positive to negative [15].

If the change of dipole separation in conventional CV measurements is ignored, the loop width registered by forward pulse CV curve (W_f) and the loop width obtained by

reverse pulse CV curve (W_r) relative to those in the quasi-static case can be expressed as:

$$W_f = \frac{\frac{(d_2 - d_1)}{2} * Q}{\varepsilon_{ox}}, \tag{3.2}$$

$$W_r = \frac{-(d_1 - d_3)/2 * Q}{\varepsilon_{ox}}, \tag{3.3}$$

where d_1 is the dipole separation in the conventional measurement and, d_2 and d_3 ($d_2>d_1>d_3$) are the dipole separations under pulse measurements as indicated in Figure 3.8, Q is dipole charge per unit area, ε_{ox} is the permittivity of the oxide. Therefore, the loop width attributed to the interface dipoles in pulse CV curves is,

$$\text{Loop Width} = W_f - W_r = \frac{-(d_2 - d_3)/2 * Q}{\varepsilon_{ox}}, \tag{3.4}$$

If the directions of interface dipoles are not perpendicular to the interface, Formula (3.4) will be written as:

$$\text{Loop Width} = W_f - W_r = \frac{-\frac{(d_2 - d_3)}{2} * Q * \sin\theta}{\varepsilon_{ox}}, \tag{3.5}$$

where θ is the angle between the dipole and the interface as shown in Figure 3.9.

In regards to the formation of the interface dipoles, a model related to the oxygen atom density difference has been proposed by Kita [15] and is shown in Figure 3.10. When the interface between the high-*k* and SiO_x is formed, the positions of oxygen atoms are moved to relax the structure due to the oxygen density difference in the high-*k* materials and native oxides.

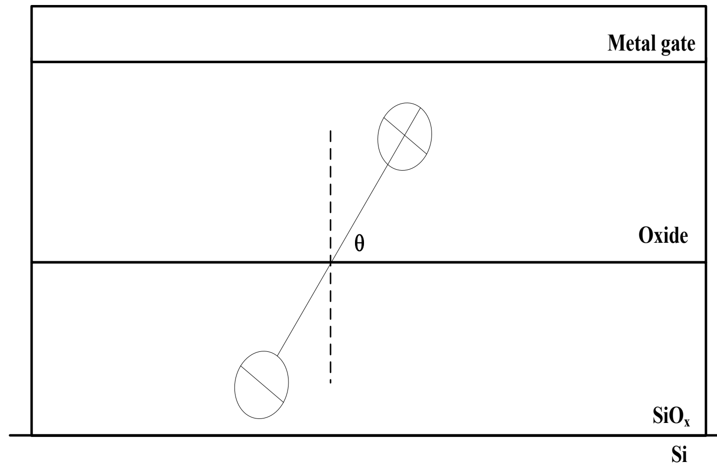


Figure 3.9 The separation of interface dipoles with an angle between the dipole and interface.

The higher density of oxygen atoms in the high-*k* oxides diffuse into the SiO_x area which has a lower oxygen atom density. In other words, the negatively charged oxygen ions move to the smaller oxygen density layer and a positively-charged oxygen vacancy is left in the oxygen rich layer. Therefore, interface dipoles are formed.

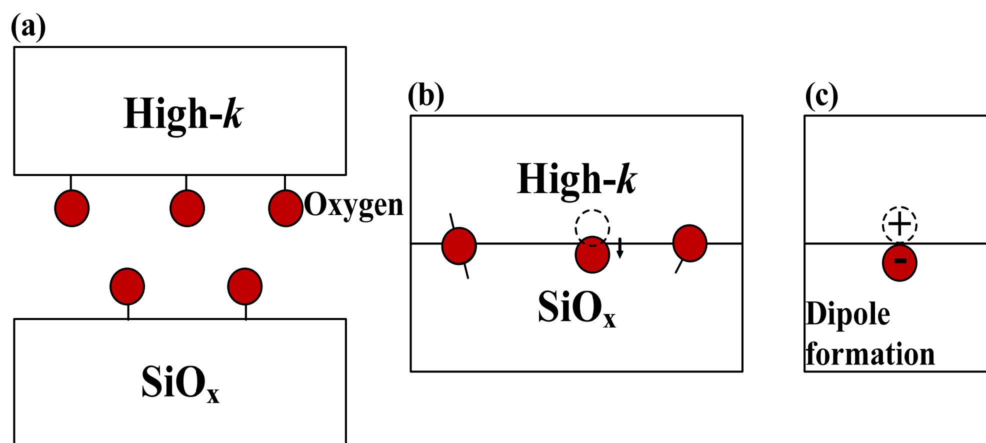


Figure 3.10 The formation process of interface dipoles [15].

Apart from the interface dipoles, traps in oxides also lead to shifts in the CV traces, or a change of loop width as defined above. From previous research, it is known that the number of trapped charges are dependent on the stress time (pulse width), applied voltage, etc. [1, 18]. Two selected CV characteristics extracted from the samples with

ZrO_2 dielectrics are representatively shown in Figure 3.11 (a) with pulse widths of 800 μs and 50000 μs. The stress time, defined as the interval between the 90% points of the peak voltage, is indicated in the inset of Figure 3.11 (a). The relationship between loop width and pulse widths of 800 μs to 50000 μs with V_{PP}'s of 3 V and 4 V are concluded in Figure 3.11 (b). The loop width is measured at the point at which the capacitance becomes 50% of its maximum value. All of the pulse CV measurements were performed for a rising edge time of 400 μs. The applied pulse voltage (a positive stress on the gate electrode) leads to a positive shift of the reverse trace due to the response of the electrons trapped in the oxide. The longer the pulse width, the more charges are supplied into the traps from the substrate. This in turn leads to more trapped charges and an even greater positive shift of the reverse CV trace [19]. Thus, loop width increases with the stress time as illustrated in Figure 3.11 (b). In regards to the applied voltage, more traps in the deeper/higher energy levels are detected with a larger V_{PP}. This also results in a more positive shift of the reverse trace. In addition, it can be seen that the loop width for a V_{PP} of 4 V still increases for a pulse width of 50000 μs while it is saturated in the case of 3 V. It implies that more traps are located at the energy levels corresponding to the voltage between 3 V and 4 V and the traps cannot be fully filled with charges for a pulse width of 50 ms. A negative value for the loop width implies that the shift contributed by the interface dipoles is more than that of the trapped electrons.

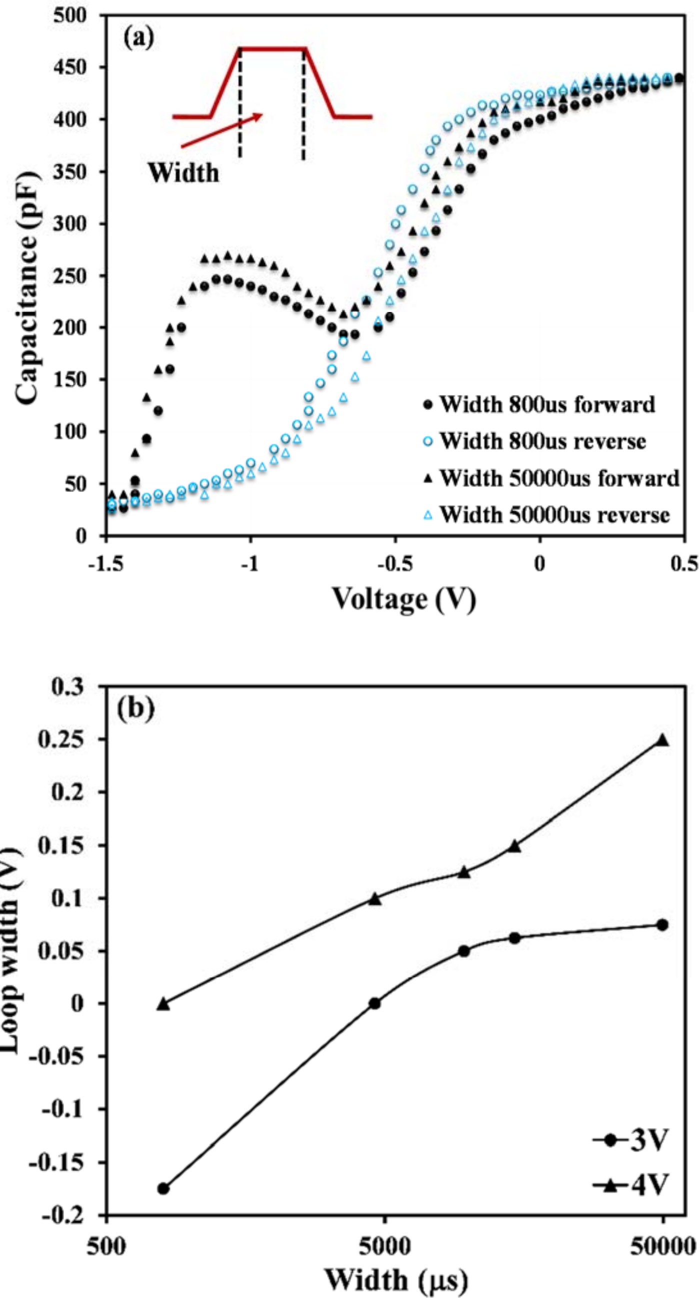


Figure 3.11 (a) Two selected CV characteristics of the 200 °C as-deposited sample with ZrO_2 dielectrics with different stress time. (b) The relationship between loop width and pulse width under different V_{PP} (3 V and 4 V). The pulse CV technique was performed with various pulse width times for a rising edge of 400 μs.

Figure 3.12 illustrates the relationship between loop width and pulse width which ranges from 800 μs to 50000 μs for the samples with ZrO_2 and HfO_2 dielectrics under a V_{PP} of 3 V and 4 V, respectively. In the first period (pulse width<12000 μs), the loop

width increases with the pulse width rapidly for both samples, which is mainly due to the response of the electrons trapped in the oxide induced by the positive stress on the gate electrode [20]. The longer the pulse width, the more electrons are supplied into the traps from the substrate. When the pulse width is larger than 12000 μs, the increase of the loop width becomes negligible despite the large increase in pulse width (from 12000 μs to 50000 μs). In regards to the loop width extracted from conventional CV measurements, they are larger than those obtained from pulse CV for both samples. This interesting behavior is mainly attributed to the significant dipole response in the pulse technique, which leads to the negative loop width and the effect of trapped electrons is compensated.

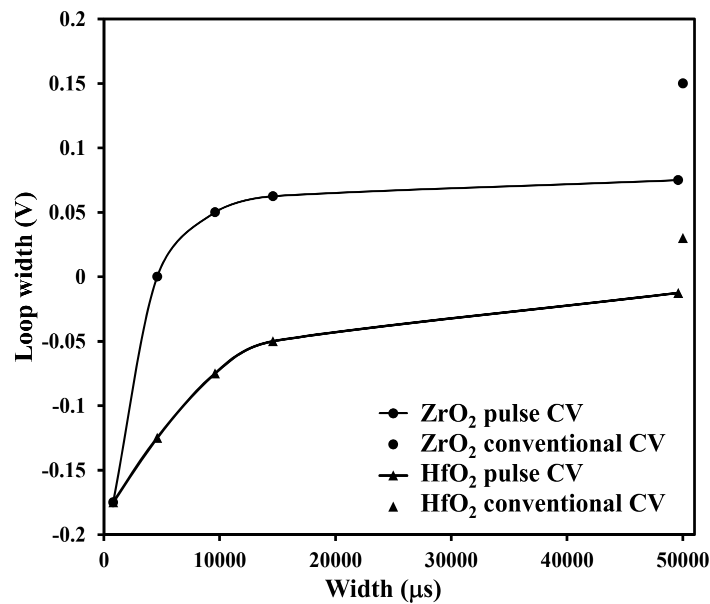


Figure 3.12 The relationships between loop width and pulse width for the samples with ZrO_2 and HfO_2 dielectrics under the V_{PP} of 3 V and 4 V, respectively. The loop width extracted from conventional CV is also presented for comparison.

From the above discussion, it is concluded that both interface dipoles and oxide traps affect the loop width of as-deposited samples when the pulse CV measurement is

implemented. With respect to the samples annealed in the FG and nitrogen environments, the effect of pulse width on loop width has also been investigated and the results for the samples with ZrO_2 dielectric layers are representatively summarized in Figure 3.13 and Figure 3.14. The pulse CV curves were measured with an edge time of 400 μs, a pulse width of 800 μs and a V_{PP} of 3 V using the pulse CV technique. The extraction of the CV characteristics is based on Formula (2.5). A zero loop width is measured using a pulse with a relatively small pulse width of 800 μs and an applied V_{PP} of 3 V for both samples (annealed in a nitrogen and FG environment). However, under the same measurement conditions, the as-deposited sample has a negative loop width. From these results, it seems that the abnormal CV behavior is suppressed after either FG or N_2 annealing. This behavior is due to suppression of the pulse-voltage-induced change of dipole separation, which contributes to the shift in the CV curves. Also, from the similar profile and trend of the FG and N_2 CV curves, it can be further inferred that the annealing process is responsible for the quenching of dipole separation rather than the annealing environment. Furthermore, only the reverse CV traces of both samples shift positively with the increase of pulse width. The above analysis implies that the changes of loop width are mainly attributed to captured electrons for the samples after annealing.

Figure 3.15 shows the dependence of loop width on the deposition temperature. The loop width was extracted from the pulse CV traces of the samples with ZrO_2 dielectrics deposited under different deposition and annealing conditions. The pulse CV

measurements were carried out with a pulse edge time of 400 μs, a pulse width of 800 μs and a V_{PP} of 3V for all samples.

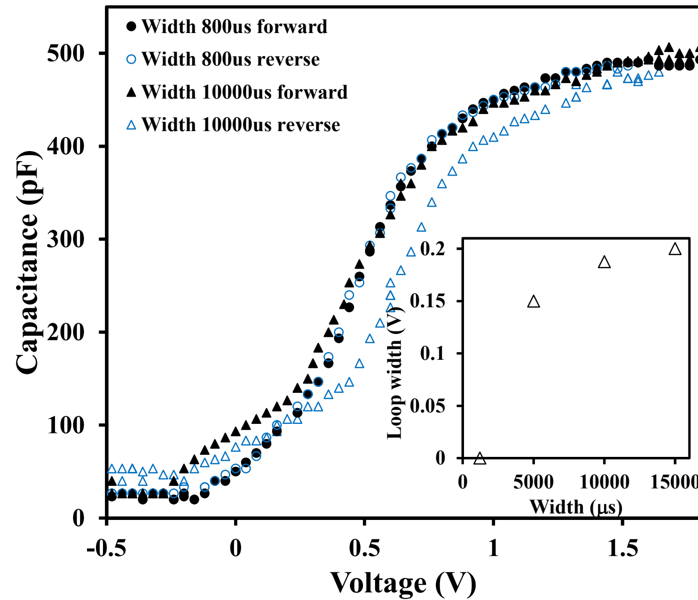


Figure 3.13 Pulse CV characteristics of the samples with ZrO_2 dielectric layers annealed in FG. The inset shows that the loop width increases with pulse width. The pulse technique was performed with various pulse time with at a rise time of 400 μs and V_{PP} of 3 V.

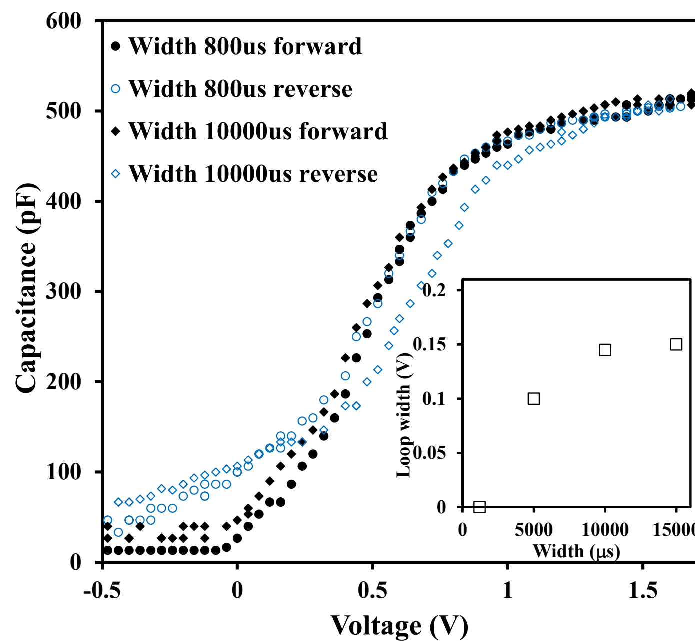


Figure 3.14 Pulse CV characteristics of the samples with ZrO_2 dielectric layers annealed in nitrogen. The relationship between pulse width and loop width is illustrated in the inset. The pulse CV technique was performed with various pulse width time at a rise time of 400 μs and VPP of 3 V.

In the above discussion, it was stated that the effect of interface dipoles is related to the annealing process rather than the annealing environment, therefore, the loop width extracted from the FG annealed samples are demonstrated representatively to compare with those from as-deposited ones for various deposition temperatures. From the observed changes of loop width for as-deposited samples, it is clear that loop width decreases with increasing of deposition temperature e.g. -0.2 V -0.15 V, and -0.125 V for 150 °C, 200 °C, and 250 °C, respectively. After annealing, the loop width becomes negligible for the samples deposited at 200 °C and 250 °C, while it still remains negative (-0.16 V) for the 150 °C sample, which implies that it is more difficult to suppress the effect of interface dipoles for the thin films deposited at lower temperatures.

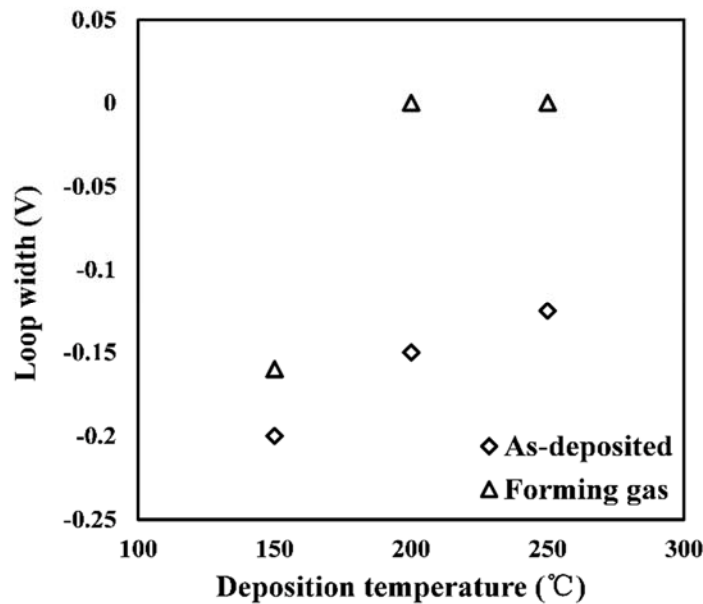


Figure 3.15 The comparison of loop width before and after FG annealing for the samples with ZrO_2 dielectric layer at various deposition temperatures.

Besides the anomalous CV behavior in loop width, another distinction (a hump) in the weak inversion region of the forward pulse CV trace is observed in comparison to the conventional CV curves shown in Figure 3.11 (a) and Figure 3.16 (a) for ZrO_2 and

HfO_2 dielectric MOS capacitors, respectively. Since the HfO_2 and ZrO_2 samples show similar behavior, only detailed discussions for the HfO_2 dielectric sample are presented. The pulse CV measurements were carried out with an edge time of 400 μs, a pulse width of 800 μs and a V_{PP} of 4 V. As shown in Figure 3.16 (b), a MOS capacitor with an n-type silicon substrate is employed in this discussion. A pn junction is formed between the p-type inversion layer and n-type substrate when the applied voltage is smaller than the mid-band voltage (-0.75 V in this case). When the MOS capacitor is switched rapidly from inversion to accumulation, the pn junction is forward biased and the injection and recombination of the channel carriers with carriers in the substrate produces an additional current displacement. This leads to the hump around the weak inversion region. In addition, the hump becomes more obvious with an increase in rise time as shown in Figure 3.16 (a). This phenomenon is related to the response time of the carriers. For relatively longer rise times, (the rise time is short enough that the pn junction still exists before the voltage becomes positively biased) the device has enough time to approach equilibrium and inversion before the ramp-up. The longer the rise time, the more holes that are available and the stronger the inversion becomes [2]. Thus, it will lead to a larger additional current displacement contributed to by the pn junction and a larger hump in the forward CV traces when compared with cases with a relatively shorter rise time [21].

However, in regards to the cases for reverse pulse CV traces, representing accumulation to inversion, the formed pn junction in the inversion region will never have the chance to be forward biased (The voltage sweeps from positive to negative).

Thus, no hump appears in the reverse CV traces. In conventional CV, due to the slow changing rate of the DC bias, several hundred milliseconds per step, the pn junction formed by the inversion layer and substrate in the inversion condition does not exist anymore when the applied signal sweeps to a positive voltage. Therefore, no additional current displacement is observed and in turn no hump is observed.

In regards to the formation of the hump, it is related to the response time of the carriers in the inversion region and the characterization speed of the measurement system. The hump will be observed in the condition that the rise time is short enough that the pn junction still exists when the voltage becomes positively biased (sweeping from negative to positive for n-type substrates). The response time of the carrier in the inversion region is related with the high-*k*/substrate interface quality. Improved interface quality, which can be achieved by PMA annealing, contributes to a faster response of the carrier. Therefore, no hump is observed in the forward pulse CV traces for the samples after PMA (Figure 3.13 and Figure 3.14) since the pn junction does not exist when the pulse voltage becomes positively biased due to the fast response of the carriers.

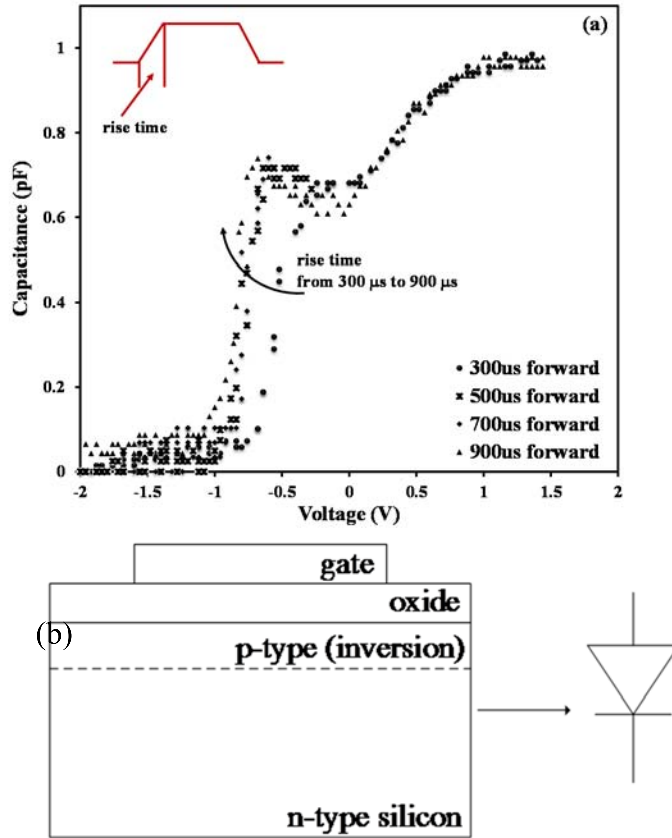


Figure 3.16 The behavior of forward pulse CV trace with different rising time for HfO_2 dielectric sample. An applied voltage from -2 V to 1.5 V was used. (b) The model for the pn junction formed between the p-type inversion layer and n-type substrate.

3.4 Summary

In summary, $LaZrO_x$ thin films were deposited on the n-type Si (111) substrates using ALD. A pulse CV technique was employed to investigate the traps in the oxides. It is found that the traps in the stack are highly dependent on the pulse edge time, pulse width and V_{PP} of the gate voltage pulse. The recovery of trapped electrons/holes is sensitive to the measurement time and shorter test times will lead to larger trap density measurements. Also, the longer the pulse width, the larger the electron fluency supplying charges into the traps in the oxide, this, in turn, leads to more trapped charges. With the higher voltage level, more traps are detected since the traps in the

deeper/higher energy level in the oxide are probed.

In addition, an anomalous CV characteristic was observed in the MOS capacitor if interface dipoles were formed during the deposition of the dielectric thin films. Relative positions of forward and reverse traces measured by a pulse CV technique are opposite to those measured using conventional CV methods. The reverse trace of the conventional CV curve is positively shifted with reference to the forward trace, whilst the shift becomes negative for pulse CV measurements. A model relating to interface dipoles was proposed to explain this anomalous behavior in CV traces. Also, this behavior is highly dependent on deposition temperature. The effect of interface dipoles is observed to be more significant for the samples deposited at lower temperatures. However, the effect of dipoles is suppressed when the samples are annealed in either FG or nitrogen environments at 350 °C for 30 minutes.

In regard to the humps observed in the forward CV traces, they are related to the edge rise time of the applied pulse signal and response time of the carrier. Usually, the hump is observed under the condition that the rise time is short enough that the pn junction still exists when the voltage becomes positively biased (sweeping from negative to positive for an n-type substrate). In addition, for a relatively longer rise time (but still on the order of microseconds), the device has enough time to approach equilibrium and the inversion condition before the ramp-up. When more holes are available the device becomes more strongly inverted, which leads to a larger hump in the forward CV traces.

3.5 References

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Chapter 4: Investigation of $Ti_xHf_{1-x}O_2$ deposited on Germanium substrates

Germanium has emerged as a promising candidate as a channel material for high-speed MOSFETs, mainly due to its high carrier mobility (approximately×2 for electrons and×4 for holes compared with those of silicon). However, due to the lack of a stable native oxide of germanium, it is difficult to fabricate a Ge MOSFET. A variety of dielectric materials have been investigated for this purpose. In this research, HfO_2 was mixed with varying amounts of a dielectric material, titanium oxide, permittivity k≈50-80, and used as the dielectric layer in MOS capacitors. The interface quality and chemical structure at the high-*k*/Ge interface was analyzed using XPS. Agilent B1500A was employed to investigate the CV/IV characteristics. All of the results are presented in Section 4.1. Development of an effective passivation of the germanium surface is a critical issue for the Ge MOS device, because deterioration of the interface will lead to an increase in leakage current and distortion of its CV curves. In a previous study, HfO_2 was deposited on a GaAs wafer and it was reported that a smaller frequency dispersion and a lower interface state were obtained when an in-situ ZnO passivation layer was employed [1]. Therefore, the trial of an in-situ ZnO passivation layer on Ge was carried out in Section 4.2. Furthermore, the effect of PDA on the CV/IV characteristics of the MOS capacitor was investigated.

4.1 Investigation of $Ti_xHf_{1-x}O_2$ on Germanium Substrates

XPS was used to characterize the interface quality and thin film structure of high-*k*/Ge stacks. Firstly, XPS was performed on 5 nm and 10 nm HfO_2 thin films to find out the chemical structure of the HfO_2 dielectrics in the depth direction. XPS is a

surface sensitive technique so the interface was probed using a thin film with a nominal thickness of 5 nm on a germanium substrate. As shown in Figure 4.1 (a) and (b), the Hf 4*f* line shape is typically composed of a $4f_{5/2}$ and $4f_{7/2}$ spin-orbit doublet [2]. With respect to the Hf $4f_{7/2}$ peak positions, there is a clear difference between the two thin films with different thicknesses. The sample with a thickness of 10 nm exhibits a lower binding energy (BE) peak at a position of 16.5 eV, which is tentatively assigned to stoichiometric HfO_2. For the sample with a thickness of 5 nm, the binding energy of the peak is centered at 17.3 eV, a difference of 0.8 eV in comparison with the 10 nm one. This increase is indicative of a greater interaction between the HfO_2 and Ge, and suggests stoichiometric and chemical changes at the interface. This is in accord with previous research, which has reported that the binding energy of the Hf $4f_{7/2}$ peak in $HfSi_xO_y$ is 1 eV higher than that from HfO_2, whose binding energy is in the range of 16.5-17 eV [3, 4]. Similar results were also found in Ge substrate MOS devices, which showed that there was about a 0.5 eV shift in binding energy for the Hf $4f_{7/2}$ peak from $HfGeO_x$ compared with that from HfO_2 [5, 6]. The shift in the Hf 4*f* binding energy is attributed to the formation of a germinate, $HfGeO_x$. In contrast, the XPS results in Figure 4.2 (a) and (b) for the TiO_2 samples in this experiment show that the Ti $3p_{3/2}$ peaks for the 5 nm and 10 nm samples are centered at the same position with a binding energy of 36.9 eV, suggesting that no chemical structure change occurs for the TiO_2 samples in the depth direction. Based upon the above analysis, it is inferred that HfO_2 will react with the Ge atoms at the interface without effective passivation of the substrate. Formation of $HfGeO_x$ at the interface deteriorates the interface quality and increases the leakage current in the stack [5, 7].

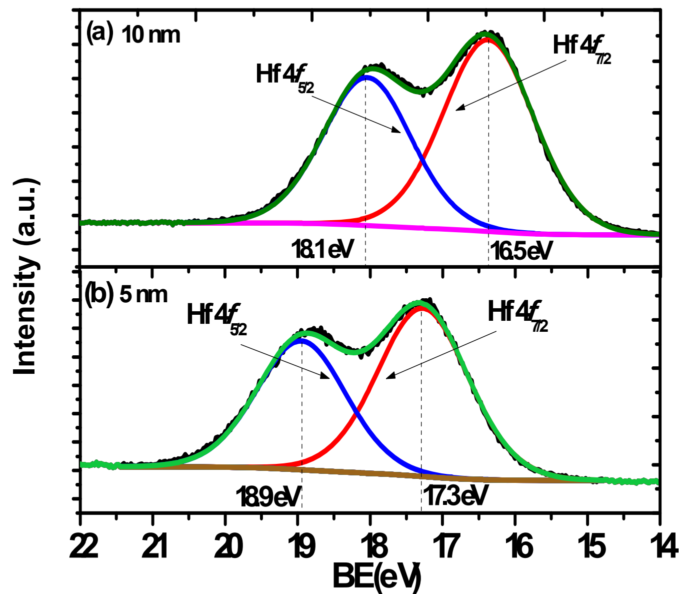

Figure 4.1. The XPS line shape for HfO_2 thin films with a thickness of (a) 10 nm and (b) 5 nm.

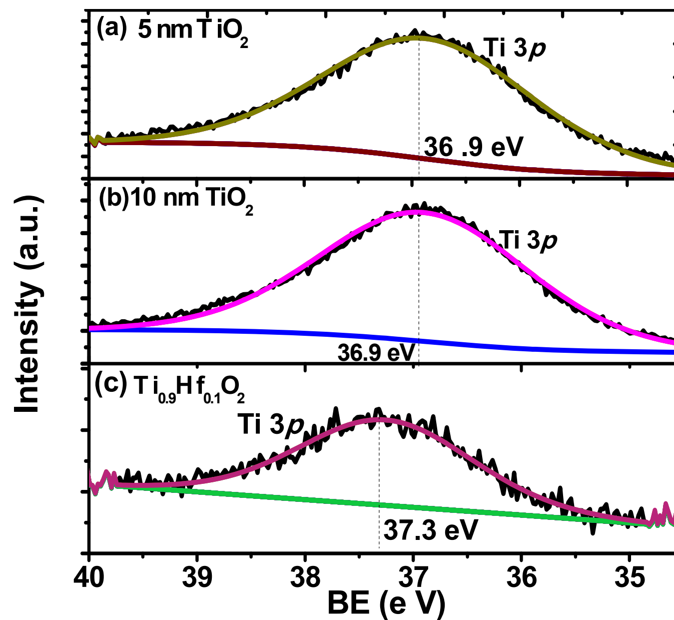

Figure 4.2. The Ti 3p spectra from (a) 5 nm TiO_2, (b) 10 nm TiO_2, and (c) 5 nm $Ti_{0.9}Hf_{0.1}O_2$ thin films.

Figure 4.2 (c) compares the Ti 3p spectrum from the $Ti_{0.9}Hf_{0.1}O_2$ sample with the Ti 3p from the pure TiO_2 sample, each thin film on a germanium substrate. Figure 4.3 shows the Hf 4$f_{7/2}$ spectra from the same $Ti_{0.9}Hf_{0.1}O_2$ sample (5 nm) and compares it with Hf 4$f_{7/2}$ from the pure HfO_2 thin film (5 nm). It is clear that the Hf 4$f_{7/2}$ binding energy from the $Ti_{0.9}Hf_{0.1}O_2$ sample, 17 eV, is smaller than that from the pure HfO_2

sample, 17.3 eV (The $Ti_{0.25}Hf_{0.75}O_2$ sample also has the same Hf 4*f* $_{7/2}$ binding energy as the $Ti_{0.9}Hf_{0.1}O_2$ sample, 17 eV). In addition, Figure 4.2 (a) and (c) show that there is also a difference of 0.4 eV in the binding energy of the Ti 3*p* spectra between TiO_2 (36.9 eV) and $Ti_{0.9}Hf_{0.1}O_2$ (37.3 eV). For the $Ti_{0.25}Hf_{0.75}O_2$ sample, the Ti 3*p* spectrum is found to be shifted to a higher binding energy by about 0.2 eV, while Hf 4*f* shifts to a lower binding energy by around 0.3 eV. The shift of the Hf $4f_{7/2}$ peak in the $Ti_xHf_{1-x}O_2$ sample to a lower binding energy and the Ti 3*p* to a higher binding energy suggests that an electron transfer from HfO_2 to TiO_2 takes place as a result of mixing the TiO_2 and HfO_2.

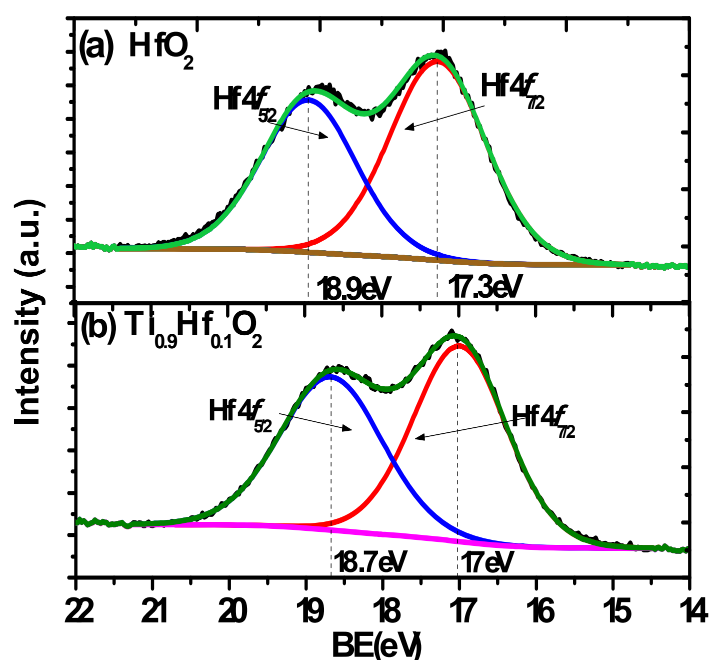

Figure 4.3. The Hf 4*f* spectra from 5 nm thin fims of (a) HfO_2 and (b) $Ti_{0.9}Hf_{0.1}O_2$ on Ge.

In addition, from the analysis of the Ge 3*d* spectra from the four samples with a thickness of 5 nm shown in Figure 4.4, more information about the Ge surface can be deduced. The corresponding O 1*s* spectra for each of the four samples is shown in Figure 4.5. The peaks corresponding to Ge from elemental Ge and GeO_x are labeled in the figures. The presence of Ge^{2+}, Ge^{3+}, and Ge^{4+} is due to the oxidation of the germanium substrate in the interfacial region, as well as germinate formation. Table 4-1

shows the compositions extracted from the line fits, relative to the bulk substrate Ge^0 peak, of the various components at the interface for the four samples. It is clear that the oxidation is much less for the TiO_2 dielectric sample (Figure 4.4 (a)) in comparison to the other samples, while the oxidation of the substrate in the case of HfO_2 is much greater (Figure 4.4 (d)). The fitting of the spectra shows an absence of Ge^{+4} in the TiO_2 sample, while an incremental increase of the GeO_x intensity, especially Ge^{+4}, is observed with increasing HfO_2 content. This suggests that increasing the amount of HfO_2 in the dielectric films provides more oxidation sources to the interface [8]. This was also observed in other research, which stated that Ge atoms were oxidized by the oxygen atoms provided by the HfO_2 layer [9]. Furthermore, the Hf $4f_{7/2}$ binding energy difference for the HfO_2 samples with different thicknesses are shown in Figure 4.1 (a) and (b) as discussed above, and also support this finding. Therefore, it is inferred that HfO_2 is a factor in the oxidation of the interface. With regard to the significant binding energy shift of the Ge 3*d* spectra from the samples, it is partially attributed to the presence of a mixture of oxides of GeO_x (where $x<2$) and GeO_2 at the interfacial region. The GeO_x, referred to as a suboxide in the following discussion, consists of a structure with fewer than four oxygen atoms attached to one Ge atom. GeO is known to exhibit a signal at a binding energy lower than that of GeO_2 [10]. In this experiment, the concentration of GeO_2 and the x value differ from each other for the four samples. Ge^{4+} is absent in the pure TiO_2 layer and minimal for the $Ti_{0.9}Hf_{0.1}O_2$ sample on the germanium, while it is at a maximum for the pure HfO_2 layer. Therefore, this behavior causes the resultant intensity of the spectral component due to GeO_2 to increase, with a concomitant decrease in intensity of the peak of GeO_x for oxygen rich samples. This intensity variation leads to a shift of the overall peak [10, 11]. A similar phenomenon in the Ge 3*d* spectra shift was also observed by Caymax in an interface study of the

HfO_2 gate dielectric deposited on Ge [12]. In addition, the formation of $HfGeO_x$ due to the reaction between HfO_2 and Ge is also a contributing factor in the shift of the Ge 3*d* spectra [13, 14].

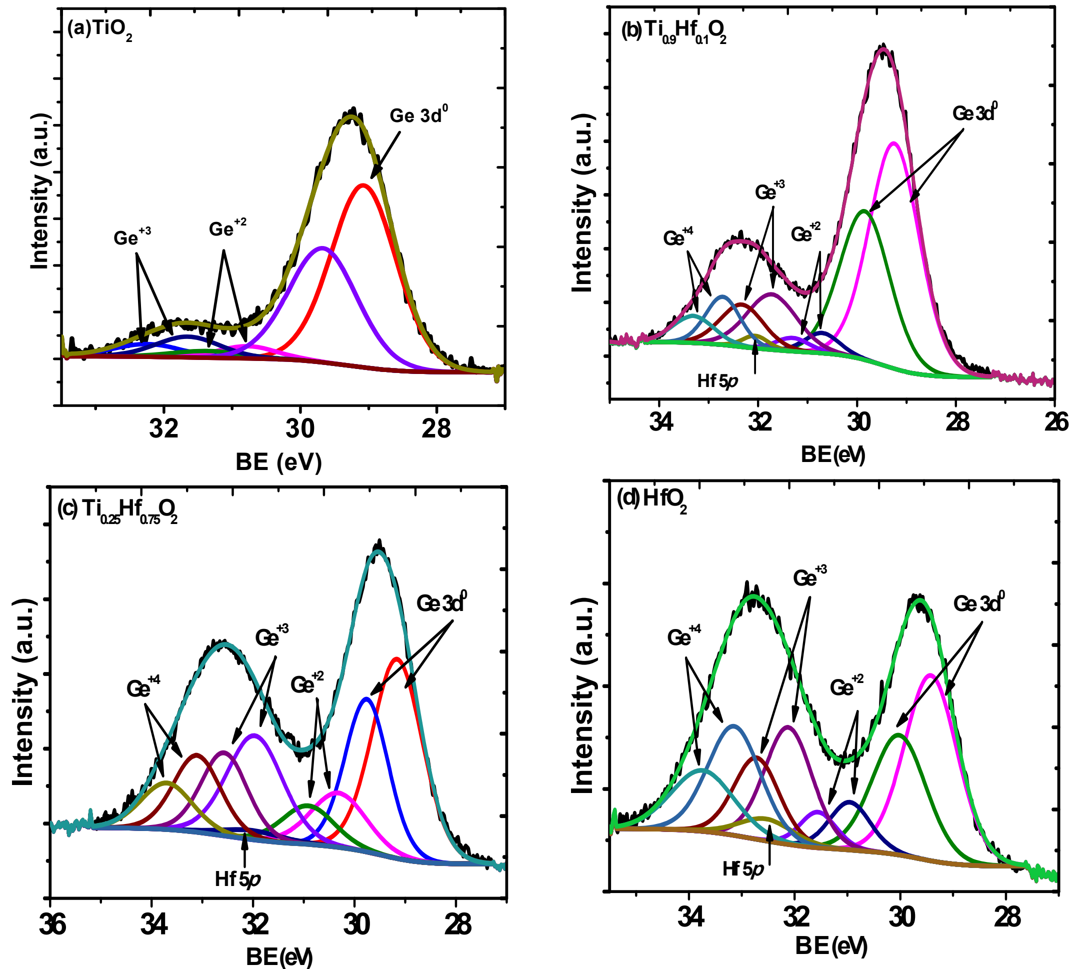

Figure 4.4 Ge 3*d* spectra from 5 nm thin films of (a) TiO_2, (b) $Ti_{0.9}Hf_{0.1}O_2$, (c) $Ti_{0.25}Hf_{0.75}O_2$, and (d) HfO_2 samples.

An AFM was used to examine the surface roughness of the samples for a scan area of 100 nm×100 nm. The surface roughness of the samples was quantitatively determined by the root-mean-squared roughness (R_{rms}) as defined by Formula (2.1) in Chapter 2. All samples exhibit smooth surfaces with calculated R_{rms} roughnesses of 0.325 nm, 0.431 nm, 0.425 nm, and 0.202 nm for TiO_2, $Ti_{0.9}Hf_{0.1}O_2$, $Ti_{0.25}Hf_{0.75}O_2$, and HfO_2 respectively. A roughness for the thin films of <0.5 nm demonstrates a nearly atomically smooth surface [15].

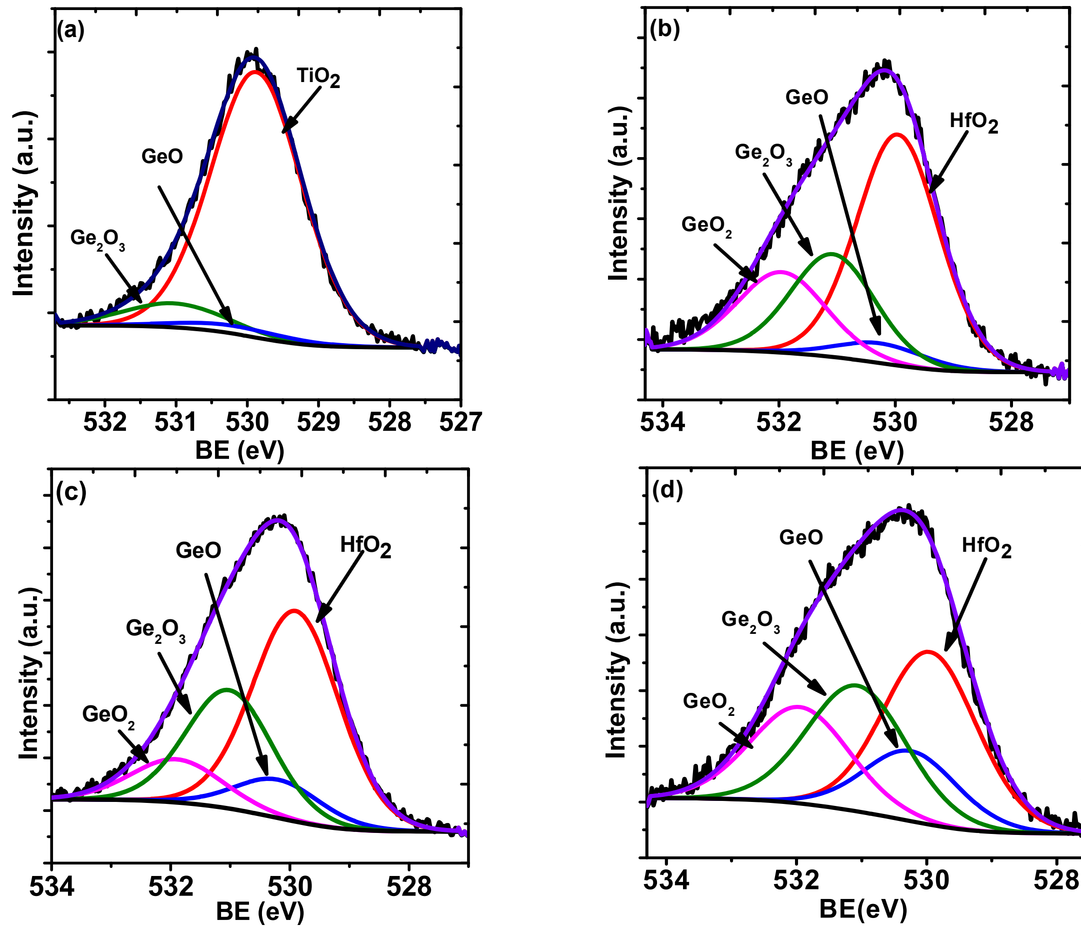

Figure 4.5 O 1s spectra from 5 nm thin films of (a) TiO_2, (b) $Ti_{0.9}Hf_{0.1}O_2$, (c) $Ti_{0.25}Hf_{0.75}O_2$, and (d) HfO_2.

Table 4-1 Compositions extracted from the line fits shown in Figure 4.4, relative to the bulk substrate Ge^0 peak for the four samples.

Materials	Ge^{+2}	Ge^{+3}	Ge^{+4}
TiO_2	0.06	0.12	–
$Ti_{0.9}Hf_{0.1}O_2$	0.06	0.24	0.14
$Ti_{0.25}Hf_{0.75}O_2$	0.17	0.24	0.41
HfO_2	0.13	0.45	0.75

Figure 4.6 shows XRD patterns for the four samples with different compositions of TiO_2 and HfO_2. Measurements were performed on the samples with a nominal thickness of 10 nm (the actual thickness was in the range of 8-11 nm determined by ellipsometer). For all samples, no noticeable diffraction peaks were observed, except for the one

coming from the substrate centered at around 31.5°. According to the results of the XRD measurements, it seems that all of the thin films remain amorphous under these deposition conditions. However, due to the small thickness of the thin films, around 10 nm, the sensitivity of the XRD may not be sufficient to detect a limited amount of a crystalline phase if it is present, as described in [16, 17]. It is possible that a Transmission Electron Microscope (TEM) or Selected Area Electron Diffraction (SAED) could offer more information as to the exact morphology of the thin films in future work.

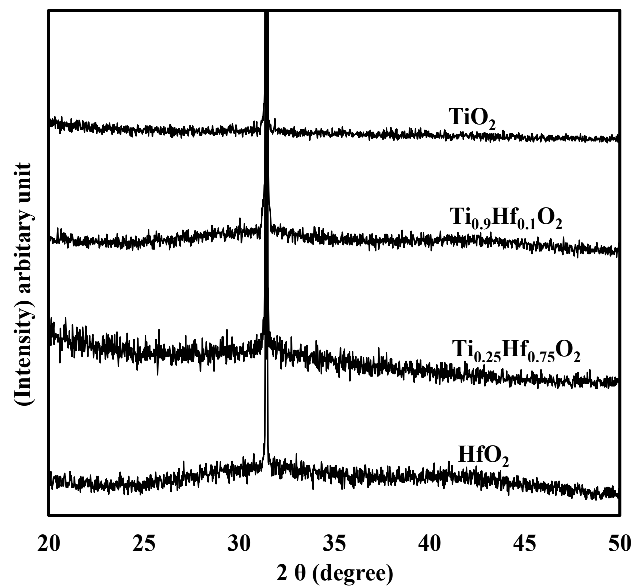

Figure 4.6 XRD patterns for the 10 nm HfO_2, $Ti_{0.25}Hf_{0.75}O_2$, $Ti_{0.9}Hf_{0.1}O_2$, and TiO_2 thin films deposited on the germanium substrate.

Conventional CV curves were obtained by sweeping the gate voltage from −1 V to 0.5 V in both directions (forward and reverse) at a frequency of 1 MHz using an Agilent 4284A LCR meter. Due to an unacceptable distortion of the CV characteristics caused by the leakage current for the TiO_2 sample, reported below, only the CV curves extracted from HfO_2, $Ti_{0.25}Hf_{0.75}O_2$, and $Ti_{0.9}Hf_{0.1}O_2$ samples are presented in Figure 4.7. The high frequency CV measurements on the three as-grown thin films show that the samples have low trap densities because there is almost no hysteresis

between the forward and reverse traces of the CV curves [18, 19]. Due to the dielectric relaxation, an obvious frequency dispersion is observed [20-22]. The change of the measurement capacitance due to the dielectric relaxation is not covered in this section but will be discussed in Section 5.2. Regarding the CV characteristics of the $Ti_{0.25}Hf_{0.75}O_2$ sample, it is noted that saturation in the accumulation region (NMOS in this section) is not obtained, regardless of the bias voltage level. This behavior is attributed to the large leakage current of this sample, which is partially related to the deterioration of the interface as discussed above in the XPS analysis. Further comments regarding the leakage current are made in the following section.

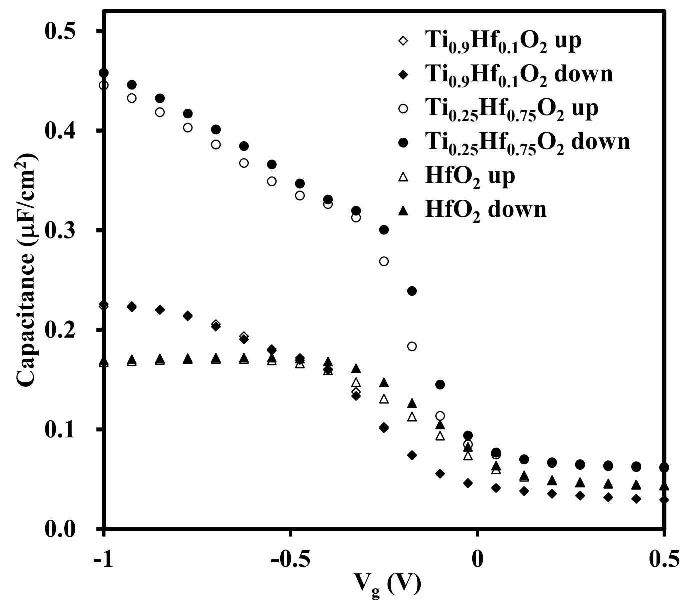

Figure 4.7. CV characteristics of the samples with $Ti_{0.9}Hf_{0.1}O_2$, $Ti_{0.25}Hf_{0.75}O_2$, and HfO_2 dielectrics.

Figure 4.8 illustrates the relationship between the gate leakage current density and the bias voltage of the samples. The maximum current limit of the instrument is set at 2 mA. From observations of Figure 4.8, it is apparent that the titanium oxide has the highest leakage current level, followed by the HfO_2 and $Ti_{0.25}Hf_{0.75}O_2$ thin films, both of which have similar leakage current levels. The $Ti_{0.9}Hf_{0.1}O_2$ sample has the lowest leakage current. The large leakage current for the TiO_2 sample is attributed to the small

band gap of TiO_2 as shown in Figure 4.9 (a) and discussed further below. For the $Ti_{0.9}Hf_{0.1}O_2$, $Ti_{0.25}Hf_{0.75}O_2$, and HfO_2 samples with larger band gaps, it is clear that the leakage current increases with an increase of HfO_2 concentration. Previous research also reports that a large leakage current is caused by the formation of $HfGeO_x$ at the interface between HfO_2 and Ge, and the leakage current is reduced if a germanium nitride barrier layer is first introduced, preventing the formation of $HfGeO_x$ [9]. High leakage current behavior, therefore, is probably due to the deterioration of the interfacial layer caused by the interaction of HfO_2 and Ge, which is consistent with the results shown in Figure 4.4 [6, 23]. Thus, the increase in the leakage current clearly correlates with the HfO_2 rich samples. For the TiO_2 doped samples, the TiO_2 will react with HfO_2 to form $HfTiO_x$, consuming the HfO_2, which will otherwise have reacted with the Ge at the interface. It is possible that other mechanisms also exist to suppress the leakage current as observed in the titanium doped tantalum oxide [24]. Titanium doping was found to suppress the oxygen vacancies in tantalum oxide capacitors, which resulted in a significant reduction in the leakage current [24]. For the HfO_2 capacitors, there are a considerable number of oxygen vacancies [25-28], which could potentially be suppressed when titanium is doped into the HfO_2.

Although the titanium incorporation seems to suppress the leakage current, the leakage current density is still relatively large (~10^{-3} A/cm^2). The energy band diagrams in Figure 4.9 provide an explanation in conjunction with the XPS results discussed previously [29, 30]. From the energy band diagram in Figure 4.9 (a), titanium oxide has a relatively small band gap (3.2 eV), while the band gap and conduction band minimum for germanium are 0.66 eV and 4.13 eV, respectively.

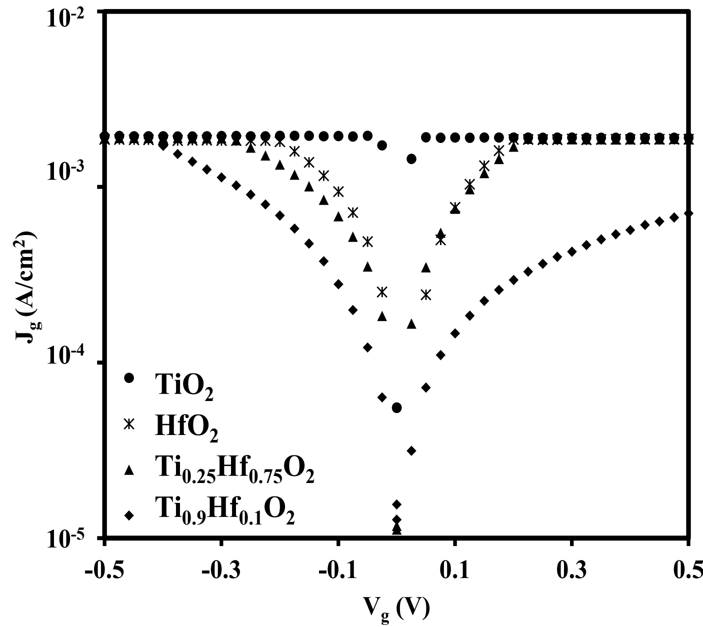

Figure 4.8. Gate leakage current density (J_g) versus gate voltage (V_g) for the samples with HfO_2, $Ti_{0.25}Hf_{0.75}O_2$, $Ti_{0.9}Hf_{0.1}O_2$, and TiO_2 dielectrics.

A thin aluminum oxide with a thickness of around 0.3 nm is used to passivate the germanium surface and makes almost no contribution to suppressing the leakage current. If a voltage is applied at the gate on the TiO_2/Al_2O_3 stack, a dramatic leakage current will be induced, considering the energy band diagram shown in Figure 4.9 (a). Regarding the energy band diagram of the HfO_2 shown in Figure 4.9 (b), the band gap is wider and the conduction band minimum is higher than that of the TiO_2. Thus, the HfO_2 sample has a higher potential barrier across the oxide. Therefore, the leakage current of the HfO_2 is five times smaller than that of the TiO_2, regardless of the deterioration of the interface caused by the oxidation of the substrate. When TiO_2 is doped into HfO_2, the reaction of the TiO_2 and HfO_2 adjusts the energy band diagram as shown in Figure 4.9 (c), and the leakage current should be between that of TiO_2 and HfO_2. However, as mentioned above, HfO_2 is considered to be an oxidation source and contributes to the formation of hafnium germinate, which enhances the leakage current for the HfO_2 rich samples. Fortunately, the formation of $HfTiO_x$ in TiO_2-doped HfO_2 reduces the reaction between HfO_2 and germanium and suppresses the formation of

$HfGeO_x$, which results in a significant reduction in leakage current. Therefore, in this case, the $Ti_{0.25}Hf_{0.75}O_2$ dielectric sample has almost the same leakage current as the HfO_2 sample while the $Ti_{0.9}Hf_{0.1}O_2$ sample with much less HfO_2 has the smallest leakage current among all samples.

4.2 Effect of PDA on $Ti_xHf_{1-x}O_2$ Dielectric MOS Capacitors

$Ti_{0.1}Hf_{0.9}O_2$ thin films were deposited with 100 ALD cycles on germanium substrates. Before the deposition of the $Ti_xHf_{1-x}O_2$ dielectrics, ZnO thin films (10 ALD cycles) to be used as passivation layers were deposited. The ZnO interfacial layer has been reported to improve the device performance with GaAs substrates as discussed previously. After the deposition of the high-*k* dielectrics, two samples received PDA in nitrogen for 30 seconds at 450 °C and 550 °C, respectively. An AFM was employed to examine the surface roughness of the samples for a scan area of 500 nm×500 nm. Nearly atomically smooth surfaces with roughnesses of 0.282 nm, 0.532 nm and 0.398 nm for the as-deposited, 450 °C PDA and 550 °C PDA samples respectively are quantitatively determined by the root-mean-squared roughness (R_{rms}) as defined in Formula (2.1) in Chapter 2 [15].

After the examination of the surface roughness of the sample, the electrical properties in terms of CV characteristics and leakage current, were investigated. Due to the distortion of the CV curves for the as-deposited samples, they are not presented for comparison.

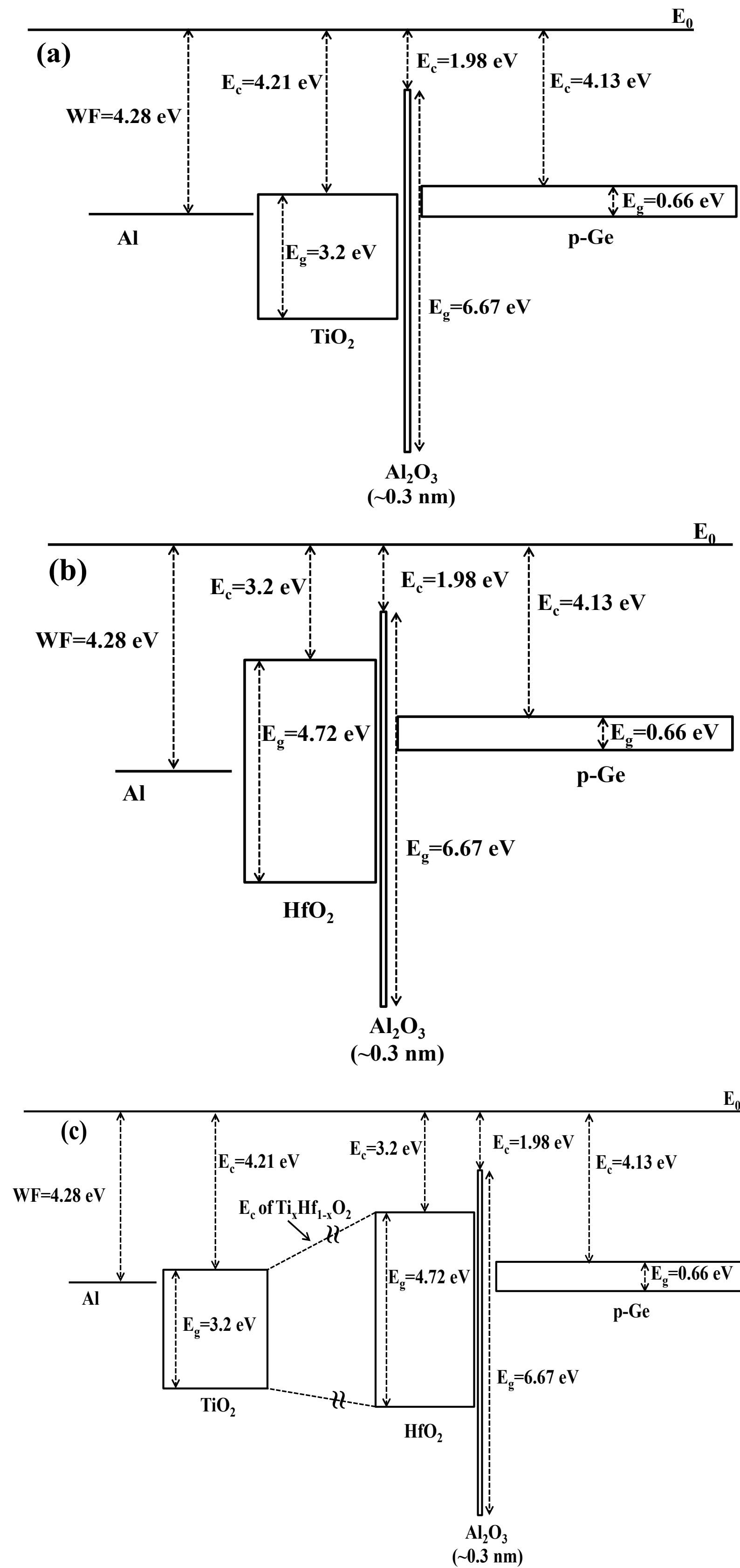

Figure 4.9. Energy band diagrams for (a) TiO_2, (b) HfO_2, and (c) titanium doped hafnium oxide.

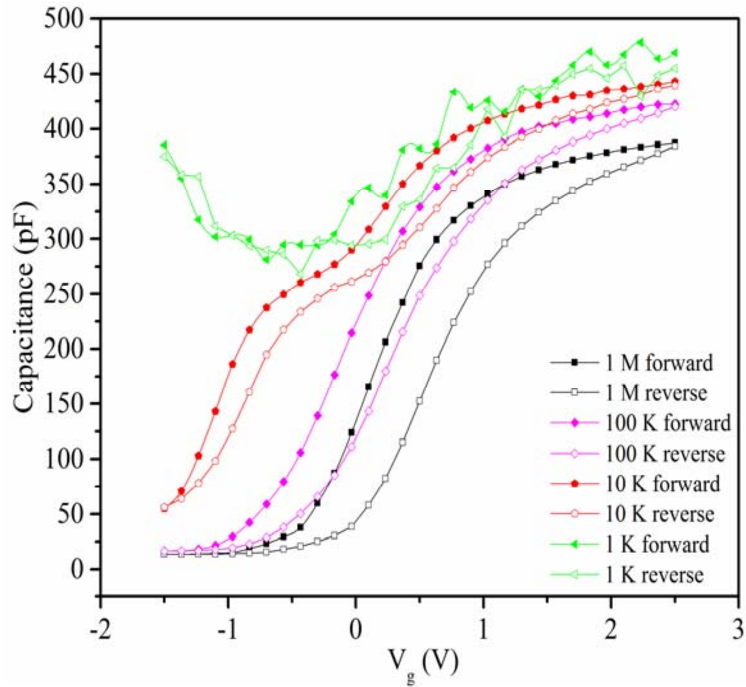

Figure 4.10 CV characteristics of the $Ti_{0.1}Hf_{0.9}O_2$ dielectric MOS capacitor after 450 °C PDA for 30 seconds.

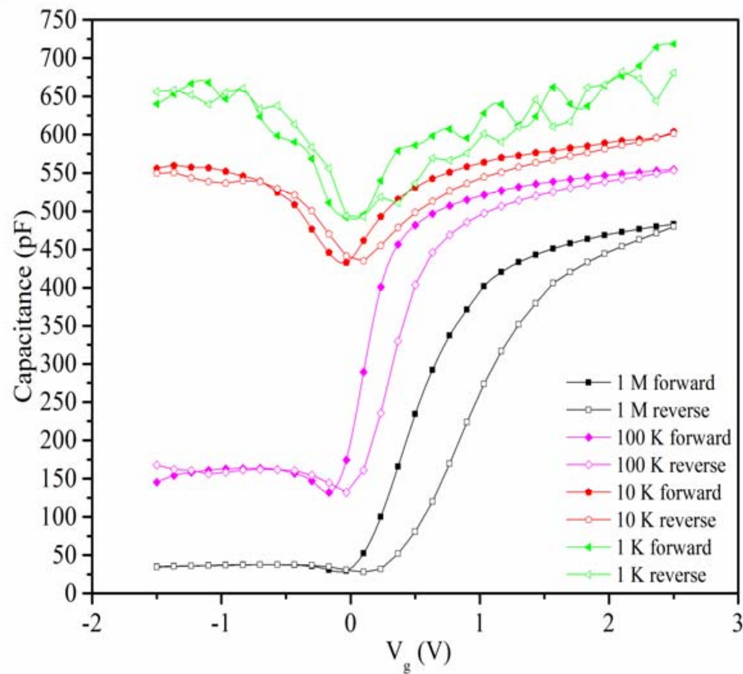

Figure 4.11 CV characteristics of the $Ti_{0.1}Hf_{0.9}O_2$ dielectric MOS capacitors after 550 °C PDA for 30 seconds.

In order to overcome this problem, PDA in nitrogen for 30 seconds at 450 °C and 550 °C was attempted. The corresponding CV characteristics are illustrated in

Figure 4.10 and Figure 4.11. Although the large distortion of the CV curves has been overcome and smooth CV curves have been obtained, significant frequency dispersion still exists, which can be seen from the change in capacitance for different measurement frequencies. The CV characteristics of the 450 °C annealed sample measured using frequencies from 1 kHz to 1 MHz, are shown in Figure 4.10. This phenomenon is caused by dielectric relaxation, likely due to parasitic effects, a lossy interfacial layer, and the surface roughness of the samples as reported in previous research outputs [20, 31, 32].

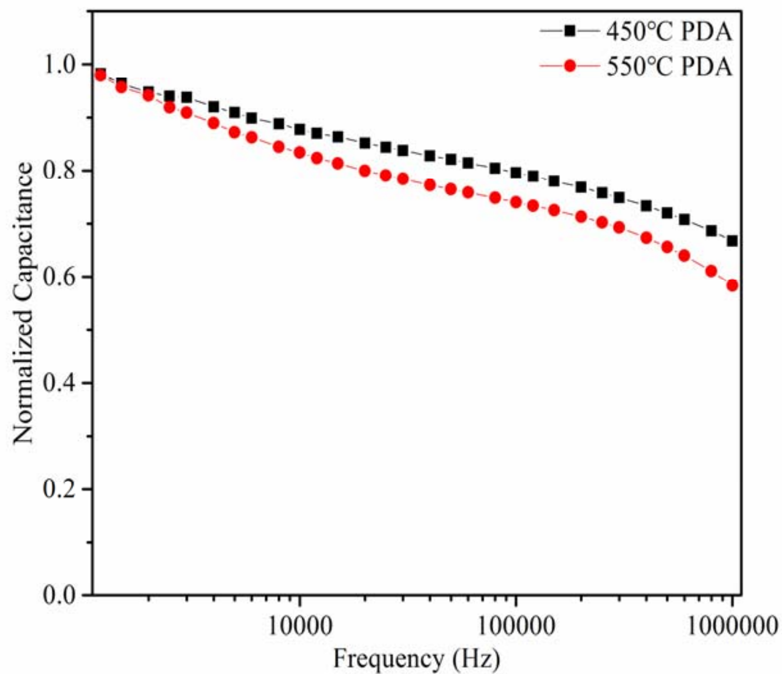

Figure 4.12 Capacitance versus frequency for the 450 °C PDA and 550 °C PDA samples.

In order to present the frequency dependence of the capacitance clearly, the relationship between normalized capacitance and frequency (C-f) for the 450 °C and 550 °C PDA samples is summarized in Figure 4.12. The capacitance is normalized by its maximum capacitance at a frequency of 1 kHz. A more significant frequency

dispersion is observed for the 550 °C PDA sample. (due to the distortion of the CV traces for the as-deposited sample, the C-f is not presented here. The results are presented provided in Figure A.1 of the Appendix) The more significant frequency dispersion of the 550 °C PDA sample is due to greater crystallization of the dielectric following the higher temperature annealing [22, 32].

Due to the small thickness of the dielectric, it is difficult to analyze the crystallization of the thin films by XRD. However, from previous research, it can be inferred that the thin film is highly likely to be crystalized since the crystallization temperature of HfO_2 is around 400 °C-500 °C and 550 °C PDA was performed in this experiment [8, 33, 34]. In addition, the higher leakage current density extracted from the 550 °C PDA sample compared with that from the 450 °C PDA sample is shown in Figure 4.13, which also indicates greater crystallization in the 550 °C PDA sample [34].

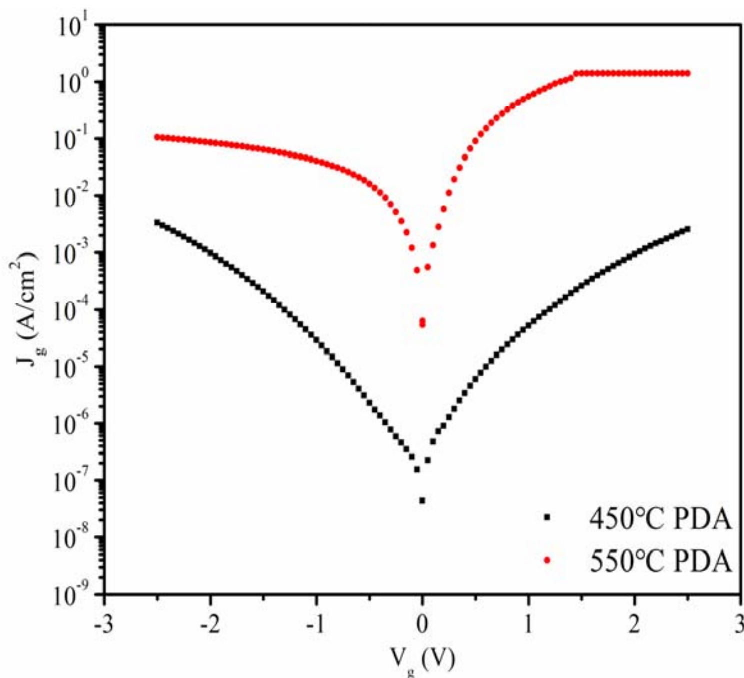

Figure 4.13 Leakage current densities for the 450 °C and 550 °C PDA samples.

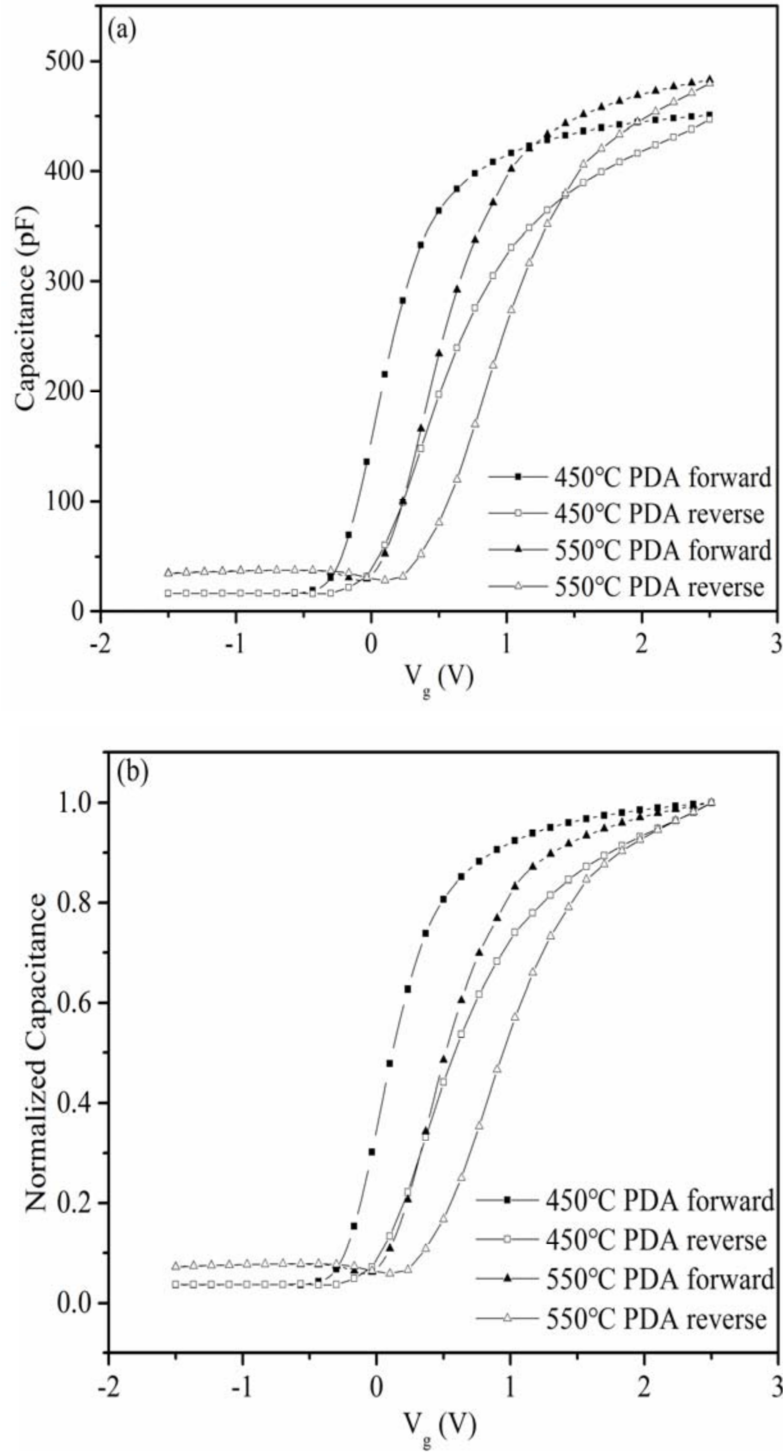

Figure 4.14 (a) Comparison of the CV characteristics extracted from the 450 °C PDA and 550 °C PDA sample and (b) The corresponding normalized CV characteristics.

Hysteresis and interface quality degradation during the measurement of the CV traces was also observed. The 450 °C PDA and 550 °C PDA samples have a difference in

accumulation capacitance as shown in Figure 4.14 (a), the corresponding normalized capacitance is shown in Figure 4.14 (b). From the normalized capacitance, a positive shift in the CV characteristics is observed for the 550 °C PDA samples, which results in a reduction of the oxygen vacancies due to the higher PDA temperature [35]. For the reverse CV trace (empty square) extracted from the 450 °C PDA sample, a degradation of the interface quality is observed by the change of the slope in the CV traces. This phenomenon is attributed to defect generation due to the applied voltage stress [36].

4.3 Summary

In this chapter, $Ti_xHf_{1-x}O_2$ thin films were deposited on n-type germanium wafers using ALD at 300 °C. XPS was used to analyze the interface quality and chemical structure. The results indicate that the GeO_x and germinate are formed at the interface and a severe deterioration of the interface quality occurs, which leads to an enhanced leakage current. The large leakage current is partially attributed to the deterioration of the interface between the Ge and $Ti_xHf_{1-x}O_2$ caused by the oxidation source from the HfO_2. The small band gap of the dielectric materials is also a cause for the observed leakage current behavior. The electrical characterization shows very low hysteresis between forward and reverse CV traces, which indicates low trap densities in the stack. In the sample with a ZnO passivation layer, a larger distortion in the CV trace of the as-deposited sample was observed. After PDA, a smooth CV trace was obtained and there was an obvious increase in frequency dispersion and leakage current. Therefore, the ZnO interfacial layer cannot effectively passivate the germanium substrate.

4.4 References

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Chapter 5: Passivation of the Ge MOS devices with high-*k* dielectrics

In Chapter 4, it was concluded that the reaction between the high-*k* dielectric and germanium substrate will deteriorate interface quality and hence increase the gate leakage current of the device. Therefore, a suitable passivation technique constitutes a major stepping stone in moving toward the use of Ge in producing high-performance MOSFETs. Recently, a number of techniques have been proposed to passivate the germanium surface and it has been reported that the introduction of sulfur into the GeO_x can result in a superior Ge gate stack [1, 2]. In addition, nanowires passivated by organic chemicals containing sulfur, such as alkanethiol solutions, show better properties in preventing the surface from oxidation [3, 4]. This method may also be helpful for the performance of Ge MOS devices. Among the frequently used alkanethiol solutions, the propanethiol (C_3H_7HS) and octanethiol ($C_8H_{17}HS$) have less carbon than hexadecanethiol ($C_{12}H_{25}HS$) due to short alkyl chains, which means less impurity will be introduced. Also, the surface coverage efficiency is acceptable for propanethiol and octanethiol (better surface coverage is obtained for alkanethiols with longer alkyl chains). Therefore, the propanethiol and octanethiol solutions are investigated here for their ability to effectively passivate the germanium substrates. In addition, FG annealing has also been reported to have an influence on the device performance, such as the suppression of frequency dispersion, reduction of fixed charges and interface states, though this is largely dependent on the annealing time and temperature used [5, 6]. Furthermore, GeO desorption from the gate oxide/Ge interface into the dielectric

thin film is considered as one of the main factors resulting in the deterioration of the device performance. Therefore, reduction of the GeO formation is also an important issue. In this chapter, HfO_2 thin films were deposited onto germanium wafers passivated using different methods including the organic solutions discussed. PMA was then performed to investigate its effect on the electrical characteristics of the MOS capacitors. Finally, a MOS capacitor with a TiN cap layer was fabricated and the influence of the TiN cap layer was explored.

5.1 Deposition of High-*k* Dielectrics on Ge Wafers with Chemical Treatments

In this section, germanium substrates were passivated using three different wet chemical solutions, namely propanethiol (C_3H_7HS, labelled PT), octanethiol ($C_8H_{17}HS$, labelled OT) and ammonium sulfide ($(NH_4)_2S$, labelled NS). A control sample without any treatment was labelled WT. The effect of the passivation techniques on the physical and electrical properties was investigated. Firstly, an AFM was used to examine the surface roughness of the thin films deposited on the substrates using the three different passivation methods. The root-mean-squared roughness for the control sample, propanethiol passivated, octanethiol passivated and ammonium sulfide passivated samples are 0.783 nm, 0.636 nm, 0.649 nm and 0.696 nm, respectively. The samples with chemical treatments exhibit better surface roughness than the control sample due to the effect of surface passivation as has also been observed in other research [7]. The lower surface roughness leads to a reduction in the carrier scattering effects between

the gate oxide and the substrate, which is beneficial to the carrier mobility of the device [8, 9].

Figure 5.1 shows the XRD patterns for the four samples with different passivation methods. The measurements were performed on the samples with thicknesses of around 20 nm, as measured by ellipsometer. For all the samples, no noticeable diffraction peaks were observed, except for the one coming from the substrate centered at around 31.5 ° corresponding to the Ge substrate. According to the results of the XRD patterns, it appears that all of the thin films remain amorphous under these deposition conditions. These results indicate that the morphology of the dielectrics is not influenced by the chemical pretreatments on the substrates. Also, the amorphous nature of the HfO_2 thin films brings the benefit of relatively smaller leakage current levels [10]. This will be discussed later.

Figure 5.2 (a) shows the CV characteristics of the four samples with different passivation methods and the corresponding normalized CV curves are presented in Figure 5.2 (b). Conventional CV measurements were performed at a frequency of 1 MHz using an Agilent 4284A LCR meter. The loop width, or hysteresis, is included in the inset of Figure 5.2 (b). Although all of the dielectrics have almost the same thickness (around 20 nm), there is a large difference in capacitance. The sample passivated by the octanethiol solution has the largest capacitance followed by propanethiol and $(NH_4)_2S$ treatments. The control sample has the lowest capacitance. The increase in the capacitance of the samples after chemical treatment is due to a thinner GeO_x layer as a result of the passivation applied.

Also, for the samples passivated by organic solutions (PT and OT), the formation of alkyl chains (or subsequent reaction products) also enhances the dielectric constant [11]. In addition, the PT and OT passivated samples have slightly smaller loop widths. This results from less interfacial slow traps and/or mobile charges in the oxides [12]. In other words, passivation by organic solutions will reduce the trap density.

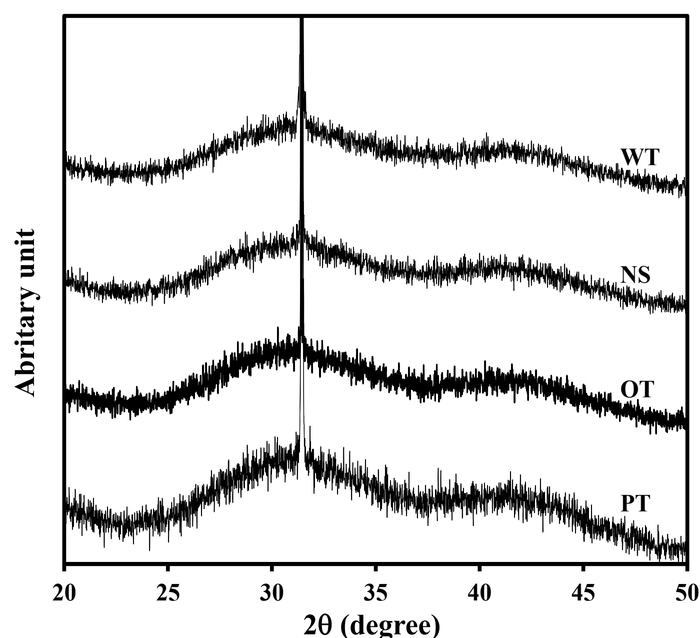

Figure 5.1. XRD patterns of the samples with different passivation methods showing only the diffraction peak for the Ge substrate at 31.5°.

Figure 5.3 shows the leakage current densities of ALD grown HfO_2 films on Ge substrates treated by different surface passivation methods. Apart from the smaller loop width of the CV characteristics obtained by the surface passivation method as discussed above, the leakage current densities for the passivated samples are also reduced dramatically. The sample passivated by the $(NH_4)_2S$ solution has the smallest leakage current density followed by the ones passivated by octanethiol and propanethiol solutions (labeled OT and PT in Figure 5.3). In particular, the leakage current density

of the NS sample is one order of magnitude smaller than that of the control sample (labeled WT in Figure 5.3).

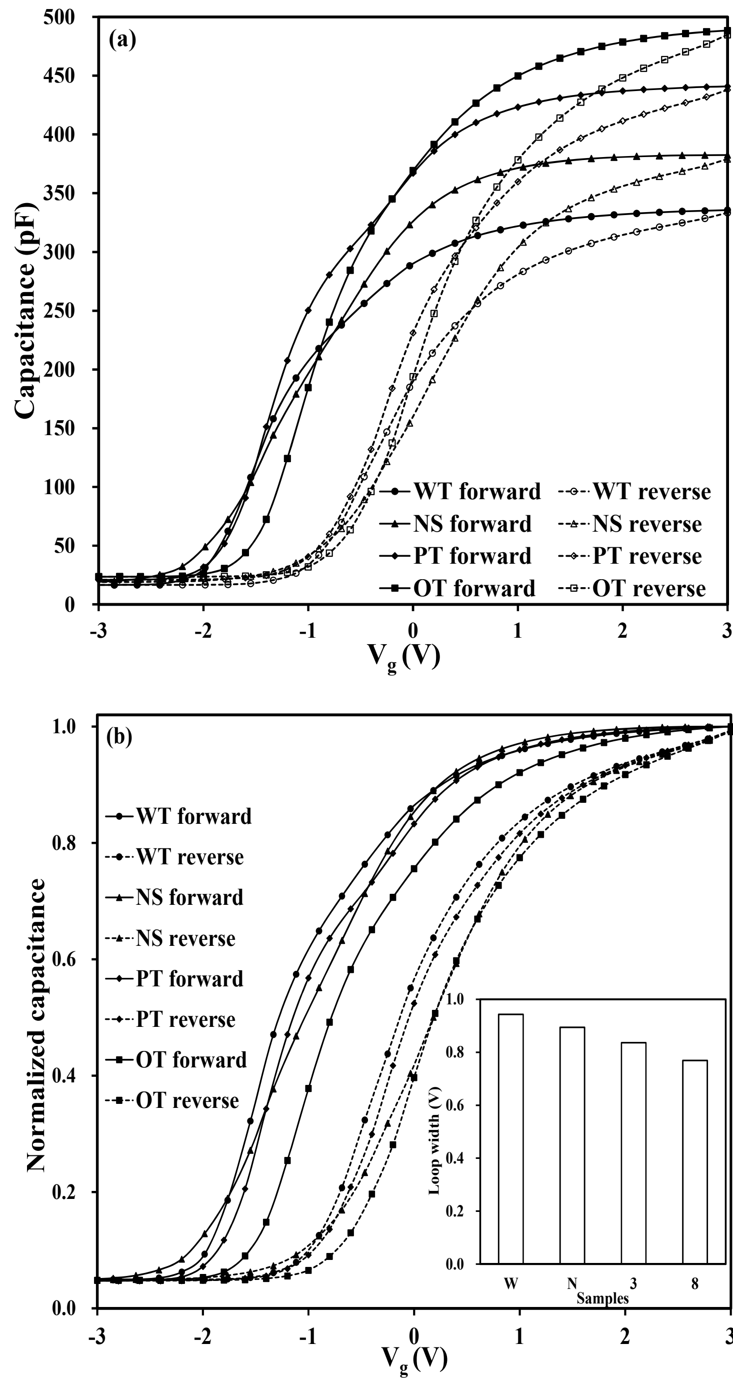

Figure 5.2 (a) The CV characteristics and (b) corresponding normalized CV characteristics extracted from the four samples.

This reduction in leakage current is due to the passivation of the germanium surface, which suppresses the formation of $HfGeO_x$ [13-16]. As previous research reports, an increase in leakage current is caused by the formation of defective $HfGeO_x$ at the interface between the HfO_2 and Ge. The leakage current can be reduced if a germanium nitride barrier layer is first introduced, preventing the formation of $HfGeO_x$ [6, 16, 17]. With regard to the slight increase in leakage current density for the PR and OT samples compared with that of the NS sample, it is due to the difference in monolayer coverage of the three passivation techniques [18-20]. However, the leakage current densities extracted from all four samples remain at relatively low levels with gate leakage current densities smaller than 1×10^{-6} A/cm^2 at $V_g - V_{fb}$=1 V [21]. Usually, the maximum tolerable gate leakage density is 1 A/cm^2 at a supply voltage of 1 V with an EOT of 0.9 nm for HfO_2 [22].

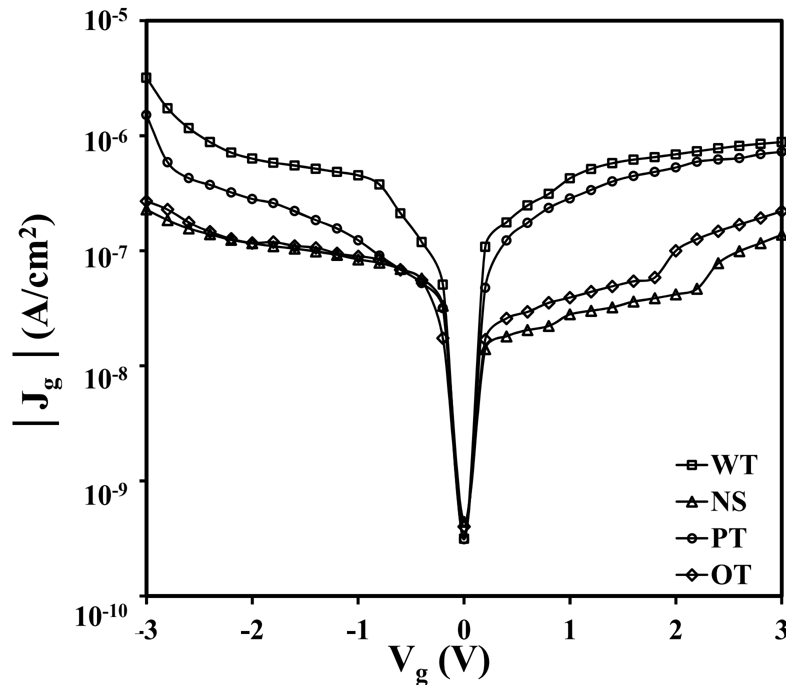

Figure 5.3 Gate leakage current density (J_g) versus gate voltage (V_g) of the four samples.

Besides the reduction in leakage current obtained from the surface passivation methods, FG annealing also had an effect on the electrical properties and was applicable to all samples. The CV characteristics and normalized CV curves of the NS sample for various frequencies (50 kHz-1 MHz) before and after FG annealing are shown in Figure 5.4. (other samples display similar behavior and the results are shown in Figure A.2 to Figure A.4 of the Appendix) Firstly, a positive shift of the CV traces after FG annealing has been observed. This implies a decrease in positive charges or oxygen vacancies resulting from FG annealing. In addition, it can clearly be seen that the as-deposited samples have larger CV stretch-out when compared with the annealed samples resulting from more interface states, which respond to low measurement frequencies. Also, a noticeable shoulder appears in the CV curves at lower measurement frequencies. This is also convincing evidence for a large number of interface states. It is likely that PMA in a FG environment reduces the number of traps based on comparisons of the CV characteristics for as-deposited samples and the FG-annealed ones [23-25]. In addition, there is a negative shift in the CV curves with a decrease in measurement frequency for both as-deposited and FG-annealed samples This is related to the donor-like traps near/at the interface [25].

Apart from the effect of FG annealing on the interface quality, an impact on the electrical characteristics was also observed when a long-time bias stress voltage was applied. Figure 5.5 (a) to (d) illustrate the shift in CV characteristics with a stress time of 21,000 seconds (either negative or positive stress) for samples with different treatments (WT, NS, PT and OT respectively). The shift in the CV curves (ΔV_g) is

measured at the point at which the capacitance reaches 50% of its maximum value, as shown in Figure 5.5 (e) and the changes of total charges, ΔN_{ot}, after different stress times are summarized in Figure 5.5 (f).

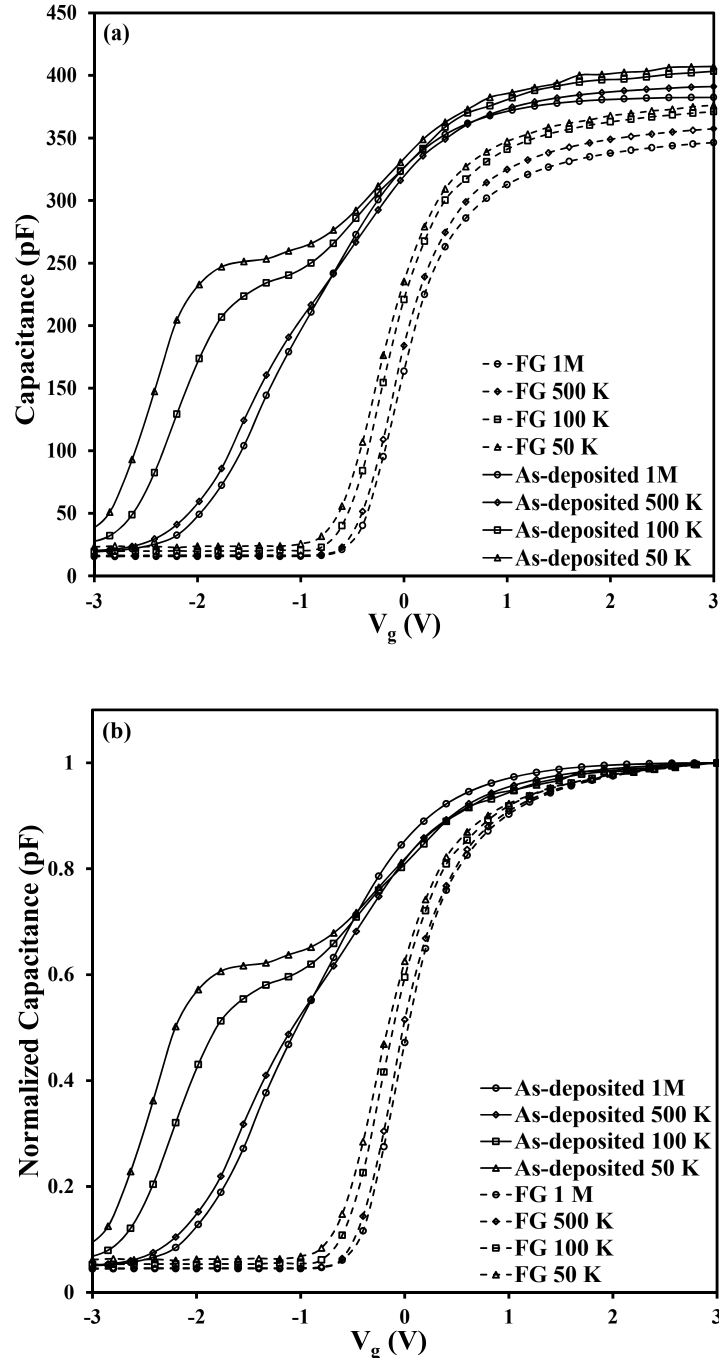

Figure 5.4 (a) The CV characteristics and (b) normalized ones of the sample with $(NH_4)_2S$ pretreatment before and after FG annealing.

The changes in the total charge are obtained by $\Delta N_{ot} = -C_{ox} \cdot (\Delta V_g)/q$. Similar to the results reported in previously published research, the ΔN_{ot} for the as-deposited samples shown in Figure 5.5 (f) increases with the stress time [26]. The change trend of ΔN_{ot} is related to the characteristic trapping time of carriers and the corresponding effective energy depth of the trapping sites. The variation of ΔN_{ot} under positive (or negative) gate bias is indicative of charge trapping in the gate insulator. In addition, with the increase of stress time, a CV slope degradation becomes noticeable. This can be attributed to the creation of field induced interface states [27]. In particular, for the sulfur passivated samples, the H^+ ions drift to the interface from the oxide under the applied electric field caused by the positive bias and the de-passivation of passivated dangling bonds by -HS occurs via the following reaction. A schematic diagram of this is shown in Figure 5.6 [28, 29].

$$\text{Ge-HS} + H^+ \rightarrow Ge^{2+} + H_2S \qquad (5.1)$$

Therefore, the increase of ΔN_{ot} is probably caused by an increase in oxide trap, interface state and border trap densities as reported by other works [30, 31]. With regard to the larger change of ΔN_{ot} for the passivated samples compared with the control sample, it is related to the band-tail states, which act as transport states for the emitted lower energy trapped state charge [27] and the reaction described by Formula (5.1). In addition, the stronger Ge-O bond compared with the Ge-HS (or Ge-S($C_nH_{2n+}1$)) bond is also a factor leading to the larger ΔN_{ot} [25]. Fortunately, after FG annealing, it has been observed that there is a significant reduction of the ΔN_{ot} for the FG sample as shown in Figure 5.7 (f), further indicating a higher interface quality and fewer traps in

the oxides achieved through PMA [25, 26].

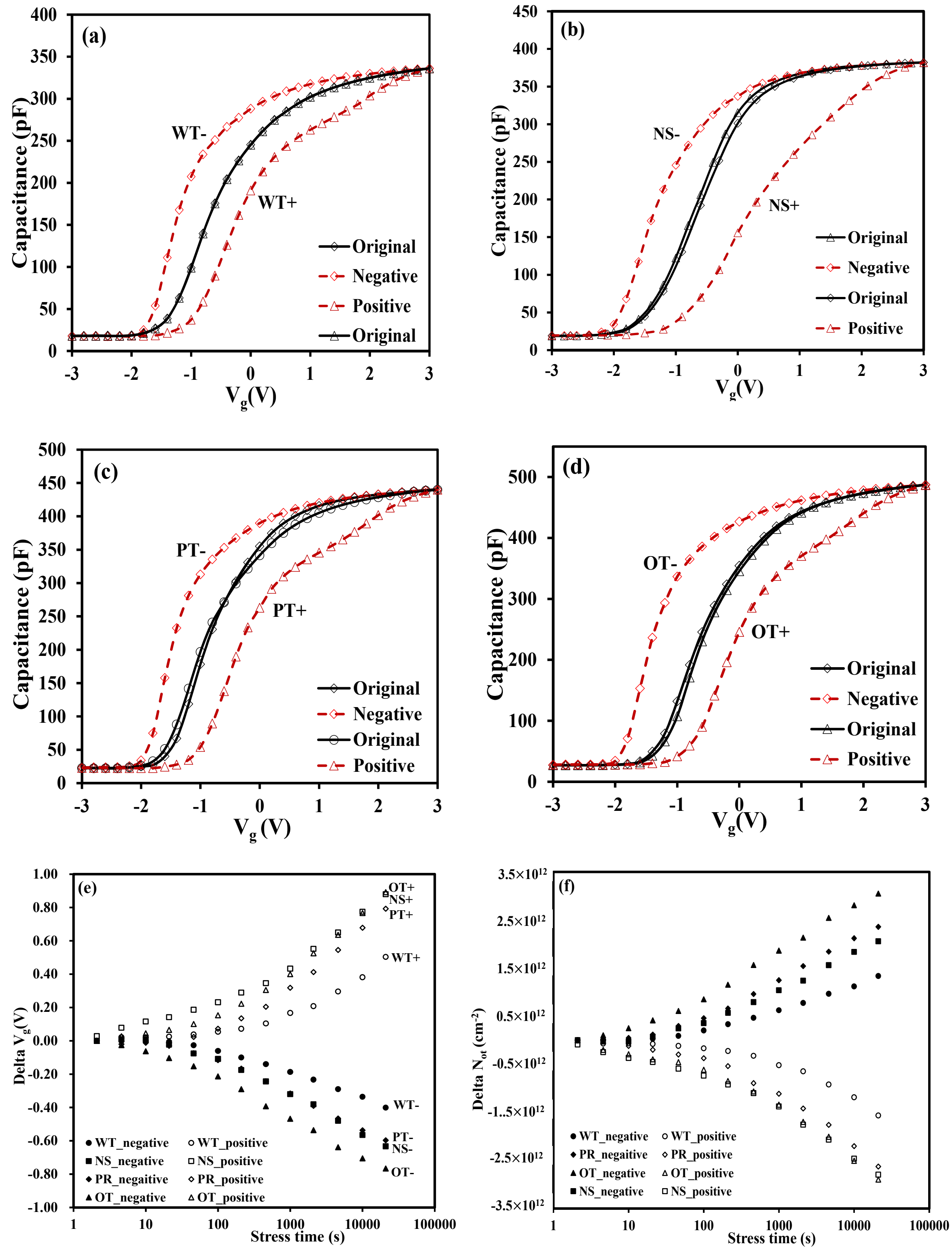

Figure 5.5. The forward CV curves under positive and negative stress of 21,000 seconds for as-deposited (a) WT (b) NS, (c) PT and (d) OT samples. The variation of gate voltage shift and the corresponding variation of N_{ot} for the samples with stress time are illustrated in (e) and (f), respectively.

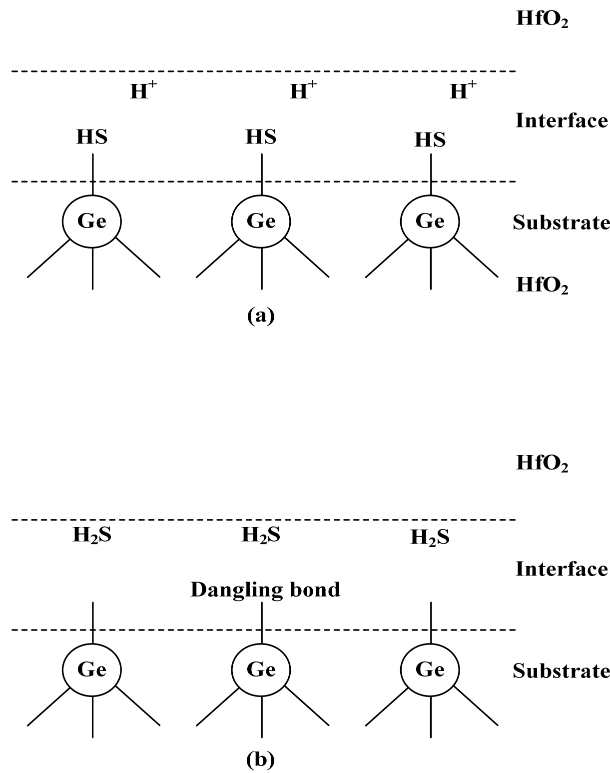

Figure 5.6 Schematic diagram of the depassivation process: (a) The protons (H^+ ions) move to the interface under the electric field; (b) the H^+ ions react with the -HS groups to form H_2S.

Figure 5.8 (a) to (d) show CV traces of the four samples before and after FG annealing and the corresponding loop widths are indicated in Figure 5.8 (e). From the loop widths summarized in Figure 5.8 (e), it is clear that the loop widths of the as-deposited samples are about two times those of the FG annealed samples (0.5 V) for all samples. These results indicate that the traps can be reduced by FG treatment. In addition, the positive shift of the CV curves after FG annealing can be attributed to a decrease in fixed positive charges as in the discussion of the results of Figure 5.4. It indicates that the appropriate PMA process of the thin films makes it possible to recover the negative shift of the CV curves without increasing loop width as reported in other published work [32].

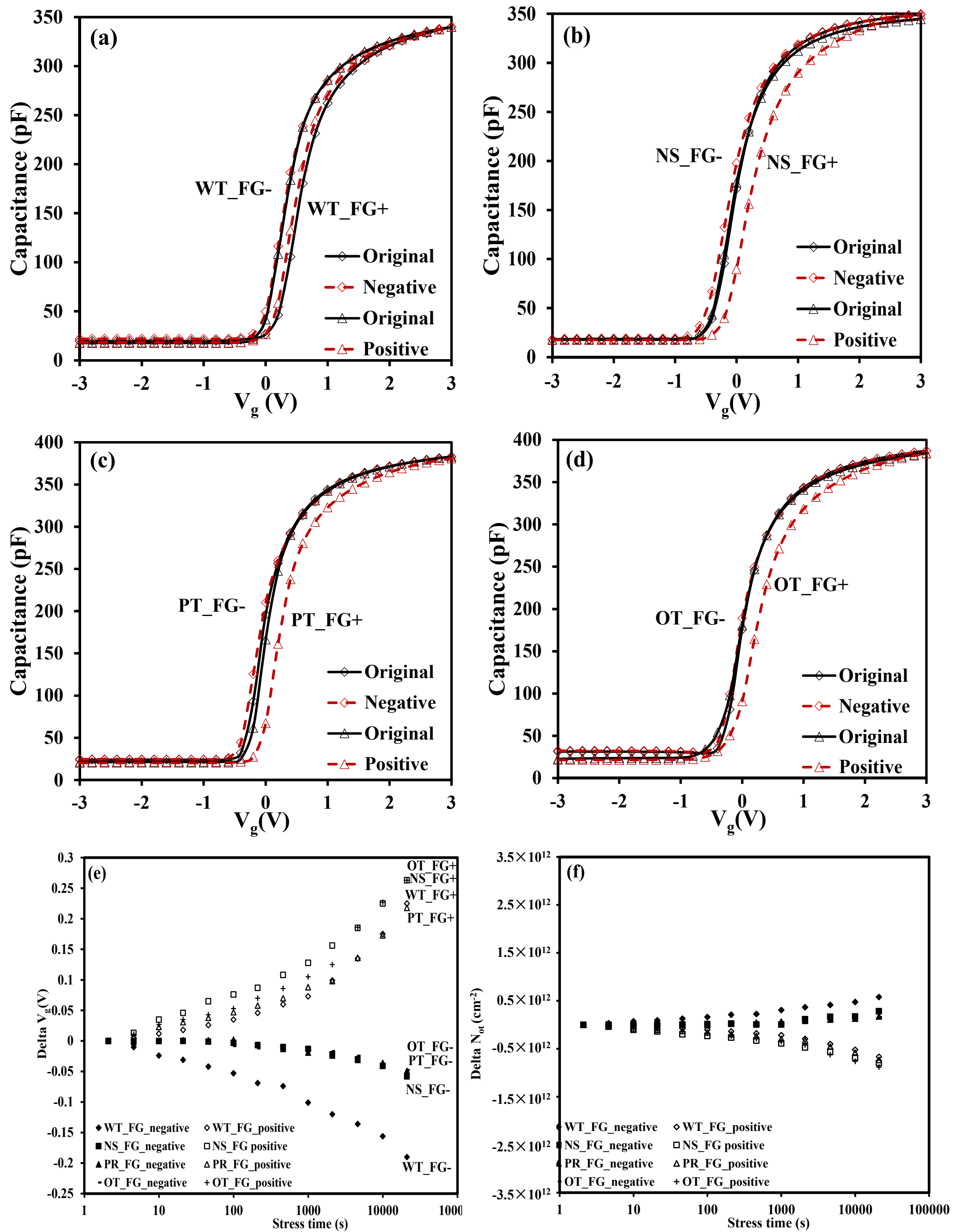

Figure 5.7 Forward CV curves under positive and negative stress of 21,000 seconds for (a) WT_FG, (b) NS_FG, (c) PT_FG and (d) OT_FG samples, which underwent FG annealing. The gate voltage shift and corresponding change of N_{ot} for the samples with stress time are given in (e) and (f), respectively.

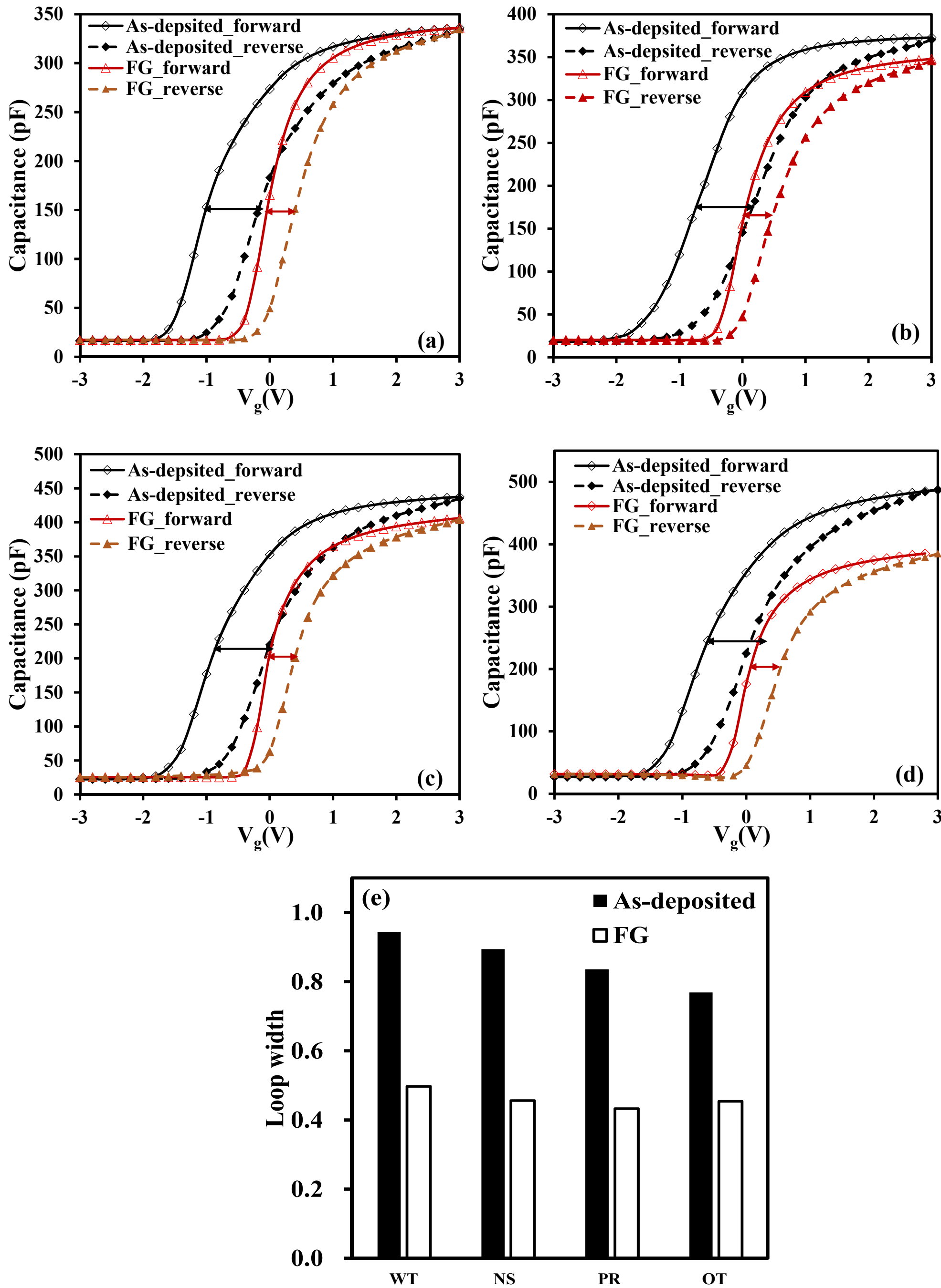

Figure 5.8. Comparison of the loop width for (a) WT, (b) NS, (c) PT and (d) OT samples between the as-deposited and FG-annealed ones, with (e) summarizing the change of the loop width.

Besides the reduction of the loop widths of these devices, the variation of the loop width (delta loop width in Figure 5.9) is also reduced after FG treatment. Since the as-deposited WT sample has a noticeable delta loop width under both negative and

positive stress conditions, the CV curves for the as-deposited WT sample after 21,000 seconds positive and negative stresses, are shown in Figure 5.9 (a) and (c), respectively. The CV characteristics of other samples have the similar behavior and they are not included here. From observation of the CV curves, it is clear that a positive shift of the CV traces (both forward and reverse) is obtained after a positive stress while a negative shift is obtained when a negative stress is applied. This shift is due to the trapped charges under long-time stress and this has already been discussed in reference to Figure 5.5 and Figure 5.7. In addition, an increase in loop width is observed for the samples after stress as indicated in Figure 5.9 (a) and (c).

The variations in loop width and delta loop width, for different stress time are summarized in Figure 5.9 (b) and (d). Obviously, there is an increase in delta loop width of around 0.15 V under either positive or negative stress bias for the as-deposited samples. However, for the samples after FG annealing, there is almost negligible delta loop width if the accuracy of the system is taken into account. This improvement is due to a reduction in interface traps and decreased creation of stress induced interface states after FG annealing. These results can be inferred from the negligible slope degradation of the CV curves extracted from the FG-annealed samples [27, 33].

Figure 5.10 shows the leakage current densities for all of the FG annealed samples, which are around one order of magnitude larger than those extracted from the as-deposited ones in Figure 5.3. However, the leakage current still remains relatively low [34-36]. This increase in leakage current density is caused by the diffusion of Ge atoms into the gate oxides after annealing [17, 37]. An excess of Ge in the high-*k* layer

is likely to quickly result in poor electrical performance [17]. Subsequently, the excessive Ge diffusion into the gate dielectrics causes defects in the HfO_2 thin film itself.

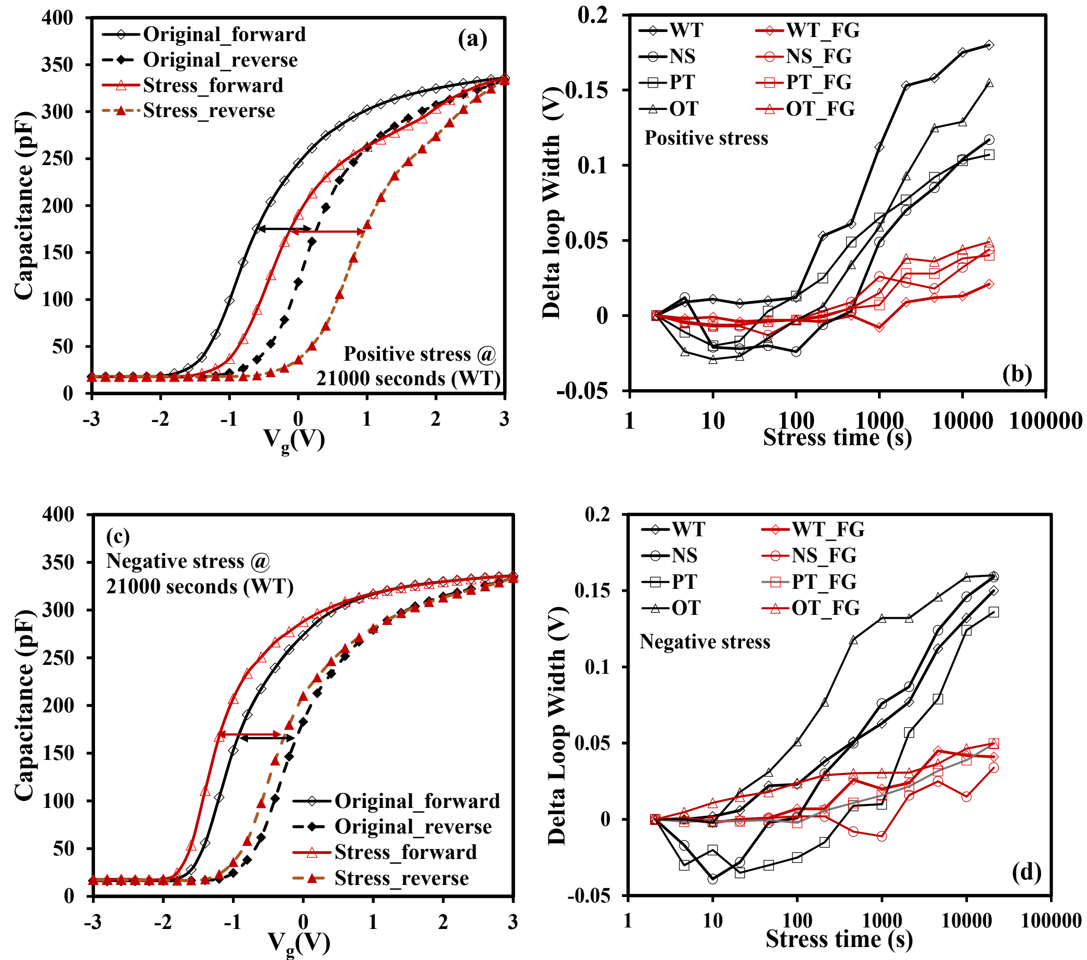

Figure 5.9 Comparison of the loop width between the as-deposited and FG-annealed samples under positive (negative) stress. Subset (a) and (c) representatively show CV traces of the WT samples to indicate the change of the loop width under positive and negative stress for 21,000 seconds, respectively. The change of the loop widths under different stress time are summarized in (b) with positive stress and in (d) with negative stress for both the as-deposited and FG-annealed samples.

This will contribute to leakage paths and thus lead to the observed increase in leakage current [38]. The increase in leakage current is related with the annealing process regardless of the annealing environment. Interestingly, the control sample has the

smallest leakage current after FG annealing. It is speculated that it is related to a more severe degradation of the HfO_2 thin films caused by the monolayer or sulfur (the passivation layer) diffusing into the gate oxides during annealing [39]. In order to confirm this speculation, deep analysis is required in future work.

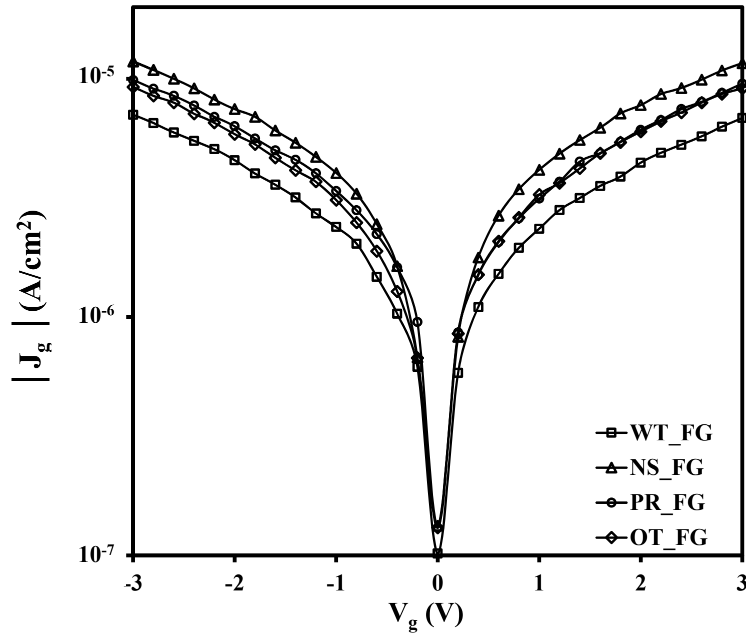

Figure 5.10 Gate leakage current density (J_g) versus gate voltage (V_g) of the four samples after FG annealing.

5.2 Effect of TiN Cap Layer on the Performance of Ge MOS capacitors

In addition to the chemical treatment of the Ge substrates, another method to improve device performance is to deposit a cap layer on the dielectric. This method has been proven to affect the electrical properties of MOS devices significantly [40, 41]. The fabrication process of the samples has been presented in Section 2.1. Compared with the Si cap layer, no additional process, such as ex-situ plasma enhanced chemical vapor deposition (PECVD), is required for the TiN cap layer technique. Therefore, the samples can be fabricated with fewer steps. Figure 5.11 and Figure 5.12 show the

multi-frequency CV characteristics of the samples with and without TiN cap layers, respectively. From a comparison of the CV characteristics, firstly, a more significant frequency dispersion is observed for the sample with the cap layer. In order to illustrate the frequency dispersion clearly, the capacitance-frequency (C-f) relationships for the two samples (with and without a TiN cap layer) are presented in Figure 5.13. The capacitance is normalized by its maximum capacitance at a frequency of 1 kHz. Since the dielectric layers were deposited under exactly the same conditions, it is inferred that the frequency dispersion is caused by extrinsic factors. The parasitic effect of the series resistance caused by the TiN layer (including the resistance due to the interface) is the main reason for the resulting frequency dispersion.

For the device used in this experiment, it has a large resistance (>1 MΩ), so the parallel model of the device is employed for analysis and is presented in Figure 5.14. With regards to the sample with the cap layer, there is one more pair of R_c and C_c (including the effect caused by the interface) connected in parallel due to the TiN cap layer in comparison to the control sample (without the TiN cap layer). According to the mathematical model for the parasitic effect, the extra R_c and C_c will lead to significantly greater frequency dispersion [42-44].

Although significant frequency dispersion is observed for the sample with the TiN cap layer, a dramatic increase in capacitance, or dielectric constant, is also obtained. From observation of Figure 5.15 (a), a larger capacitance is obtained by depositing a TiN cap layer on the high-*k* dielectric thin film. Since the two samples have the same dielectric thickness, around 12.9 nm, before the deposition of the metal gate or cap layer,

it can be inferred that the cap layer has a significant impact on the dielectric constants of the samples.

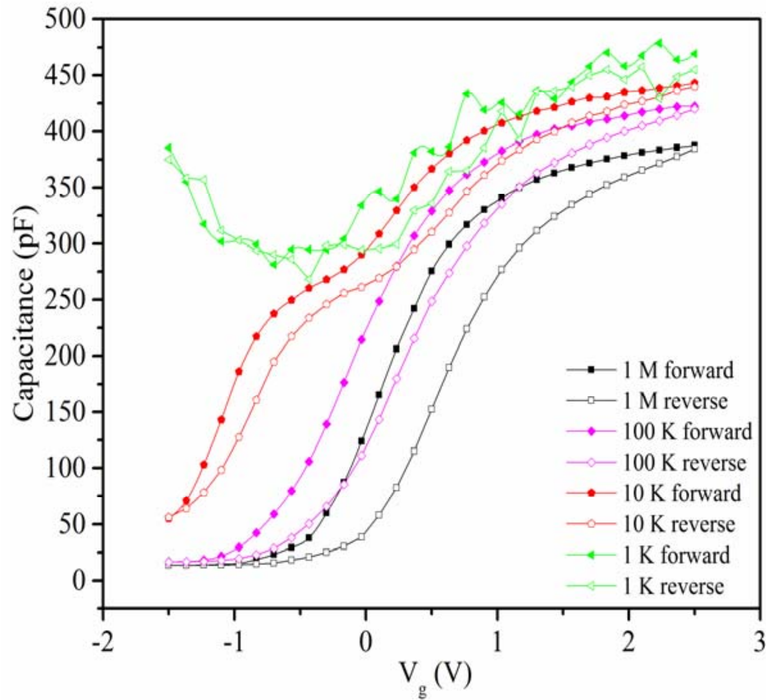

Figure 5.11 The CV characteristics of the sample without TiN cap layer.

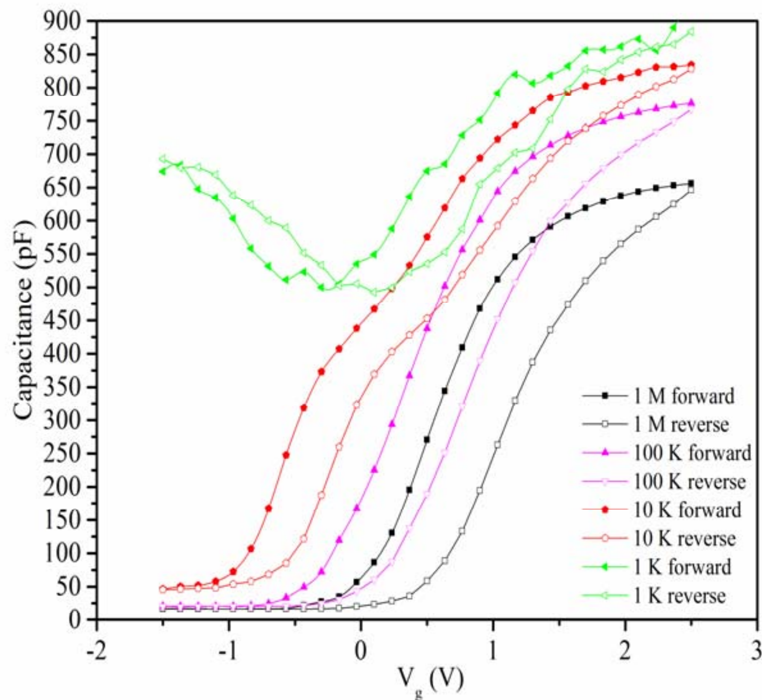

Figure 5.12 The CV characteristics of the sample with TiN cap layer.

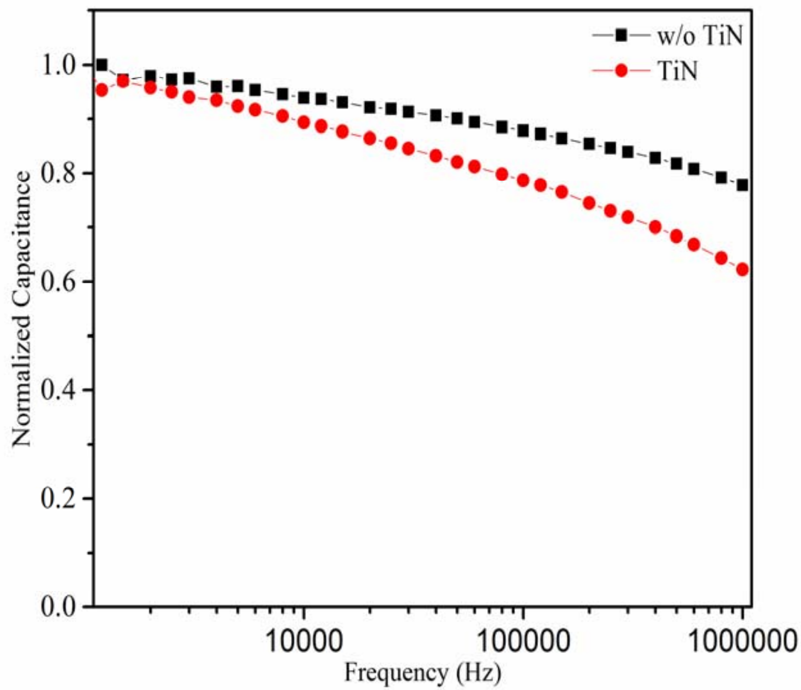

Figure 5.13 The C-f relationship for the samples with and without TiN cap layer.

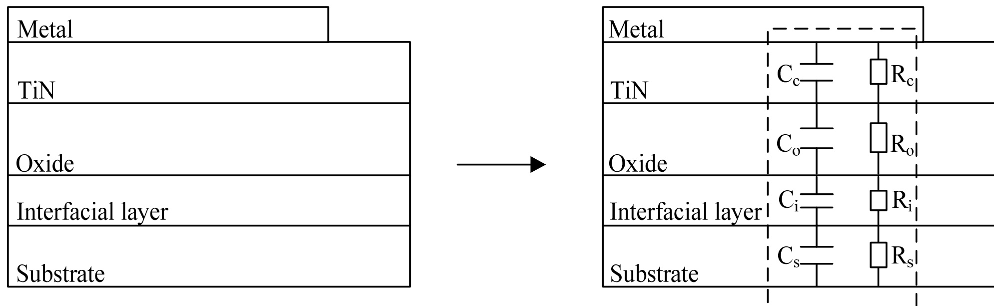

Figure 5.14 Schematic model of the parasitic effect for the sample with TiN cap layer.

For the sample without cap layer, a lower dielectric constant, around 8.2, is obtained. However, for the same dielectric oxide capped with TiN layer, a higher dielectric constant of around 13.5 is obtained, which is close to that deposited on the Si substrate with the dielectric constant of around 15. This result implies that a deterioration of the dielectric constant occurs if aluminum electrodes are directly used as the contact gates for Ge MOS devices.

A model related to the desorption of GeO shown in Figure 5.16 provides an explanation for this phenomenon [45]. When the Al electrodes are deposited on the oxide dielectrics by E-beam evaporation, volatile GeO is formed as described by Formula (5.2). The GeO will then diffuse across the thin dielectric layer and react with the aluminum to form a thin layer of aluminum oxide.

$$HfO_2 + Ge \rightarrow GeO + HfO_x \quad (5.2)$$

However, when a TiN cap layer is deposited on the top of the dielectric thin film prior to the aluminum metal gate, it is considered that the chemical potential of GeO inside the thin film will increase. Therefore, the reaction rate to form GeO is expected to be reduced, as a result of blocking the continuous desorption of GeO form the gate oxide/Ge interface [45]. In other word, the reaction rate of HfO_2 and Ge at the interface as described by Formula (5.2) is reduced due to the equilibrium and the process is schematically shown in Figure 5.16. This is a key mechanism in suppressing the GeO desorption from the gate oxide/Ge interface by the cap layer. Therefore, less oxidation of the Al metal gate occurs and the dielectric constant of the capacitor is similar to that obtained on Si substrate. This conclusion is useful for the design and fabrication of Ge devices. In addition, from the normalized CV characteristics in Figure 5.15 (b), a positive shift in the CV traces detected from the sample capped with a TiN layer is observed compared to that without a TiN cap layer. This mainly results from the higher work function of TiN to that of Al [46, 47].

The gate leakage current densities of the Ge MOS capacitors are presented in Figure 5.17. Relatively low leakage current densities ranging from 10^{-7} to 10^{-6} A/cm^2

are observed for all samples. However, in the inversion region (negative bias for a PMOS with n-type substrate), the sample without the TiN cap layer has a larger leakage current density than that with the TiN cap layer. This is due to a larger trap-assisted tunneling current caused by the traps, which are formed during the GeO desorption for the sample without the cap layer [17, 45, 48].

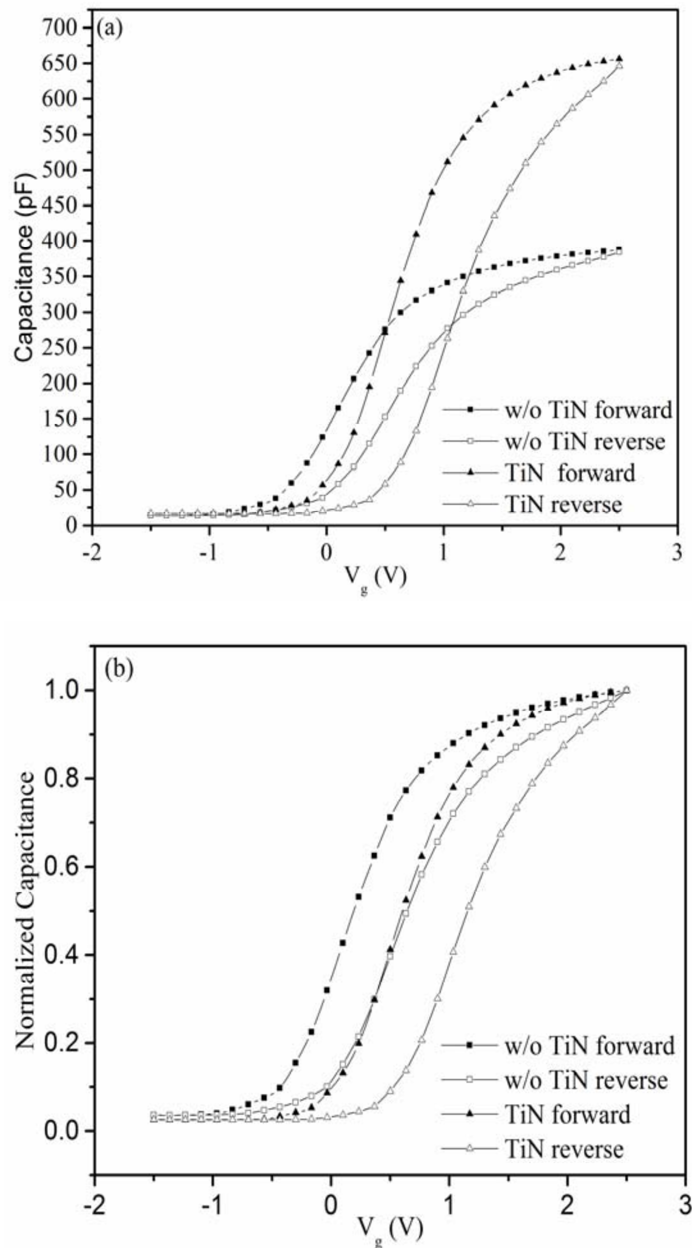

Figure 5.15 (a) Comparison of the high frequency CV characteristics (1 MHz) detected from the samples with and without TiN cap layer and (b) the normalized CV characteristics.

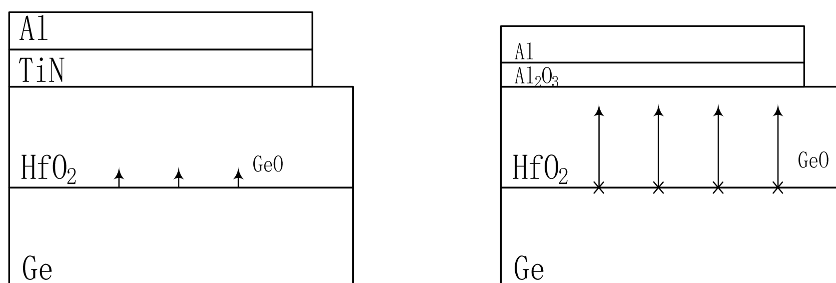

Figure 5.16 Schematic model for the mechanism of cap layer to suppress GeO desorption. (a) TiN works as the cap layer to suppress the GeO desorption. (b) On the other hand, GeO diffuses out to the metal gate and reacted with Al.

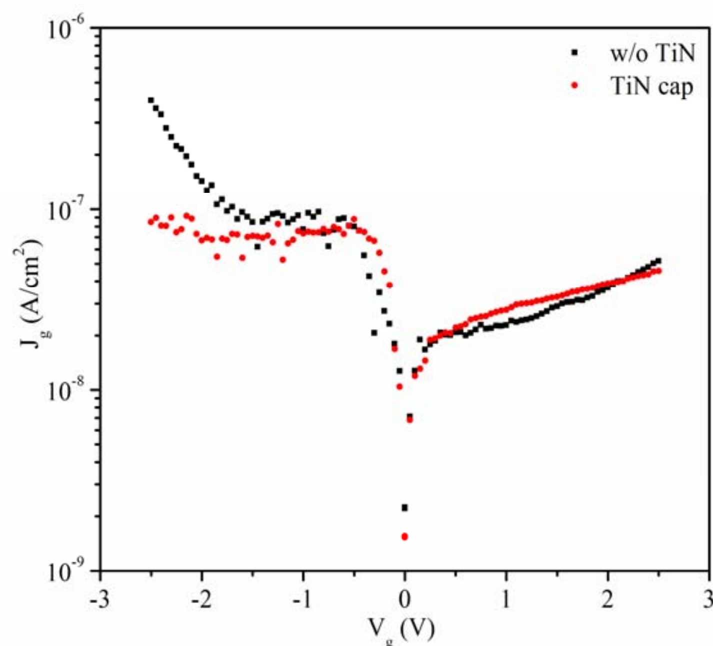

Figure 5.17 Gate leakage current density (J_g) versus gate voltage (V_g) for samples with and without TiN cap layer.

5.3 Summary

In this chapter, propanethiol solution (0.1 mol/L) in 2-propanol, octanethiol solution (0.1 mol/L) in 2-propanol and 20% $(NH_4)_2S$ solution in DI water were used to passivate n-type germanium wafers. HfO_2 thin films were used as the dielectric layers in MOS capacitors. The results show that all of the passivated samples have larger dielectric constants and lower leakage current densities when compared with the control sample.

In particular, the sample passivated by octanethiol has the largest dielectric constant. The lowest leakage current density is observed for the sample passivated by the $(NH_4)_2S$ solution followed by the one passivated by octanethiol. Also, the interface quality is improved and a smaller change in loop width under long-time stresses is obtained when the samples are annealed in a FG environment. In addition, the cap layer technique is able to suppress the formation of volatile GeO. As a result, the dielectric constant of the capacitor increases from 8.2 to 13.5 and a lower leakage current density for a negatively applied voltage is obtained. Therefore, the passivation of the substrates by octanethiol or $(NH_4)_2S$ solution followed by the cap layer technique and FG annealing are useful techniques in the fabrication Ge MOS devices.

5.4 References

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Chapter 6: Conclusions and Future Works

6.1 Conclusions

In this research, the structure of a MOS capacitor (shown in Figure 1.2) was employed, since it simplifies the manufacturing process, whilst providing all of the same components which can be tested for traps in a similar manner to the MOS transistor. All of the results and discussion in this thesis are therefore based on a MOS capacitor structure. In the fabrication of the MOS capacitors, ALD was employed to deposit high-*k* dielectrics and an E-beam evaporator was used to form the metal gates.

To investigate oxide traps in $LaZrO_X$ dielectrics accurately and comprehensively, $LaZrO_X$ oxides were deposited on n-type silicon wafers and used as the gate dielectrics of MOS capacitors. The CV characteristics of the MOS capacitors with these dielectric oxides were then extracted using a conventional CV measurement system and a pulse CV system developed as part of this work. All of the discussions were presented in Section 3.2. It was found that more traps are sensed when using the pulse CV characterization method in comparison to the conventional technique. This is due to the fact that the charge trapping/de-trapping in the stack is highly dependent on the test time, with longer test times leading to smaller trap densities detected. This is confirmed by increasing the edge time used in the pulse CV system. When the test time is long enough, the result obtained from the pulse CV technique is the same as that from the conventional method. In addition, the pulse width and V_{PP} also affect the trap density measured. Additionally, the longer the pulse width, the larger the electron fluency

supplying the charge into the traps in the oxide and this in turn leads to greater amounts of trapped charges. As the voltage level increases, higher trap densities are detected since the traps in the deeper/higher energy levels in the oxide are detected.

There are two distinctions in the CV curves measured by the pulse CV technique when compared with those measured by the conventional methods, as described in Section 3.3. To explain the distinct behaviors in the pulse CV curves, models related to interface dipoles and imposed currents, due to the pn junction formed by the substrate and inversion layer, were confirmed. Firstly, an anomalous CV behavior was observed when the pulse CV technique was applied to MOS capacitors made with either ZrO_2 or HfO_2 as the dielectric on an n-type silicon substrate, especially for devices with non-stoichiometric oxides native to the substrate. Opposite relative positions of forward and reverse traces were observed for the CV curves extracted from the conventional method and the pulse CV technique. The reverse traces of the conventional CV curves were positively shifted with reference to the forward trace, while the shift became negative for the pulse CV curves. The interface dipoles formed at the high-k/SiO_x interface are believed to be responsible for this unusual CV behavior. In addition, the interface dipoles are highly dependent on the deposition temperature and annealing conditions used. The effect of interface dipoles is suppressed and the relative positions of CV characteristics measured by the pulse technique are identical to those obtained by the conventional method, when the samples are annealed in either an FG or nitrogen environment at 350°C for 30 minutes.

Apart from the unusual CV behavior, there was a hump in the weak inversion region

of the forward CV trace measured by the pulse technique. This hump is caused by the imposed current due to the pn junction formed by the substrate and inversion layer. It is related to the rising edge of the applied pulse voltage and response time of the carriers. The hump is observed when the rise time is short enough that the pn junction still exists when the voltage becomes positively biased (sweeping from negative to positive for an n-type substrate).

To analyze the interface quality and chemical structure at the high-*k*/Ge interface and their relationship to the CV/IV characteristics. $Ti_xHf_{-x}O_2$ thin films, with a titanium content of x=0, 0.25, 0.9, and 1 were deposited on p-type germanium wafers. XPS was used to analyze the interface quality and chemical structure. Discussions regarding these investigations were given in Section 4.1. The results indicate that the HfO_2 deteriorates the interface quality, leading to an increased leakage current.

Surface roughness was analyzed with an AFM, and all the samples exhibited relatively good surface morphology with RMS roughnesses of 0.202 nm, 0.425 nm, 0.431 nm, and 0.325 nm for HfO_2, $Ti_{0.25}Hf_{0.75}O_2$, $Ti_{0.9}Hf_{0.1}O_2$, and TiO_2, respectively. XRD analysis shows that all samples are amorphous under these deposition conditions.

From conventional CV traces, it is found that there is almost no hysteresis between the forward and reverse CV curves, suggesting low trap densities. However, relatively large leakage current densities (>10^{-3} A/cm^2) are obtained for these samples. The large leakage current density is partially attributed to the deterioration of the interface between Ge and $Ti_xHf_{1-x}O_2$ caused by the oxidation source supplied by the HfO_2. The energy band diagrams also provide insight into the cause of the observed leakage

current.

To investigate the effect of in-situ deposited ZnO passivation layers of germanium wafers on the CV/IV characteristics of the MOS capacitors in Section 4.2. In-situ ZnO interfacial layers were deposited before the deposition of $Ti_{0.1}Hf_{0.9}O_2$ thin films on the n-type germanium wafers using ALD. PDA in nitrogen for 30 seconds at 450 °C and 550 °C, respectively, was carried out. A larger distortion of the as-deposited sample with an in-situ ZnO interfacial layer is observed. After the PDA, smooth CV traces are obtained, however, there is an increase in frequency dispersion. The leakage current density is increased by two orders of magnitude. Therefore, ZnO interfacial layers cannot effectively passivate germanium wafers, although an improvement is obtained using ZnO passivation layers on GaAs wafers. The analysis for this difference can be further investigated in future work.

To investigate the effect of different wet chemical treatments on germanium wafers and the impact of a TiN cap layer on the electrical properties of Ge MOS capacitors, two experiments were carried out in Chapter 5.

Propanethiol solution (0.1 mol/L) in 2-propanol, octanethiol solution (0.1 mol/L) in 2-propanol, and 20% $(NH_4)_2S$ solution in DI water were each used to passivate n-type germanium wafers, then HfO_2 thin films were deposited on each of the passivated wafers by ALD. The morphology and surface roughness of the thin films were investigated by XRD and AFM, respectively. It was found that the morphology is not affected and smaller surface roughness is obtained after the chemical treatment. Also,

lower leakage current densities are observed in the passivated samples when compared with the control sample. This is due to the suppression of the formation of defective $HfGeO_x$. In addition, a high interface quality and smaller change of delta loop width under long-time stresses are obtained when the samples are annealed in an FG environment. This improvement is attributed to a reduction in interface traps and reduced creation of stress-induced interface states after FG annealing.

A TiN cap layer was deposited on the high-*k* gate oxide (HfO_2) prior to metal contacts. With regard to the cap layer technique, it has been proven that it has a significant influence on the electrical properties of MOS devices. In this research, significant frequency dispersion was observed for the sample with a TiN cap layer. This frequency dispersion is mainly caused by extrinsic factors. However, a dramatic increase in the capacitance, and hence dielectric constant, also occurred. These results imply that a deterioration of the dielectric constant occurs if the aluminum electrodes are directly used as the contact gates for Ge substrate devices. A model related to the desorption of GeO from the high-*k*/Ge interface and diffusion across the dielectric thin films is employed to explain this phenomenon. For the device with a TiN cap layer, it is considered that the TiN cap layer increases the chemical potential of the GeO inside the thin film. Therefore, the interface reaction rate to form GeO is reduced due to the equilibrium of the reaction, as a result of blocking the continuous desorption of GeO. In addition, a reduction of the leakage current density is obtained when the sample is capped with a TiN layer. This is due to a larger trap-assisted tunneling current caused by the traps, which are formed during the diffusion of GeO across the thin films if the

samples do not have cap layers.

Based upon the above analysis, it can be concluded that several steps are required to fabricate a MOS device with the best performance in this thesis. Firstly, the Ge substrates should be passivated by either octanethiol solution or $(NH_4)_2S$ solution, dependent on the balance between the leakage current and dielectric constant. Following the passivations, a TiN cap layer should be deposited on the high-*k* dielectrics prior to the deposition of the Al metal gate.

6.2 Future Work

Although the research outcomes related to the aims and objectives listed in Section 1.3 have been accomplished in this thesis, further research is needed to explore the area in greater detail. Firstly, the pulse CV system developed based on use of a function generator, a current amplifier and an oscilloscope can be further updated to characterize the CV traces with a faster pulse. This would allow the traps in the oxides to be probed more accurately. Other interesting phenomena may also be observed with a shorter pulse voltage.

An anomalous CV behavior was observed in the pulse CV characteristics for the MOS capacitor with a relatively thick non-stoichiometric native oxide for the substrate in Section 3.3. However, the thickness of the native oxide was not discussed quantitatively. The effect of the interface dipoles may be related to the thickness of the native oxide between the high-*k* materials and substrates. Thus, a quantitative

relationship can be investigated.

In Section 4.1 the crystal states of the thin films were analyzed using an XRD. The XRD measurements show that all of the thin films are amorphous under these deposition conditions. However, due to the small thicknesses of the dielectric thin films, the sensitivity of the XRD may not be sufficient to detect a limited amount of a crystalline phase if it is present. In future, a TEM or an SAED can be employed to offer more information about the exact morphology of the thin films.

In Section 4.2 it was reported that ZnO interfacial layers cannot effectively passivate germanium substrates despite the improvement seen in GaAs substrates using a ZnO passivation layer. In depth analysis of this difference should also be investigated in future work.

Finally, the smallest leakage current was observed for the control sample when compared with those for the samples that were chemically passivated and annealed in FG in Section 5.1. It is speculated that it is related to more severe degradation of HfO_2 thin films caused by diffusion of the monolayer into the thin films during annealing in this research. However, no direct evidence for this was obtained. Therefore, it can also form part of future research.

Appendix

Figure A.1 shows the CV curves for the as-deposited samples with ZnO interfacial layer. A larger distortion in the CV curves was observed and it is presented in the comparison with the PDA samples in Section 4.2.

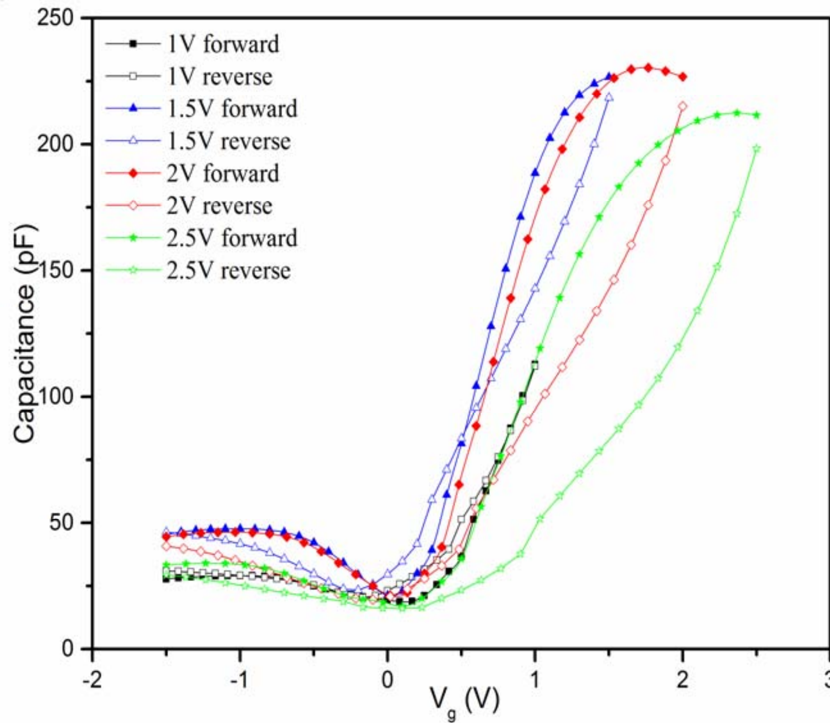

Figure A.1 CV curves for the as-deposited samples with ZnO interfacial layer.

Figure A.2 to Figure A.4 show the CV characteristics the WT, PT and OT samples, respectively, before and after FG annealing. The passivated samples show similar results and these results are not presented in Section 5.1. A positive shift of the CV traces after FG annealing has been observed for all the samples, implying a decrease of positive charges after FG annealing.

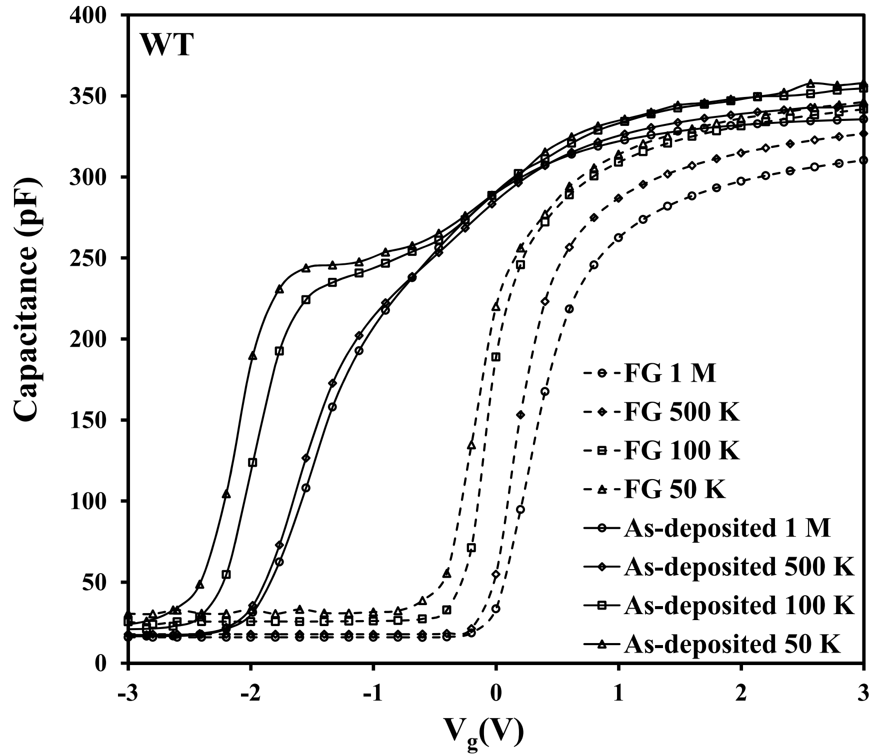

Figure A.2 The CV characteristics of the control sample (WT) before and after FG annealing.

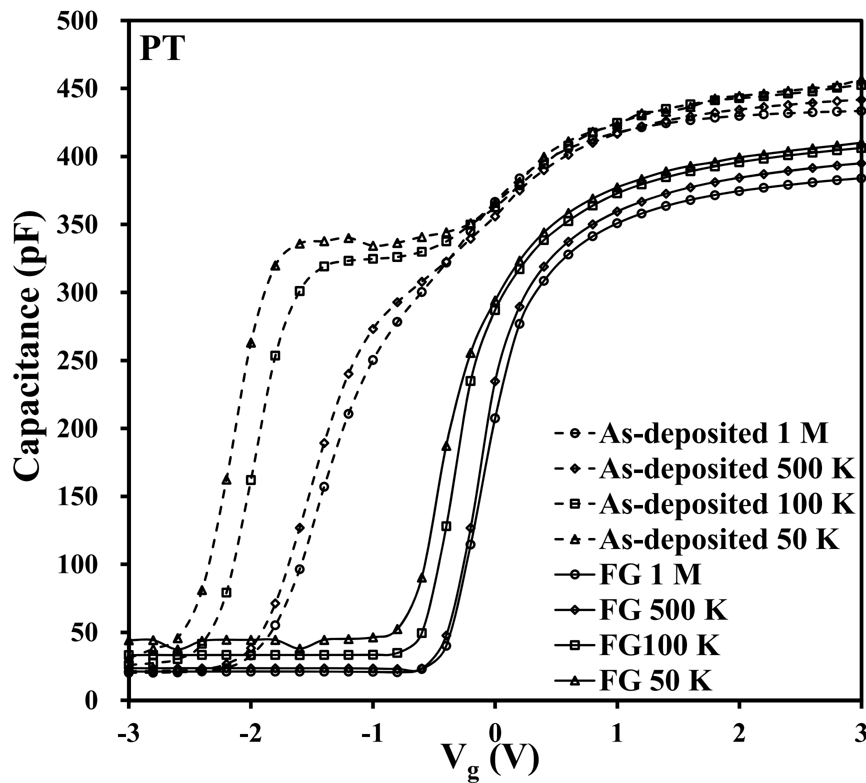

Figure A.3 The CV characteristics sample with PT passivation before and after FG annealing.

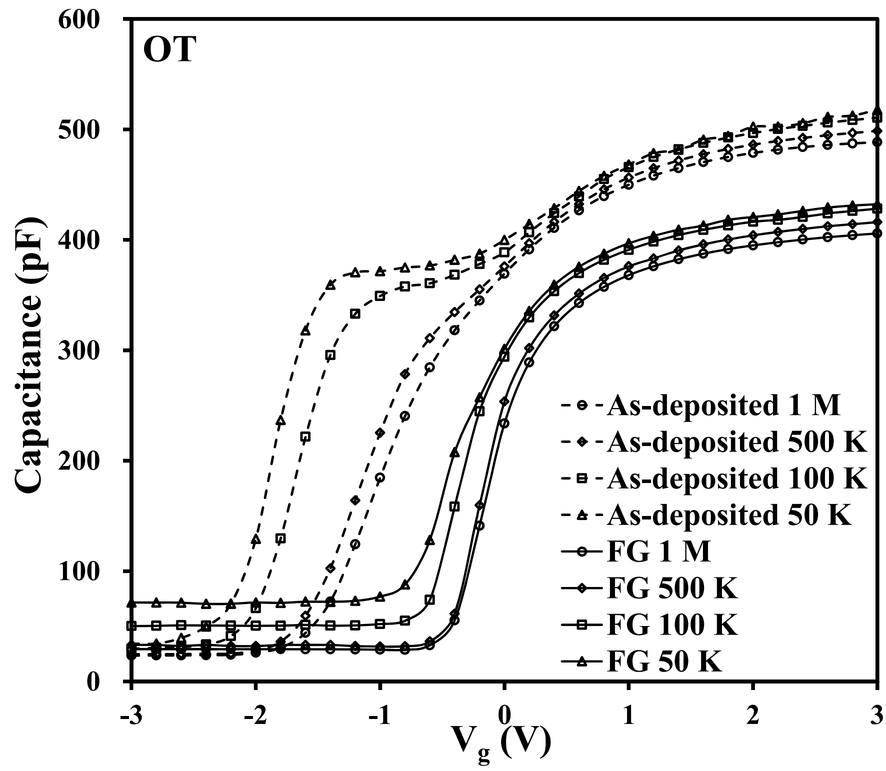

Figure A.4 The CV characteristics of the sample with OT passivation before and after FG annealing.