Device Loss Model of a Fully SiC Based Dual Active Bridge Considering the Effect of Synchronous Rectification and Deadtime

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***Abstract*—It is becoming a great interest to employ SiC based power devices in dual active bridge (DAB) converter as an alternative to conventional Si-IGBT, due to its higher switching frequency potential, smaller switching losses as well as the capability to operate at synchronous rectification (SR) condition. This paper introduces the device loss model of a SiC MOSFET power module based DAB converter considering the effect of synchronous rectification, and the dead-time effect is also discussed. The calculated device loss for both SiC-MOSFET and Si-IGBT are discussed. The results show that the overall device loss is reduced by 40%, where the conduction loss is reduced by 38% because of SR capability of SiC-MOSFET, and the switching loss is reduced by 48% due to the faster transient of SiC-MOSFET during dead-time. On the other hand, the device losses are not even between the primary bridge and the secondary bridge of the DAB converter, and it is more significant for SiC-MOSFET based DAB due to the effect of SR with a maximum of 20%. At last, the dead-time range is given based on the device properties.**

***Index Terms*—SiC MOSFET power module, Dual Active Bridge Converter, Device Loss, Synchronous Rectification, Dead-time.**

I. Introduction

With the increasing demand of on-board micro-grids, such as aerospace, shipboard or electric vehicle, the power converter employed in these applications are required to provide high reliability, high efficiency as well as minimum volume, where dual active bridge (DAB) converters are considered to be one of the options to meet such requirements [1]. The concept of DAB has been proposed for more than two decades [2], Fig 1 shows the basic topology of a DAB converter, which consists of a high-side H-bridge, a high-frequency isolated transformer, a power inductor and a low-side H-bridge. Compared with conventional power transformer, the capability of higher switching frequency of DAB converter, as part of the solid state transformer, reduces the volume of both magnetic components and capacitors. On the other hand, the bi-directional power control ability makes the DAB converter more attractive for on-board micro-grid applications.

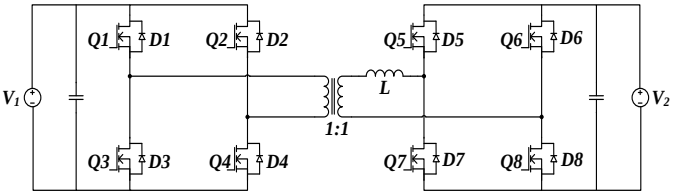

Fig. 1. Dual Active Bridge Converter (DAB) Topology

Fig. 2. Employed SiC MOSFET Power Module

The development of silicon carbide (SiC) devices provides DAB converter the capability to reduce the total converter losses as well as the size of the converter compared with Si-IGBT based counterpart. The impact of SiC technology in DAB converter has been discussed [3] [4]. The overall efficiency of commercialized SiC-MOSFET based DAB converters are measured and discussed by [5] and [6], the experimental results show that a 2-3% efficiency increment can be brought by SiC devices. Moreover, the loss analysis of the SiC-MOSFET based DAB converter are carried out [7]. However, the effect of synchronous rectification of MOSFET as well as the effect of dead-time are not well considered and discussed. This paper will focus on the device properties, including synchronous rectification and device transient performance, to estimate the SiC-MOSFET losses and discuss the impact of device properties in the efficiency of a DAB converter. A fully SiC MOSFET based power module is employed to build the DAB converter, as Fig 2 shows, where the anti-paralleled SiC Schottky diode is included.

This paper will be arranged as following. Section II will first stress the device properties of the employed SiC-MOSFET

and Si-IGBT, and the current model as well as the device conduction loss model considering the effect of synchronous rectification will be given in this section. The modified current model and device conduction loss model including the effect of dead-time will be derived in Section III. Moreover, the transient behavior during dead-time will be analyzed and the switching loss model will be given in this section. Section IV will focus on the dead-time effect, the dead-time range will be given for both SiC-MOSFET based DAB and Si-IGBT based counterpart. The calculated device loss with respect to different dead-time will also be discussed in this section.

II. Dual Active Bridge Current Analysis with the Effect of Synchronous Rectification

Synchronous Rectification (SR) is a generally used technology to reduce the conduction losses based on MOSFET properties. Conventionally, a diode (Schottky diode or body diode of the MOSFET) is used to conduct the reverse current in a converter. However, the P-N junction voltage drop of the diode cannot be neglected. Normally, the voltage drop of Si-based diode is $0.4V$ and $0.8V$ for SiC counterpart, which brings a significant power loss to the whole converter. On the other hand, the significant reverse recovery current of Si-based diode not only increases the total loss of the converter, but also slows down the switching speed during turn-off. The idea of SR is to replace the free-wheeling diode by a MOSFET, or try to make the MOSFET operates under SR condition when conducting reverse current to reduce the conduction losses.

Compared with IGBT devices, MOSFET could achieve synchronous rectification because of its unique structure.An additional P layer exists for IGBT compared with MOSFET, which means an additional P-N junction voltage drop exists during the forward conduction of IGBT. On the other hand, the additional P-N junction blocks the reverse current and an anti-paralleled diode is often used to conduct reverse current of the IGBT devices. On the contrary, a MOSFET can be used to conduct reverse current. When the gate (G) of the MOSFET is forward biased, the P layer will temporarily reverse to N type, and creates a current path between drain (D) and source (S), which enables the current flows from both directions. When the gate (G) is reverse biased, a parasitic P-N junction exists in the MOSFET, known as body diode. However, the body diode is not often used due to its bad performance (normally, the voltage drop of the body diode is larger than $2V$), and an additional anti-paralleled diode is used.

The reverse current path has two conditions when the gate of the MOSFET is forward biased. The reverse current flows only in the channel of the MOSFET under light load (low current), and it will be shared by the MOSFET channel and anti-paralleled diode when the current exceeds a certain level, as shown in Fig.3. The current sharing between the MOSFET channel and anti-paralleled diode can be calculated using (1).

$$\begin{cases} V_{D-drop} + I_D R_{D-on} = V_{drop} \\ I_Q R_{Q-on} = V_{drop} \\ I_D + I_Q = I \end{cases} \tag{1}$$

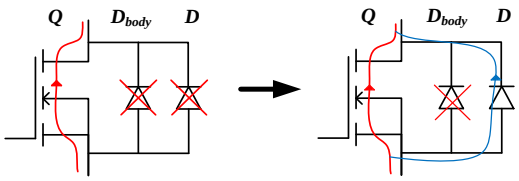

Fig. 3. Current Path During Reverse Conduction

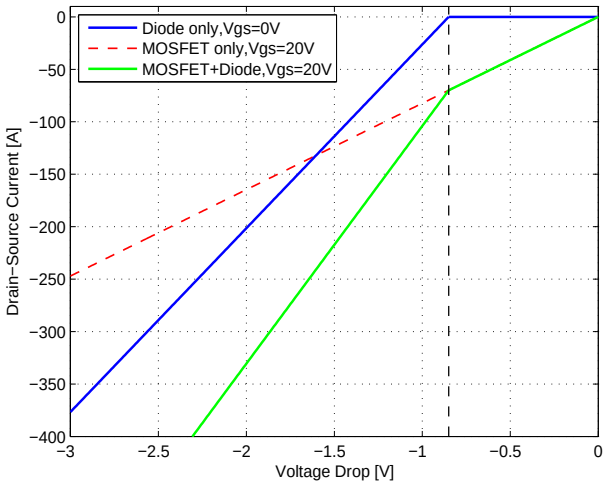

Fig. 4. 3^{rd} Quadrant Characteristics at Room Temperature from Datasheet [8]

Where V_{drop} is the total voltage drop across the device, V_{D-drop} is the initial voltage drop of the anti-paralleled diode. I, I_Q and I_D represent the current flow into the device, the current shared by MOSFET channel and the current shared by diode, respectively. R_{Q-on} and R_{D-on} represent the on-resistance for MOSFET channel and anti-paralleled diode.

When V_{drop} smaller than V_{D-drop}, it is considered that the current flows only through the channel of the MOSFET, where the body diode as well as the anti-paralleled diode are not conducted due to the insufficient voltage drop, and the MOSFET operates under fully SR. When current increases to a certain level (around $70A$ in this case, as showed in Fig.4), the voltage drop across the device is high enough to turn-on the anti-paralleled diode, and the current will be shared by the MOSFET channel and the anti-paralleled diode, as showed by the green curve in Fig.4. It is believed that a smaller conduction loss can be brought by the hybrid of SR and anti-paralleled diode conduction compared with the single anti-paralleled diode conduction, as showed in (1) and Fig.4. Moreover, with the increase of the current, the voltage drop increases and it is going to turn on the body diode that the current will be shared by the MOSFET channel, anti-paralleled diode and the body diode. However, the body diode will not be conducted in this case as the current will exceed the current rating of the employed device to get sufficient voltage drop [8].

Based on the analysis above, the effect of SR in a SiC-MOSFET based DAB converter can be analyzed. The current of the SiC-MOSFET based DAB converter can be divided into 6 segments as shown in Fig.5. The following assumptions have

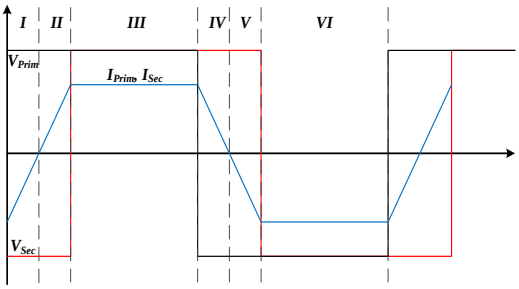

Fig. 5. Typical Switching Waveforms of DAB Converter without Dead-time

been made to simplify the analysis.

- The input and output voltage are assumed to be equal and match the transformer ratio.
- The primary bridge is assumed to be the leading bridge and the secondary bridge is the lagging bridge by φ.
- The initial current of the inductor is assumed to be negative, and the amplitude of the current is large enough to turn on the anti-paralleled diode (larger than $70A$ in this case) that it is shared by the diode and MOSFET channel.
- The effect of dead-time is temporarily neglected and will be included in next section.

1) Segment I: During this segment, $Q1$, $Q4$ on the primary bridge as well as $Q6$, $Q7$ on the secondary bridge are turned on, and the current on the both sides of the transformer increases from initial negative peak to zero. It can be concluded that even $Q1$, $Q4$ and $Q6$, $Q7$ are turned on, the devices on both side of bridge need to conduct reverse current, as shown in Fig.6(a), which means $Q1$, $Q4$ and $Q6$, $Q7$ are operating under the hybrid of SR and anti-paralleled diode conduction.

2) Segment II: In this segment, the same devices are turned on as segment I. It should be noted that the current on both sides become positive in this segment, $Q1$, $Q4$ and $Q6$, $Q7$ start to conduct forward current, as shown in Fig.6(b).

3) Segment III: In this segment, $Q1$, $Q4$ on the primary bridge are turned on while $Q6$, $Q7$ on the secondary are turned off. $Q5$, $Q6$ are turned on instead. Due to the assumption made earlier, the voltages are assumed to be equal which means there is no voltage difference on the inductor during this segment and the current on both sides of the converter should stay constant. As Fig.6(c) shows, $Q1$, $Q4$ continue conducting forward current, however, $Q5$ and $Q8$ on the secondary will operate under the hybrid mode.

4) Segment IV: When $Q1$, $Q4$ are turned off, $Q2$, $Q3$ are turned on, a voltage difference appears on the inductor and the current on both sides start to decrease, but stays positive until this segment finishes. It can be noted that $Q2$, $Q3$ on the primary side will start to conduct reverse current. The same condition happens to $Q5$ and $Q8$ on the secondary bridge, as Fig.6(d) illustrates.

5) Segment V and VI: Similar with segment II and segment III, $Q2$, $Q3$ as well as $Q5$, $Q8$ conduct forward current during Segment V. $Q2$, $Q3$ continue conducting forward current while $Q6$ and $Q7$ operate under hybrid mode during Segment VI, as shown in Fig.6(e), (f).

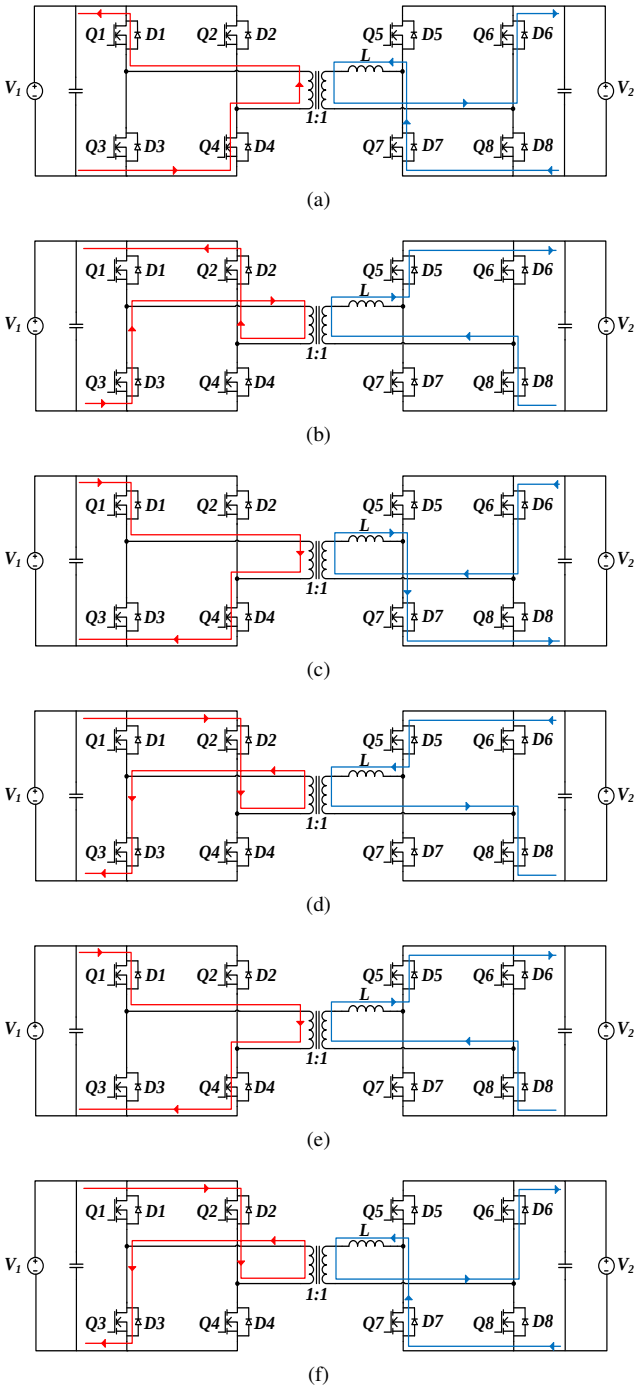

Fig. 6. DAB Current Analysis with 6 Different Segments

It is clear that, based on the analysis above, most of the time the devices of the secondary bridge (lagging bridge) operate under SR or hybrid mode, but the devices on the primary bridge (leading bridge) operate more under forward conduction mode. The conduction loss model can be derived based on the above analysis, which will be illustrated in next section. The effect of dead-time on the converter current as well as the devices current will be discussed in the next section as well.

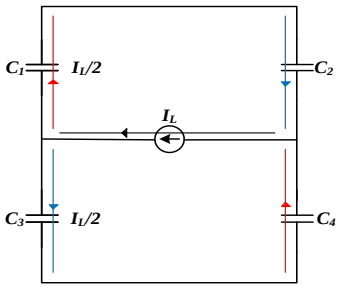

Fig. 7. Parasitic Capacitance Current Path during Dead-time (Primary)

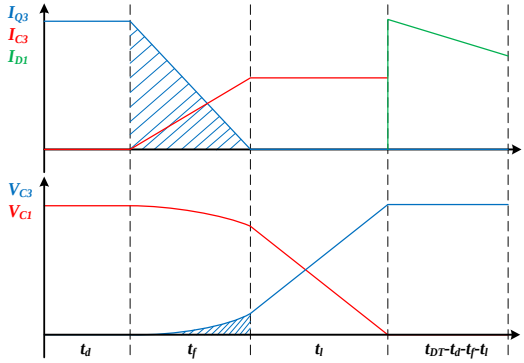

Fig. 8. Switching Transient during Dead-time (Primary)

III. Device Loss Model with SR and Dead-time

An ideal current analysis has been carried out in the previous section and the effect of dead-time is not considered. However, in a real converter, the existence of dead-time affects a lot on the transient behavior of the devices, and it is also believed to affect the overall losses of the SiC MOSFET based converter.

A. DAB Current Model

In order to analyze the effect of dead-time accurately, the transient of the SiC MOSFET current and voltage during dead-time should be discussed. Fig.7 shows the current path of the parasitic capacitance of the devices during switching transient in the dead-time. It is assumed that the inductor current at the beginning the switching transient is negative and stays constant during dead-time, $Q2$ and $Q3$ are turned on before this transient, which means the voltage of the parasitic capacitance C_2, C_3 are $0V$, and C_1, C_4 are V_1. Once the turn-off signal is applied to $Q2$ and $Q3$, after a certain amount of delay time td, the forward current flow through $Q2$ and $Q3$ will split into two parts. Half of the inductor current is used to discharge C_1 from V_1 to $0V$, another half is used to charge C_3 from $0V$ to V_1. The same condition happens for C_2 and C_4, where C_2 is charged while C_4 is discharged. It can be concluded that if the initial inductor current is large enough to charge and discharge the capacitance, the zero voltage switching (ZVS) can be achieved and there will be no turn-on loss.

However, the turn-off loss still needs to be considered. Fig.8 shows the voltage and current waveform during dead-time. As seen in the first part of Fig.8, as discussed before, a certain delay time exists due to the devices properties, and the current

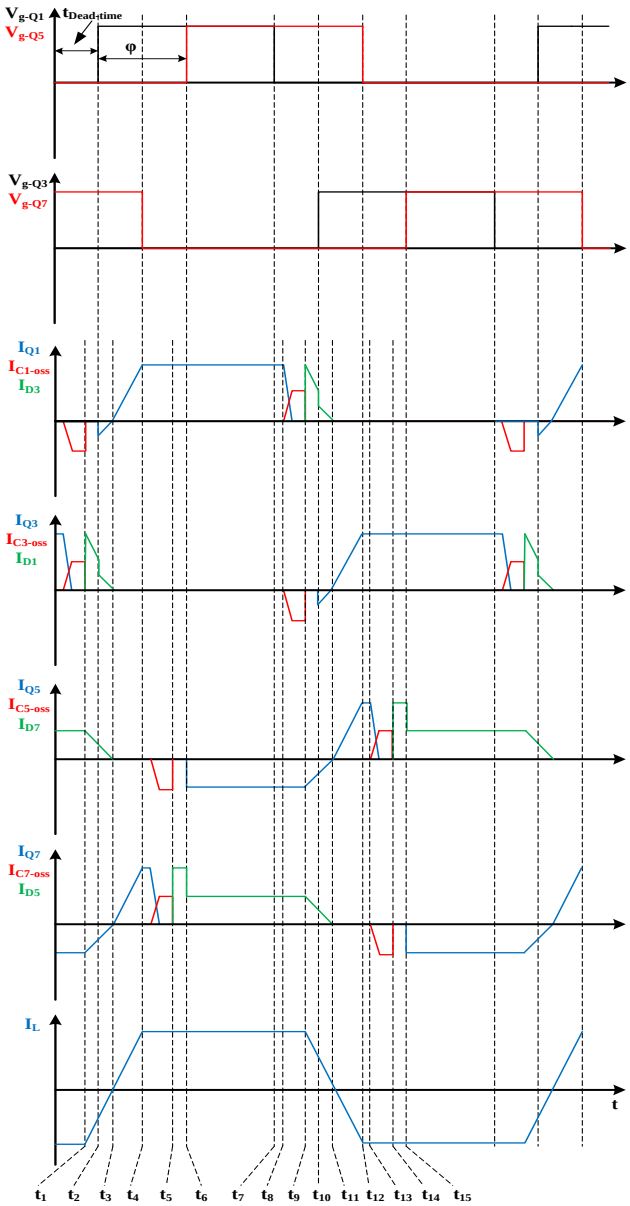

Fig. 9. DAB Current Model with Dead-time

as well as the voltage stay constant during this time. The current of $Q3$ starts to reduce after t_d and being split into the two capacitance, where the capacitance are assumed to be equal in this paper. The voltage of $Q3$ starts to increase at the same time. The amount of time for this period is t_f, which is also determined by the device properties. The value of the increased voltage during this period can be calculated by (2).

$$\begin{cases} I_{Q3}(t) = \frac{-I_L}{t_f}t + \frac{I_L}{t_f}(t_d + t_f) \\ V_{Q3}(t) = \frac{1}{C}\int I_{Q3}(t)dt \end{cases} \tag{2}$$

After $Q3$ current reaches $0A$, the voltage still needs to increase to the supply voltage V_1 that the inductor current keep charging the capacitance C_3. The amount of time for this period can

be calculated by (3).

$$t_l = \frac{2C}{I_L}\ (V_1 - V_{Q3}(t_d + t_f)) \tag{3}$$

It can be noted from the second part of Fig.8 that the voltage of $Q1$ has a reverse behavior compare with the voltage of $Q3$. The total transient time can be calculated by (4).

$$t_{transient} = t_d + t_f + t_l \tag{4}$$

If the total dead-time been set to t_{DT}, as shown in Fig.8, the remaining time after the transient is $t_{DT} - t_{transient}$. The turn-off loss happens during t_f, as can be seen in the blue area in Fig.8. It should be noted that the voltage is reversed during the transient time that V_{C1} increases from $0V$ to V_1 while V_{C3} decreases from V_1 to $0V$. Thus the current will transfer from the capacitance into the anti-paralleled diode $D1$, where the single anti-paralleled diode conduction loss occurs. On the other hand, the voltage on the primary of the transformer, from the converter point of view, is reversed, therefore the inductor current starts to decrease.

Based on the analysis on the transient behavior during dead-time above, the detailed current waveform including the effect of SR and dead-time for both devices and converter can be derived and presented in Fig.9. The current directions should be clarified. For the SiC MOSFET point of view, the forward current is considered as positive and reverse current is considered as negative in the figure. For the parasitic capacitance, positive current means the capacitor is being charged and negative current means the capacitor is being discharged. Moreover, as seen in the figure, sometimes the current is shared by the anti-paralleled diode and the SiC MOSFET channel (e.g. from t_2 to t_3 for $Q1$ and $D1$ on the primary bridge, and from t_6 to t_{10} for $Q5$ and $D5$ on the secondary bridge).

Similar with the current analysis in previous section, even the dead-time is included, the six segments still apply. The differences will be the extra single anti-paralleled diode conduction during dead-time and the small reduction caused by the device transient on the phase-shift angle (φ in Fig.9). The actual phase-shift angle will be $\varphi - t_{transient} 2\pi f_{sw}$.

$I_{Q1,D1} =$

$$\begin{cases} 0 & (0 \le t \le t_2) \\ \frac{V_1}{\pi f_{sw} L}\omega t - \frac{V_1(\varphi + 2\pi f_{sw} t_{transient})}{2\pi f_{sw} L} & (t_2 \le t \le t_4) \\ \frac{V_1(\varphi - 2\pi f_{sw} t_{transient})}{2\pi f_{sw} L} & (t_4 \le t \le t_8) \\ 0 & (t \ge t_8) \end{cases} \tag{5}$$

$I_{Q5,D5} =$

$$\begin{cases} 0 & (0 \le t \le t_6) \\ \frac{-V_1(\varphi - 2\pi f_{sw} t_{transient})}{2\pi f_{sw} L} & (t_6 \le t \le t_9) \\ \frac{V_1}{\pi f_{sw} L}\omega t & \\ \quad - \frac{V_1(\varphi + 2\pi + 2\pi f_{sw}(t_{transient} + t_{DT}))}{2\pi f_{sw} L} & (t_9 \le t \le t_{12}) \\ \frac{V_1(\varphi - 2\pi f_{sw} t_{transient})}{2\pi f_{sw} L} & (t_{12} \le t \le t_{13}) \\ 0 & (t \ge t_{13}) \end{cases} \tag{6}$$

$I_{D3-deadtime} =$

$$\begin{cases} 0 & (0 \le t \le t_1) \\ \frac{V_1}{\pi f_{sw} L}\omega t - \frac{V_1(\varphi + 2\pi f_{sw} t_{transient})}{2\pi f_{sw} L} & (t_1 \le t \le t_2) \\ 0 & (t \ge t_2) \end{cases} \tag{7}$$

$I_{D7-deadtime} =$

$$\begin{cases} 0 & (0 \le t \le t_{14}) \\ \frac{V_1(\varphi - 2\pi f_{sw} t_{transient})}{2\pi f_{sw} L} & (t_{14} \le t \le t_{15}) \end{cases} \tag{8}$$

The current model can be expressed by (5) - (8). It should be noted that the current model for the anti-paralleled diode is only given for the period of dead-time conduction, as the combined equation is given for the current sharing period with the SiC MOSFET channel, and the separated current equation can be derived using (1), (5), (6). It is more meaningful to use the combined equation as the 3^{rd} quadrant characteristics is given based on the current sharing between the channel and anti-paralleled diode, as Fig.4 and [8] showed. Moreover, due to the symmetrical property of the topology, only one device current expression is given for each bridge.

B. Device Loss Model

The device loss model can be derived based on the given current model in previous sub-section, and can be expressed by (9) - (14).

$$P_{con-Q1,D1} = \frac{1}{T_{sw}} \int_{t_2}^{t_8} V_{drop} I_{Q1.D1} dt \tag{9}$$

$$P_{con-Q5,D5} = \frac{1}{T_{sw}} \int_{t_6}^{t_{12}} V_{drop} I_{Q5.D5} dt \tag{10}$$

$P_{con-D3-deadtime} =$

TABLE I
CALCULATION PARAMETERS

Converter Parameters		
V_1		$750V$
V_2		$750V$
L		$38uH$
f_{sw}		$20kHz$
Device Parameters		
Symbol	SiC MOSFET	Si IGBT
t_d	$70ns$	$250ns$
t_f	$22ns$	$50ns$
C_{oss}/C_{oce}	$5nF$	$5.5nF$

$$\frac{1}{T_{sw}}\int_{t_1}^{t_2} V_{D-drop} I_{D3-deadtime} dt \tag{11}$$

$$P_{con-D5-deadtime} = \frac{1}{T_{sw}}\int_{t_{14}}^{t_{15}} V_{D-drop} I_{D5-deadtime} dt \tag{12}$$

$$P_{Q3-off} = \frac{1}{T_{sw}}\int_{t_d}^{t_d+t_f} V_t I_t dt \tag{13}$$

$$\begin{aligned} P_{Device} = {} & 4P_{con-Q1,D1} + 4P_{con-Q5,D5} \\ & + 4P_{con-D3-deadtime} + 4P_{con-D5-deadtime} \\ & + 8P_{Q3-off} \end{aligned} \tag{14}$$

Where f_{sw} is the switching frequency of the device. V_{drop} and V_{D-drop} can be found from the 3^{rd} quadrant characteristics in Fig.4.

C. Calculated Results

The device losses in a SiC MOSFET power module based DAB converter is calculated using the proposed loss model. For comparison, the device losses of a Si IGBT based DAB converter is also calculated to evaluate the impact of the SiC technology. Noting that the Si IGBT cannot provide the SR capability, and the reverse current will flow through the anti-paralleled diode only. The calculation parameters are illustrated in Table I.

The first part of Fig.10 shows the calculated device losses for SiC MOSFET based DAB and the Si IGBT based counterpart. As seen in the figure that a maximum device loss reduction can be achieved by 40% due to the application of SiC MOSFET. Device loss is breakdown into conduction loss and switching loss, which is shown in the second part and thrid part in Fig.10, and it is clear that a significant reduction is observed for both conduction loss and switching loss. The SR capability of SiC MOSFET contributes a lot on reducing the conduction loss with a maximum of 38%. Moreover, the conduction loss difference becomes larger at higher device current, which is the result of the hybrid of SR and anti-paralleled conduction. For the switching loss point of view, a much shorter transient time for SiC MOSFET provides a smaller switching loss. The maximum difference can be observed at $120A$ by 48%. On the other hand, the reverse recovery effect is not considered for Si IGBT based DAB, and a even larger difference is expected if the reverse recovery effect is included.

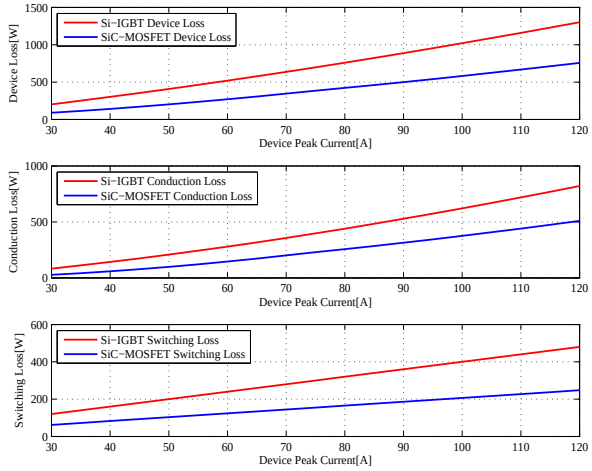

Fig. 10. Device Loss Comparison

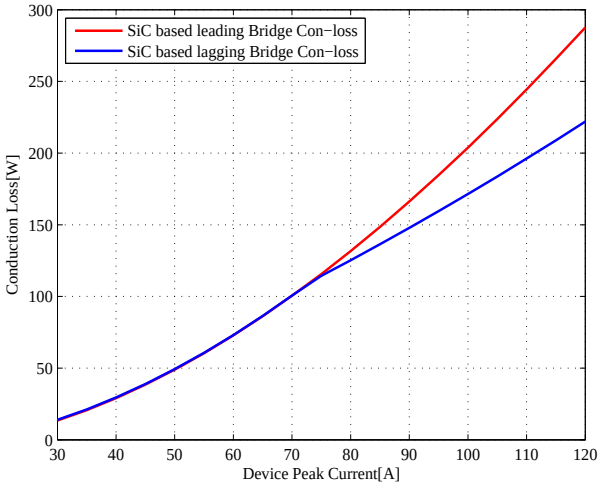

Fig. 11. Conduction Losses of the SiC MOSFET based DAB

Fig.11 shows the conduction loss for leading bridge and the lagging bridge of the SiC MOSFET based DAB, respectively. As discussed before, the leading bridge operates more under forward conduction mode while the lagging bridge operates more under the hybrid of SR and anti-paralleled diode conduction mode, which explains why the conduction loss are different. However, the difference becomes significant after $73A$, where the hybrid mode happens after this current. Due to a longer hybrid mode operation, the conduction loss on the lagging bridge becomes smaller than leading bridge, and the maximum difference is 20%.

D. Dead-time Range Discussion

The transient behavior has been analyzed in last sub-section, and the calculation equation to get the total transient time is also discussed in (3), (4), and Fig.8. The calculated transient time $t_{transient}$ is a parameter that related to the load current and device properties. Moreover, it is also the minimum dead-time to be applied and a smaller dead-time leads to the shoot-through problem of the converter. On the other hand, if the dead-time so large that even larger than half of the phase-shift period, where the inductor current will go across zero point and the directions is reversed, the dead-time effect is expected also known as dead-band effect. The dead-band effect in DAB has been discussed by several papers [9] [10] [11]. Voltage reverse and voltage sag are two major problems that caused by dead-band effect and the maximum dead-time that can be applied will be half of the phase-shift, as shown in (15).

$$t_{transient} \leq Dead - time \leq \frac{\varphi}{4\pi f_{sw}} \tag{15}$$

IV. Conclusion

A detailed device loss model of a SiC MOSFET power module based DAB converter has been proposed in this paper, which considered the effect of synchronous rectification and dead-time. The current of the SiC based DAB is analyzed and it can be concluded that SiC based DAB could provide a much lower conduction loss compared with Si counterpart due to the capability of operating under SR mode. Moreover, the transient behavior is discussed and the switching loss is calculated. Due to a much short transient time, SiC based DAB has lower switching loss. On the other hand, based on the current analysis, the conduction loss breakdown is shown, and it is proved that the lagging bridge has a lower conduction loss compared with primary bridge for SiC based DAB due to the hybrid of SR and anti-paralleled diode conduction. And last, the dead-time range is given. This analytical device loss model provides a method to estimate the device loss accurately using data-sheet values, the experimental validation is undergoing and comparison should be made in the future.

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