A Wire-bond-less 10 kV SiC MOSFET Power Module with Reduced Common-mode Noise and Electric Field

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Abstract

While wide-bandgap devices offer many benefits, they also bring new challenges for designers. In particular, the new 10 kV silicon carbide (SiC) MOSFETs can switch higher voltages faster and with lower losses than silicon devices while also being smaller in size. These features can result in premature dielectric breakdown, higher voltage overshoots, high-frequency current and voltage oscillations, and greater electromagnetic interference. In order to mitigate these side effects and thus fully utilize the benefits of these unique devices, advanced module packaging is needed. This work proposes a power module package with a small footprint (68 mm × 83 mm), low gate- and power-loop inductances (4 nH), increased partial discharge inception voltage (53 %), and reduced common-mode current (90 %).

1. Introduction

10 kV silicon carbide (SiC) MOSFETs are able to switch higher voltages faster and with lower losses than silicon IGBTs [1]. These features reduce the complexity of medium-voltage systems since simpler topologies with fewer levels can be used. However, it has been shown that the package can have profound impacts on the device performance [2]. Accordingly, to reap the full benefits of these unique devices an optimized power module package must be developed. This paper will present a wire-bond-less, synchronous, half-bridge, 10 kV SiC MOSFET module with high density, small gate- and power-loop inductances, low electric field concentration, fast switching, reduced common-mode (CM) current, and low thermal resistance.

2. 10 kV SiC MOSFET Module Design

Fig. 1 shows the designed half-bridge power module, which has three 10 kV, 350 mΩ SiC MOSFET die in parallel per switch position. No external anti-parallel diodes are used. The module uses molybdenum (Mo) posts and a direct bonded aluminum (DBA) substrate for the interconnections instead of wire bonds. This structure reduces the parasitic inductances and capacitances, and allows the capacitors to be integrated inside the module (Fig. 1c) without increasing the footprint. With the housing and integrated cooler, the module dimensions are 68 mm × 83 mm × 25 mm.

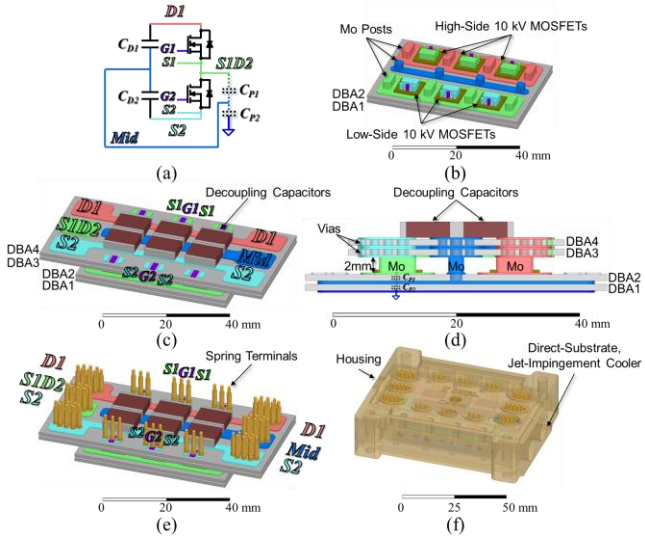


Fig. 1. (a) Schematic and 3D models of the (b) bottom and (c) complete assemblies, (d) side-view of the module, (e) terminal arrangement, and (f) housing with integrated cooler. The colors in the 3D models

correspond to the nodes in the schematic with the same color.

The 2-mm-tall Mo posts, shown in Fig. 1b and Fig. 1d, act as spacers that reduce the peak electric field between the edge termination of the 10 kV MOSFET die and the source potential on the upper DBA substrate. Mo is chosen because its coefficient of thermal expansion is close to that of SiC, and thus reduces the thermomechanical stresses compared to copper [3]. While similar structures have been explored in the past, they were developed for slower, lower-voltage silicon devices [4],[5]. This is the first work that applies this type of wire-bond-less, planar structure to 10 kV SiC devices.

In this work, 1-mm-thick aluminum nitride (AlN) DBA is used for the substrate. The DBAs have vias (Fig. 1d), which bring the electrical connections of the MOSFETs to the top DBA (DBA4 in Fig. 1c), where the module terminations are located (Fig. 1e). As can be seen from Fig. 1c and Fig. 1d, each MOSFET switch pair has its own set of decoupling capacitors placed directly above it, providing a symmetric, low-impedance, high-frequency loop for the paralleled die. The parasitic elements were simulated using ANSYS Q3D. The simulated power-loop inductance is 4.4 nH for each MOSFET switch pair. This is more than three times lower than the power-loop inductance of other 10 kV power modules reported in the literature [6]. Gate and Kelvin source contacts are distributed to each of the die to maintain symmetry and thus reduce transient imbalance among the paralleled die, as well as to decouple the gate and power loops. The simulated gate-loop inductance is 3.8 nH per die. Moreover, the gate- and power-loops are perpendicular to one another, thus further minimizing the coupling.

3. Electric Field Reduction

In order to address the enhanced electric fields associated with a high-voltage, high-density package, the DBA substrates must be carefully designed and evaluated. AlN typically has a dielectric strength around 20 kV/mm. Therefore, for a 10 kV power module, one would expect that 1-mm-thick AlN would provide sufficient margin such that the module could operate reliably at this voltage level. However, while the electric field in the bulk of the AlN will be 10 kV/mm at 10 kV, the electric field at the triple points, where the AlN, Al, and encapsulation meet, will be highly concentrated, easily exceeding 20 kV/mm. When the electric field at the triple points exceeds the dielectric strength of the insulation materials (i.e. the AlN or encapsulation), then partial discharge (PD) can occur. Repetitive PD events can ultimately result in insulation failure, thus destroying the power module [7].

In this work, two DBAs are stacked together (Fig. 1b and Fig. 1d) to reduce the peak electric field both within the bulk AlN and at the critical triple points. The concept of stacking ceramic substrates was proposed in [8]; however, in [8], only simple substrates with no patterns in the metal layers were considered. In a practical power module, the topside metal is patterned with many separate pads that are at different potentials. Therefore, the top and bottom metal layers of the substrate, and thus the isolation capacitances, are not symmetrical.

Accordingly, if the middle metal layer of the DBA stack is left floating, as it is in [8], then it may not reach a potential that will yield a meaningful reduction in the peak electric field. This phenomenon was verified by ANSYS Maxwell 2D electrostatic simulations. Fig. 2 shows the simulated electric field distribution for the case when the top metal is patterned and has two different potentials. Fig. 2a and Fig. 2c show the simulated electric field plots for a single DBA substrate and two stacked DBA substrates with the middle metal layer left floating, respectively. Comparing these two figures, it can be seen that stacking two DBAs and leaving the middle metal floating results in a slight reduction in the peak electric field at the triple point (34 percent), and that the electric field within the bulk AlN is not uniformly distributed in the two substrates. This is because the asymmetry and different potentials cause the middle metal to float to a potential that is less than half of the applied voltage (1.3 kV for this example).

If instead the middle metal is connected to half of the applied voltage (Fig. 2d), then the electric field is reduced by 58 percent compared to the single-substrate case (Fig. 2a), and the electric field in the bulk AlN is uniformly distributed in the two substrates. Therefore, in this work, the middle metal layer of the DBA stack is connected to half of the bus voltage.

The connection of the middle metal layer to half of the bus potential can be realized with the embedded decoupling capacitors. As shown in Fig. 1a and Fig. 1c, each set of decoupling capacitors consists of two, 5-kV ceramic capacitors placed in series. From Fig. 1d, it can be seen that the midpoint of the capacitors is

connected to the middle metal layer of the bottom DBA stack through vias and Mo posts. This connection allows the middle metal layer to be connected to half of the bus voltage, thus reducing the peak electric field in the power module.

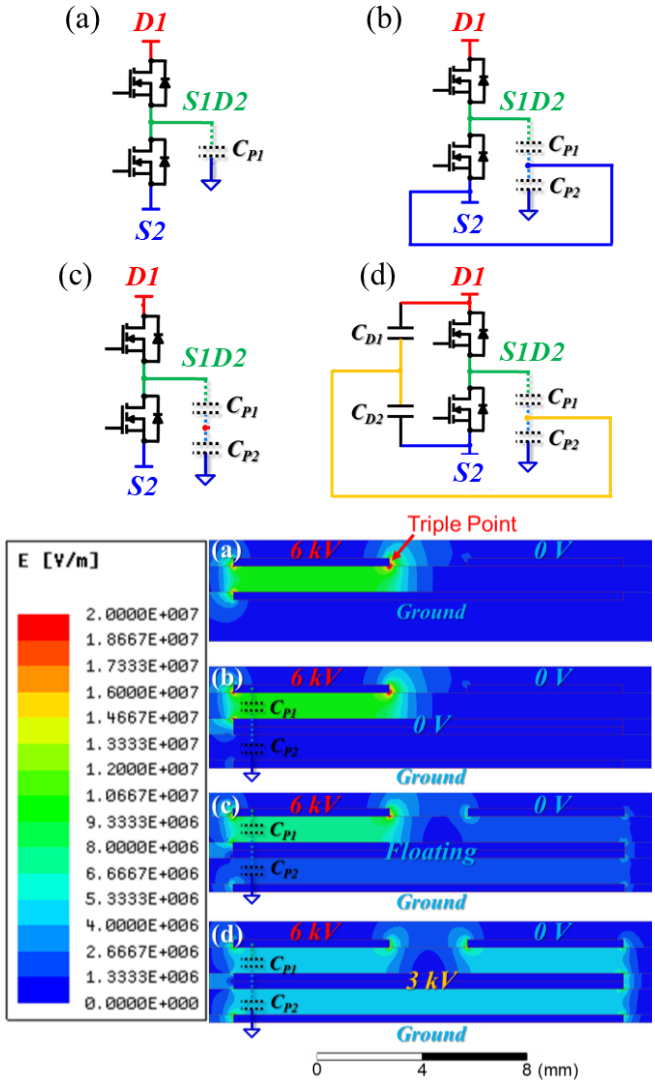


Fig. 2. Schematics and their corresponding simulated electric field plots for (a) a single DBA, (b) two stacked DBAs with middle metal connected to S2, (c) two stacked DBAs with the middle metal left floating, and (d) two stacked DBAs with the middle metal connected to half of the applied voltage (3 kV).

4. Common-mode Noise Reduction

This arrangement has another advantage: it acts as a screen for common-mode (CM) current. Due to the fast switching, specifically the high rate of voltage change (dv/dt), of the 10 kV SiC MOSFETs, the parasitic capacitances (C_{P1} and C_{P2} in Fig. 1d) that exist across the DBA substrates form a path for CM current to flow through the ground. However, by connecting the middle metal layer to the capacitor midpoint, the current flowing through C_{P1} is diverted back to the bus instead of flowing through C_{P2} and thus to the ground (Fig 1a and Fig. 2d). Therefore, because of the lower-impedance path offered by this screen, the CM current will be contained within the power module.

A similar idea was presented in [9]. However, in [9], it was proposed to connect the middle metal layer to either the positive or negative bus rail. With this connection, one of the substrates will support the majority of the voltage while the other will support a negligible amount. The simulated electric field for the case when the middle metal layer is connected to the negative rail is shown in Fig. 2b. As can be seen from the figure, there is no improvement in the electric field compared to the single-substrate case. Hence, the additional substrate is not being fully utilized.

Moreover, in [9], the screen was implemented using wire bonds and long power terminals, resulting in high inductance in the screen path. In order for the screen to effectively divert the CM current from going to the ground, a few conditions must be satisfied:

$$Z_{screen} < Z_{gnd} \quad (1)$$

$$f_{screen} > f_{sw} \quad (2)$$

$$f_{screen} > f_{gnd} \quad (3)$$

where Z_{screen} and Z_{gnd} are the impedances of the screen and ground paths, f_{screen} and f_{gnd} are the resonant frequencies of the screen and ground paths, and f_{sw} is the frequency of the switching rate (i.e. the inverse of the voltage rise or fall times) of the 10 kV SiC MOSFET.

First, the impedance of the screen path must be much lower than that of the ground path, especially at high frequency (Eq. 1). Second, the resonant frequency between the parasitic inductance of the screen path, L_{screen}, and the decoupling capacitors, C_{D1} and C_{D2}, must be greater than the switching speed of the devices, particularly during the fast turn-on transient (Eq. 2). Finally, the resonant frequency of the screen path must be larger than that of the ground path (Eq. 3).

The parasitic inductance of the ground path, and hence the resonant frequency, will be highly dependent on how the ground connection is implemented in the application. The worst-case condition will be evaluated in this analysis so as to

account for variations in the implementation of the ground connection. The worst-case condition is when the parasitic inductance of the ground path is zero, and thus the high-frequency impedance is low. Therefore, Eq. 3 will be ignored, and Eq. 1 and Eq. 2 can be rewritten as:

$$\left|\omega L_{screen} - \frac{1}{\omega C_D}\right| < \left|\frac{1}{\omega C_{P2}}\right| \quad (4)$$

$$\frac{1}{2\pi\sqrt{L_{screen}C_D}} > \frac{1}{2\pi f_{sw,on}} \quad (5)$$

From Eq. 4 and Eq. 5, it is clear that L_{screen} should be as small as possible in order to minimize Z_{screen} and maximize f_{screen}. C_D, on the other hand, should be large enough to minimize Z_{screen}, yet large enough to maximize f_{screen}. Consequently, there is a range for C_D that will make the screen the most effective:

$$\frac{1}{\omega\left(\omega L_{screen} - \frac{1}{\omega C_{P2}}\right)} < C_D < \frac{1}{L_{screen}\left(2\pi f_{sw,on}\right)^2} \quad (6)$$

In order to make L_{screen} small, this work uses vias and short Mo posts to connect the middle metal layer to the midpoint of the embedded capacitors (Fig. 1d), resulting in a low-inductance path for the CM current. For the power module shown in Fig. 1, L_{screen} is 2 nH, and C_{P2} is 160 pF, according to ANSYS Q3D simulations. Accordingly, C_D should be greater than 160 pF. The drain-source voltage rise time from preliminary double-pulse tests at 2.5 kV is on the order of 10 ns [10]. At 6 kV, the expected rise time is around 20 ns, resulting in a $f_{sw,on}$ of 50 MHz. Therefore, C_D should be less than 5.07 nF. In this work, 680-pF capacitors were selected. As shown in Fig. 1c, there are three capacitors in parallel—one above each MOSFET switch pair—giving an equivalent capacitance of 2.04 nF, and thus a resonant frequency of 80 MHz. This implementation of the screen will result in an impedance that is nearly thirteen times lower than the impedance of the ground path with only C_{P2} considered (i.e. no parasitic inductance). Preliminary testing results that demonstrate the effectiveness of this integrated screen will be shown in a later section.

In [11], further analysis on the requirements for an effective screen are presented.

5. Power Module Prototype

A prototype module that incorporates all of the above-mentioned features was fabricated with six 10 kV SiC MOSFETs (Fig. 3). A direct-substrate, jet-impingement cooler was custom-designed and integrated into the module housing (Fig. 3c). As can be seen in Fig. 3c, a jet-impingement cell is located under each MOSFET die. The module junction-to-ambient thermal resistance was measured to be 0.38 K/W with the designed cooler.

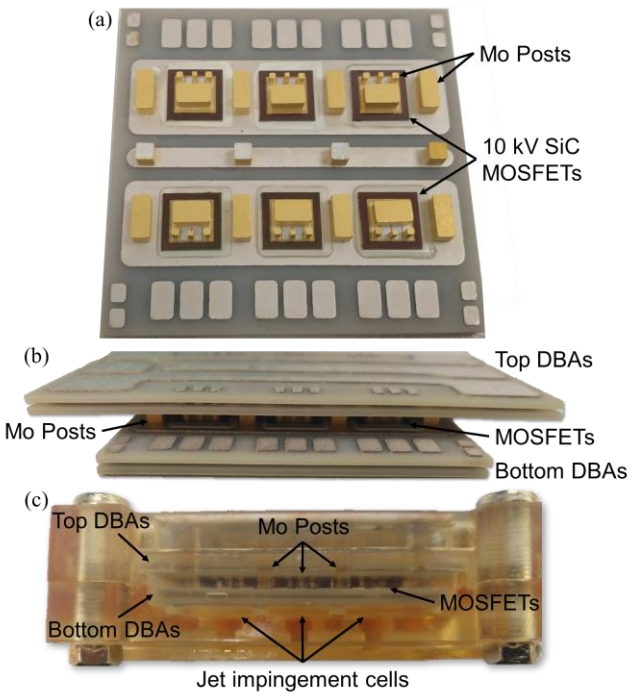


Fig. 3. Assembled module with (a) 10 kV SiC MOSFETs and Mo posts, (b) stacked DBA substrates, and (c) the housing and integrated jet-impingement cooler.

6. Partial Discharge Tests

Partial discharge tests of a patterned, 1-mm-thick AlN-DBA substrate were performed using a 60-Hz ac excitation voltage. The PD charge was measured using __. Three cases were tested: 1) a single DBA, 2) two stacked DBAs with the middle metal left floating, and 3) two stacked DBAs with the middle metal connected to half of the applied excitation voltage.

The partial discharge inception voltages (PDIV) for the three cases when the samples are tested in air are shown in Table I. When the samples are encapsulated, or submerged in oil, the PDIV exceeds 9 kV rms. The tests were limited to 9 kV rms due to the voltage rating of the capacitors used

to connect the middle metal to half of the excitation voltage.

As can be seen from the table, the PDIV increased by ? percent when the two DBAs were stacked together and the middle metal was left floating compared to the single DBA case. When the middle metal was connected to half of the applied voltage, the PDIV increased by 53 percent compared to the single DBA case. These results are consistent with the Maxwell electrostatic simulations.

Table I. Experimental partial discharge inception voltages

Condition	PDIV (kV, rms)
Single DBA	1.7 kV
Stacked DBAs (middle floating)	1.7 kV
Stacked DBAs (middle at half of applied voltage)	2.6 kV

7. Switching Tests

Switching tests were performed on the fabricated module shown in Fig. 3 to evaluate its dynamic performance and test the effectiveness of the integrated CM current screen. The tests were conducted up to 2 kV and 30 A with no external gate resistance. The voltage was limited due to the voltage rating of the test-rig bulk capacitors (2.7 kV). The hardware setup is shown in Fig. 5.

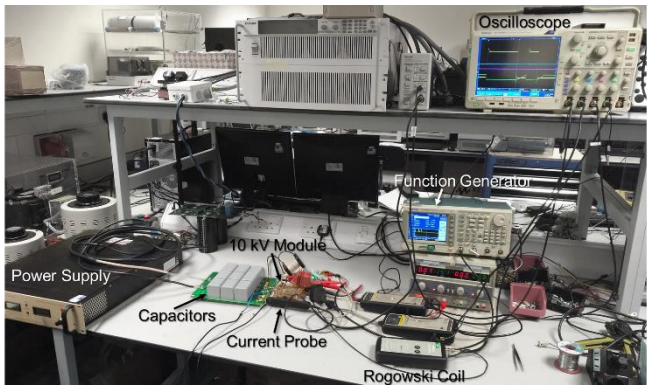
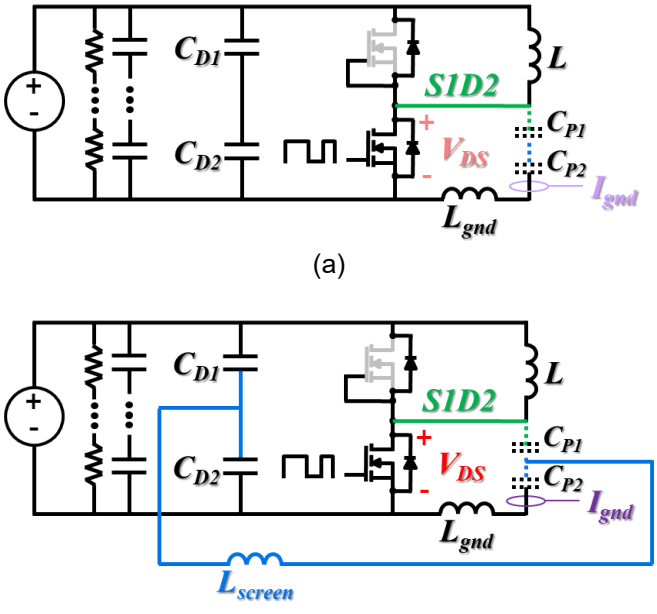


Fig. 5. Hardware setup for the switching tests of the 10 kV SiC MOSFET module.

A commercial gate driver from Wolfspeed was used to drive the low-side SiC MOSFET from –5 V in the off-state to +20 V in the on-state. The gate driver received the signal from a function generator. The gate-source and drain-source voltages of the low-side SiC MOSFET were measured using a 140-V active voltage probe with a bandwidth of 100 MHz (pico TA042), and a 7-kV active voltage probe with a bandwidth of 50 MHz, respectively. In order to measure the drain current, the decoupling capacitors were connected outside of the module encapsulation. This increased the parasitic inductance of the screen layer to approximately 25 nH. A Rogowski coil with a bandwidth of 30 MHz (CWT06) was connected between the capacitors and the power module to measure the drain current. A 10 kV, 600 W power supply was used to charge the bulk capacitors.

Fig. 6a shows the schematic of the tests when the CM screen is not connected (i.e. the middle metal layer of the bottom DBA stack is left floating). In the testing setup, a wire was used to connect the bottom metal of the module DBA to the dc bus. This connection increased the parasitic inductance of the ground loop to approximately 1410 nH. Fig. 6b shows the schematic of the tests when the CM screen is connected to the capacitor midpoint. A 420-µH inductor with high-voltage wire for the winding was connected across the high-side switch of the half-bridge module. The gate and source terminals of the high-side SiC MOSFET were shorted together such that its body diode would freewheel the current in the inductor when the low-side switch was off.



(a)

(b)

Fig. 6. Schematic of the testing setup (a) without and (b) with the CM screen connected.

In order to validate the performance of the CM screen, the current through the ground path, I_{gnd}, was measured, as shown in Fig. 6, using an RF

current transformer with a bandwidth of 200 MHz (Fisher F-33-3). C_{P1} and C_{P2} are the parasitic capacitors in the stacked DBA substrates, and C_{D1} and C_{D2} are the embedded decoupling capacitors. For these tests, the middle metal layer was connected to the midpoint of the two series 680-pF decoupling capacitors. Three capacitors were placed in parallel.

Fig. 7 shows the drain-source voltages and ground current waveforms at 2 kV and 20 A with 0 Ω gate resistance. The voltage rise time during the first turn-off transient is 66 ns, which gives a dv/dt of 24 V/ns. For a C_{P1} and C_{P2} of 46 pF and 160 pF, this dv/dt could generate a CM current up to 1 A. The measured peak current through the ground path without the proposed screen is approximately 2 A. For this testing setup, f_{gnd} and f_{screen} are estimated to be approximately 10 MHz and 22 MHz, respectively. The 66 ns (15 MHz) switching rate thus causes 10 MHz ringing in the ground current, as can be seen from Fig. 7. With the CM screen connected, the measured peak current through the ground path is 0.2 A. Hence, the proposed screen reduces the CM current by an order of magnitude for this turn-off transient.

However, during the turn-on transient, the voltage fall time is 17 ns (94 V/ns). This gives an $f_{sw,on}$ of nearly 60 MHz, which exceeds the resonant frequency of both the ground and screen paths. Accordingly, as shown in Fig. 7, the screen is not effective at reducing the ground current, and high-frequency ringing is induced. This example shows the significance of the CM screen implementation and the switching rate on the performance of the screen.

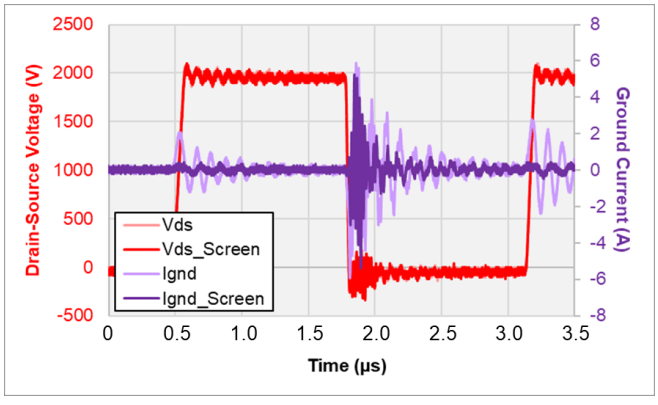


Fig. 7. Drain-source (red, left axis) and ground current (purple, right axis) waveforms with and without the CM screen.

Accordingly, with the correct implementation, the proposed integrated screen will reduce the need for filtering at the converter and/or system levels, thereby increasing the power density, lowering the cost, and simplifying the design of power electronic systems. In future tests, the decoupling capacitors will be placed inside the power module to reduce L_{screen} and thus demonstrate further improvements for the screen.

8. Conclusions

This paper proposed a compact 10 kV SiC MOSFET module with reduced electric field concentration and CM current. The stacked DBA structure with the middle metal layer connected to the capacitor midpoint increases the PDIV by 53 percent compared to the case for a single DBA substrate. This connection also forms a low-impedance path that successfully diverts the CM current that would normally flow to the system ground to the bus through the embedded decoupling capacitors. Switching tests revealed a ten-time reduction in the ground current when implementing the proposed CM screen. In order to achieve good screening performance, the implementation of the screen is critical; in particular, the parasitic inductance should be low, and the decoupling capacitor value must be chosen such that the resonant frequency is greater than the switching of the high-speed 10 kV SiC MSOFETs.

9. Acknowledgements

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