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Radiation Damage in CMOS Image Sensors for Space Applications



The Open University

Joseph Edward Rushton

School of Physical Sciences

The Open University

This dissertation is submitted for the degree of
Doctor of Philosophy

2017

To my parents

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text. This dissertation contains less than 65,000 words including appendices, bibliography, footnotes, tables and equations and has less than 150 figures.

Joseph Edward Rushton

2017

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List of Acronyms

AB Anti-Blooming

ADC Analogue to Digital Converter

APS Active Pixel Sensor

AR Anti-reflection

BI Back Illuminated

BiCMOS Bipolar Complementary Metal Oxide Semiconductor

BJT Bipolar Junction Transistor

C3D Compact CMOS Camera Demonstrator

CCD Charge Coupled Device

CDS Correlated Double Sampling

CIS CMOS Image Sensor

CLD Current Limiting Device

CTE Charge Transfer Efficiency

CTI Charge Transfer Inefficiency

CVF Charge to Voltage Factor

DAC Digital to Analogue Converter

DN Digital Number

DNW Deep N Well

DPW Deep P Well

DSNU Dark Signal Non-Uniformity

DTI Deep Trench Isolation

DUT Device Under Test

EMCCD Electron Multiplication Charge Couple Device

EPER Extended Pixel Edge Response

ESA European Space Agency

FET Field Effect Transistor

FI Front Illuminated

FPGA Field Programmable Gate Array

FWC Full Well Capacity

HIF Heavy Ion Facility

HST Hubble Space Telescope

I²C Inter Integrated Circuit

IC Integrated Circuit

IEEE Institution of Electrical and Electronic Engineers

JANUS Jovis, Amorum ac Natorum Undique Scrutator

LET Linear Energy Transfer

μC Micro Controller

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NIEL Non-Ionising Energy Loss

NOAA National Oceanic and Atmospheric Administration

PC Personal Computer

PCB Printed Circuit Board

PDF Probability Density Function

PKA Primary Knock-on Atom

PLL Phase-Locked Loop

PPD Pinned PhotoDiode

PRNU Pixel Response Non-Uniformity

PRT Platinum Resistance Thermometer

PTC Photon Transfer Curve

QE Quantum Efficiency

RF Radio Frequency

RTS Random Telegraph Signal

SAR Succesive Approximation Register

SEE Single Event Effect

SEFI Single Event Functional Interrupt

SEL Single Event Latchup

SET Single Event Transient

SEU Single Event Upset

SI Système International

SNR Signal to Noise Ratio

SOI Silicon On Insulator

SPI Serial Peripheral Interface

SRAM Static Random-Access Memory

SRH Shockley-Read-Hall

SRIM Stopping and Range of Ions in Matter

STI Shallow Trench Isolation

TCAD Technology Computer Aided Design

TDI Time Delay and Integration

TEC Thermo-Electric Cooler

TID Total Ionising Dose

TRIM TRansport of Ions in Matter

USB Universal Serial Bus

XMM X-ray Multi-Mirror

Declaration of publications containing this work

Rushton, J., Stefanov, K., Holland, A., Bugnet, H., Mayer, F., Cordrey-Gale, M. and Endicott, J., Single event effects in 0.18 μm CMOS image sensors. *Proc. SPIE 9915, High Energy, Optical, and Infrared Detectors for Astronomy VII.* (2016).

Rushton, J., Stefanov, K., Holland, A., Endicott, J., Mayer, F. and Barbier F., A CMOS TDI image sensor for Earth observation. *Proc. SPIE 9616, Nanophotonics and Macrophotonics for Space Environments IX.* 2015.

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Abstract

The space radiation environment is damaging to silicon devices, such as Complementary Metal Oxide Semiconductor (CMOS) image sensors, affecting their performance over time or causing total failure.

The first part of this work investigates a Charge Coupled Device (CCD) style CMOS image sensor designed for TDI (Time Delay and Integration) mode imaging, a mode commonly used for Earth observation. Damage from high energy protons in the space environment decreases the Charge Transfer Efficiency (CTE) and increases the dark current of such devices. Experimental work on proton damaged devices is presented, showing the effects on CTE and dark current. The results are compared to a standard CCD by a simulation to take into account the different dimensions and operating conditions of the two devices.

The second part of this work describes an experimental campaign to determine the effects of process variations (namely the introduction of deep doping wells and the variation of epitaxial silicon thickness) on the rate of Single Event Latchup (SEL) in CMOS Active Pixel Sensor (APS) devices. SEL is a potentially destructive phenomenon which occurs in CMOS technology but not in CCDs. Test devices were subjected to heavy ion bombardment and SEL rates recorded for a range of heavy ions causing varying amounts of ionisation. A simulation using Technology Computer Aided Design (TCAD) was developed to predict the SEL rates due to heavy ions and to understand the characteristic shape of the SEL cross section vs. Linear Energy Transfer (LET) curves produced by SEL experiments. The simulation was carried out for structures representative of each of the design variants.

Contents

Contents	xvii
List of Figures	xxiii
Nomenclature	xxxvii
1 Introduction	1
2 Silicon image sensors	7
2.1 The charge coupled device	7
2.2 CMOS image sensors	8
2.3 Use of solid state imaging in space	9
2.3.1 Astronomy	10
2.3.2 Surface observation	11
2.3.3 Functional imaging	11
2.4 CCD operation	12
2.4.1 Charge collection and storage	13
2.4.2 Charge transfer	15
2.4.3 Charge measurement	17
2.5 MOSFET	18
2.5.1 Source follower	20

2.6	APS operation	21
2.6.1	3T pixel operation	22
2.6.2	4T pixel operation	23
2.6.3	5T pixel operation	24
2.7	Quantum efficiency	25
2.8	Noise sources	27
2.8.1	Dark current	27
2.8.2	Fixed pattern noise and pixel response non-uniformity	27
2.8.3	Reset noise	28
2.8.4	Amplifier noise	28
2.8.5	Shot noise	29
2.8.6	Flicker noise	29
2.8.7	Random telegraph signals	29
3	Radiation effects in silicon image sensors operating in the space environment	31
3.1	Space radiation environment	32
3.1.1	Solar radiation	33
3.1.2	Cosmic rays	34
3.1.3	Radiation belts	35
3.1.4	Secondary radiation	36
3.2	Radiation damage mechanisms	36
3.2.1	Interaction in silicon of energetic particles	36
3.2.2	Interaction in silicon of photons	37
3.3	Ionisation damage	38
3.3.1	Ionising damage in MOS capacitor structures	39
3.3.2	Interface states	40
3.3.3	Dependence on electric field	41

3.4	Non-ionising damage	41
3.4.1	Displacement damage effects	43
3.4.2	Stable defects and annealing	45
3.5	Effects of radiation damage on the electro-optic performance of image sensors	46
3.5.1	CCDs	46
3.5.2	CMOS Image Sensors	47
3.6	Charge transfer inefficiency	48
3.6.1	Mechanism of CTI caused by charge trapping	48
3.6.2	Factors affecting trap capture and emission times	50
3.7	Single event effects	52
3.7.1	SEL	54
3.7.2	Latchup from heavy ions	56
3.7.3	Effective LET	56
3.7.4	Latchup mitigation	57
3.7.5	Triple wells	59
3.7.6	Epitaxial layer thickness	59
3.7.7	Potential barrier	60
3.7.8	Effect of temperature on latchup	60
3.7.9	SETs, SEUs, and SEFIs	61
4	Radiation damage in TDI charge-transfer CMOS image sensors	63
4.1	Introduction	63
4.2	TDI mode imaging	64
4.2.1	CCD-type TDI sensors in CMOS	67
4.3	Experimental details and initial characterisation	71
4.3.1	Prototype TDI CMOS image sensor	71
4.3.2	Camera electronics	73

4.3.3	Temperature control and light shielding	77
4.3.4	Characterisation by charge injection	79
4.3.5	Characterisation by mean-variance curve	80
4.4	Pre-irradiation characterisation	83
4.4.1	Dark current measurement	83
4.4.2	CTI measurement	84
4.4.3	EPER	85
4.4.4	Experimentally obtained EPER trails	87
4.4.5	Design and operation effects on CTI	90
4.5	Post-irradiation characterisation	92
4.5.1	Dark current	94
4.5.2	Dark current CCD comparison	96
4.5.3	CTI	98
4.6	Radiation hardness comparison with CCD sensors	101
4.6.1	Factors affecting CTI radiation hardness	102
4.7	EPER model	103
4.7.1	TDI-CMOS/CCD comparison	106
4.8	Conclusions	109
4.9	Further work	111
5	Experimental study of single event effects in CMOS active pixel sensors	113
5.1	Experimental details	114
5.1.1	Heavy Ion Facility at Université Catholique de Louvain	114
5.1.2	Potential structure of triple well devices	117
5.1.3	e2v Sapphire and Ruby sensors	118
5.1.4	Test devices	118
5.1.5	C3D camera board	120

5.1.6	Experimental setup	121
5.1.7	Temperature measurement	125
5.2	Experimental results	128
5.2.1	Phase locked loop	128
5.2.2	SEL susceptibility	128
5.2.3	Standard Sapphire vs. DNW Sapphire and comparison with previ- ous work	133
5.2.4	3.3 V supply latchup	135
5.2.5	Characteristics of SEL	135
5.2.6	SEU susceptibility	137
5.2.7	Frame read failure SEUs	138
5.2.8	Register read failure SEUs	139
5.3	Conclusions	140
5.4	Further work	142
6	SEL simulation	143
6.1	Introduction	143
6.2	Cross section model	144
6.2.1	Charge density threshold	144
6.2.2	Particle modelling	146
6.2.3	Cross section vs. LET	146
6.3	Silvaco models	148
6.3.1	Introduction to Silvaco ATLAS	148
6.3.2	Inverter model	149
6.3.3	Physical simulation models	151
6.3.4	Ion beam simulation	152
6.3.5	Carrier behaviour changes due to device structure changes	153

6.3.6	Latchup threshold search algorithm	159
6.3.7	Potentials and carrier concentrations during latchup and non-latchup events	159
6.3.8	Simulation outputs for devices experimentally studied	165
6.4	Extrapolation of simulation output to full device cross section model	165
6.4.1	Heavy ion beam model	167
6.4.2	Full device model	169
6.4.3	Full device model outputs	170
6.5	Conclusions	171
6.5.1	2-D modelling	172
6.5.2	Weibull fits	173
6.6	Further work	174
7	Conclusions and further work	175
7.1	Radiation damage in TDI charge-transfer CMOS image sensors	175
7.2	Experimental study of single event effects in CMOS active pixel sensors . .	176
7.3	SEL simulation	177
	Bibliography	179
A	Silvaco Atlas model printout	187

List of Figures

1.1	False colour image of the Rann of Kutch salt marshes in western India. Captured by the ESA Sentinel-2A satellite CMOS multi-spectral imager. The width of the pond cluster on the left is nearly 13 km. Photo credit: ESA	3
2.1	The e2v CCD201.	7
2.2	The e2v Sapphire APS used in Chapter 5.	8
2.3	Charge smearing in a CCD on the Hubble space telescope arising from incomplete charge transfer due to radiation damage (left) and the corrected image (right) [10].	10
2.4	Schematic of a full-frame CCD. [24]	12
2.5	The potential structure in a typical buried-channel CCD in inverted mode [25] [3]. The potential is shown for clock high at $V\phi=3$ V and clock low at $V\phi=-8$ V. Accumulation of electrons reduces the potential in the channel (shown by the dashed line) until the onset of saturation where no more charge can be collected.	14
2.6	Typical clocking scheme for a three phase CCD.	15
2.7	Full frame, frame transfer, and inter-line transfer readout styles	16
2.8	Typical CCD output amplifier	17
2.9	Cross section of an n-channel MOSFET.	18

2.10	Typical N-channel MOSFET electrical characteristics. The dashed line shows the boundary between the linear and saturation regions.	20
2.11	APS operation	21
2.12	3T pixel electronics	22
2.13	4T pixel electronics	23
2.14	5T pixel electronics	24
2.15	Layout of a 3T pixel designed by Murari et al. [32].	25
2.16	Top: Quantum efficiency of the back-illuminated, AR coated, e2v CCD91 developed for use on Gaia [33] compared with a back-illuminated, AR coated CMOS image sensor produced by the Jet Propulsion Laboratory [34]. Bottom: The same CMOS image sensor, front and back illuminated, without AR coating.	26
3.1	The sunspot count gives an indication of the level of solar activity. Radiation levels, measured here by the flux of protons with energies >10 MeV, are increased during periods of high activity. The data plotted are from NOAA Space Environment Services Center [42] [43] [44].	33
3.2	Cosmic rays can have extremely high energy which can cause damage to electronic components. These data are from various Earth based observations. Reproduced from Swordy [47].	35
3.3	The dominant interaction mechanism for a photon entering a material depends on the photon energy and the atomic number Z of the material. After Evans [51]	37
3.4	The NIEL caused by different radiation sources can be quantified. This allows the calculation of the amount of radiation required from a different source in order to produce an equivalent amount of damage. Data plotted from compilation by Vasilescu and Lindström [54].	43

3.5	Energy levels introduced in the silicon bandgap by displacement damage have five main effects on the operation of devices: (a) recombination; (b) generation; (c) trapping; (d) compensation; and (e) tunnelling.	44
3.6	Annealing of defects happens rapidly once a sufficient temperature is reached. These are some of the known defects in silicon crystals. Reproduced from Watkins [56].	45
3.7	Charge trapping can lead to CTI. At $t = 0$ the trap under ϕ_2 is empty. At $t = T_c$ the trap is filled with charge captured from the arriving charge packet. Capture happens quickly relative to emission. If the trap emits the trapped electron before $t = 3T_c$ it will join the original charge packet. If the trap emits after this time, the electron emitted will become part of a following charge packet resulting in CTI.	49
3.8	When vacancies produced by displacement damage combine with impurities (here, oxygen and phosphorus) or with other vacancies they can form permanent traps which lead to CTI. Reproduced from Watkins [56].	52
3.9	Electron traps cause the CTI in CCDs when the emission time constant is comparable to the CCD clock period.	52
3.10	A charged particle producing an ionisation track in a CMOS device can cause a variety of effects.	53
3.11	(a) A simple inverter circuit using two MOSFETs. (b) The parasitic circuit resulting from the well doping structure of typical CMOS processes. The cross-connected BJTs make this implementation of CMOS circuits susceptible to latchup. (c) Cross section of the inverter circuit as fabricated in dual-well CMOS (after Johnston [63]). The parasitic circuit is also shown.	55
3.12	Effective LET	57

3.13	Triple well devices typically contain either a deep n or deep p well underneath the standard n and p wells. A deep well is formed by ion implantation and usually occupies a large fraction of the device area. Certain circuits on chip may not be compatible with the deep well, APS pixels being an important example.	59
3.14	An ion strike in a MOSFET which is "off" can cause the MOSFET to conduct temporarily (an SET). In this example the voltage V_{OUT} is low until the ion strike at time $t = t_{strike}$ when the PMOS transistor begins to conduct. This takes V_{OUT} from below the threshold for a low signal, V_L , to above the threshold for a high signal, V_H . The result is the input to the following circuit being a "1" instead of a "0" for a short time.	61
4.1	A moving linear sensor can be used to capture a two-dimensional image by using a line rate $1/t_L$ to correspond to the image motion.	64
4.2	A two-dimensional sensor, in which charge is transferred row-by-row to the readout (serial) register, can also be used for moving images. If the charge transfer between rows is synchronised with the image motion, the signal from each point on the scene will increase as charge is transferred. Fast read-out is required in the serial register which limits the width of CCD-like devices, but can be achieved relatively in CMOS by directly reading each column (column-parallel readout [81]), thus avoiding the need for a serial register.	66
4.3	A 3D model of the virtual phase pixel implemented in a $0.18\mu\text{m}$ CMOS image sensor process designed by Mayer et al. [82]	68
4.4	Clocking scheme for the virtual phase pixel sensor [82]	68
4.5	Simulated potential structure within the virtual phase pixel for clock high ("on") and clock low ("off") states [82].	69

4.6	A 3D model of the four phase pixel implemented in a $0.18\mu\text{m}$ CMOS image sensor process designed by Mayer et al. [82]	70
4.7	Clocking scheme for the four phase sensor [82]	70
4.8	Chip micrograph showing the location of the 64×40 pixel array (top) and the arrangement of the design blocks (bottom).	71
4.9	Pixel, transfer gate, and floating diffusion physical cross section (top). Read-out/injection circuitry (bottom).	72
4.10	Equipment setup	73
4.11	Charge is accumulated under ϕ_2 , ϕ_3 and ϕ_4 during integration. ϕ_1 acts as a barrier phase. Charge can also be injected under ϕ_1 if the top reset and transfer gates are clocked ($RES0_U$ and TRA_U). If $RES0_U$ and TRA_U are held low no charge is injected. The ADC sampling is on the rising edge of ADC_trig	75
4.12	For testing purposes the sensor was driven to produce single column "frames" (as opposed to the constant read out which would be used for TDI). A frame consists of 3 sections which are read out in succession. After an integration time t_{int} the first section is read out which contains the signal gathered in the 40 pixels of the column during the integration time. The second section contains any injected signal. Injected signal appears at the output 40 transfers after it is injected at the top of the column. The number of injections $N_{inj} \geq 0$. Finally, a third section, the overscan, is read out, with length $N_{os} \geq 0$. After the overscan, integration begins again.	76
4.13	The TDI-CMOS chips are mounted in 25×25 mm ceramic packages. A temporary glass window was placed over the central area of the package (not shown).	77

- 4.14 The temperature was stabilised by a TEC heating or cooling a thermal mass. The thermal mass was in contact with the glass window on the chip package. The temperature of the thermal mass was monitored by a PRT connected to a TEC controller. The TEC itself was cooled using PC fan/heatsink combination. 78
- 4.15 Current measurement into the reset drain can be used to determine the CVF. Here, the CVF data points are shown as well as a fit to the data points (shown here for chip 1, block 1, column 3). The CVF varies with the voltage, probably due to the floating diffusion capacitance C_{FD} being voltage dependent. The mean CVF for this column is $9.13 \mu\text{V}/e^-$ with a 95% confidence interval of between 8.73 and $9.53 \mu\text{V}/e^-$ 80
- 4.16 An idealised mean-variance curve. At low signal read noise dominates, and the read noise variance can be read from the graph. The gradient in the shot noise dominated region can be used to calculate the CVF (in units of DN/e^- or $\mu\text{V}/e^-$). Variance increases in the fixed pattern noise region until the onset of full well when the variance begins to fall. The FWC can also be read from the graph. 81
- 4.17 Mean-variance curve. A linear fit to mean signal values from 0 to 12,000 DN was used to compute a CVF estimate of between 8.50 and $9.06 \mu\text{V}/e^-$ (0.111 and $0.119 \text{DN}/e^-$), depending on the column. This curve is obtained by plotting mean and variance of each of the 40 pixels obtained over 100 frames for the 8 columns in chip 1, block 1. Each line is the fit for a single column. 82

- 4.18 Dark current is calculated from the gradient of signal vs. integration time. Results here are for all 40 pixels in chip 3, block 1, column 1. Dashed lines show the two integration times between which the slope was used to calculate the dark current. 84
- 4.19 CTI can be calculated from a frame using EPER. The deferred charge is found in the N transfers following the edge pixel transfer. The read-out dark signal in the overscan (which is the dark signal accumulated during readout) indicates the zero-signal level. 85
- 4.20 Signals used for EPER measurement (left hand scale, transfer number ≤ 40) and the resulting charge trails (right hand scale, transfer number ≥ 40). There is a discrepancy between the charge trail sizes despite the fact that the final signal level is the same (33 ke^-) in each case. A further anomaly is that the zero-signal level at the end of the overscan is different in each case, and changing over time. 87
- 4.21 Deferred charge magnitude as estimated using three different charge trail length estimates (N) for a simple linear fit and an improved exponential fit. The quantity of deferred charge increases rapidly when the signal size exceeds 70 ke^- as electrons start to be trapped at interface states due to the growing charge cloud volume extending up to the interface. Below 70 ke^- the quantity of deferred charge rises slowly, signifying that the charge cloud is growing only a small amount and in a volume of constant trap density. In this region the CTI is approximately proportional to $1/n_{sig}$ 89

- 4.22 EPER charge trails did not decay to a constant value. Therefore, a fitting function was required to estimate a suitable offset for summation of deferred charge. The fitted function eventually used was $f_{fit}(x) = Ae^{-Bx} + Cx + D$, where A, B, C, and D were all fitting parameters and x the transfer number. $f_{offset}(x) = Cx + D$ was used as the offset function. The inset shows the overscan in more detail. 90
- 4.23 CTI vs. signal for 6 blocks. Block 2 (implant split B) has a lower FWC but best CTI. Blocks 0 and 1 and blocks 4 and 5 share implant splits (A and D) and have similar FWC. There is no clear correlation between either the interpolate gap or the anti-blooming gate choices and the FWC or CTI. . . . 91
- 4.24 Increasing V_ϕ causes the signal packet to be transported closer to the surface which causes a reduction in FWC as excess charge becomes trapped in interface states causing the onset of surface full well. 92
- 4.25 TDI-CMOS device with protective window (above left) and with window removed, mounted for proton irradiation (top right). Device mounted at the beam-line ready for irradiation (below). 93
- 4.26 Dark current at 298 K in design block 1. Left: results for chip 2 pre-irradiation and at the two 10 MeV proton equivalent fluences of $5 \times 10^9 \text{ cm}^{-2}$ and $5 \times 10^{10} \text{ cm}^{-2}$. Right: results for chip 3 pre-irradiation and at $1 \times 10^{10} \text{ cm}^{-2}$ and $1 \times 10^{11} \text{ cm}^{-2}$ 94
- 4.27 Mean dark current increase for each of the 6 design blocks at all fluences. The dark current increase is similar in each block. 95
- 4.28 Dark current in the CCD201 EMCCD over a range of temperatures. The shielded region (blue) exhibits approximately half of the dark current of the irradiated region (green). The 10 MeV equivalent proton fluence used in the irradiation was $1 \times 10^9 \text{ cm}^{-2}$ 97

- 4.29 CTI data for block 1 at all fluences. After the first irradiation the CTI increase was difficult to measure, so a further irradiation was carried out to higher fluences. The inset shows the data points. Since integration time, not signal level, was controlled the signal values for each column are slightly different due to the variation of dark currents. The curves are the averages of interpolated data points for each column. 99
- 4.30 Comparison of CTI in each design block after irradiation to the maximum fluence ($1 \times 10^{11} \text{ cm}^{-2}$ 10 MeV equivalent). Block 2 has relatively good CTI but maintains lower FWC. Block 3 has higher CTI at all signal levels than the other 5 design blocks. 100
- 4.31 CTI vs. fluence for each of the 6 design blocks on chip 3. 100
- 4.32 CTI per pixel is usually calculated by assuming that the amount of deferred charge in the EPER charge trail is proportional the number of pixels. This assumption is valid for $\tau_c \approx 0$. Simulating the TDI-CMOS transfer for array sizes of 1 to 40 pixels at $T=298 \text{ K}$ we see that the amount of deferred charge per pixel increases by approximately 32% over the deferred charge in a single pixel array. The increase in deferred charge per pixel as the array size grows beyond 40 pixels becomes negligible. This result highlights how each evaluation of CTI is specific to the exact method used to measure it. . . 105
- 4.33 Deferred charge as a function of temperature. Simulated results for EPER measurement after transfer through 160 phases. Simulation parameters are shown in Table 4.6. 106
- 4.34 Deferred charge vs. charge cloud volume at $T=298 \text{ K}$. The estimated charge cloud volumes are $10 \mu\text{m}^3$ and $15 \mu\text{m}^3$ for the TDI-CMOS and CCD201 devices respectively. 107

4.35	There is a significant difference in dark signal and therefore in the size of the "fat zero" present during the EPER measurement of the CCD201 and TDI-CMOS devices. In order to rule out this difference as the cause of the different peak deferred charge amounts due to the divacancy observed in the simulation, deferred charge is shown here as a function of dark signal at 298 K. The CCD201 dark signal is 0.00329 e^- and the TDI-CMOS dark signal is 16.9 e^- (shown by the dashed lines). Although the dark signal does affect the amount of deferred charge, it does not fully explain the difference in peak amounts between the two devices.	108
5.1	LET as a function of target depth for the four heavy ion species and energies used. Data calculated using SRIM.	115
5.2	Ion paths calculated by TRIM simulation of 12,000 995 MeV xenon ions in a Silicon target.	115
5.3	Simulated potential along two cut-lines A and B in a deep p well device (left) a deep n well device (right). In the deep p well device, electrons must overcome a potential barrier in the epitaxial layer in order to reach the p well or n well sensitive areas. Holes must overcome a barrier to leave the epitaxial layer. The deep p well therefore rejects electrons from the substrate and traps holes. In the deep n well device, electrons are repelled from the epitaxial layer and the deep n well. However, holes experience no barrier in drifting from the substrate all the way to the n well sensitive area.	117
5.4	Summary of device layers	119
5.5	The test board with sensor mounted, awaiting shielding, before being placed in the beam. The motor to rotate the board is shown on the right. The angle of rotation is visible to the operator via a camera system to the control room.	120
5.6	Overview of the experimental setup	121

- 5.7 The power supply current measurement circuit and connections to the sensor. The manual reset was added to connect the 1.8 V A line to ground through the body diode of the reset transistor. This was necessary when latchup current was sustained by the high logic level on CS. 122
- 5.8 Example current log excerpt for all three supplies. There are also two unusual features shown: 3.3 V latchup and a <50 mA latchup around 800 s. The dashed line shows the detection threshold. 124
- 5.9 The C3D board showing the temperature measurement configuration (bottom right) 126
- 5.10 The temperature profile of the sensor for each of the six experiment runs. Each sensor has a similar profile. The device serial number are listed in Table 5.2. 127
- 5.11 The temperature logged over the same period as Figure 5.8. No individual latchups seem to have a noticeable effect on the temperature. 127
- 5.12 SEL cross-sections for the standard Sapphire with PLL on and off at two different fluences. No significant change in cross-section is apparent. . . . 129
- 5.13 SEL cross sections for the four device variants tested. The DNW Sapphire device with serial number #539 was only tested at a single LET. 130
- 5.14 The SEL cross section data. Also shown are Weibull fits to the data, calculated with σ_0 , L_0 , W and S as free parameters. In the experiment the Sapphire began to latchup at a higher LET than the DNW Sapphire. However, because of the shape of the curve, the threshold LET is calculated to be lower. Error bars are based on 10% uncertainty of flux, angle of incidence uncertainty of 2° , and the uncertainty introduced by the finite number of latchups, according to [99]. Fit parameters are given in Table 5.3. . . . 131

5.15	Here the Weibull fits to the data are calculated with W and S fixed across the four devices. Now all four curves have similar shapes, although the fits are not as good. The threshold LET is now higher for the Sapphire than for the DNW Sapphire which seems to represent the real data better. Once again the 18 μm thick Ruby performs better than either the Sapphire or the DNW Sapphire.	132
5.16	Comparison of the Sapphire SEL cross-sections measured in previous work with the two Sapphire devices tested at multiple LETs in this work. The previous work was on a device without a triple-well, however the results are in better agreement with the DNW device tested in this work.	134
5.17	Latchup current distribution at $50.41 \text{ MeV cm}^2 \text{ mg}^{-1}$. Standard Sapphire (top left), DNW Sapphire (top right), 5.5 μm thick Ruby (bottom left), 18 μm thick Ruby (bottom right). Note: the number of latchups is not normalised to the run time.	136
5.18	Average currents during latchup. There is no clear correlation between LET and average latchup current, which is as expected. There is a clear difference between the 5.5 μm thick Ruby latchup current and the other 4 devices which is not easily explained.	137
5.19	Frame capture failure rates.	138
5.20	Register corruption rates.	140
6.1	Behaviour of a hypothetical single cell, area dA , with a hard charge density threshold . This is what is obtained from a simulation with no Monte Carlo methods (i.e. Silvaco Atlas).	145
6.2	Hypothetical distribution of charge density threshold required for latchup, ρ_0 , across chip. For a beam which is uniform in x and y it is not necessary to know the spatial distribution.	145

- 6.3 PDF of actual charge density for a chosen particle LET, which deposits a mean charge density of $\langle \rho \rangle$. The distribution will depend on mean LET chosen and must be estimated in order to account for probabilistic effects, including LET variations. 147
- 6.4 Inverter cross section used to make the 2D TCAD model. The structure was simulated without a deep well, with a deep n well, and with a deep p well. The epitaxial layer thickness was also varied. 149
- 6.5 The four device structures simulated. No deep well (top left); deep p well (top right); deep p well with 18 μm epitaxial layer (bottom left); deep n well (bottom right). The doping is shown here and the full extent of the structure. A close up, showing the inverter in detail is in Figure 6.6. 150
- 6.6 The no deep well structure, showing in detail the inverter. 151
- 6.7 No deep well. Right: electron current density immediately after ion strike at $x = 1 \mu\text{m}$ (top) and $x = -1 \mu\text{m}$ (bottom). The doping in these locations is shown on the left. 156
- 6.8 Deep p well. Right: electron current density immediately after ion strike at $x = 1 \mu\text{m}$ (top) and $x = -1 \mu\text{m}$ (bottom). The doping in these locations is shown on the left. 157
- 6.9 Deep n well. Right: electron current density immediately after ion strike at $x = 1 \mu\text{m}$ (top) and $x = -1 \mu\text{m}$ (bottom). The doping in these locations is shown on the left. 158

- 6.10 In order to find the charge density threshold the device is simulated with multiple charge densities. The sequence of charge densities simulated is computed by a Brent search algorithm. The search algorithm attempts to optimise the charge density to achieve a final current (at 20 ns) midway between the latchup current and the non-latchup current. In this case the midpoint is chosen as 20 mA. The charge densities indicated for each curve have units of $\text{pC } \mu\text{m}^{-1}$. Here the algorithm has been allowed to run up to 100 iterations and therefore shows the current logs a charge densities very close to the threshold ($0.88000 \text{ pC } \mu\text{m}^{-1}$). The current can remain unstable for tens of nanoseconds before the current either increases to the latchup current or drops to the leakage current. In each case the latchup current and leakage current are identical. 160
- 6.11 Electron concentration and the potential structure plotted for a charge density of $1 \text{ pC } \mu\text{m}^{-1}$ after $5.11 \times 10^{-12} \text{ s}$ (top) and $2 \text{ pC } \mu\text{m}^{-1}$ after $5.25 \times 10^{-12} \text{ s}$ (bottom). The potential barrier between n and p wells has broken down in both cases. 161
- 6.12 Electron concentration and the potential structure plotted for a charge density of $1 \text{ pC } \mu\text{m}^{-1}$ after $1 \times 10^{-11} \text{ s}$ (top) and $2 \text{ pC } \mu\text{m}^{-1}$ after $1 \times 10^{-11} \text{ s}$ (bottom). In the former case the potential barrier has been restored (at $x = 0$, below the STI). In the latter, the higher density charge cloud has triggered a latchup event which prevents the barrier from re-forming. 162
- 6.13 At $t = 1 \times 10^{-10} \text{ s}$ the charge from the lower density strike has largely dissipated. The higher density cloud remains. The effect of the high purity epitaxial silicon can be seen. The electrons diffuse quickly in this region, but there is little recombination. 163

- 6.14 At $t = 1 \times 10^{-9}$ s the concentrations and potentials after the $1 \text{ pC } \mu\text{m}^{-1}$ strike are almost back to where to they were before the strike (top). After the same amount of time, the larger strike (bottom) is not yet dissipated, but the electron concentration has started to increase again around both source regions. These injected electrons are carrying I_{VDD} . This device is now in latchup. 164
- 6.15 Charge density threshold vs. x location of ion strike. The high error bar is the lowest charge density at which latchup occurred. The low error bar is the highest charge density at which latchup did not occur. This 1D model is extrapolated to make the 2D map shown in Figure 6.16. The no deep well structure from Figure 6.6 is shown below for reference. 166
- 6.16 Extrapolated 2-D charge density threshold map for the no deep well device. 167
- 6.17 Energy distributions for some of the low range "cocktail", ions available at the HIF. A Gaussian fit is shown for each species. The standard deviations resulting from the fits are as follows: nitrogen $\sigma=0.87$ MeV; neon $\sigma=1.05$ MeV; argon $\sigma=1.52$ MeV. There are smaller peaks noticeable at other energies. Nevertheless, these standard deviations can be used as a rough estimate for the standard deviations on LET which, for our model, is assumed to have a Gaussian distribution. 168
- 6.18 Simulated cross section vs. LET. simulations (left to right) using charge density standard deviations of $\sigma_p=20, 10$ and $5 \text{ MeV cm}^2 \text{ mg}^{-1}$ 170

Chapter 1

Introduction

The work in this thesis concerns silicon image sensors produced using the Complementary Metal Oxide Semiconductor (CMOS) fabrication process and their applications in space. The Active Pixel Sensor (APS) and its variations are the most well established CMOS Image Sensor (CIS) implementation and comprise the majority of devices produced. Such devices are commonplace in consumer and industrial imaging and are steadily replacing the traditional Charge Coupled Device (CCD) in many applications, including scientific imaging where performance requirements are often the most challenging.

The APS takes advantage of the small feature sizes available in CMOS. The most basic APS pixel has three transistors inside the pixel itself. The use of APSs in space is mostly limited to functional machine vision, such as star trackers rather than scientific payloads. Some CMOS sensors have been used for Earth observation from satellites (Figure 1.1). The use of the CMOS APS as a replacement for CCDs in scientific space imaging will increase as their noise performance improves. Recently, as well as development of the APS, there has also been some progress in using the CCD architecture and its derivatives in devices built on the CMOS process.

Requirements which characterise the space imaging field are high reliability and predictable performance over the mission lifetime. The need for radiation hardness is particularly

challenging. For scientific space imaging, CCD devices are often bespoke one-offs. Companies such as e2v, who design and manufacture CCDs in house, can tailor the devices and the process to meet specifications such as full-wafer CCDs, or CCDs with high X-ray Quantum Efficiency (QE). The space heritage of CCDs is therefore well established and their performance proven. Radiation damage effects in CCDs are also well understood. The CMOS APS is potentially more suitable for the space radiation environment than a CCD, primarily because of the thinner oxide layers used and because charge transfer only occurs in-pixel. In contrast, charge transfer of the signal from a single pixel may occur thousands of times in a CCD.

It is anticipated that CMOS will become the standard image sensor technology for space deployment in the near future. It is also possible that CMOS will replace CCDs as the highest performance scientific sensor for space. This is expected to happen as a result of both the decline of CCD manufacturing capability and the continual development of the CMOS state-of-the-art.

CMOS in general has proved to be a very versatile technology. Globally there is a great deal of design experience available in producing high speed, highly integrated digital circuits, as well as high performance analogue Integrated Circuits (ICs), and combinations of the two. The interchangeability of these designs between fields means a function such as imaging, that can be implemented in CMOS, can be developed to market quickly.

CMOS image sensors have therefore brought with them features that were not readily available on CCDs, such as on-board Analogue to Digital Converters (ADCs), clock generators, memory and image processing. In the mean-time, the performance of CMOS pixels and camera systems have improved to the point where they are competitive against CCDs in all but a few specialised applications. Recently, some devices have been produced which use a CCD charge transfer architecture but are produced on modern CMOS processes.

This thesis addresses two issues related to using CMOS image sensors in the space ra-

radiation environment. Firstly, how proton irradiation affects the performance of CCD-on-CMOS devices and how this compares to the well understood effects on classical CCDs. Secondly, whether the possibility of single event latchup (a potentially catastrophic device failure mechanism) can be reduced in CMOS circuits by fabrication process modifications and how susceptibility to single event latchup can be modelled successfully.

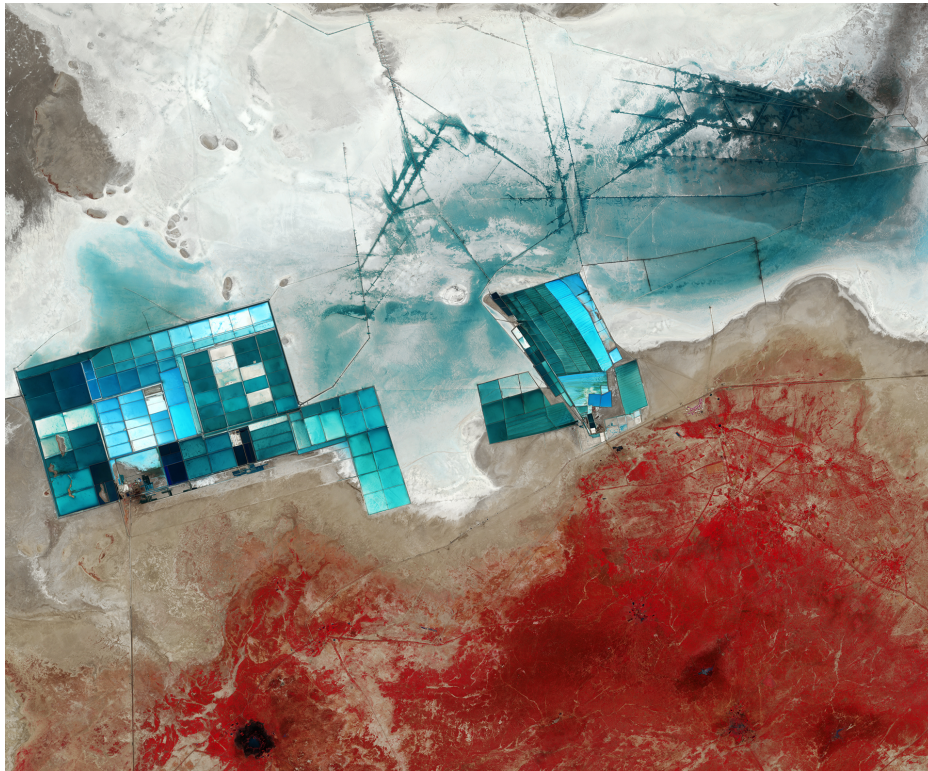


Figure 1.1: False colour image of the Rann of Kutch salt marshes in western India. Captured by the ESA Sentinel-2A satellite CMOS multi-spectral imager. The width of the pond cluster on the left is nearly 13 km. Photo credit: ESA

Thesis organisation

Chapter 2 contains an introduction to the silicon image sensors. The CCD and APS architectures and their performance are described. Noise sources affecting performance are also discussed.

Chapter 3 describes the space radiation environment and the effects of radiation on sili-

con image sensors.

Chapter 4 contains the first experimental work in this thesis. The work aims to establish the effects of high energy proton damage on CCD-on-CMOS devices. As in standard scientific CCDs, the efficiency of charge transfer between pixels is decreased after irradiation. Dark signal is also increased. Both effects are thought to occur in CCD-on-CMOS devices due to the same phenomena seen in standard CCDs. Comparing the effects of proton irradiation on each technology allows CCD-on-CMOS designers to use well established CCD methods to mitigate the effects of the space radiation environment at both the design and operation stages. An attractive application of CCD-on-CMOS is in small array size, room temperature, slow pixel rate Time Delay and Integration (TDI) devices for Earth observation. Results of proton damage on such a device are presented. A simulation of charge transfer using models originally developed for CCDs is also presented.

Chapter 5 describes an experiment to further the understanding of the susceptibility to single event latchup of CMOS APS devices. CMOS is potentially susceptible to single event effects when operated in the space radiation environment. This is an unwanted side effect of the features afforded by CMOS technology on image sensor devices. Single event effects generally do not occur in the CMOS image sensor pixel itself. The effects seen in CMOS image sensor circuitry are generally either errors in digital data or the more dangerous latchup, which effectively short circuits the device's power supply. Single event effects are so called because they can occur due to a single high energy particle interacting with the device, unlike cumulative effects. In this chapter, the occurrence of latchup in an APS during irradiation with heavy ions is measured. Measurements are made on devices with process variations to introduce deep doping wells in the device silicon and to modify the epitaxial layer thickness.

Chapter 6 describes a simulation of the latchup phenomenon in a CMOS circuit as found in a CMOS APS. The availability of both n and p channel Metal Oxide Semiconductor Field

Effect Transistors (MOSFETs) on the CMOS process is taken advantage of in the peripheral on-chip circuitry of CMOS sensors. The presence of both kinds of MOSFETs, without suitable hardening and the associated performance penalties, creates a risk of device malfunction in the presence of ionising radiation. In this chapter, new approach is developed for taking a relatively simple device model and particle interaction simulation, using TCAD (Technology Computer Aided Design) and using the simulation outcome to predict the actual performance of a full device.

Chapter 7 contains conclusions and further work arising from this thesis.

Chapter 2

Silicon image sensors

2.1 The charge coupled device

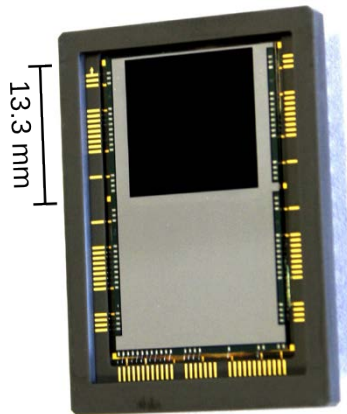


Figure 2.1: The e2v CCD201.

The CCD was invented in 1969 by Boyle and Smith of Bell Telephone Laboratories [1]. Boyle and Smith were awarded the Nobel prize for physics in 2009 for their work on CCDs. The application to imaging was first realised by Tompsett et al. in 1970 [2]. Tompsett received the 2010 National Medal of Technology and Innovation and the 2012 IEEE Edison Medal for his work. A comprehensive early history of the CCD can be found in Janesick [3]. An example of a CCD is shown in Figure 2.1.

The CCD greatly enhanced the field of electronic imaging, becoming the standard in television cameras, and led to the development of the digital still camera [4]. The CCD has also been extremely valuable in scientific imaging applications, including use in space, such as the Hubble Space Telescope [5].

Until recently, the CCD dominated the electronic imaging market with applications in scientific, medical and industrial imaging as well as consumer products.

2.2 CMOS image sensors

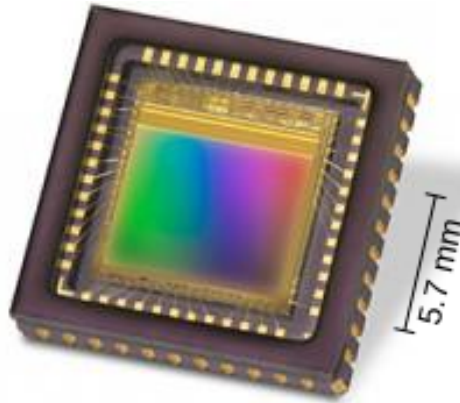


Figure 2.2: The e2v Sapphire APS used in Chapter 5.

Since the early 1990s CMOS Image Sensors (CIS) (see Figure 2.2) have undergone rapid development. The Active Pixel Sensor (APS) was first developed in the late 1960s in order to improve the performance of what are now known as passive pixel sensors. Passive pixel sensors consist of an array of pixels in which light is converted to charge. A switch then connects pixels to an output in turn to measure charge. Passive pixels are slow, noisy and have limited scalability. The APS alleviates these problems by incorporating a dedicated amplifier into each pixel. To achieve this on a chip requires a high level of integration. Therefore, designers of APSs have favoured small feature size CMOS processes, where the level of integration has rapidly increased following Moore's law [6]. CIS feature sizes are

typically $0.18\ \mu\text{m}$, but many sensors are now produced in 65 nm [7] technology or smaller.

While CCDs still offer superior performance in some respects, the APS is now ubiquitous in low cost, low power consumer imaging with over 2 billion chips sold in 2011 [8].

2.3 Use of solid state imaging in space

CCDs have historically dominated space imaging since replacing vidicon. Despite the complexity and high power consumption of a CCD system compared to the CIS, their performance in scientific applications still makes them worthwhile. CISs are only just catching up with the low noise performance of CCDs [9].

One of the main challenges to operating image sensors in space is the space radiation environment. The radiation hardness of CCDs (compared to film) was one of the reasons for their adoption on early space missions [3]. Film becomes exposed when subjected to radiation, as do CCDs. However, the signal in a CCD can be cleared upon readout whereas the image on film is permanent. It is still the long term damage to the CCD structure from exposure to radiation which limits the useful life of CCDs in space. APSs are, in some respects, considered to be more tolerant of radiation damage. Radiation damage to CCDs reduces the Charge Transfer Efficiency (CTE) between pixels. CTE degradation typically leads to the smearing of image features as charge is trapped temporarily while being transferred through damaged pixels (see Figure 2.3). APSs suffer a lot less from this problem, since charge is read directly from each pixel. The fabrication processes used in CMOS also increase the tolerance of APS to ionising radiation effects in the oxide, since a thinner oxide layer is used, but introduce new problems, such as single event latchup. Radiation damage in both kinds of sensor is covered in Chapter 3.

Applications for image sensors in space can be split into three categories as follows.

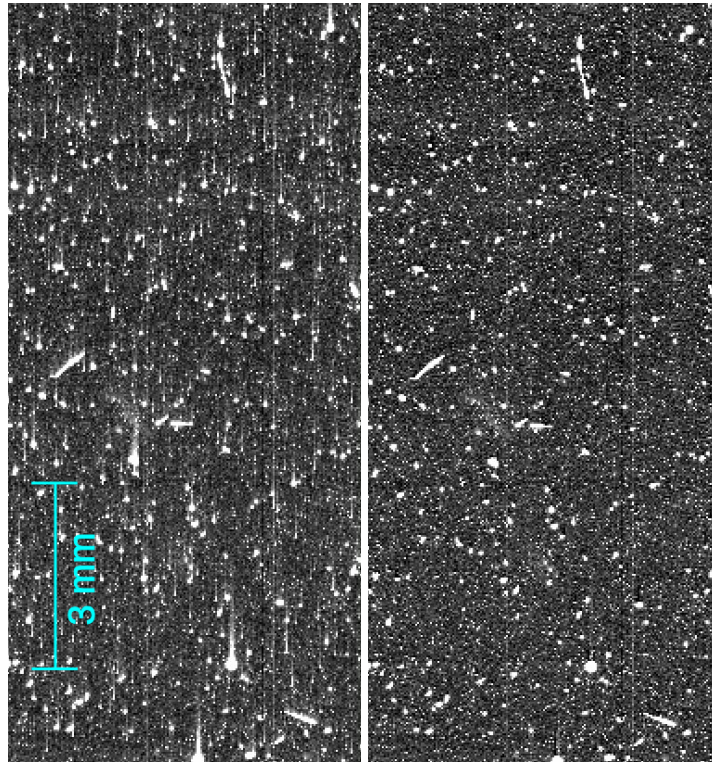


Figure 2.3: Charge smearing in a CCD on the Hubble space telescope arising from incomplete charge transfer due to radiation damage (left) and the corrected image (right) [10].

2.3.1 Astronomy

Astronomy applications are characterised by high dynamic range requirements, given the range of source brightnesses. To achieve this, and to image faint sources, low noise is crucial. For high dynamic range, a large Full Well Capacity (FWC) is also required. The CCD has superior performance in both of these areas. Space-based astronomy started in earnest with the Hubble Space Telescope (HST) [10]. The noise performance of the HST is just a few electrons [11].

Low noise is also important in X-ray astronomy and spectroscopy missions, such as XMM-Newton [12]. The thicker depletion depth of CCDs also gives them greater X-ray sensitivity than CISs.

The latest astronomy missions, such as Gaia which will map the positions of more than 1 billion stars in the Milky Way, are still using CCDs [13] (The Gaia focal plane has 106

CCDs). Future missions, Euclid [14] for example which aims to measure weak gravitational lensing, continue to stretch the performance requirements placed on CCDs.

2.3.2 Surface observation

The surfaces of planets or moons, observed from orbit or fly-past, are typically brighter than stars. In these applications, spacecraft motion limits the useful exposure time of image sensors. Consequently, the dynamic range and noise requirements of these sensors are less demanding, allowing CISs to gain market share. The Voyager spacecrafts used vidicon, a cathode ray tube system where the scene is imaged on a photoconductive surface which is scanned with a focused electron beam. The voltage produced on the surface forms the video signal [15]. The JANUS instrument on the JUICE mission [16] will use a CIS in its fly-pasts of Jupiter and its icy moons.

For Earth observation CCDs are still popular, for example the ESA Pleiades satellites [17]. ESA's Sentinel 2 constellation uses multi-spectral CMOS imaging [18]. Earth observation from Cube-Sats, using CISs, has also been reported [19].

2.3.3 Functional imaging

Image sensors are also used to support spacecraft whose primary purpose is not imaging (communication satellites for example). Star trackers, such as the HAS2 [20] and star250 [21] CISs are used for determining a spacecraft's orientation. Low cost is a major requirement for these sensors, as well as low mass and volume of the instrument for which smaller pixels are favourable. The radiation tolerance of sensors used in star trackers is important. Especially if image processing and attitude detection is performed onboard, the algorithms must be able to continue functioning even after performance has been degraded over several years. The dynamic range requirements of these sensors vary depending on the number of stars being tracked, typically fewer than 100 of the brightest stars and increasing if more

accuracy is required.

Rovers also require information about their surroundings for navigation. The Mars curiosity rover is using CCDs [22]. A CIS is currently planned for the PanCam instrument on the ExoMars rover launch in 2020 [23]

2.4 CCD operation

The CCD is an array of photosensitive pixels. Light falling on a pixel generates free charge carriers. This charge is then moved through the device from pixel-to-pixel until it reaches the readout node. At the readout node, the charge is converted to a voltage signal which can be used to reconstruct the image. The schematic of typical CCD is shown in Figure 2.4. The operation of the CCD is covered in the following sections.

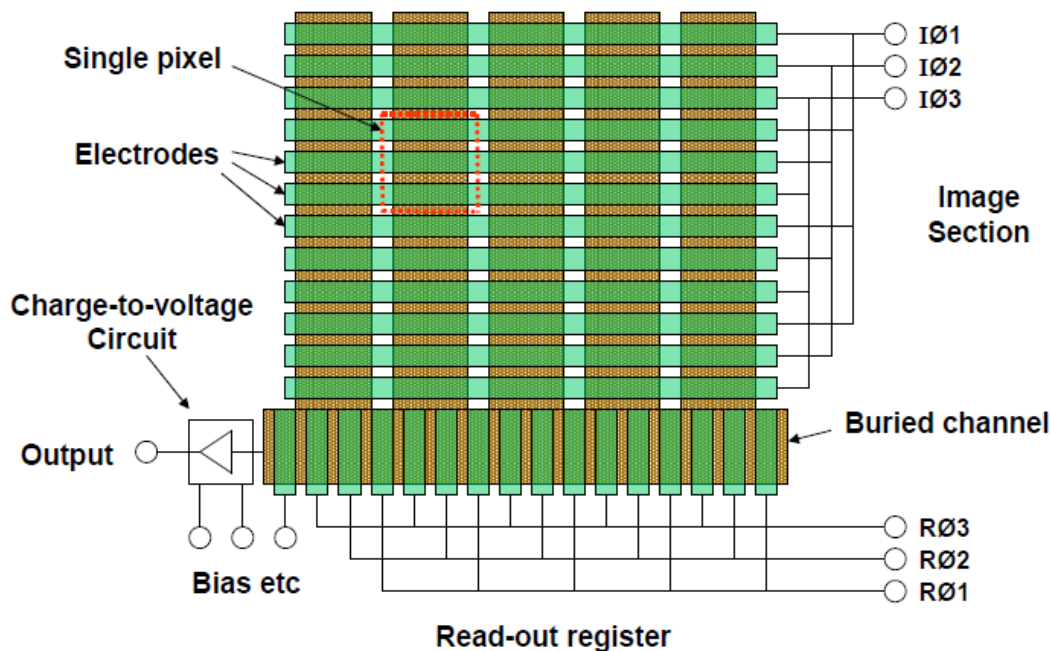


Figure 2.4: Schematic of a full-frame CCD. [24]

2.4.1 Charge collection and storage

Photons incident on the CCD silicon generate electron-hole (e-h) pairs. According to the photoelectric effect, in order for a photon to excite an electron from the valance band into the conduction band, leaving a hole in the valance band, it must have an energy of $E \geq E_g$, where E_g is the band gap energy which in silicon is ≈ 1.1 eV. The energy of a photon is given by

$$E = h\nu \quad (2.1)$$

where ν is the photon frequency and h is Planck's constant.

The majority of CCDs produced are n-channel. In an n-channel CCD, it is the photo-generated electrons which are collected in the pixel. Charge collection is determined by the potential structure inside the pixel. Pixels are defined by two or more "phases" (or gates) in the column direction. A buried-channel CCD has an implant (n-type in n-channel) under the oxide so that charge collects further below the oxide, away from the Si-SiO₂ surface.

Figure 2.5 shows the potential structure under a typical buried-channel CCD phase for high and low clock voltage, and at high clock voltage after the accumulation of charge up to Full Well Capacity (FWC). The FWC is the maximum number of electrons that a pixel can usefully measure. FWC can be increased by changing the pixel potentials (either by doping or by using a higher clock voltage) or by increasing the pixel area. A typical CCD FWC is around 200 ke^- [26].

During integration of electrons, the gates of these phases are biased such that one or more phases per pixel act as a barrier preventing transfer of electrons from one pixel the next (see Figure 2.6). A channel-stop (which in buried channel CCDs may simply be an absence of buried channel) between adjacent columns prevents parasitic charge transfer between columns.

The field within the pixel (normal to the image plane) can be determined from Poisson's

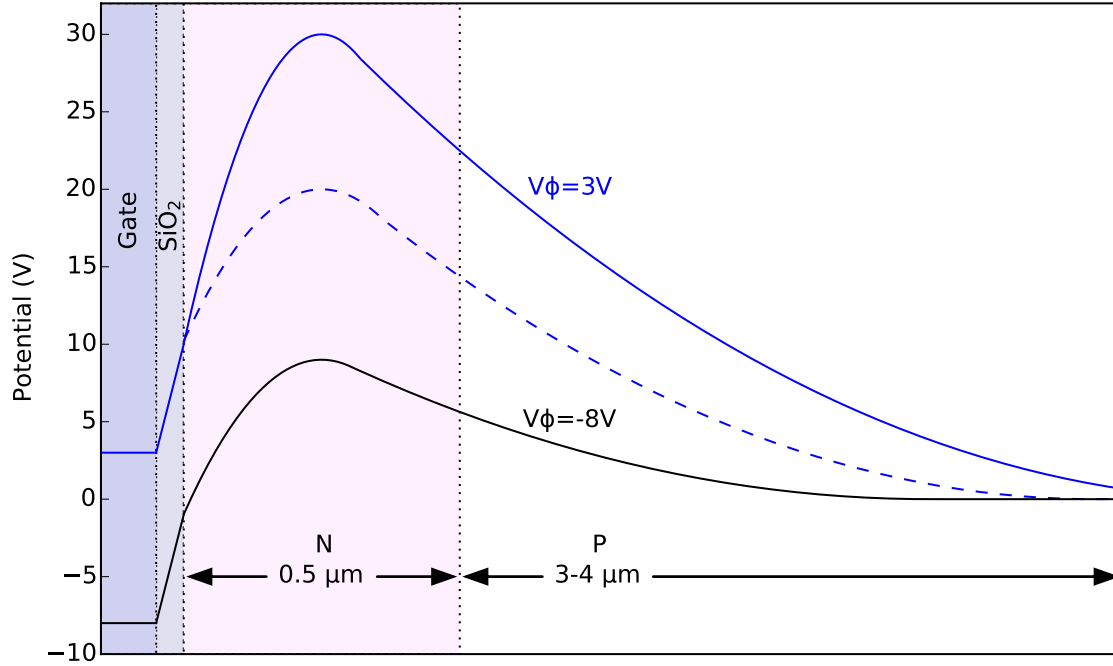


Figure 2.5: The potential structure in a typical buried-channel CCD in inverted mode [25] [3]. The potential is shown for clock high at $V\phi=3$ V and clock low at $V\phi=-8$ V. Accumulation of electrons reduces the potential in the channel (shown by the dashed line) until the onset of saturation where no more charge can be collected.

equation

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon} \quad (2.2)$$

where x is the distance into the substrate, V is the potential, ρ is the charge density and ϵ is the dielectric permittivity of the material.

The onset of full well can occur when the potential in the storage phase has reduced to the point that further electrons will not be confined within the pixel by the potential structure and will instead join the signal charge in adjacent pixels. This is known as bloomed full well. Blooming can be avoided at the expense of useful pixel area and FWC adding an anti-blooming drain to the pixel (examples can be found in [3, pg. 301]). Alternatively, surface full well can occur first, whereby the size of the charge cloud containing the signal electrons expands to the point where electrons start to become trapped temporarily at the

Si-SiO² interface.

2.4.2 Charge transfer

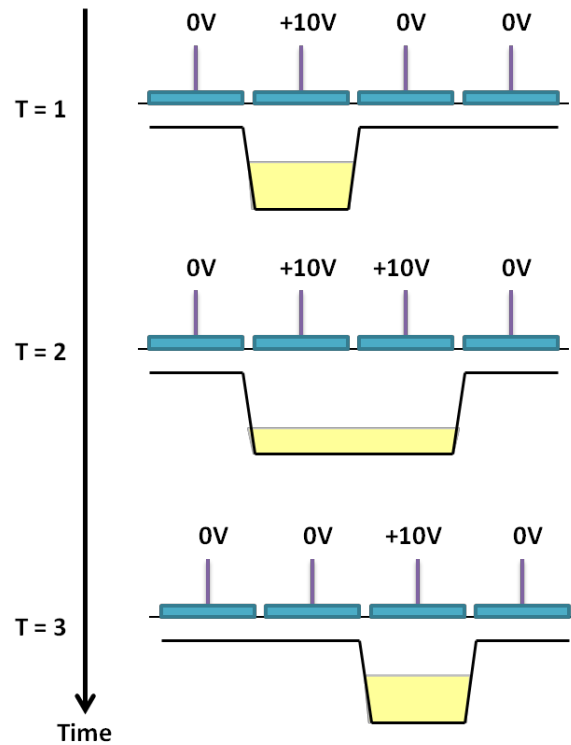


Figure 2.6: Typical clocking scheme for a three phase CCD.

Photo-generated charge is collected in-pixel under one or more storage phases. At the end of the integration period, the collected charge is transferred towards an output node. The transfer scheme is arranged so that charge packets arrive sequentially at the output node for measurement. The simplest scheme is to transfer vertically in the column direction (through the parallel register). Charge at the bottom of the parallel register is then transferred onto a serial register which transfers the charge horizontally (see Figure 2.4). A typical three-phase clocking scheme, which could be applied to either the parallel or serial register, is shown in Figure 2.6.

During the read-out process, pixels are still exposed to light. Once readout has begun,

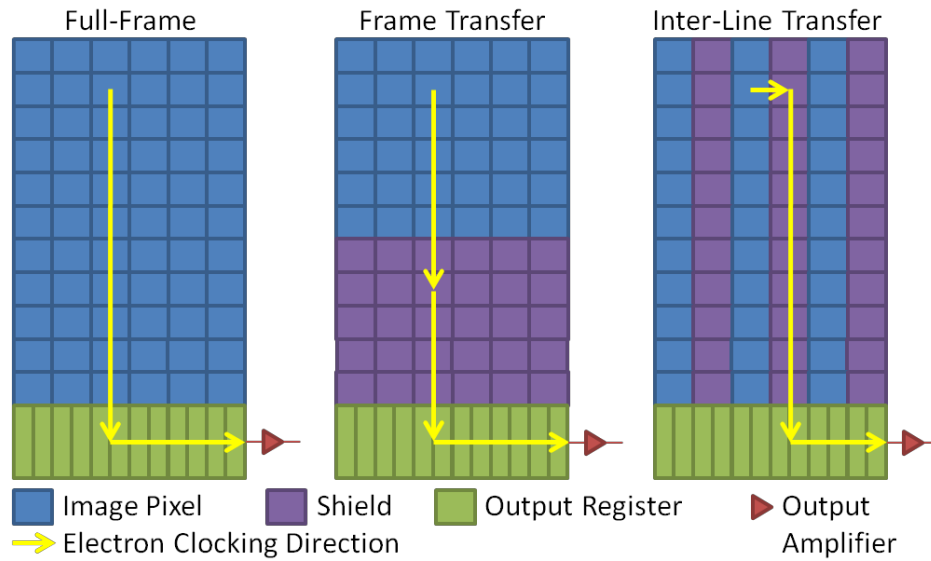


Figure 2.7: Full frame, frame transfer, and inter-line transfer readout styles

the location of signal charge is shifted, so any additional signal will be spatially distorted when the image is reconstructed. Three common CCD architectures with differing readout schemes are shown in Figure 2.7. The simplest is the full-frame architecture. In the frame-transfer architecture, charge is transferred from an exposed "image" region vertically into a covered "store" region of equal size. This can be performed quickly without clocking the serial register, which would otherwise act as a bottleneck on the transfer speed. Once charge is in the store region readout can continue as in the full-frame CCD but without any further signal being produced. The frame-transfer CCD requires an approximate doubling of device area. The inter-line transfer architecture uses the first charge transfer step to move charge one step horizontally into shielded parallel registers which prevents further exposure. This again requires increased area but also halves the light sensitive area of the focal plane. Furthermore, unless the pixel dimensions are compressed horizontally, the image aspect ratio will be altered.

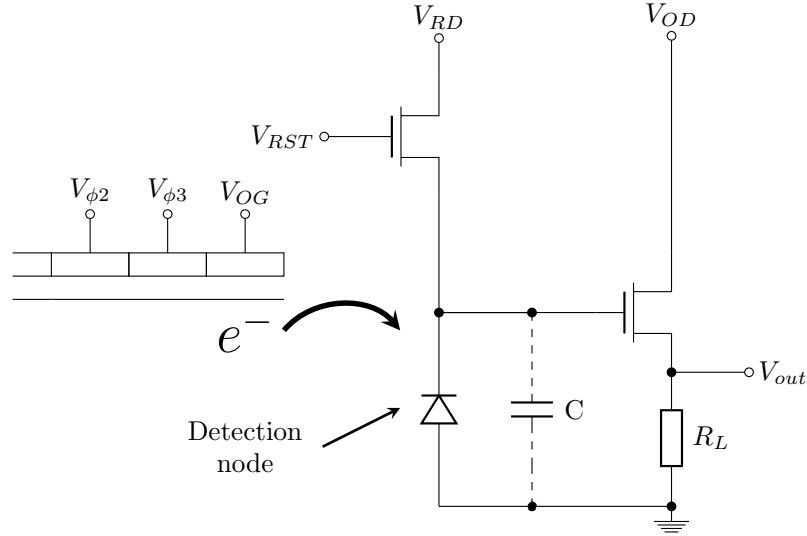


Figure 2.8: Typical CCD output amplifier

2.4.3 Charge measurement

A typical CCD output circuit is shown in Figure 2.8. The output gate voltage V_{OG} is biased appropriately, so that charge arriving under the last serial register phase is transferred onto the detection node. The detection node capacitance determines the sensitivity of the sensor. The output voltage change for a signal change of n electrons is

$$\Delta V = \frac{qn}{C} \quad (2.3)$$

where q is the elementary charge, and C is the detection node capacitance. The Charge to Voltage Factor (CVF) of the sensor is given by

$$CVF \equiv \frac{\Delta V}{\Delta n} = \frac{Gq}{C} \quad (2.4)$$

where G is the output buffer amplifier gain. The output buffer amplifier is usually a source-follower MOSFET biased to the output drain voltage V_{OD} , with a load resistor R_L located off-chip. Once charge has been measured, the reset gate voltage V_{RST} is clocked high to

empty electrons from the detection node through a MOSFET to the reset drain voltage V_{RD} .

2.5 MOSFET

MOSFETs can be produced on both CCD and CMOS processes. One of the main advantages of CMOS is the small feature sizes available, as well as the availability of both p-channel and n-channel MOSFETs on the same device. This allows a very high density of MOSFETs and subsequently many thousands of devices on a single chip. The cross section of an n-channel MOSFET is shown in Figure 2.9. The source, gate, drain and body voltages are denoted V_S , V_G , V_D and V_B respectively.

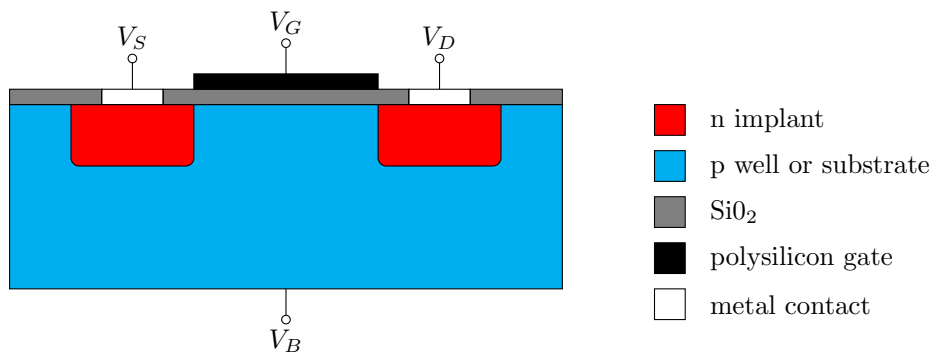


Figure 2.9: Cross section of an n-channel MOSFET.

Functions such as ADCs, clock generation, and image processing can all be performed on chip if desired, as well as the in-pixel transistors and the peripheral circuitry required for the APS. Because of the importance of the MOSFET, and to highlight its versatility, MOSFET operation is described here. The MOSFET has three modes of operation as follows.

Sub-threshold ($V_{GS} < V_{th}$)

For a gate to source voltage V_{GS} below the threshold voltage V_{th} the I-V relationship resembles a forward-biased diode and is approximately

$$I_{DS} = I_{DS0} e^{\left(\frac{V_{GS} - V_{th}}{nV_T} \right)} \quad (2.5)$$

where I_{DS0} and n are constants and $V_T = kT/q$ is the thermal voltage.

Linear ($V_{GS} > V_{th}$, $V_{DS} < V_{GS} - V_{th}$)

In the linear mode, the drain-source current is approximately

$$I_{DS} = \beta \left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (2.6)$$

where $\beta = \mu C_{ox} \frac{W}{L}$ and μ is the carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area and W and L are the transistor width and length respectively.

The name “linear mode” is due to the fact that I_{DS} has a linear dependency on V_{GS} . The source and drain terminals have ohmic characteristics, i.e. the MOSFET can be used as a resistor. This mode is used for switching applications.

Saturation ($V_{GS} > V_{th}$, $V_{DS} \geq V_{GS} - V_{th}$)

In saturation I_{DS} is mainly determined by V_{GS} and is approximated as (neglecting channel-length modulation)

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_{th})^2 \quad (2.7)$$

This mode is the most widely used for amplification applications. For small signals, the

MOSFET biased in saturation is a voltage controlled current source with transconductance

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{2I_{DS}}{V_{GS} - V_{th}} \quad (2.8)$$

The electrical characteristics of an n-channel MOSFET are shown in Figure 2.10.

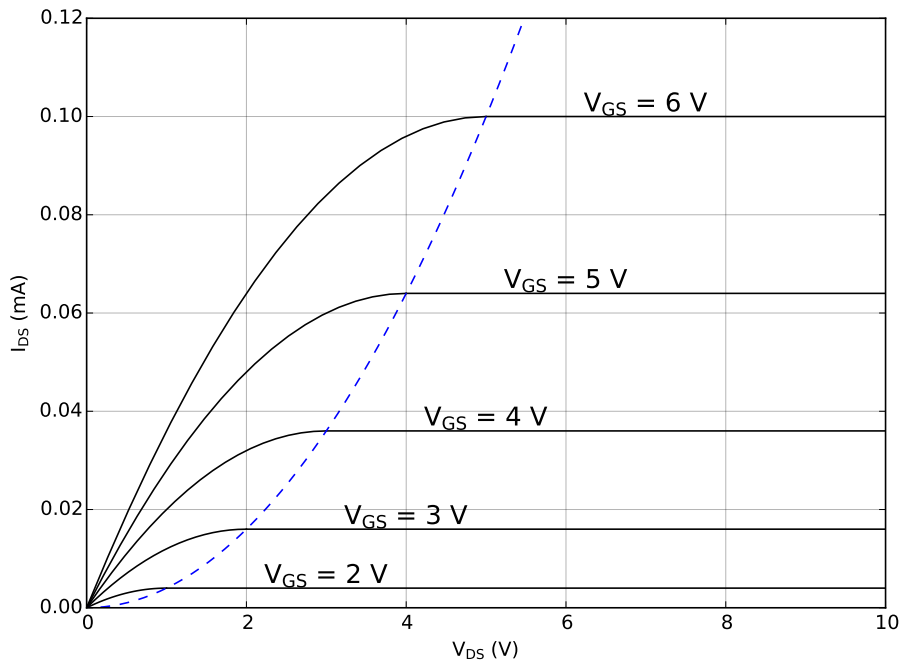


Figure 2.10: Typical N-channel MOSFET electrical characteristics. The dashed line shows the boundary between the linear and saturation regions.

2.5.1 Source follower

The MOSFET source follower is MOSFET biased with a constant bias current I_{DS} . Input is to the gate and output is at the source. The source follower is a high impedance buffer used as the first stage of the charge measurement circuit in both the CCD and APS.

Assuming constant I_{DS} , the output is

$$V_{out} = V_{in} - V_{th} - \sqrt{\frac{2I_{DS}}{\beta}} \quad (2.9)$$

Variation in threshold voltage between source follower transistors across pixels causes a significant amount of fixed pattern noise by adding a signal offset. This effect isn't seen in CCDs, as the source follower is shared between pixels.

2.6 APS operation

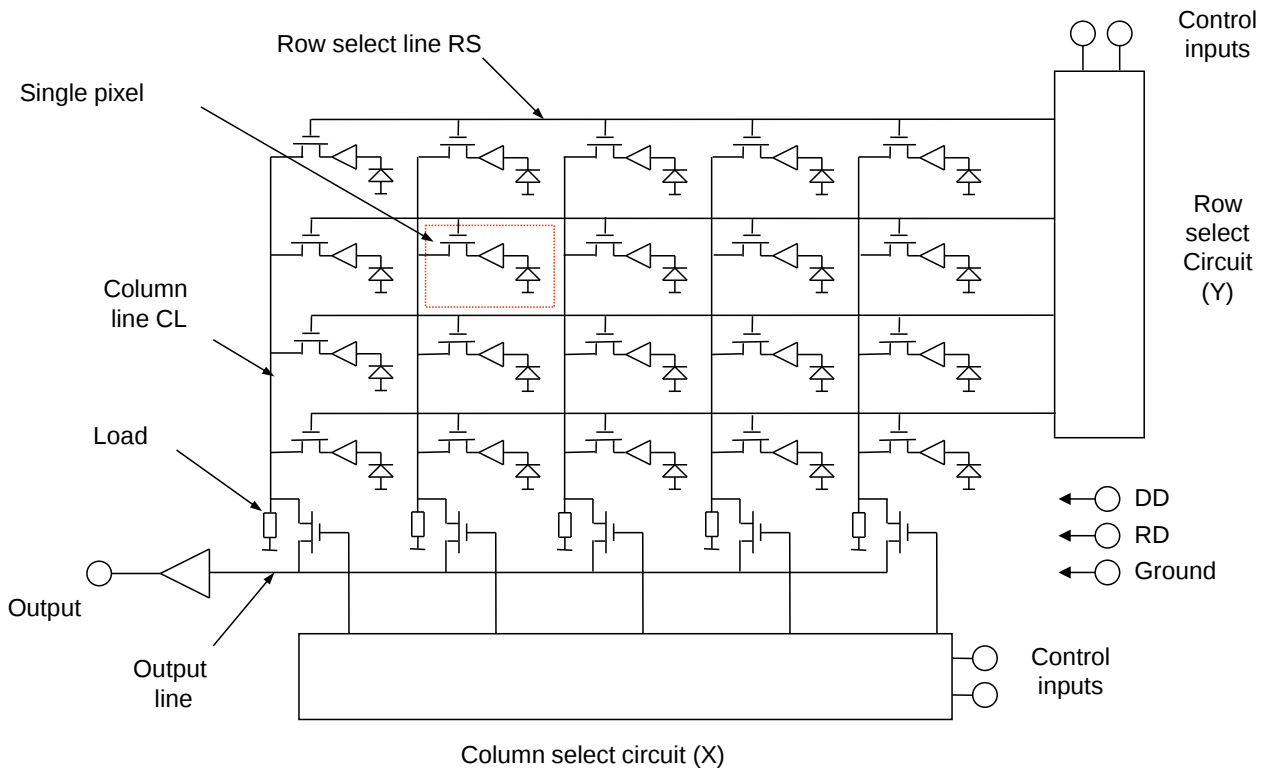


Figure 2.11: APS operation

The CMOS APS is also composed of an array of pixels, the main difference compared to a CCD being that each pixel contains within it a charge-to-voltage amplifier (see Figure 2.11). Pixel sizes for scientific devices can be comparable to CCD pixel sizes of $5 - 15 \mu\text{m}$, whereas consumer device pixels can be as small as $1 \mu\text{m}$ [27]. Photogenerated electrons collect in a photodiode in each pixel and remain there until a reset gate is pulsed. The output from each pixel is addressed using row and column select signals. These signals control MOSFET switches which connect individual pixels in turn to a common output line

and output buffer.

In the simplest APS pixel, there is no charge transfer before readout, however more sophisticated pixels (e.g. 4T and 5T covered in Sections 2.6.2 and 2.6.3) require charge transfer. One of the major potential advantages of the APS over CCDs is that charge transfer only occurs once for each pixel at read out.

2.6.1 3T pixel operation

Figure 2.12 shows the basic 3 Transistor (3T) APS circuit. Photogenerated electrons collect on the photodiode which reduces the voltage measured at the gate of the source-follower M_{SF} . The voltage on the photodiode can be measured at any time on the column bus by setting RS (row select) high. The column is selected by a multiplexer outside of the pixel array. Typical CVF is around $7 \mu\text{V}/e^-$ [28] or greater. The pixel is reset by setting RST high to remove the electrons, bringing the voltage on the photodiode back to V_{RS} .

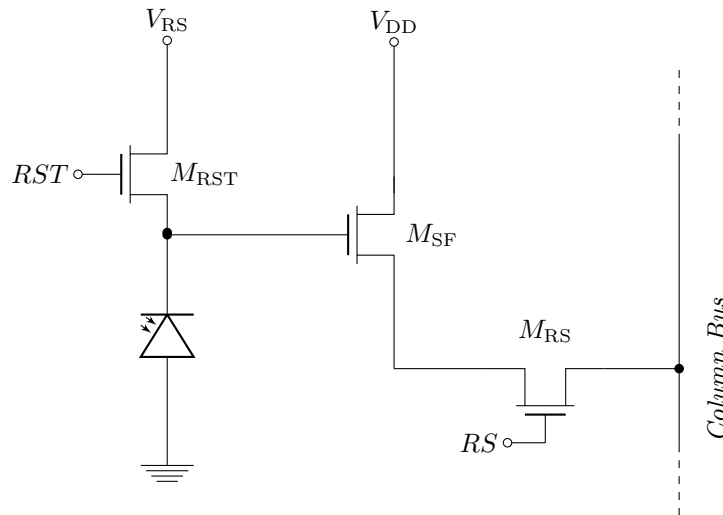


Figure 2.12: 3T pixel electronics

The advantage of the 3T pixel is its simplicity. A lower number of transistors takes up less space and means that a higher proportion of the pixel area can be made photoactive. The percentage of the pixel area which is photosensitive is called the fill factor.

The main limitation with the 3T pixel array is that integration (i.e. the collection of light and conversion to measurable charge) starts and ends at reset. Since reset occurs at different times for different pixels this causes what is known as the rolling shutter effect, whereby different parts of scene will be captured at different times. This can cause significant distortion when capturing a scene with moving objects.

The 3T pixel also suffers from lag, whereby the photodiode is not completely reset. This results in a ghost image when a bright frame is followed by a dark one. Furthermore, correlated double sampling (see Section 2.8.3) cannot be properly used to reduce the effect of reset noise. Non-linearity in 3T pixels can also be high, up to 200%. in some cases [29].

2.6.2 4T pixel operation

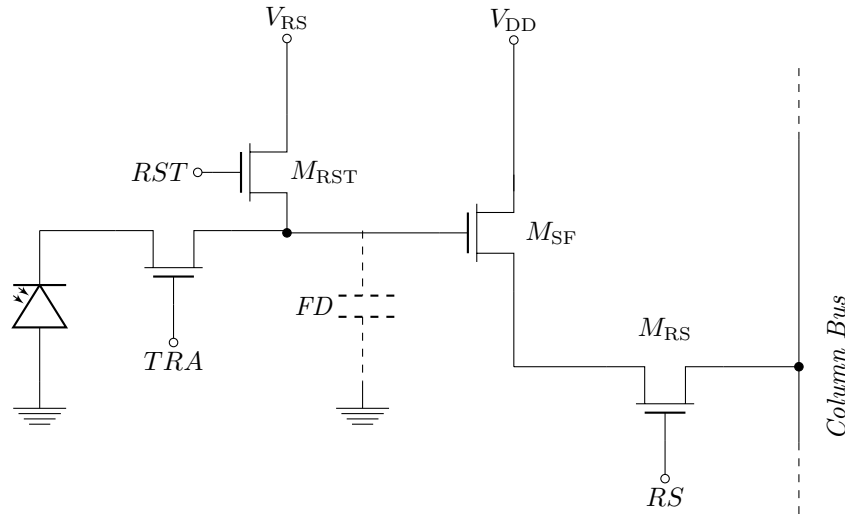


Figure 2.13: 4T pixel electronics

The 4T pixel incorporates a Pinned PhotoDiode (PPD). The PPD was invented to reduce lag in inter-line transfer CCDs [30] and uses a p+ implant at the surface of the photodiode. Pinning the surface of the photodiode greatly reduces dark current produced at the Si-SiO₂ interface. A transfer gate is required to hold charge on the photodiode during integration and then move charge onto a separate floating diffusion at readout. The higher potential

of the floating diffusion relative to the photodiode results in complete charge transfer and therefore reduced lag.

The 4T pixel circuit is shown in figure 2.13. The transfer gate allows integration to be interrupted in all pixels simultaneously by transferring charge to the floating diffusion. Furthermore, the floating diffusion can be made to have a far smaller capacitance than the photodiode. The reduction in capacitance increases the sensitivity over the 3T. CDS can be used on the 4T with resulting read noise levels below $1 e^-$ r.m.s. reported under some circumstances [9] and commercial devices regularly achieving $<3 e^-$ r.m.s. [8].

2.6.3 5T pixel operation

In the 4T, the photodiode voltage is reset upon transfer of charge to the floating diffusion which is usually done just before pixel readout. Integration continues immediately after transfer. The 5T, by using an extra transistor as shown in Figure 2.14 can hold the photodiode at V_{RS} until the entire pixel array has been read out. Integration can then be started (by setting GS low) and then stopped (by pulsing TRA high then holding GS high) at the same time in each pixel in the array. This ability is known as global shutter [31].

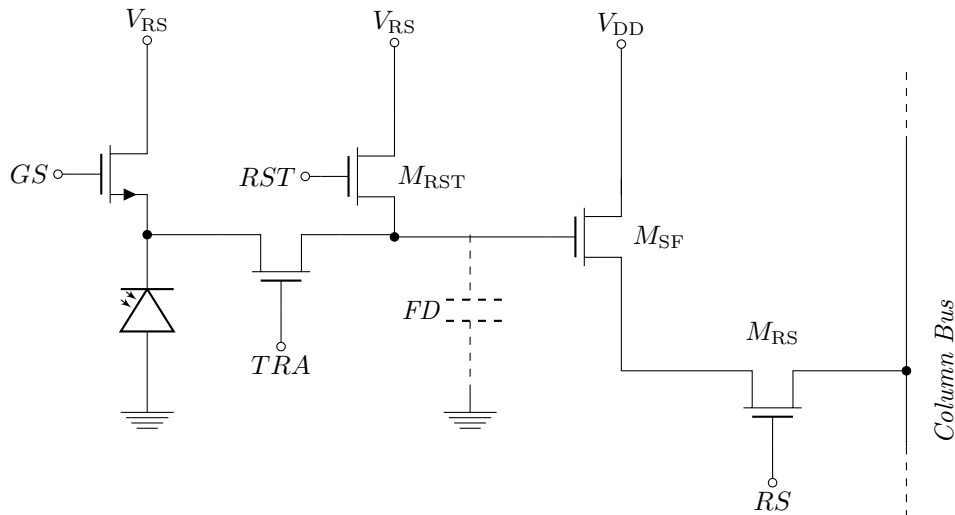


Figure 2.14: 5T pixel electronics

2.7 Quantum efficiency

Not all photons incident on the CCD will produce a free electron, and not all free electrons produced will be collected. The absorption depth for photons incident on silicon is wavelength dependent. Quantum Efficiency (QE) is the probability of an incident photon producing an electronic signal.

The QE for a certain wavelength is largely determined by the absorption length. Short wavelength light (i.e. blue) will tend to be absorbed after a very short distance. In Front-Illuminated (FI) CCDs, a significant number electrons are collected before the depletion region (in the gate polysilicon or gate oxide), especially at short wavelengths. Long wavelength light is likely to be absorbed in the field-free region or the substrate, below the depletion depth. Electrons created here are more likely to recombine with holes. The same is true in CMOS sensors, with an additional loss of QE due to the fact that much of the pixel area is covered with opaque metallisation.

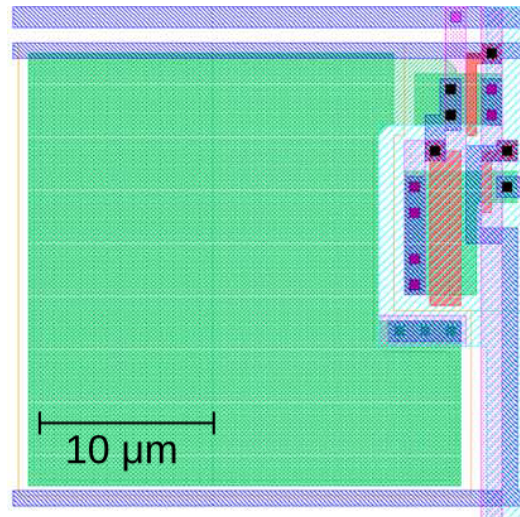


Figure 2.15: Layout of a 3T pixel designed by Murari et al. [32].

Figure 2.15 shows the layout of a 3T pixel designed by Murari et al. [32]. On the right hand side of the pixel are the 3 transistors. The fill factor in CMOS sensors can be less than 50%. The space taken up by in-pixel transistors and connections becomes more of a

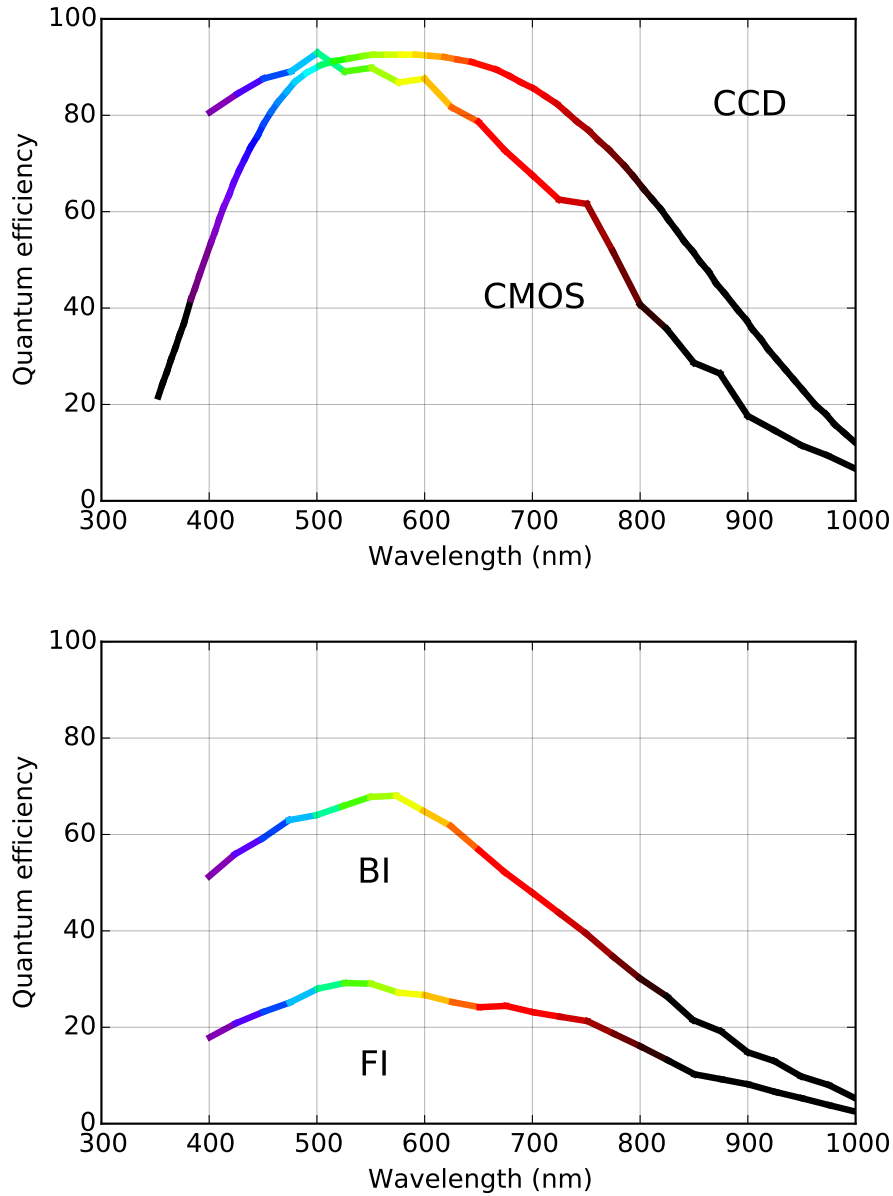


Figure 2.16: Top: Quantum efficiency of the back-illuminated, AR coated, e2v CCD91 developed for use on Gaia [33] compared with a back-illuminated, AR coated CMOS image sensor produced by the Jet Propulsion Laboratory [34]. Bottom: The same CMOS image sensor, front and back illuminated, without AR coating.

problem as the pixel size shrinks. Backside-Illumination (BI) [35] avoids this problem, but requires back-thinning (i.e. thinning of the substrate down to a few tens of microns) to be effective. BI CMOS sensors are now standard in many consumer applications. BI CCDs

are also used when QE needs to be maximised. A further improvement to QE is made by the using an Anti-Reflective (AR) coating, generally a coating with a refractive index of the geometric mean of the indices of silicon and air. Typical QE measurements for a CCD and a CMOS sensor with AR coating, and for an uncoated CMOS sensor, are shown in Figure 2.16.

2.8 Noise sources

2.8.1 Dark current

Not all electrons collected are produced by photons incident on the device. So called "dark signal" is formed from thermally generated electrons produced in defects in the bulk silicon and at the Si-SiO₂ interface. Dark current in a 5T CIS pixel is typically 10 nA cm⁻² at room temperature [36]. The fact that dark current varies from pixel-to-pixel is described by Dark Signal Non-Uniformity (DSNU) which is usually around 1% in both CCDs and CIS devices [11].

2.8.2 Fixed pattern noise and pixel response non-uniformity

Fixed pattern noise is a measure of the variation in measured signal in pixels on the same device when exposed to the same light level. This is a result of variations in sensitivity (the pixel response non-uniformity or PRNU) and variations in signal offset (caused by variations in flatband voltage).

2.8.3 Reset noise

Resetting of the photodiode (3T) or floating diffusion (4T, 5T, CCD output) adds noise. The variance in added signal, in electrons, is

$$\sigma_{reset}^2 = \frac{kTC}{q} \quad (2.10)$$

[37] where k is Boltzmann's constant, T is the absolute temperature, q is the magnitude of electronic charge and C is the photodiode or floating diffusion capacitance. Reset noise can be reduced by first sampling after reset and then sampling the signal after charge has been transferred onto the floating diffusion. This process is called Correlated Double Sampling (CDS) [37]. Since both samples contain the reset noise contribution, subtracting the samples leaves only the signal. Reset noise can be brought below source follower noise levels (i.e. less than 1 e^- r.m.s. in CCDs) when using a clamp and sample ADC with sufficient capacitance. This is difficult to achieve in an on-chip ADC as found in CISs [36]. A typical raw value for reset noise at 200 K is 180 e^- [38].

2.8.4 Amplifier noise

The output transistor(s) also add noise (Johnson and shot noise). Electronics later in the signal chain such as buffer amplifiers and ADCs may also add significant amounts of noise. CCDs have the source-follower load, amplifiers and the ADC off chip. The off-chip amplifier can use large capacitors to reduce bandwidth and thus reduce noise, whereas this is not practical on CMOS devices [11]. The r.m.s. Johnson noise voltage on a resistance R is

$$v_n = \sqrt{4kTRB} \quad (2.11)$$

where k is Boltzmann's constant, and B is the system bandwidth.

2.8.5 Shot noise

Image sensors are used to measure source intensity, however this quantity is time-averaged. The actual rate of photon production is Poisson distributed. This statistical property of light (dark signal has the same statistical property) can be used to determine the sensitivity of an image sensor without a calibrated light source (see Section 4.3.5).

2.8.6 Flicker noise

Flicker noise [39], also known as $1/f$ noise particularly affects MOSFET amplifiers in CISs, as its magnitude increases with the reciprocal of the MOSFET size. It is understood to occur due to carrier mobility fluctuations or carrier number fluctuations. Flicker noise has a power spectral density with the form

$$S \approx n \frac{1}{f^\beta} \quad (2.12)$$

where n is a constant, f is frequency and β is a constant usually assumed to be unity.

2.8.7 Random telegraph signals

Random Telegraph Signals (RTS) are fluctuations in signal commonly observed in MOSFETs and CISs. The magnitude in CIS pixels affected by RTS is typically tens of electrons [29]. Characteristics of RTS behaviour are an output signal randomly fluctuating between two or more pseudo-stable values. The limiting sources of read noise in CCDs and CISs are RTS and flicker noise [9].

Chapter 3

Radiation effects in silicon image sensors operating in the space environment

The use of image sensors in space relies on the sensor being able to withstand the radiation environment in which it is operating. This chapter begins by discussing the three steps which must be followed to predict the performance of a CMOS image sensor in the space environment.

Firstly, the space radiation environment in which the sensor is bound to operate must be understood. The orbit or trajectory that a spacecraft will follow determines the quantity and type of radiation that it will encounter. The timing of the mission is also crucial. Radiation damage effects can be considered cumulative (dose rates and annealing times, however, are also factors) and the duration of the mission also determines the rate of destructive varieties of single event effects that can be tolerated. There are also transient radiation sources, such as solar storms, which must also be anticipated and accounted for. The space radiation environment is covered in Section 3.1.

Once the radiation environment is quantified, the next step is to understand the damage which the environment will impart on the image sensor. Practical radiation sources available for Earth testing use a small range of species and energies of particles, usually at elevated

dose rates. Equivalent doses must be used in order to simulate the damage done by the space environment. The limitations of Earth testing must be properly appreciated. Testing is usually divided into the basic mechanisms by which silicon image sensors are damaged by radiation: ionising damage; displacement damage; and the effects of single highly ionising particles. Predicting the exact damage mechanisms is still an active area of research, for example understanding the effect of the temperature profile of the sensor between irradiation and testing. The ways in which radiation causes damage in silicon sensors are discussed in Sections 3.2, 3.3 and 3.4

Finally, the performance of the sensors post-irradiation must be qualified. The effect of each kind of damage on the sensor performance and the physical processes that limit the post-irradiation performance should be understood. The effects of radiation on the performance of image sensors is introduced in Section 3.5.

Section 3.6 gives details of the way in which charge transfer efficiency is decreased by radiation damage in CCD style devices.

The remainder of the chapter in Section 3.7 then discusses effects in CMOS image sensors that are caused by single particles. In particular, the phenomenon of latchup, and how latchup can be prevented by design.

3.1 Space radiation environment

The space radiation environment can be categorised into transiting sources, such as solar radiation and cosmic rays, and trapped sources such radiation belts around Earth. The latter can be more easily avoided by choosing to operate a mission away from trapped sources.

3.1.1 Solar radiation

The outer layer of the Sun, known as the corona, consists of a plasma at over one million °C. The plasma is mostly formed from electrons, protons, and helium ions. Thermal turbulence within the plasma causes a continued ejection of these particles which is known as the solar wind. The solar wind has a cycle with a period of roughly 11 years. For 7 of these there is high activity and for 4 the activity is reduced [40]. The general composition of the solar wind is protons of energy less than 1 keV and electrons less than 100 eV. These result in a particle density of 10 cm^{-3} in the Earth's orbit. The Sun's magnetic poles produce a fast wind at around 800 km s^{-1} . The speed of particles ejected from the solar equator is slower, at around 400 km s^{-1} [41].

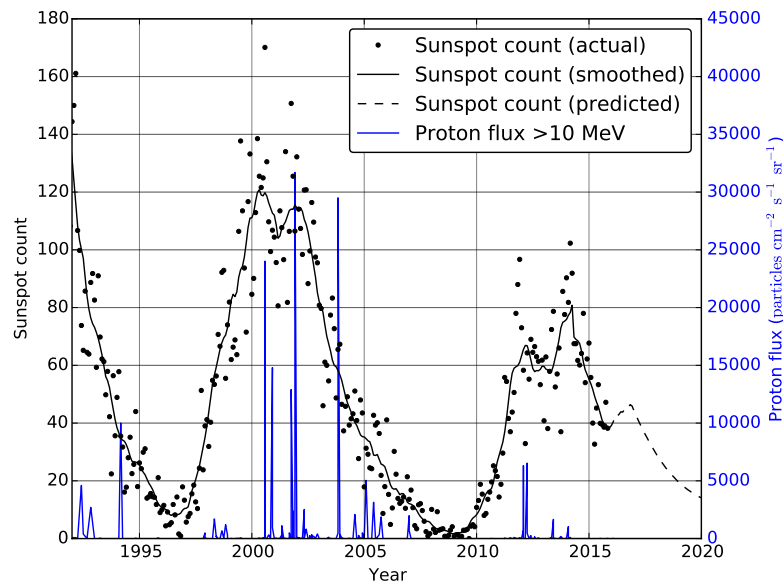


Figure 3.1: The sunspot count gives an indication of the level of solar activity. Radiation levels, measured here by the flux of protons with energies $>10 \text{ MeV}$, are increased during periods of high activity. The data plotted are from NOAA Space Environment Services Center [42] [43] [44].

Most solar wind particles do not have sufficient energy to penetrate beyond the coating of an image sensor and do not cause any damage. Solar storms, however, cause jets of high energy particles to be emitted into space and these can be very damaging. These

events result from the rearrangement of the sun's magnetic fields and are more likely during the high activity part of the solar cycle. Solar storms occur about 10 times per year, with extreme events once or twice per year. Solar storms produce jets of protons, heavy ions, and electrons. During extreme events protons with energy up to 20 GeV and electrons with 10s of MeV can be produced with particle fluxes as high as $10^{10} \text{ cm}^{-2} \text{ s}^{-1}$ [45]. Solar storms can be very damaging and are hard to shield against. A single solar flare has been known to produce a 10 MeV equivalent proton fluence of $8.5 \times 10^8 \text{ cm}^{-2}$ [46]. The sunspot count is a good indicator of solar activity. Sunspot counts since 1992 to the present day, and the predicted count until 2020, are shown in figure 3.1. Also shown is the recorded flux of protons with energies above 10 MeV in the same time period.

3.1.2 Cosmic rays

Cosmic rays (or galactic cosmic rays) are charged particles which originate outside of the solar system but within our galaxy. They have extremely high energies. The source of cosmic rays is believed to be the explosion of large stars at the end of their life (known as a supernova).

Cosmic rays consist of roughly 85% protons, 12.5% alpha particles, 1.5% electrons and 1% heavy ions (especially iron and nickel) [48]. Solar activity modulates the flux of particles with energy below 10 MeV. The flux of these particles is reduced during periods of increased solar activity and vice versa. Despite the relatively low flux of cosmic rays their extremely high energy means they can have serious consequences for electronic equipment and so cannot be overlooked. Figure 3.2 shows the flux of cosmic rays of energy above 100 MeV as observed by numerous experiments on Earth.

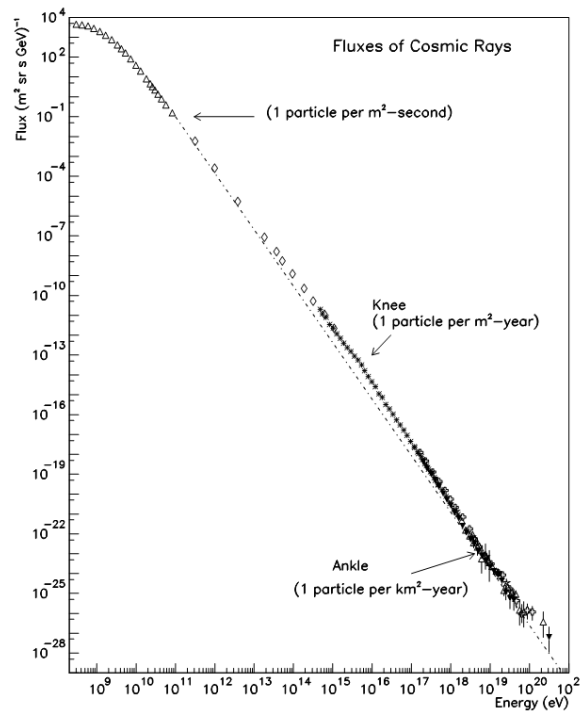


Figure 3.2: Cosmic rays can have extremely high energy which can cause damage to electronic components. These data are from various Earth based observations. Reproduced from Swordy [47].

3.1.3 Radiation belts

The Van Allen belts surround the Earth in toroidal regions of trapped charged energetic particles [49]. They are created by the Earth's magnetic field and populated with the constant flux of particles arriving in the Earth's vicinity. The Van Allen belts are formed of two distinct zones. The inner zone, at an altitude of 100 km to 5000 km traps high energy protons with energies of 100 MeV to 1000 MeV from the solar wind and cosmic rays. The outer zone is at an altitude of 20000 km to 36000 km and consists of electrons with energies below 5 MeV. Within these two zones the density of particles can vary significantly. The density also varies for a particular orbit depending on the position relative to the surface of the Earth.

Of particular importance is the South Atlantic Anomaly (SAA) which is a high density region affecting spacecraft in a low Earth orbit. A four year mission in an 800 km Sun

synchronous orbit leads to a dose of approximately 1.4 krad(Si), which is mostly due to protons in the SAA [50].

3.1.4 Secondary radiation

Secondary radiation sources are produced when high energy particles interact with the spacecraft material. Particles which are slowed or stopped will give off Bremsstrahlung radiation in the form of X-rays. Shielding is often used around image sensors to reduce the flux of damaging high energy particles (without blocking photons from the optics). Well designed shielding should be efficient at blocking high energy particles but also ensure that any secondary radiation produced is not more damaging than the raw radiation environment.

3.2 Radiation damage mechanisms

Below is a short summary of the physical processes by which an incoming particle can interact with a silicon crystal. These processes may result in ionising damage (covered in Section 3.3), displacement damage (covered in Section 3.4) or single event effects (Section 3.7).

3.2.1 Interaction in silicon of energetic particles

Electronic Coulomb interaction (ionising)

Particles with energies between 1.1 eV and a few MeV, when interacting with the electric field of electrons in the silicon, will primarily undergo Coulomb scattering. In Coulomb scattering, energy is lost to the ionisation of the atoms with which the incoming particle interacts.

Nuclear Coulomb interaction (displacement)

Charged particles can also interact with the electric field of the nuclei of target atoms, possibly ejecting the nuclei from their position in the lattice.

Nuclear reaction

Protons with high energy ($> \text{MeV}$) can overcome the electrostatic potential barrier around nuclei, while for neutrons there is no barrier to overcome. These particles can then interact with the nucleus directly causing nuclear fission. This process is described as inelastic because kinetic energy is not conserved. The resulting isotopes can be released with high kinetic energy. Such an event can cause cascading collisions and be extremely damaging.

3.2.2 Interaction in silicon of photons

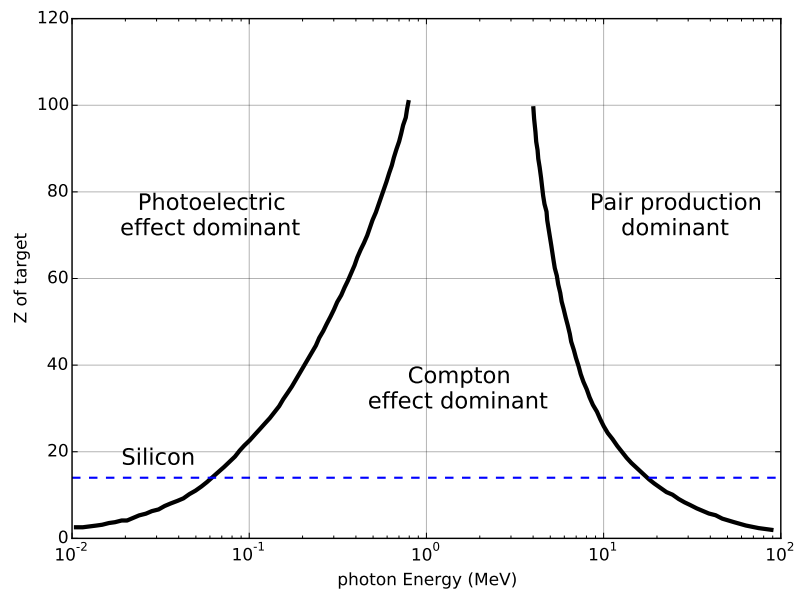


Figure 3.3: The dominant interaction mechanism for a photon entering a material depends on the photon energy and the atomic number Z of the material. After Evans [51]

Photons interact with silicon via three mechanisms. At low energies, the photoelectric effect dominates and atoms are ionized. At higher energies Compton scattering dominates

which excites electrons while the photon continues with a longer wavelength. At even higher energies, the incoming photon can produce an electron-positron pair. In all of the situations the resulting energetic particles (electrons, positrons) etc. can go on to cause further damage by the mechanisms outlined for non-zero rest mass particles. Figure 3.3 shows how the photon energy ranges for which the photoelectric effect, Compton scattering or electron-positron pair production dominates. The effects are material dependent and a dashed line shows the position of silicon with atomic number $Z = 14$.

3.3 Ionisation damage

Total ionising dose

The amount of ionising damage caused by radiation is quantified by the Total Ionising Dose (TID) defined as

$$TID = LET \cdot \phi \quad (3.1)$$

where ϕ is the total radiation flux and the LET is given by

$$LET = \frac{1}{\rho} \frac{dE}{dx}. \quad (3.2)$$

The LET (Linear Energy Transfer) is the rate at which energy E is lost to the material by the radiation along a length x . The SI units of TID are the Gray (Gy), although the rad=0.01 Gy is commonly used. The Gray is defined as 1 J kg^{-1} being deposited in the material. Since the same radiation will deposit a different amount of ionising energy into different materials the unit usually includes the material in question such as Gy(Si) for silicon or Gy(SiO₂) for silicon dioxide.

Ionising radiation damage has two primary effects in silicon image sensors. These effects arise from the use of insulators (e.g. SiO_2) in a Metal-Oxide-Semiconductor (MOS) structure, or from the interface between silicon and an insulator.

3.3.1 Ionising damage in MOS capacitor structures

Ionisation in doped silicon does not cause damage because electrons and holes both have relatively high mobility. In insulators such as SiO_2 however electrons have high mobility but holes do not. In addition, free electrons are not readily available in an insulator so holes will rarely get a chance to recombine. When an electron-hole (e-h) pair is created in SiO_2 through ionisation the electron is therefore likely to move away from the hole if there is an electric field present, leaving the positively charged hole. The bandgap of SiO_2 is approximately 8 eV and the mean ionisation energy is about 18 eV.

Flatband voltage shift

The flatband voltage in a MOS capacitor, when used in CCDs, is defined as the voltage required on the polysilicon gate to compensate for the different work functions of the polysilicon and the silicon and thus create the same Fermi level in both materials. In other words, the potential in the silicon is equal to the gate potential minus the flatband voltage. An undamaged, charge-neutral, oxide does not alter the electric field between the two conducting materials (if fringing is neglected). Flatband voltage shift occurs when the oxide becomes charged. Positively charged holes remaining in the oxide after ionising damage produce their own electric field in the oxide thus changing the flatband voltage. If it is assumed that all holes become trapped at the Si- SiO_2 interface, the flatband voltage shift can be written as [3].

$$\Delta V_{FB} = -\frac{qQ_h x_{ox}}{\epsilon_{ox}} \quad (3.3)$$

where Q_h is the two-dimensional hole density at the interface, x_{ox} is the oxide thickness and ϵ_{ox} is the oxide permeability. Typically, a flatband voltage shift of $-0.1 \text{ V krad(Si)}^{-1}$ is seen in CCDs, although radiation-hard CCDs can have shift as low as $-0.001 \text{ V krad(Si)}^{-1}$ [3, pg. 722].

Threshold voltage shift

Other devices using MOS structures suffer the oxide charging effect that results in flatband voltage shift. Different nomenclature is sometimes used. For example, when discussing MOSFETs, the effect is called threshold voltage shift. This is due to fact that the gate voltage required to take the MOSFET from the sub-threshold region to the linear region changes as a result of the oxide charging. This in turn alters the gate voltages required to turn the MOSFET "on" and "off".

3.3.2 Interface states

At the oxide-semiconductor interface there is a lattice constant mismatch which results in "dangling bonds", i.e. covalent bonding is not complete for all atoms. The additional mid-band energy levels introduced by these interface states contribute to dark signal. In order to counteract this, hydrogen passivation is performed during manufacturing whereby hydrogen diffuses into the device and becomes bonded at the interface states. Ionising radiation can break the weak bonding of the hydrogen passivation allowing the hydrogen to diffuse again through the device leaving the dangling bonds. These dangling bonds can behave in the same way as defects introduced by displacement damage, trapping electrons, or increasing charge carrier generation.

The interface states also trap holes as they migrate to the edge of the insulator in the presence of an electric field. The holes are trapped when they form stable defect centres at the Si-SiO₂ interface.

3.3.3 Dependence on electric field

Not all the e-h pairs created in the oxide result in trapped holes. Electrons and holes can recombine. Recombination is less likely if the electron and hole are quickly separated from each other by the presence of an electric field. The fractional yield is a measure of the fraction of e-h pairs that do not recombine

$$\eta_{FY} = \frac{h_t}{h_{e-h}} \quad (3.4)$$

where h_t is the number of trapped holes and h_{e-h} is the number of e-h pairs [3].

The fact that the fractional yield is increased with the presence of an electric field means that biased oxides suffer more from trapped charge. Therefore, for example, an operational CCD will suffer a greater flatband voltage shift than a non-operational one. For this reason, biasing is often applied during the irradiation to mimic the state of the device when being damaged in space.

3.4 Non-ionising damage

Displacement damage dose

The displacement damage dose, or non-ionising dose, is given by

$$Dose_{NI} = \int \frac{d\phi(E)}{dE} \cdot NIEL \cdot dE \quad (3.5)$$

where the Non-Ionising Energy Loss (NIEL) is defined as

$$NIEL = \left. \frac{dE}{dx} \right|_{non-ionising} \quad (3.6)$$

i.e. the rate of energy loss along a path x to processes other than ionisation. These processes are displacement damage and phonon production (a relatively small effect) [52].

Displacement damage mechanisms

Displacement damage occurs when a silicon atom is dislodged from its position in the lattice due to scattering of an incoming energetic particle. This can be Rutherford scattering or nuclear scattering. The displaced silicon atom is called the Primary Knock-on Atom (PKA) and can collide with other atoms causing further damage to the lattice, possibly producing further recoils. The most common immediate result of a damaging collision is the Frenkel pair which consists of a vacancy and an interstitial atom [52]. The type of defect produced depends on the energy, mass and charge of the incoming particle. Electrons and photons tend to cause single defects whereas neutrons can cause clusters (concentrations of multiple defects) [3]. If the nuclear scattering from a proton is non-elastic (the proton particle passes within the k-shell orbit) a nuclear decay occurs producing an alpha particle which has a very short stopping distance and therefore causes a lot of damage [3, pg. 773] [53, pg. 303].

NIEL scaling

NIEL scaling, also known as bulk damage equivalence, is used to convert between the amount of damage cause by different particle species and particles with different energies. The scaling factors are found from simulation and experimentation. Figure 3.4 shows the NIEL caused by electrons, neutrons, pions, and protons at various energies. The NIEL scaling hypothesis is very useful given that the radiation sources available for testing silicon do not cover all energies. Proton sources for example typically have a single energy available (which can be reduced but doing so increases the energy range). Using the NEIL scaling hypothesis, the actual radiation environment a device will operate in can be synthesised with a single energy radiation source. NIEL scaling is not perfect. It does not take into account

the stopping distances of particles. It also assumes that the "amount of damage" can be represented by a single number. In reality, different sources will cause different relative concentrations of certain defects and the relative concentrations of defect clusters will be different.

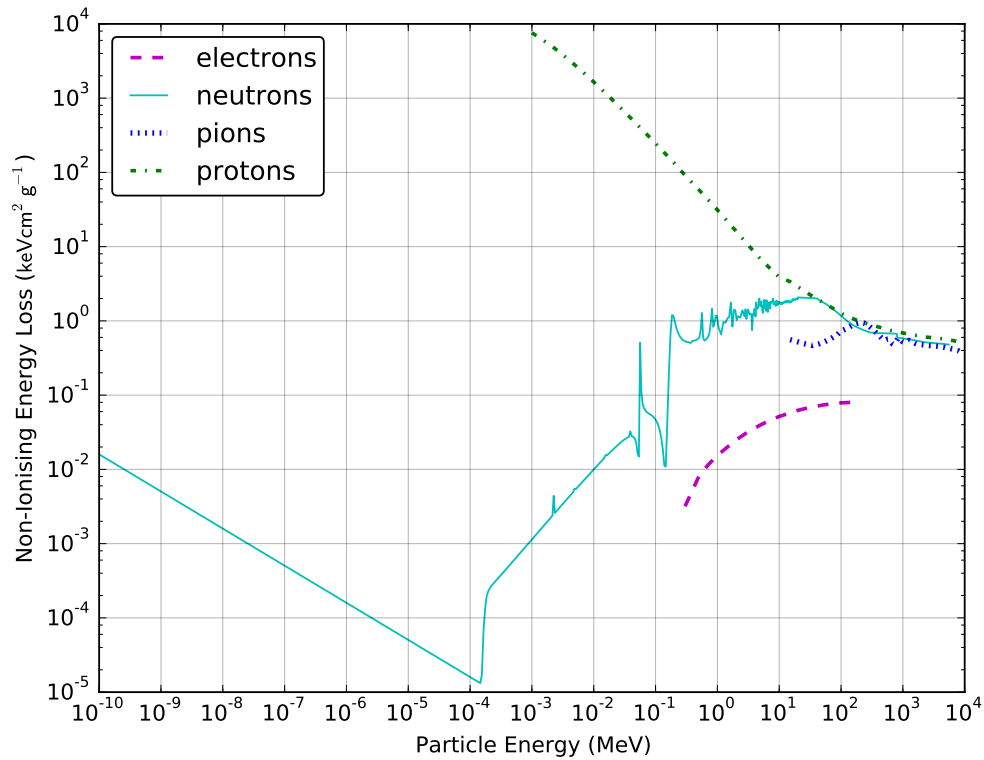


Figure 3.4: The NIEL caused by different radiation sources can be quantified. This allows the calculation of the amount of radiation required from a different source in order to produce an equivalent amount of damage. Data plotted from compilation by Vasilescu and Lindström [54].

3.4.1 Displacement damage effects

Figure 3.5 shows some of the effects that occur due to defects caused by displacement damage that introduce energy levels in the silicon bandgap. These effects are discussed below.

(a) Recombination: The reverse of the e-h pair generation is recombination. The re-

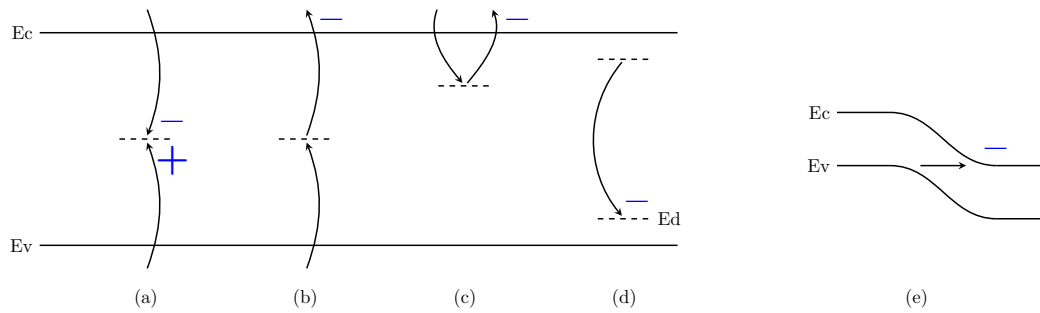


Figure 3.5: Energy levels introduced in the silicon bandgap by displacement damage have five main effects on the operation of devices: (a) recombination; (b) generation; (c) trapping; (d) compensation; and (e) tunnelling.

combination rate is increased by the presence of mid-band energy level defects. This can cause a loss of signal in image sensors, which collect and measure optically-generated free electrons.

(b) Thermal generation of e-h pairs: Electrons can make the jump from the valence band to the conduction band (leaving a hole in the valence band) much more easily by making the transition in two steps, first to the energy level of the defect in the bandgap and then from the defect energy level to the conduction band. When this happens in depleted silicon the free carriers produced can contribute to dark or leakage current.

(c) Trapping of carriers: Electrons moving in the conduction band can become trapped at defect sites which offer lower energy states. After a random amount of time (with a time constant) the electron is released back into the conduction band through thermal excitation. This is a problem for devices such as CCDs which rely on the timely transfer of electrons from pixel to pixel during readout.

(d) Dopant compensation: The amount of dopants in the silicon is controlled in order to give properties such as the equilibrium majority carrier concentration and the resistivity. The effective dopant concentration can be distorted by displacement damage. For example, a donor energy level produced can provide an electron that fills an acceptor dopant energy level therefore effectively removing an acceptor.

(e) Tunnelling: Defect energy levels can assist carriers in tunnelling between energy

bands. This can affect the reverse bias current across narrow abrupt pn junctions.

3.4.2 Stable defects and annealing

The majority of vacancies and interstitials (more than 90% [55]) produced by displacement damage are not permanent and the silicon lattice repairs itself. Defects which remain after around one minute however tend to be permanent. These defects migrate through the lattice until they form stable defects which can involve atoms other than silicon (for example oxygen, which is a contaminant in silicon, or dopants such as phosphorous).

Defects will anneal if sufficient heat is provided. Figure 3.6 shows the temperatures required to anneal some common defects.

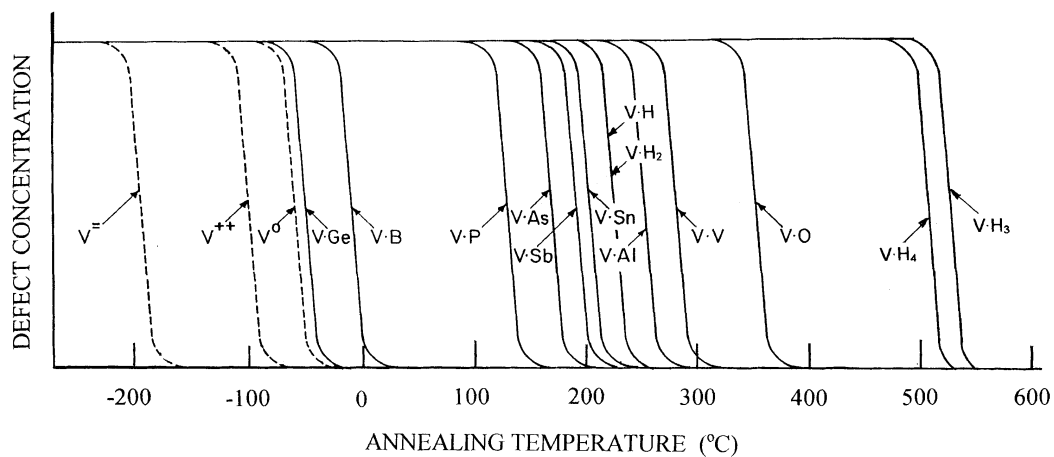


Figure 3.6: Annealing of defects happens rapidly once a sufficient temperature is reached. These are some of the known defects in silicon crystals. Reproduced from Watkins [56].

3.5 Effects of radiation damage on the electro-optic performance of image sensors

3.5.1 CCDs

Flatband voltage shift

The gate voltages used for CCD clocks are carefully chosen to maximise performance parameters such as dark current, charge transfer inefficiency and full well capacity. Flatband voltage shift changes the effective voltage applied to the clocks. The flatband voltage shift present at each gate also varies due to the random distribution of the radiation damage. These effects can lead to degradation in image sensor performance.

In addition, with high levels of radiation, the relative shift of voltages within the pixel and register clocks and within the readout circuitry can lead to a complete loss of function in the device.

Dark current

Displacement damage to the bulk silicon and ionising damage at the Si-SiO₂ interface both lead to increased dark current. Bright pixels are a common feature in sensors that have suffered displacement damage.

Charge transfer inefficiency

Charge trapping is most significant in CCDs which rely on the timely transfer of charge between pixels as part of the image readout process. Electrons which become temporarily trapped may appear instead in the signal of a pixel which is read out later on.

Charge transfer inefficiency due to trapping of charge carriers is covered in more detail in section 3.6.

3.5.2 CMOS Image Sensors

Dark current

Ionising damage to Si-SiO₂ interfaces in CMOS active pixel sensors will cause an increase in dark current, typically a few pA cm⁻² per krad(Si) at room temperature [57] [58]. As in CCDs, displacement damage to the bulk silicon will cause increased dark current and an increase in the number of bright pixels.

Threshold voltage change

The threshold voltage shift experienced by MOSFETs in CMOS devices will alter the way in which some circuits work. An example of this is the in-pixel source-follower transistor where the threshold voltage shift adds an offset to the output voltage from the pixel. Ionising damage can therefore cause increased fixed pattern noise. High levels of ionising damage can completely prevent some circuits from functioning. For radiation hardened devices, a gamma dose of >5 Mrad(Si) can cause a threshold voltage shift of as little as 80 mV [57].

Random telegraph signals

Random Telegraph Signals (RTS) are usually caused by damage to the bulk silicon. The symptoms of RTS are a random switching between two or more dark current levels within a single pixel. The effect can also be present as a fluctuating offset in the in-pixel source-follower amplifier.

Single event effects

Single Event Effects (SEE) are those radiation effects which can occur due to the interaction of a single particle. The small feature sizes and large variety of electronic circuits present on CMOS devices compared to CCDs make most SEEs a more common occurrence in CMOS.

Some SEEs are not "damage" per se, but some can cause total device failure after a single particle strike. SEEs are covered in detail in Section 3.7.

3.6 Charge transfer inefficiency

Charge Transfer inefficiency (CTI) is a measure of the inability to completely transfer charge packets between pixels in a CCD. Deferred charge (charge which is not transferred as part of the correct charge packet) is eventually transferred as part of later signals. CTI for a device is usually averaged across pixels (and inside each pixel there will be one transfer per phase). The CTI per pixel is defined as

$$CTI = \frac{\text{deferred charge}}{\text{signal charge} \times \text{number of transfers}} \quad (3.7)$$

and the Charge Transfer Efficiency

$$CTE = 1 - CTI \quad (3.8)$$

Trapping of charge can be caused by potential barriers between pixels that does not allow complete charge transfer. This can be because of the shape of the electric field created by gate voltages. This effect can be almost entirely eliminated by design in CCDs. Charge can also be trapped by defects caused by radiation damage. This section deals with charge trapping by defects.

3.6.1 Mechanism of CTI caused by charge trapping

Figure 3.7 shows charge trapping in a 3-phase CCD. Charge is captured from the signal charge packet by the trap. If the trapped charge is released quickly it can re-join the original charge packet. If not, it will become part of the signal packet in the following pixels. It

should be clear that the emission time of the trap is critical to how much CTI is experienced. If the emission time is short compared to the clock period, most charge will stay in the correct pixel. If the emission time is long, then the trap will stay occupied for a long time and trapping will be relatively infrequent.

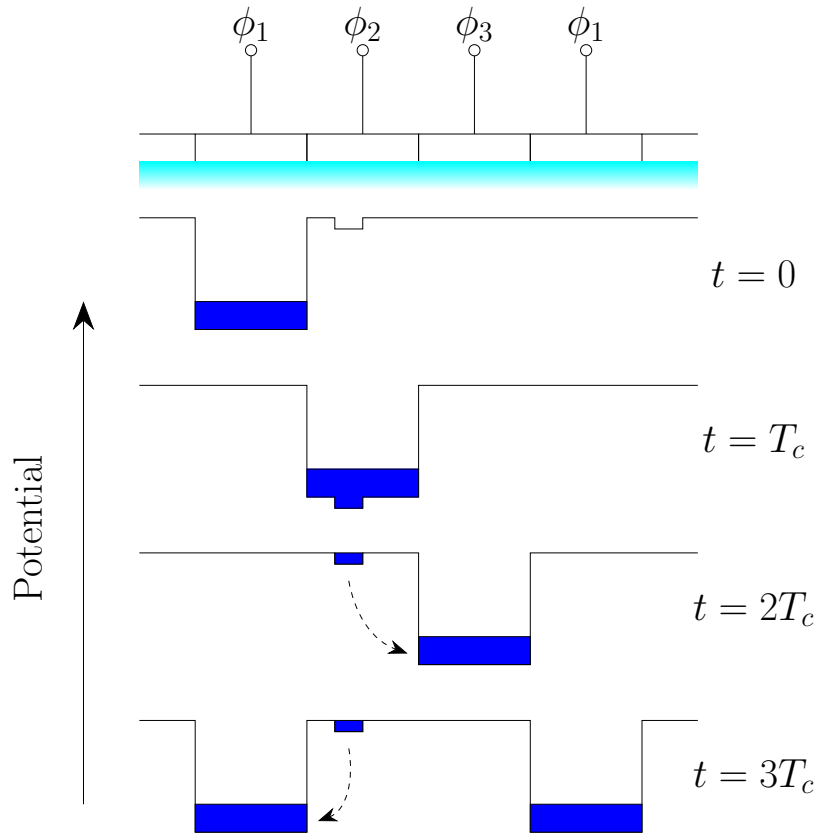


Figure 3.7: Charge trapping can lead to CTI. At $t = 0$ the trap under ϕ_2 is empty. At $t = T_c$ the trap is filled with charge captured from the arriving charge packet. Capture happens quickly relative to emission. If the trap emits the trapped electron before $t = 3T_c$ it will join the original charge packet. If the trap emits after this time, the electron emitted will become part of a following charge packet resulting in CTI.

3.6.2 Factors affecting trap capture and emission times

The kind of defect determines the trap capture and emission time constants. The probability of an empty trap having captured an electron after time t is given by

$$P(t) = 1 - \exp\left(-\frac{t}{\tau_c}\right) \quad (3.9)$$

where τ_c is the capture time constant. Likewise, the probability that a full trap will have released an electron is given by

$$P(t) = 1 - \exp\left(-\frac{t}{\tau_e}\right) \quad (3.10)$$

where τ_e is the emission time constant. The capture time constant is given by

$$\tau_c = \frac{1}{\sigma_n v_{th} n_s} \quad (3.11)$$

where σ_n is the capture cross section, v_{th} is the electron thermal velocity and n_s is the electron signal concentration in the vicinity of the trap. The emission time constant is given by

$$\tau_e = \frac{1}{\sigma_n X_n v_{th} N_c} \exp\left(\frac{E}{kT}\right) \quad (3.12)$$

where X_n is the entropy change factor by electron emission and N_c is the conduction band effective density of states. The entropy change factor accounts for the fact that energy is conserved during a capture-emission cycle but entropy must increase. It is often approximated to unity.

Equations 3.9 - 3.12 are from what is known as Shockley-Read-Hall (SRH) theory [59][60].

Trap species	E (eV)	σ_n (cm ⁻²)
P-V (E-centre)	0.46	5×10^{-15}
(V-V) ⁻ (divacancy)	0.41	5×10^{-16}
(V-V) ⁻⁻ (divacancy)	0.21	5×10^{-16}
O-V (A-centre)	0.17	5×10^{-14}

Table 3.1: Summary of trap energy levels and capture cross sections for trap species known to cause charge transfer inefficiency in phosphorous doped n-channel CCDs [62]

The electron thermal velocity can be calculated as

$$V_{th} = \sqrt{\frac{3kT}{m_e^*}} \quad (3.13)$$

where m_e^* is the electron effective mass in the conduction band $0.26m_e$ (m_e is the free electron mass). The conduction band effective density of states is given by

$$N_c = 2 \left(\frac{2\pi m_{de}^* kT}{h^2} \right)^{3/2} \quad (3.14)$$

where m_{de}^* is the electron density of states effective mass which at 300 K is $0.33m_e$ [61].

Certain common known defect centres are of particular importance to CCDs. These species are summarised in table 3.1. The defect centres are the E-centre which is formed from a phosphorus atom and a vacancy, the two divacancies which are both caused by the combination of two vacancies, and the A-centre which is formed from an oxygen atom and a vacancy. The arrangement of these defects in the silicon crystal are shown in figure 3.8.

The reason that these defects are of interest is that their emission time constants can be close to the clock period T_c used in CCDs. CTI is maximised when $T_c \approx \tau_e$. The emission time constants of the traps formed by these defects are plotted in figure 3.9 as a function of temperature.

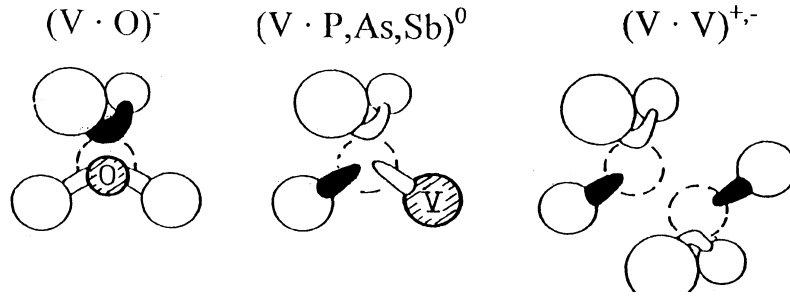


Figure 3.8: When vacancies produced by displacement damage combine with impurities (here, oxygen and phosphorus) or with other vacancies they can form permanent traps which lead to CTI. Reproduced from Watkins [56].

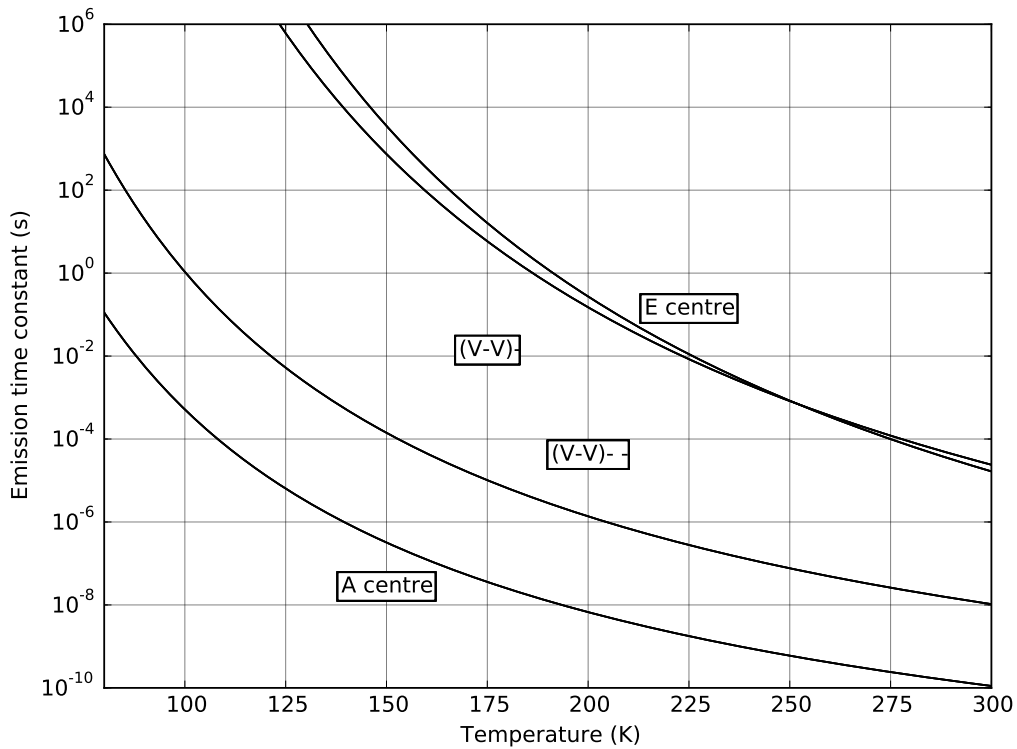


Figure 3.9: Electron traps cause the CTI in CCDs when the emission time constant is comparable to the CCD clock period.

3.7 Single event effects

Individual charged particles producing ionisation in CMOS devices (Figure 3.10) can cause a variety of effects. These are summarised below and detailed in the following sections.

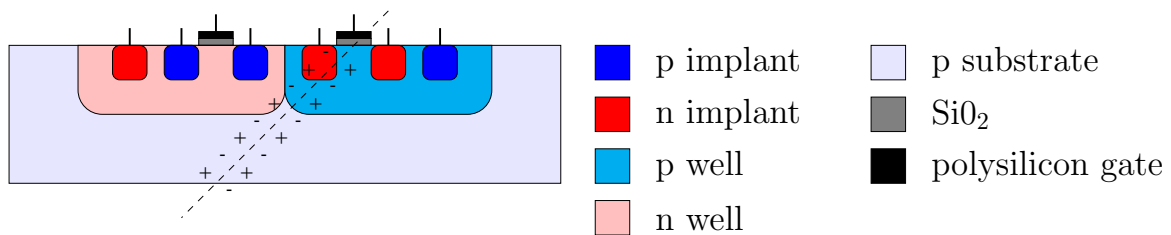


Figure 3.10: A charged particle producing an ionisation track in a CMOS device can cause a variety of effects.

Single Event Upset (SEU)

The voltage on a circuit node can be altered by the creation of a charge cloud in or near that node. This change of voltage is called a Single Event Transient (SET) and if large enough can constitute a change of logic level, i.e. an error. If the error manages to propagate to an output, it is called an SEU and will typically result in a bit-flip in data. SEUs are discussed in more detail in Section 3.7.9.

Single Event Functional Interrupt (SEFI)

When an SEU causes a state machine to enter an incorrect state this is called a SEFI. This is generally more serious than an SEU as it can cause the system to crash. SEUs are discussed in more detail in Section 3.7.9.

Single Event Latchup (SEL)

CMOS logic gates have a parasitic built in npnp semiconductor structure between the positive and the negative supply which forms a thyristor. Under normal circumstances the thyristor is off and there is no conduction but a charge cloud can trigger conduction. Positive feedback ensures that conduction does not cease and the device "latches up". There is effectively a short circuit across the power supply until the supply is disconnected from the device. If sufficient current flows for enough time, latchup can cause permanent destruction. Unhardened CIS circuits are typically found to suffer from SEL due to particles producing

an LET of $20 \text{ MeV cm}^2 \text{ mg}^{-1}$, or even lower. Radiation hard sensors such as the STAR-250 have been reported to be latchup-tollerant up to $68 \text{ MeV cm}^2 \text{ mg}^{-1}$ [57]. SEL is discussed in more detail in Section 3.7.1.

Single Event Gate Rupture (SEGR)

Gate rupture can occur if a charge cloud causes breakdown within the normally insulating gate. This tends to be more of a problem in Electron Multiplying CCDs (EMCCD) and power electronics.

3.7.1 SEL

CMOS processing allows, by definition, the fabrication of n and p channel Field Effect Transistors (FETs) on the same silicon substrate. Traditionally this is achieved by implanting wells of dopants of opposite type to the dopants in the substrate. For example, n channel FETs can be fabricated on a p type substrate by implanting donor impurities to form the n type drain and source regions. To fabricate a p channel FET in a p substrate, first a well of n type silicon is created in the substrate and the p type drain and source regions are then implanted into the well. In more advanced processes a p type substrate is usually used, but a high purity layer of epitaxial silicon (with a low concentration of acceptor dopants) is grown onto the substrate. Wells of n type and p type silicon are then formed in the epitaxial silicon as required.

Although wells may be separated to some extent by growing oxide between them, known as Shallow Trench Isolation (STI) or Deep Trench Isolation (DTI), the n and p wells usually touch each other. The effectiveness of STI and DTI in preventing latchup is discussed in section 3.7.4.

A typical CMOS circuit such as an inverter (Figure 3.11a) is built using p and n wells. A side effect of this implementation is that it connects V_{DD} to V_{SS} via a pnpn structure (Figure

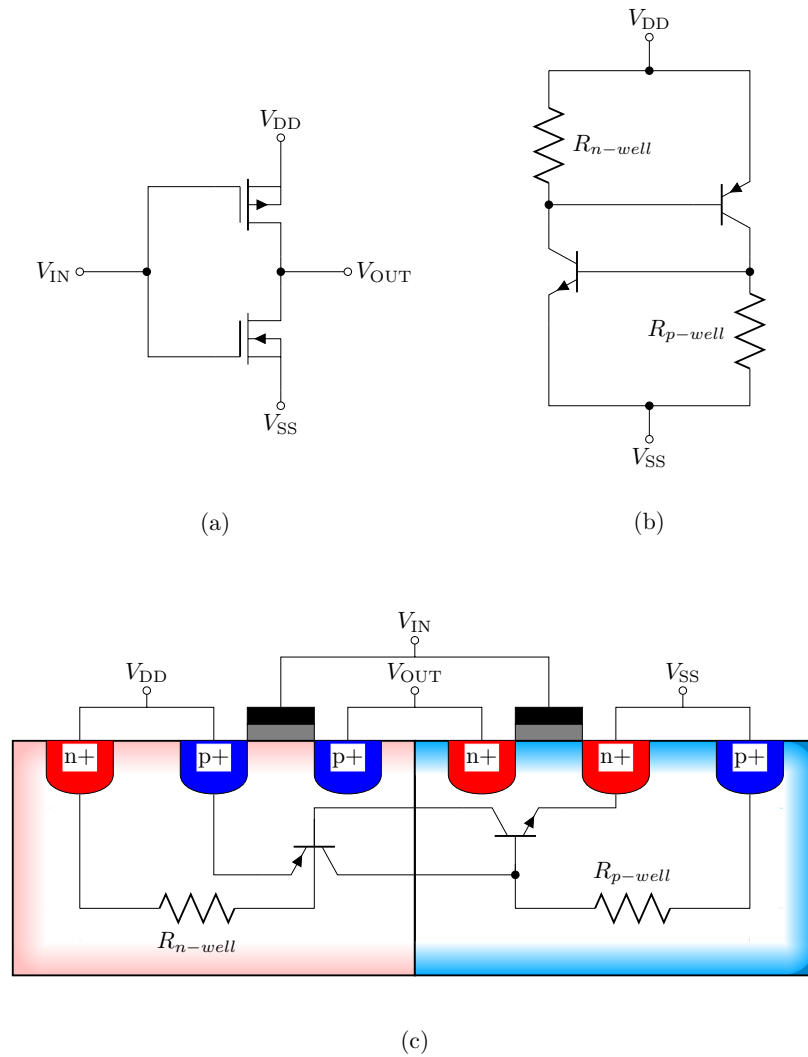


Figure 3.11: (a) A simple inverter circuit using two MOSFETs. (b) The parasitic circuit resulting from the well doping structure of typical CMOS processes. The cross-connected BJTs make this implementation of CMOS circuits susceptible to latchup. (c) Cross section of the inverter circuit as fabricated in dual-well CMOS (after Johnston [63]). The parasitic circuit is also shown.

3.11c) which is equivalent to two Bipolar Junction Transistors (BJT) (or a thyristor). If the resistance of the wells is taken into account a parasitic circuit (Figure 3.11b) can be drawn. A similar parasitic circuit can exist whenever sources are connected to the power supply, regardless of the logical connections made with the drains and gates of the FETs.

Under normal circuit operation the parasitic circuit only contributes a small leakage current from V_{DD} to V_{SS} . However, the cross-linked arrangement of the BJTs means that

the collector current will be amplified by the other BJT and fed back as a base current. If the current gain, β , of the BJTs is such that $\beta_{pnp} \cdot \beta_{npn} > 1$ then the circuit is bi-stable. If sufficient collector current is achieved in either BJT the current I_{VDD} will increase until it is limited by either the internal resistances of the chip or by the power supply. This runaway current condition is known as a latchup. Stopping (or quenching) the latchup requires intervention to reduce the supply current. The current to trigger a latchup condition can be provided either by a disturbance in supply voltage (e.g. from electrostatic discharge into the device) or by the introduction of a cloud of free charge carriers in the wells through ionising radiation. Latchup, when triggered by an ionising particle, is called Single Event Latchup (SEL).

3.7.2 Latchup from heavy ions

SEL may be caused in the space environment by a range of ionising particles and is one of the potential disadvantages of using CMOS technology in space for image sensor applications [64] [65]. The expected rate of SEL of CMOS devices must be assessed before use in space to ensure that the expected rate of events and their effects will be manageable.

Heavy ions (ions with nucleon number $A > 4$) and neutrons are commonly used experimentally to investigate SEL rates in Integrated Circuits (ICs). Heavy ions produce a charge trail as soon as they impact silicon. Neutrons are charge neutral, so they do not create a charge cloud themselves. However, neutrons can displace an atom from the silicon crystal, producing a PKA. An energetic PKA will produce an ionisation trail.

3.7.3 Effective LET

For the purposes of studying SEEs, heavy ion interaction in silicon can be quantified by the Linear Energy Transfer (LET). The LET is a measure of the energy lost by the particle to ionisation per unit length, normalised to the density of the target material (Equation 3.2).

It is common practice to quote the LET of the particle at the point where it first enters the target material.

If the sensitive volume of the device (the volume in which a charge cloud can contribute to SEEs) is assumed to be thin, then the size of the charge cloud can be increased by tilting the beam away from normal to the target. By doing so the particle path within the sensitive volume is increased. If the sensitive volume also covers a large area of the target, then the effect of tilting the beam can be considered to be the same as increasing the LET of the normal beam. Thus the "effective LET" is given by

$$LET_{eff} = LET \sec \theta \quad (3.15)$$

where θ is the tilt angle (see Figure 3.12).

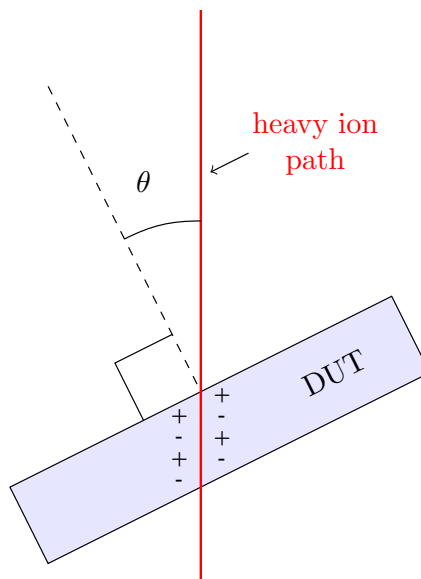


Figure 3.12: Effective LET

3.7.4 Latchup mitigation

To prevent or reduce the susceptibility of CMOS circuits to latchup several techniques can be used at design level.

- The supply voltage can be reduced. In fact, the supply voltage (as opposed to the LET) at which latchup occurs is often used as a metric when comparing designs [66].
- SEL can be controlled with a Current Limiting Device (CLD) (see [67] for example) which is generally on-chip circuitry which will automatically quench latchups by reducing the current when they occur. This adds area and complexity to the design.
- The potential structure within the device can be controlled thus diverting the charge cloud away from sensitive areas.
- Recombination rates can be increased by reducing the field in which the charge cloud is created.
- Decreasing the well or substrate resistances increases the current required to forward bias the base-emitter junctions [66].
- Certain technologies are intrinsically immune to latchup. For example, Silicon On Insulator (SOI) is often assumed to be latchup immune [68] [69] but the exact technology must be examined. For example, some Bipolar CMOS (BiCMOS) technologies do have a pnpn path from V_{DD} to V_{SS} .
- Triple wells are formed when a layer of n or p doping is implanted under the usual wells. An example of a deep p well implementation is shown in figure 3.13. Triple wells have been shown to reduce SEL [70] [71] in some situations. The inclusion of a triple well option, which is common in processes of $0.18\mu\text{m}$ or below, originally had the purpose of allowing back-biasing and noise isolation in analogue and Radio Frequency (RF) circuits [72].

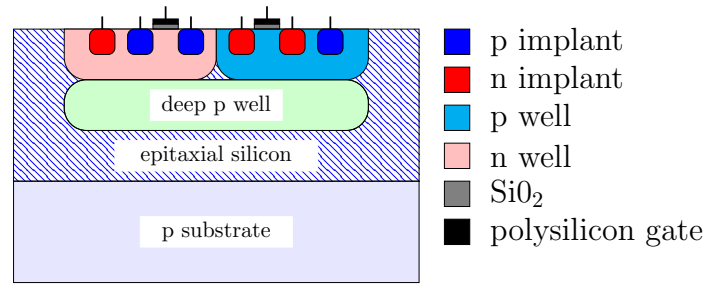


Figure 3.13: Triple well devices typically contain either a deep n or deep p well underneath the standard n and p wells. A deep well is formed by ion implantation and usually occupies a large fraction of the device area. Certain circuits on chip may not be compatible with the deep well, APS pixels being an important example.

3.7.5 Triple wells

There are at least two important competing effects of using triple wells. In the case of a deep n well device for example the deep n well connects multiple n wells which significantly reduces the resistance to the BJT base [70] and reduces the pnp BJT gain. However, the deep n well has the opposite effect on the npn BJT, whose base to V_{SS} resistance and gain increase [72]. Uemura *et al* [73] explored some of the ways in which SEL can be reduced through the use of deep n wells and deep p wells and increasing the doping of the triple wells. In the Static Random-Access Memory (SRAM) devices (50 nm and 90 nm processes) tested with neutron irradiation, those with deep p wells showed the best resistance to SEL and they did not show the increased SEU rate associated with deep n wells. Deep p wells were shown by Kato *et al* [74] to harden against SEL from neutrons and this effect was explored with a 3D TCAD simulation.

3.7.6 Epitaxial layer thickness

The effect of epitaxial thickness on LET threshold (the minimum LET required to produce a latchup) has been investigated experimentally [75][64]. It was demonstrated that increasing the epitaxial layer thickness from 9 μm to 12 μm decreased the LET threshold. A good summary of alternative strategies for SEL hardening can be found in Dodds *et al* [66].

3.7.7 Potential barrier

A potential barrier is formed when two volumes of silicon (e.g. volume x and volume y) with different dopant types or different dopant concentrations are brought into contact with each other. At the junction of two p type or two n type volumes the built in potential is given by $V = \frac{kT}{q} \ln \frac{N_A|_x}{N_A|_y}$ and $V = \frac{kT}{q} \ln \frac{N_D|_x}{N_D|_y}$ respectively where $N_A|_x$ is the acceptor concentration in volume x and $N_D|_y$ is the donor concentration in volume y etc. Similarly, the built-in potential at the junction of two differently doped regions is given by $V = \frac{kT}{q} \ln \frac{N_A|_x N_D|_y}{n_i^2}$ where n_i is the intrinsic carrier concentration. Potentials structures obtained through simulation are shown in Section 5.1.2. The effect of the original potential structure may be outweighed by the large number of carriers introduced by an ionising particle.

3.7.8 Effect of temperature on latchup

Device temperature has implications for SEL studies. Several factors increase the susceptibility of circuits to latchup at increased temperature [76]:

- The base-emitter forward voltage drop goes down by approximately 2 mV/°C, so BJT turn-on happens at a lower voltage.
- The leakage current through the transistors doubles roughly every 10 °C. This leakage current contributes to the voltage drop on the resistive paths.
- Metal tracks, and n well resistors, have increased resistance at high temperatures.
- β increases with temperature.

The effect of temperature on latchup has been investigated with a numerical simulation of by Iwata *et al.* [77]. The simulation showed the latchup threshold increasing (i.e. SEL hardness increasing) at reduced temperature, up to a peak in LET threshold at 120 K. Below 120 K the threshold decreased with temperature, until carrier freeze-out at ≈ 77 K. Therefore,

when operating at temperatures above 120 K, LET threshold can be expected to reduce as temperature increases.

3.7.9 SETs, SEUs, and SEFIs

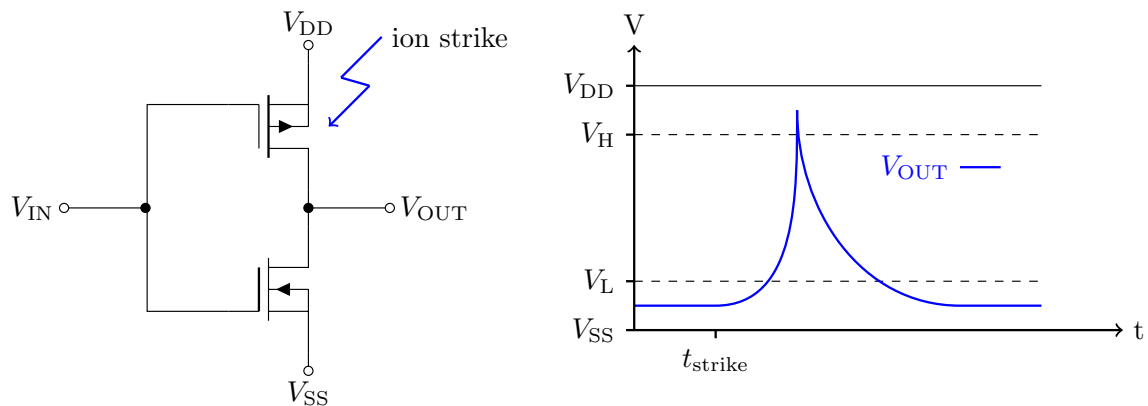


Figure 3.14: An ion strike in a MOSFET which is "off" can cause the MOSFET to conduct temporarily (an SET). In this example the voltage V_{OUT} is low until the ion strike at time $t = t_{strike}$ when the PMOS transistor begins to conduct. This takes V_{OUT} from below the threshold for a low signal, V_L , to above the threshold for a high signal, V_H . The result is the input to the following circuit being a "1" instead of a "0" for a short time.

In CMOS logic, the voltage at any node is set by modulating the drain to source impedance of MOSFETs. This impedance is set by controlling the MOSFET gate voltages. A charge cloud of free carriers near a MOSFET (e.g. produced by ionising radiation) can allow conduction in a MOSFET which should be "off" (high impedance). This can result in a temporary change of logic state at the node the MOSFET drives. This is known as a Single Event Transient (SET) (see Figure 3.14). Once the charge cloud has dissipated the correct logic state is restored (assuming no feedback is present). SETs can also affect the correct function of analogue circuits.

SETs can occur without causing any errors when they occur in combinational logic alone in a time frame in which the logic state is not sampled. However, if the logic output is sampled by a latch or flip-flop the error can be propagated. Worse still, an SET in a flip-flop

itself is liable to change the output of the flip-flop regardless of the clock state. SETs which cause an incorrect logic state at an output node of the circuit are called an SEU and typically appear as a bit flip in data (i.e. a 1 becomes a 0 or vice versa). Often more serious is the SEFI which occurs when a state machine in the circuit enters the wrong state. This can cause the circuit to behave unpredictably.

Chapter 4

Radiation damage in TDI charge-transfer CMOS image sensors

4.1 Introduction

Time Delay and Integration (TDI) sensors are used to increase the Signal to Noise Ratio (SNR) when imaging a moving scene. This is achieved by transferring collected charge across the sensor to track the motion of the image across the sensor, effectively increasing the integration time and allowing imaging of faint sources. This chapter looks at the performance of a new image sensor designed for TDI mode imaging based on CMOS technology. One important application for such image sensors is Earth observation from space. In this application, the radiation hardness of a sensor is crucial to its performance. For this reason, the effect of proton irradiation on the TDI image sensor is also explored in this Chapter.

This Chapter begins by explaining TDI mode imaging and why CCD architecture devices have advantages over APSs. The TDI-CMOS prototype charge-transfer image sensor used in the experimental work is introduced. Then, the characterisation of the TDI-CMOS sensor performance is presented. The measurement of CTI is particularly important for charge-transfer devices. Finally, the change in performance (dark current and CTI) after an

irradiation with high energy protons is presented. The radiation hardness of the devices is compared to the radiation hardness of a CCD of similar pixel specification.

4.2 TDI mode imaging

The most basic aircraft or satellite borne imaging systems for Earth observation generally use a linear image sensor which is oriented at right angles to the direction of motion. By means of downward-looking optics, a continuous two-dimensional image is generated by the motion of the sensor and associated line-by-line read-out, as shown schematically in Figure 4.1.

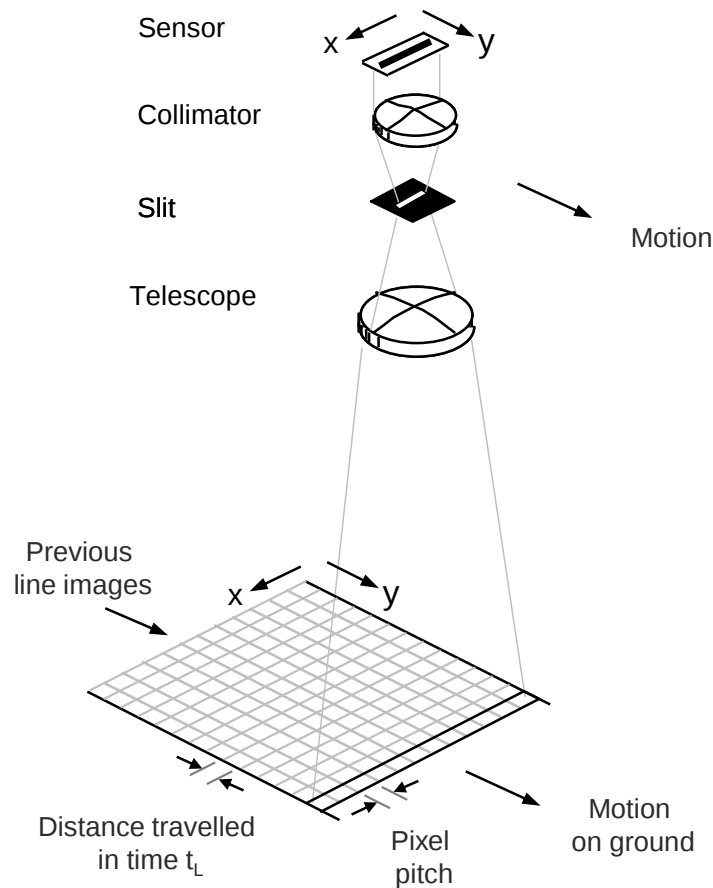


Figure 4.1: A moving linear sensor can be used to capture a two-dimensional image by using a line rate $1/t_L$ to correspond to the image motion.

The system is generally quantified in terms of the feature size on the ground, which corresponds to the pixel pitch on the sensor. Depending on the velocity of the craft, signal read-out is such that the time to collect and readout out a line of charges t_L corresponds to a distance travelled equal to the on-ground pixel pitch. In this way, the horizontal and vertical resolution in the scan-generated image can be comparable. Another name for this type of imaging is "push-broom" imaging.

A limitation of imaging with a rate of relative motion is that the time to collect charges in the pixel can be very short. This short integration time means that signal levels are also small and, in comparison with the noise introduced by the final read-out amplifier, the SNR is also small. A solution to this difficulty is the TDI approach, described using a CCD implementation shown in Figure 4.2. The sensor is now a two-dimensional full-frame device with a serial read out register and amplifier. The image section is clocked continuously at a rate that matches the parallel transfer to that of the image crossing the sensor by virtue of the craft's velocity. As any line of charges reached the bottom of the image section, it is transferred into the register which is then clocked to read out the line of charges in such a time that it is empty before the next line of image section charges arrives. If there are N lines in the image section and time to traverse a single line of pixels is t_L , the same as that of the linear image sensor, then the signal will be a factor N times larger and the dynamic range (assuming similar output amplifier noise) will also increase by this factor. Some devices are designed with the option of varying the number of TDI lines such that, irrespective of the image brightness, the increased signal size is always within the full-well capacity of the CCD [78]. The Gaia CCD221 can have up to 2340 TDI lines [79]. For Earth observation, typically up to 128 TDI lines are required [80].

Similar TDI mode sensing is also used for certain industrial applications, for example items on a conveyer belt.

Along with the general trend for imaging applications to be performed with CISs, vari-

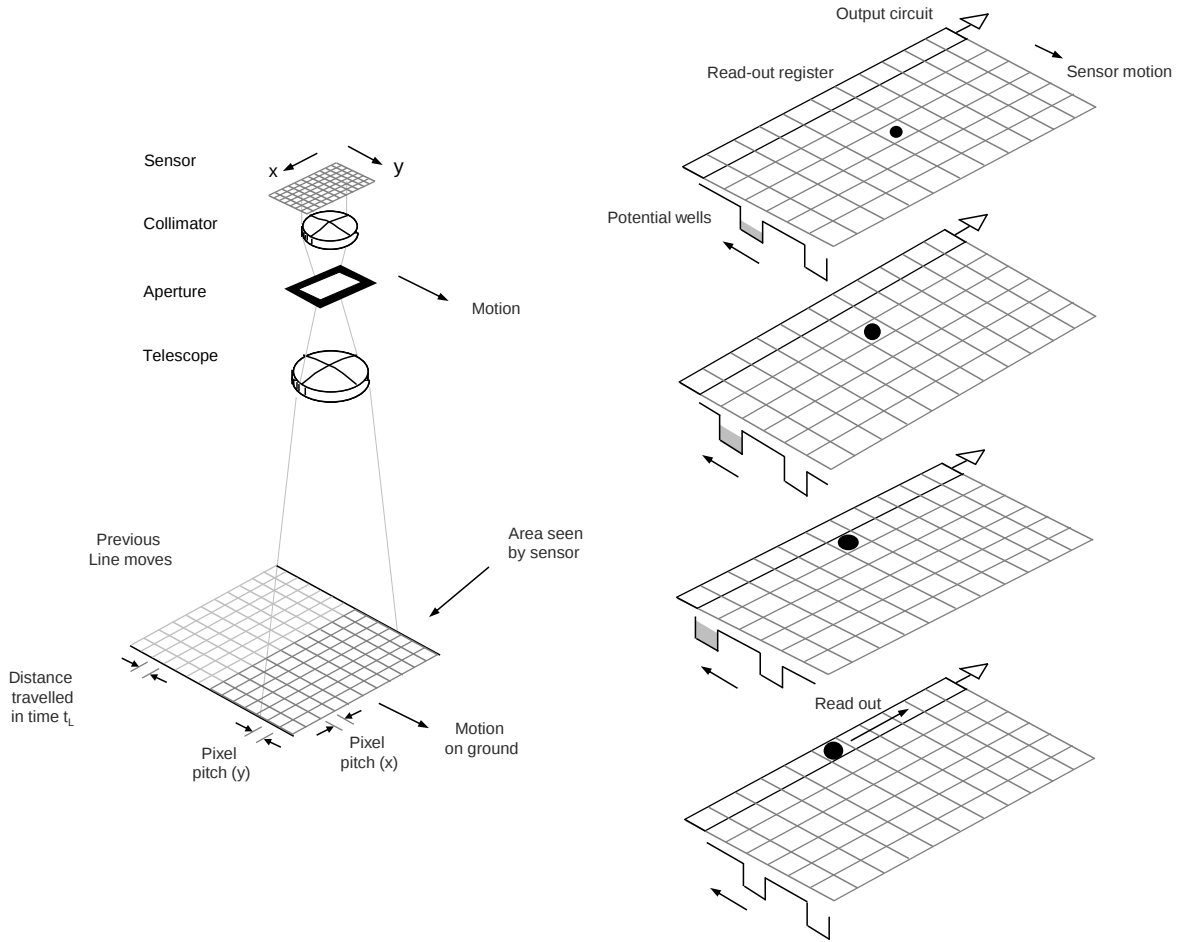


Figure 4.2: A two-dimensional sensor, in which charge is transferred row-by-row to the readout (serial) register, can also be used for moving images. If the charge transfer between rows is synchronised with the image motion, the signal from each point on the scene will increase as charge is transferred. Fast read-out is required in the serial register which limits the width of CCD-like devices, but can be achieved relatively in CMOS by directly reading each column (column-parallel readout [81]), thus avoiding the need for a serial register.

ous forms of push-broom sensors are now being produced. In comparison with CCDs, the major difference in standard CMOS APS is that signal charges are converted to a voltage in each pixel before readout. This has no significance in linear sensors as shown in Figure 4.1, but CCD-type TDI sensors involving the collection of charges in potential wells that are clocked in synchronism with the sensor motion are not possible with the standard APS structures. Instead an N row sensor has to be produced as an array of N linear sensors, and all pixels have to be read out as a group during the line time t_L . This means that there has

to be a very high data rate or there have to be multiple read-out lines. The TDI function is achieved by storing the line outputs in external circuitry and simply adding the line outputs of successive groups staggered by one line (e.g. add line 2 in group 2 to line 1 in group 1, then add line 3 from group 3 and so on). This operation results in signals which are multiplied by a factor N , but noise is multiplied by a factor \sqrt{N} . The overall signal to noise ratio is therefore a factor \sqrt{N} higher than a single line of sensors.

4.2.1 CCD-type TDI sensors in CMOS

As the design of a CCD is essentially a MOS transistor with multiple gates, in principle there is no fundamental reason why CCD structures cannot be fabricated using CMOS technology. However, most commercial CCD technologies are of a relatively coarse geometry (a few μm) and can use an overlapping polysilicon electrode structure to achieve the necessary small inter-electrode gap. The overlapping electrode structure is not implemented in modern fine geometry (e.g. $0.18\ \mu\text{m}$ CMOS processes) on account of the very shallow depth of focus provided by the photolithographic optics and because the device has to remain planar after every processing step. Only a single layer of polysilicon is usually used.

A first structure to be designed by e2v with the single polysilicon constraint is shown in Figure 4.3. Detailed information can be found in Mayer et al. [82]. The two phase clocking scheme for this structure is shown in Figure 4.4.

Polysilicon gates (shown in brown) are interspersed with virtual phase gates [83] (shown in yellow) comprising the n-type region used for photodiodes and the associated surface p+ pinning layer. By using a thin extension of the polysilicon gate into the photodiode, designated "pinching gate", a step in the channel potential is obtained by virtue of the effects of channel narrowing, as shown in Figure 4.5.

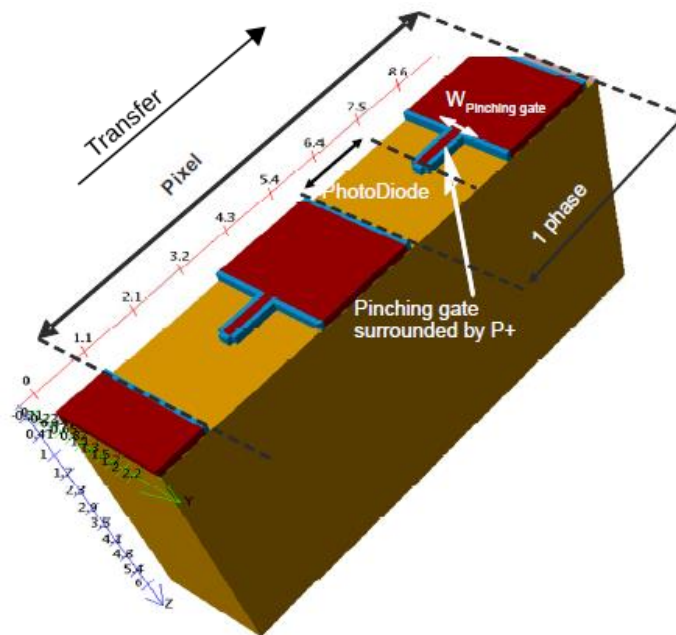


Figure 4.3: A 3D model of the virtual phase pixel implemented in a $0.18\mu\text{m}$ CMOS image sensor process designed by Mayer et al. [82]

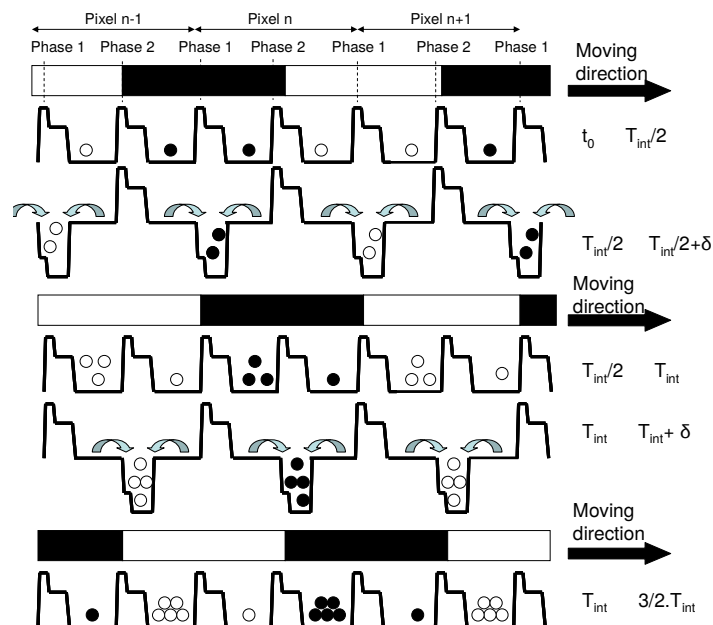


Figure 4.4: Clocking scheme for the virtual phase pixel sensor [82]

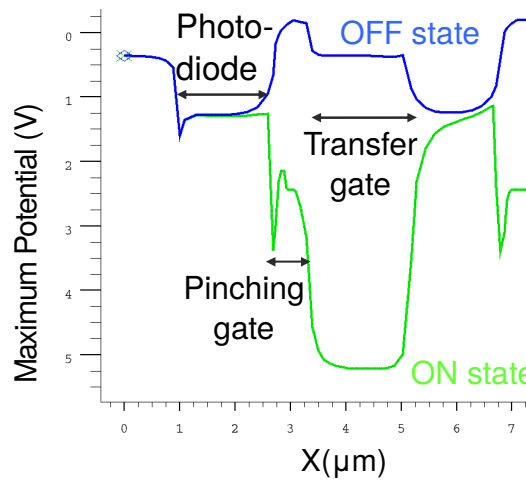


Figure 4.5: Simulated potential structure within the virtual phase pixel for clock high ("on") and clock low ("off") states [82].

A second possibility is to simply fabricate an all-electrode structure using etched gaps between the electrodes (in a similar manner to the fabrication methods used in the early days of CCDs), as shown in Figure 4.6. In CMOS the polysilicon is normally doped after definition, at the same time as forming the adjacent silicon source-drain regions of a transistor, and a proprietary technique is required to dope only the polysilicon electrodes, as there should be no doping in the adjacent gaps.

Charge transfer is now possible using the classic four phase clocking, as shown in Figure 4.7.

The primary advantage of using CMOS technology for TDI mode sensors is that the high level of integration and small feature sizes (typically $0.18\ \mu\text{m}$ or below) compared to the pixel width (typically greater than $3\ \mu\text{m}$) can easily allow column-parallel readout (i.e. an output circuit at the end of each transfer column). This removes the need for a serial register (although it can increase the power consumption). Consequently, CTI does not limit the number of columns and wide devices can be produced. Furthermore, the small feature sizes available in CMOS allow for smaller pixels, which can increase the horizontal resolution and potentially reduce vertical motion blur. On top of this, all the usual advantages of CMOS

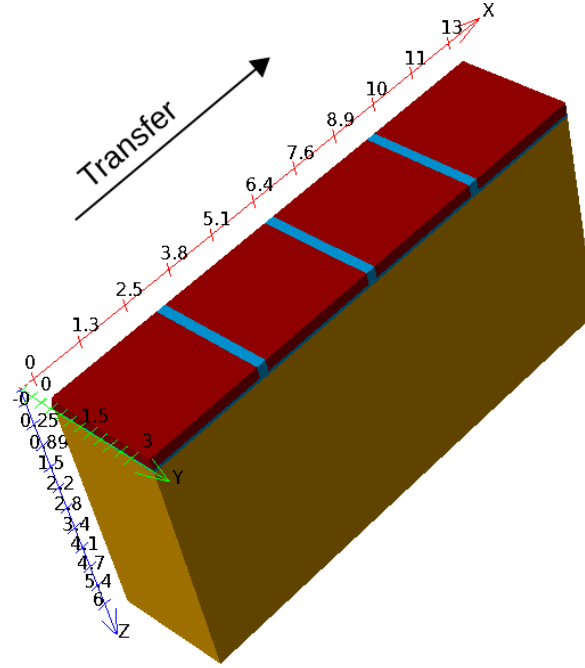


Figure 4.6: A 3D model of the four phase pixel implemented in a $0.18\mu\text{m}$ CMOS image sensor process designed by Mayer et al. [82]

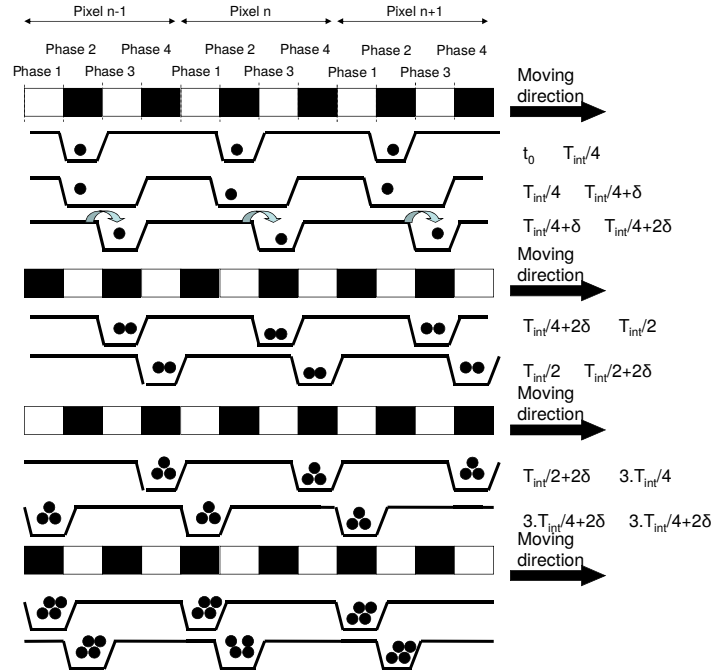


Figure 4.7: Clocking scheme for the four phase sensor [82]

apply: radiation hardness (particularly to ionising radiation), lower power consumption, extra on chip systems (clock drivers, ADCs, signal processing), lower cost etc..

4.3 Experimental details and initial characterisation

4.3.1 Prototype TDI CMOS image sensor

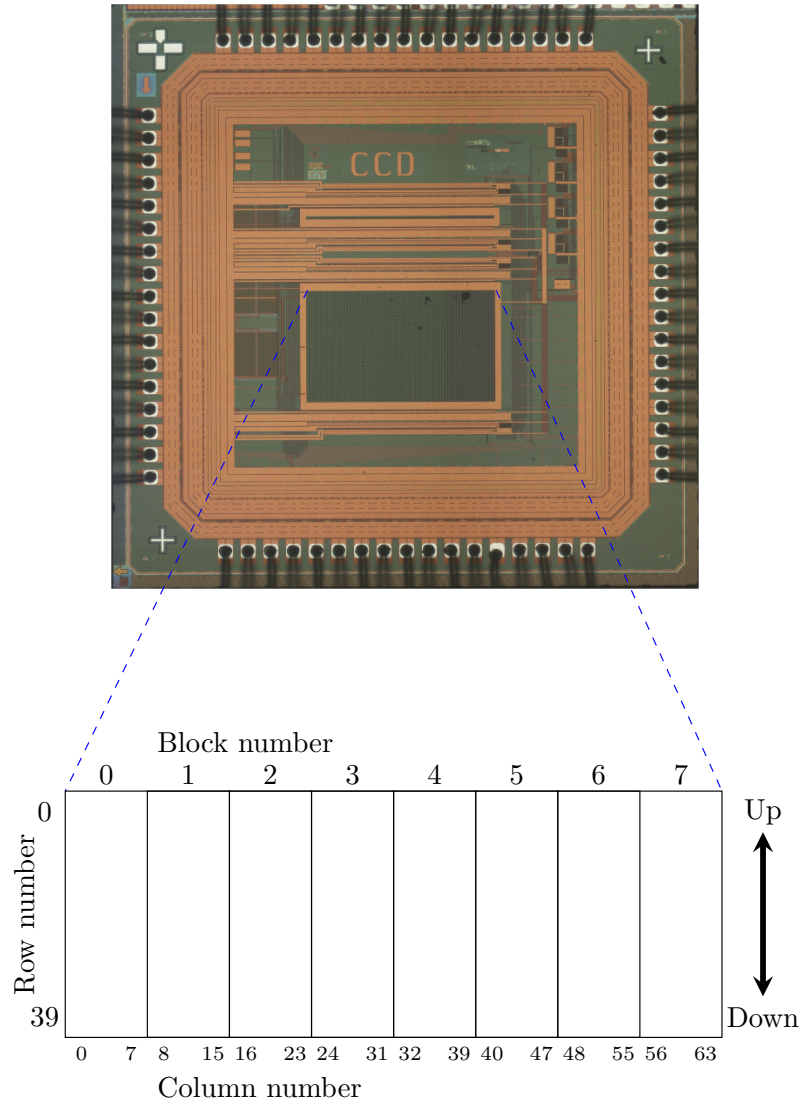


Figure 4.8: Chip micrograph showing the location of the 64×40 pixel array (top) and the arrangement of the design blocks (bottom).

The sensor used in this work [82] [84] (Figure 4.8) is a TDI mode CCD-style image sensor chip designed by e2v technologies. The chip uses $13\mu\text{m}$ pixels and is built on a $0.18\mu\text{m}$ CMOS image sensor process. The pixel design is as shown in Figure 4.6, except with an anti-blooming gate and anti-blooming drain added. The prototype has two imaging

arrays on each chip: one with a single pixel row and one with 40 rows. The 64 columns are arranged into 8 design blocks, with each design block consisting of 8 columns.

The pixel full well capacity for the 5 V device is in the region of 110ke^- with Anti-Blooming (AB) disabled. A 3 V variant was also produced. In this work, 3 chips of the 5 V variety were characterised.

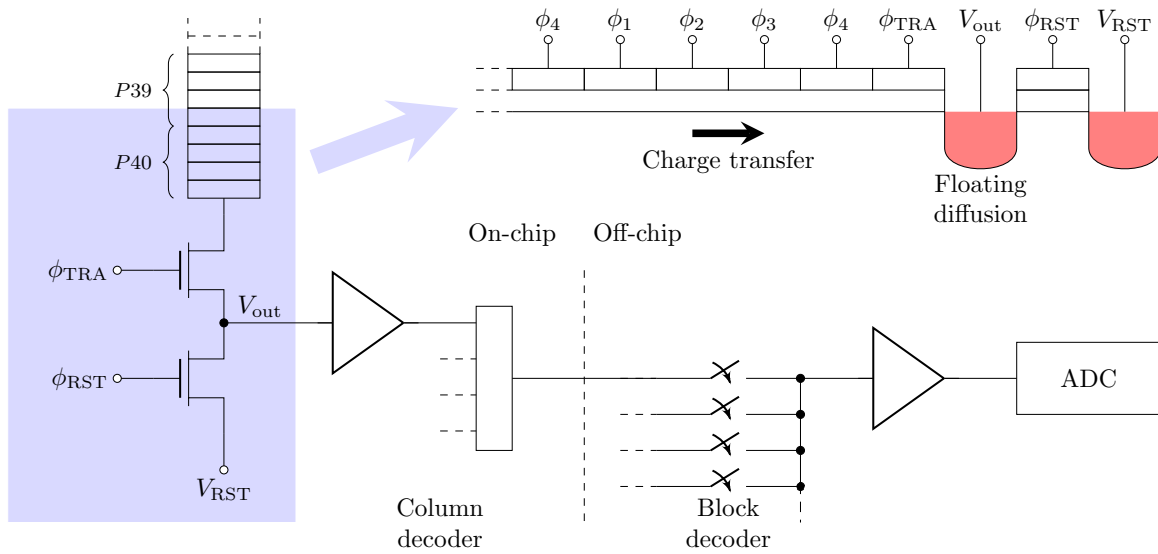


Figure 4.9: Pixel, transfer gate, and floating diffusion physical cross section (top). Read-out/injection circuitry (bottom).

The four phase buried channel CCD-style architecture (Figure 4.9) has readout circuitry consisting of a transfer gate driven by ϕ_{TRA} onto a floating diffusion and a reset gate driven by ϕ_{RST} . The floating diffusion feeds a charge-to-voltage amplifier on-chip. Column selection within each block is performed on chip. Each block output then goes to a separate pin on the device and the block can be selected off-chip.

The same readout circuitry is mirrored at the top and bottom of each column. If readout is in the "down" direction, charge injection can be performed for test purposes by lowering ϕ_{RST} and V_{RST} at the top of the column. Charge injection can be used to fill the pixels with charge for characterisation or testing purposes. The default transfer direction is "down", however the pixels can be clocked backwards and charge transferred in the "up" direction if

desired.

Block no.	0	1	2	3	4	5
AB gate	Buried	Buried	Buried	Surface	Surface	Surface
Interpoly gap (μm)	0.2	0.25	0.25	0.25	0.25	0.2
Wafer split	A	A	B	C	D	D

Table 4.1: Summary of the design choices for the six pixel designs studied in this work. Each wafer splits uses different implant conditions to achieve the doping of the buried channel.

Design blocks 0 to 5 consist of pixels as depicted in Figure 4.6 and are clocked using identical sequences. Blocks 6 and 7 were not studied in this work. The three principal design differences between blocks 0 to 5 are shown Table 4.1, namely AB gate type, inter-gate spacing (interpoly gap) and the implant conditions used on the wafer.

4.3.2 Camera electronics

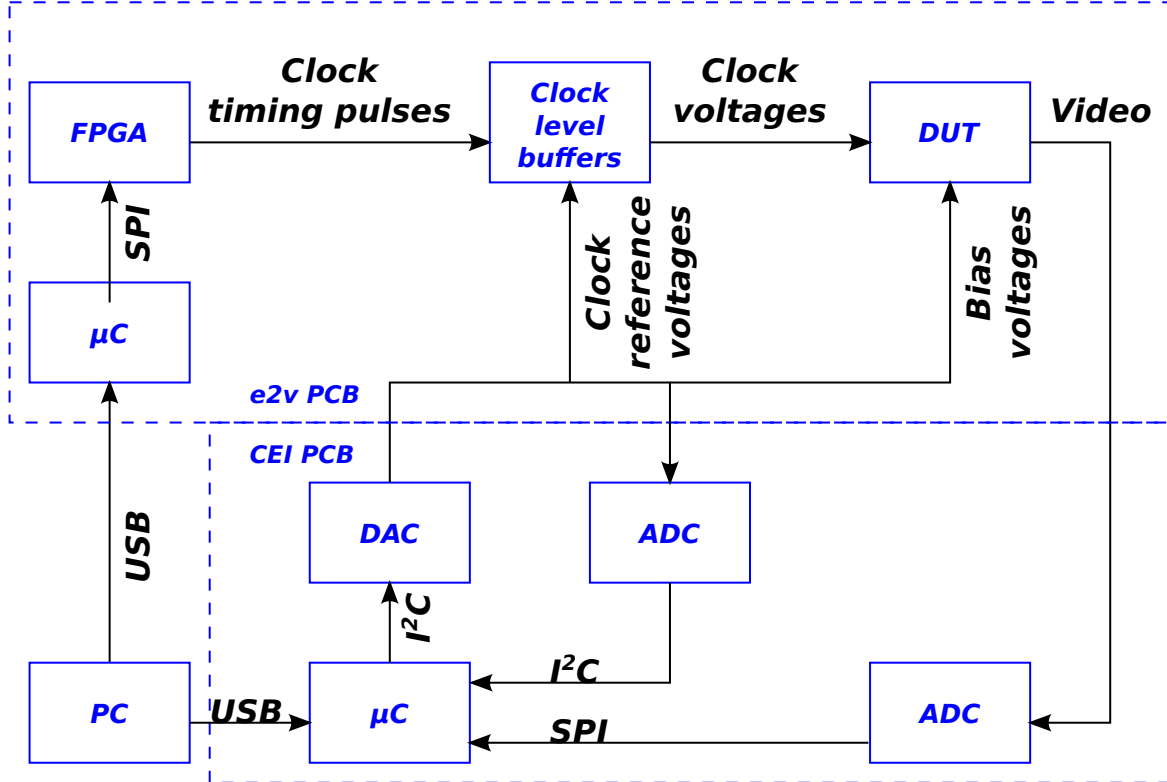


Figure 4.10: Equipment setup

An overview of the camera electronics is presented in Figure 4.10. A Field Programmable Gate Array (FPGA) generates the clock timing pulses for the sensor (Device Under Test or DUT) and these pulses are amplified to voltage levels determined by a Digital to Analogue Converter (DAC). Constant bias voltages are supplied directly from the DAC.

The e2v PCB (Printed Circuit Board) was provided along with the FPGA code. The CEI PCB design and assembly, Micro-Controller (μ C) code, further FPGA development, and the data acquisition software at the PC were done by the author.

The sensor output is buffered and then sampled by a 16-bit Successive Approximation Register (SAR) ADC (AD7980). The sample triggers are generated on the FPGA. Two samples are required (signal and reset) for each line period t_L . The maximum sample rate of the ADC was 1 Msample/s. Since the signal and reset sample points are not equally spaced the maximum practical line rate at the ADC was < 500 ksample/s. The sample rate was further limited by the μ C due to the time taken to respond to the interrupt from the sample trigger and subsequently retrieve data from the ADC.

The camera electronics allows only two columns from the sensor to be read out at once (information from the other columns is lost), although the output at the top and bottom can be read simultaneously, giving a total of 4 outputs. Only one output at a time was recorded by the single ADC. The signal and reset samples were subtracted digitally to perform basic digital CDS.

The waveforms used to clock the sensor are shown in Figure 4.11. In this work the line rate (number of pixels read per second) was maintained at $1/t_L = 12.5$ kHz. The clock resolution was $1.25 \mu\text{s}$ (1/64 of the pixel transfer time). A relatively long clock phase overlap of $5 \mu\text{s}$ was used.

Figure 4.11 shows clock waveforms at the end of an integration period, where charge is accumulated under phases ϕ_2 , ϕ_3 , and ϕ_4 . After the integration period, it is possible to inject charge into the first pixel by pulsing $RES0_U$ and TRA_U . The injected charge appears at

the output after 40 transfers.

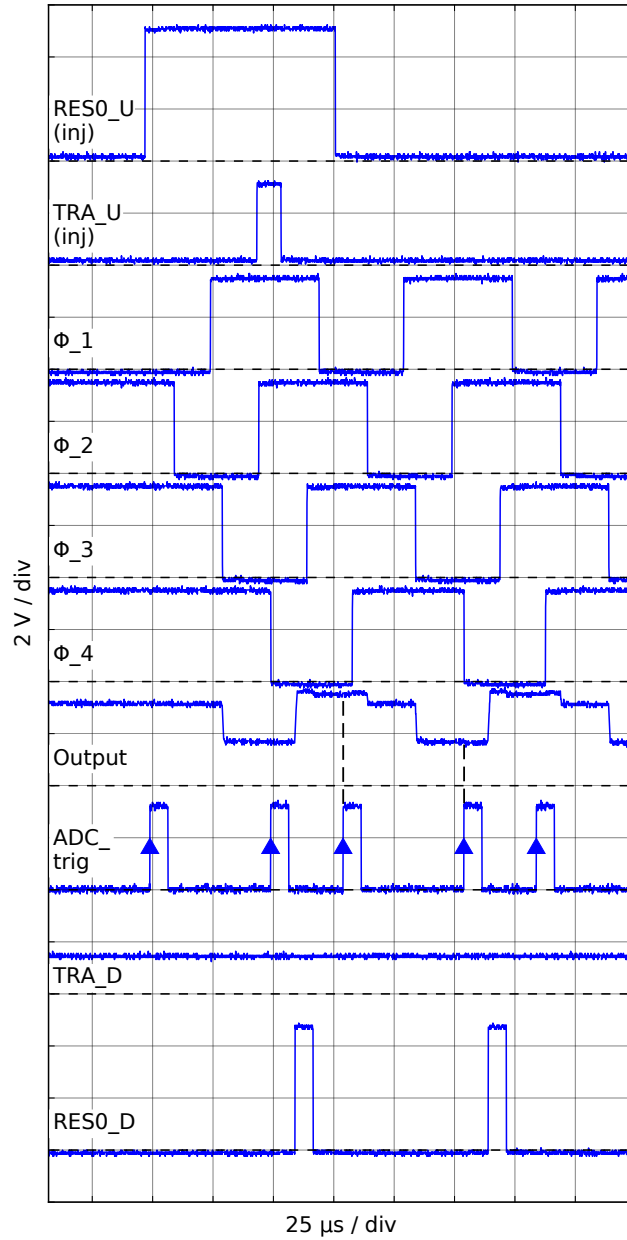


Figure 4.11: Charge is accumulated under ϕ_2 , ϕ_3 and ϕ_4 during integration. ϕ_1 acts as a barrier phase. Charge can also be injected under ϕ_1 if the top reset and transfer gates are clocked ($RES0_U$ and TRA_U). If $RES0_U$ and TRA_U are held low no charge is injected. The ADC sampling is on the rising edge of ADC_trig .

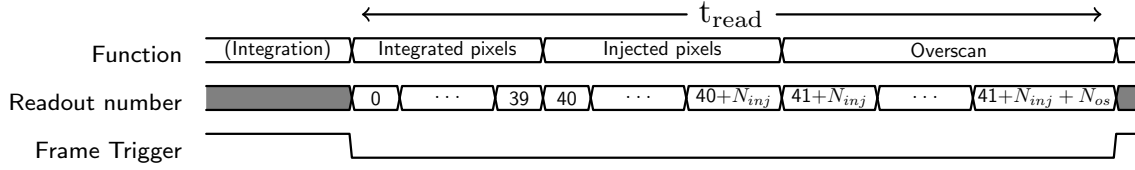


Figure 4.12: For testing purposes the sensor was driven to produce single column "frames" (as opposed to the constant read out which would be used for TDI). A frame consists of 3 sections which are read out in succession. After an integration time t_{int} the first section is read out which contains the signal gathered in the 40 pixels of the column during the integration time. The second section contains any injected signal. Injected signal appears at the output 40 transfers after it is injected at the top of the column. The number of injections $N_{inj} \geq 0$. Finally, a third section, the overscan, is read out, with length $N_{os} \geq 0$. After the overscan, integration begins again.

Signal	Voltage (V)	Function
VPHIG_High	3.6	Pixel clock high $V\phi$
VPHIG_Low	0	Pixel clock low
VPHITRA_Down	1.3	Column bottom ϕ_{TRA} high
V_READ/INJ	5	Amplifier bias
VPHITRA_Up_H	3	Column top ϕ_{TRA} high
VPHITRA_Up_L	0	Column top ϕ_{TRA} low
PHI_RES_H	5	Column bottom ϕ_{RST} high
D_R1_COM_EVEN	5	Column bottom even columns reset drains
D_R1_COM_ODD	5	Column bottom odd columns reset drains
V_INJ_40	5	40 row array column top reset drains
V_RST_40	3.6	40 row array column bottom reset drains
V_INJ_1	5	1 row array column top reset drains
V_RST_1	5	1 row array column bottom reset drains
V_Ampli	1	Amplifier bias
AB_Drain	4.1	Anti-blooming drains
VDD	5	Device power supply

Table 4.2: Clock and bias voltages.

Figure 4.12 shows the timeline in capturing each frame. Firstly, there is an integration period, during which no transfers occur. Then the integrated charge is read-out during the first 40 transfers. During this time, any number of charge injections N_{inj} can be made. These injected charges follow immediately after the first 40 read-outs. Any further read-outs are

designated overscan and contain no signal except the dark signal accumulated during the time taken to clock charge through the 40 pixels, $40t_L$. After the overscan, integration begins again.

Table 4.2 shows the reference voltages supplied to the camera board to provide the bias voltages and clock level references as specified for device operation.

4.3.3 Temperature control and light shielding

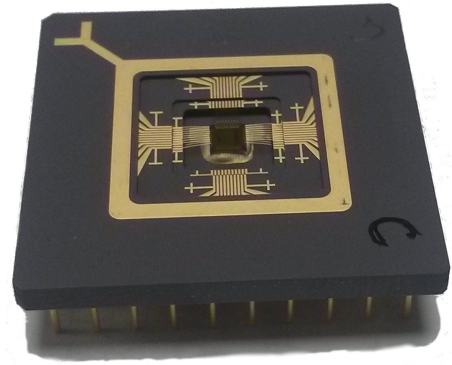


Figure 4.13: The TDI-CMOS chips are mounted in 25×25 mm ceramic packages. A temporary glass window was placed over the central area of the package (not shown).

All of the measurements described in this chapter were performed on devices in the dark, at 298 ± 1 K.

The chip package is shown in Figure 4.13. Light shielding was constructed from aluminium foil covering the front surface of the device. The effectiveness of this shielding was confirmed using a torch to illuminate the outside of the light shield.

The temperature stabilisation setup is shown in Figure 4.14. Temperature was measured using a Platinum Resistance Thermometer (PRT) fixed to a thermal mass. The thermal mass was attached to the glass window on the device package. A temperature controller reading the temperature of the PRT then drove a Peltier effect Thermo-Electric Cooler (TEC) which heated or cooled the thermal mass as required. The TEC was cooled with a fan and heatsink.

The temperature at the PRT could be consistently kept within 1 K of the set point of 298

K. The package temperature was also confirmed to be stable, by attaching a PRT to the edge of the ceramic package (not shown).

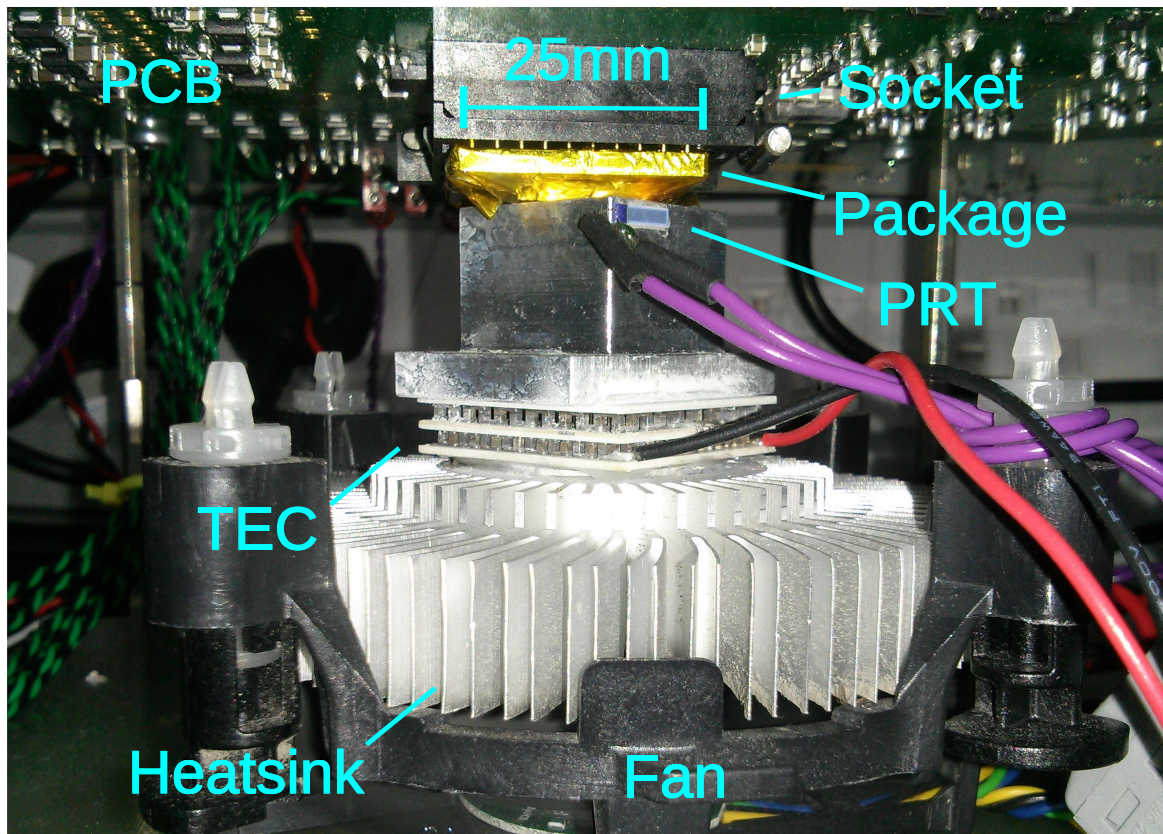


Figure 4.14: The temperature was stabilised by a TEC heating or cooling a thermal mass. The thermal mass was in contact with the glass window on the chip package. The temperature of the thermal mass was monitored by a PRT connected to a TEC controller. The TEC itself was cooled using PC fan/heatsink combination.

4.3.4 Characterisation by charge injection

During read out, a change of signal charge ΔQ on the floating diffusion produces a voltage swing

$$\Delta V = \frac{\Delta Q}{C_{FD}} \quad (4.1)$$

where C_{FD} is the floating diffusion capacitance. The Charge to Voltage conversion Factor (CVF) is the voltage produced at the output per signal electron (see Equation 2.4)

$$CVF = \frac{\Delta V}{\Delta n} \quad (4.2)$$

where V is the output voltage ($V_{reset} - V_{signal}$) and n is the number of signal electrons.

A value for CVF was obtained by measuring the reset current I_{RST} (see Figure 4.9). For a constant signal level of n electrons the current drawn from the reset drain is

$$I_{RST} = qnf \quad (4.3)$$

where f is the pixel rate. The actual measurement was done using a sequencer with an overscan of length $N_{os} = 60$ such that a signal was present for a fraction of the time $\delta = 40/(40 + N_{os}) = 0.4$ and the signal was approximately zero for the remaining fraction time $1 - \delta = 0.6$. The current is then

$$I_{RST} = qnf\delta \quad (4.4)$$

Combining equations 4.2 and 4.4 produces

$$CVF = \frac{qVf\delta}{I_{RST}} \quad (4.5)$$

Figure 4.15 shows the reset drain pin current measured with a Keithley 486 picoammeter as a function of output voltage. The pin provides current to the 8 drains in a block. The

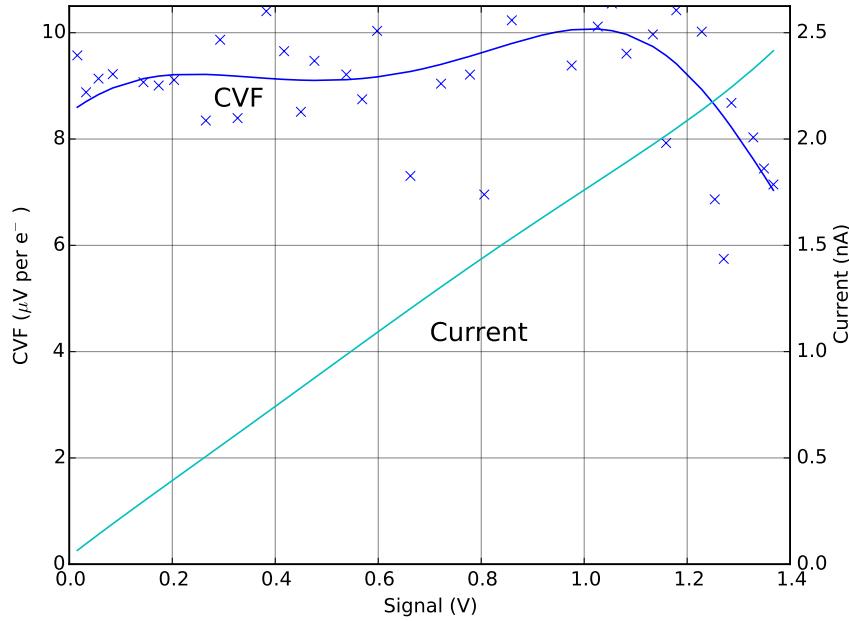


Figure 4.15: Current measurement into the reset drain can be used to determine the CVF. Here, the CVF data points are shown as well as a fit to the data points (shown here for chip 1, block 1, column 3). The CVF varies with the voltage, probably due to the floating diffusion capacitance C_{FD} being voltage dependent. The mean CVF for this column is $9.13 \mu\text{V}/e^-$ with a 95% confidence interval of between 8.73 and $9.53 \mu\text{V}/e^-$

computed CVF from the local slope of the current is also shown on the same graph. The CVF varies a little over the range and decreases suddenly as full well is approached. The relationship between output voltage and integration time is linear. The non-linear reset current (seen as the variation of CVF with signal) could be due to C_{FD} being a function of V .

4.3.5 Characterisation by mean-variance curve

An alternative way to calculate CVF is the mean-variance curve (also known as a Photon Transfer Curve or PTC) [85]. The standard mean-variance curve is obtained by measuring the signal mean and variance over a range of illumination levels. An idealised mean-variance curve is shown in Figure 4.16.

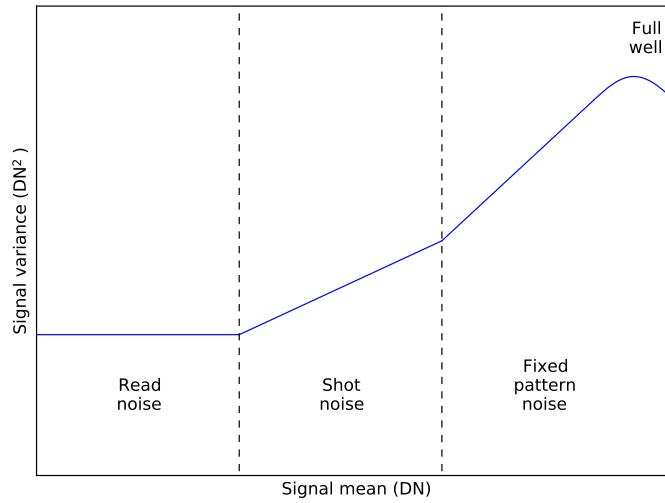


Figure 4.16: An idealised mean-variance curve. At low signal read noise dominates, and the read noise variance can be read from the graph. The gradient in the shot noise dominated region can be used to calculate the CVF (in units of DN/e^- or $\mu\text{V}/e^-$). Variance increases in the fixed pattern noise region until the onset of full well when the variance begins to fall. The FWC can also be read from the graph.

The signal mean and variance are usually calculated over the pixels in a single frame (with zero-offset correction). This makes sense in a large format device but, since there are only 40 pixels read-out in a frame on the TDI-CMOS sensor, multiple frames must be used to gain sufficient statistics. The mean variance curve shown in Figure 4.17 was constructed using 100 frames at each illumination level. The signal mean and variance were calculated on a per pixel basis, meaning that there is no fixed-pattern noise region. The read noise region is also not visible because the integration time could not be made short enough to reduce dark current to negligible levels. The high dark current (at room temperature) means that the signal cannot be made small enough for the read noise to dominate.

The mean-variance curve in Figure 4.17 has two regions. The first region is shot-noise limited. In the shot-noise limited region the signal variance σ^2 (in units of electrons squared) is equal to the signal mean μ (in units of electrons). The convention is that image sensor ADC outputs are in units of Digital Number (DN) (equivalent to the least significant bit). A

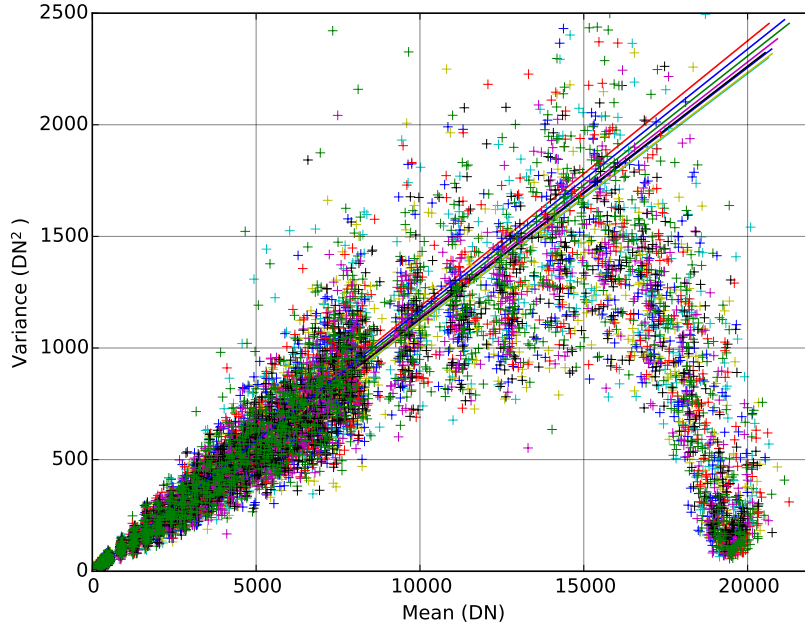


Figure 4.17: Mean-variance curve. A linear fit to mean signal values from 0 to 12,000 DN was used to compute a CVF estimate of between 8.50 and 9.06 $\mu\text{V}/e^-$ (0.111 and 0.119 DN/e^-), depending on the column. This curve is obtained by plotting mean and variance of each of the 40 pixels obtained over 100 frames for the 8 columns in chip 1, block 1. Each line is the fit for a single column.

factor c in units of DN/e^- can then be found from the gradient

$$c = \frac{d\sigma^2}{d\mu} \quad (4.6)$$

The CVF is then

$$CVF = d.c \quad (4.7)$$

expressed in units of $\mu\text{V}/e^-$ where d is the ADC conversion gain in units of $\mu\text{V}/\text{DN}$.

A linear fit to the shot noise region in the mean-variance curve shown in figure 4.17 produces an estimate for the CVF of between 8.50 and 9.06 $\mu\text{V}/e^-$ for each of the 8 columns in chip 1, block 1. This is close to the range of values found in Figure 4.15 by measuring the reset current. The value for column 3 is 8.67 $\mu\text{V}/e^-$. This is not with the 95% confidence

interval of for the mean CVF value found by the reset current method. However, an estimate of CVF to within 10%-20% of the true value using the mean-variance method is expected [3, pg. 108].

4.4 Pre-irradiation characterisation

This section describes the measurement of the dark current and CTI of the TDI-CMOS sensor before proton irradiation.

4.4.1 Dark current measurement

The dark current density (units of nA cm^{-2}), often simply called dark current, can be calculated by measuring the gradient of sensor output vs. integration time, over a linear part of the curve (see Figure 4.18). The dark current can be calculated for each pixel.

The dark current density is given by

$$J_{dark} = -\frac{dQ}{dt} \frac{1}{A_{pix}} \quad (4.8)$$

where $Q = ne$ is the charge on the n signal electrons, t is the integration time and A_{pix} is the pixel area. The pre-irradiation dark current in the TDI-CMOS sensor at 25°C is approximately 20 nA cm^{-2} . Typical dark current in a PPD CMOS image sensor at 27°C is 0.1 nA cm^{-2} [86]. The difference is due to the TDI-CMOS CCD structure having a depleted surface, whereas the PPD in the CMOS sensor has a pinned structure, which suppresses this component. Dark current is discussed more in section 4.5.1.

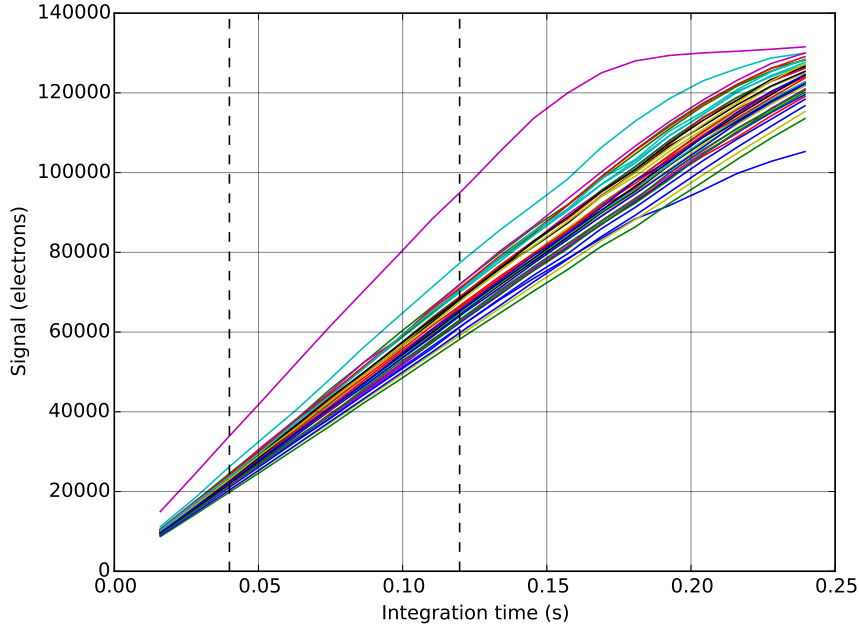


Figure 4.18: Dark current is calculated from the gradient of signal vs. integration time. Results here are for all 40 pixels in chip 3, block 1, column 1. Dashed lines show the two integration times between which the slope was used to calculate the dark current.

4.4.2 CTI measurement

In an ideal CCD pixel, when a signal charge packet is clocked from one pixel to the next, all of the charge packet is transferred. In reality, the charge transfer is not always complete. Some charge is "deferred". The CTI per pixel, denoted ϵ , is a measure of the incompleteness of charge transfer and is defined as

$$\epsilon = \frac{n_{def}}{n_{sig}} \quad (4.9)$$

where n_{sig} is the charge packet signal which should be transferred, and n_{def} is the amount of charge which is deferred after each transfer. ϵ is dependent on the signal level n_{sig} , since n_{def} is not necessarily proportional to n_{sig} (see Figure 4.21). The capture and emission of electrons by traps within the transfer channel, which is responsible for CTI, happens at random times (with time constants τ_c and τ_e). Therefore, CTI is dependent on the history of all preceding transfers through the pixel. The practical implication of these effects is that

values of CTI obtained will depend on the measurement technique used. They will also depend of course on factors such as line rate and dark current signal level (dark current signal level is critical for X-ray CTI measurement).

Extended Pixel Edge Response (EPER) [3] was used as the measurement technique for CTI in the TDI-CMOS devices. This method is described in the next section. Another common method, used in CCDs, is to use an X-ray source to produce a known signal across the sensor. There is a signal loss as the X-ray produced charge packets are clocked through the CCD, due to deferred charge. The total amount of charge deferred is greater for pixels located far from the read out node. The spatial gradient of signal level can therefore be used to determine the CTI. EPER has the advantage of easily adjusting the signal level. Also, X-ray detection is less efficient in CMOS because of lower depletion depths. A high X-ray flux would also have been needed due to the small pixel array size.

4.4.3 EPER

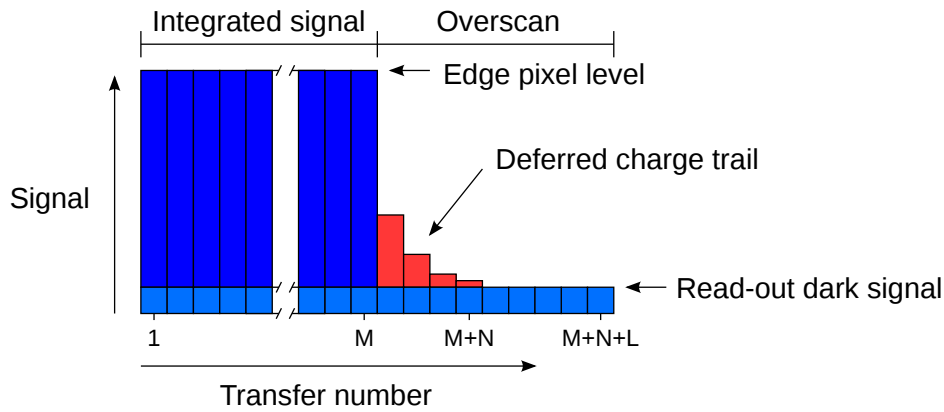


Figure 4.19: CTI can be calculated from a frame using EPER. The deferred charge is found in the N transfers following the edge pixel transfer. The read-out dark signal in the overscan (which is the dark signal accumulated during readout) indicates the zero-signal level.

An EPER measurement can be performed by capturing frames complete with overscan (as shown in Figure 4.12). The principle is shown in Figure 4.19. Each of the $M=40$ pixels in

the array contains the signal n_{sig} , which is either generated from flat-field illumination or by dark signal during the integration period. The subsequent read outs contain the sum of the deferred charges from each of the 40 pixels, which form a "charge trail" which decays to the zero-level after a few transfers. The zero-level n_{ds} is equal to the dark signal accumulated during the 40 transfers at the line rate $1/t_L$.

The CTI calculated by EPER is defined as

$$\epsilon_{EPER} = \frac{\sum n_{def}}{M n_{sig}} \quad (4.10)$$

where $\sum n_{def}$ is the total amount of deferred charge measured after all M pixels have been read out.

The original peak signal n_{sig} is not seen at the output, since charge deferred reduces the measured signal level. However, the amount of deferred charge is usually small compared to the signal size. The Charge Transfer Efficiency (CTE) defined as $\alpha = 1 - \epsilon$ can therefore be approximated as unity so that the n_{sig} can be measured as the M^{th} pixel read out (the last element before the overscan)

$$n_{sig} = n[M] \approx \alpha^M n_{sig} \quad (4.11)$$

where $n[i]$ is the output after the i^{th} transfer.

Using the approximation for n_{sig} in Equation 4.11, the amount of deferred charge can be found by summing the first N samples of the overscan

$$M \epsilon_{EPER} n_{sig} = \sum_{i=M+1}^{M+N} (n[i] - n_{ds}) \quad (4.12)$$

where N is the number of transfers required for the charge trail to become invisible above the noise floor. An estimate for the zero-level n_{ds} is computed in the same frame using the

mean

$$\overline{n_{ds}} = \frac{1}{L} \sum_{i=M+N+1}^{M+N+L} n[i] \quad (4.13)$$

where $M + N + L$ is the total frame length.

4.4.4 Experimentally obtained EPER trails

The signal used for EPER was generated in the dark, since the first and last pixels in each column were partly shielded from light, making flat field illumination impractical. The integrated dark signal up to approximately 33 ke^- can be seen in Figure 4.20. The effect of DSNU can be seen and the actual signal level in each pixel varies by up to approximately 10% from the maximum.

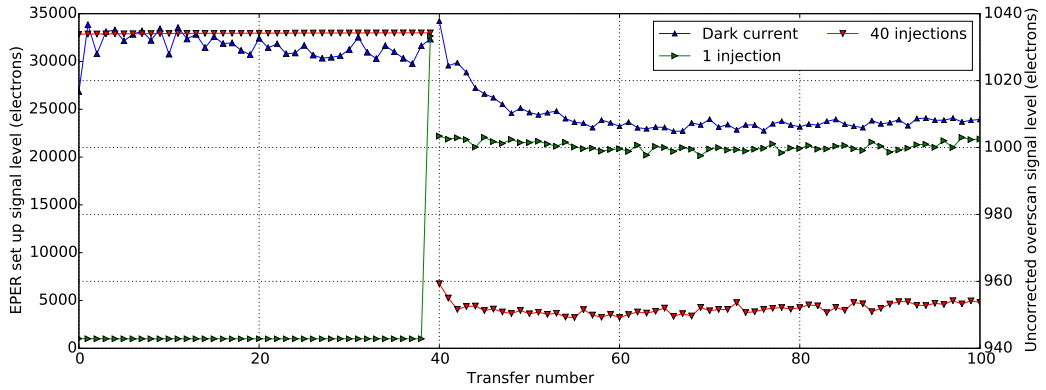


Figure 4.20: Signals used for EPER measurement (left hand scale, transfer number ≤ 40) and the resulting charge trails (right hand scale, transfer number ≥ 40). There is a discrepancy between the charge trail sizes despite the fact that the final signal level is the same (33 ke^-) in each case. A further anomaly is that the zero-signal level at the end of the overscan is different in each case, and changing over time.

When using EPER, an assumption is made that, as long as the final signal (before the overscan) transferred through each pixel is the maximum signal, it is irrelevant what the preceding signals were. This assumption is considered valid given that electron capture times are very short in comparison to the line rate. An attempt was made to create the same signal level using three methods: dark-current integration; a single charge injection pulse;

and 40 charge injection pulses. In each case the same final signal is achieved. Figure 4.20 shows experimentally obtained charge trails resulting from each the three signal generation methods. The charge trail magnitude is significantly different for each of the three methods. This is an unexpected result and is not well understood. Further EPER measurements were performed using the dark signal generation method, since this method is most commonly used in CCD sensors where charge injection may not be practical.

A further complication can be seen in the discrepancy between final overscan values. Further investigation showed that, after sufficient settling time, the overscan in each case settles to the same value. Unfortunately, the shape of the overscan, which is never completely flat, was found to be dependent on the signal level, on the integration time, and on the total length of overscan. Because the same signal was reached with a shorter integration time in the sensor post-irradiation (due to increased dark-current), the overscan shape was different for the same signal level pre- and post-irradiation. This unusual behaviour of the overscan was not fully explained and to the author's knowledge has not been reported in either CCD or CMOS devices.

The first method used was to select the first N overscan elements as the charge trail. A fit to the next L elements were then backwards-extrapolated in a straight line. This straight line was then subtracted from the charge trail. L was chosen to be 10.

Figure 4.21 shows how N affects the measurement of deferred charge. It can be assumed that the actual amount of deferred charge is a monotonically increasing function of signal and that any deviation is due to an experimental error. Lower N reduces the amount of "noise" on the deferred charge estimation. However, a low N also tends to give a lower estimate of the magnitude of deferred charge, but the trend is the same and the difference is small. Results are for an irradiated device.

A better method, shown in Figure 4.22, was to fit a function $f_{fit}(x) = Ae^{-Bx} + Cx + D$ and remove the exponential term to give the function $f_{offset} = Cx + D$ as an estimate for the

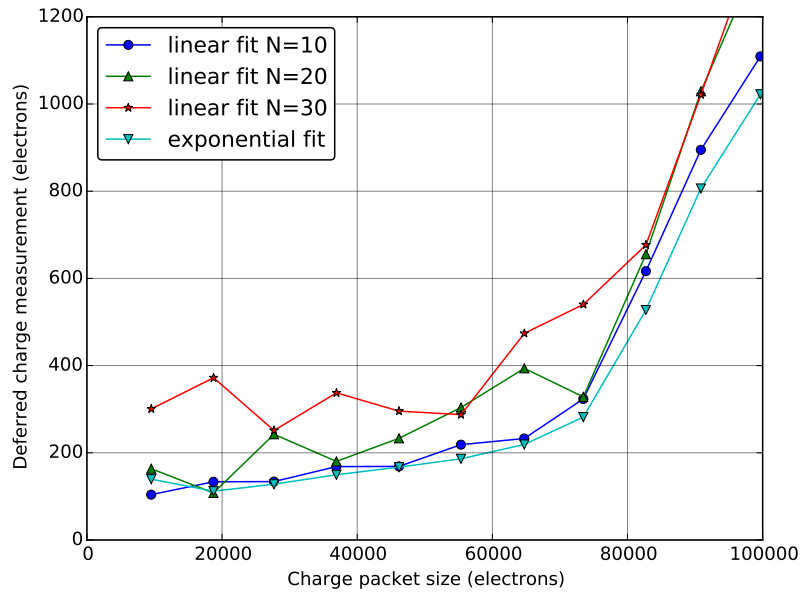


Figure 4.21: Deferred charge magnitude as estimated using three different charge trail length estimates (N) for a simple linear fit and an improved exponential fit. The quantity of deferred charge increases rapidly when the signal size exceeds 70 ke^- as electrons start to be trapped at interface states due to the growing charge cloud volume extending up to the interface. Below 70 ke^- the quantity of deferred charge rises slowly, signifying that the charge cloud is growing only a small amount and in a volume of constant trap density. In this region the CTI is approximately proportional to $1/n_{sig}$.

offset to be subtracted. The amount of deferred charge was calculated from the total sum of the charge trail minus the offset function. Results from this method are shown in Figure 4.21.

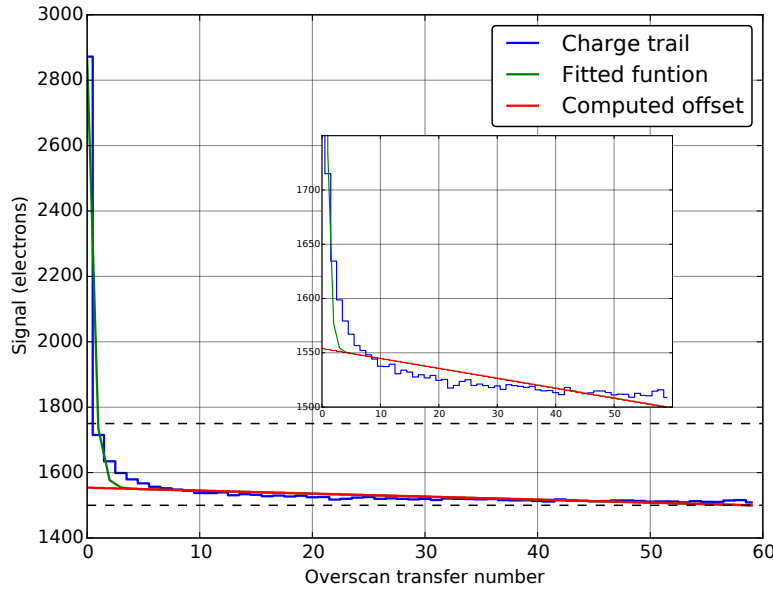


Figure 4.22: EPER charge trails did not decay to a constant value. Therefore, a fitting function was required to estimate a suitable offset for summation of deferred charge. The fitted function eventually used was $f_{fit}(x) = Ae^{-Bx} + Cx + D$, where A, B, C, and D were all fitting parameters and x the transfer number. $f_{offset}(x) = Cx + D$ was used as the offset function. The inset shows the overscan in more detail.

4.4.5 Design and operation effects on CTI

Figure 4.23 shows the CTI (measured by EPER) against signal level for 6 of the different pixel designs on the chip, listed in Table 4.1. CTI was averaged across columns in the same design block. The sharp increase in CTI for large signals indicates the onset of saturation at Full Well Capacity (FWC). The FWCs of the pixel designs show some variation but the mid signal CTI is similar across designs at $< 2 \times 10^{-4}$. Block 2 has the lowest CTI but also the lowest FWC, which may be linked.

As explained in the next section, 3 devices were characterised for this work. The performance of each device was similar. However, there was enough variation in the pre-irradiation CTI to make the pre-irradiation CTI value for each device important when evaluating the increase in CTI due to proton irradiation. The individual behaviour of different

design blocks was repeated across the devices.

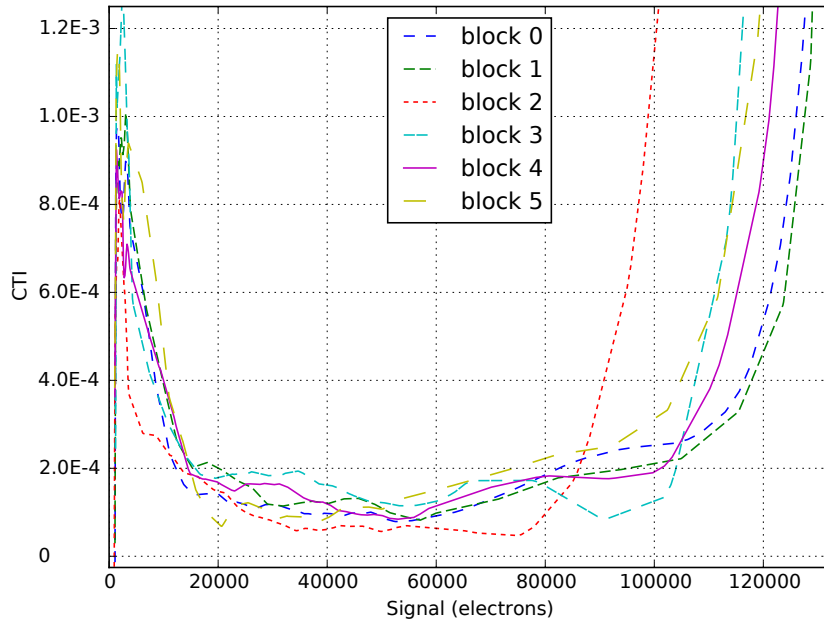


Figure 4.23: CTI vs. signal for 6 blocks. Block 2 (implant split B) has a lower FWC but best CTI. Blocks 0 and 1 and blocks 4 and 5 share implant splits (A and D) and have similar FWC. There is no clear correlation between either the interpoly gap or the anti-blooming gate choices and the FWC or CTI.

Figure 4.24 shows how CTI is affected by a change of clock voltage V_ϕ for design block 0. An increase in FWC can be seen as V_ϕ is reduced. This is consistent with the signal packet moving closer to the Si-SiO² interface as clock voltage is increased and indicates that the FWC is limited by surface full well as opposed to bloomed full well [87]. Bloomed full well would be due to the potential in the pixel being reduced by the presence of signal electrons, to the point where further electrons would bloom into neighbouring pixels (or flow into the anti-blooming drain in this case). Bloomed full well capacity would increase with V_ϕ .

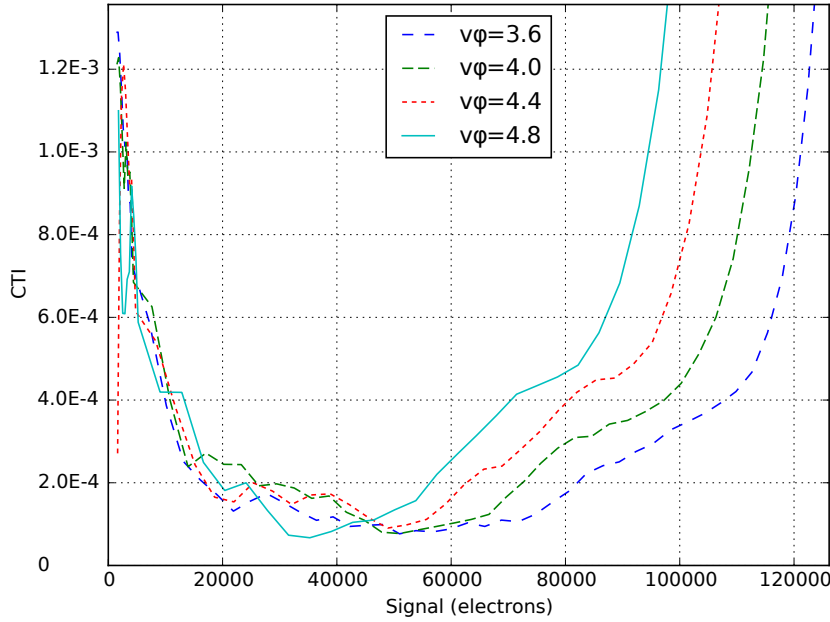


Figure 4.24: Increasing V_{ϕ} causes the signal packet to be transported closer to the surface which causes a reduction in FWC as excess charge becomes trapped in interface states causing the onset of surface full well.

4.5 Post-irradiation characterisation

In order to assess the suitability of the TDI-CMOS sensor for use in low earth orbit applications two test devices were irradiated with 74 MeV protons at the Paul Scherrer Institut in Switzerland. The 10 MeV equivalent fluences used were $5 \times 10^9 \text{ cm}^{-2}$ and $1 \times 10^{10} \text{ cm}^{-2}$. For comparison, the Hubble space telescope experiences a 10 MeV equivalent fluence of approximately $1 \times 10^9 \text{ cm}^{-2}$ per year [88].

The irradiations for this chapter were carried out by Matthew Soman and George Winstone of the CEI, as per the author's instructions (Figure 4.25). The irradiations were performed with the devices unbiased, at room temperature. The storage temperature was not controlled, except for the usual precautions. The maximum storage temperature was below 300 K.

After this irradiation it was found that the increase in CTI was only small (see Section

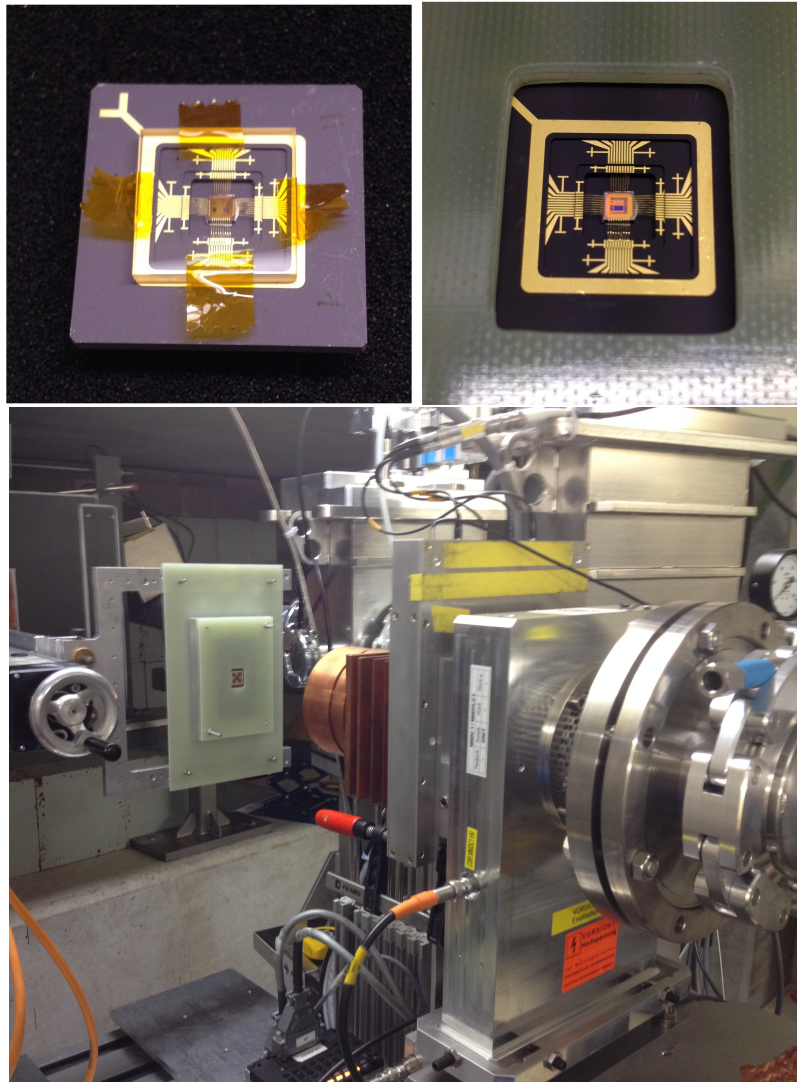


Figure 4.25: TDI-CMOS device with protective window (above left) and with window removed, mounted for proton irradiation (top right). Device mounted at the beam-line ready for irradiation (below).

4.5.3). In light of this result a second irradiation was carried out on the same devices to 10 times higher total fluences ($5 \times 10^{10} \text{ cm}^{-2}$ and $1 \times 10^{11} \text{ cm}^{-2}$). A summary of the fluences given to the 3 devices is given in Table 4.3.

Device marking	Voltage (Batch)	Characterised	Proton irradiation (cm^{-2}) (10 MeV equiv.)
1 (back)	5 V (1)	Yes	-
2 (back)	5 V (1)	Yes	5×10^9 , 5×10^{10}
3 (back)	5 V (1)	Yes	1×10^{10} , 1×10^{11}

Table 4.3: TDI CMOS devices used in this work and summary of irradiations.

4.5.1 Dark current

The average dark current at 25 °C was measured before irradiation at around 20 nA cm^{-2} .

This is equivalent to $\approx 211 \text{ ke}^- \text{ pixel}^{-1} \text{ s}^{-1}$, or 676 e^- after 40 transfers at $1/t_l = 12.5 \text{ kHz}$.

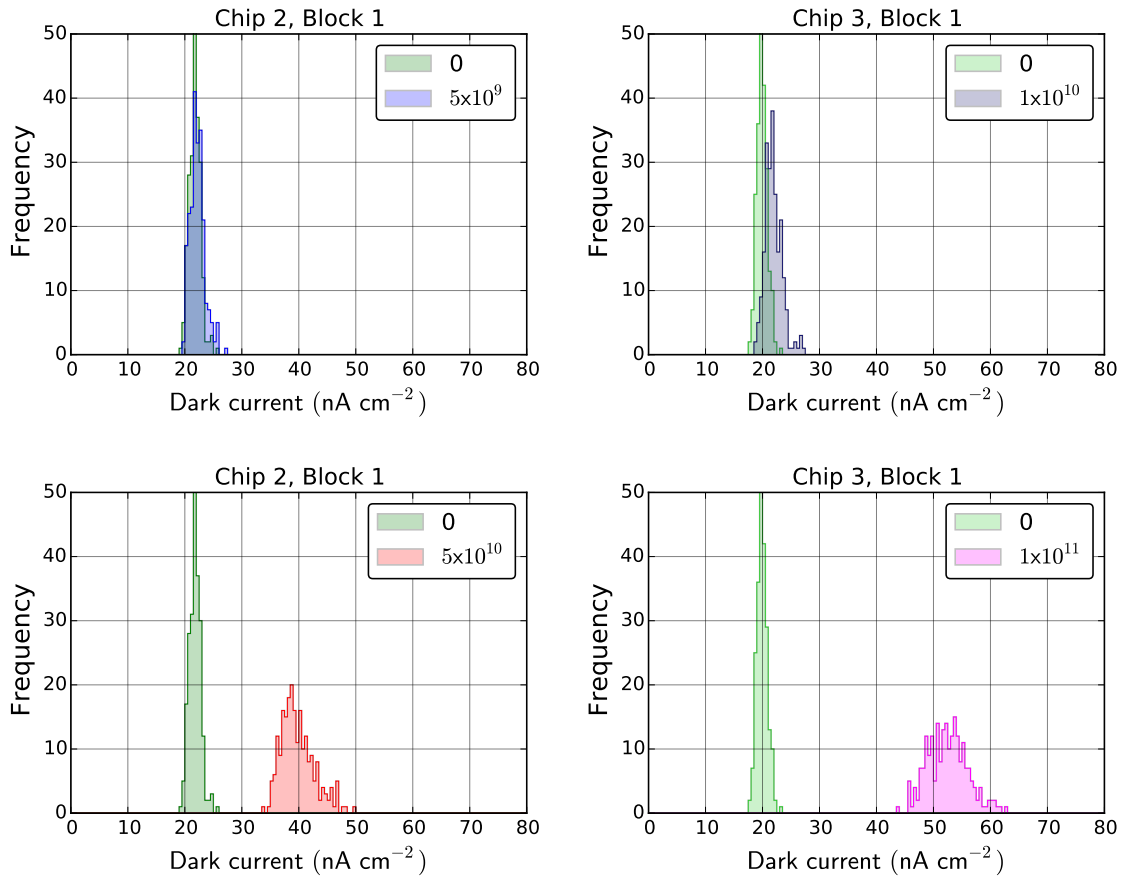


Figure 4.26: Dark current at 298 K in design block 1. Left: results for chip 2 pre-irradiation and at the two 10 MeV proton equivalent fluences of $5 \times 10^9 \text{ cm}^{-2}$ and $5 \times 10^{10} \text{ cm}^{-2}$. Right: results for chip 3 pre-irradiation and at $1 \times 10^{10} \text{ cm}^{-2}$ and $1 \times 10^{11} \text{ cm}^{-2}$.

The dark current increased by 10-15% after the first irradiation to a 10 MeV equivalent proton fluence of $1 \times 10^{10} \text{ cm}^{-2}$ in chip 3. After the second irradiation, to $1 \times 10^{11} \text{ cm}^{-2}$, the mean dark current had increased beyond its pre-irradiation value by 100-150%. Dark current histograms, for design block 1, for pre-irradiation and for both fluences used in chips 2 and 3 are shown in Figure 4.26. After a 10 MeV equivalent proton fluence of $1 \times 10^{11} \text{ cm}^{-2}$ bright pixels are starting to be seen.

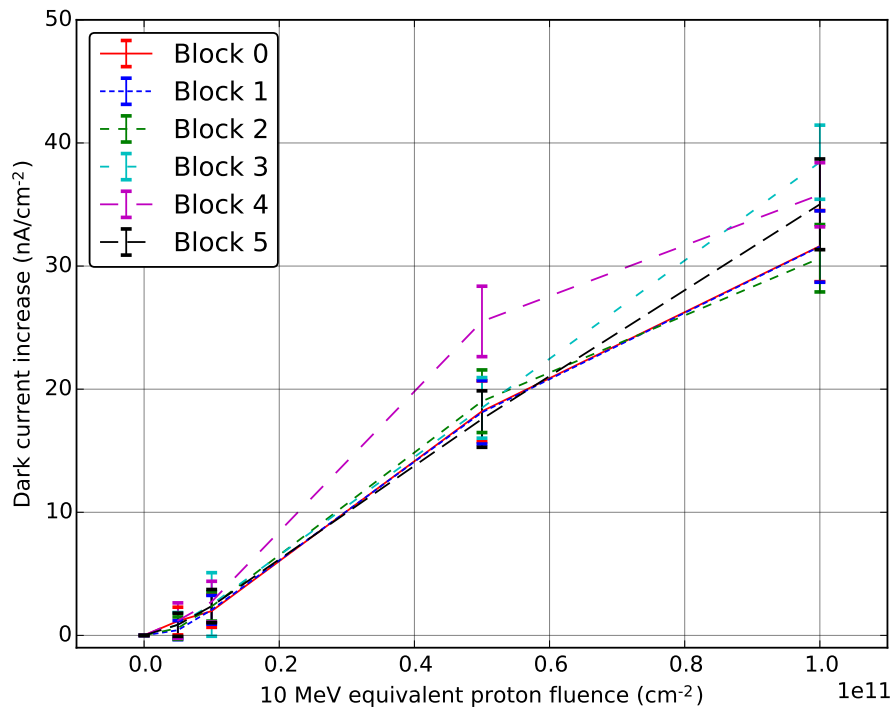


Figure 4.27: Mean dark current increase for each of the 6 design blocks at all fluences. The dark current increase is similar in each block.

The increase in dark current was different for each design block, and the Dark Signal Non-Uniformity (DSNU) increased considerably. In block 1 on chip 2 the dark current range increased from 7 nA cm^{-2} pre-irradiation to 16 nA cm^{-2} at the final fluence. In chip 3 the dark current range increased from 6 nA cm^{-2} pre-irradiation to 19 nA cm^{-2} at the final fluence. The mean dark current increase in all blocks at each fluence for chips 2 and 3 is shown in Figure 4.27. In all design blocks the proportional dark current increase was

greater at the higher fluence which could be due to a saturation or annealing effect.

The mean dark current increase at the highest fluence ranged between 31 to 38 nA cm⁻², which is approximately a doubling of dark current.

4.5.2 Dark current CCD comparison

In order to compare the TDI-CMOS sensor with standard CCD technology, some dark frames were analysed from an e2v CCD201 Electron-Multiplication CCD (EMCCD). The CCD201 has a pixel size of 24 $\mu\text{m} \times 13 \mu\text{m}$. The data were provided by Nathan Bush of the CEI.

Since the CCD201 was run in inverted mode, the dark current pre-irradiation was far lower in the CCD201 than in the TDI-CMOS sensor, where the surface is not pinned.

The CCD201 was operated without electron-multiplication gain at a range of temperatures between -120 °C and 20 °C. Half of the CCD had been subject to a proton irradiation to a 10 MeV equivalent fluence of $1 \times 10^9 \text{ cm}^{-2}$, while the rest of the sensor was shielded from radiation.

CCD dark current in the depletion region was approximated by [89].

$$J = aT^n e^{-\frac{E_G - E_T}{kT}} \quad (4.14)$$

where k is Boltzmann's constant, E_G is the band gap, E_T is the defect energy and a and n are constants.

The dark current in the CCD201 is plotted as a function of temperature in Figure 4.28. For a CCD operating in inverted mode the dark signal is generated in the bulk and has two components [90]: below $T \approx 240 \text{ K}$ the depletion current dominates; and above $T \approx 240 \text{ K}$ diffusion current dominates. This is because of the different activation energies of each component is different. The transition between the two components can be seen at around

240 K in Figure 4.28. The fitted curve in Figure 4.28 show uses equation 4.14 with $a = 1.57 \times 10^3 \text{ A cm}^{-2} \text{ K}^{-1}$, $n = 0$ and $E_G - E_T = 0.76 \text{ eV}$ to fit the data above $T=240 \text{ K}$.

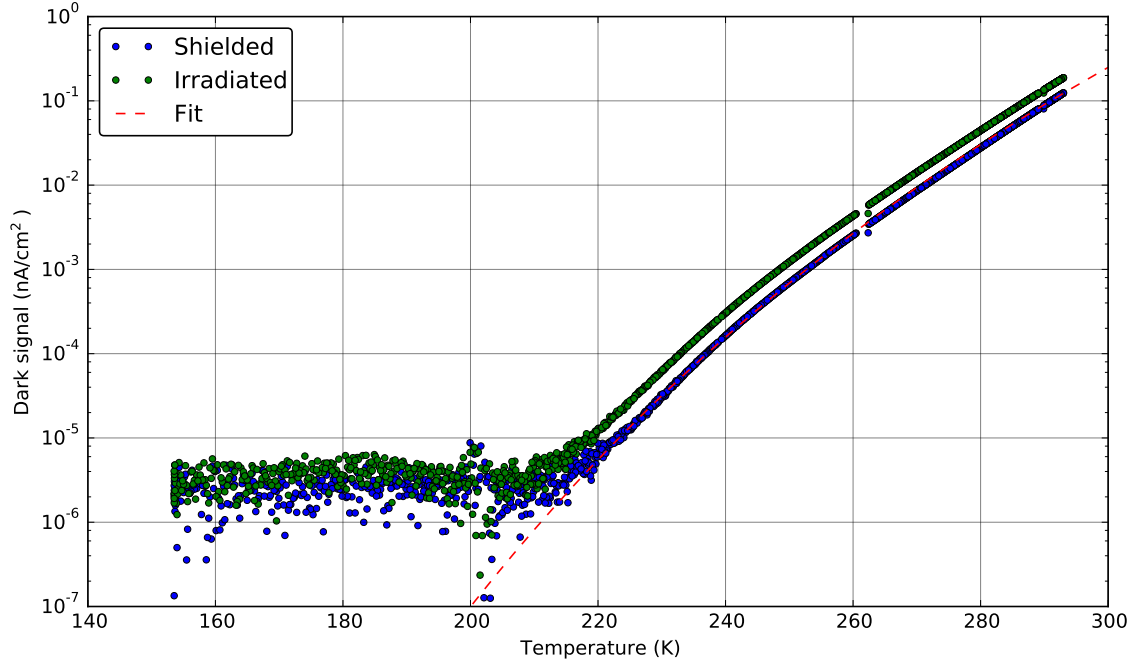


Figure 4.28: Dark current in the CCD201 EMCCD over a range of temperatures. The shielded region (blue) exhibits approximately half of the dark current of the irradiated region (green). The 10 MeV equivalent proton fluence used in the irradiation was $1 \times 10^9 \text{ cm}^{-2}$.

Using Equation 4.14 to give a , n and E_T , the curves in Figure 4.28 were extrapolated to 298 K. The result is an expected increase in CCD201 dark current at 298 K, after irradiation, of approximately 0.1 nA cm^{-2} . Again, the dark current has approximately doubled from its pre-irradiation value, however the equivalent fluence responsible for this increase is 100 times smaller.

The sensitivity of the TDI-CMOS sensor to dark-current increase after proton irradiation (scaled for pixel size) is only slightly worse than that of the CCD201. The greater sensitivity of the TDI-CMOS sensor could be explained by the fact that its surface dark current will increase with irradiation. Any displacement damage at the Si-SiO₂ interface in the CCD201 would cause a negligible increase in dark current due to pinning. However, the majority of

dark current increase from displacement damage is due to bulk damage [91] which would affect both devices. Table 4.4 summarises the dark current measurements on both sensors.

	TDI-CMOS	CCD201
10 MeV eq. proton fluence delivered	$1 \times 10^{11} \text{ cm}^{-2}$	$1 \times 10^9 \text{ cm}^{-2}$
Pre-irradiation dark-current (at 298 K)	20 nA cm^{-2}	0.1 nA cm^{-2}
Absolute dark-current increase (at 298 K)	$18\text{-}32 \text{ nA cm}^{-2}$	0.1 nA cm^{-2}
Dark-current increase per 10 MeV proton	$1.8\text{-}3.2 \times 10^{-10} \text{ nA}$	$1 \times 10^{-10} \text{ nA}$
Dark-signal increase per 10 MeV proton	$1.1\text{-}2.0 \text{ e}^- \text{ s}^{-1}$	$0.62 \text{ e}^- \text{ s}^{-1}$

Table 4.4: Summary of pre- and post-irradiation dark current measurement results for the TDI-CMOS and CCD201 sensors. The pre-irradiation dark current in the TDI-CMOS sensor is 200 times greater. The increase with proton irradiation (per unit fluence) is only 1.8-3.2 times greater.

4.5.3 CTI

As mentioned, the CTI increase after the first irradiation was difficult to measure, especially given the uncertainty added to the measurement by the non-flat overscan. Figure 4.29 shows CTI vs. signal size for design block 1 at all 5 fluences. The pre-irradiation data (zero fluence) is from chip 3. Post-irradiation measurements used an increased number of frame averages (from 50 to 300 frames) in order to reduce the effect of read noise in determining the CTI and this is apparent from the smoother curves at higher fluences.

Figure 4.30 shows a comparison of CTI data for each design block after irradiation to the maximum fluence. Block 3 shows higher CTI at all signal levels. Block 3 is the only design block to use implant type C, the AB gate and interpoly split are the same as block 4. Further investigation is required, but it seems that implant type C might reduce the radiation hardness of the devices, probably due to a larger charge cloud volume.

To quantify the CTI increase per unit fluence the CTI at a signal size of 80 ke^- in each block on chip 3 is compared in Figure 4.31. The results for chip 2 showed a similar trend, although the pre-irradiation CTI varied between chip 2 and chip 3. The increase per unit fluence was approximately linear in each case, and gradients similar. The increase in CTI at

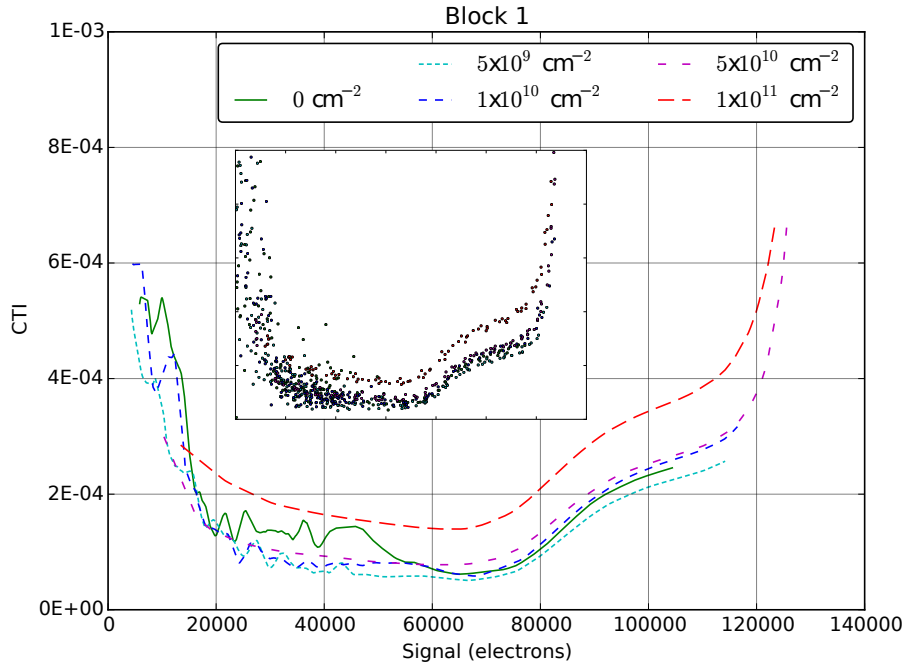


Figure 4.29: CTI data for block 1 at all fluences. After the first irradiation the CTI increase was difficult to measure, so a further irradiation was carried out to higher fluences. The inset shows the data points. Since integration time, not signal level, was controlled the signal values for each column are slightly different due to the variation of dark currents. The curves are the averages of interpolated data points for each column.

the maximum fluence (except block 2) was between 0.5×10^{-4} and 2×10^{-4} . In block 2 the increase was negligible, and further investigation is required to explain this result. Block 2 is the only block that uses implant type B, otherwise it is the same as block 1. Error bars are at one standard deviation above and below the mean. Measurements from each of the central 6 columns in each block are included. In conclusion, block 0 and block 1, with low starting CTI and similar increases after irradiation, seem to be the best blocks (Buried AB gate, implant type A and 0.2 and 0.25 μm interpoly gap respectively). Block 2 has the lowest CTI at low signals, both before and after irradiation, but suffers from a lower FWC.

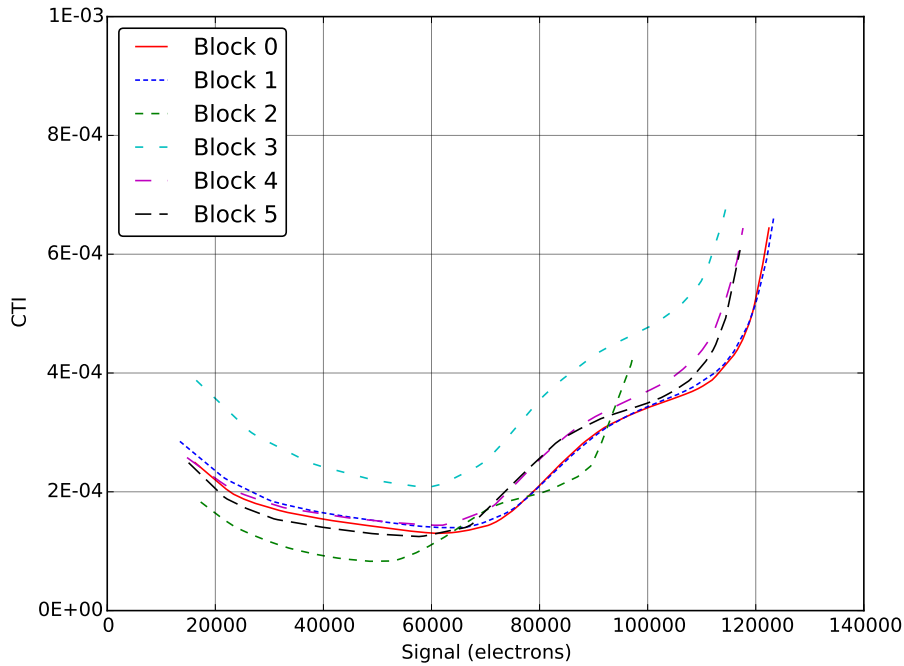


Figure 4.30: Comparison of CTI in each design block after irradiation to the maximum fluence ($1 \times 10^{11} \text{ cm}^{-2}$ 10 MeV equivalent). Block 2 has relatively good CTI but maintains lower FWC. Block 3 has higher CTI at all signal levels than the other 5 design blocks.

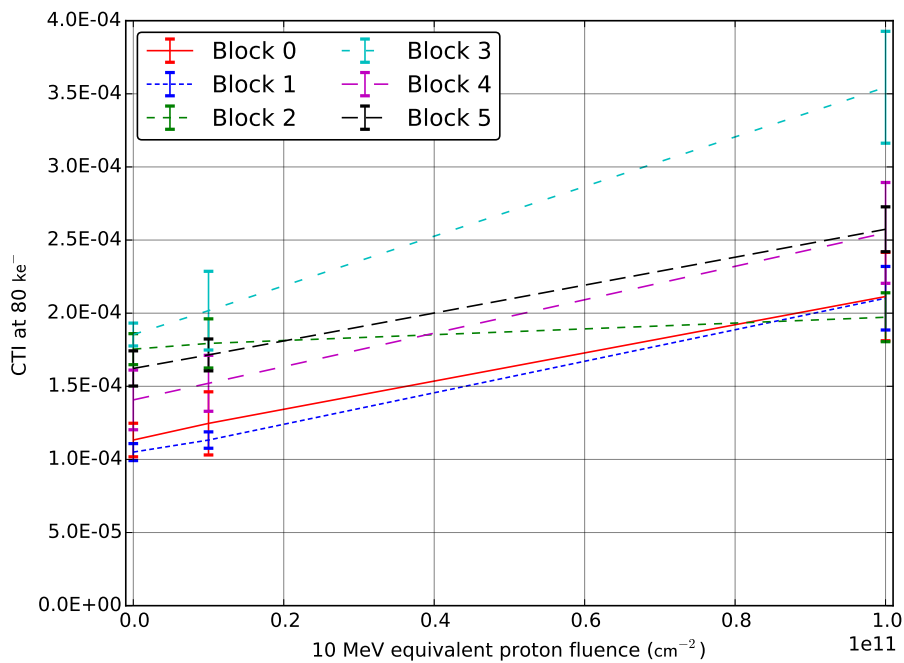


Figure 4.31: CTI vs. fluence for each of the 6 design blocks on chip 3.

4.6 Radiation hardness comparison with CCD sensors

The pre-irradiation CTI of the TDI-CMOS sensor could be caused by either potential pockets or by electron traps resulting from stable defects in the silicon crystal. However, it can be assumed that any increase in CTI due to proton irradiation is a result of an increase in the bulk trap density in the channel. The trap density is assumed to increase linearly with the fluence of proton irradiation and, as can be seen from Figure 4.31, the increase in CTI is also approximately linear with fluence.

EPER measurement results for calculating CTI in the CCD201 device were provided, both pre-irradiation and at 10 MeV proton equivalent fluence of $1 \times 10^9 \text{ cm}^{-2}$. The CTI results for both the TDI-CMOS device and the CCD201 are summarised in Table 4.5. Also included are the physical dimensions of the pixels, estimates for the charge cloud volumes at the signal levels used for the CTI measurement, measurement temperature and line rate.

	TDI-CMOS	CCD201
Pixel	$13 \mu\text{m} \times 13 \mu\text{m}$ 4 phase	$13 \mu\text{m} \times 24 \mu\text{m}$ 3 phase
Transfer rate $1/t_L$	12.5 kHz (line rate)	700 kHz (serial clock)
Temperature	293 K	298 K
EPER signal level	80 ke^-	40 ke^-
Charge cloud volume	$10 \mu\text{m}^3$	$15 \mu\text{m}^3$
Pre-irradiation CTI	2×10^{-4}	1×10^{-6}
10 MeV eq. proton fluence used	$1 \times 10^{11} \text{ cm}^{-2}$	$1 \times 10^9 \text{ cm}^{-2}$
Post-irradiation CTI	$3\text{-}4 \times 10^{-4}$	$1\text{-}2 \times 10^{-4}$
Damage equivalence	$1\text{-}2 \times 10^{-15} \text{ cm}^{-2}$	$1\text{-}2 \times 10^{-13} \text{ cm}^{-2}$

Table 4.5: Comparison of TDI-CMOS and CCD201 serial register proton irradiation studies. The damage equivalence is defined as $\Delta\text{CTI}/f$ where f is the 10 MeV equivalent proton fluence.

4.6.1 Factors affecting CTI radiation hardness

The CTI for a CCD style device can be approximated by [92]

$$\varepsilon \approx \frac{N_t}{N_s} F(t_D, T, N_s) \quad (4.15)$$

where

$$N_s = \frac{Q}{abd} \quad (4.16)$$

is the signal charge density. Here Q is the original signal size, N_t is the trap density and $F(t_D, T, N_s)$ is a function of the phase dwell time t_D , temperature T , and N_s . The approximation assumes that the change in signal level due to the loss of deferred charge is small and therefore has a negligible effect on trap capture time constant τ_c . a , b and d are the channel width, pixel pitch, and size of the charge in depth respectively.

The charge remaining in the signal packet after M transfers will be

$$Q_M = Q_0(1 - \varepsilon)^M \approx Q_0(1 - M\varepsilon) \quad (4.17)$$

for $CTI \ll 1$ and an original signal of Q_0 . The resulting charge loss will be

$$Q_e \approx M\varepsilon Q_0 \approx N_t abd F(t_D, T, N_s) M \quad (4.18)$$

Equation 4.18 shows that the charge loss due to the transfer of a signal is proportional to the distance over which the charge is transferred Mb . It also shows that the charge loss per transfer is proportional to the charge cloud volume abd and the trap density. Only one trap species is taken into account here. More accurately Q_e will be the sum of multiple terms i.e.

$$Q_e \approx Mabd \sum_{i=0}^I N_{ti} F_i(t_D, T, N_s) \quad (4.19)$$

where N_{ti} is the trap density for the i_{th} trap species and $F_i(t_D, T, N_s)$ is the deferred charge contribution per trap for the i_{th} trap species of I different species.

The magnitude of CTI increase per unit proton fluence in a particular sensor and signal size is then due to the following factors.

- The concentration of each defect species, which can be considered proportional to the proton fluence and may be affected by the impurities in the silicon (for example E-centre formation requires the presence of phosphorous impurities).
- The volume of the signal charge cloud.
- The influence that each trap species has on CTI, which is described by $F(t_D, T, N_s)$.

4.7 EPER model

A model was constructed to calculate the effect of defect centres on CTI, as predicted by SRH theory (see Section 3.6.2). The basis of the model is the solution of differential equations governing the ratio of filled traps after the transfer of charge packets under clock phases in a CCD like device. This method is based on the model developed by Konstantin Stefanov [92] where the CTI was calculated in a CCD for signal generated by X-rays (1620 e^-). However, in the model here, CTI is instead measured by EPER.

The model is configured to run for one trap species at a time and is configured for either the E-centre or the $(V-V)^-$ divacancy. The electron emission time constant τ_e (a function of temperature) is first calculated from Equations 3.12, 3.13 and 3.14.

The core of the model is the calculation of the ratio of filled traps r_f under a phase after a transfer, which is based on the solution of differential equations [92]. For each transfer, the ratio of filled traps after transfer is calculated by solving these equations based on the ratio of filled traps before transfer and the size of the charge packet being transferred into the phase.

The ratio of filled traps after a transfer is then a function of the size of the charge packet transferred under the phase (denoted N), and of the ratio of filled traps before the transfer r_f (which depends on all previous transfers and the initial occupancy). This function is denoted $f(n_s, r_f)$. During the m^{th} transfer, the charge packet from the $p - 1^{th}$ phase, which arrived there after the $m - 1^{th}$ transfer, is transferred onto the p^{th} phase:

$$r_{f[p,m]} = f(n_{s[p-1,m-1]}, r_{f[p,m-1]}) \quad (4.20)$$

where $r_{f[p,m]}$ is then the ratio of filled traps in the p^{th} phase after the m^{th} transfer etc.. The number of electrons released from traps under this phase is

$$n_{rel[p,m]} = (r_{f[p,m-1]} - r_{f[p,m]}) \frac{N_t}{V} \quad (4.21)$$

where N_t is the trap density under the phase and $V = abd$ is the charge packet volume. The released electrons join the charge packet giving

$$n_{s[p,m]} = n_{rel[p,m]} + n_{s[p-1,m-1]} \quad (4.22)$$

The initial value for r_f in each phase is calculated by performing 100 transfers, starting with $r_f = 1$ and with n_s equal to the edge pixel signal level. Each transfer onto phase 0 uses a signal equal to the dark current as $n_{s[-1,m-1]}$.

The electron capture time constant τ_c is calculated from Equation 3.11. The phase timing is as shown in Figure 4.11.

The first result of the model is shown in Figure 4.32, which shows the relationship between the number of pixels in the device and the deferred charge per pixel, as predicted by the model. This result suggests that the approximation that the amount of deferred charge measured in the charge trail is proportional to the number of pixels is reasonable.

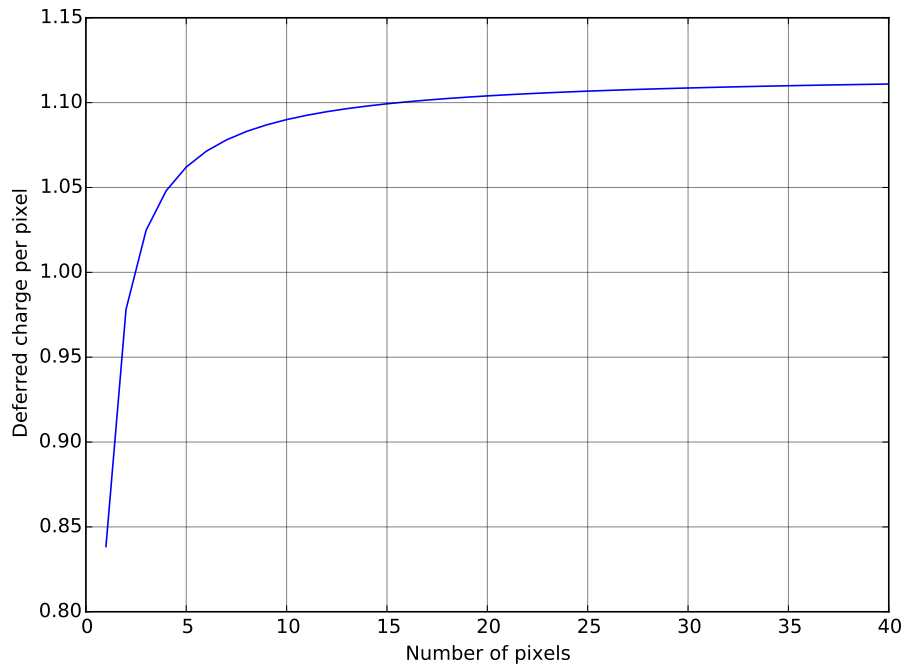


Figure 4.32: CTI per pixel is usually calculated by assuming that the amount of deferred charge in the EPER charge trail is proportional the number of pixels. This assumption is valid for $\tau_c \approx 0$. Simulating the TDI-CMOS transfer for array sizes of 1 to 40 pixels at $T=298$ K we see that the amount of deferred charge per pixel increases by approximately 32% over the deferred charge in a single pixel array. The increase in deferred charge per pixel as the array size grows beyond 40 pixels becomes negligible. This result highlights how each evaluation of CTI is specific to the exact method used to measure it.

4.7.1 TDI-CMOS/CCD comparison

Figure 4.33 shows the predicted charge trail magnitude as a function of temperature for each device. The contributions from the divacancy and the E-centre are plotted separately. This simulation is based on a uniform distribution of traps, with a single trap under each phase, and the conditions stated in Table 4.5.

As expected, the peak deferred charge level occurs at a different temperature in each device, primarily due to the different line-rates. However, the nearly factor 3 difference in peak deferred charge was not expected.

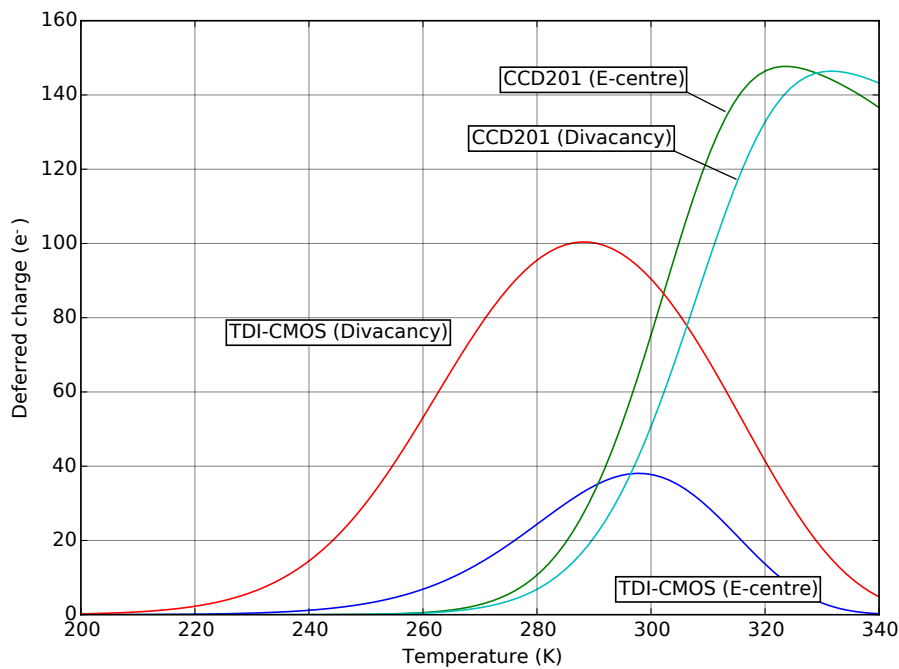


Figure 4.33: Deferred charge as a function of temperature. Simulated results for EPER measurement after transfer through 160 phases. Simulation parameters are shown in Table 4.6.

The least-well defined parameter for the model is the charge cloud volume. In order to rule out a large error, the deferred charge magnitude as a function of charge cloud volume is plotted for both devices, and both defect species at $T=298$ K in Figure 4.34.

The dark signal in the overscan provides a "fat zero" [93] which fills traps in the absence

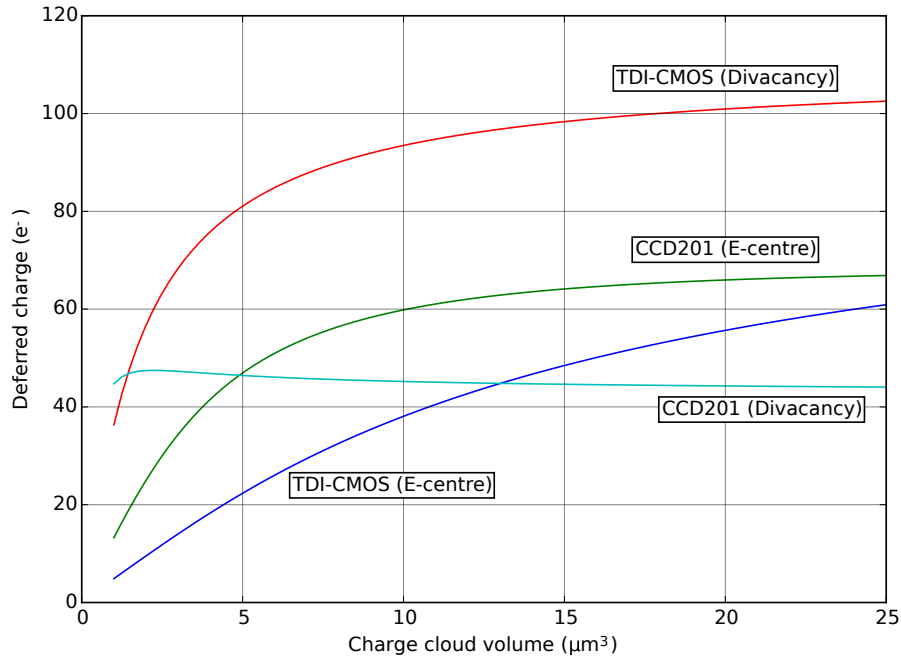


Figure 4.34: Deferred charge vs. charge cloud volume at $T=298$ K. The estimated charge cloud volumes are $10 \mu\text{m}^3$ and $15 \mu\text{m}^3$ for the TDI-CMOS and CCD201 devices respectively.

of signal. The dark signal in each device is significantly different. For the TDI-CMOS device it is approximately $16.9 e^-$, whereas in the CCD201 it is only $0.00329 e^-$. This is due to the combination of lower dark current and a much faster transfer rate in the CCD201 serial register compared to the TDI-CMOS pixels.

To calculate the effect of the different dark signals accumulated in each device, the deferred charge amount was simulated for both devices for a range of dark signal values between 1×10^{-3} and $1 \times 10^2 e^-$. Results are shown in Figure 4.35. Although dark signal does have an effect on the deferred charge amount, the change in the divacancy is not enough to explain difference in peak deferred charge between the TDI-CMOS divacancy and CCD201 divacancy simulations. The conclusion is therefore that the effect of the electron capture time constants τ_c relative to the line rate is mostly responsible for the different peaks in deferred charge amount.

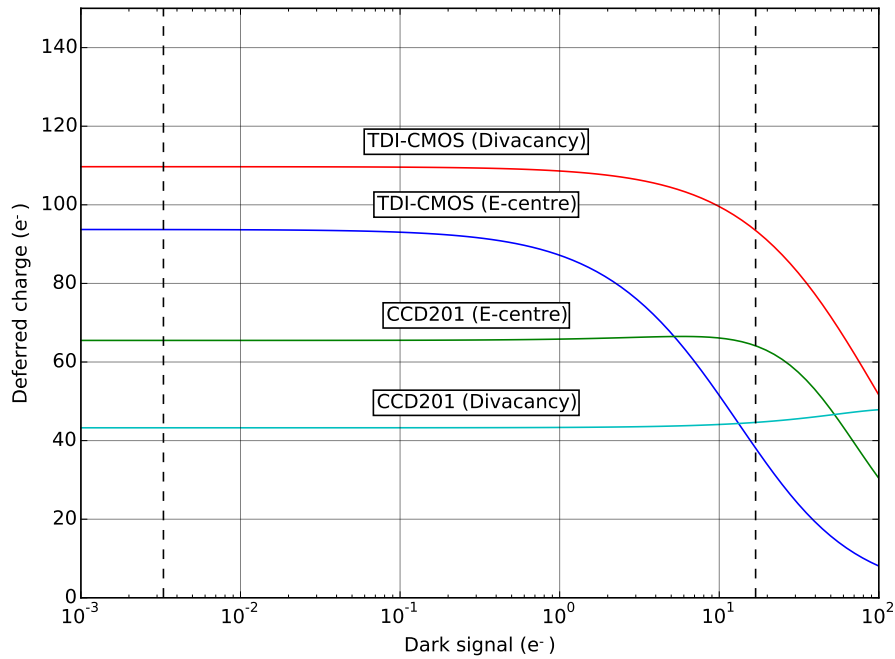


Figure 4.35: There is a significant difference in dark signal and therefore in the size of the "fat zero" present during the EPER measurement of the CCD201 and TDI-CMOS devices. In order to rule out this difference as the cause of the different peak deferred charge amounts due to the divacancy observed in the simulation, deferred charge is shown here as a function of dark signal at 298 K. The CCD201 dark signal is 0.00329 e^- and the TDI-CMOS dark signal is 16.9 e^- (shown by the dashed lines). Although the dark signal does affect the amount of deferred charge, it does not fully explain the difference in peak amounts between the two devices.

Increase in CTI per unit proton fluence is approximately 100 times higher in the CCD. With the similar pixel sizes, this has to be mostly due to different operation, the effect of which we have generalised into the function $F(t_D, T, N_s)$. The difference in performance is partly explained by a simulation of EPER. At the experimental temperatures, the simulation output finds the amount of deferred charge in the TDI-CMOS device at 89 e^- due to the divacancy and 37 e^- due to the E-centre. In the CCD201 it is 50 e^- due to the divacancy and 75 e^- due to the E-centre.

The TDI-CMOS chip was operated slow and warm, meaning that the dominant trap species in producing CTI was the E-centre, and this operation mode is representative of

	TDI-CMOS	CCD201
Pixel	$13\ \mu\text{m} \times 13\ \mu\text{m}$ 4 phase	$13\ \mu\text{m} \times 24\ \mu\text{m}$ 3 phase
Transfer rate $1/t_L$	12.5 kHz (line rate)	700 kHz (serial clock)
Temperature	293 K	298 K
EPER signal level	$80\ \text{ke}^-$	$40\ \text{ke}^-$
Charge cloud volume	$10\ \mu\text{m}^3$	$15\ \mu\text{m}^3$
Dark signal	$16.9\ \text{e}^-$	$0.00329\ \text{e}^-$

Table 4.6: Parameters used for the simulation of EPER in the TDI-CMOS and CCD201 devices.

potential applications. In practical applications, CCDs are usually operated at much colder temperatures in order to suppress dark current. Large format CCDs also need to have relatively fast line rates (hundreds of kHz in the serial register in order to achieve hundreds of Hz for parallel transfer). The line rate at which the TDI-CMOS was tested, which is similar to the rate which would be used in the application, sits between these two rates.

The relatively low CTI increase per unit proton fluence seen in the TDI-CMOS devices also suggests one of two things. If it is assumed that the reason for the low CTI increase with proton irradiation is that the device is operating at a speed and temperature where CTI due to the E-centre is only moderate, then the number of defects (E-centres) which would need to have been present after device fabrication in order to cause the initial CTI is very high (approximately the same defect concentration as was introduced by a 10^{11} protons/cm² 10 MeV equivalent fluence). The way to test whether the initial CTI was due to defects or potential pockets would be to measure CTI in an unirradiated device over a range of line rates or temperatures and look for peaks in CTI which occur due to favourable trapping conditions at certain temperatures.

4.8 Conclusions

The TDI-CMOS image sensor used in this chapter is a promising prototype sensor for Earth observation applications. The sensor uses a charge-transfer architecture to increase the SNR

over the digital summation approach which would be used in a traditional CMOS active pixel sensor. The high levels of integration in modern CMOS processes allow an amplifier per column and potentially an ADC per column. This allows relatively fast readout in arbitrarily wide arrays. The performance of the sensor, in terms of dark current and CTI, is not as strong as traditional CCDs. The significance of the dark current and CTI of the TDI-CMOS sensor is diminished in Earth observation applications. A relatively small number of transfers is required and the integration time is limited by the image motion speed.

The pre-irradiation dark current is high compared to a CCD. The process is optimised for 0.18 μm CMOS APS designs. It may be possible to optimise the process in order to lower the dark current in charge-transfer style devices. The excess dark current is likely produced at a Si-SiO₂ interface. CMOS does not have the gettering [33] that CCDs have.

The increase in dark current and CTI after proton irradiation was compared with a typical CCD with similar pixel dimensions. The data used was collected in a CCD running with different timing and at a different temperature. It is therefore difficult to make a direct comparison regarding the radiation harness of each device. The dark current increase per unit fluence was very similar for each technology.

The CTI increase per proton was approximately 100 times lower in the TDI-CMOS device. Transfer rate, dark current, temperature and charge packet size within the pixel all determine the amount of CTI generated by a certain concentration of defects. Since the transfer rates and dark current were very different for the two devices this is not a fair comparison by any means.

Simulations showed that, at 298K, in both devices the contribution to CTI of the divacancy and E-centres was significant. The simulation took into account both the measured dark current and an estimated charge cloud volume. The sensitivity of the simulation output to charge cloud volume and dark current would not fully explain the large difference in CTI increase per proton. A possible explanation could be the different relative concentrations of

divacancy and E-centre produced by the proton irradiations. Hall et al. estimate an E-centre to divacancy concentration ratio of 5:1 [62]. Such a ratio would increase the CCD201 CTI by a greater factor than the TDI-CMOS CTI. More data would be needed to determine the relative concentrations of divacancies and E-centres produced by proton irradiation in these particular devices.

While a direct comparison is difficult, we conclude that the TDI-CMOS device is sufficiently radiation hard to be competitive against CCDs. In fact, the TDI-CMOS has the added advantage of being able to operate at a single line rate (due to the column-parallel readout). CCDs, by comparison, generally use different clock rates for the serial and parallel transfers (the ratio between clocks is typically equal to the number of rows in the array). The single line rate in the TDI-CMOS sensor means that, even if the line rate is fixed by the application, the temperature can be selected to minimise the effect of any one defect species on CTI.

The initial CTI and dark current are not yet competitive with CCDs for large format general purpose imaging, but are sufficient in the application of high dynamic range Earth observation from space, for which the sensor was developed.

4.9 Further work

So far, the TDI-CMOS sensor has only been tested at a temperature of 298 K and with a line rate of 12.5 kHz. Changing either or both of these operating points would allow investigation into the relative influence of different defect species on CTI. Such an investigation would also be necessary before the use of the sensor in space, since the operating temperature, if kept constant, is unlikely to be so high.

Radiation damage from protons was investigated which gives a good indication of the kinds of performance change likely to result from displacement damage effects in natural radiation environment, i.e. in space. A further irradiation using, for example, gamma rays

should be carried out to see the effects of ionisation damage, which are likely to be an increase in dark current, flatband voltage shift resulting in a reduction in dynamic range, and a threshold voltage shift in the output circuitry. It can be expected that the results of ionisation damage will be significantly more favourable than the equivalent results in CCDs, since the gate oxide layer in the CMOS process is so much thinner.

The unexplained charge trail behaviour of the device made CTI measurement difficult but not impossible. However, this behaviour is still not explained and it may have consequences for the electro-optical performance of the sensor. Even if the sensor is well characterised in terms of QE, CVF and linearity, care should be taken to ensure there is no unexpected behaviour when handling a large change in signal over a short time period (i.e. imaging a bright feature immediately followed by a dark feature).

A comparison of the TDI-CMOS sensor and a CCD at the same frequency, temperature and dark signal (using light top-up in the CCD) would be very valuable.

Finally, more work is required to understand the effects of the design choices in each of the six design blocks studied. So far, we have demonstrated some tradeoffs between CTI performance and FWC. There is also a significant amount of work which could be undertaken to optimise performance by adjusting the clock timing (speed and overlaps) and bias voltages. This work is best undertaken with the device designers who have access to detailed design information.

Chapter 5

Experimental study of single event effects in CMOS active pixel sensors

This chapter describes an experimental investigation into the effect of heavy ion irradiation of CMOS image sensors. The experiment was carried out to measure the rate of SEEs in four different image sensor device variants. The primary aim was to study rate of SELs in the devices as a function of the amount of free charge deposited by the heavy ions. In addition to SELs, SEUs and SEFIs were recorded. The results are compared against the expectations in relative SEE performance given the device variants. The predictions of performance are based on the implementation of process modifications, such as deep doping wells. The aim of these process modifications used in the device variants is to reduce the occurrence of SEL when using such devices in the space radiation environment.

5.1 Experimental details

5.1.1 Heavy Ion Facility at Université Catholique de Louvain

m/q	Ion	Energy on DUT (MeV)	Range in Si (μm)	LET in Si ($\text{MeV cm}^2\text{mg}^{-1}$)	Effective LET ($\text{MeV cm}^2\text{mg}^{-1}$)		
					30°	45°	60°
3.25	$^{13}\text{C}^{4+}$	131	269.3	1.3	1.5	1.8	2.6
3.5	$^{14}\text{N}^{4+}$	122	170.8	1.9	2.2	2.7	3.8
3.14	$^{22}\text{Ne}^{7+}$	238	202	3.3	3.8	4.7	6.6
3.33	$^{40}\text{Ar}^{12+}$	379	120.5	10.0	11.5	14.1	20.0
3.218	$^{58}\text{Ni}^{18+}$	582	100.5	20.4	23.6	28.8	40.8
3.35	$^{84}\text{Kr}^{25+}$	769	94.2	32.4	37.4	45.8	64.8
3.54	$^{124}\text{Xe}^{35+}$	995	73.1	62.5	72.2	88.4	125.0

Table 5.1: Heavy ion species available in the high range (high energy) cocktail at the HIF ($m/q \simeq 3.33$). This information is provided by the HIF [94] except the effective LETs at beam inclinations of 30°, 45° and 60° which are calculated from equation 3.15.

The heavy ion irradiation in this work was carried out at the Cyclone cyclotron at the Heavy Ion Facility (HIF) of the Université Catholique de Louvain. Table 5.1 shows the ion species, energies, LET and range of the heavy ions available in the high range cocktail at the HIF. From this point on any LET value other than the seven "pure" LETs at normal incidence will refer to an effective LET.

The high range cocktail uses a mass to charge ratio of $m/q \simeq 3.33$. A different cocktail is available using $m/q \simeq 5$ which allows a slightly higher maximum pure LET of 69.2 $\text{MeV cm}^2\text{mg}^{-1}$. However, the higher range cocktail allows high effective LETs and the greater range means high tilt angles can be used if necessary.

Figure 5.1 shows the LET as a function of distance into a silicon target for the four ion species used in this work. This has been calculated using SRIM (Stopping and Range of Ions in Matter) software.

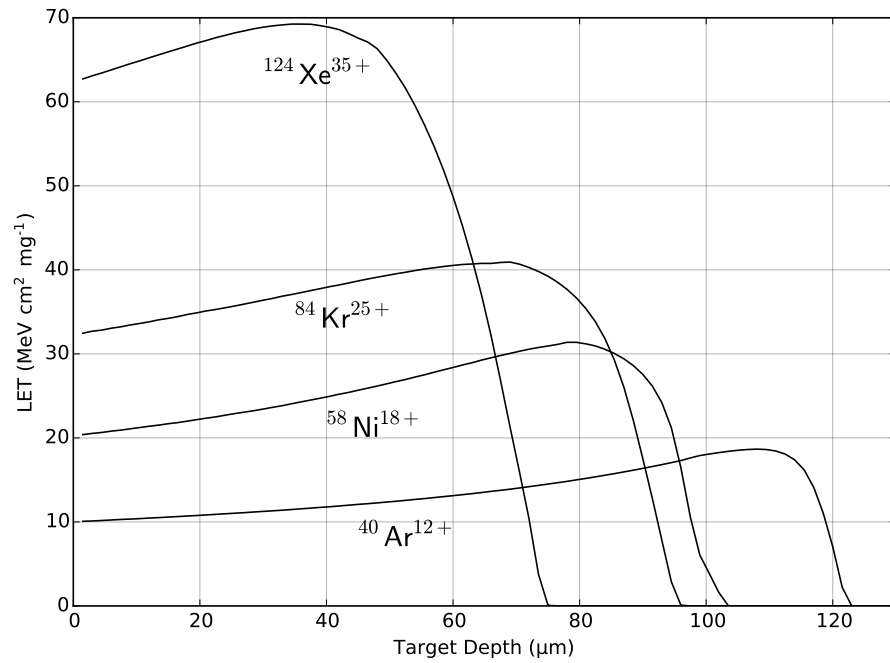


Figure 5.1: LET as a function of target depth for the four heavy ion species and energies used. Data calculated using SRIM.

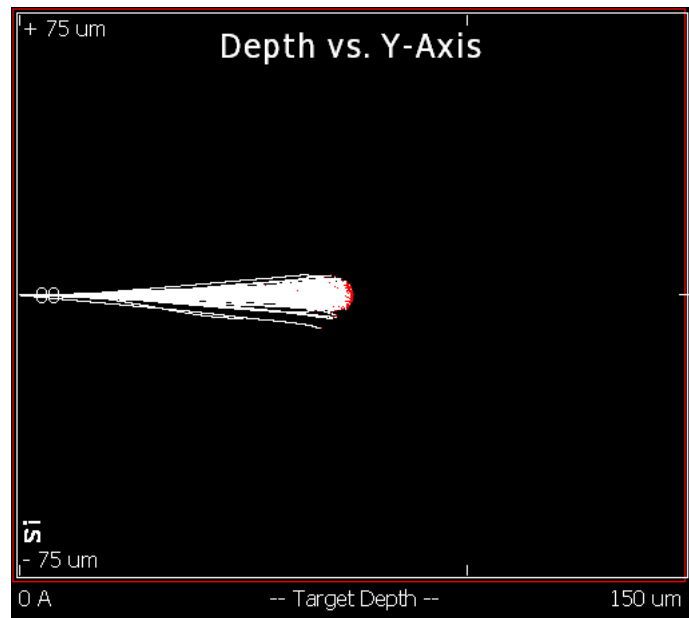


Figure 5.2: Ion paths calculated by TRIM simulation of 12,000 995 MeV xenon ions in a Silicon target.

Details on the SRIM software can be found in [95]. The LET and target depth quoted in Table 5.1 are the LET as the ion hits the target and the maximum penetration depth, beyond the Bragg peak.

The SRIM package contains the TRIM (Transport of ions in matter) Monte Carlo simulator. Each ion species (argon, nickel, krypton, xenon) was simulated at the energy in Table 5.1. A simple silicon target was chosen for simplicity. Very similar results were obtained for thin ($10\text{ }\mu\text{m}$) surface layers of aluminium and silicon dioxide. Each simulation was run for an excess of 10,000 ion strikes using the "Ion Distribution and Quick Calculation of Damage" calculator which gives accurate results for target ionisation. Figure 5.2 shows the paths of xenon ions into the target. Deviation from the ion incidence direction is minimal, especially near the surface.

5.1.2 Potential structure of triple well devices

The simulated potential structure along a one-dimensional path from substrate to well for deep n well and deep p well devices is shown in Figure 5.3.

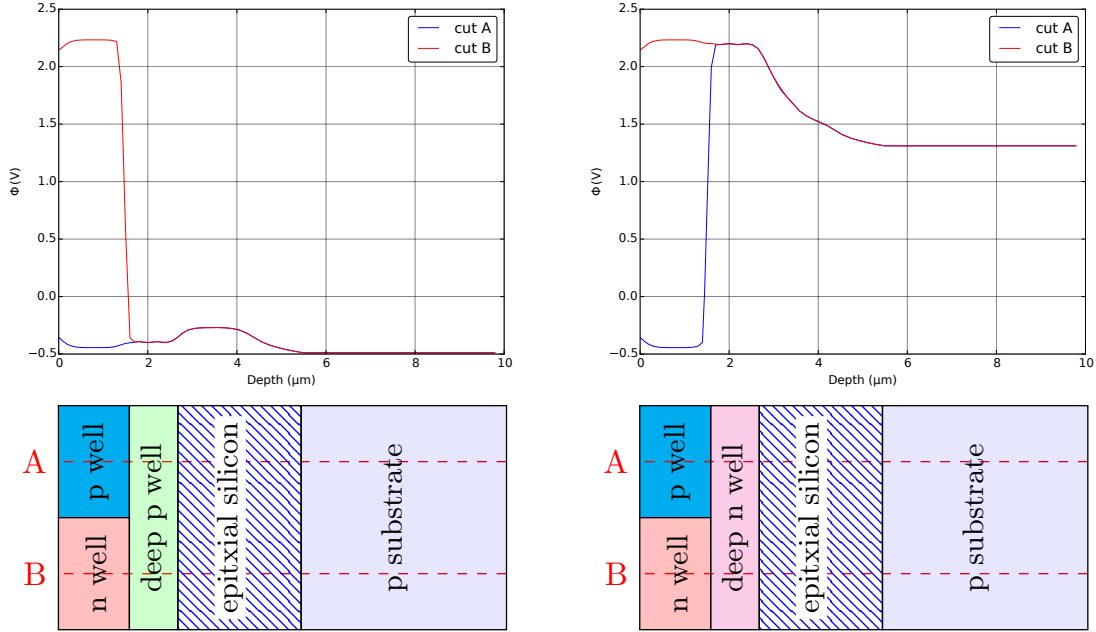


Figure 5.3: Simulated potential along two cut-lines A and B in a deep p well device (left) a deep n well device (right). In the deep p well device, electrons must overcome a potential barrier in the epitaxial layer in order to reach the p well or n well sensitive areas. Holes must overcome a barrier to leave the epitaxial layer. The deep p well therefore rejects electrons from the substrate and traps holes. In the deep n well device, electrons are repelled from the epitaxial layer and the deep n well. However, holes experience no barrier in drifting from the substrate all the way to the n well sensitive area.

A heavy ion with a LET of $10 \text{ MeV cm}^2 \text{ mg}^{-1}$ in silicon will create a charge trail with a density of approximately $1.02 \text{ pC } \mu\text{m}^{-1}$. If the charge trail is modelled as a cylinder of diameter $0.5 \mu\text{m}$ then initial e-h pair concentration will be approximately $3.11 \times 10^{18} \text{ cm}^{-3}$. This is three to five orders of magnitude higher than typical doping concentrations and therefore much larger than the possible charge density in an equilibrium depletion region. At least initially the local potential structure will collapse. The equilibrium potential structure must therefore be used with caution when anticipating the movement of such a dense charge

cloud.

More simulations of triple well devices and their latchup susceptibility are given in Chapter 6.

5.1.3 e2v Sapphire and Ruby sensors

The e2v Sapphire 1.3M and Ruby 1.3M sensors are 1.3 megapixel front illuminated CMOS image sensors with $5.6\ \mu\text{m}$ square pixels [96] [97]. Variants in 3T (rolling shutter) or 4T (global shutter) are available. The Ruby shares the same digital circuitry as the Sapphire. However, the Ruby has enhanced near infra-red QE.

5.1.4 Test devices

Four device variants were provided by e2v. The first of these is a standard Sapphire device, the second a special Sapphire device with a Deep N Well (DNW). The third and fourth devices were Ruby sensors with Deep P Wells (DPW): one on standard $5.5\ \mu\text{m}$ and one with $18\ \mu\text{m}$ thick epitaxial silicon. Since the image area only has n channel transistors it is not subject to latchup. SEUs, however, are possible in the image array and would appear as spurious signals. The design of the image array is the only difference at the layout state between the Sapphire and Ruby devices. Therefore, only the process modifications (summarised in Table 5.2) affect the SEE sensitivity of the different sensors.

The structures of the four test device variants are shown in Figure 5.4. The initial hypothesis was that the $5.5\ \mu\text{m}$ triple well devices should exhibit higher LET thresholds than the dual well standard Sapphire. The presence of the thicker $18\ \mu\text{m}$ epitaxial layer was expected to reduce the effect of the DPW to some extent.

Device	Serial	Epi thickness (μm)	Epi resistivity ($\Omega\text{ cm}$)	Buried layer	Remarks
Sapphire	#545	5.5	30	No	
DNW Sapphire	#538, #539	5.5	30	DNW	DNW added under 1.8V logic
Ruby 5.5 μm	#550	5.5	30	DPW	DPW added under all circuits except pixels
Ruby 18 μm	#546	18	1000	DPW	DPW added under all circuits except pixels

Table 5.2: Details of the device variants used for SEL testing

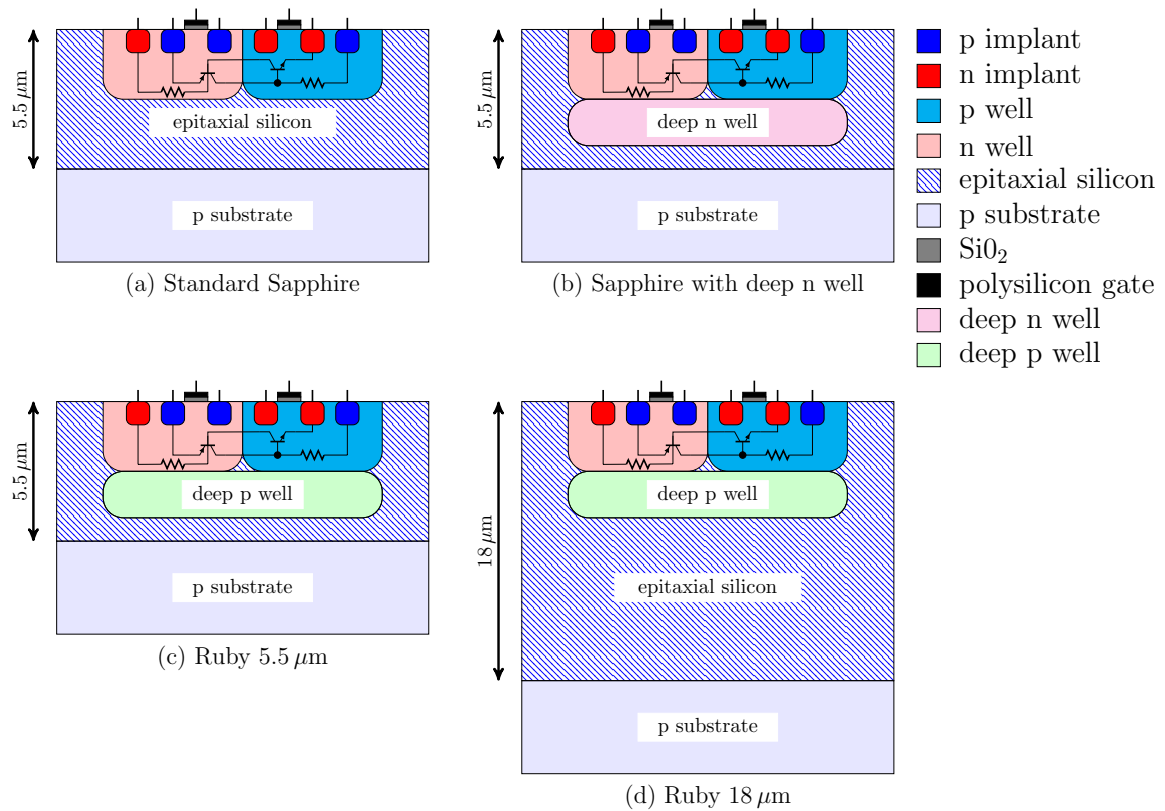


Figure 5.4: Summary of device layers

5.1.5 C3D camera board

The camera system used for running the sensors in this experiment was the Compact CMOS Camera Demonstrator (C3D) camera developed by Richard Harriss and XCAM [98]. The C3D camera was initially designed to run on board the UKube-1 CubeSat mission, launched in July 2014. Aboard UKube-1 the C3D ran three Sapphire devices: two for imaging and one for studying radiation damage in the sensor. The C3D camera was used previously for SEL testing of standard Sapphire sensors at LETs from $10 \text{ MeV.cm}^2/\text{mg}$ to $25 \text{ MeV.cm}^2/\text{mg}$. In flight mode the C3D board interfaces with the spacecraft's I²C bus. Simple I²C commands sent from the spacecraft are executed by the Altera FPGA running on the C3D and the FPGA controls each of the image sensors and returns image data to the spacecraft. By using a USB to I²C converter board and modifying the firmware on the FPGA the C3D becomes a convenient system for running Sapphire or Ruby sensors from a PC. The C3D board mounted in the vacuum chamber at the HIF is shown in Figure 5.5.

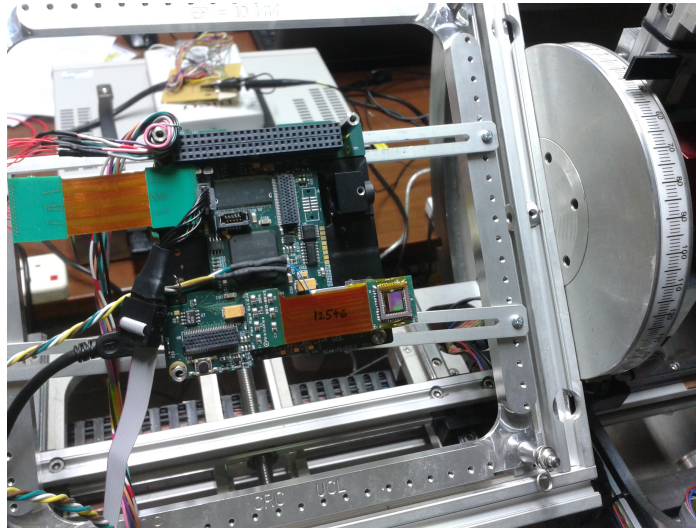


Figure 5.5: The test board with sensor mounted, awaiting shielding, before being placed in the beam. The motor to rotate the board is shown on the right. The angle of rotation is visible to the operator via a camera system to the control room.

5.1.6 Experimental setup

A high level schematic of the entire test system, including those parts of the HIF used, is shown in Figure 5.6. The temperature measurement is described in Section 3.7.8.

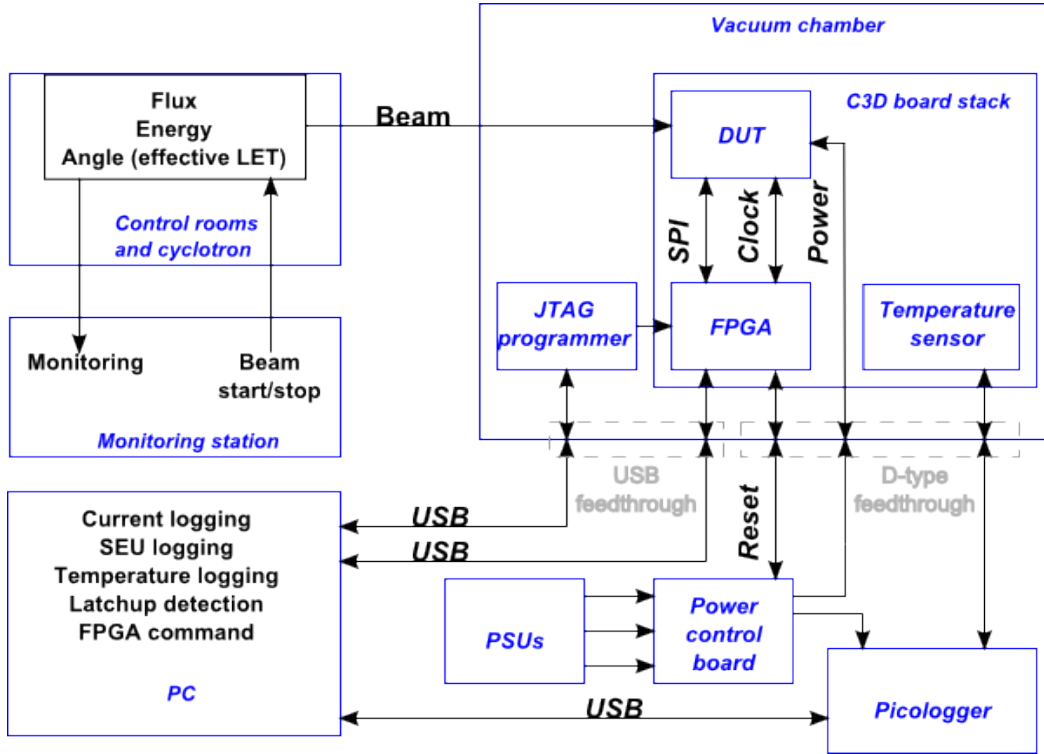
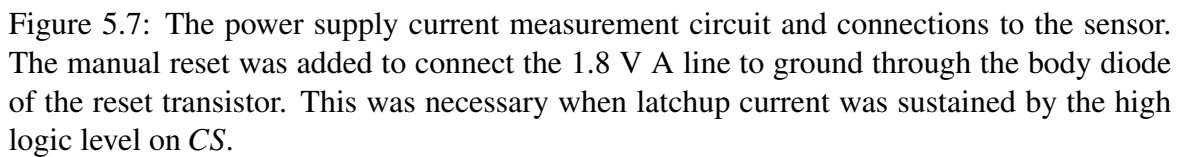


Figure 5.6: Overview of the experimental setup

Once in the beam the sensors performed regular operations requested by the software. The steady state operation of the sensors, including logging of SEUs, is covered in section 3.7.9. To measure the SEL rate of the sensor under heavy ion irradiation the same circuitry was used as in previous work [98]. The current measurement circuit is shown in Figure 5.7. Current draw in each of the three sensor supplies was measured. The three supplies are 1.8 V analogue, 1.8 V digital and 3.3 V analogue. The 1.8 V digital circuits in the sensor are those using CMOS logic are therefore most likely to suffer from SEL.

The current draw was measured from the potential difference on the 1 Ω sense resistor.

Supply current was recorded on a Picologger ADC-20 connected to a PC. Whenever



a current draw of more than 50 mA was detected (due to a latchup) by software on the PC, a reset command was sent to the FPGA on the C3D board. On receipt of the reset command the FPGA I/O operated FET switches to disconnect all three power supplies from the sensor in order to quench the latchup. The FPGA then reset the sensor and configured its internal registers before resuming steady state operations. In the event that a latchup was not properly reset, the protection diode in the disconnect MOSFET provides a current path to short the supply with a manual reset through the switch. SEU information was downloaded from the FPGA every six seconds and the download was completed even in the event of a latchup. The current was sampled every second. Each time a latchup occurred it took up to six seconds before the reset operation was carried out. The delay before reset was

in order to download every SEU log. The SEL rate was measured whilst the sensors were under irradiation and where necessary the ion flux was adjusted to bring the SEL rate within a sensible range (an average of one SEL event every 10 to 20 seconds). This was a good compromise between the uncertainty on rate determination given by the sampling interval of 1 second and the uncertainty given by a low number of events. Once a suitable flux was adopted at each LET the policy was to use a run time of 20 minutes, or up to 100 latchup events, whichever was the soonest. The flux at the HIF can be adjusted from $<10 \text{ ions cm}^{-2} \text{ s}^{-1}$ to $10^4 \text{ ions cm}^{-2} \text{ s}^{-1}$ [94].

The power control board electronics was prepared by the author, as was the PC logging and latchup detection code. The FPGA code was also modified from the previous work, including the addition of phase locked loop options (see Section 5.2.1). The temperature measurement hardware and the beamline mounting jig and feedthroughs were also prepared by the author.

The irradiations were carried out by the author and Konstantin Stefanov during two 12 hour sessions separated by a 12 hour break. The irradiations were assisted by the HIF staff who set the ion species and flux as instructed. Beam alignment with the DUT was confirmed by the HIF's laser sight and a camera inside the vacuum chamber, provided by the HIF.

Figure 5.8 shows an example current log taken. The 50 mA detection threshold is marked with a dashed line. Most latchups are on the 1.8 V digital supply and are reset as expected. The repeated latchups are dealt with in section 5.1.6. The log in Figure 5.8 is atypical because of two features. A latchup event with a current draw of less than 50 mA is seen at around 800 s - the only time this occurred in the experiment - and is only reset after a higher current latchup event. Secondly there are multiple instances of 3.3 V latchup which is discussed in section 5.2.4. To calculate the latchup cross-sections dead time was removed from the current log time series data. The time during which latchup could occur was measured as the time between resets and latchups.

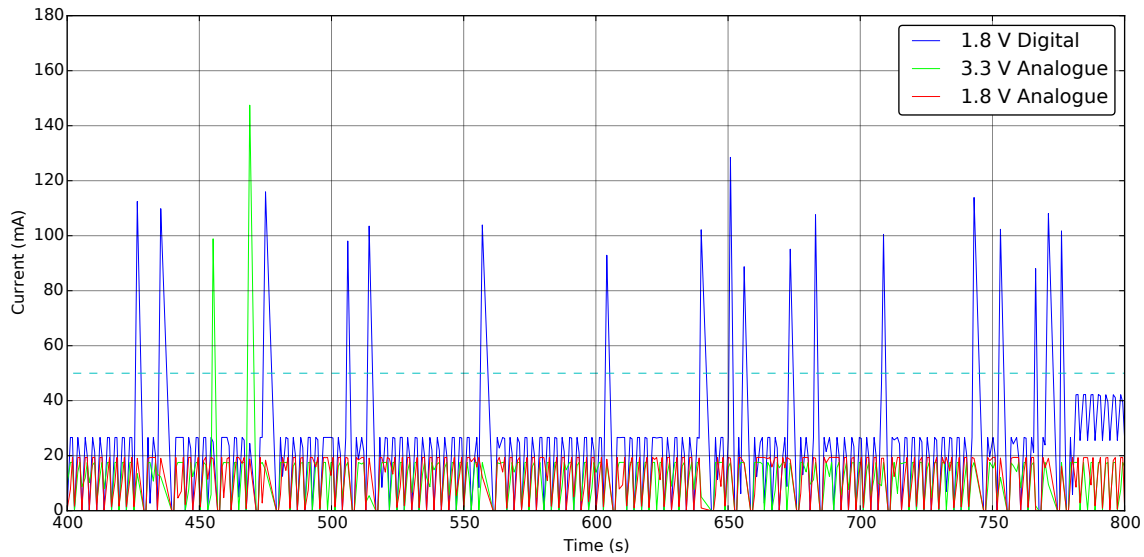


Figure 5.8: Example current log excerpt for all three supplies. There are also two unusual features shown: 3.3 V latchup and a <50 mA latchup around 800 s. The dashed line shows the detection threshold.

Sustained latchups

Some latchups were not quenched correctly. The MOSFET used to disconnect the power supply from the sensor did not stop the latchup in every case. When the MOSFET disconnect did not quench a latchup, that latchup had to be quenched manually by physically disconnecting the power supply and short circuiting the sensor supply rails. The problem was also unexpected, since it did not occur in previous work. Nevertheless, the occurrence of these "sustained" latchups was logged. The cause of the failure to quench latchups is a holding current provided by some other means than the supply rails. The suspected source of this holding current is the SPI pins, namely the chip select. Figure 5.7 shows the connections to the sensor including the power supply and measurement circuit. Duplicate connections to the sensor are not shown. In future, a more robust method of disconnecting all current sources from the sensor would be appropriate. In the previous testing of the standard Sapphire [98] no sustained latchups were recorded. It is not fully understood why they occurred in this experiment. Our work included the recommended supply decoupling capacitors on

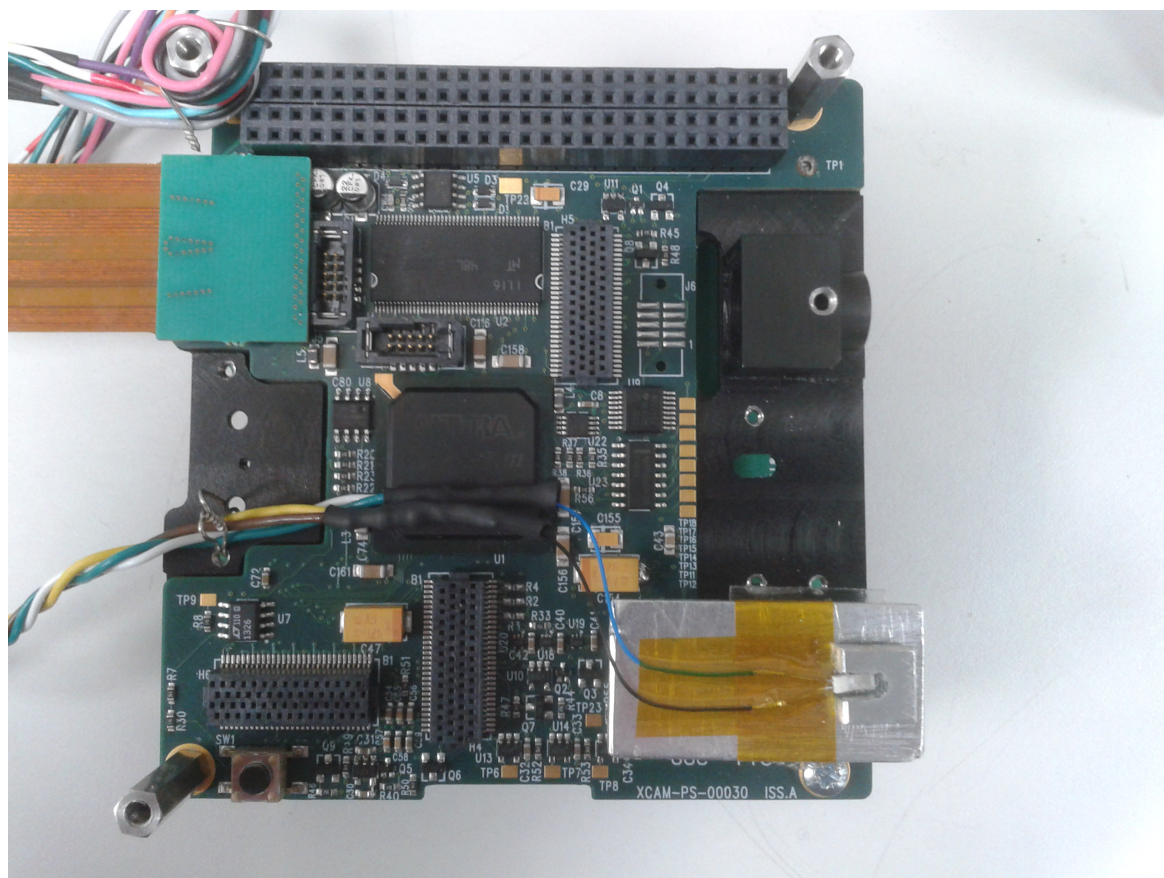
the sensor flex where the previous work did not and this could be the cause. Another difference between the experiments is the time between resets: previously it was a fixed window of one minute whereas our experiment reduced the time window from latchup to reset to a maximum of six seconds. The significance of this decreased window is that, despite the higher flux, instances of multiple simultaneous latchups were greatly reduced. Multiple simultaneous latchups introduce extra current paths through the device, so the holding current is shared between these paths. It follows that the holding current is higher when multiple simultaneous latchups are present since, multiple current paths must be supported. The D.C. holding current available through the SPI chip select was the same in each experiment, but in the present work the effective holding current was likely decreased as a result of fewer multiple simultaneous latchups.

5.1.7 Temperature measurement

In order to measure the temperature of the sensor, a block of aluminium was built onto the C3D board. A PRT was fixed to the block and the sensors were attached to the block. Care was taken to ensure the flatness of the sensor to achieve the correct effective LET. Temperature at the PRT was logged on the Picologger. The temperature setup is shown in Figure 5.9.

Temperature logs for each of the six experimental runs are shown in Figure 5.10. The DNW Sapphire #538 testing was split over two days, so the temperature profile was interrupted. Any effect of this interruption is not reflected in the cross sections for the DNW Sapphire (see Figure 5.13). This suggests that temperature control was adequate and did not influence significantly the errors on SEL sensitivity measurements. In each experiment the temperature was measured between 30 and 42 °C.

An example temperature log for a single LET run is shown in Figure 5.11. This temperature log is from the same run that produced the current log in Figure 5.8.



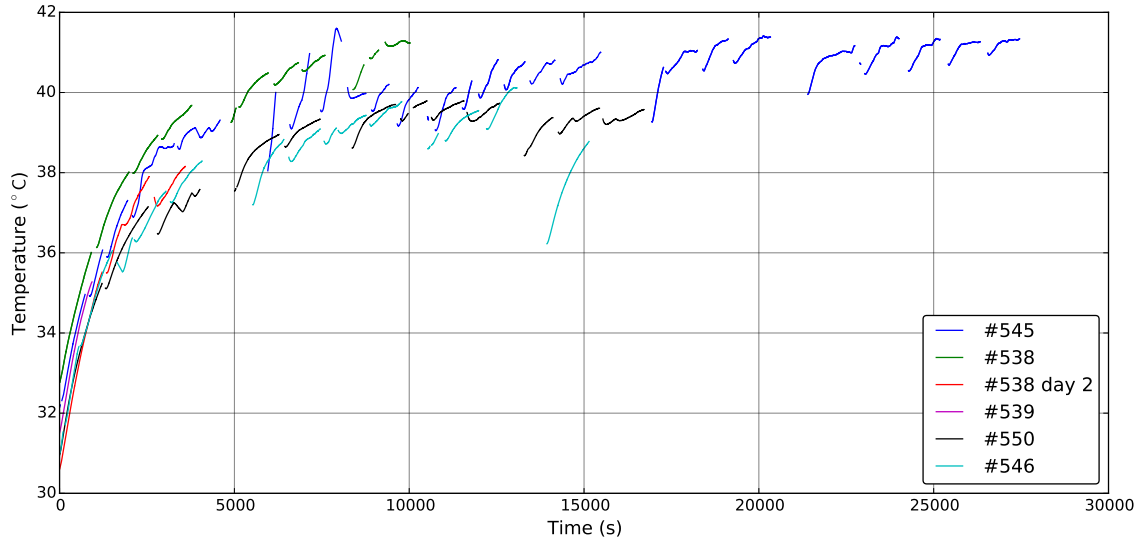


Figure 5.10: The temperature profile of the sensor for each of the six experiment runs. Each sensor has a similar profile. The device serial number are listed in Table 5.2.

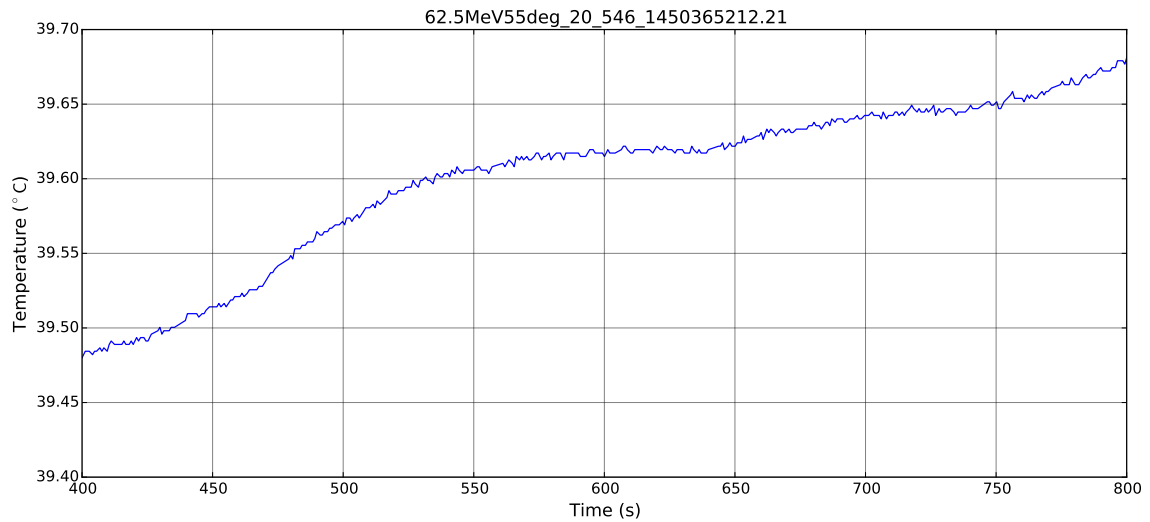


Figure 5.11: The temperature logged over the same period as Figure 5.8. No individual latches seem to have a noticeable effect on the temperature.

5.2 Experimental results

5.2.1 Phase locked loop

The Sapphire and Ruby sensors have on-board Phase Locked Loops (PLL) which allow the use of a lower frequency external clock which is multiplied up on chip. It was not possible for the PLL to be implemented with the deep n well underneath it. Consequently, the PLL circuitry on the deep n well Sapphire does not have deep n well underneath. Therefore, the first investigation was to whether the PLL itself was a significant source of latchup. If the PLL was much more susceptible to latchup than the rest of the chip it could obscure measurements into the effectiveness of the DNW in preventing SEL. The standard Sapphire was run with an external clock at 12 MHz (with the PLL on) and at 118 MHz (with the PLL off) and the SEL cross-section measured at $24.90 \text{ MeV cm}^2 \text{ mg}^{-1}$. Two fluxes were used: 1000 and 2000 ions $\text{cm}^{-2} \text{ s}^{-1}$. The results are shown in Figure 5.12. The cross sections are similar, although it was at this stage of the experiment that the uncertainty on estimating the cross-sections was realised (mostly due to the limited number of latchup events). However, it was decided that the PLL did not significantly affect the overall latchup cross-section of the sensors. This is not surprising as the PLL takes up only 0.3% of the chip area. All subsequent tests proceeded with the PLL enabled.

5.2.2 SEL susceptibility

The SEL cross sections for the four devices are plotted in Figure 5.13. The error bars (where given) are based on 10% uncertainty of flux and the uncertainty introduced by the finite number of latchups according to [99]. These results demonstrate that the standard Sapphire has a similar performance to the DNW Sapphire and to the $18 \mu\text{m}$ thick Ruby. The $5.5 \mu\text{m}$ thick Ruby has significantly better performance in terms of both saturation cross-section and threshold LET.

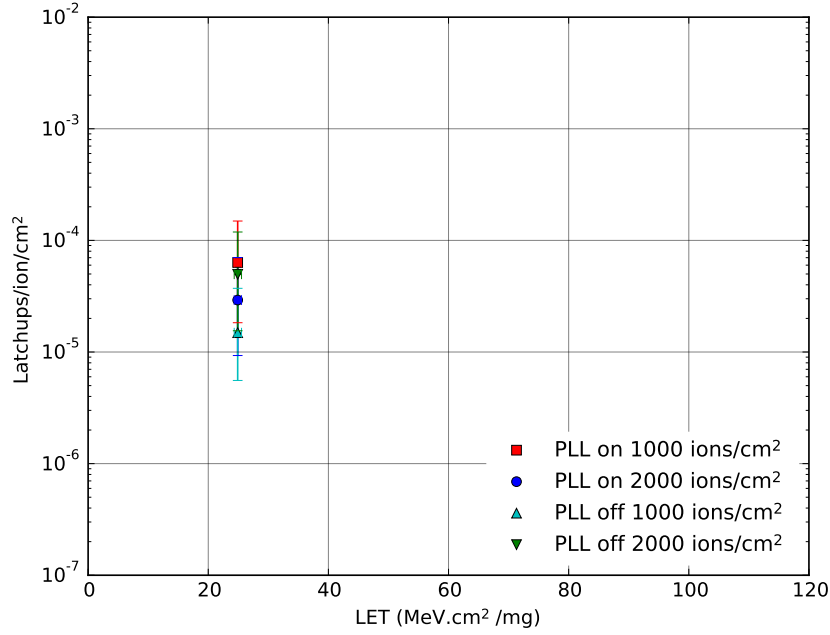


Figure 5.12: SEL cross-sections for the standard Sapphire with PLL on and off at two different fluences. No significant change in cross-section is apparent.

SEL cross section as a function of LET is usually modelled using the Weibull cumulative distribution function [100]

$$\sigma(L_i) = \sigma_0 \left(1 - \exp \left[- \left(\frac{L_i - L_0}{W} \right)^S \right] \right) \quad (5.1)$$

where L_i is the LET, L_0 is the threshold LET, σ_0 is the saturation cross-section, and W and S are fitting parameters. This model provides two parameters for characterising SEL susceptibility: The saturation cross section σ_0 which is the maximum possible cross section for any value of LET; and the threshold LET, L_0 , which is the LET below which SEL events do not occur. Such Weibull fits to the data, using a weighted least-mean-squares fit, are shown in Figure 5.14. The fitting parameters used are given in Table 5.3. The fits are to all data points, including at LETs where no SEL events occurred. The shaping parameter S has been constrained to $S \geq 1$ which implies that latchups become more likely with LET

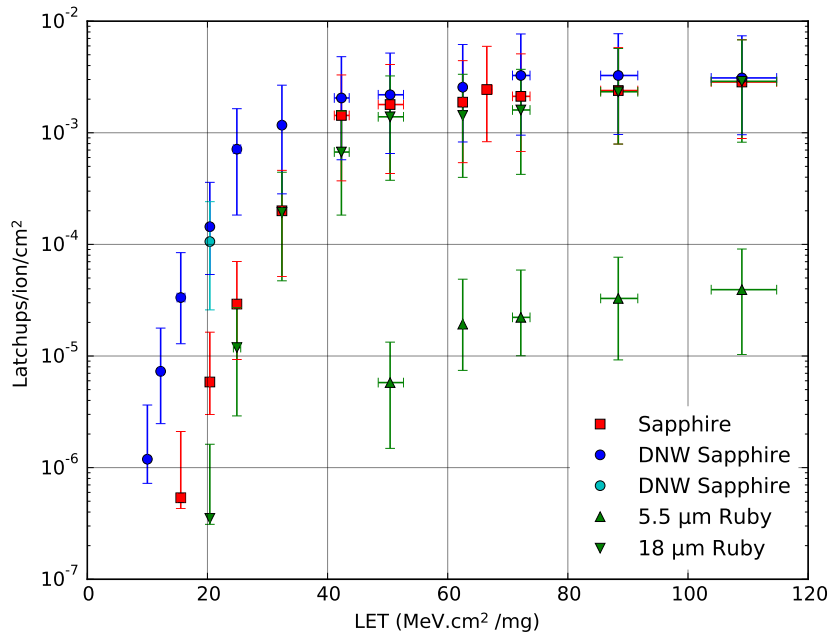


Figure 5.13: SEL cross sections for the four device variants tested. The DNW Sapphire device with serial number #539 was only tested at a single LET.

(as evidenced by the data).

Device	σ_0 (cm ²)	L_0 (MeV cm ² mg ⁻¹)	W (MeV cm ² mg ⁻¹)	S
Sapphire #545	2.19×10^{-3}	3.71	39.9	6.83
DNW Sapphire #538	2.76×10^{-3}	6.79	30.8	3.45
Ruby 5.5 μ m #550	4.11×10^{-5}	46.2	27.8	1.00
Ruby 18 μ m #546	1.80×10^{-3}	18.1	29.5	3.36

Table 5.3: Fitting parameters which provide the curves in Figure 5.14. Here, W and S are chosen independently for each device.

The characteristics described by Table 5.3 imply that the LET thresholds of the devices increase in the order: Sapphire; DNW Sapphire; 18 μ m thick Ruby; 5.5 μ m thick Ruby. The saturation cross sections are in the reverse order. The order of LET thresholds is interesting, because it places the LET threshold of the DNW Sapphire higher than the LET threshold of the Sapphire, even though a first glance at the data might give the impression given by the data is that the Sapphire has a higher LET threshold. In particular, the actual onset of

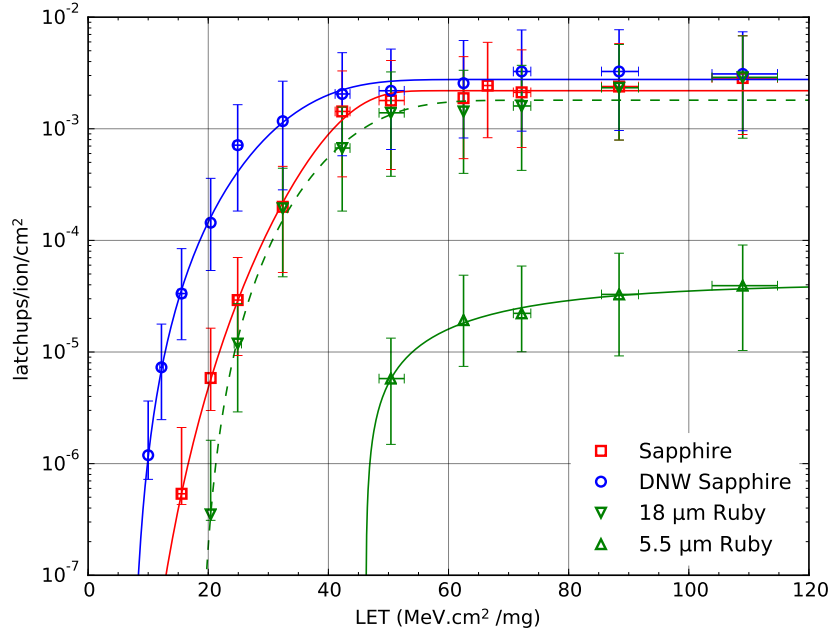


Figure 5.14: The SEL cross section data. Also shown are Weibull fits to the data, calculated with σ_0 , L_0 , W and S as free parameters. In the experiment the Sapphire began to latchup at a higher LET than the DNW Sapphire. However, because of the shape of the curve, the threshold LET is calculated to be lower. Error bars are based on 10% uncertainty of flux, angle of incidence uncertainty of 2° , and the uncertainty introduced by the finite number of latchups, according to [99]. Fit parameters are given in Table 5.3.

SEL was at a higher LET in the Sapphire compared to the DNW Sapphire. The apparent disagreement between the data and the extracted parameter of LET threshold comes about from the fact that the shapes of the fitted curves (i.e. the W and S parameters) differ.

To explore this, the same data is plotted in Figure 5.15 with weighted least-mean-squares fit amongst all data points in all four series, with the condition that W and S are the same for every series. The resulting fitting parameters are shown in Table 5.4.

From this analysis, the order of the extracted saturation cross sections are reversed for the Sapphire and the DNW Sapphire. The effect of the addition of the deep n well can be seen as simply reducing the hardness of the devices to latchup, since the threshold LET is reduced. Alternatively, the deep n well can be seen as changing the characteristic shape of the LET vs. cross section curve such that the metric of threshold LET is no longer useful

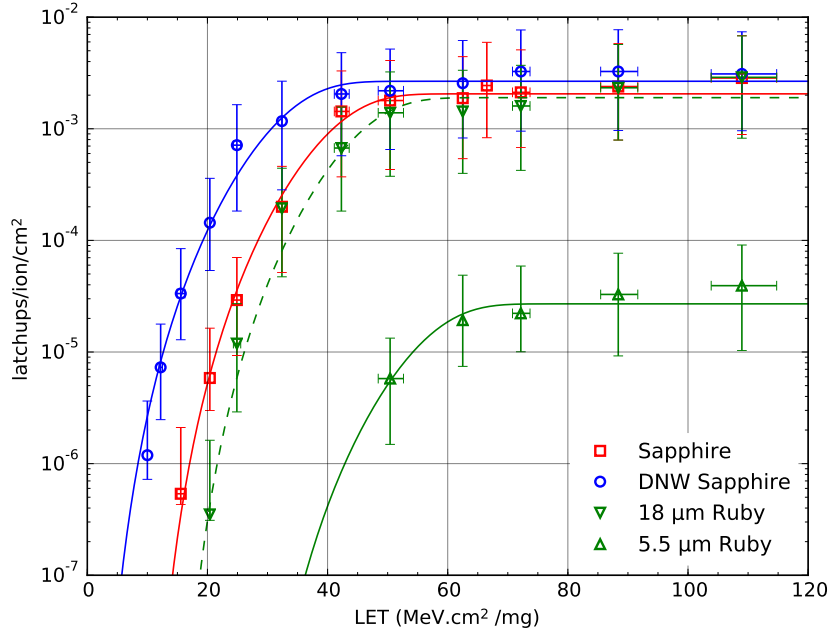


Figure 5.15: Here the Weibull fits to the data are calculated with W and S fixed across the four devices. Now all four curves have similar shapes, although the fits are not as good. The threshold LET is now higher for the Sapphire than for the DNW Sapphire which seems to represent the real data better. Once again the 18 μm thick Ruby performs better than either the Sapphire or the DNW Sapphire.

Device	σ_0 (cm ²)	L_0 (MeV cm ² mg ⁻¹)	W (MeV cm ² mg ⁻¹)	S
Sapphire #545	2.06×10^{-3}	9.08	34.4	4.21
DNW Sapphire #538	2.66×10^{-3}	0.87	34.4	4.21
Ruby 5.5 μm #550	2.70×10^{-5}	24.5	34.4	4.21
Ruby 18 μm #546	1.90×10^{-3}	13.6	34.4	4.21

Table 5.4: Fitting parameters which provide the curves in Figure 5.15. Here, W and S are kept constant for all four devices and are chosen to give the best fit overall.

for comparing the Sapphire and the DNW Sapphire.

It is possible that the deep n well has made the Sapphire more susceptible to latchup. The deep n well connects multiple n wells which reduces the resistance from V_{DD} to the pnp BJT base and reduces the pnp BJT gain. However, at the same time the deep n well has the opposite effect on the npn BJT. The base to V_{SS} resistance, and the gain, of the npn BJT both increase. In the deep n well device studied in this work the latter effect may

dominate, making SEL more probable. In the deep p well device the effects of reduced gain and resistance dominate, making SEL less probable.

In both analyses, the 18 μm thick Ruby has an increased threshold LET and we therefore suggest that the use of a deep p well in order to reduce latchup susceptibility in this process is worthy of further study.

The 5.5 μm thick Ruby has an LET threshold that is more than double any of the others and a saturation cross-section that is $\simeq 50$ times lower. This seems to be an anomalous result and should be discounted. The similarity in shape between the four curves (including the 5.5 μm thick Ruby) suggest that the 5.5 μm thick Ruby has reached saturation cross section. This means that the cross section will not increase beyond this at any LET and so a large proportion of the device area is simply not sensitive to SEL. This seems unlikely, as the device is designed to have the same topology as the 18 μm thick Ruby. A simple explanation would be that the ion flux reading was inaccurate, although this was double checked. Furthermore, the simulations of the 5.5 thick μm Ruby in Chapter 6 do not support the experimental findings in this chapter (in the simulations the grouping of the four devices is much closer). It should be mentioned that is a possibility that 5.5 μm thick Ruby results were correct and results for the other devices, plus those from the previous work, were anomalous but this is unlikely. Due to the high cost of using the HIF and the limited experimental time, the measurements on the 5.5 μm thick Ruby were not repeated.

5.2.3 Standard Sapphire vs. DNW Sapphire and comparison with previous work

As mentioned the impression from the SEL cross sections is that the DNW Sapphire has a lower threshold LET than the DNW Sapphire. It was hoped that the deep n well would harden the sensor against SEL. However, when the cross-sections are compared with those of previous work [98] the DNW Sapphire cross-section is more similar to that of the standard

Sapphire used in previous work as shown in Figure 5.16. This suggests that there is sufficient variation in manufacturing, or an experimental uncertainty which has not been accounted, which masks any differences in the SEL behaviour of the two device variants.

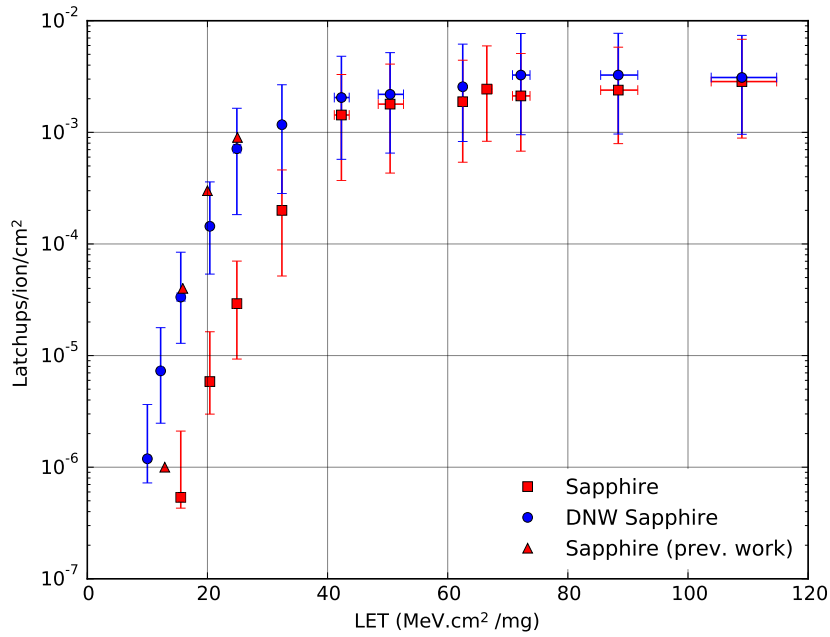


Figure 5.16: Comparison of the Sapphire SEL cross-sections measured in previous work with the two Sapphire devices tested at multiple LETs in this work. The previous work was on a device without a triple-well, however the results are in better agreement with the DNW device tested in this work.

5.2.4 3.3 V supply latchup

The 3.3 V supply powers amplifiers and the ADC on the Sapphire and Ruby devices. Both of these circuits contain PMOS and NMOS transistors. Table 5.5 shows the occurrences of latchup measured in the 3.3 V analogue supply. It is clear that when the high flux used when testing the 5.5 μm thick Ruby is taken into account the rate of 3.3 V latchup is much lower than the other three sensors. The low number of events makes precise cross-section estimation difficult. However, the 5.5 μm thick Ruby seems to have a higher threshold LET and lower saturation cross-section than the other three sensors.

Device	Effective LET ($\text{MeV cm}^2 \text{mg}^{-1}$)	Flux ($\text{ions cm}^{-2} \text{s}^{-1}$)	Number of 3.3 V latchups	Run time (s)
Sapphire #545	50.41	50	1	781
	72.17	21	3	786
	88.39	18	2	743
	108.97	16	3	810
DNW Sapphire #538	62.50	17	1	780
	88.39	22	1	585
	108.97	18	4	681
Ruby 5.5 μm #550	108.97	1864	10	777
Ruby 18 μm #546	62.50	48	4	713
	72.17	51	1	686
	88.39	19	6	677
	108.97	20	3	794

Table 5.5: Occurrences of 3.3 V latchups across all experiments.

5.2.5 Characteristics of SEL

Current consumption during each latchup was extracted from the current logs. Figure 5.17 shows the distribution of latchup currents in the four device variants at a single LET (50.41 $\text{MeV cm}^2 \text{mg}^{-1}$). The distributions show the latchup count, so the total area is dependent on the number of recorded events, not the cross-section. The number of sustained latchups per unit flux is lower in both of the Ruby sensors (sensors with deep p well).

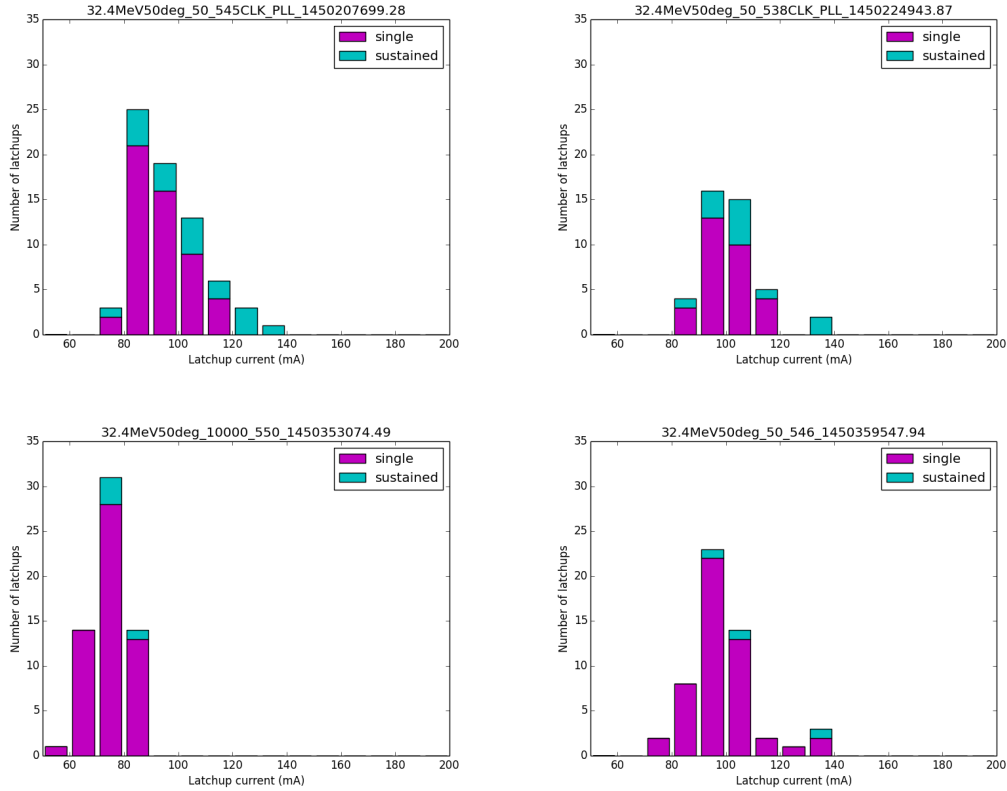


Figure 5.17: Latchup current distribution at $50.41 \text{ MeV cm}^2 \text{ mg}^{-1}$. Standard Sapphire (top left), DNW Sapphire (top right), $5.5 \mu\text{m}$ thick Ruby (bottom left), $18 \mu\text{m}$ thick Ruby (bottom right). Note: the number of latchups is not normalised to the run time.

Figure 5.18 shows the average current during latchup for each sensor as a function of LET. The average latchup current does not appear to be correlated to LET. The current in the $5.5 \mu\text{m}$ thick Ruby was significantly lower. The other devices had average currents between 89 and 119 mA, whereas the $5.5 \mu\text{m}$ thick Ruby current was between 74 and 77 mA. This result suggests that the $5.5 \mu\text{m}$ thick Ruby did not simply have an incorrect heavy ion flux, which could have partially explained the SEL cross section results. The significantly lower latchup current suggests that the device itself is different to the others.

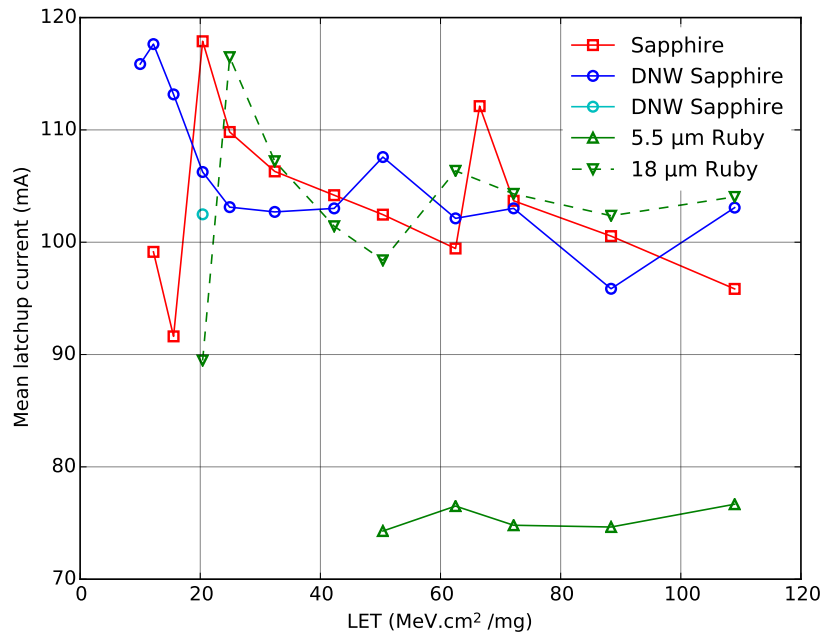


Figure 5.18: Average currents during latchup. There is no clear correlation between LET and average latchup current, which is as expected. There is a clear difference between the 5.5 μm thick Ruby latchup current and the other 4 devices which is not easily explained.

5.2.6 SEU susceptibility

The steady state operation of the device served two purposes: to simulate a realistic device operation mode and to collect information about SEUs. The SEU testing was not extensive and was a secondary objective of the testing. For this experiment the operation loop was:

- Write known values to 16 of the sensor's configuration registers.
- Read 10 frames of a test pattern image pre-programmed into the sensor to record frame read failure SEFIs (Section 5.2.7).
- Read back the 16 configuration registers to record register read bit-flip SEUs (Section 5.2.8).

The SEU test sequence was modified from previous work in [98]. The number of frame read attempts was reduced to make the sequence much faster: 6 seconds in our experiment.

The decision was made to continue with SEU recording even in the event of a latchup, even though this meant introducing dead time between latchups. In our experiment the maximum dead time is reduced from 60 seconds to 6 seconds. There is still a compromise between latchup dead time and losing SEU data in the case of a high frequency of latchups. However, we adjusted the balance in favour of recording latchups for this experiment. An interesting piece of further work would be to see whether SEU rate increased or decreased during an SEL.

5.2.7 Frame read failure SEUs

Frame read success or failure was recorded. A frame read failure is categorised as a SEFI since it indicates a failure of the sensor to communicate properly. In some cases, the failure was recoverable. In other cases, all subsequent reads also failed which certainly constitutes a SEFI within the sensor (as opposed to a bit-flip causing a communication protocol error).

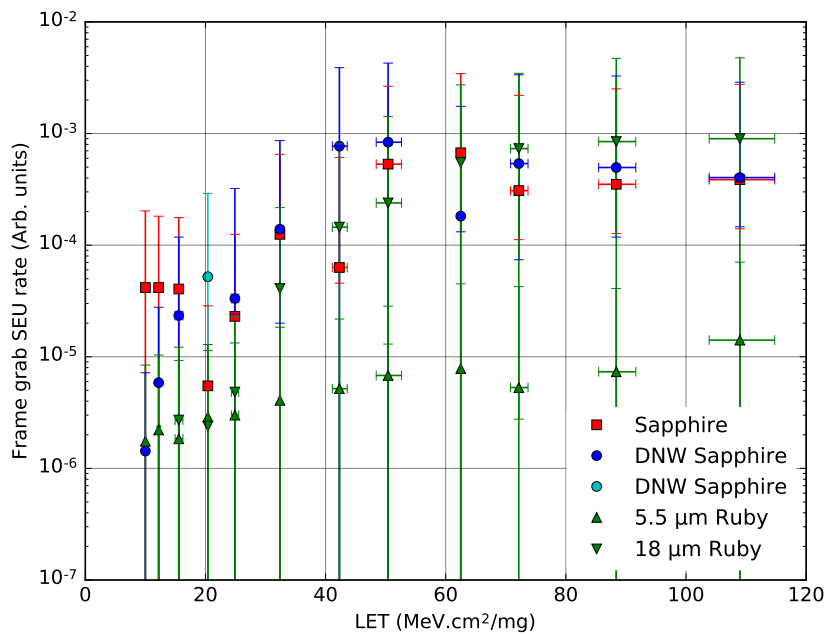


Figure 5.19: Frame capture failure rates.

Figure 5.19 shows the frame read failure cross-sections recorded for the five devices. The experimental uncertainty is large, but some information is apparent. Firstly, the 5.5 μm thick Ruby is the best performer at all but two LETs. Secondly, there is a trend in all the devices for the cross-section to increase with LET. However, this behaviour is not as pronounced in the 5.5 μm thick Ruby and the cross-section does not increase significantly with LET.

5.2.8 Register read failure SEUs

Corruptions in the 16 configuration registers which were read back were also recorded, as well as the contents of the registers. A bug in the code meant that only half of the actual value was recorded at the PC (the most significant byte). Nevertheless, the register corruptions are evidence of SEUs. The register failure cross sections are shown in Figure 5.20. Again, the experimental uncertainties are large. The register failure cross-sections increase with LET in all devices and again the 5.5 μm thick Ruby is the best performing. It can be argued that the worst performer is the standard Sapphire. The fact that the SEU and SEFI cross section curves do not have the characteristic shape as shown by the SEL cross sections is certainly influenced by the large uncertainties. However, it also suggests that the LETs and fluxes used were not suitable for finding soft error rates. The saturation LET may be well below the minimum LET used in our experiment which makes determining the threshold impossible. Indeed, soft errors of both kinds occurred at all LETs in all devices. The same was not true for SELs. The fact that these are complex, heterogeneous devices is also significant. Many circuits are involved in carrying out even simple operations. Circuits with vastly different LET thresholds may be operating. Therefore, a steady increase in cross-section as seen in SEL testing should not necessarily be expected. Finally, the effective flux for each circuit may be very different. For example, register upsets can happen when a flip-flop bit-flip occurs. This is possible at any time, whereas a communication error is likely to happen only

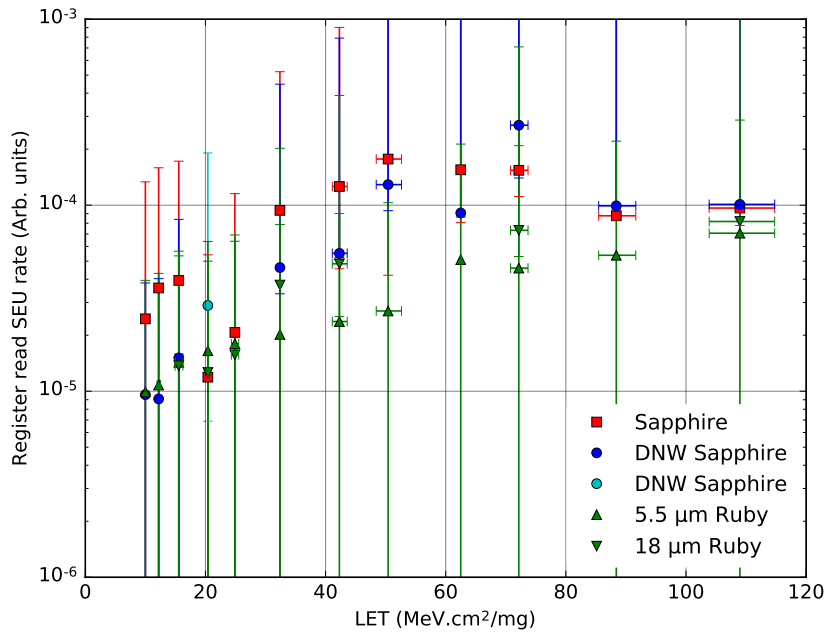


Figure 5.20: Register corruption rates.

while communications are taking place.

5.3 Conclusions

This chapter investigated the susceptibility to SEL of e2v CMOS image sensors. The two main aims were to investigate the effect of different process options (deep n well, deep p well, and varying epitaxial layer thickness and resistivity) on latchup threshold and cross section, and to establish the latchup cross-section of the standard Sapphire image sensor at higher LETs than previous work.

The standard Sapphire was the first sensor tested. Results were in reasonably good agreement with previous work.

The DNW Sapphire, which was manufactured with a deep n well under all of its 1.8 V digital circuitry, was expected to be resistant to latchup but in fact showed a slightly lower LET threshold (making latchup more likely at lower energies). The cross section at high

LETs was very similar to the standard Sapphire.

The 18 μm thick Ruby with a thicker and higher resistivity epitaxial layer than standard showed a slightly higher threshold and a similar cross section to the standard Sapphire. The Ruby has a deep p well. The 5.5 μm thick Ruby performed significantly better than the other three sensors. The saturation cross section was nearly two orders of magnitude lower, and the threshold LET approximately 2-10 times higher. This result is being treated as an anomaly requiring further investigation.

Latchup was observed a handful of times in the 3.3 V supply at high LETs, which was unexpected due to the relatively small circuit area. This could have occurred in the protection diodes at the chip pads, or in any of the 3.3 V analogue circuitry such as amplifiers, ADCs and voltage references.

The current consumption during latchup was measured in every instance. The main result from this data is that the 5.5 μm thick Ruby generally exhibits approximately 20% lower average current consumption during latchup than the other three sensors.

SEUs were measured during the normal operation of the sensor between latchups. A log was taken of frame-grab failures and register corruptions. The 5.5 μm thick Ruby outperformed the other devices but the experimental LETs were not in the correct range to find SEU threshold LETs.

The main conclusion from this chapter is that the use of deep n well did not have a strong effect on SEL sensitivity and may have made the sensors slightly more susceptible to SEL. The combination of deep p well and 18 μm epitaxial layer made the sensors slightly less susceptible to latchup, and should be considered as an option for increasing radiation hardness. These test devices feature complex circuitry with a wide range of transistor sizes and arrangements. It is quite possible that the different process options had opposite effects, in regards to SEL, on different circuits. Also, the sample size of one (two in the case of the DNW Sapphire) is small. Experimental uncertainties have been estimated, but the variation

in cross section between devices is not yet known.

5.4 Further work

The next chapter in this work is a computer simulation of SEL in device models based on the sensors used in this chapter. The results in this chapter could be improved by repeating the same experiments with a greater number of devices, particularly the 5.5 μm thick Ruby. It would also be worthwhile creating dedicated test chips with the same deep well structures but transistors of fixed sizes.

Ideally the simulation work in the next chapter would have been performed before the experimental work in this chapter. The experimental workflow evolved successfully during testing at the HIF where there are strict time constraints. Although the simulation work did not occur until many months after the experimental work, in future it would be useful to do simulations first. Better still, the experimental work should be split into two phases, where possible, with a separation to allow reflection on any unusual results and to confirm by simulation that the initial results are credible. In the case of this work, with hindsight (and knowing the results of the simulations) the 5.5 μm thick Ruby device should have been carefully retested using a fresh device. The break between the two sessions at the HIF in this work was 12 hours, which was enough time to reflect on the results but would not have been enough time to complete simulations.

Chapter 6

SEL simulation

6.1 Introduction

In this chapter, Technology Computer Aided Design (TCAD) is used to simulate the effect of heavy ion interaction causing latchup in a simple inverter circuit. Firstly, the motivation for producing the simulation output, which is a spatial map of threshold LET, and the steps necessary to use the simulation output to construct a realistic physical model are described. Then the Silvaco Atlas software used for the simulation is introduced, and the model described. Four models were constructed to represent the four devices used in the previous chapter: no deep well, deep n well, deep p well, and deep p well with 18 μm epitaxial layer.

Simulation outputs are shown in order to visualise qualitatively the effects of the different layers on SEL susceptibility, current density maps are shown for each of the devices. These show the current density immediately after the charge cloud is created and how the combinations of differently doped layers of silicon direct the newly created charge.

Plots of potential and electron concentration, developing over time, are shown in one device for LETs just above and just below the latchup threshold.

Finally, the LET threshold map in 2D is presented for each device, and these results are used to form cross-section vs. LET curves to allow a comparison with the results from the

previous chapter. The random processes, which must be accounted for in order to recreate the shapes of experimental cross section curves, are also discussed.

6.2 Cross section model

The purpose of the models in this chapter is to produce realistic cross section vs. LET curves using relatively simple device models.

6.2.1 Charge density threshold

In a real physical situation involving ion strikes there are uncertainties (discussed in Sections 6.2.2 and 6.4.1) which make SEL due to these energetic ions a probabilistic phenomenon. To simplify matters, it can be assumed that when an ion passes through the silicon a quantity of electrons and holes are placed at known locations within the device, each moving with known speed and direction. In this way, the latchup behaviour of the device can be modelled as being deterministic. After extracting the device behaviour under these assumptions from simulations, the results can be modified to reintroduce the effects of the random processes which were ignored during the simulations.

By using the *SINGLEEVENTUPSET* statement in Atlas, a volume of electron hole pairs of a specified density can be injected into the device model volume. The initial carrier velocities are zero. The subsequent time-domain solutions are deterministic (i.e. no Monte Carlo method is employed).

This assumption of deterministic behaviour leads to the concept of a latchup charge density threshold at every location (x,y) on the device [101]. For a particle at normal incidence, charge carriers are deposited with a density ρ . The cross section of each infinitesimally small area on the device (dA) is then either 0 (no latchup), or, above some threshold ρ_0 , is dA (latchup).

Figure 6.1 shows a plot of charge density (due to an interacting particle) and latchup cross section for such a hypothetical point cell on the device surface.

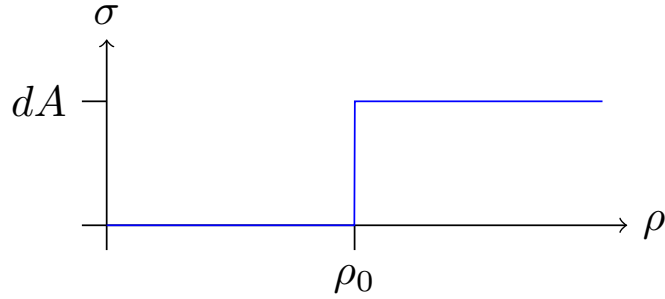


Figure 6.1: Behaviour of a hypothetical single cell, area dA , with a hard charge density threshold. This is what is obtained from a simulation with no Monte Carlo methods (i.e. Silvaco Atlas).

Under this assumption of fixed latchup threshold, it is in principle possible to construct a map of charge density threshold over the whole surface of the device. An example of a simple hypothetical 1-D map is shown in Figure 6.2.

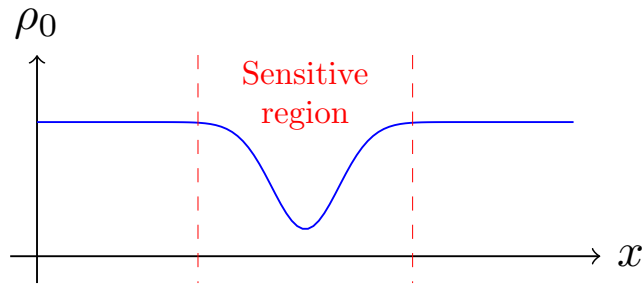


Figure 6.2: Hypothetical distribution of charge density threshold required for latchup, ρ_0 , across chip. For a beam which is uniform in x and y it is not necessary to know the spatial distribution.

When calculating SEL cross sections, it is not necessary to know positional information (in x and y) about the charge density threshold map $\rho_0(x,y)$. It is assumed that the ion strike location is uniformly distributed in x and y , so all that is needed is the Probability Density Function (PDF) for the random variable produced when sampling the charge density threshold map $\rho_0(x,y)$ for random, uniformly distributed values of (x,y) .

It is therefore possible to completely characterise the device susceptibility to latchup with the PDF $f_P(\rho)$. However, during the Silvaco simulation, the structure in $(x, y$ and $z)$ must be maintained to properly model the movement of electrons and holes.

6.2.2 Particle modelling

As mentioned, in the physical device there is no hard SEL threshold. However, the uncertainty on how particles of a certain energy, on a certain path, generating a cloud of e-h pairs with a certain shape and distribution will interact can be modelled as an uncertainty on the LET of the particle. The effect of such a distribution of particle LETs incident on a target with a hard threshold can then be calculated.

Additional sources of uncertainty act on particles with a nominal LET L_0 to determine the actual e-h pair cloud shape and distribution. The following can be considered intrinsic noise sources (as opposed to experimental error):

- The energy of the ions produced (i.e. by a cyclotron) will have a non-zero spread ΔE .
- Fano noise [102] will cause fluctuations in the actual number of e-h pairs generated per unit energy deposited.
- The path of each ion, and location of interactions, within the device will be random.

The model used here considers the charge density ρ at the ion strike location, so it is sufficient to use the PDF of ρ , $f_P(\rho)$. This describes the distribution of charge cloud densities achieved (for the purposes of the model) by particles which on average produce a charge density $\langle \rho \rangle$ (Figure 6.3).

6.2.3 Cross section vs. LET

The mean charge density will be proportional to the particle LET and depends on the size and shape of the charge cloud chosen for the model. From here on it is assumed that the

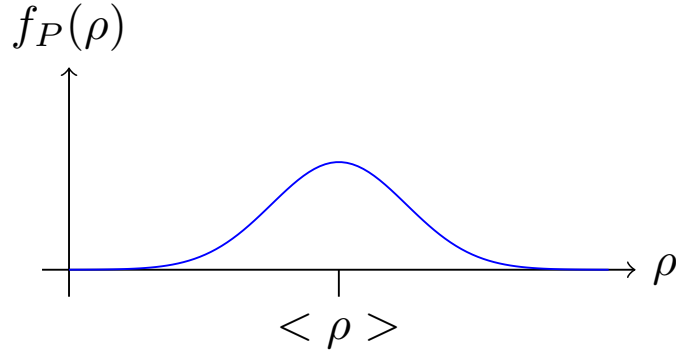


Figure 6.3: PDF of actual charge density for a chosen particle LET, which deposits a mean charge density of $\langle \rho \rangle$. The distribution will depend on mean LET chosen and must be estimated in order to account for probabilistic effects, including LET variations.

charge cloud is cylindrical in shape with the centre of the cylinder in the z direction. The distribution about the centre of the cylinder is a decaying exponential (see Section 6.3.4). This corresponds to an ionisation track from a particle travelling on a straight path in the z direction.

Once models for the charge density threshold and for the beam charge density have been established the chip cross section can be expressed as

$$\sigma = \int_0^{\infty} f_P(\rho) \int_0^Y \int_0^X g(\rho_0(x,y) - \rho) dx dy d\rho \quad (6.1)$$

where

$$g(x) = \begin{cases} 1 & x > 0 \\ 0 & x \leq 0 \end{cases} \quad (6.2)$$

and X and Y are the device chip dimensions in x and y respectively. In order to find a relationship between expected charge density (i.e. expected LET) and the device cross section, Equation 6.1 must be evaluated for the distribution $f_P(\rho)$ corresponding to each particle LET of interest.

6.3 Silvaco models

6.3.1 Introduction to Silvaco ATLAS

The Silvaco Atlas simulator [103] is a general purpose semiconductor device simulator. Atlas solves a set of fundamental equations, which are discretised, on a finite element grid used to represent the simulation domain.

The equations which are solved are Poisson's equation (Equation 6.3), the carrier continuity equations (Equations 6.4 and 6.5) and the transport equations.

Poisson's equation

$$\text{div}(\epsilon \nabla \phi) = -\rho \quad (6.3)$$

where ϕ is the electrostatic potential, ϵ is the local permittivity, and ρ is the local space charge density. The carrier continuity equations

$$\frac{\partial n}{\partial t} = \frac{1}{q} \text{div} \mathbf{J}_n + G_n - R_n \quad (6.4)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} \text{div} \mathbf{J}_p + G_p - R_p \quad (6.5)$$

where n and p are the electron and hole concentrations respectively, \mathbf{J}_n and \mathbf{J}_p are the electron and hole current densities respectively, G_n and G_p are the generation rates for electrons and holes respectively, R_n and R_p are the recombination rates for electrons and holes respectively and q is the elementary charge.

The transport equations provide physical models for the quantities \mathbf{J}_n , \mathbf{J}_p , G_n , R_n , G_p and R_p , and these equations make up the rest of the physics simulation. The simplest model is the drift-diffusion model.

6.3.2 Inverter model

In order to model the latchup behaviour of the 1.8 V digital circuitry on the Sapphire and Ruby devices, a model of an inverter circuit was constructed in Silvaco. Although simple, the circuit is susceptible to latchup. It is not practical to model every type of logic cell on the image sensor device, but results from the simulation of an inverter can be extrapolated.

A 2D model was constructed based on a cross section of the actual device layout, and on the available information on the process (i.e. the doping profile). This is only one of the many inverters on the image sensors. A cut-line was drawn on which to base the 2-D simulation. Because the drains and source are in different planes, only one logical connection, the source, was used in the simulation. For simplicity, the gates were not implemented, as they are not required for latchup. However, the latchup behaviour in different logic states (modified by the gates) would make an interesting further study.

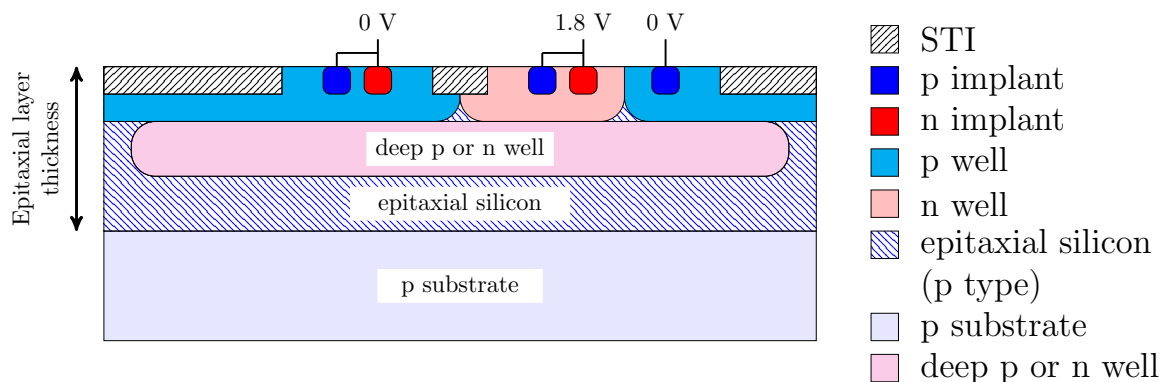


Figure 6.4: Inverter cross section used to make the 2D TCAD model. The structure was simulated without a deep well, with a deep n well, and with a deep p well. The epitaxial layer thickness was also varied.

Figure 6.4 gives an overview of the extent of the model. The epitaxial layer thickness, and the presence of a deep well of either doping are options in the model. Also shown is the Shallow Trench Isolation (STI) which is implemented on this process. The deep well extent was limited in order to allow correct biasing of the substrate. Well contacts and the two sources from the inverter are included in this structure, which is based on an actual inverter

layout. In the actual layout, sources and drains are not located in the same x, z plane. An additional well contact is included on the right hand side p implant which corresponds to an adjacent inverter.

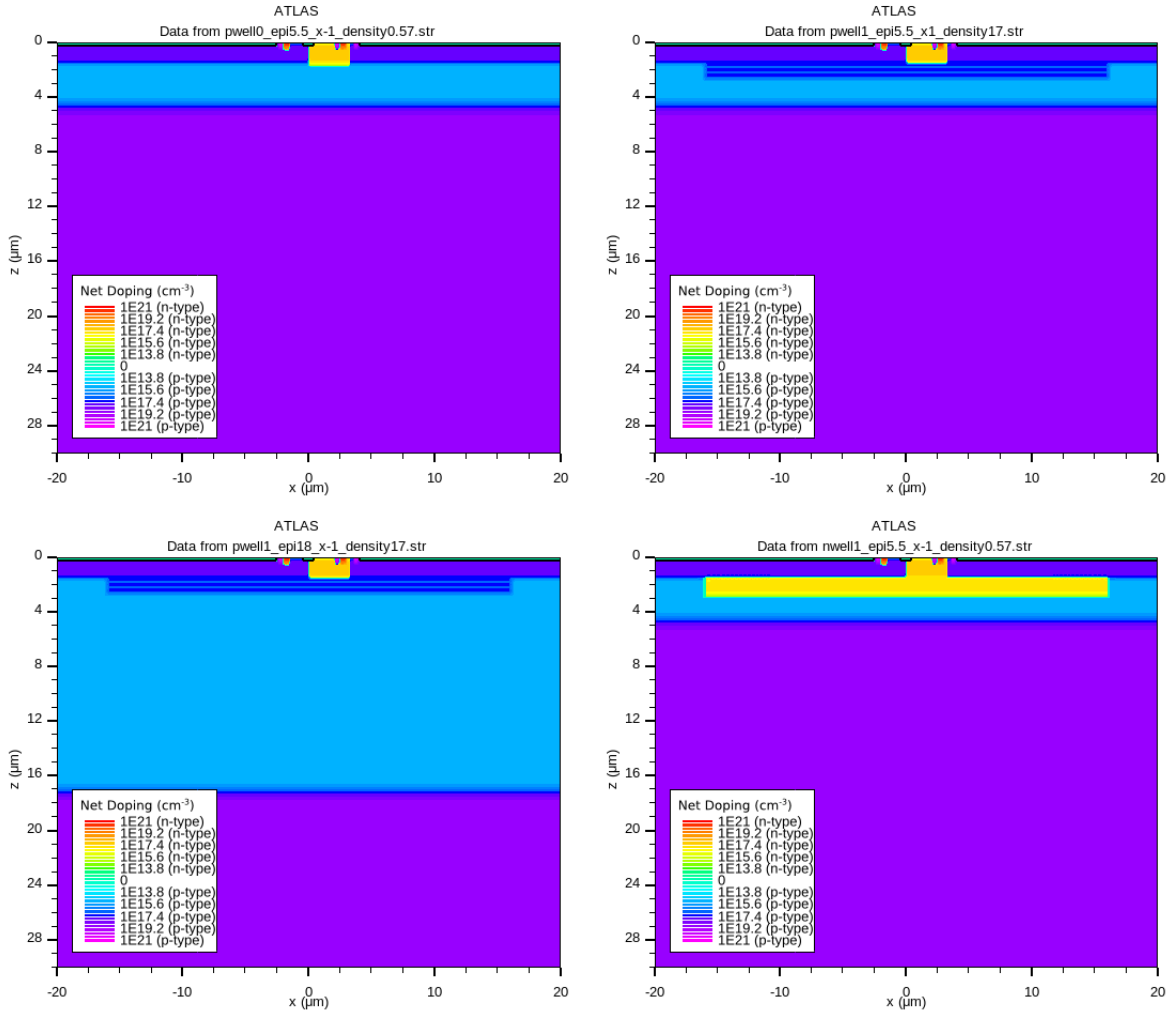


Figure 6.5: The four device structures simulated. No deep well (top left); deep p well (top right); deep p well with 18 μm epitaxial layer (bottom left); deep n well (bottom right). The doping is shown here and the full extent of the structure. A close up, showing the inverter in detail is in Figure 6.6.

A scale diagram of the models, zoomed in to the inverter itself, is shown in Figure 6.5. The absolute doping is plotted showing the actual implementation of the various implants. Figure 6.6 shows the inverter without either deep n or deep p well. The model extends far from the inverter itself for two reasons. Firstly, although device spacing will not usually be

so sparse on an actual device ($20\text{ }\mu\text{m}$ between cells), it is interesting to know how the effect of an ion strike changes as the strike location moves far away from the inverter. Secondly, the substrate bias is maintained by having the deep well not extend to the full width of the simulation. In reality, the deep well would be much larger (in x) so this width was chosen as a compromise.

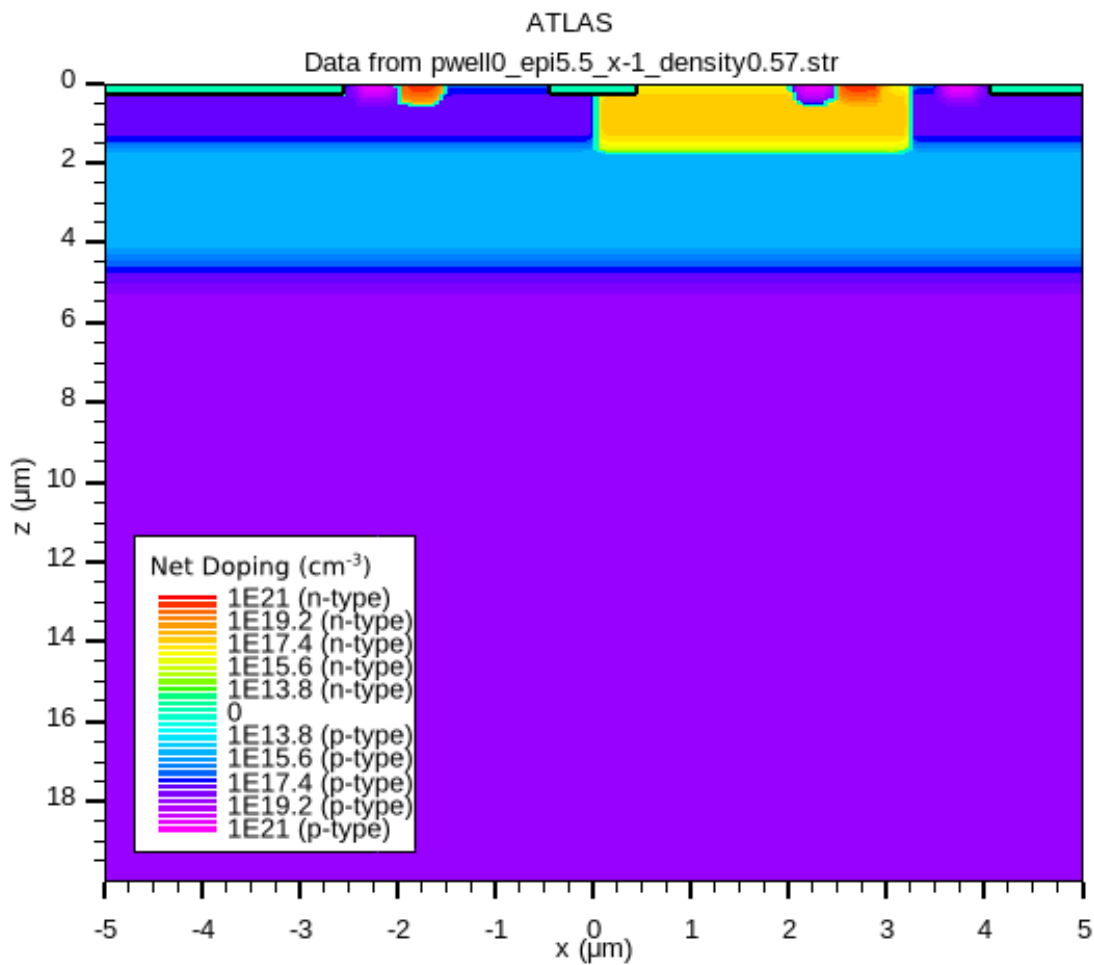


Figure 6.6: The no deep well structure, showing in detail the inverter.

6.3.3 Physical simulation models

The simulation was run using the following physical models: *fermi* (Fermi-Dirac statistics); *bgn* (Bandgap narrowing); *consrh* (Concentration dependent carrier lifetimes); *auger*

(Auger recombination); *cvt* (Lombardi inversion layer mobility model); and *impact selb* (Selberherr's Impact Ionization Model). Additionally, the majority carrier lifetimes were adjusted from their defaults to better reflect the long lifetimes present in the high-purity silicon used in image sensor processes. $\tau_n = 1e-3$ and $\tau_p = 1e-3$ were used. The full listing of simulation parameters (using the *print* statement) is given in Appendix A.

6.3.4 Ion beam simulation

In order to model the ionisation caused by a heavy ion the *SINGLEEVENTUPSET* statement was used. Statement parameters were chosen to give a charge generation rate in e-h pairs per cm^3 along the track length (from $z = 0$ to $30\mu\text{m}$) is given in the Atlas manual [103].

$$G(r,t) = S \cdot \text{DENSITY} \cdot R(r) \cdot T(t) \quad (6.6)$$

where r is the radial distance away from the ion path in μm and t is the simulation time in seconds. *DENSITY* is supplied in units of $\text{pC } \mu\text{m}^{-1}$ which is approximately equal to $100 \text{ MeV cm}^2 \text{ mg}^{-1}$. The factor

$$S = \frac{1}{q\pi \text{RADIUS}^2} \quad (6.7)$$

corrects the three-dimensional charge concentration according to *RADIUS* parameter which sets the rate at which the concentration falls off away from the ion path. The fall off is described by the term

$$R(r) = \exp\left(-\frac{r}{\text{RADIUS}}\right)^2 \quad (6.8)$$

The charge generation rate time dependency is given by the term

$$T(t) = \frac{2e - \left(\frac{t - T0}{TC}\right)^2}{TC\sqrt{\pi}\text{erfc}\left(\frac{-T0}{TC}\right)} \quad (6.9)$$

where $erfc(x)$ is the complementary error function

$$erfc(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \quad (6.10)$$

and $T0$ and TC are constants. For this work $T0 = 4 \times 10^{-12}$, $TC = 7 \times 10^{-14}$ and $RADIUS = 0.05 \mu\text{m}$ was used.

6.3.5 Carrier behaviour changes due to device structure changes

The electric fields present in the devices are determined by the doping profile and the bias applied. Large fields are present in a depletion region between n and p regions due to the opposite polarities of the ionised atoms in the crystal in these regions. A smaller field exists between regions of different doping concentration. These fields govern the movement of the e-h pairs generated in a charge cloud due to ionising particles. It will be seen in Section 6.3.7 that these fields can collapse when charge clouds approaching the magnitude required for latchup are present. Nevertheless, once the fields are restored they play a crucial role in directing the charge towards or away from sensitive areas.

Figures 6.7 to 6.9 show the simulated electron current density (both magnitude and direction) immediately after an ion strike. The current density has the conventional sense, i.e. opposite to the direction of electron movement. The top of each figure shows an ion strike at $x = 1 \mu\text{m}$, which means that the ion integration begins in the n well. The bottom of each figure is for an ion strike at $x = -1 \mu\text{m}$, which corresponds to an equal distance on the opposite side of the p-n junction. The charge density is constant in the z dimension. The three figures are for no deep well, deep p well, and deep n well respectively.

In the case of the ion strike into the no deep well device (Figure 6.7) there is a large flow of electrons into the n well from the epitaxial layer. The lateral electron flow (in the x dimension) is largest in the epitaxial layer (*ii*), smaller in the n well (*i*), and smallest in the

substrate (iii). The electron flow into the p well from the epitaxial layer is smaller than the flow into the n well from the epitaxial layer. Electrons flow laterally out of the p well at a similar rate to the n well (vi). The flow of electrons upwards through the substrate and the epitaxial layer towards the p well is greatly reduced (vii).

Structure	Strike location	Label	Effect of deep well
No deep well	$x = 1 \mu\text{m}$	-	-
	$x = -1 \mu\text{m}$	-	-
Deep p well	$x = 1 \mu\text{m}$	iv	Rate of electron movement away from n well - p well junction is increased.
	$x = -1 \mu\text{m}$	-	None/weak.
Deep n well	$x = 1 \mu\text{m}$	v	Rate of electron movement into n well is reduced by the presence of deep n well.
	$x = -1 \mu\text{m}$	viii ix	Electrons flow away from centre of p well; Electrons move towards centre of deep n well.

Table 6.1: A summary of the effects on electron movement due to deep n well or deep p well. Based on electron current density immediately following an ion strike as shown in Figures 6.7 - 6.9

Observations of the effects of the additional deep wells on the electron current density immediately after the ion strike are summarised in Table 6.1. The deep p well has a small effect, slightly increasing the lateral flow away from the p-n junction (iv). The effect of the deep p well when the ion strikes in the p well is negligible (vi). In the case of the deep n well, the electron flow into the n well is reduced (v), due to the movement of the junction (the deep n well replaces the deep p well or the epitaxial layer). Electrons flow into the deep n well from both the p well and the epitaxial layer.

The observations detail only the movement of electrons. The latchup behaviour ultimately depends on whether the resulting concentrations lead to sufficient currents in the parasitic BJTs to trigger a latchup condition. The effects of these various structures are assumed to have an equal and opposite effect on hole currents, since at the time of the ion

strike the electron and hole concentrations are almost equal.

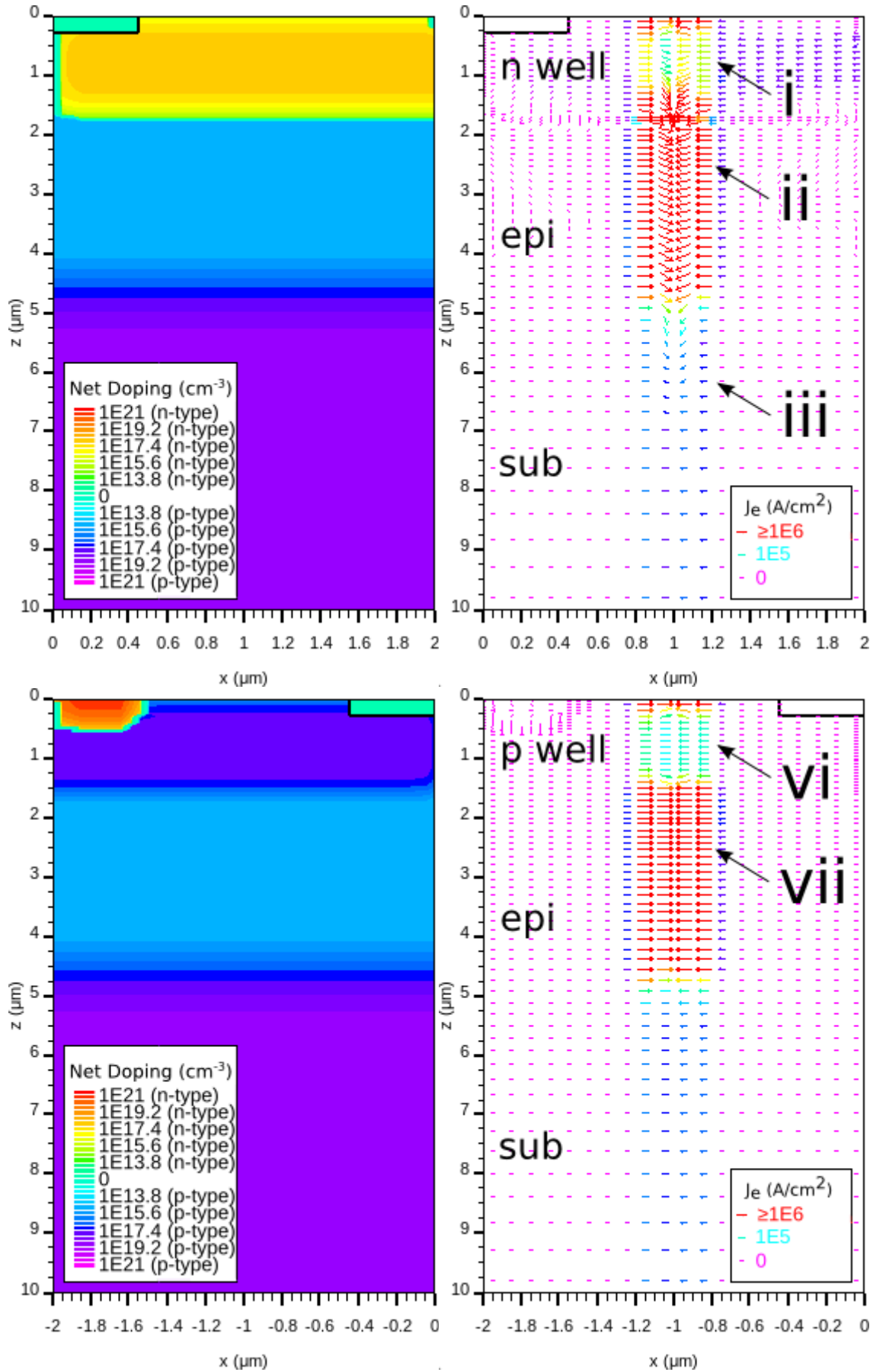


Figure 6.7: No deep well. Right: electron current density immediately after ion strike at $x = 1 \mu\text{m}$ (top) and $x = -1 \mu\text{m}$ (bottom). The doping in these locations is shown on the left.

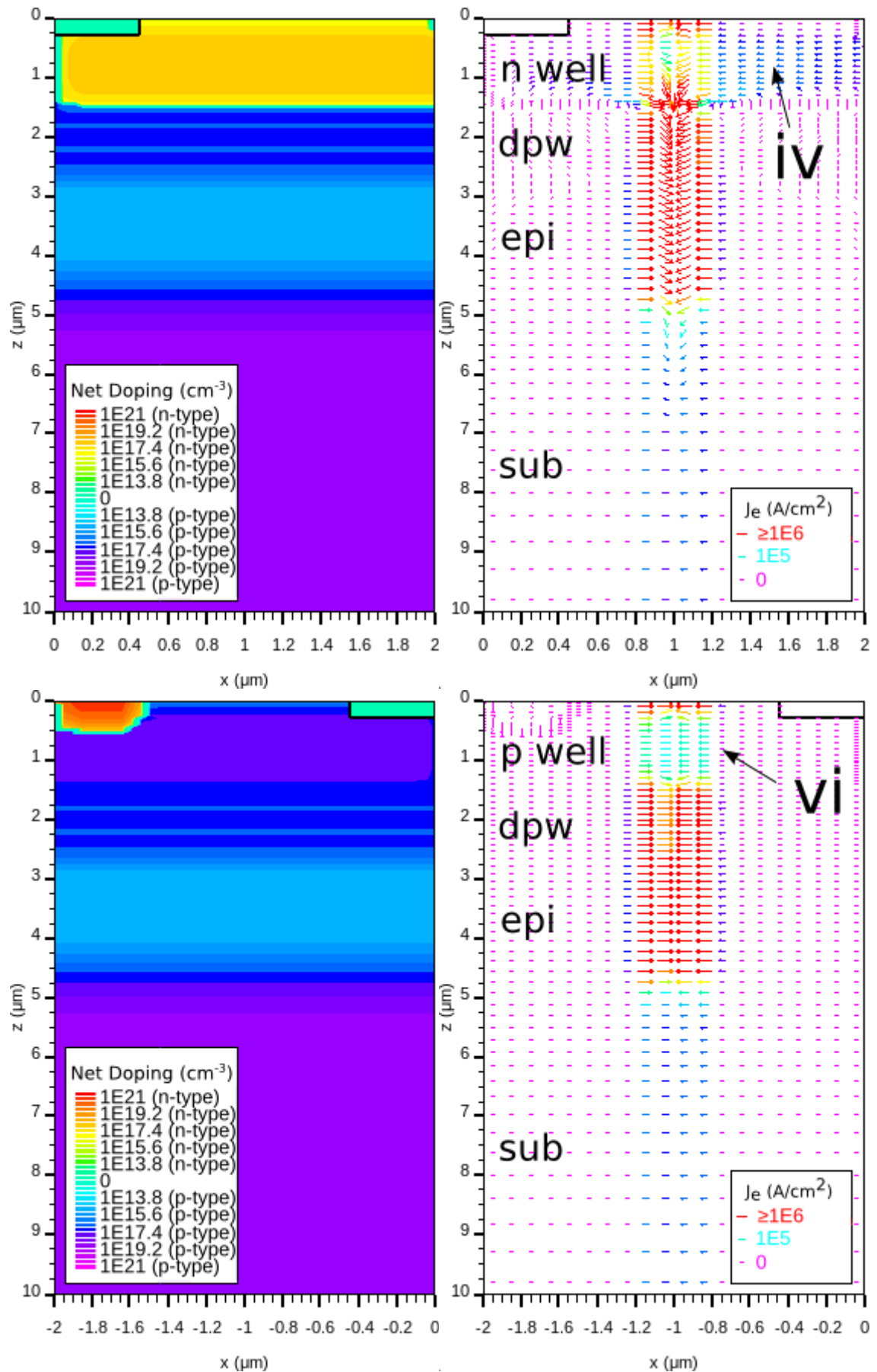


Figure 6.8: Deep p well. Right: electron current density immediately after ion strike at $x = 1 \mu\text{m}$ (top) and $x = -1 \mu\text{m}$ (bottom). The doping in these locations is shown on the left.

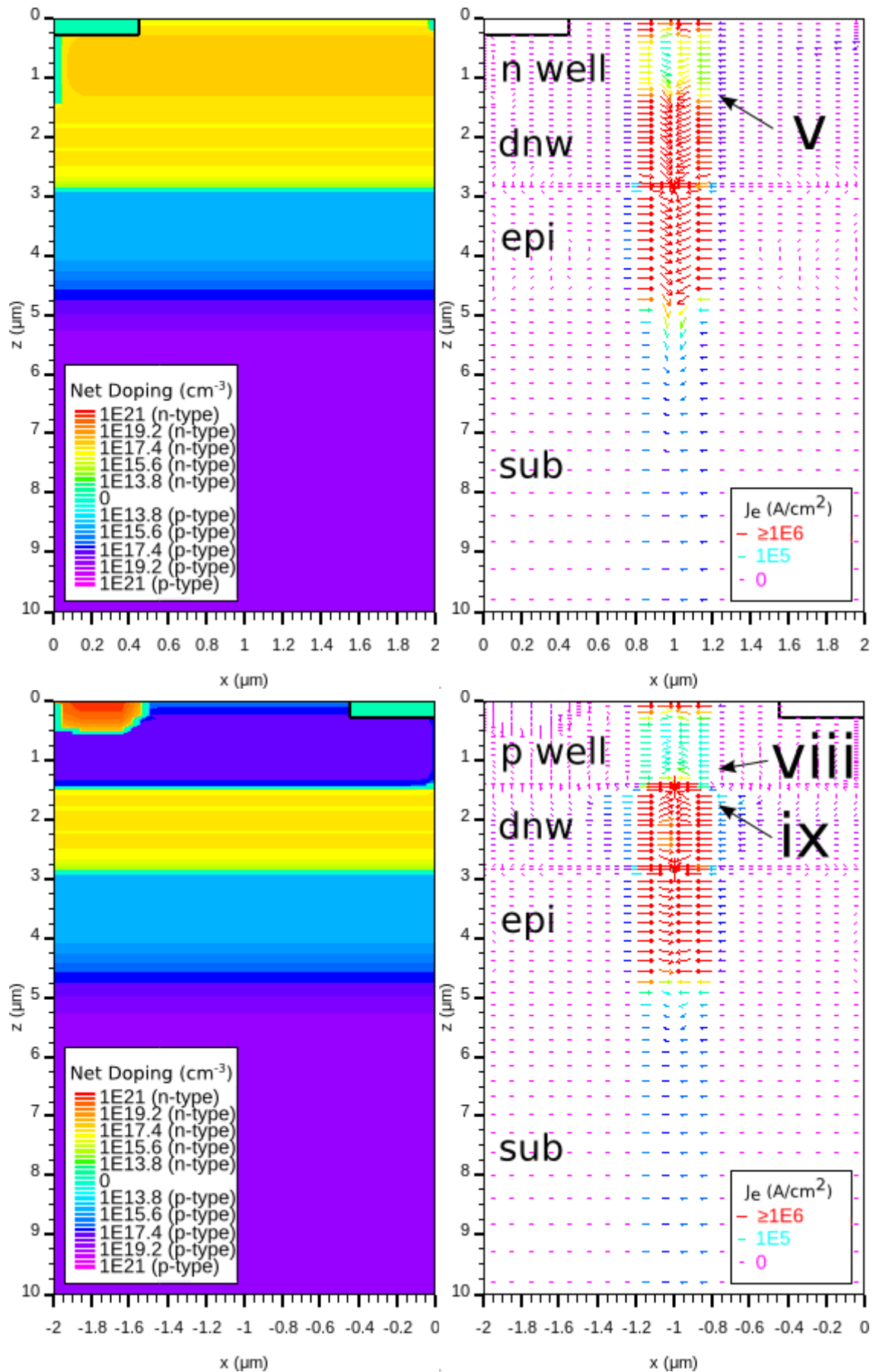


Figure 6.9: Deep n well. Right: electron current density immediately after ion strike at $x = 1 \mu\text{m}$ (top) and $x = -1 \mu\text{m}$ (bottom). The doping in these locations is shown on the left.

6.3.6 Latchup threshold search algorithm

In order to find the latchup charge density threshold ρ_0 , simulations were run with different charge densities. The output from the simulation was taken as the final current I_{final} achieved after a simulation time of 20 ns. The Brent search algorithm [104] from the scipy optimize library was then used to find the root of

$$0 = I_{final}(DENSITY) - I_{thresh} \quad (6.11)$$

where $DENSITY$ is the charge density and I_{thresh} is a value for current chosen to be

$$I_{thresh} \approx (I_{max} - I_{min})/2 \quad (6.12)$$

where I_{max} is a typical final settling current for latchup (≈ 40 mA) and I_{min} is the final settling current when latchup does not occur (≈ 0 mA). In all cases I_{final} was chosen as 20 mA. The maximum number of iterations was set at 15.

Figure 6.10 shows the current ($I_{V_{DD}}$) change over time during simulation of the no deep well device model. Here, the simulation was allowed to continue to 100 iterations in order to show the current for charge densities very close to the threshold. Only selected charge densities are shown.

6.3.7 Potentials and carrier concentrations during latchup and non-latchup events

Figures 6.11 to 6.14 show the potential and electron concentration in the no deep well device at different times after an ion strike. In each figure the concentrations and potentials are plotted for a strike of $1 \text{ pC } \mu\text{m}^{-1}$ (upper plot), and for $2 \text{ pC } \mu\text{m}^{-1}$ (lower plot). The location of ion strike is $x=1 \text{ } \mu\text{m}$. The SEL threshold for the device at this location is between the

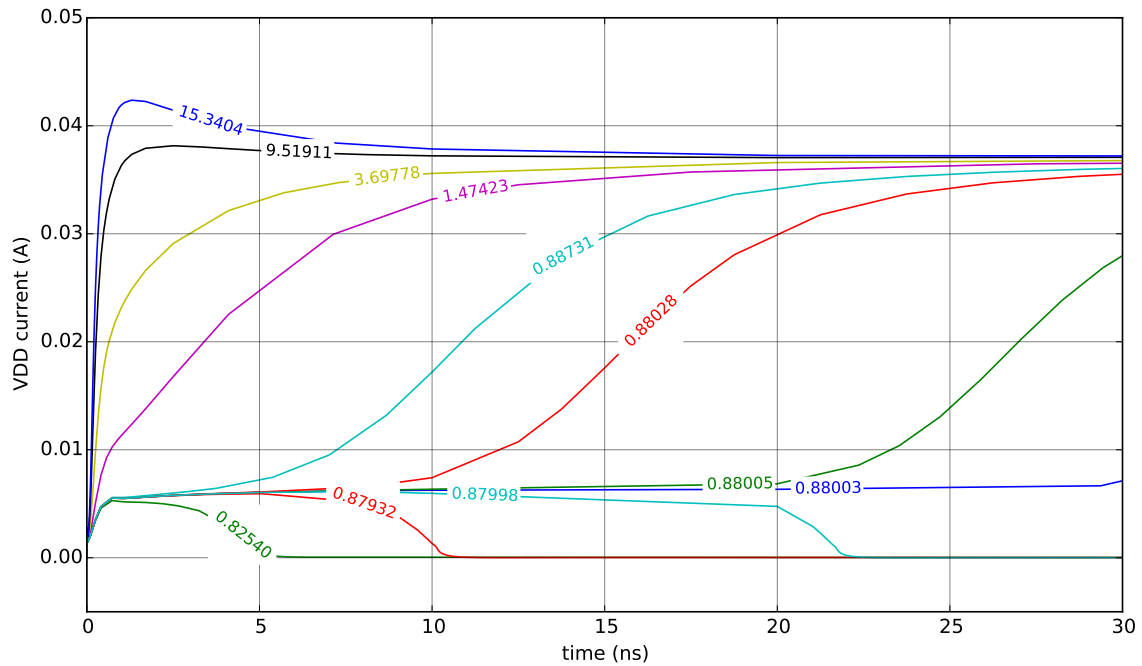


Figure 6.10: In order to find the charge density threshold the device is simulated with multiple charge densities. The sequence of charge densities simulated is computed by a Brent search algorithm. The search algorithm attempts to optimise the charge density to achieve a final current (at 20 ns) midway between the latchup current and the non-latchup current. In this case the midpoint is chosen as 20 mA. The charge densities indicated for each curve have units of $\text{pC } \mu\text{m}^{-1}$. Here the algorithm has been allowed to run up to 100 iterations and therefore shows the current logs a charge densities very close to the threshold ($0.88000 \text{ pC } \mu\text{m}^{-1}$). The current can remain unstable for tens of nanoseconds before the current either increases to the latchup current or drops to the leakage current. In each case the latchup current and leakage current are identical.

two charge cloud densities, so these plots track the changes in quantities after an ion strike leading to latchup, and after an ion strike which does not cause a latchup.

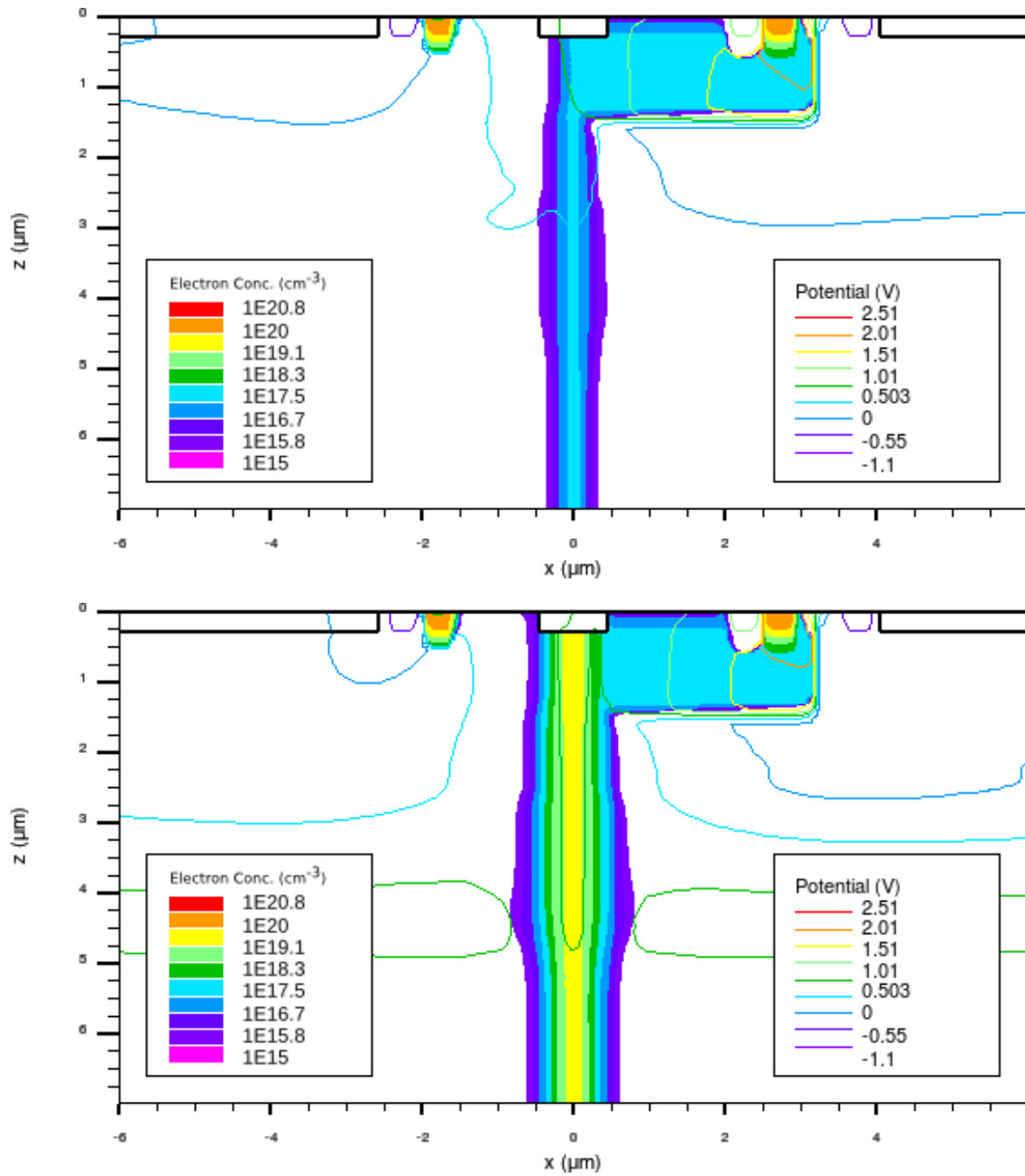


Figure 6.11: Electron concentration and the potential structure plotted for a charge density of $1 \text{ pC } \mu\text{m}^{-1}$ after $5.11 \times 10^{-12} \text{ s}$ (top) and $2 \text{ pC } \mu\text{m}^{-1}$ after $5.25 \times 10^{-12} \text{ s}$ (bottom). The potential barrier between n and p wells has broken down in both cases.

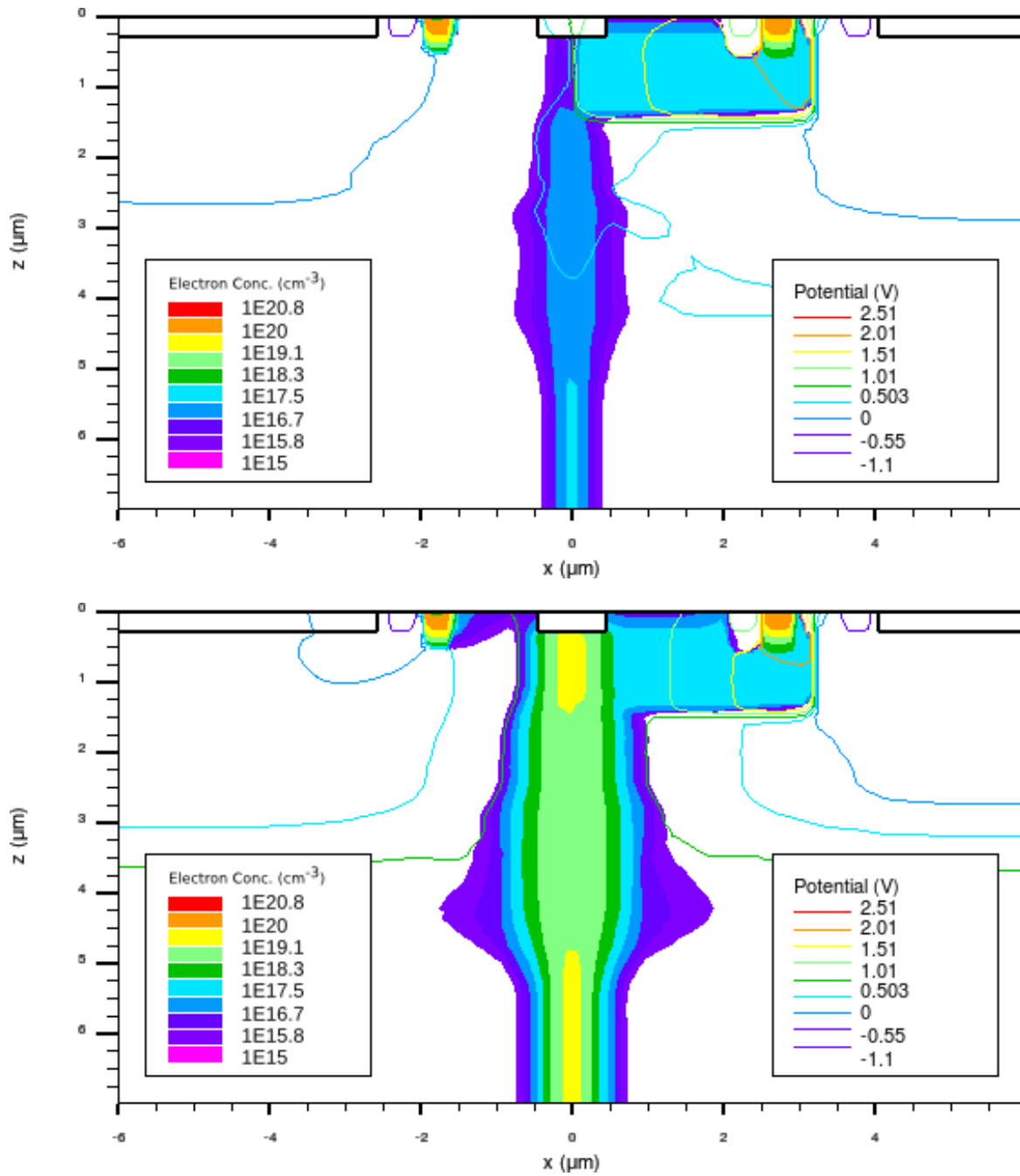


Figure 6.12: Electron concentration and the potential structure plotted for a charge density of $1 \text{ pC } \mu\text{m}^{-1}$ after 1×10^{-11} (top) and $2 \text{ pC } \mu\text{m}^{-1}$ after $1 \times 10^{-11} \text{ s}$ (bottom). In the former case the potential barrier has been restored (at $x = 0$, below the STI). In the latter, the higher density charge cloud has triggered a latchup event which prevents the barrier from re-forming.

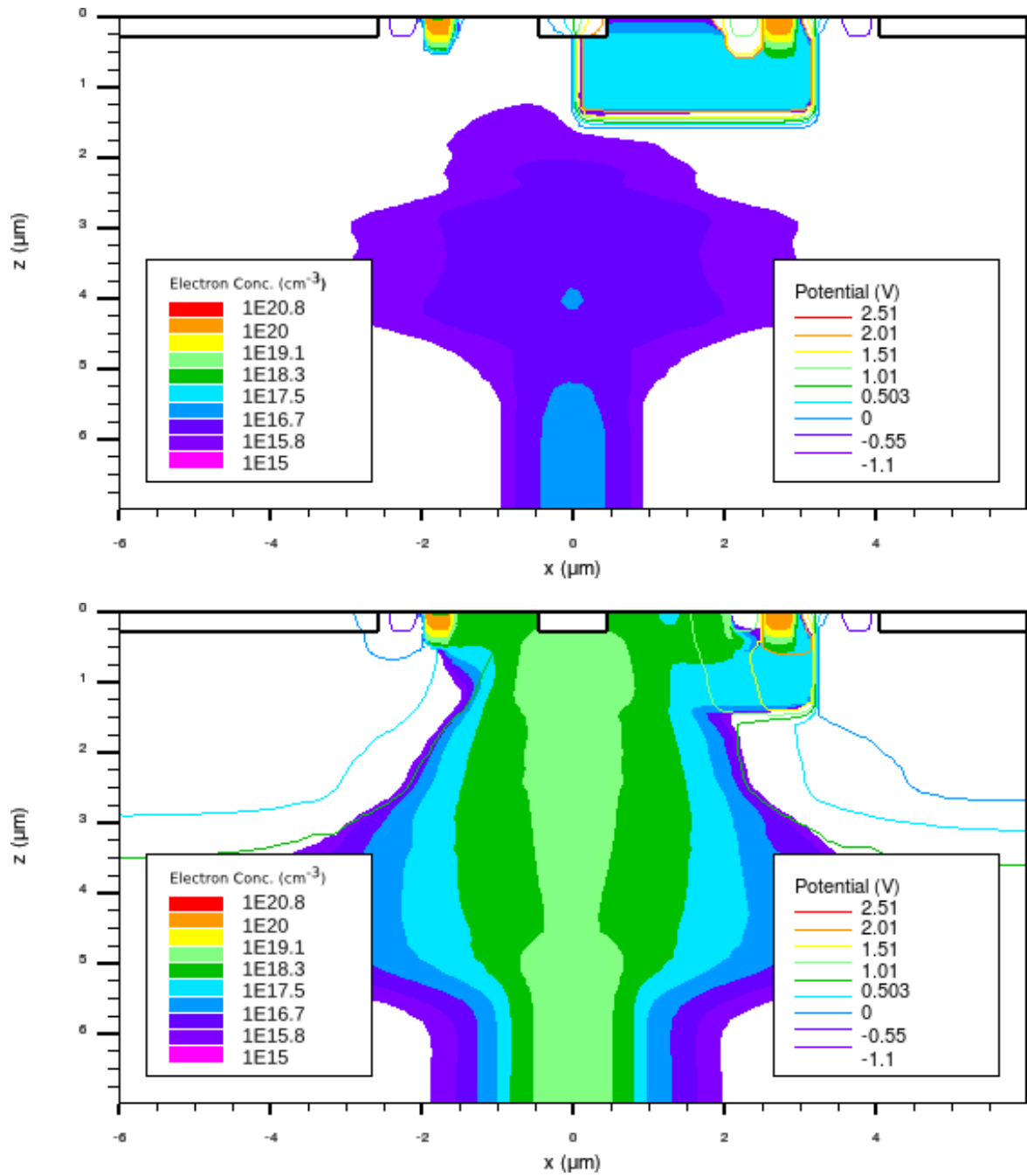


Figure 6.13: At $t = 1 \times 10^{-10}$ s the charge from the lower density strike has largely dissipated. The higher density cloud remains. The effect of the high purity epitaxial silicon can be seen. The electrons diffuse quickly in this region, but there is little recombination.

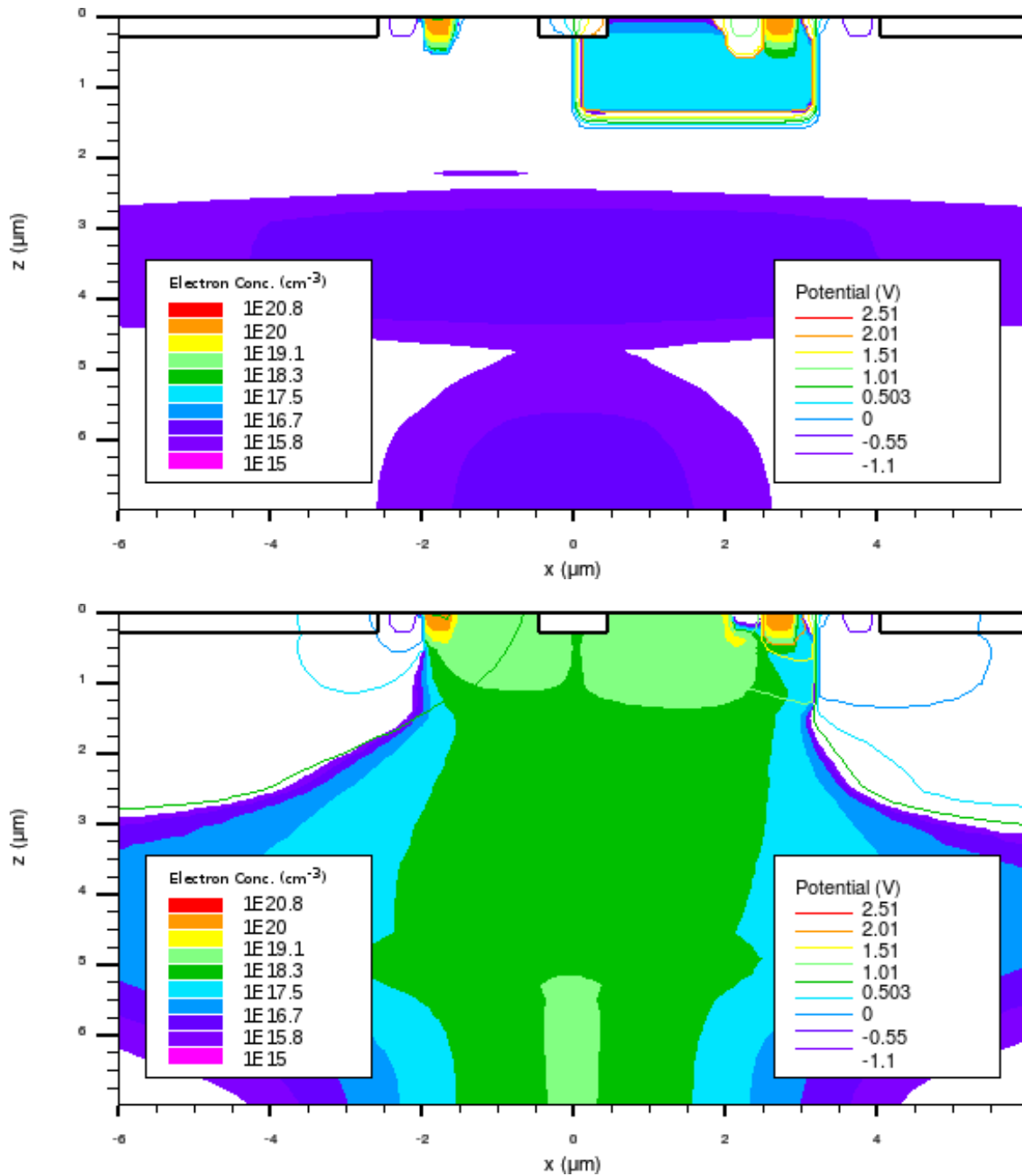


Figure 6.14: At $t = 1 \times 10^{-9} \text{ s}$ the concentrations and potentials after the $1 \text{ pC } \mu\text{m}^{-1}$ strike are almost back to where they were before the strike (top). After the same amount of time, the larger strike (bottom) is not yet dissipated, but the electron concentration has started to increase again around both source regions. These injected electrons are carrying I_{VDD} . This device is now in latchup.

6.3.8 Simulation outputs for devices experimentally studied

Using the method described in Section 6.3.6, latchup charge density thresholds were found in models representing the four devices analysed experimentally in Chapter 5. The thresholds were found for ion strike locations between $x=-5\text{ }\mu\text{m}$ and $x=5\text{ }\mu\text{m}$, at intervals of $1\text{ }\mu\text{m}$. The results are shown in Figure 6.15. This provides a 1-dimensional map of the latchup charge density threshold for each device. The p-n junction at the centre of the inverter (at $x=0\text{ }\mu\text{m}$) is the most sensitive region of the device as expected, and the sensitivity falls off further away from this point. The asymmetry of the plot shows how the n well and p well sides of the inverter have their sensitivity affected differently by the presence of the different deep wells and the epitaxial thickness. However, the main result from these curves is that the charge density thresholds are remarkably similar for each device. At the edge ($x=5\text{ }\mu\text{m}$) there is only a factor of two difference, and at the p-n junction ($x=0\text{ }\mu\text{m}$) approximately 10% more charge is required to produce latchup in the $5.5\text{ }\mu\text{m}$ deep n well device over the $5.5\text{ }\mu\text{m}$ no deep well device.

The results in Figure 6.15 suggest that the experimental results for the $5.5\text{ }\mu\text{m}$ Ruby were anomalous.

6.4 Extrapolation of simulation output to full device cross section model

In order to contextualise the 1-dimensional charge density threshold map results, first the results are extrapolated into a 2-D map. This map was a simple rotation of the positive and negative x data by $\pm\pi/2\text{ rad}$ about the point $x=0, y=0$ with a linear interpolation. The model is now rather crude, and somewhat removed from the original inverter 2-D layout information. However, this extension to 2-D is an attempt to adequately represent the relative size of the sensitive p-n junction compared to the larger, relatively insensitive, area around it.

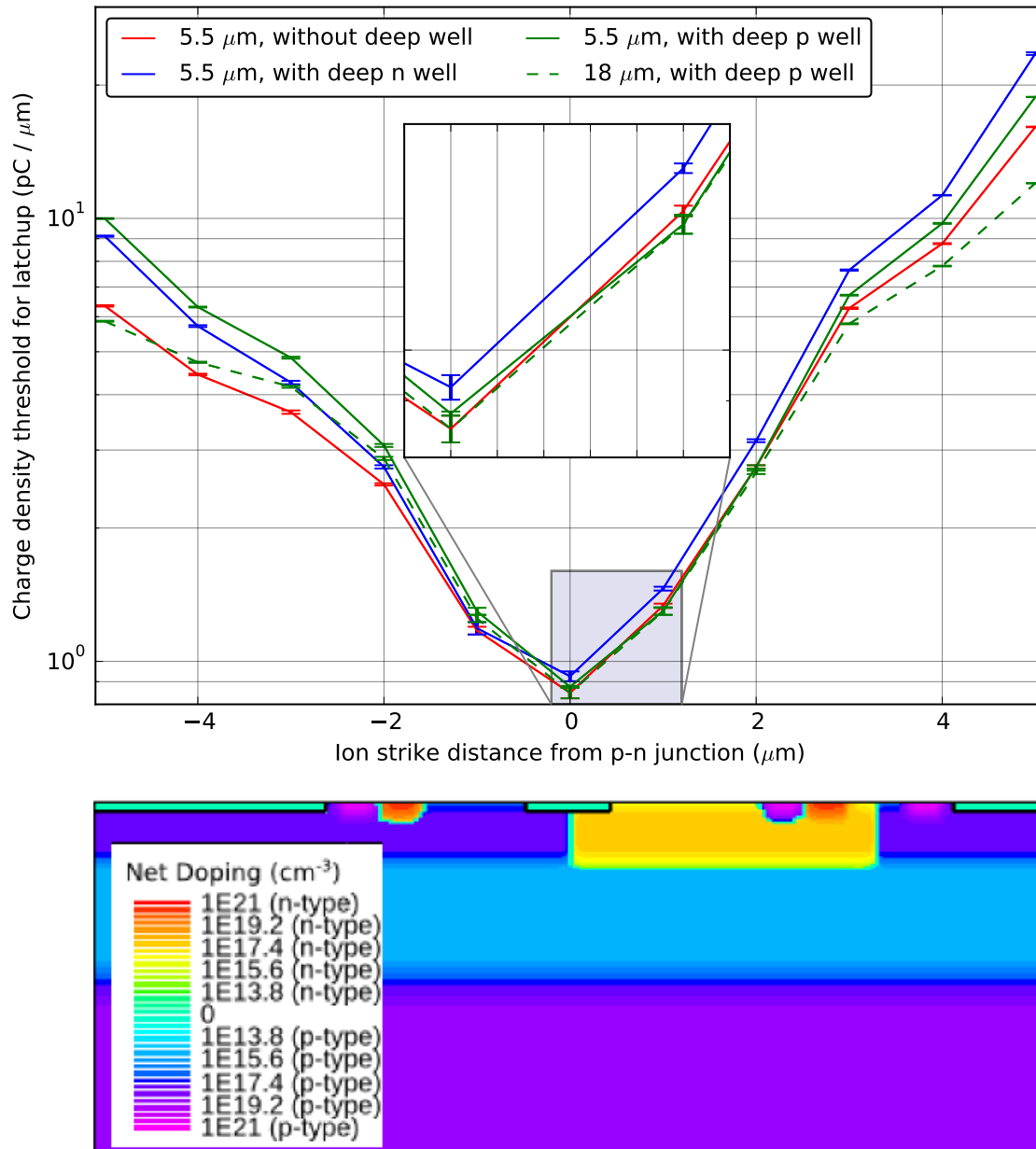


Figure 6.15: Charge density threshold vs. x location of ion strike. The high error bar is the lowest charge density at which latchup occurred. The low error bar is the highest charge density at which latchup did not occur. This 1D model is extrapolated to make the 2D map shown in Figure 6.16. The no deep well structure from Figure 6.6 is shown below for reference.

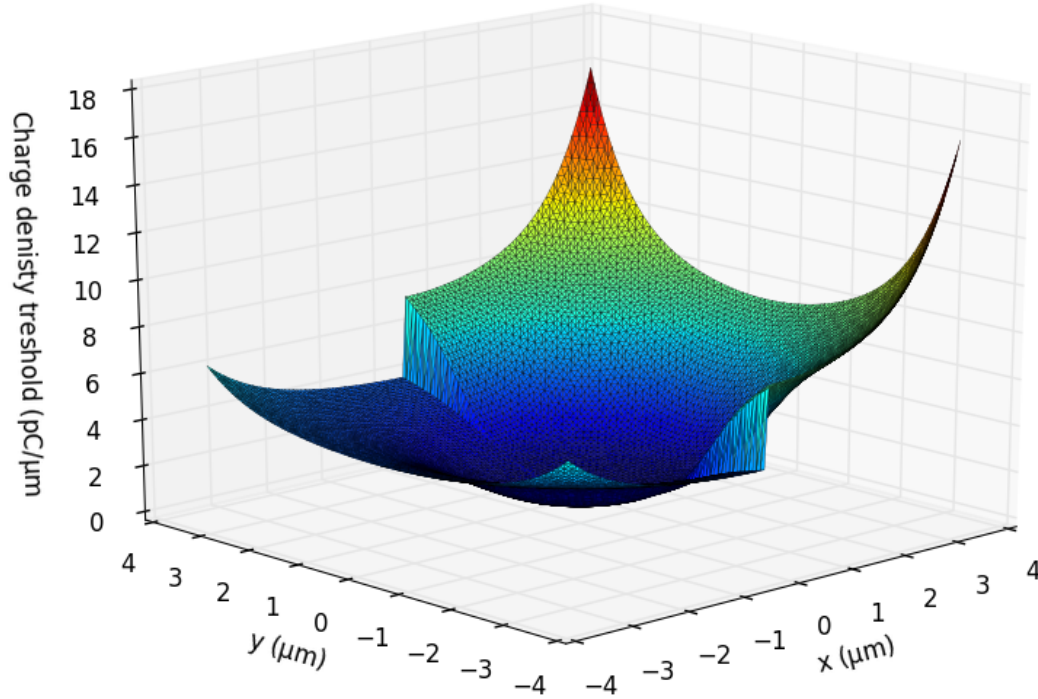


Figure 6.16: Extrapolated 2-D charge density threshold map for the no deep well device.

6.4.1 Heavy ion beam model

Now that the charge density threshold map has been created through simulation, estimates of the charge density distributions for particular experimental particle LETs need to be calculated.

Firstly, there is a variation on the actual energy of particles which make up the beam. The heavy ion energy distributions for the nitrogen, neon and argon ions at the HIF is shown in Figure 6.17. Assuming that the energy variation produces a proportional variation in LET, the standard deviations from Gaussian fits to these energy profiles can be translated into standard deviations of LET.

Next, Fano noise will cause a variation the number of electron-hole pairs produced by

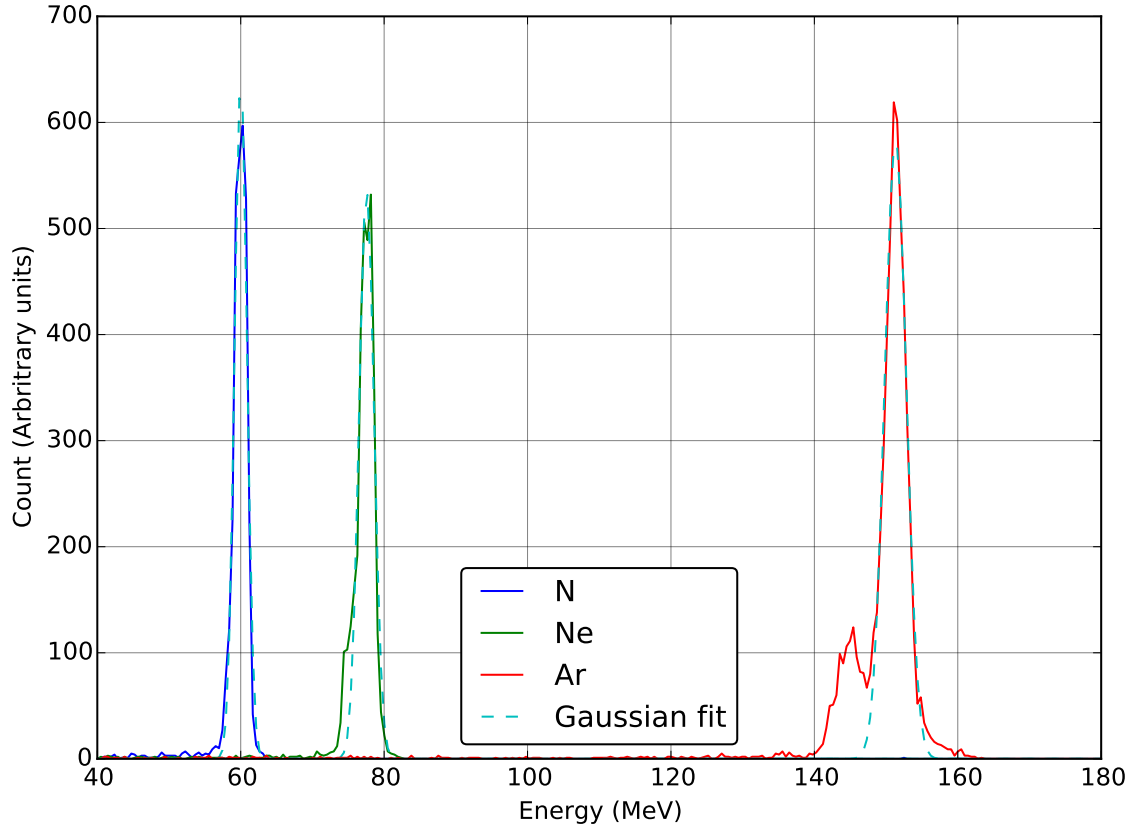


Figure 6.17: Energy distributions for some of the low range "cocktail", ions available at the HIF. A Gaussian fit is shown for each species. The standard deviations resulting from the fits are as follows: nitrogen $\sigma=0.87$ MeV; neon $\sigma=1.05$ MeV; argon $\sigma=1.52$ MeV. There are smaller peaks noticeable at other energies. Nevertheless, these standard deviations can be used as a rough estimate for the standard deviations on LET which, for our model, is assumed to have a Gaussian distribution.

particles imparting the same LET. The Fano factor is defined as

$$F = \frac{\sigma}{\mu} \quad (6.13)$$

where σ is the variance of a random process and μ is the mean value. In silicon, the theoretical Fano factor is 0.115 [105].

The Fano factor accounts for variations in the number of electron-hole pairs created, but not for variations in their spatial distribution (either the location of their creation, or their

momentum at the time of creation). This is important, since latchup sensitive devices are, by definition, not a homogenous medium. Developing a method for estimating these effects with any precision is beyond the scope of this work, and they may turn out to be relatively minor.

These variances will add together to produce an effective variance on the charge density

$$\sigma_p^2 = \sqrt{\sigma_I^2 + \sigma_F^2 + \sigma_V^2} \quad (6.14)$$

where σ_I^2 is the variance on the ion beam energy, σ_F^2 is the variance on the electron hole pair number due to Fano noise, and σ_V^2 is a variance added to model the random spatial distribution and momentum of the charge cloud.

6.4.2 Full device model

In order to calculate cross sections using the charge density threshold maps and the effective charge density variance, the device area and composition must be considered.

In the case of the e2v Sapphire and Ruby sensors (which have identical circuitry but are manufactured using deep wells) the 1.8 V device area is approximately 0.1 cm². The image area is considered immune to latchup, since there are no p-channel MOSFETs, and the 3.3 V circuitry has been shown in Chapter 5 to produce orders of magnitude fewer latchups than the 1.8 V digital circuitry.

For simplicity, it is assumed that the 1.8 V digital circuitry is composed of identical inverter cells of dimensions matching the dimensions of the 2-D charge density threshold map produced.

6.4.3 Full device model outputs

Figure 6.18 shows the cross section as a function of experimental LET as calculated using Equation 6.1. Three curves are plotted, using $\sigma_p=5, 10$ and $20 \text{ MeV cm}^2 \text{ mg}^{-1}$. A curve is plotted for each of the four models representing the processes used to produce the devices analysed experimentally in Chapter 5.

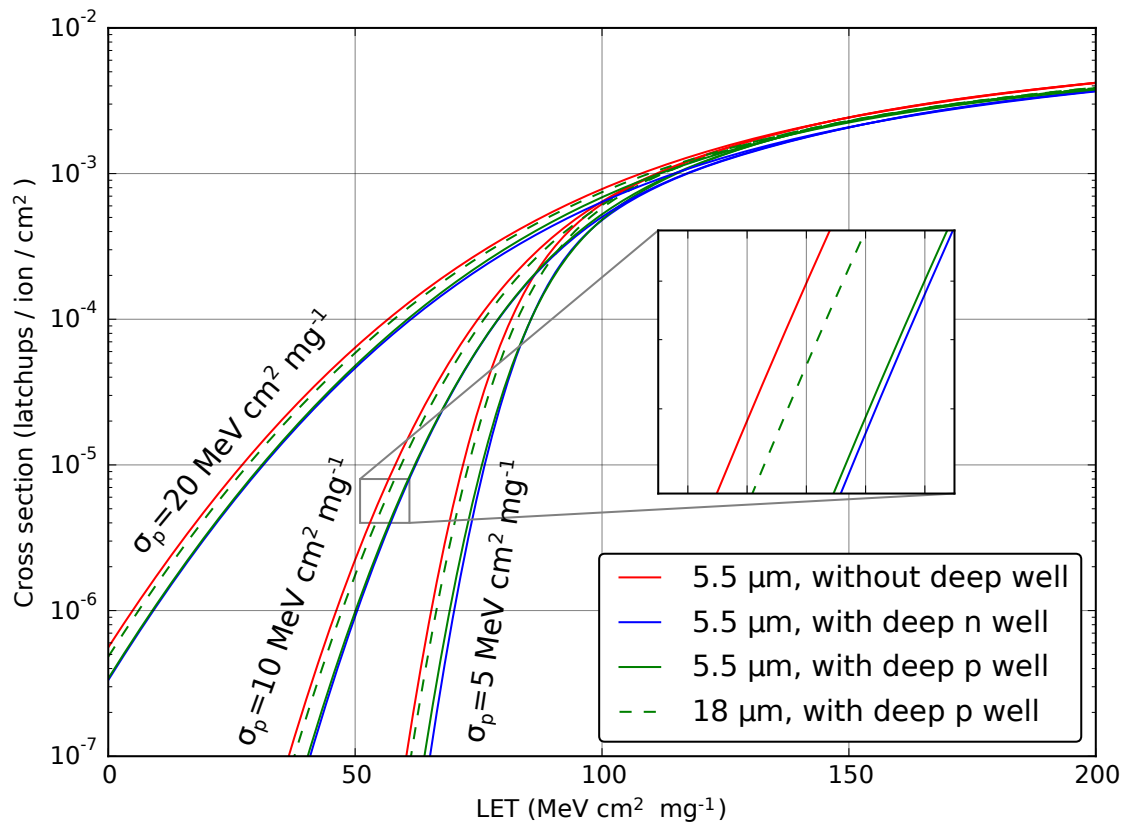


Figure 6.18: Simulated cross section vs. LET. simulations (left to right) using charge density standard deviations of $\sigma_p=20, 10$ and $5 \text{ MeV cm}^2 \text{ mg}^{-1}$.

The SEL threshold LETs increase in the order: standard Sapphire without deep well; $18 \mu\text{m}$ Ruby; $5.5 \mu\text{m}$ Ruby; Sapphire with deep n well. This order is not in agreement with the experimental results from Chapter 5.

The results in general, however, are close to the experimental results. The experimental results placed the LET thresholds of the standard Sapphire, the deep n well Sapphire, and

the 18 μm Ruby close together. (The 5.5 μm Ruby threshold was much higher, but this is being considered an anomaly.)

The saturation cross section calculated by the simulation is approximately equal to the device area. This follows from the fact that a finite charge density threshold was calculated at every device location. Therefore a high enough charge density will trigger latchup at any location. The threshold LET is strongly dependent on the charge density standard deviation σ_ρ . Charge density standard deviations of $\sigma_\rho=20, 10$ and $5 \text{ MeV cm}^2 \text{ mg}^{-1}$ are plotted in Figure 6.18. The curves whose shapes bear most resemblance to the experimental curves are for $\sigma_\rho=5$ and $10 \text{ MeV cm}^2 \text{ mg}^{-1}$. In these cases the threshold LET is approximately double the threshold LET of the experiments. This could be due to a number of factors including the 2-D nature of the model and the device spacing. It is also possible some cells on the real devices latch up at a lower charge density than an inverter.

6.5 Conclusions

This chapter has presented a framework for predicting the SEL cross sections of devices. We have concentrated on heavy ions as the cause of latchup, and simulated simple inverters with the deep well structures and epitaxial thickness variations of the image sensors studied experimentally in Chapter 5. The TCAD models used were relatively simple, using 2-D device simulation of a single circuit. The results have been extrapolated to simulated a device composed entirely of these inverters. Latchup charge density thresholds were extracted from the TCAD model at 1 μm steps. These were combined with estimates for the probabilistic phenomena associated with using a heavy ion beam, and with the variation on the ion interaction within the silicon. Cross section vs. experimental LET was plotted. The results are quantitatively quite close to the actual experimental curves. However, the models failed to predict the relative SEL behaviour of the standard Sapphire, deep n well Sapphire, and 18 μm Ruby.

6.5.1 2-D modelling

TCAD simulation requires significant processing time, and the iterative nature of the latchup charge density threshold search meant running simulations for each device multiple times. The simulation time for each charge density varied from approximately 4 to 6 minutes for the 5.5 μm thick epitaxial layer devices and 6 to 8 minutes for 18 μm thick device. To establish the charge density threshold 18 different charge densities were simulated and the process was repeated for the 11 ion strike locations. 3-D simulations would have required significantly more time (by an order of magnitude or so) to complete. The disadvantage of 2-D is that the inverter (like most circuits) is a 3-D structure, but the 2-D simulation uses parts of the structure along a cut line. Sources were included in the simulation, instead of the drains, which are on another plane. The drains are spaced much closer together than the sources, and this may be significant. A second problem with the 2-D simulation is the way that the 3-D charge cloud is handled. Silvaco Atlas assumes that the 2-D simulation is a 1 μm thick slice of a device, and that the device is formed from a stack of identical slices. In fact, the charge cloud emanates from one slice only, so this approach is not accurate.

An interesting result from Figure 6.15 is that no single device has the highest latchup charge density threshold, ρ_0 , at all locations. The device with the highest charge density threshold varies depending on the ion strike location. This is particularly noticeable for ion strikes in the p well ($x < 0$) compared to strikes in the n well ($x > 0$). This highlights a difficulty in predicting cross sections, namely that the charge density threshold is not simply higher or lower for devices with different structures. To understand the device behaviour properly, charge density threshold data must be collected and analysed for as many potential ion strike locations as possible.

It is plausible that the order of SEL threshold LETs found in Chapter 5 would have been simulated correctly, were enough different circuits modelled in enough detail.

6.5.2 Weibull fits

Weibull fits were used in Chapter 5 to fit the experimental cross section vs. LET data. From these fits the parameters threshold cross section, SEL threshold LET, and a shape parameter can be found. The cumulative Weibull distribution is useful for this purpose, and is commonly used. However, the SEL threshold LET and the shape parameter do not have any physical meaning but are empirical quantities.

In this chapter, we have demonstrated that the cross section vs. LET curves can be approximated using our models. The basis for the model is the charge density threshold map and the random distribution of ion strike location. These alone provide a SEL cross section that increases with LET. On top of these, assumptions about other random processes (such as the ion energy) have been used.

The saturation cross section can be found from our model by simply taking the total area for which a charge density threshold has been calculated. Whatever the value of charge density threshold, this area will latchup if a particle has sufficiently large LET. The threshold LET is no longer a well-defined concept, although it is still useful. Instead, because of the long tails of the distributions for beam energy etc., latchup is possible at all LETs (assuming the charge density threshold is finite somewhere on the device). However, the shape parameter is no longer without a clear physical meaning. The characteristic shape of the cross section vs. LET curve can be explained by the various random processes involved in SEL. In Chapter 5 it was demonstrated that, when using a Weibull fit, the choice of shape parameter has an effect on the value of threshold LET extracted. In this chapter, we have demonstrated that the shape of the cross section vs. LET curve is due to physical processes that can be accounted for. This is useful for two reasons. Firstly, the shape parameter can now be seen as an experimental result, rather than a necessary step when calculating the threshold LET. Secondly, the environment for which SEL testing is performed (i.e. space) is invariably different from the environment in which the testing is performed (e.g. a heavy

ion facility). From our simulations, it is possible to begin to separate those factors affecting SEL which are due to the device itself, and those which are due the experimental setup. After discounting the experimental factors, a more accurate prediction can be made of the performance in an actual space radiation environment.

6.6 Further work

The simulations in this chapter would benefit from being extended to full 3-D device simulations. As mentioned, this would resolve issues around the charge cloud density as approximated in 2-D and would significantly include the accuracy of the simulation by including more of the device geometry. Of particular interest would be to bring the drains into the simulation, as so far only sources have been used which are spaced relatively far from each other.

Another relatively straightforward extension to the simulations would be to include the MOSFET gates, and to run the simulations again for gate voltages of $V_G = V_{DD}$ and $V_G = V_{SS}$.

The simulations in the chapter have been with ion strikes normal to the surface of the sensor. By altering the angle, or even contriving to have the charge cloud covering a short distance in the z direction, it may be possible to more accurately locate the regions of the device structures which are potentially most sensitive to SEL.

Image sensors are complex devices with many different circuits. Performing similar simulations on simpler test devices, i.e. devices with only a single circuit type and comparing them to experiment, would verify the methods used in this chapter.

Chapter 7

Conclusions and further work

The effects of radiation in two CMOS image sensor device families have been investigated. This work has increased the understanding of radiation effects which are relevant when operating image sensors in the space environment.

7.1 Radiation damage in TDI charge-transfer CMOS image sensors

Chapter 4 covered radiation damage effects in a CCD architecture device fabricated on a $0.18\ \mu\text{m}$ CMOS image sensor process. Devices were irradiated with 74 MeV protons up to a 10 MeV equivalent fluence of $1 \times 10^{11}\ \text{cm}^{-2}$. The pre- and post-irradiation CTI and dark current were compared.

The pre-irradiation dark current was high compared to CCDs or to CMOS image sensors using pinned photodiodes. The pre-irradiation dark current compared with a CCD201, for which pre- and post-irradiation data was available was approximately 200 times greater. This is due to the CCD201 being operated in inverted mode. However, the increase in dark current per unit proton fluence is only 1.8 to 3.2 times greater.

CTI was measured by EPER. The pre-irradiation CTI was two orders of magnitude higher than a CCD201 at a similar temperature. The CTI increase was approximately linear with proton fluence. After adjusting for temperature and clock rates it was shown with modelling of electron trap behaviour that the CTI behaviour post-irradiation could be explained and accurately predicted by introduction of the E-centre and divacancy during irradiation.

7.2 Experimental study of single event effects in CMOS active pixel sensors

Chapter 5 detailed the results of an experimental campaign to measure the occurrence of single event effects in CMOS APS sensors. Heavy ions were used to produce a range of LETs from 10.0 to 125.0 MeV cm² mg⁻¹. The main single event of interest was latchup. The latchup cross section was recorded as well as single event upsets measured in selected memory registers and the communications interface.

Four device variants were evaluated. One of the devices contained a deep n well and two contained deep p wells in two thicknesses of epitaxial silicon. An anomalous result was recorded for the deep p well 5.5 μm epitaxial layer device. The other three devices, which included a device without any deep well, showed similar latchup cross sections at the LETs of interest. The deep p well device with thicker (18 μm) epitaxial layer showed a slightly higher LET threshold. It was shown that extracting the usual figures of merit, namely threshold LET and saturation cross section, from the data could not be performed without making some assumptions about the causes of the different cross section curve shapes. Some of the factors leading to the characteristic curve shapes were investigated in simulations in Chapter 6. The single event upsets were too infrequent to determine any causality between the different device layers and the likelihood of single event upsets.

Further work in this area should include a further investigation of the single event latchup

behaviour of the four device variants. Using more examples of each device variant would determine whether the threshold LET variation results are repeatable and are in fact due to the deep well structures.

7.3 SEL simulation

In Chapter 6 a method was described for using TCAD simulations to predict the SEL behaviour of an inverter circuit. Four inverter circuits were simulated to match the four device structures used in the experiment of Chapter 5. The charge density required to produce a latchup was calculated at 1 μm steps along the 2D structure and this was extrapolated to make a map of charge density threshold. Estimates were made for the distribution of charge densities produced by real heavy ion strikes. These estimates of charge density distributions were then combined with the map to predict the SEL cross section as a function of LET. The model successfully produced cross section curves with the correct characteristic shapes. Although the model was relatively simple the threshold LET and saturation cross section were accurate to within an order of magnitude. The model did not show the different device variants to have a large range of threshold LETs.

An interesting result from the charge density threshold maps was that different areas of the device variants had different susceptibility to latchup. For example, some areas of the deep n well device had a higher charge density threshold than the same area of the deep p well device, whereas other areas had a lower threshold. Clearly the more detailed the device model the better the SEL behaviour can be predicted. Useful further work would be to extend these simulations to 3D and to experiment with different device geometries.

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Appendix A

Silvaco Atlas model printout

1

2 CONSTANTS:

3 Boltzmann's constant = 1.38066e-23 J/K

4 Elementary charge = 1.60219e-19 C

5 Permittivity in vacuum = 8.85419e-14 F/cm

6 Temperature = 300 K

7 Thermal voltage = 0.025852 V

8

9 REGIONAL MATERIAL PARAMETERS:

10 Region : 1 2 3 4 5 6 7 8 9

11 Material : Silicon SiO2 SiO2 SiO2 Conductor Conductor Conductor Conductor Conductor

12 Type : semicond. insulator insulator insulator metal metal metal metal metal

13

14 Average Composition Fraction

15 X-composition: 0 0 0 0 0 0 0 0 0

16 Y-composition: 0 0 0 0 0 0 0 0 0

17

18 Band Parameters

```
19  Epsilon : 11.8 3.9 3.9 3.9
20  Eg (eV) : 1.08
21  Chi (eV) : 4.17
22  Nc (per cc) : 2.8e+19
23  Nv (per cc) : 1.04e+19
24  ni (per cc) : 1.45e+10
25
26  Bandgap narrowing parameters
27  bgn.e (eV) : 0.009
28  bgn.n (/cc) : 1e+17
29  bgn.c : 0.5
30  ubgn.b : 3.1e+12
31  ubgn.c : 3.9e-05
32  bgn.shnk.me : 0.321
33  bgn.shnk.mh : 0.346
34  bgn.shnk.eps : 11.7
35  bgn.shnk.ge : 12
36  bgn.shnk.gh : 4
37
38  Effective Richardson Constants
39  An** : 110
40  Ap** : 30
41
42  Incomplete Ionization Parameters
43  Gc : 2
44  Gv : 4
45  Ed (eV) : 0.044
46  Ea (eV) : 0.045
```

47

48 Recombination Parameters

49 taun0 : 1e-07

50 taup0 : 1e-07

51 etrap : 0

52 nsrhn : 5e+16

53 nsrhp : 5e+16

54 ksrhtn : 0.0025

55 ksrhtp : 0.0025

56 ksrhcn : 3e-13

57 ksrhcp : 1.18e-12

58 ksrhgn : 1.77

59 ksrhgp : 0.57

60 nsrhn : 5e+16

61 nsrhp : 5e+16

62 augn : 2.8e-31

63 augp : 9.9e-32

64 augkn : 0

65 augkp : 0

66 kaugcn : 1.83e-31

67 kaugcp : 2.78e-31

68 kaugdn : 1.18

69 kaugdp : 0.72

70 aug.cn1 : 2.2e-31

71 aug.cpl : 9.2e-32

72 aug.chi : 1.66e-30

73 hns.ae : 6.7e-32

74 hns.ah : 7.2e-32


```
75  hns.be : 2.45e-31
76  hns.bh : 4.5e-33
77  hns.ce : -2.2e-32
78  hns.ch : 2.63e-32
79  hns.he : 3.47
80  hns.hh : 8.26
81  hns.n0e : 1e+18
82  hns.p0e : 1e+18
83  copt : 0
84
85  Impact Ionization Model Parameters (Selberherr model)
86  an1 : 7.03e+05
87  an2 : 7.03e+05
88  ap1 : 6.71e+05
89  ap2 : 1.58e+06
90  bn1 : 1.23e+06
91  bn2 : 1.23e+06
92  bp1 : 1.69e+06
93  bp2 : 2.04e+06
94  betan : 1
95  betap : 1
96  egran : 4e+05
97
98  Band-to-band tunneling Parameters
99  mass.tunnel : 0.25
100 me.tunnel : 0.322
101 mh.tunnel : 0.549
102
```

103 Thermal Velocities

104 vn (cm/s) : 1.08e+07

105 vp (cm/s) : 1.3e+07

106

107 Saturation Velocities

108 vsatn (cm/s) : 1.03e+07

109 vsatp (cm/s) : 1.03e+07

110

111 REGIONAL MODEL FLAGS:

112 Region: 1 2 3 4 5 6 7 8 9

113 SRH T

114 consrh F

115 klasrh F

116 Auger T

117 klaaug F

118 picaug F

119 hnsaug F

120 auggen F

121 optr F

122 bgn(std/kla) T

123 ubgn F

124 bgn.alamo F

125 bgn.bennett F

126 bgn.schenk F

127 incomplete F

128 bbt F

129 bbt F

130 bbtauto F

```
131  bbthurkx F
132  bbt Kane F
133  bbtschenk F
134  bbt nonlocal F
135  tat(local) F
136  tat nonlocal F
137  tat(coulombic) F
138  impact T
139  Boltzmann F
140  Fermi-Dirac T
141
142  Gain and Rsp scaling
143      Gain scale factor : 1 1 1 1
144      Rsp scale factor : 1 1 1 1
145
146
147  REGIONAL MOBILITY MODEL SUMMARY:
148
149      Region #1:
150
151      Model for Electrons:
152
153          Concentration Dependent Mobility
154          @ Temperature = 300 Kelvin
155          Using CVT low field mobility model.
156              cs = 3.43e+20
157              cr = 9.68e+16
158              alpha = 0.68
```

```
159         beta = 2
160         gamma = 2.5
161         pc = 0
162         mu0 = 52.2
163         mu1 = 43.4
164         mumax = 1417
165
166     Parallel Field Dependent Mobility
167     Using parallel field model.
168     Using built-in Silicon model for Vsat.
169     alpha = 2.4e+07
170     theta = 0.8
171     tnom = 600
172     beta = 2
173
174     Perpendicular Field Dependent Mobility
175     Using CVT model.
176     B = 4.75e+07
177     C = 174000
178     D = 0.333333
179     E = 1
180     tau = 0.125
181     delta = 5.82e+14
182     k = 2
183
184     Model for Holes:
185
186     Concentration Dependent Mobility
```

```
187      @ Temperature = 300 Kelvin
188      Using CVT low field mobility model.
189      cs = 6.1e+20
190      cr = 2.23e+17
191      alpha = 0.71
192      beta = 2
193      gamma = 2.2
194      pc = 9.23e+16
195      mu0 = 44.9
196      mu1 = 29
197      mumax = 470.5
198
199      Parallel Field Dependent Mobility
200      Using parallel field model.
201      Using built-in Silicon model for Vsat.
202      alpha = 2.4e+07
203      theta = 0.8
204      tnom = 600
205      beta = 1
206
207      Perpendicular Field Dependent Mobility
208      Using CVT model.
209      B = 9.925e+06
210      C = 884200
211      D = 0.333333
212      E = 1
213      tau = 0.0317
214      delta = 2.0546e+14
```

```
215         k = 2
216
217
218 Contacts:
219 Name Num Work fn Resist. Capacit. Induct.
220         (eV) (Ohms) (Farads) (Henries)
221 vssbody 1 0.000 0.000E+00 0.000E+00 0.000E+00
222 vssbodydum 2 0.000 0.000E+00 0.000E+00 0.000E+00
223 vss 3 0.000 0.000E+00 0.000E+00 0.000E+00
224 vddbody 4 0.000 0.000E+00 0.000E+00 0.000E+00
225 vdd 5 0.000 0.000E+00 0.000E+00 0.000E+00
226
227
228 Single Event Upset / Photogeneration initialization
229
230 SEU track #1 parameters:
231
232 Temporal distribution: Gaussian function.
233 Peak time (s) = 4e-12
234 Gaussian width (s) = 7e-14
235 Radial distribution: exponential.
236 Entry point in microns (x,y,z) = (5, 0, 0)
237 Exit point in microns (x,y,z) = (5, 120.5, 0)
238 Track radius = 0.05 microns
239 Track length = 120.5 microns
240 Charge discretisation error = 0.000156314
```
