High Efficiency Class E Microwave Frequency Multipliers

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The candidate confirms that the work submitted is her own and that appropriate credit has been given where reference has been made to the work of others.

Abstract

A novel design methodology for the successful implementation of high efficiency class E frequency multipliers is presented in this work. An innovative class E configuration is proposed for a frequency tripler that provides an advantage over the conventional designs, by allowing a 50 % duty cycle drive with a realisable load for 100 % DC-to-RF efficiency operation.

A novel quantitative analysis of class E networks is developed that aids in the rapid yet accurate assessment of circuit performance. The first-order analysis provides an intuitive evaluation of class E operation and harmonic content of the switch waveforms. The analysis is shown to be applicable to both class E amplifiers and multipliers, providing closed-form equations for an intelligent first design. The proposed class E tripler configuration is evaluated using this technique and is shown to be a practically viable solution for achieving high DC-to-RF efficiency.

Techniques involved in the design and implementation of the novel frequency tripler are investigated, and three microstrip circuits are presented that provide high drain efficiency, high unwanted harmonic rejection and low DC power consumption. Innovative design of the input matching circuit that exploits the nonlinear input capacitance of the device, and the output matching circuit that simultaneously provides appropriate harmonic terminations and unwanted harmonic rejection, ensure a simultaneously high achievable conversion gain and DC-to-RF efficiency. Practical demonstration of the three novel circuits display the highest reported DC-to-RF efficiency and conversion gain for microwave frequency triplers to date. Trade-offs between circuit complexity, size and simultaneously achievable high efficiency and high conversion gain are identified and elucidated with the three novel designs.

Contents

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List of Principal Symbols

C	Capacitance
C_p	Output power capability
C_{ds}	Drain source capacitance
C_{gd}	Gate drain capacitance
C_{gs}	Gate source capacitance
f_0	Fundamental frequency
f_{IF}	Intermediate frequency
f_{LO}	Local oscillator frequency
f_{max}	Maximum frequency for ideal class E behaviour
f_t	Cut-off frequency
f_{ct}	Cut-off frequency for a transmission line
f_{RF}	RF frequency
g_d	Output conductance
g_m	Transconductance
h	Height of substrate
I_{DC}	DC current
I_{ds}	Drain source current
I_d	Drain current
I_0	Output current
I_1	Current through the fundamental resonator
I_c	Current through the capacitor
L	Inductance
L_d	Drain inductance
L_g	Gate inductance

L_s	Source inductance
N	Multiplication factor
P_{DC}	DC power consumed
P_{in}	Input Power
P_{out}	Output Power
R_d	Drain resistance
R_g	Gate resistance
R_s	Source resistance
T	Time period
V_{DD}	DC Drain supply voltage
V_{DS}	DC drain source voltage
V_{GG}	DC Gate supply voltage
V_d	Drain voltage
V_{ds}	Drain source voltage
V_g	Gate voltage
V_p	Pinch-off voltage
w	Width of transmission line
Z_0	Characteristic impedance
Z_L	Load impedance
Z_{in}	Input impedance
Γ_L	Load reflection coefficient
Γ_S	Source reflection coefficient
$\eta_{DC/RF}$	DC-to-RF efficiency
$\eta_{overall}$	Overall efficiency
ϵ_{eff}	Effective permittivity
ϵ_0	Free space permittivity
ϵ_r	Relative permittivity
$\Delta\phi$	Phase shift
λ	Wavelength
λ_0	Wavelength in free-space
λ_g	Guided wavelength
θ	Electrical length

θ_c	Conduction angle
ω	Angular frequency

List of Principal Abbreviations

2DEG	Two Dimensional Electron Gas
ADS	Advanced Design System
AlGaAs	Aluminium Gallium Arsenide
BPF	Band Pass Filter
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CPFSK	Continuous Phase Frequency Shift Keying
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
HPF	High Pass Filter
HPBW	Half Power Beam Width
IEEE	Institute of Electronic and Electrical Engineers
IF	Intermediate Frequency
InGaAs	Indium Gallium Arsenide
LO	Local Oscillator
LPF	Low Pass Filter
MESFET	Metal Semiconductor Field Effect Transistor
MIC	Monolithic Integrated Circuit
MMIC	Monolithic Microwave Integrated Circuit

PAE	Power Added Efficiency
pHEMT	Pseudomorphic High Electron Mobility Transistor
PLL	Phase Locked Loop
RF	Radio Frequency
RFC	Radio Frequency Choke
RFID	Radio Frequency Identification
S	Scattering Parameter
SMA	Sub Miniature Adaptor
SRD	Step Recovery Diode
TEM	Transverse Electro-Magnetic
TOM	Triquint's Own Model
VCO	Voltage Controlled Oscillator
WLAN	Wireless Local Area Network

Chapter 1

Introduction

Wireless communication systems have seen phenomenal and unprecedented growth in the last two decades. Mobile wireless systems such as cellular telephony, wireless remote sensing, radio frequency identification (RFID) and global positioning systems (GPS) have seen increased interest and research in recent years. Mobile and satellite communications in particular have become an integral part of daily life, with the number of mobile subscribers outstripping that predicted a decade ago, and increasingly higher demands being placed on satellite-based video, telephone and data communication systems. Newer generation satellite systems have undergone an increase in frequency of operation from C-band to X-band in order to provide higher data rates and more facilities, with current trends extending this further into the Ka-band.

One of the most critical design aspects of mobile wireless systems is to facilitate efficient use of valuable electrical power resources by minimising power wasted as heat. This is driven by the need to lower the cost of system operation and services, whilst providing reliable service and maintaining excellent quality. Effective thermal waste management in power-critical systems reduces the amount of heat generated from inefficient power usage, and not only conserves valuable battery or solar cell power, but also prevents thermal degradation of electronic devices [1].

Whilst power amplifiers have seen consistent and detailed investigation into optimum design and high efficiency techniques, frequency multipliers have been relatively overlooked both in terms of optimum design procedures and high efficiency consideration. Higher order multipliers in particular have been neglected in favour of doublers due to arduous design, higher circuit complexity, and lower achievable gain and efficiency.

Load-pull techniques to overcome these obstacles remain dependent on trial-and-error iterations and lack a definite mathematical treatment.

This work presents a detailed design methodology for a novel configuration of high efficiency Class E frequency multiplier. A novel mathematical analysis of Class E networks is presented, and a definitive approach to the design of high efficiency higher order multipliers is provided. It is backed up by nonlinear simulations of the novel high efficiency multiplier and is demonstrated with the successful design and implementation of high efficiency triplers.

1.1 Frequency Multiplier Applications

The most common use of frequency multipliers is as part of signal generating circuitry in electronic systems. This involves the implementation of frequency multipliers to extend the frequency range of low-frequency oscillators. In communications systems, the local oscillator (LO) signal in a transceiver is required for purposes of up/down conversion. A vital factor in obtaining a high performance communication link is the availability of a LO signal that is free from spurious frequencies. It becomes, however, increasingly difficult to meet the stringent phase noise specifications and stability at higher frequencies with a fundamental oscillator. A common and preferred solution is to generate a low-frequency (typically below 2 GHz), low-phase noise signal from a high Q fundamental oscillator, and multiply the frequency up to the required level by a superseding frequency multiplier, or frequency multiplier chain as shown in Figure 1.1. This technique is also used for LO generation for mixers within test instruments or frequency synthesisers [2]. The output power level of the LO signal required for the mixer ranges from approximately 0 dBm for active mixers, to +17 dBm for passive mixers [3].

Frequency multipliers also find application in dual-conversion transmitters [4, 5], where up-conversion is performed in two stages instead of one, to obtain a higher intermediate frequency (IF) thus easing the design of highly-selective filters and avoiding excessive LO leakage at the output [5]. Using a frequency multiplier to provide a coherent LO signal for the second stage of up-conversion enables a reduction in components as only a single oscillator is needed, as shown in Figure 1.2. Frequency multipliers also find

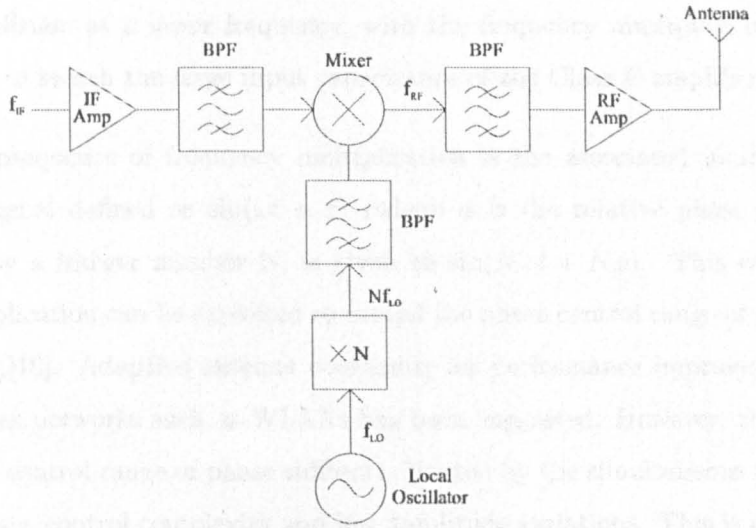


Figure 1.1: Basic transmitter architecture.

application in both transmitter and receiver sections of transceivers suitable for WLAN IEEE 802.11b standard [6] and wireless transceivers for CDMA [7].

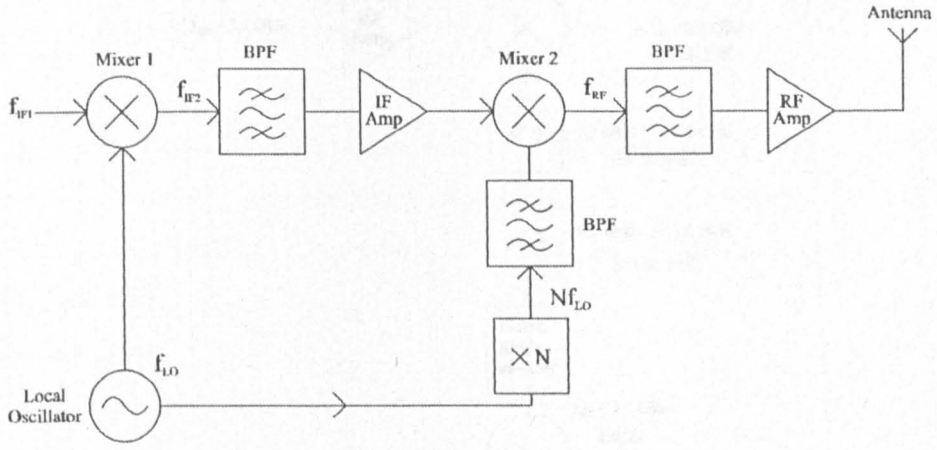


Figure 1.2: Dual-conversion transmitter architecture [5].

Frequency multipliers can be used not only to mitigate the design of high-frequency oscillators but also the design of driver circuits at high frequencies in transmitters [2]. It has been shown that the drive of a Class E amplifier can be miniaturised and made more efficient by replacing the sole CMOS driver circuit operating at high frequencies, with a driver stage consisting of a CMOS driver operating at low frequencies followed by a frequency multiplier [8]. The output of the CMOS driver is relaxed to a lower

current amplitude at a lower frequency, with the frequency multiplier providing the gain needed to switch the large input capacitance of the Class E amplifier.

A useful consequence of frequency multiplication is the associated multiplication in phase. A signal defined as $\sin(\omega t + \phi)$ (where ϕ is the relative phase shift), when multiplied by a integer number N, is given as $\sin(N\omega t + N\phi)$. This corresponding phase multiplication can be exploited to extend the phase control range of phased array antennas [9],[10]. Adaptive antenna combining for performance improvement of high speed wireless networks such as WLANs has been suggested. However, the achievable linear phase control range of phase shifters is limited by the simultaneous requirements of low loss, low control complexity and low amplitude variations. This is circumvented by providing a fractional phase shift range (eg. 0° to 90°) from a phase shifter that satisfies the above requirements, and then providing the full 0° to 360° phase shift through subsequent phase multiplication via two cascaded doublers as shown in Figure 1.3.

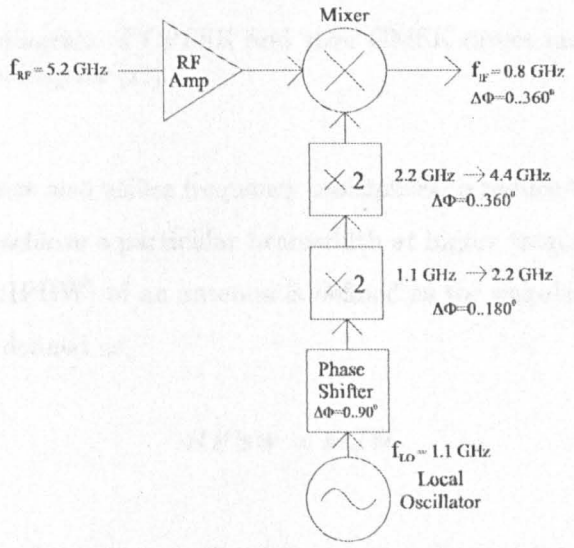


Figure 1.3: Full 360° phase control for each element of a phased array antenna [9].

The technique of extending the range of phase shifters is also implemented in Continuous Phase Frequency Shift Keying (CPFSK) modulators to combine modulation techniques and frequency translation [11]. Here, a phase shifter of range 0 to $2\pi/N$ radians is fed by a stable reference signal of frequency $1/N$ of the eventual carrier frequency. The phase of this signal is continuously modulated over a phase range of $\pm\pi/N$ radians by

a baseband modulation generator. This modulated CPFSK signal is then multiplied up to the required carrier frequency by an N^{th}-order frequency multiplier to provide the full $\pm\pi$ radian range, as shown in Figure 1.4. This signal can then be fed to a PLL incorporating a Gaussian filter to provide a GMSK (Gaussian Minimum-Shift Keying) signal via a VCO.

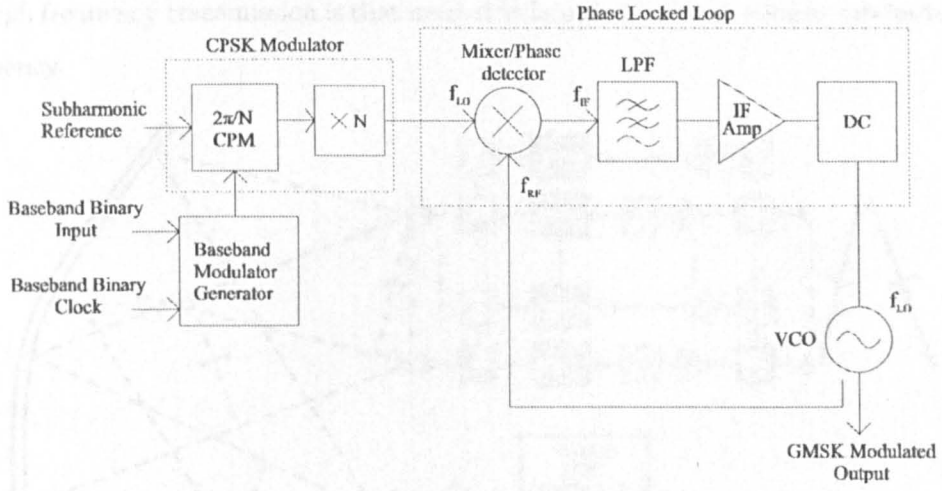


Figure 1.4: Block diagram of CPFSK and then GMSK direct modulator with incorporated frequency multiplier [11].

Phased array antennas also utilise frequency multipliers to reduce the required number of phase shifters to achieve a particular beamwidth at higher frequencies [12]. The half power beamwidth (HPBW) of an antenna is defined as the angular width of the beam at half power. It is defined as,

$$HPBW = k\lambda/D,$$

where is k is a factor dependent on the shape of the reflector, D is the diameter of the circular antenna and λ is the wavelength. Therefore, HPBW is inversely proportional to frequency, resulting in narrower beamwidths at higher frequencies of transmission. This necessitates a larger number of elements, and hence phase shifters, in order to achieve the desired field of view. This limitation can be overcome if the process of generating the required beamwidth is separated from the process of generating the required higher frequency of transmission, which can be achieved with the set up shown in Figure 1.5. An initial wavefront is produced by the first array at a lower frequency that is a sub-

multiple of the frequency ultimately to be transmitted. The wavefront is intercepted by a reflector and a second array placed at the image plane receives the wavefront and multiplies up the frequency and the phase shifts by an integer number. The resultant signal is then radiated out via a third array and the resultant wavefront is in the same direction as that of the original wavefront. Hence, the number of phase shifters required for high frequency transmission is that needed to launch a beam at a lower sub-harmonic frequency.

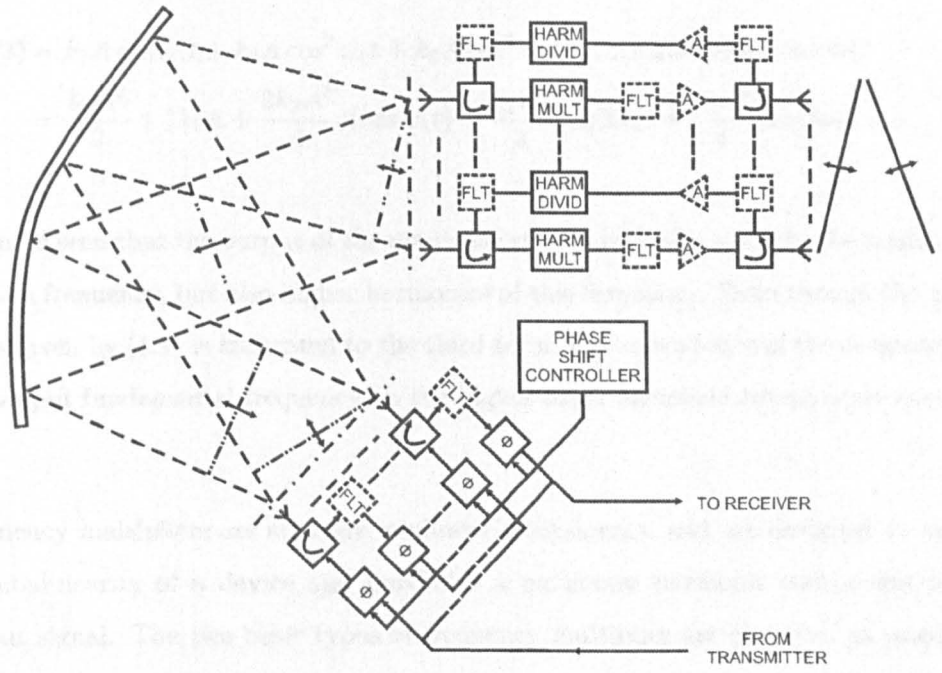


Figure 1.5: Schematic representation of a phased array antenna using frequency multipliers for reduced number of phase shifters [12].

1.2 Principles of Frequency Multiplication

Harmonic generation in a nonlinear component can be expressed in a simple fashion for a memoryless weakly-nonlinear system. The output voltage $v_o(t)$ can be expressed as a power series of the input voltage $v_i(t)$,

$$v_o(t) = k_1 v_i(t) + k_2 {v_i}^2(t) + k_3 {v_i}^3(t) + k_n {v_i}^n(t).... \tag{1.1}$$

If the input is a single-tone signal given by,

$$v_i(t) = A\cos\omega_1 t, \tag{1.2}$$

then the output signal is derived by substituting (1.2) into (1.1),

$$v_o(t) = k_1 A\cos\omega_1 t + k_2 A\cos^2\omega_1 t + k_3 A\cos^3\omega_1 t + ...(\text{higher order terms}) \tag{1.3}$$

$$= \frac{k_2 A^2}{2} + (k_1 A + \frac{3k_3 A^3}{4})(\cos\omega_1 t) + \frac{k_2 A^2}{2}\cos 2\omega_1 t + \frac{k_3 A^3}{4}\cos 3\omega_1 t + ... \tag{1.4}$$

It can be seen that the output of the nonlinear system contains not only the original excitation frequency, but also higher harmonics of this frequency. Even though the power series given by (1.1) is truncated to the third term, the dependence of the magnitude of the output fundamental frequency on the higher order harmonic components is clearly seen.

Frequency multipliers are strongly nonlinear components, and are designed to exploit the nonlinearity of a device and maximise a particular harmonic component in the output signal. The two basic types of frequency multiplier are classified as passive or active.

1.2.1 Passive Frequency Multipliers

Passive frequency multipliers employ diodes as the nonlinear device, and are classified according to the particular nonlinear mechanism of the diode that is utilised. A generic configuration of a diode frequency multiplier is shown in Figure 1.6.

Resistive multipliers exploit the nonlinear I/V characteristics of a Schottky barrier diode in order to produce distortion of the input signal through rectification, and hence generate harmonics [13]. Resistive multipliers are inherently broadband in nature, however they are inefficient and lossy, restricted to providing conversion losses of no better than $1/N^2$, where N is the multiplication factor.

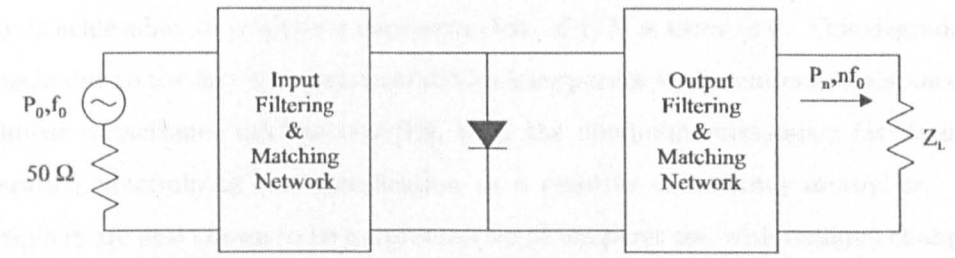


Figure 1.6: Generic diode frequency multiplier circuit configuration.

Alternatively, varactor multipliers employ a nonlinear reactance in the form of the reverse-biased junction capacitance of a Schottky or pn junction diode as the principle mechanism for generating harmonics [14]. They are capable of low conversion loss for low multiplication orders, and can operate at frequencies into the mm-wave region. However, the nonlinearity is not strong, which makes it difficult to achieve acceptable conversion loss for higher order multipliers due to the large input drive level that is required. A frequency quadrupler presented by Johnson [15] at an output frequency of 9 GHz, required an input power level of 1 W at 10 % duty cycle for a conversion loss of 5.3 dB. These types of multipliers also suffer from extreme circuit sensitivity and stability issues.

A stronger nonlinearity is achieved by exploiting the diffusion charge storage of a pn junction. Step Recovery Diodes (SRDs) can be viewed as charge-controlled switches where, under forward bias conditions, charge is inserted into the diode causing it to appear as a low impedance; if the bias is then reversed the charge is removed from the diode in a time t_s, after which the diode rapidly appears as a high impedance [16]. This generates extremely fast rise time pulses that are rich in harmonics, and the required harmonic is filtered out using a resonant output network. This type of multiplier is suitable for achieving higher order multiplication at frequencies reaching tens of gigahertz. SRD multipliers, however, are also very sensitive to circuit parameters and are prone to instabilities. They are also reported to be difficult to analyse using CAD [17]. The strong nonlinearity of the diode, large number of harmonics and stability issues makes convergence of a harmonic balance analysis quite difficult to achieve.

Diode-based frequency multipliers typically provide conversion loss due to the passive nature of diodes. Signal gain is not obtainable, and though in theory a maximum gain of

unity is achievable, in practice a conversion loss of $1/N$ is usual [14]. This degradation in loss is due to the fact that practical diodes incorporate both nonlinear resistance and nonlinear capacitance mechanisms [18], with the dominant mechanism for harmonic generation determining the classification as a resistive or varactor multiplier. Such multipliers are also known to be quite sensitive to temperature, with nominal changes in temperature capable of inducing a significant output power variation and even parasitic oscillation. The two terminal nature of diodes provides little input/output isolation, and these multipliers typically require large input drive levels ($\approx 100mW$ or more) making them unsuitable for power critical systems.

1.2.2 Active Frequency Multipliers

Unlike passive multipliers, active multipliers provide the possibility of conversion gain. FET devices are commonly used as the nonlinear device, and offer the advantage of possible integration into a single technology if monolithic implementation is required. A large signal equivalent circuit of a FET is shown in Figure 1.7. The nonlinear mechanisms that can be utilised for harmonic generation are the nonlinear input gate-source capacitor, C_{gs}, the nonlinear transconductance, g_m, the nonlinear output conductance, g_d, and the intentional clipping of the output drain-source current due to pinch-off and/or gate junction forward conduction. FET multipliers require much lower input drive levels compared to diode based multipliers, are less sensitive to temperature variation and are capable of wideband operation.

A generic configuration of a FET frequency multiplier is shown in Figure 1.8. The FET device is frequently a MESFET, HEMT or pHEMT device with a cut-off frequency f_t, higher than that of the required harmonic. The input matching network presents harmonic terminations $\Gamma_S(f_0, 2f_0, ..)$, to typically present an optimum fundamental impedance which ensures maximum power transfer from the source to the input of the device and also provides appropriate termination to the remaining harmonics. The output matching network presents harmonic terminations $\Gamma_L(f_0, 2f_0, ..)$ to transform the 50 Ω load to the optimum impedance at the required harmonic and unwanted harmonics, in order to maximise the power of the former and provide suppression of the latter. The gate and drain of the device are typically biased through an RF choke

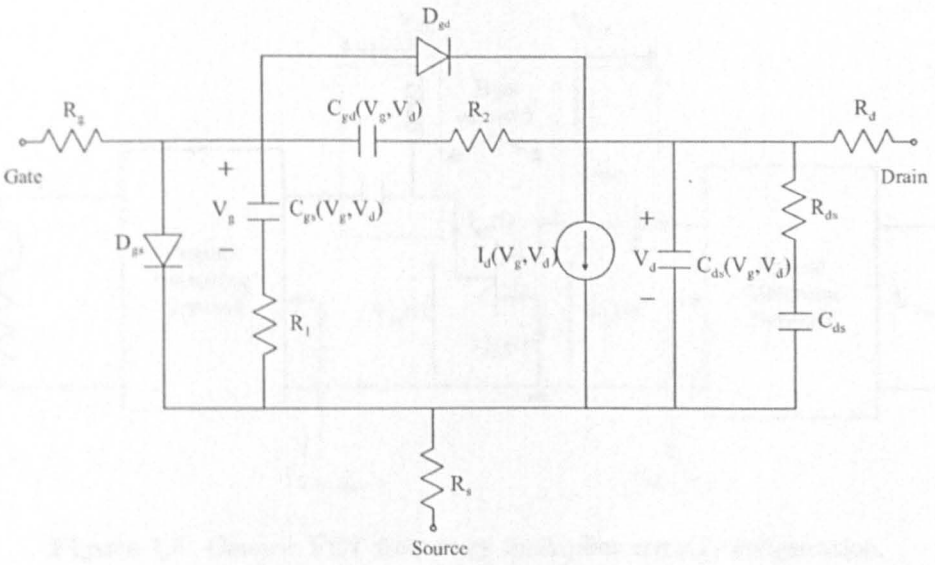


Figure 1.7: Large signal equivalent circuit of a MESFET [1].

and DC blocking capacitor. The bias levels coupled with the input and output matching networks are designed to maximise the power of the required harmonic at the 50 Ω load. The harmonic content of the drain voltage and drain current are related to the bias supply as follows,

$$V_{ds}(t) = V_{DD} + \sum_{n=1}^{n=\infty} V_n \cos(n\omega t + \phi_n) \tag{1.5}$$

$$I_{ds}(t) = I_{DC} + \sum_{n=1}^{n=\infty} I_n \cos(n\omega t + \epsilon_n) \tag{1.6}$$

1.2.2.1 Frequency multiplier terms and quantities

The important performance parameters for a frequency multiplier are its output power, gain, DC-to-RF efficiency, power added efficiency and harmonic rejection. Referring to Figure 1.8, the output power at the required harmonic, N, is given by,

$$P_{out}(Nf_0) = \frac{1}{2} Real(V_{load,N} \cdot I^*_{load,N}). \tag{1.7}$$

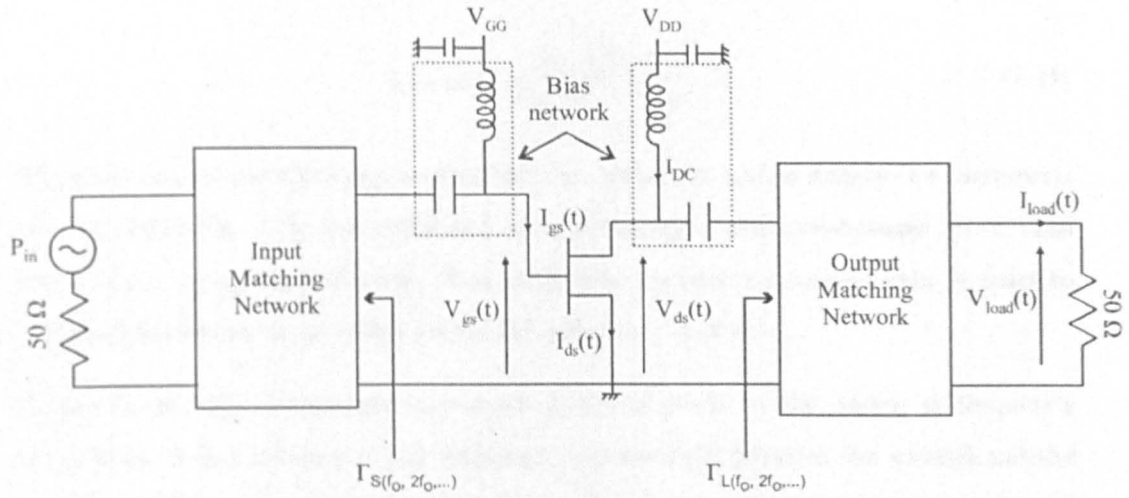


Figure 1.8: Generic FET frequency multiplier circuit configuration.

The conversion gain is defined by the ratio of output power at the required harmonic and the available input power at the fundamental frequency, and is given by,

$$Gain = \frac{P_{out}(Nf_0)}{P_{in}(f_0)}. \tag{1.8}$$

The DC-to-RF efficiency is a measure of the amount of DC power that is converted to RF power at the desired frequency, and is defined as the ratio of output power at the required harmonic and the DC power consumption as given by,

$$\eta_{DC/RF} = \frac{P_{out}(Nf_0)}{P_{DC}}. \tag{1.9}$$

Power-added-efficiency (PAE) is the ratio of the difference in output and input RF power to the total DC power consumption, and is given as,

$$PAE = \frac{P_{out}(Nf_0) - P_{in}(f_0)}{P_{DC}} \tag{1.10}$$

Another useful measure is the overall efficiency, which incorporates the total amount of power injected into the circuit and the amount of output power obtained at the required harmonic, and is given by,

$$\eta_{overall} = \frac{P_{out}(Nf_0)}{P_{in}(f_0) + P_{DC}}. \tag{1.11}$$

The term conversion efficiency is often used in literature, and is simply the conversion gain as defined in (1.8) but expressed as a percentage, with percentages lower than 100 % implying a conversion loss. This work uses the term conversion gain in order to address the efficiencies as either DC-to-RF efficiency or PAE.

Harmonic rejection is another important figure of merit in the design of frequency multipliers. It is a measure of the difference in power level between the wanted and the unwanted harmonics, and is expressed in dBc. Improved harmonic rejection is achieved through appropriate harmonic terminations at the ports of the device, with optimum design providing reactive terminations to the unwanted harmonics in order to maximise the conversion gain of the multiplier.

Output power capability C_p provides a useful measure for comparing different Class E circuits. It is defined as the maximum power that can be delivered to the load when the device has a peak voltage of 1 V and a peak collector current of 1 A, for standard normalized values of $R = 1\Omega$ and $V_{DD} = 1V$. It is defined as,

$$C_p = \frac{P_o}{V_{ds,max} \cdot I_{ds,max}}. \tag{1.12}$$

For circuits with $R \neq 1\Omega$ and $V_{DD} \neq 1V$, the following normalisations are needed [19]: $V_{ds,max}/V_{DD}$, $I_{ds,max}R/V_{DD}$ and P_oR/V_{DD}^2.

1.2.2.2 Nonlinear Analysis Tools for Frequency Multipliers

Harmonic Balance (HB) is the prevalent circuit solver engine for nonlinear circuits, and can be applied to strongly nonlinear systems such as frequency multipliers, that are excited by large-signal periodic sources. Harmonic balance operates by first splitting up a circuit into its linear and nonlinear constituent components. The linear portion of the circuit is treated as one multiport network and is described at each harmonic by S,Y or ABCD parameters, in a matrix of a certain size. Each nonlinear element of the circuit is modelled in the time domain based on its I/V or Q/V characteristics and is

described in a subcircuit. Each of these nonlinear subcircuits is connected to the ports of the linear multiport network as shown in Figure 1.9. Linear circuit analysis techniques are first used in the frequency domain to determine the harmonic port voltages and corresponding currents of the linear multiport network. An inverse Fourier transform is then performed in order to transform the frequency domain port voltages to time domain voltage waveforms[1]. These voltage waveforms are next used to calculate current time domain waveforms at the ports of the nonlinear elements via their describing models. The port current waveforms are converted into the frequency domain and compared to the port currents obtained at the linear multiport. The error between the two is used to produce a new estimate for the port voltages and is repeated until convergence to within a set error value is achieved.

A useful consequence of HB in the design of switching frequency multipliers (or switching circuits in general) is the access to voltage and current time domain waveforms through the Fourier and inverse Fourier transform process. This is invaluable in determining the behaviour of the multiplier and its deviation from the ideal terminal waveforms at the active device for optimum performance. One of the drawbacks associated with HB is the difficulty in convergence for highly nonlinear environments such as switching circuits, often resulting in erroneous results and numerical instability. Other associated problems relate to the possibility of some circuits to possess more than a single solution, where the solver may converge to a solution that is non-physical [21].

1.3 Frequency Multipliers - A Review

1.3.1 Nonlinear Mechanisms of a FET for Harmonic Generation

One of the first authors to recognise the potential for FETs to be used in frequency multipliers was Pan [22] in 1978. The advantages of FET based multipliers over varactor based multipliers were identified as achievable conversion gain, wideband operation, better isolation, lower noise performance and lower required input drive power. The device nonlinearities targeted were the gate-source capacitance C_{gs}, and the nonlinear transconductance g_m. The MESFET was biased at pinch-off. However, no details of

[1] HB is based on the assumption that a steady-state solution exists for a given sinusoidal excitation, and can be approximated by a finite Fourier series [20]

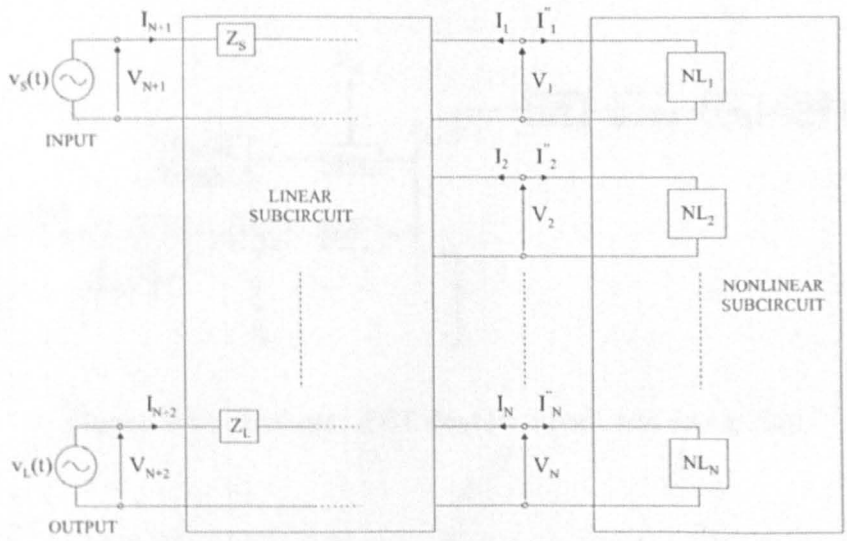


Figure 1.9: Harmonic Balance operation by dividing a circuit into linear and nonlinear subcircuits [2].

the input or output matching networks were given. Doublers at 8 GHz were fabricated in common-gate and common-source configurations and a higher conversion gain was claimed for the latter. A conversion gain of 1 dB was achieved with 66 % efficiency and output power of 13 dBm at $2f_0$.

In the same year, Chen [23] investigated the merits of dual-gate GaAs FETs for frequency multiplication. This type of device was previously used in the design of mixers and variable-gain amplifiers that exploited the fact that the transconductance of the FET can be controlled by the voltage on the second gate. The input drive was applied to the first gate and a sliding short at the second gate to enhance the doubling efficiency, as shown in Figure 1.10. The output was coupled to a HPF to reject the fundamental frequency followed by a second harmonic tuner to maximise output power at $2f_0$. The gate and drain bias voltages were also varied to provide optimum conversion gain at each level of input drive. A conversion gain of 8 dB was achieved at 12 GHz with an input power of 0 dBm. A similar set-up was also used to investigate the tripling performance of the FET. A conversion gain of 2.5 dB was observed at an output frequency of 12 GHz and -2 dB at 18 GHz. However the DC-to-RF efficiency cannot be deduced as details of the bias conditions are not given.

A comparison of single-gate and dual-gate FET frequency doublers was presented by

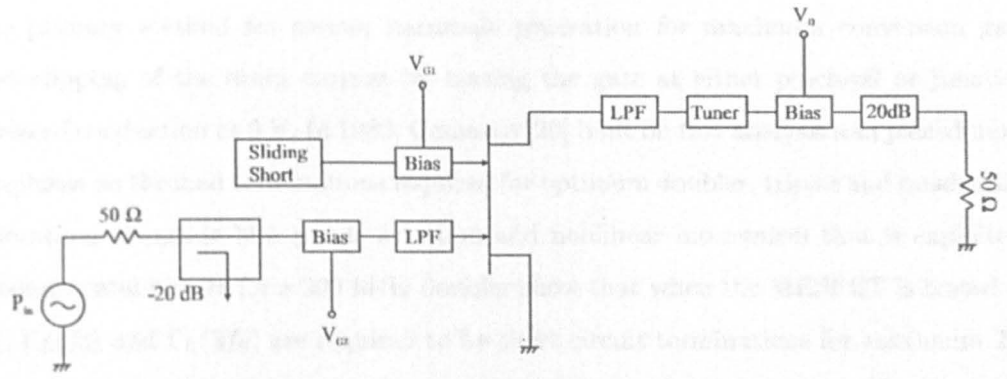


Figure 1.10: Dual-gate FET doubler circuit test set-up [23].

Gopinath *et al* [24] in terms of each of the four nonlinearities, C_{gs}, g_d, g_m, and drain current clipping due to pinch-off and gate-source junction forward conductance. It was claimed that the large series resistance associated with C_{gs} renders it an inefficient mechanism for harmonic generation. The nonlinearity of the output conductance was also affirmed to be insufficient for significant harmonic generation. The current clipping due to pinch-off or forward conduction by biasing the gate at pinch-off voltage V_p or near 0 V respectively results in a half-wave rectified $I_{ds}(t)$ with a second harmonic power 6 to 8 dB lower than the fundamental. For bias levels between V_p and 0 V, the nonlinear g_m displaying a square-law characteristic, contributes to a second harmonic component 12 dB below the fundamental. The dual-gate FET is modelled as two single-gate FETs in series and it is noted that its small signal gain is 6 dB higher than that of a comparable single-gate device, with corresponding higher doubler conversion gain. The second harmonic power however still remains 6 to 8 dB lower than the fundamental as expected. It was concluded that the enhanced performance of dual-gate FET doublers was mainly the result of increased intrinsic device gain than of any increased nonlinearity.

In 1982, Gopinath [25] presented a detailed analysis of the contributions of each of the nonlinear mechanisms inherent in a FET device to harmonic generation. Each of the nonlinearities were described mathematically and quantitatively analysed for their potential for harmonic generation. These nonlinearities were included in a unilateral model of a complete FET device and computer simulations were used to verify the harmonic contribution of each of the nonlinearities individually. It was shown that

the primary method for second harmonic generation for maximum conversion gain was clipping of the drain current by biasing the gate at either pinch-off or junction forward conduction at 0 V. In 1983, Camargo [26] built on this analysis and placed more emphasis on the load terminations required for optimum doubler, tripler and quadrupler operation, alongside bias points selection and nonlinear mechanism that is exploited. Experimental results for a 200 MHz doubler show that when the MESFET is biased at V_p, $\Gamma_L(f_0)$ and $\Gamma_L(3f_0)$ are required to be short circuit terminations for maximum $2f_0$ output power, with the transconductance being the predominant harmonic generator. Biasing the MESFET near 0 V however, requires an open circuit $\Gamma_L(f_0)$, with the output conductance g_d being the major harmonic generator in this case. An 8 GHz doubler was presented that gives 5 dB gain, 14 dBm output power and PAE of 8 % when biased at pinch-off, but 6 dB of gain, and 4 % PAE at the same output power when biased near forward conduction. It is suggested that input matching was more easily accomplished and more efficient harmonic generation was achieved when a bias near 0 V was chosen. Results for a 12 GHz tripler were also given with 3 dB of gain and 13 dBm of output power, with a PAE of 3 %. However the load terminations for the tripler are not clear, and 0 V bias is assumed based on the doubler results.

Biasing the FET near forward conduction of the gate has been shown to be an efficient harmonic generator, and it has been claimed to provide high gain at odd order harmonics [27]. The merits of clipping via forward gate conduction over pinch-off seem to be marginal though, with an added 1 dB of gain achieved in forward conduction. The drawbacks of this bias plan, as outlined by Camargo [26] and Rauscher [28], are the associated higher DC drain currents which severely compromises the achievable DC-to-RF efficiency, and the associated greater risks of device failure due to high gate current spikes during forward conduction. With these disadvantages considered, the design of frequency multipliers subsequently tended to favour bias at pinch-off. This was followed by Maas' analytical description of optimally biased frequency multipliers near pinch-off that exploit the nonlinearities generated through single-sided drain current clipping, and has come to be known as classical multiplier design [2].

1.3.2 Classical Frequency Multipliers

Maas [2] assumes an ideal FET with piecewise linear transconductance g_m, to simplify the analysis and develop a first order estimate for the optimum input drive and gate bias combination. The ideal circuit is shown in Figure 1.11, and consists of a parallel tank circuit tuned to the required harmonic, thus terminating all unwanted harmonics in a short circuit, and presenting an optimum load R_L to the wanted harmonic. R_L is chosen to provide maximum output voltage swing between V_{min} (determined by the knee voltage of the IV characteristic) and V_{max} (determined by the breakdown voltage of the FET) with the drain bias midway between these two values, as per usual power amplifier design. The FET is biased below the pinch-off voltage V_p, similar to that of a Class-C amplifier.

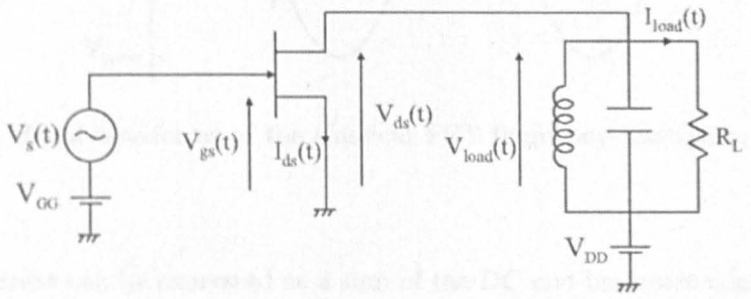


Figure 1.11: Ideal classical FET frequency multiplier, as proposed in [2].

The drain waveforms of the circuit are shown in Figure 1.12, and it can be seen that by biasing the FET below V_p, conduction occurs for only a fraction of the input signal cycle when the gate voltage exceeds V_p, thus producing drain current pulses that are rich in harmonics. The peak value of the current pulses I_{max}, corresponds to the maximum gate voltage value $V_{g,max}$. The fraction of the full input signal cycle during which the FET conducts is called the conduction angle $2\theta_c$, and is related to the duration of the drain pulse t_o to the period of the excitation signal T by,

$$2\theta_c = 2\pi\frac{t_o}{T}, \tag{1.13}$$

where the ratio $\frac{t_o}{T}$ is the duty cycle of the pulse.

The assumption of a linear g_m implies the current pulses are sinusoidal in nature, and

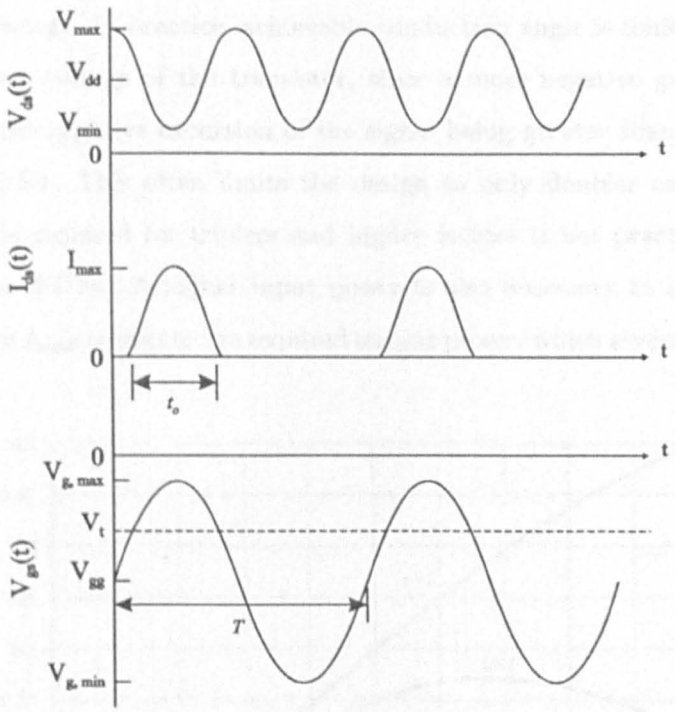


Figure 1.12: Ideal waveforms of the classical FET frequency multiplier, as proposed in [2].

the drain current can be expressed as a sum of the DC and harmonic content,

$$I_d(t) = I_0 + I_1 \cos \omega_o t + I_2 \cos 2\omega_o t + ..., \tag{1.14}$$

where ω_o is the frequency of the input signal. A Fourier series expansion for the cosine pulse train gives the coefficients as,

$$I_n = I_{max} \frac{4t_o}{T} \left| \frac{\cos n\pi t_o/T}{1-(2n\pi t_o/T)^2} \right| \qquad \text{for} \quad n \geq 1, \tag{1.15}$$

$$I_0 = I_{max} \frac{2t_o}{T} \qquad \text{for} \quad n = 0. \tag{1.16}$$

A plot of (1.15) given in Figure 1.13 shows that in order to maximise a particular required harmonic current I_n in R_L, the appropriate duty cycle ratio must be chosen. This is determined by the input gate bias level and the level of the input excitation signal. It can be seen, however, that smaller conduction angles are required for higher

multiplication factors. In practice, achievable conduction angle is limited by the gate-source breakdown voltage of the transistor, since a more negative gate bias voltage could result in the negative excursion of the signal being greater than the breakdown voltage of the FET. This often limits the design to only doubler capability, as the conduction angle required for triplers and higher factors is not practically realisable in most available FETs. A higher input power is also necessary to achieve a higher $V_{g,max}$ and hence I_{max} to obtain the required output power, which severely compromises conversion gain.

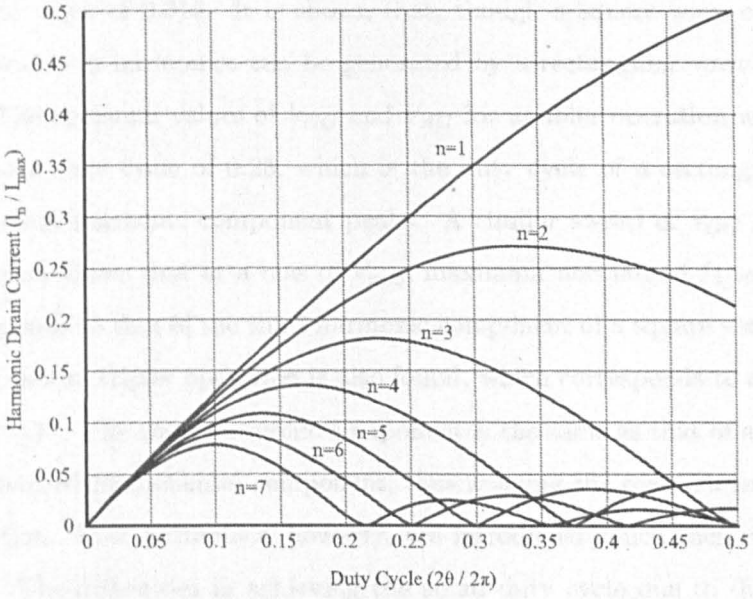


Figure 1.13: Harmonic components of the drain current as a function of duty cycle for classical multipliers, [20].

An improvement in tripler design, which addressed the issue of unachievable conduction angle, was presented by Fudem *et al* [29] in 1998. They proposed a double-sided clipping mechanism instead of the single-sided clipping provided by the classical approach. A 0.25μm pHEMT transistor was biased in Class A condition at V_{mid} which is midway between V_p and forward conduction. The device was then heavily overdriven by a large input signal, resulting in clipping of the drain current on the negative excursion due to pinch-off and on the positive excursion due to gate forward conduction. With sufficiently large drive, the drain current waveform tends towards a square waveform rich in odd harmonics, with a third harmonic power 4.8 dB lower than the fundamental power. The ideal theoretical efficiency for the tripler was calculated to be 16.7 %. However, the

drawbacks include reduced conversion gain due to the large input drive required and low efficiency due to forward conduction. A balanced broadband tripler was presented in this scheme, and output power of above 5 dBm was achieved over 42-51 GHz, with a peak power of 12.5 dBm. A large drive power of 23.6 dBm was required, resulting in a conversion loss of 11.1 dB. An in-depth analysis of the double-sided clipping mechanism was presented by O'Ciardha [30]. A Fourier series of the drain current was given dependent on the DC gate bias and AC amplitude of the input signal. A sweep of these values shows that, in the case of a doubler, normalized maximum I_2 reaches an asymptotic value of 0.318. It is shown that, though a square wave contains only odd harmonics, even harmonics can be generated by a rectangular wave of a certain duty cycle. The optimum values of V_{GG} and V_{AC} for doubler operation were found to correspond to a duty cycle of 0.25, which is the duty cycle of a rectangular wave at which the second harmonic component peaks. A similar sweep of V_{GG} and V_{AC} for tripler operation shows that at a bias of V_{mid}, maximum normalised I_3 tends to 0.212 which corresponds to that of the third harmonic component of a square wave. A second regime for optimum tripler operation is also found, which corresponds to a rectangular duty cycle of 0.17. The third harmonic component is the same as that of a square wave but with a reduced fundamental component, thus relaxing the requirements for fundamental rejection. Even harmonics, however, are introduced which then would require suppression. The difficulties in achieving the small duty cycle due to the breakdown voltage of the FET is also of major concern. A MMIC frequency tripler at 56.2 GHz was presented with optimum bias and drive conditions imposed as predicted above, and a minimum conversion loss of 14.1 dB was achieved.

An alternative improvement to the classical approach was proposed by Zhang et al [31] in 1996. In the classical approach, all unwanted harmonics at the output are terminated in a short circuit. The design, therefore, depends solely on the non-linearity provided by current clipping to produce the required harmonic, resulting in relatively low conversion gain for triplers. Zhang proposed to improve the conversion gain by introducing a fundamental rejection feedback mechanism to the design, as shown in Figure 1.14. The feedback allows for some independence in the output load presented to the fundamental and the third harmonic. The HEMT is biased near V_p, where classical multipliers would provide no third harmonic content. The gate bias, input

and output matching networks, and third harmonic load were optimised to provide the maximum conversion gain. However, details of the harmonic terminations are not given. The output fundamental load was then swept to improve the conversion gain. A 34.5 GHz tripler is presented and the variation in conversion gain with the phase of the fundamental load angle is shown to be significant. A maximum conversion gain of -6 dB is achieved with an input power of 0 dBm.

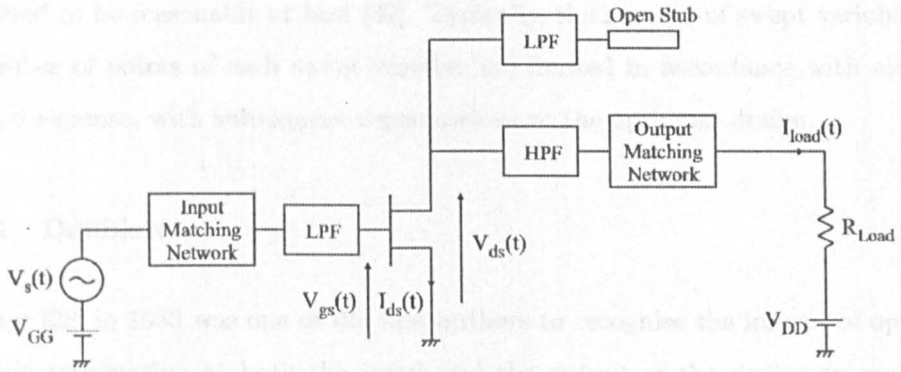


Figure 1.14: HEMT tripler topology with fundamental rejection feedback, as proposed in [31].

The work described above indicates the beginning of a shift in focus in multiplier design from the optimum gate bias and input drive level, to the terminating impedances presented to the harmonics. It was recognised that the short-circuit termination to all unwanted harmonics at the output, and the simple fundamental conjugate match at the input may not produce a multiplier with optimum operation. This led to the popular load/source pull analysis for the design of frequency multipliers, where the bias levels and harmonic terminations at both the input and output of the active device are swept simultaneously to determine the optimum operating conditions.

1.3.3 Load/Source Pull design for Frequency Multipliers

Whilst previous studies concentrated mainly on the output terminations and bias conditions of the device, it was recognised that different reactive harmonic terminations at the input and output of the device could be implemented that would result in the unwanted harmonics constructively adding to the required harmonic whilst destructively interfering with other unwanted harmonics. The source/load pull design procedure in-

volves adjusting the harmonic impedances presented to the active device at its input and output, and sweeping the bias points and input power level at each stage for optimum performance. Purely reactive harmonic terminations are used in order to prevent power being dissipated at unwanted harmonics. With the availability of nonlinear simulators in CAD packages and large signal device models, source/load pull can be simulated. However, a comparison between simulated and actual source/load pull measurements is reported to be reasonable at best [32]. Typically, the number of swept variables and the number of points of each swept variable are limited in accordance with available time and expense, with subsequent repercussions to the optimum design.

1.3.3.1 Doublers

Rauscher [28] in 1983 was one of the first authors to recognise the impact of optimum harmonic termination at both the input and the output of the device on multiplier performance. The model used assumes a nonlinear current generator and output conductance, and linear fixed values for C_{gs} and C_{gd}. Rauscher assumes $\Gamma_S(f_0)$ and $\Gamma_L(2f_0)$ to be conjugate matches at the input and output of the device respectively. The effect of $\Gamma_L(f_0)$ at the output of the device on doubler performance was then investigated with $\Gamma_S(2f_0)$ as a short circuit termination. A short circuit stub of varying electrical length θ was implemented to realise a sweep of fundamental loads. It was shown that the conversion gain is markedly dependent on the output fundamental termination, with the dependence being linked to the parasitic feedback of the transistor. The conversion gain was seen to theoretically approach infinity at values of $\Gamma_L(f_0)$ that provide a fundamental parallel resonance with the output parasitic elements of the device. It was mentioned that any improvements in conversion gain through exploitation of the feedback mechanism is achieved at the expense of signal bandwidth. At the input, Rauscher investigated the dependence of doubler performance on second harmonic input termination. The second harmonic frequencies lay beyond the range of transistor operation, and hence parasitic feedback was attributed to the effect of $\Gamma_S(2f_0)$ on doubler performance. A drop in conversion gain for certain values of $\Gamma_S(2f_0)$ was observed and coincides to the maximum loss of $2f_0$ output power due to parasitic feedback. These destructive feedback effects can be circumvented by implementing additional external feedback at the second harmonic of appropriate amplitude and phase to cancel out the

effects, as shown in Figure 1.15. This, however, has implications on bandwidth and circuit complexity and is dependent on application. A 30 GHz doubler was implemented with a GaAs FET and a maximum conversion gain of -0.6 dB.

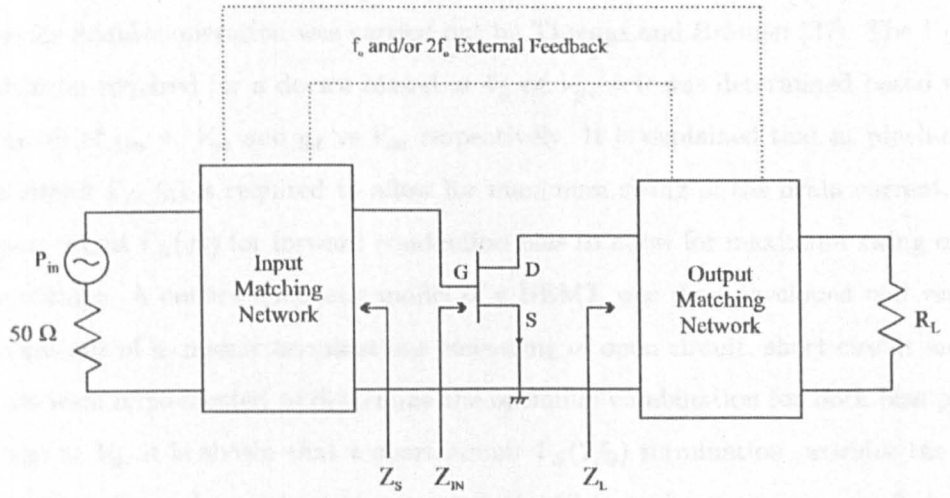


Figure 1.15: GaAs frequency doubler with external feedback at f_0 and/or $2f_0$, as proposed in [28].

Gilmore [33] also investigated $\Gamma_L(nf_0)$ terminations that lead to the unwanted harmonics maximising the desired harmonic power. The input and output were conjugately matched at f_0 and $2f_0$ respectively. The effect of $\Gamma_L(f_0)$ on doubler performance was found to be consistent with the findings of Rauscher. It was claimed that the optimum $\Gamma_L(f_0)$ load is an open circuit but shifted by the conjugate of the output capacitance of the FET. Stancliff [34] claimed that this condition provides a horizontal loadline on the IV characteristics of the FET, with a small variation in input voltage swing resulting in a large distortion of the output voltage swing. The open circuit $\Gamma_L(f_0)$ termination is optimum for both pinch-off bias and Class A bias conditions. Dow et al [35] however, arrived at the conflicting conclusion that an open circuit $\Gamma_L(f_0)$ for forward gate conduction bias, and a short circuit $\Gamma_L(f_0)$ for pinch-off bias provides optimum doubler operation.

The results presented by Larose et al [36] also seem to contradict the above findings. An experimental active load-pull characterisation was carried out on a MESFET, with the aid of a six-port analyser and frequency selective power detectors. Signals at different frequencies were handled simultaneously with the test set-up, allowing for independent

harmonic load control. It was found that maximum harmonic generation is obtained if the output of the device is presented with an short circuit at the fundamental frequency.

An in-depth study of the harmonic terminations at the input and output of the active device for doubler operation was carried out by Thomas and Branner [37]. The $\Gamma_L(f_0)$ termination required for a device biased at V_p or $V_{gs} = 0$ was determined based upon the curves of g_m v. V_{gs} and g_d vs V_{ds} respectively. It is explained that at pinch-off, a short circuit $\Gamma_L(f_0)$ is required to allow for maximum swing of the drain current, and an open circuit $\Gamma_L(f_0)$ for forward conduction bias to allow for maximum swing of the drain voltage. A curtice-quadratic model of a HEMT was then developed and various combinations of harmonic terminations consisting of open circuit, short circuit and 50 Ω loads were implemented to determine the optimum combination for both bias plans. For bias at V_p, it is shown that a short circuit $\Gamma_S(2f_0)$ termination provides the best conversion gain, and an output short circuit $\Gamma_L(f_0)$ provides optimum overall doubler performance. A termination of 50 Ω was assumed for $\Gamma_S(f_0)$, and it is shown that with conjugate match instead a 5 dB increase in conversion gain can be achieved. It is also claimed that a further 1.2 dB of conversion gain can be achieved if the third harmonic is open circuited. A conjugate match of $2f_0$ at the output instead of 50 Ω results in an additional 2dB of conversion gain. Experimental results were presented for a 6 GHz doubler utilising the above harmonic terminations. A conversion gain of 5.5 dB was achieved when biased near pinch-off with $\Gamma_L(f_0)$ a short circuit, and 0 dB when biased near forward conduction with $\Gamma_L(f_0)$ an open circuit.

1.3.3.2 Triplers

In general, frequency triplers and higher order multipliers have not seen the prominence and detailed investigation benefited by doublers, due to challenging design, higher circuit complexity and lower achievable conversion gain and efficiency. Zhao et al [38] investigated the harmonic loading effects on the output power of a tripler for gate bias ranging from Class A to C, with the drain biased at 3V. A large signal Tajima model was used for the MESFET load-pull simulations, and $\Gamma_L(f_0)$, $\Gamma_L(2f_0)$ and $\Gamma_L(3f_0)$ along with $\Gamma_S(f_0)$ were sequentially swept to find the optimum performance. $\Gamma_S(2f_0)$ and $\Gamma_S(3f_0)$ were kept at short circuit. At Class B bias, it is shown that with $\Gamma_L(2f_0)$

a short circuit, the effect of $\Gamma_L(f_0)$ on the third harmonic output power is significant. An offset inductive fundamental load ($\approx 60°$) from open circuit is shown to be optimum. With $\Gamma_L(f_0)$ set as a short circuit, the effect of $\Gamma_L(2f_0)$ is negligible and third harmonic output power is low, implying that $\Gamma_L(f_0)$ is more critical than $\Gamma_L(2f_0)$. A short circuit $\Gamma_L(2f_0)$ is optimum. A maximum third harmonic power of 4.2 dBm was shown to be possible, although with restraints placed on $I_g(t)$, $V_g(t)$, $V_{gd}(t)$ and $V_d(t)$ to ensure device reliability, maximum output power was restricted to 3.7 dBm, with a conversion loss of 6.5 dB and an efficiency of 2 %. The effects of $\Gamma_S(f_0)$ and input power level, however, are not included, and experimental results of the above tripler are not given. It is concluded that triplers biased in Class A fashion also require the same optimum harmonic loading, and have a higher conversion gain but lower efficiency than those biased in Class B. Class C bias is shown to result in both low conversion loss and efficiency.

Mima et al [39] provide an ideal analytical investigation of third harmonic conversion gain, and to a certain extent conflict with the findings of Zhao. With Class A bias, the optimum $\Gamma_S(2f_0)$ and $\Gamma_S(3f_0)$ are shown to be short circuits, optimum $\Gamma_L(f_0)$ to be an offset capacitive open circuit ($\approx -4°$) and $\Gamma_L(2f_0)$ an inductive open circuit offset, contradicting Zhao. Practical realisations of the ideal terminations were implemented in microstrip [40] by open stubs to realise the short circuit terminations, and a high-self-resonant chip capacitor in parallel with a length of bond wire to realise the series open circuit elements. A 9 GHz tripler was demonstrated with a conversion gain of 2.9 dB at an output power of 7.9dBm. This work was further extended by Johnson et al [41]. A full nonlinear pHEMT model was used and various combinations of harmonic input and output short and open circuits were first investigated to determine the optimum case. These terminations were then offset from their ideal value to maximise conversion gain. Initial optimum terminations were found to be short circuits for $\Gamma_S(2f_0)$ and $\Gamma_S(3f_0)$, and an open circuit for $\Gamma_L(f_0)$ and short circuit at $\Gamma_L(2f_0)$. Final offsets were 90°, 120°, 180°, and 90° respectively with respect to f_0. The output termination $\Gamma_L(3f_0)$ was not investigated and is assumed to be 50 Ω. A fabricated tripler at 8.8 GHz was presented biased near forward conduction at $V_{gs} = 0.1$ V, with a conversion gain of 3.67 dB and input power 4 dBm.

It has been shown that load/source pull multiplier designs provide an improvement on

achievable conversion gain by introducing reflective networks with the aim of maximising the power at the required harmonic. Although this procedure has been investigated in depth, several inconsistent conclusions have been drawn regarding the types of harmonic terminations required. For most cases, this can be attributed to the different systematic procedures in optimising the various terminations and bias levels of the circuit, the specific harmonic terminations that are assumed fixed and those that are varied, and even the load and source terminations that are considered. As an example, the discrepancy between Rauscher [28] and Larose [36] for optimum doubler design could be attributed to the fact that Rauscher provides a short circuit for $\Gamma_S(2f_0)$ whereas Larose only considers the load terminations, and source termination can only be assumed to be a conjugate match at the fundamental. Discrepancies can also arise due to the extreme sensitivity of multiplier performance on the device used. The type of device, its size and the model used can all have a profound effect on a multiplier's performance. In some cases, however, inconsistencies are arrived at even when using the same device at the same frequency. For example, Mima et al [39],[40] perform a load and source pull for the ATF-36163 FET to determine optimum tripler performance at 8.8 GHz. However, the work presented by Johnson [41] expands on the previous work but results in different harmonic terminations for a tripler at 8.8 GHz using the same FET. This highlights the fact that load/source pull designs remain somewhat dependent on trial and error iterations with blind optimisation procedures, lacking in a tangible and definite mathematical treatment. This is mainly due to its significant sensitivity to the device used.

1.3.4 High Efficiency Frequency Multipliers

The design criteria for work reviewed thus far were mainly focussed on achieving maximum conversion gain and output power. However, optimising DC-to-RF efficiency ($\eta_{DC/RF}$) soon gained prominence as an important performance parameter for multipliers. Le [42] in 1992 was one of the first authors to consider a load-pull investigation to optimise both conversion gain as well as $\eta_{DC/RF}$. A full load-pull set up was used to independently tune $\Gamma_L(f_0)$, $\Gamma_L(2f_0)$ and $\Gamma_L(3f_0)$ for a 7.5 GHz tripler. Contrary to previously published results, optimum $\Gamma_L(f_0)$ was found to be an offset short circuit. The optimal $\Gamma_L(2f_0)$ was found to be a load that is 180° from the f_0 termination, sug-

gesting an equal amount of offset from the open circuit. Third harmonic termination was also tuned and an optimum $\Gamma_L(3f_0)$ of $0.6\angle 70°$ was established. The fabricated tripler was biased near pinch-off and provided 1.6 dBm of output power with a conversion loss of 2.4 dB, and a $\eta_{DC/RF}$ of 13 %. An investigation into input harmonic terminations, however, was not included.

In 2001, Penn [43] investigated efficient S - X band frequency triplers with application to space communications. Three sections were proposed for the complete tripler: a harmonic generator, filter and amplifier. A 300μm GaAs MESFET biased at pinch-off with +5 V on the drain was implemented as the harmonic generator and conjugate matching at the input and output was chosen for optimum performance. This was followed by a tuneable bandpass filter with a 15 % bandwidth to suppress the fundamental and second harmonic, with low attenutation of the third harmonic. The output level of the tripler was required to be +10 to +13 dBm, and both a one-stage and two-stage amplifier were investigated as a final stage to amplify the third harmonic component. Measurements at 6.9 GHz of a broadband 6.6-7.5 GHz tripler using the two-stage amplifier were presented at an input power of +8 dBm showing -0.7 dB conversion gain, 7.3 dBm output power and $\eta_{DC/RF}$ of 4 %.

A similar strategy was adopted by Beaulieu [44] using GaAs/InGaP HBT technology for a 25.5-31.5 GHz tripler. The tripler was biased in class B configuration and broadband conjugate matches at the input and output were chosen. This stage was followed by a two-stage amplifier, and an input power of +15 dBm was required. An output power of +10 dBm with 5 % $\eta_{DC/RF}$ was achieved. InP-based high efficiency multipliers were also demonstrated by De Los Santos [45] for particular application to wireless communications. InP-based and Si-based x6 (127 to 762 MHz) and x4 (762.5 to 3050 MHz) multipliers were compared in terms of output power and $\eta_{DC/RF}$. The InP-based x6 multiplier achieved 6 dBm of output power and 11 % efficiency, compared to 7.2 dBm and 4.8 % of the Si-based one. The InP-based x4 circuit achieved 3.74 dBm of output power and 8 % efficiency, compared to -6.1 dBm and 0.4 % of the Si-based multiplier, thus demonstrating the superiority of InP-based frequency multipliers over Si-based ones due to their higher transconductance and lower input threshold voltage.

In 2006, Adahl [46] proposed a high efficiency doubler at 5.75 GHz by implementing a

negative feedback loop via a parallel RC network at the source of the FET. Two 0.15 μm mHEMT were biased in deep class C in a balanced configuration, with the RC network shared at the sources. The doubler was shown to provide 8 dBm of output power with 1.58 dB of conversion gain and $\eta_{DC/RF}$ of 16 %.

Whilst the $\eta_{DC/RF}$ reported above are significant improvements on previous designs, they are subject to the trial and error iterations of load/source pull designs designs and the inconsistencies that can arise for optimum design. Performing full load/source pull measurements, where the complete bias and impedance planes for each harmonic are sequentially swept, can be time consuming and expensive. This, as shown earlier, can lead to only a chosen set of terminations or bias planes to be investigated, resulting in inconsistent optimum design parameters. Class E frequency multipliers offer a convincing alternative by presenting a definite design plan for the harmonic terminations, and it has been shown to result in higher achievable efficiencies and conversion gains over the load/source pull designs, making it an attractive option for space-borne or other power critical systems.

1.3.4.1 Class E Frequency Multipliers

Class E frequency multipliers, like their amplifier counterparts, offer higher drain efficiencies by shaping the voltage and current waveforms at the drain of the active device such that overlap is reduced, resulting in minimal power dissipation [47]. They benefit from lower device sensitivity and explicit closed-form design equations thus offering *a priori* designability. A simplified schematic of a class E frequency multiplier is shown in Figure 1.16.

The active device is operated as a switch by the input drive waveform, and the operation of the multiplier is determined by the switch current when ON and by the transient response of the load network when the switch is OFF. Harmonic generation is achieved through the switching behaviour of the device, and maximisation of the power at the required harmonic is achieved at a particular duty cycle. A detailed analysis of Class E multipliers was performed by Zulinski et al [48] in 1986. It was shown that the optimum duty cycle D, of an N^{th} harmonic multiplier for a theoretical $\eta_{DC/RF}$ of 100 % and maximum output power capability is given by (1.17).

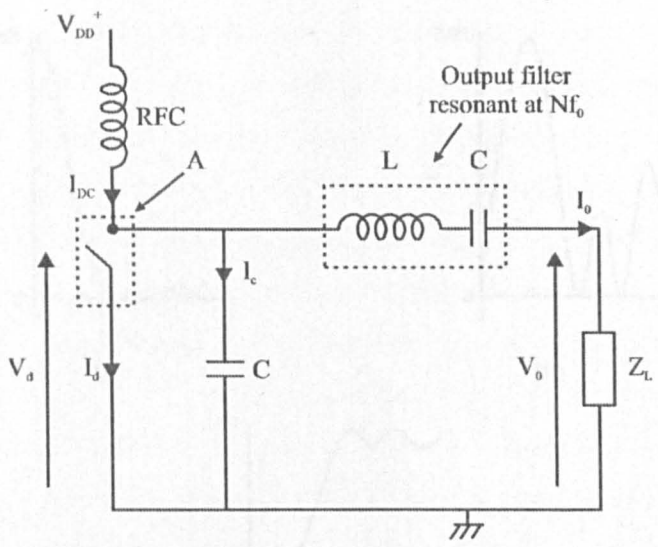


Figure 1.16: Simple representation of an N^{th} harmonic class E frequency multiplier

$$D = \frac{1}{2N}. \tag{1.17}$$

The duty cycle in this case was defined as the ratio of switch OFF time to the period of the excitation signal. This, in turn, can be interpreted as the duration of time that the excursion of the input drive signal is below V_p to the period of the excitation signal. This is opposite to the duty cycle as defined by Maas [2] for classical multipliers. It was shown that duty cycles other than that given in (1.17) are also capable of providing a $\eta_{DC/RF}$ of 100 % but at a much reduced output power and output power capability, as shown in Figure 1.17 for the case of a doubler. The load angles required for optimum Class E operation at these duty cycles is also shown in Figure 1.17, and can be seen to approach 90° for duty cycles above $\frac{1}{N}$, implying a load close to being purely reactive. It can be seen from (1.17) that higher multiplication factors require smaller duty cycles, and hence the gate and input drive level need to be adjusted accordingly to provide the required duty cycle.

It was also demonstrated in [47] that for an N^{th} harmonic multiplier, duty cycles up to $\frac{1}{N}$ (the first lobe of the C_p plot) produce positive voltage waveforms but positive and negative current waveforms. Duty cycles encompassing the last lobe produce positive current waveforms but positive and negative voltage waveforms, and duty cycles

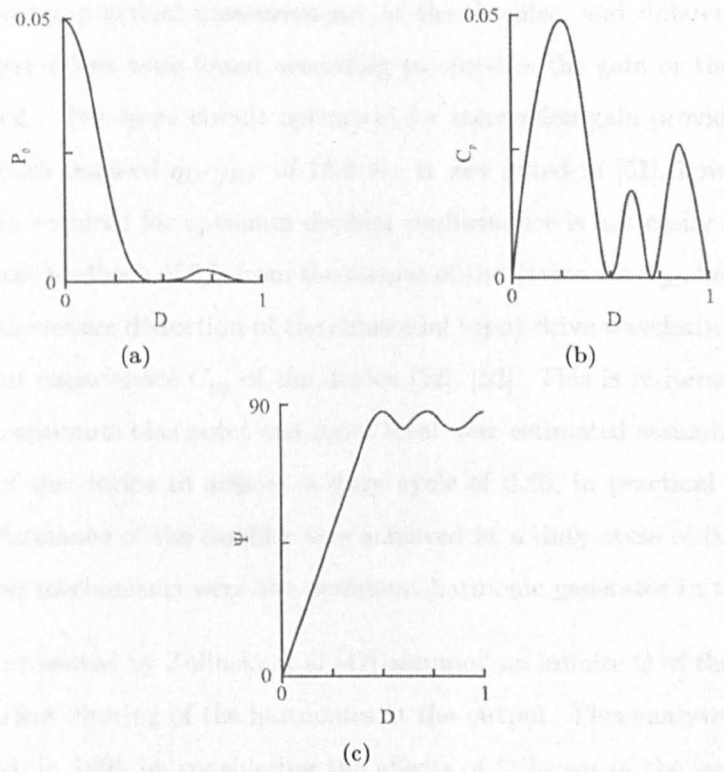


Figure 1.17: (a) Output power, (b) Output power capability and (c) Load angle as a function of duty cycle for a Class E doubler [47].

that fall between these outer lobes result in positive and negative voltage and current waveforms. Optimum operation according to (1.17) therefore results in positive voltage and positive/negative current waveforms. It was claimed that FET devices cannot withstand negative drain voltages due to the forward conduction of a parasitic diode regardless of gate voltage, but can withstand positive and negative drain current.

The first high efficiency class E doubler was reported in 1986 by Zulinski et al [47] at an output frequency of 3.37 MHz with 95 % $\eta_{DC/RF}$, 20.7 dBm of input power and 0.26 dB of conversion loss. The measured switch current waveforms, however, are shown to be continuous sine waves which is inconsistent with the switching behaviour that is theoretically predicted. In 1999, Weiss et al [49] reported class E doublers at 1 GHz and 5 GHz with PAE of 35 % and 29 % with corresponding conversion gains of 8.5 dB and 5.2 dB at input powers of 23.5 dBm and 20 dBm respectively. A higher frequency doubler was also reported in 2001 [50],[51] at an output frequency of 20.8 GHz with 51 % $\eta_{DC/RF}$, 7.5 dBm of output power and a conversion gain of -1.77 dB. Sweeps were

carried out during practical measurements of the doubler, and different sets of bias levels and input drives were found according to whether the gain or the $\eta_{DC/RF}$ was to be optimised . The same circuit optimised for conversion gain provided 7.18 dB of gain with a much reduced $\eta_{DC/RF}$ of 13.8 %. It was noted in [51], however, that the 0.25 duty cycle required for optimum doubler performance is not easily achieved. It is attributed to the feedback of $2f_0$ from the output of the device via C_{gd}, however, is more likely due to the severe distortion of the sinusoidal input drive waveform mainly by the nonlinear input capacitance C_{gs} of the device [52], [53]. This is re-iterated in the fact that although optimum bias point and input level were estimated assuming linear input components of the device to achieve a duty cycle of 0.25, in practical measurements optimum performance of the doubler was achieved at a duty cycle of 0.04, suggesting other nonlinear mechanisms were the dominant harmonic generator in this case.

The analysis presented by Zulinski et al [47] assumed an infinite Q of the load network and hence perfect filtering of the harmonics at the output. This analysis was extended by Albulet [54] in 1995 by considering the effects of Q factor of the series tuned load network and the on-resistance of the active device on the performance of a multiplier. It was demonstrated that output power at the required harmonic of a multiplier decreases with decreasing values of Q factor. However, efficiency decreases with increasing values of Q but is less sensitive to Q at low values of on-resistance. Also shown, is that output power and efficiency both decrease with increasing values of on-resistance. The effect of the Q factor and on-resistance becomes more pronounced at higher multiplication factors. Albulet [19] also investigated the effect of switch duty cycle on the performance of Class E multipliers. The design values for the circuit components were given in terms of duty cycle, and were shown to significantly vary with duty cycle. It was claimed that for an N^{th} harmonic multiplier with a low Q value, higher output power capability can be achieved for duty cycles that are less than given by (1.17). The variation of output power capability of a tripler with duty cycle is shown in Figure 1.18, and it was claimed that the output power for a tripler is 15-50 times larger in the first lobe zone than in the last lobe zone.

Class E frequency multipliers have been shown to provide the best achievable efficiencies with excellent conversion gain. Accurate initial designs can be achieved due to the closed-form equations that determine optimum circuit elements, hence eliminating the

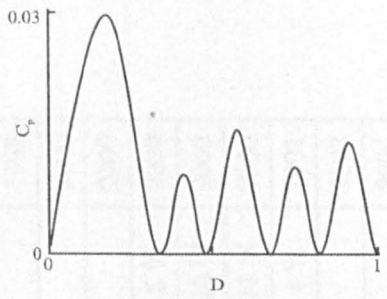


Figure 1.18: Output power capability for a Class E tripler as a function of duty cycle D [19].

need for time consuming load/source pull. As described above, the optimum duty cycle required for class E multipliers given by (1.17) becomes progressively smaller for larger multiplication factors. This implies that a smaller portion of the negative excursion of V_{gs} is below V_p. A small input drive leads to small excursions of V_{gs}, and hence the negative peak of V_{gs} that is below V_p may not be large enough to switch the device sufficiently off. A larger input drive is needed in order to provide enough voltage below pinch-off to ensure proper turn off of the device. A larger input drive, however, not only compromises the conversion gain but also increases the chances of undesirable forward conduction of the gate. This can limit the operability of most commercially available devices to not more than doubler operation.

A further problem arises as achieving the correct duty cycle to switch the device is more involved than simply choosing the correct bias and input drive levels [51], due to distortion caused by the nonlinear input capacitance, C_{gs}, of the device. A sweep of bias and input drive in large signal simulation may provide the best operating conditions, but since the shape of the distorted drive is not controlled it may not provide the optimum conditions necessary to switch the device efficiently. It has been shown [52] that the distortion of the input drive signal can be exploited in order to provide a more rectangular drive that is advantageous for class E design. Providing an open circuit to the odd harmonics and a short circuit to the even harmonics at the gate provides a square drive waveform with 50 % duty cycle. A square waveform drive, however, severely degrades the performance of class E multipliers as shown in Figures 1.17 and 1.18, as it deviates from the optimum value given in (1.17).

A summary of previously published results for frequency triplers is given in Table 1.1.

Triplers	Device	f_0 /GHz	P_{input} /dBm	P_{output} /dBm	Conversion Gain /dB	$\eta_{DC/RF}$	Year
Le [42]	GaAs FET	2.5	+4	+1.6	-2.4	13 %	1992
Henkus [55]	MESFET	2.8-3.5	+10	-0.4	-10.4	1.5 %	1993
Zhao [38]	MESFET	5	+10.2	+3.7	-6.5	2 %	1995
Zhang [31]	pHEMT	11.5	0	-6	-6		1996
Von Stein [56]	GaAs MESFET	2	+6	+2.4	-3.64		1996
Fudem [29]	GaAs FET	14	+23.6	+12.5	-11.1		1998
Thibaud [57]	pHEMT	11.5-13		+10			1999
O'Ciardha [30]	pHEMT	18.7	+17.5	+3.5	-14.0		2000
Mima [40]	pHEMT	2.95	+0.1	+3	+2.9		2000
Beaulieu [44]	HBT	9.5	+15	+10	-5	5 %	2000
Madriz [58]	pHEMT	2.125	-1	+3.1	+4.1	10 %	2000
Boudiaf [59]	pHEMT	12.6	+6.5	+3.1	-3.4	11 %	2000
Penn [43]	MESFET	2.3	+8	+7.3	-0.7	4 %	2001
Allen [27]	pHEMT	24.3	+17	0	-17		2003
Bunz [60]	HEMT	1.78-2.25	+3.0	+3.5	+0.5		2004
Johnson [41]	pHEMT	2.94	+4	+7.67	+3.67		2005
Chiu [61]	pHEMT	12.0	+14	+5	-9	16 %	2006

Table 1.1: Summary of previously published results for frequency triplers.

1.4 Contributions and Outline of the Thesis

Class E frequency multipliers have been shown to suffer from drive implementation limitations imposed by the smaller duty cycles that are required for higher multiplication factors. Smaller duty cycles also complicate the drive circuitry in order to obtain proper drive. A 50 % duty cycle relaxes these limitations, but has been shown to severely compromise the performance of class E multipliers.

This work demonstrates a novel class E multiplier configuration that allows for a 50 % duty cycle drive, whilst retaining the 100 % theoretical efficiency of the conventional class E circuit. A quantitative analysis of a novel tripler is provided that results in closed-form explicit design equations for the load network with 50 % duty cycle drive. It is shown that its maximum output power is not degraded and is theoretically the same as that of the conventional case. The optimum output power and efficiency, however, are more easily achieved since the 50 % duty cycle drive can be readily implemented, allowing for higher achievable conversion gains especially in case for higher order multipliers. The waveforms obtained for the novel tripler are shown to be positive current and positive/negative voltage. It was claimed by Zulinski [48] and Albulet [54], that FET devices cannot withstand negative drain voltages due to the forward conduction of a parasitic diode regardless of gate voltage, but can withstand the positive and negative drain current of conventional class E multipliers. In this work it will be shown that on the contrary, with appropriate choice of gate voltage, FET devices can withstand negative drain voltages with negligible draw of current, making them suitable for high efficiency design. This bi-directional operation of GaAs FET switches, for example, are extensively used for point-to-point and point to multipoint broadcast systems [62]. Also, although FET devices can support the positive and negative current of the conventional design, the voltage that is dropped whilst the current is negative is noteworthy, making them unsuitable for high efficiency operation in this configuration.

Chapter 2 introduces a novel first-order circuit analysis technique for Class E networks which provides more tangible insight into class E operation than previously published analyses, whilst being more compact and easily executed. It is used to analyse a class E amplifier and design equations obtained are confirmed with published results. A 100 MHz class E amplifier is demonstrated to verify the usefulness of the novel technique

in providing an excellent initial design. The analysis is then applied to the design of a novel class E frequency tripler to generate explicit closed-form design equations. The performance of the new design is then compared to conventional class E triplers.

Chapter 3 details the design and simulation of three different implementations of the 3 GHz frequency tripler as proof of concept. Details of the design procedure including device selection and characterisation and microstrip implementation of the input and output matching circuits are provided. Simulated results of the triplers highlight the merits of each of the designs, and their capability for high efficiency and high conversion gain operation.

Chapter 4 presents the first ever practical demonstration of higher order (> x2) class E multipliers. It details the fabrication procedure of the novel class E triplers developed in the preceding chapter, and describes the experimental test and measurement of the hybrid MIC implemented triplers. Measurements of the three circuits show the highest reported drain efficiencies of 59.7 %, 47 % and 29 % are achieved, along with unprecedented conversion gain of 7.22 dB, 6.8 dB and 1.8 dB respectively, thus demonstrating the powerful capabilities of the proposed design in terms of achieving simultaneous high drain efficiency and conversion gain.

Chapter 5 concludes the work carried out in this thesis and offers a direction for future investigations that may be carried out for further development of the novel class E multiplier.

Chapter 2

Class E Circuit Analysis

2.1 Introduction

Switched mode Class E networks were introduced by Sokal and Sokal in 1975 [63, 64]. They offer high achievable efficiency, low sensitivity to device characteristics, and a priori designability arising from explicit design equations for the load network. These networks operate the active device as a switch, and offer exceptionally high achievable $\eta_{DC/RF}$ through specific response of the output load network. The output network is designed to provide time domain waveform shaping of the switch voltage and current at the device such that they are not only displaced in time from each other but also the switching losses between ON and OFF states are minimised. The conditions for Class E operation have been defined as [64]:

- The rise in voltage across the switch (device) during the off-period is delayed until after the device is switched off.
- The switch voltage returns to zero at the time of switch (device) turn on.
- The gradient of the voltage should be zero at the time of switch (device) turn on.

A simplified schematic of a Class E network is shown in Figure 2.1, and it can be seen that a distinct advantage offered by Class E networks resides in the fact that the parasitic capacitance of the device can be absorbed into the output load network. The network is tuned to eliminate the cyclic power dissipation that can occur with the charging and discharging of the shunt capacitance [65] through the switch resistance,

and is accomplished by fulfilling the above criteria for Class E operation. The first condition ensures that there is minimal overlap between switch voltage and current. The second condition ensures that the voltage across the switch (and hence the shunt capacitance) is zero at the time of switch turn on. Any residual voltage at turn-on discharges through the switch which results in dissipating the stored energy of $\frac{1}{2}CV^2$. The third condition ensures that at the start of switch on, the current rises gradually from an initial value of zero.

An idealised analysis of Class E amplifiers based on simplifying assumptions (ideal switch, infinite output filter Q factor and RF choke in the DC supply) was first presented by Raab [66, 67] in 1977. Zulinski et al [47] followed suit in 1986 with an idealised analysis of Class E multipliers that was based on the analysis presented by Raab. These analyses, by the author's admission [66], are tedious, incorporating numerous variables with long and complex equations that do not inherently describe circuit behaviour. It is also mentioned, that the analysis does not guarantee an analytical solution, with some duty cycles or component values requiring a numerical solution through iteration. Several subsequent analyses followed that aimed to incorporate one or a combination of non-ideal effects such as finite DC feed [68, 69, 70], finite on resistance of the active device [71, 54], finite Q factor of the output network [72, 73, 74], and nonlinear output capacitance [75, 76]. These analyses whilst being informative, often require numerical iterative solutions with look-up tables for design variables. This detracts from the intuition that is required for initial design, and is more expensive to implement in terms of computational time. While these 'nonideal' analyses may provide more accurate results, with sophisticated analysis tools such as Harmonic Balance popularly used in the design of multipliers and available accurate nonlinear device models, an approximate design can suffice with the optimiser refining the performance for optimum design solution to provide a prudent compromise. Furthermore, once within the microwave and millimetre wave region, lumped components no longer behave ideally and depart from idealized components [77]. Parasitic elements of real lumped components cause resonances that can deteriorate the performance of the class E circuit as it requires multi-harmonic control for optimum performance. It can been seen in [78] for the design of pioneering transmission-line based class E amplifiers, that a first-order solution providing quick assessment and an intelligent initial design was much preferred

to the exact time-domain solution involving time-varying third-order set of differential equations.

With the focus of this work on a novel circuit configuration for a class E tripler, a simple yet accurate analysis was required for quick evaluation of circuit performance. Also, microwave transmission line implementations of the novel tripler was envisaged, and hence a first-order analysis to provide an intelligent initial design was required with harmonic balance being relied on further fine tuning for optimal design. The novel analysis presented in this work is a first-order time domain description of Class E networks that provides a more tangible treatment of circuit behaviour by better describing its operation and harmonic content of the output waveforms. The analysis is first applied for a Class E amplifier and the results are verified against previously published results in order to validate the analysis. Experimental verification is also provided in the design and measurement of a Class E amplifier, with a design frequency of 100 MHz in order to best illustrate the design equations. The analysis is shown to provide a valid basis for the design of optimum load networks, and the definitive treatment of the output harmonics makes the analysis ideal for formulating novel load networks. The technique is then used in the design and analysis of a Class E frequency tripler with 50% duty cycle. The results of the novel tripler are then compared to that of the conventional Class E tripler as defined in [47].

2.2 Analysis of Class E Amplifiers

A simplified schematic of a Class E amplifier is shown in Figure 2.1.

The active device is represented as an ideal switch, and its intrinsic output capacitance, C_{ds} is included in the shunt capacitance, C of the load network. This is followed by an output series LC resonator tuned to the fundamental switching frequency, and by a complex load impedance Z_L. The operation of the class E amplifier when the switch is OFF is determined by the transient response of the load network, and by the current flowing in the switch when it is ON. During the OFF interval, the current I_{DC} splits between the capacitor current I_c, and load current I_0. The capacitor C charges up and a voltage is produced across the capacitor and switch. The load network is designed to ensure that at the end of the OFF period, the voltage across the switch returns to

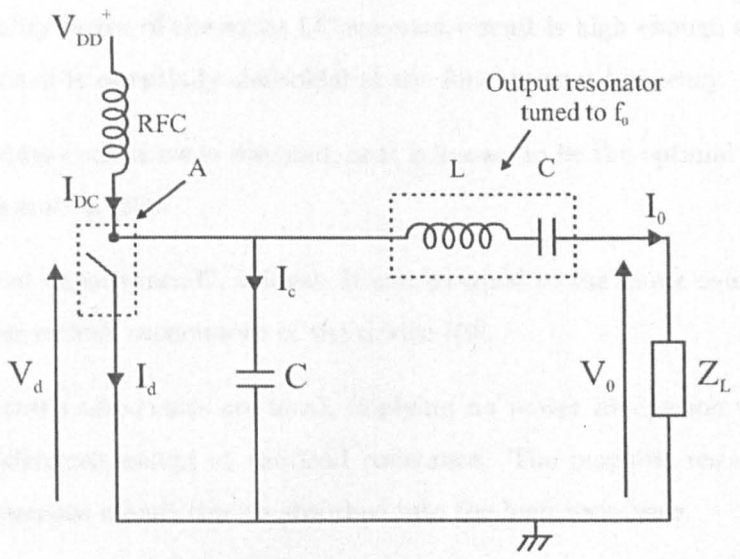


Figure 2.1: Simple equivalent circuit of a Class E amplifier.

zero with zero gradient. This ensures that at the ON transition, when the current I_{DC} is split between I_0 and drain current I_d, the switch voltage and current do not overlap and no charge is left stored in C to dissipate into the switch.

2.2.1 Assumptions

The assumptions for this analysis follow those suggested in [66, 47], and serve to concentrate the equations to the core operation of the circuit. A complicated exact time-domain Laplace solution can be found with fewer assumptions. However, as shown in [78], the equations are long and complicated thus detracting from the usefulness and insight gained from the analysis. A simpler analysis was developed in this work to obtain insightful results and for straightforward initial design of a class E amplifier.

The assumptions are as follows:

1. An infinite impedance RF choke is provided at the bias feed. This implies only DC flows through the bias line.

2. The active device operates as an ideal switch, with sufficiently low on-resistance such that the switch current and voltage remain unchanged, and fast enough switching times to allow the OFF-transition time to be neglected.

3. The quality factor of the series LC resonant circuit is high enough such that the load current is essentially sinusoidal at the fundamental frequency.

4. A 50% duty cycle drive is assumed, as it is known to be the optimal case for class E PA operation [66].

5. The shunt capacitance C, is ideal. It can be equal to the linear equivalent of the nonlinear output capacitance of the device [79].

6. The circuit components are ideal, implying no power dissipation occurs in the circuit elements except at the load resistance. The parasitic resistances of the series resonant circuit can be absorbed into the load resistance.

2.2.2 Derivation of Switch Current and Voltage Waveforms

The currents in the various branches of the circuit, namely drain current I_d, capacitor current I_c, and load current I_0 are described according to their harmonic content. From Figure 2.1, and the assumptions above, the following statements can be derived about the harmonic composition of the branch currents:

1. I_d contains all harmonics.

2. I_c does not contain any DC component.

3. I_0 contains only fundamental components.

Nodal analysis is then performed at node A, and the following expression relating the branch currents is obtained,

$$I_{DC} = I_d + I_c + I_0. \tag{2.1}$$

If the second harmonic and higher harmonic components are represented by $G_2(\theta)$, then I_d can be expressed as,

$$I_d = I_{DC} + A_1 \sin \omega t + A_2 \cos \omega t + G_2(\theta) \tag{2.2}$$

and,

$$I_c = B_1 \cos \omega t + B_2 \sin \omega t - G_2(\theta) \tag{2.3}$$

where, ω is the switching frequency in rads^{-1}, and $\theta = \omega t$. A_1 and A_2 are the coefficients of the fundamental component in the switch current, and B_1 and B_2 are the coefficients of the fundamental component in the capacitor current. Substituting (2.2) and (2.3) into (2.1) and evaluating at the fundamental, we obtain,

$$I_0 = -A_1 \sin \omega t - A_2 \cos \omega t - B_1 \cos \omega t - B_2 \sin \omega t \tag{2.4}$$

For a theoretical efficiency of 100%, the switch current and voltage are required to be displaced in time with no overlap for minimum dissipation of power at the device. This implies that the following conditions must be satisfied:

Switch ON: $I_c = 0$, for $0 \leq \theta \leq \pi$
Switch OFF: $I_d = 0$, for $\pi \leq \theta \leq 2\pi$

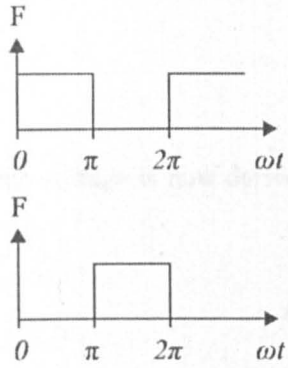
Therefore, from (2.2) and (2.3), during switch ON,

$$G_2(\theta) = B_1 \cos \omega t + B_2 \sin \omega t \tag{2.5}$$

and during switch OFF,

$$G_2(\theta) = -(I_{DC} + A_1 \sin \omega t + A_2 \cos \omega t) \tag{2.6}$$

The above expressions for $G_2(\theta)$ are relevant when the switch is on and off respectively, and can be combined by multiplying by the corresponding square wave functions shown in Figure 2.2 to produce a single expression for $G_2(\theta)$.



$$= \frac{1}{2} + \frac{2}{\pi}\left[\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t...\right]$$

$$= \frac{1}{2} - \frac{2}{\pi}\left[\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t...\right]$$

Figure 2.2: Harmonic composition of square waveforms for determining $G(2\theta)$.

This gives,

$$G_2(\theta) = (B_1\cos\omega t + B_2\sin\omega t).\left(\frac{1}{2} + \frac{2}{\pi}\left[\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t...\right]\right) - (I_{DC} + A_1\sin\omega t + A_2\cos\omega t).\left(\frac{1}{2} - \frac{2}{\pi}\left[\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t...\right]\right)$$

The above expression for $G_2(\theta)$ cannot contain any DC or fundamental components, as it represents the second and higher harmonic content. Therefore the DC terms, fundamental cosine and sine terms are equated to zero in order to determine the coefficients. A fourth relationship is obtained by considering the continuity of $G_2(\theta)$ at $t = 0$ and equating the two expressions for $\lim_{t\to 0} G_2(\theta)$. The coefficients are then solved in terms of I_{DC}, and are given below,

$$A_1 = \left(\frac{\pi^2+8}{4\pi}\right) I_{DC}, \quad A_2 = \frac{-I_{DC}}{2}, \quad B_1 = \frac{-I_{DC}}{2}, \quad B_2 = \left(\frac{\pi^2-8}{4\pi}\right) I_{DC}. \tag{2.7}$$

Expressions for the switch current and switch voltage can now be determined. During the on-period, from (2.1),

$$I_d = I_{DC} - I_0 \quad \text{for} \quad 0 < \theta < \pi \tag{2.8}$$

The coefficients in (2.7) are substituted into (2.8), and using (2.4) gives the switch current as,

$$I_d = I_{DC}\left(1 + \frac{\pi}{2}\sin\theta - \cos\theta\right). \tag{2.9}$$

Switch voltage is now derived as follows. During the off-period, from (2.1),

$$I_c = I_{DC} - I_0 \quad \text{for} \quad \pi < \theta < 2\pi \tag{2.10}$$

The switch voltage, V_d, across the shunt capacitance C is given by,

$$V_d(\theta) = \frac{1}{\omega C}\int_{\pi}^{\theta}(I_{DC} - I_0)d\theta. \tag{2.11}$$

Expanding the integral and substituting the coefficients gives,

$$V_d(\theta) = \frac{1}{\omega C}\left(I_{DC}\theta - \frac{3\pi I_{DC}}{2} - \frac{\pi I_{DC}}{2}\cos\theta - I_{DC}\sin\theta\right). \tag{2.12}$$

The switch waveforms are depicted in Figure 2.3 and it can be seen that the switch voltage and switch current waveforms do not overlap at the on/off transitions. The switch current waveform drops down to zero at the beginning of the off period, and similarly the voltage waveform drops to zero with zero gradient at the beginning of the on period.

The three specific criteria for optimum Class E operation as established in [63] for switch voltage and current are:

1. Rise in switch voltage across the active device must be delayed until the transistor is off.

2. Switch voltage must return to zero at the time of transistor turn-on.

3. The derivative of the switch voltage must be zero at turn-on.

Interpreting these criteria in (2.12), it can be shown that,

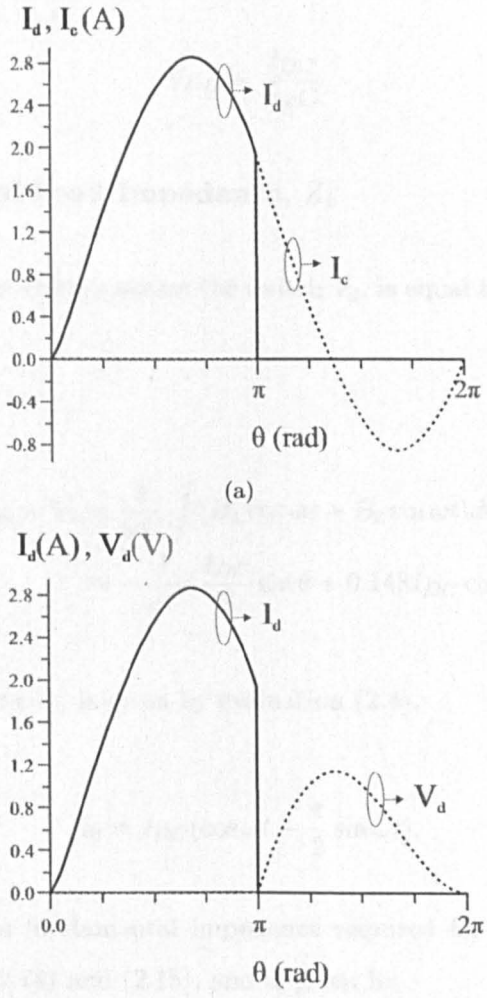


Figure 2.3: (a) Switch current I_d (solid), and capacitor current I_c (dashed) and (b) switch current I_d (solid), and switch voltage V_d (dashed) of a class E amplifier. (Normalised to $I_{DC} = 1$, $\omega C = 1$).

$$V_d|_{\theta=\pi} = 0, \;\; V_d|_{\theta=2\pi} = 0 \quad , \quad \left.\frac{dV_d}{d\theta}\right|_{\theta=2\pi} = 0.$$

This satisfies the conditions for optimum Class E operation and 100% theoretical efficiency.

The switch bias voltage V_{DD}, is the average of the switch voltage and is found from the DC component of the Fourier series of the switch voltage from (2.12),

$$V_{DD} = \frac{I_{DC}}{\pi\omega C} \tag{2.13}$$

2.2.3 Derivation of Load Impedance, Z_L

At the fundamental, the voltage across the switch V_d, is equal to the voltage across the load V_o, therefore,

$$\begin{aligned} V_d|_{f_0} = V_o &= \frac{1}{\omega C}\int (B_1 \cos\omega t + B_2 \sin\omega t)d\theta \\ &= -\frac{1}{\omega C}(\frac{I_{DC}}{2}\sin\theta + 0.148 I_{DC}\cos\theta). \end{aligned} \tag{2.14}$$

The fundamental current I_0, is given by evaluation (2.4),

$$I_0 = I_{DC}(\cos\omega t - \frac{\pi}{2}\sin\omega t). \tag{2.15}$$

Therefore the optimum fundamental impedance required for 100% efficiency can be found by the ratio of (2.14) and (2.15), and is given by,

$$Z_L = \frac{1}{\omega C}0.28015 e^{j48.97^\circ} \tag{2.16}$$

and agrees with the equations presented in [66] and [78].

2.2.4 Waveform Parameters

Peak switch current is derived by solving its derivative when equated to zero, and is given by,

$$I_{d,peak} = 2.86 I_{DC} \quad \text{at} \quad \theta = 2.138 \text{ rad} \tag{2.17}$$

Similarly, peak positive drain voltage is found to be,

$$V_{d,peak} = 3.569 V_{DD} \text{ at } \theta = 4.27 \text{ rad} \tag{2.18}$$

The maximum frequency at which a device can be operated and still obtain optimum Class E behaviour is determined by the maximum peak switch current that it can support. From (2.17) and (2.13),

$$\begin{aligned} f &= \frac{I_{DC}}{2\pi^2 C V_{DD}} \\ f_{max} &= \frac{I_{max}}{56.3 C V_{DD}}. \end{aligned} \tag{2.19}$$

2.2.5 Output Power

Output RF power at the fundamental frequency at the load is given by,

$$P_{out} = \frac{1}{2} I_{0,peak}^2 \cdot \Re(Z_L). \tag{2.20}$$

Substituting 2.17 and 2.13 in (2.20) we get,

$$\begin{aligned} P_{out} &= \frac{(1.86 I_{DC})^2}{2} \cdot 0.28015 \cdot \frac{1}{\omega C} \cos 48.9^\circ \\ &= \frac{I_{DC}^2}{\pi \omega C} \\ &= V_{DD}^2 \pi \omega C. \end{aligned} \tag{2.21}$$

The total DC power is given by,

$$\begin{aligned} P_{DC} &= I_{DC} \cdot V_{DD} \\ &= V_{DD}^2 \pi \omega C, \end{aligned} \tag{2.22}$$

and is equivalent to the fundamental RF output power dissipated at the load impedance given in (2.21), thus implying 100% DC-to-RF efficiency.

2.3 Experimental Verification - Class E Amplifier

The results obtained were verified with the design and fabrication of a pHEMT class E amplifier. In order to best elucidate the design equations, 100 MHz was chosen as the design frequency and the amplifier was implemented with lumped components.

The device used was the Filtronic 0.25 μm LP6836 SOT343 pHEMT packaged device. The gate was biased at the pinch-off voltage of -1.2 V and drain was biased at 2 V. The input network was designed to provide a conjugate match to the input impedance of the device at the fundamental switching frequency for maximum power transfer and hence efficient switching of the device. The output load network includes an additional shunt capacitance of 2 pF to supplement the 0.103 pF C_{ds} of the device for a higher output power. This is followed by a series resonant circuit tuned at the fundamental switching frequency. This is followed by the optimum load reactance of 0.25 μH as calculated in (2.16), and an output matching network to transform the optimised load resistance of 127 Ω to 50 Ω, as shown in Figure 2.4. The parasitic resistances associated with the lumped inductors are shown, as they contribute to the optimum load resistance as calculated in (2.16).

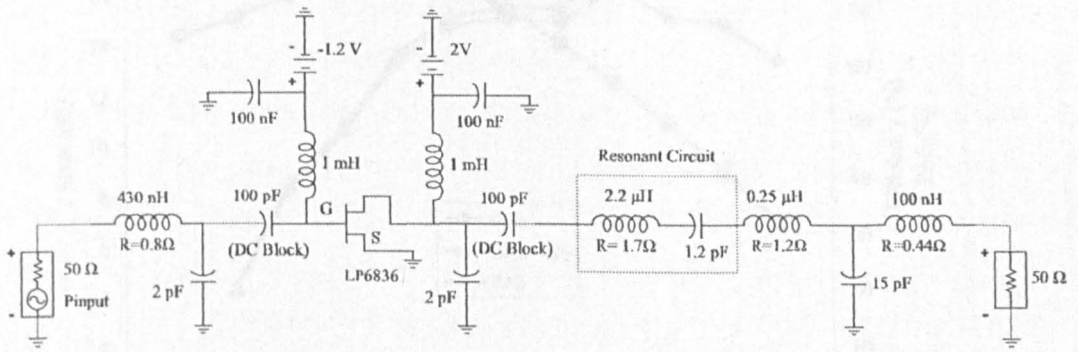


Figure 2.4: Schematic layout of the fabricated 100 MHz lumped class E amplifier.

Measured performance of the amplifier is given in Figures 2.6 and 2.7. A maximum PAE of 73 % and a drain efficiency of 78 % was achieved with an output power of 10 dBm and a gain of 12.6 dB. A simultaneous second harmonic suppression of 54 dBc was

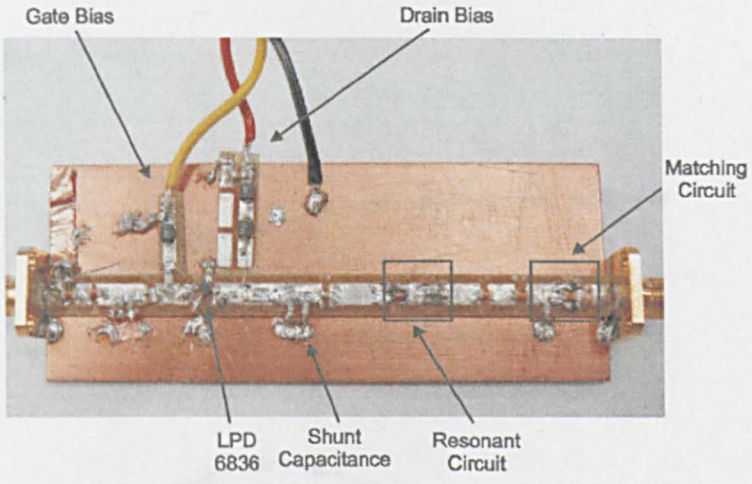


Figure 2.5: Photograph of the fabricated 100 MHz class E amplifier.

also achieved. These results demonstrate that the first-order design theory provides an excellent foundation for high efficiency amplifier design. The treatment is also highly suited for higher frequency designs as an intelligent starting point for determining the required harmonic impedances to be presented at the output of the device.

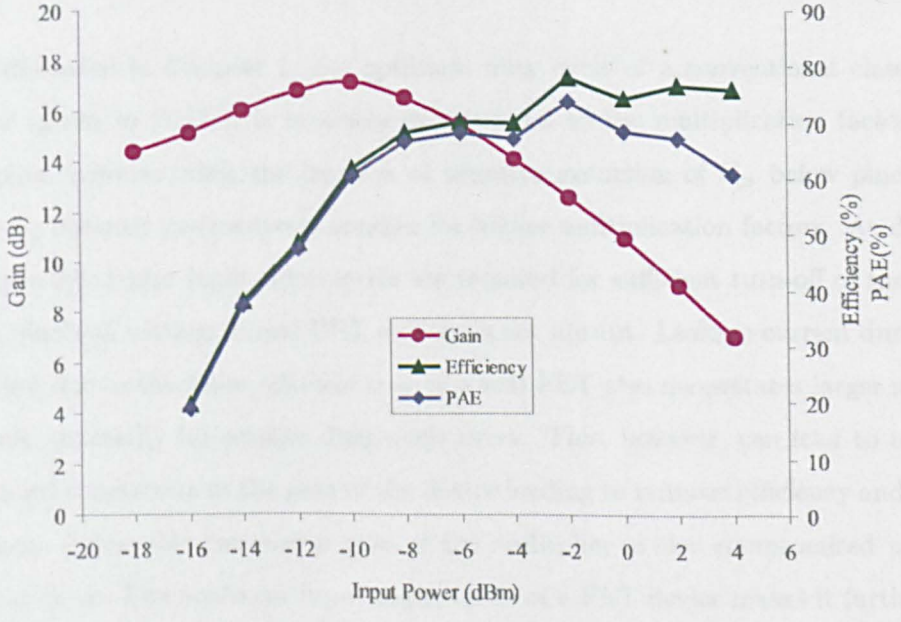


Figure 2.6: Measured results of the fabricated 100 MHz lumped class E amplifier.

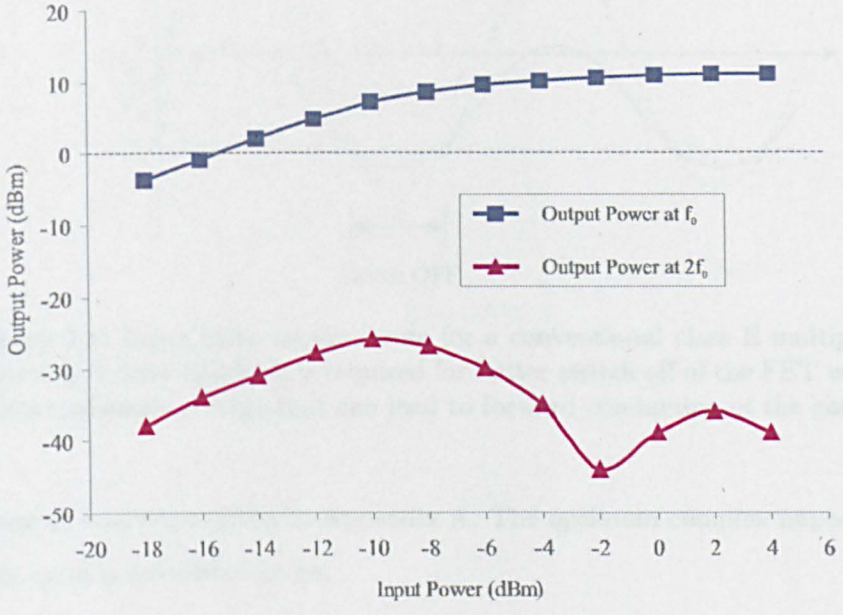


Figure 2.7: Measured results of the fabricated 100 MHz lumped class E amplifier.

2.4 Overview of Conventional Class E Tripler

As discussed in Chapter 1, the optimum duty cycle of a conventional class E multiplier (given in (1.17)), is inversely proportional to the multiplication factor, N. This implies, however, that the fraction of negative excursion of V_{gs} below pinch-off voltage V_p becomes progressively smaller for higher multiplication factors. As depicted in Figure 2.8, larger input drive levels are required for sufficient turn-off of the device as the pinch-off voltage in real FET devices is not abrupt. Leakage current during the off period due to the finite off-resistance of a real FET also necessitates larger input drive levels, especially for smaller duty cycle drive. This, however, can lead to undesirable forward conduction of the gate of the device leading to reduced efficiency and reliability issues. Achievable conversion gain of the multiplier is also compromised with higher input drive. The nonlinear input capacitance of a FET device makes it further difficult to achieve the correct fractional duty cycle without a degree of trial and error [51].

The analysis presented in section 2.2, was applied to a conventional class E tripler. The

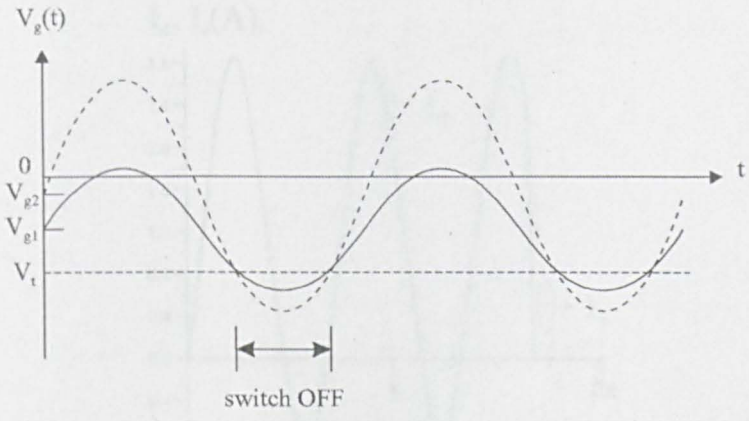


Figure 2.8: Input drive requirements for a conventional class E multiplier showing a larger input drive (dashed) is required for better switch off of the FET with consequent higher maximum voltage that can lead to forward conduction of the gate.

complete analysis is given in Appendix A. The optimum complex impedance at 16.7% duty cycle is calculated to be,

$$Z_L = \frac{1}{3\omega C} 0.0934 e^{j49.05^\circ}, \tag{2.23}$$

where, as before, ω is the fundamental switching frequency and C is the shunt capacitance across the switch as shown in Figure 1.16. The switch voltage and current waveforms are shown in Figure 2.9, and highlight a second disadvantage with the topology. The switch current is shown to be negative for certain parts of the cycle.

A typical IV characteristic of a FET is given in Figure 2.10, and shows that with negative drain current, a noticeable amount of drain voltage appears across the switch due to the on-resistance of the FET. This will cause the switch current and voltage to exist simultaneously causing dissipation at the switch and reduced efficiency. It can be seen in Figure 2.10 that a more suitable dynamic loadline would utilise the positive and negative swing of V_{ds} and only the positive swing of I_{ds} to minimise the power dissipated at the FET.

Further potential problems arise from the switch current waveform shown in Figure 2.4. Peak positive switch current occurs at $\theta = 0.71$ radians, 2.81 radians and 4.90 radians. Assuming peak current coincides with I_{max} of the active device (I_{DS} at $V_{GS} = 0$) for maximum output power and optimum utilisation of the device, the drive waveform

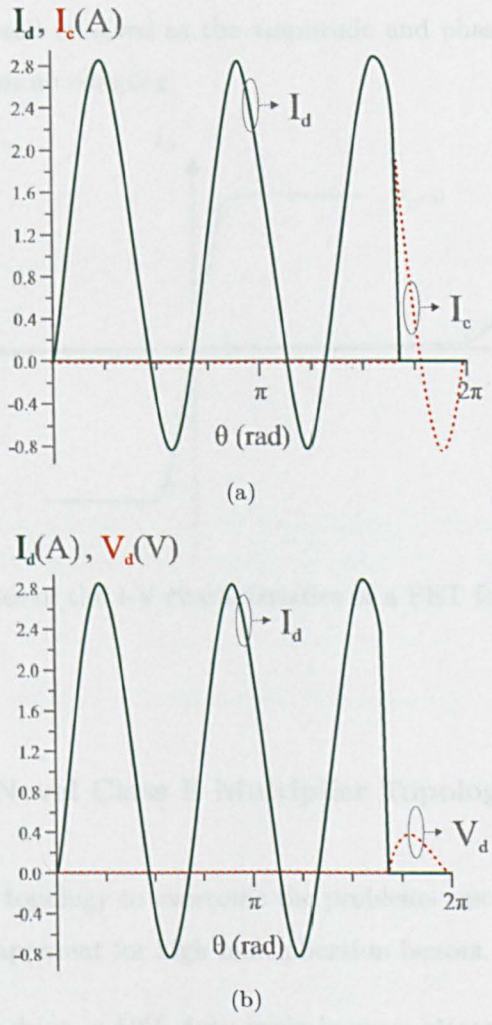


Figure 2.9: (a) Switch current I_d (solid), and capacitor current I_c (dashed) and (b) switch current I_d (solid), and switch voltage V_d (dashed) of the conventional class E tripler with 16.7% duty cycle. (Normalised to $I_{DC} = 1$, $\omega C = 1$).

must therefore continuously provide the required input voltage to sustain the three peaks in current. This implies that a rectangular input drive, instead of a sinusoidal one, is required with a peak voltage of $V_{gs} = 0$ if deterioration in performance is to be avoided. It will be shown later on that the sinusoidal input drive is severely distorted by the nonlinear input capacitance (C_{gs}) of a FET, and that this nonlinearity can be exploited to tailor the input waveform to a more desirable shape. An approximation to a square drive function can be simply achieved by biasing the FET at V_p and providing short circuit terminations at the second and fourth harmonics. However, manipulating the harmonics to achieve a rectangular drive waveform with much smaller duty cycle

is much more complex and involved as the amplitude and phase relationship between the harmonics is much more complex.

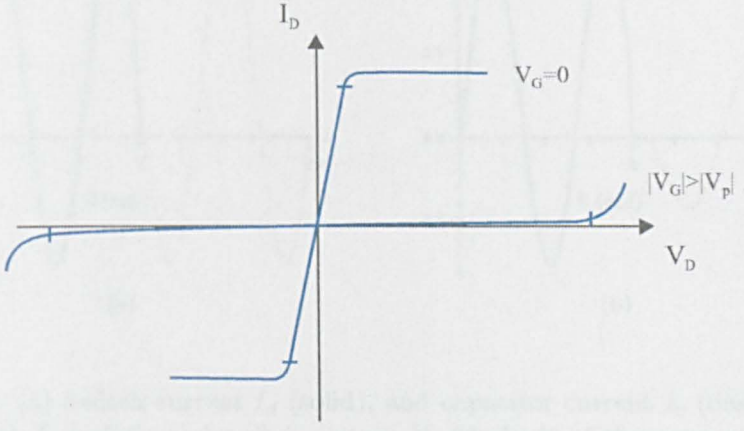


Figure 2.10: Boundaries of the I-V characteristics of a FET for operation as a switch [80].

2.5 Overview of Novel Class E Multiplier Topology

We now present a new topology to overcome the problems associated with the conventional case, especially apparent for high multiplication factors.

With regards to input drive, a 50% duty cycle is more attractive in terms of ease of practical implementation. However, in the case of the conventional class E multiplier a 50% duty cycle is much above the predicted limit of $\frac{1}{N}$ beyond which the load angle is close to 90° ([47]), i.e. a purely reactive load. The required complex load is calculated to be,

$$Z_L = \frac{1}{3\omega C} 0.457 e^{j88.9^\circ}, \tag{2.24}$$

The associated waveforms are shown in Figure 2.11, and the drain current can be seen to be both positive and negative. This, as described above, causes simultaneous existence of drain current and voltage of a practical FET as predicted by its IV characteristics.

The novel topology, shown in Figure 2.12, allows for a realisable load with a 50% duty cycle drive by introducing a fundamental short circuit trap in the load network, to

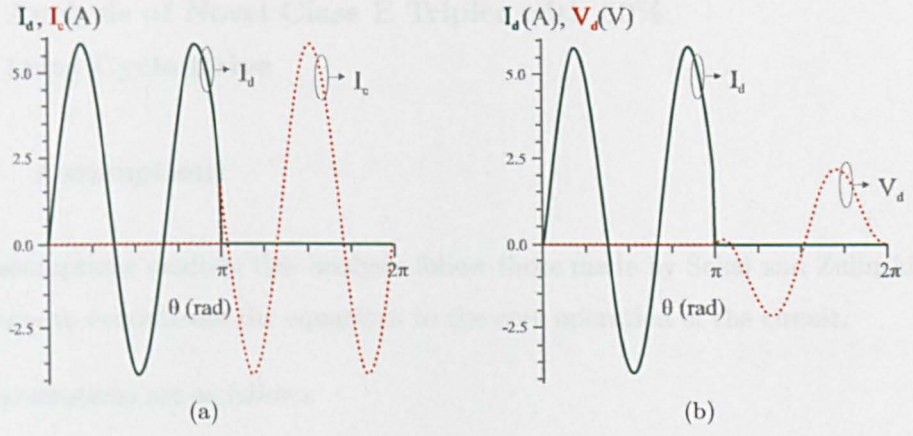


Figure 2.11: (a) Switch current I_d (solid), and capacitor current I_c (dashed) and (b) switch current I_d (solid), and switch voltage V_d (dashed) of the conventional class E tripler with 50% duty cycle. (Normalised to $I_{DC} = 1$, $\omega C = 1$).

provide a fundamental switching component in the drain current.

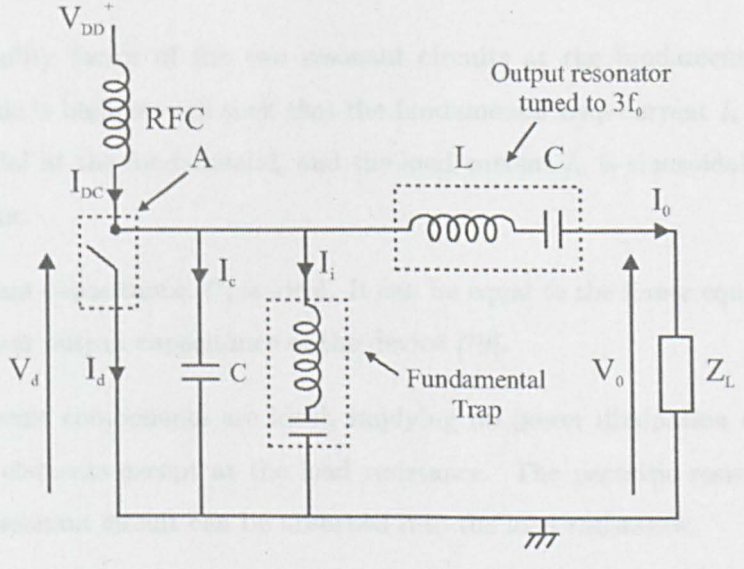


Figure 2.12: Idealized circuit of the proposed Class E tripler.

The quantitative analysis previously described for the case of the class E amplifier is easily applied to the new topology and is detailed in the next section. It is will be shown that this topology utilises the more attractive dynamic load-line of positive/negative V_{ds} and a positive I_d, which as can be seen from Figure 2.10 would result in a more suitable mode of operation to achieve high efficiency.

2.6 Analysis of Novel Class E Tripler with 50% Duty Cycle Drive

2.6.1 Assumptions

The assumptions made in this analysis follow those made by Sokal and Zulinski [9,13] and serve to concentrate the equations to the core operation of the circuit.

The assumptions are as follows:

1. An infinite impedance RF choke is provided at the bias feed. This implies only DC flows through the bias line.
2. The active device operates as an ideal switch, with sufficiently low on-resistance such that the switch current and voltage remain unchanged, and fast enough switching times to allow the OFF-transition time to be neglected.
3. The quality factor of the two resonant circuits at the fundamental and third harmonic is high enough such that the fundamental trap current I_i is essentially sinusoidal at the fundamental, and the load current I_0 is sinusoidal at the third harmonic.
4. The shunt capacitance, C, is ideal. It can be equal to the linear equivalent of the non-linear output capacitance of the device [79].
5. The circuit components are ideal, implying no power dissipation occurs in the circuit elements except at the load resistance. The parasitic resistances of the series resonant circuit can be absorbed into the load resistance.

2.6.2 Derivation of Switch Current and Voltage Waveforms

The currents in the different branches of the circuit shown in Figure 2.12, namely drain current I_d, capacitor current I_c, fundamental trap current I_i, and load current I_0 are described according to their harmonic content. From Figure 2.12, and the assumptions above, the following statements can be made about the harmonic composition of the branch currents:

1. I_d contains all harmonics.
2. I_c does not contain any DC component.
3. I_i contains only fundamental components.
4. I_0 contains only third harmonic components.

Nodal analysis is then performed at node A, and the following expression relating the branch currents is obtained,

$$I_{DC} = I_d + I_c + I_i + I_0. \tag{2.25}$$

If we represent the fourth harmonic and higher harmonic components by $G_4(\theta)$, which is a function of ωt, then I_d can be expressed as:

$$\begin{aligned} I_d = I_{DC} &+ A_1 \sin \omega t + A_2 \cos \omega t + B_1 \sin 2\omega t \\ &+ B_2 \cos 2\omega t + C_1 \sin 3\omega t + C_2 \cos 3\omega t \\ &+ G_4(\theta) \end{aligned} \tag{2.26}$$

and,

$$\begin{aligned} I_c = &- B_1 \sin 2\omega t - B_2 \cos 2\omega t + E_1 \sin 3\omega t \\ &+ E_2 \cos 3\omega t - G_4(\theta) \end{aligned} \tag{2.27}$$

where, ω is the switching frequency in rads^{-1}, A_1 and A_2 are the coefficients of the fundamental component in the switch current, B_1 and B_2 are the coefficients of the second harmonic and C_1 and C_2 are the coefficients of the third harmonic. E_1 and E_2 are coefficients of the third harmonic in the current through the capacitor. Substituting (2.26) and (2.27) into (2.25), and evaluating at the fundamental we obtain:

$$I_i = -A_1 \sin \omega t - A_2 \cos \omega t \tag{2.28}$$

For a theoretical efficiency of 100%, we require that the switch current and voltage are displaced in time and do not overlap for minimum dissipation of power at the device. This implies that the following conditions must be satisfied:

Switch ON: $I_c = 0$, for $0 \leq \theta \leq \pi$

Switch OFF: $I_d = 0$, for $\pi \leq \theta \leq 2\pi$

where $\theta = \omega t$. Therefore, from (2.26) and (2.27), during switch ON:

$$G_4(\theta) = -B_1 \sin 2\omega t - B_2 \cos 2\omega t + E_1 \sin 3\omega t + E_2 \cos 3\omega t$$

and during switch OFF:

$$\begin{aligned} G_4(\theta) = -I_{DC} &- A_1 \sin \omega t - A_2 \cos \omega t - B_1 \sin 2\omega t \\ &- B_2 \cos 2\omega t - C_1 \sin 3\omega t - C_2 \cos 3\omega t. \end{aligned}$$

The above expressions for $G_4(\theta)$ are relevant when the switch is on and off respectively, and can be combined by multiplying by the corresponding square wave functions shown in Fig. 2.2 to produce a single expression for $G_4(\theta)$.

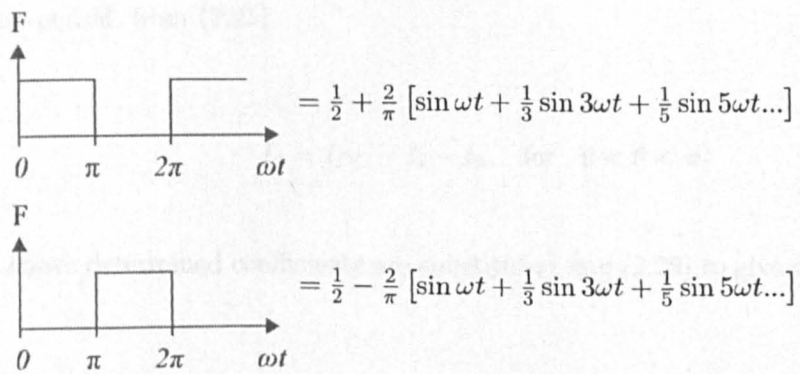


Figure 2.13: Harmonic composition of square waveforms in order to determine $G_4(\theta)$.

This gives,

$$
\begin{aligned}
G_4(\theta) = \\
&(-B_1 \sin 2\omega t - B_2 \cos 2\omega t + E_1 \sin 3\omega t + E_2 \cos 3\omega t) \\
&\cdot \left(\frac{1}{2} + \frac{2}{\pi}\left[\sin \omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t ...\right]\right) - \\
&(I_{DC} + A_1 \sin \omega t + A_2 \cos \omega t + B_1 \sin 2\omega t \\
&+ B_2 \cos 2\omega t + C_1 \sin 3\omega t + C_2 \cos 3\omega t) \\
&\cdot \left(\frac{1}{2} - \frac{2}{\pi}\left[\sin \omega t + \frac{1}{3}\sin \omega t + \frac{1}{5}\sin 5\omega t ...\right]\right)
\end{aligned}
$$

The above expression for $G_4(\theta)$ cannot contain any DC, fundamental, second harmonic or third harmonic components, as $G_4(\theta)$ represents the fourth and higher harmonic content. Therefore the cosine and sine terms of these components in $G_4(\theta)$ are equated to zero to determine the coefficients. An eighth relationship is obtained by considering the continuity of $G_4(\theta)$ at $t = 0$ and equating the two expressions for $\lim_{t\to 0} G_4(\theta)$. The coefficients are then solved in terms of I_{DC}, and are given as,

$$
\begin{aligned}
&A_1 = \tfrac{4I_{DC}}{\pi}, && A_2 = 0, && B_1 = \tfrac{4I_{DC}}{5\pi}, \\
&B_2 = \tfrac{I_{DC}(27\pi^2-256)}{15\pi^2}, && C_1 = \tfrac{I_{DC}(9\pi^2-64)}{12\pi}, && C_2 = \tfrac{-I_{DC}}{2}, \\
&E_1 = \tfrac{I_{DC}(9\pi^2-80)}{12\pi}, && E_2 = \tfrac{-I_{DC}}{2}.
\end{aligned}
$$

Expressions for the switch current and switch voltage can now be determined. During the on-period, from (2.25),

$$I_d = I_{DC} - I_i - I_0 \quad \text{for} \quad 0 < \theta < \pi \tag{2.29}$$

The above determined coefficients are substituted into (2.29) to give the switch current as:

$$I_d(\theta) = I_{DC}(1 + 1.2732 \sin \theta + 0.8926 \sin 3\theta - \cos 3\theta) \tag{2.30}$$

During the off-period, from (2.25):

$$I_c = I_{DC} - I_i - I_0 \quad \text{for} \quad \pi < \theta < 2\pi \tag{2.31}$$

The switch voltage, V_d, across the shunt capacitance, C is given by,

$$V_d(\theta) = \frac{1}{\omega C} \int_{\pi}^{\theta} (I_{DC} - I_i - I_0) d\theta$$

Expanding the integral and substituting in the coefficients gives,

$$V_d(\theta) = \frac{1}{\omega C} \left(I_{DC}\theta - 1.2732 I_{DC} \cos\theta - 0.2975 I_{DC} \cos 3\theta - \frac{I_{DC}}{3} \sin 3\theta - \frac{3\pi}{2} I_{DC} \right) \tag{2.32}$$

The switch waveforms are depicted in Figure 2.14 and it can be seen that the switch voltage and switch current waveforms do not overlap at the on/off transitions. The switch current waveform drops down to zero at the beginning of the off period, and similarly the voltage waveform drops to zero with zero gradient at the beginning of the on period.

The three specific criteria for optimum Class E operation as established in [66] for switch voltage and current are:

1. Rise in switch voltage across the active device must be delayed until the transistor is off.
2. Switch voltage must return to zero at the time of transistor turn-on.
3. The derivative of the switch voltage must be zero at turn-on.

Interpreting these criteria in (2.32), it is seen that,

$$V_d|_{\theta=\pi} = 0, \quad V_d|_{\theta=2\pi} = 0 \quad , \quad \left.\frac{dV_d}{d\theta}\right|_{\theta=2\pi} = 0$$

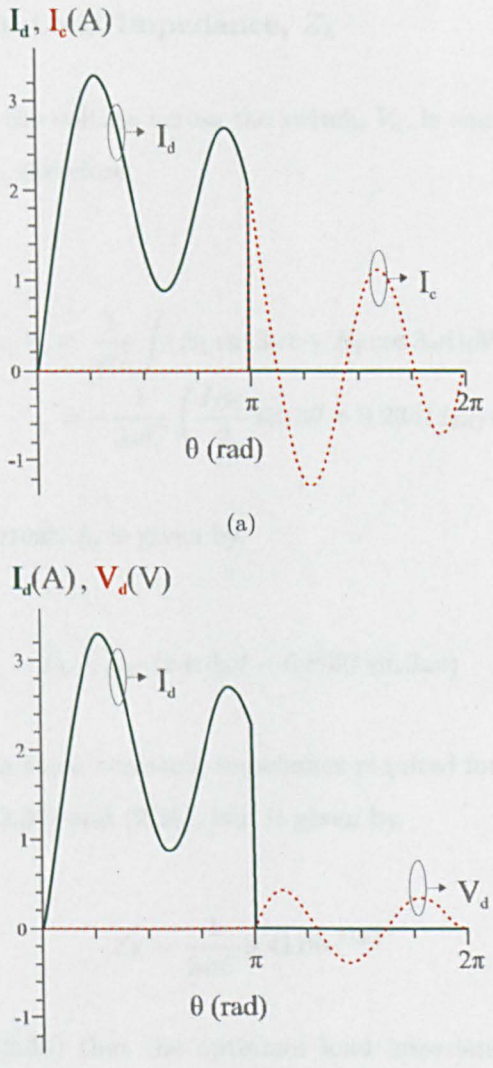


Figure 2.14: (a) Switch current I_d (solid), and capacitor current I_c (dashed) and (b) switch current I_d (solid), and switch voltage V_d (dashed) of the novel class E tripler. (Normalised to $I_{DC} = 1$, $\omega C = 1$).

This satisfies the conditions for optimum Class E operation and 100% theoretical efficiency.

The switch bias voltage V_{DD}, is the average of the switch voltage and is found from the DC component of the Fourier series of the switch voltage from (2.32), and is given by,

$$V_{DD} = \frac{I_{DC}}{9\pi\omega C} \tag{2.33}$$

2.6.3 Derivation of Load Impedance, Z_L

At the third harmonic, the voltage across the switch, V_d, is equal to the voltage across the load impedance, V_0, therefore,

$$\begin{aligned} V_d|_{3f_0} = V_0 &= \frac{1}{\omega C}\int (E_1 \sin 3\omega t + E_2 \cos 3\omega t)d\theta \\ &= -\frac{1}{3\omega C}\left(\frac{I_{DC}}{2}\sin 3\theta + 0.2341 I_{DC}\cos 3\theta\right) \end{aligned} \tag{2.34}$$

The third harmonic current, I_0 is given by,

$$I_0 = I_{DC}(\cos 3\omega t - 0.8927 \sin 3\omega t) \tag{2.35}$$

Therefore, the optimum third harmonic impedance required for 100% efficiency can be found by the ratio of (2.34) and (2.35), and is given by,

$$Z_L = \frac{1}{3\omega C} 0.4118 e^{j73.3^\circ} \tag{2.36}$$

It can be seen from (2.36) that the optimum load impedance is dependent on the *fundamental* switching frequency, ω, and the shunt capacitance, C. With a 50% duty cycle drive, the load angle required for class E operation is 73.3°, and is an improvement on the near unrealizable load angle of 88.9° obtained for conventional class E multipliers with the same drive.

Figure 2.15 compares the optimum impedance as a function of C presented by the output network to the device for the conventional and proposed class E tripler. It can be seen that for higher values of C and hence output power, the optimum impedance at the required harmonic rapidly approaches the vicinity of a short circuit for the conventional tripler. This poses further problems as small values of load resistance R, are difficult to realise accurately and to match to 50Ω. Furthermore for small load resistances, parasitic resistances in the circuit form larger fractions of the optimum load and can be detrimental to the drain efficiency.

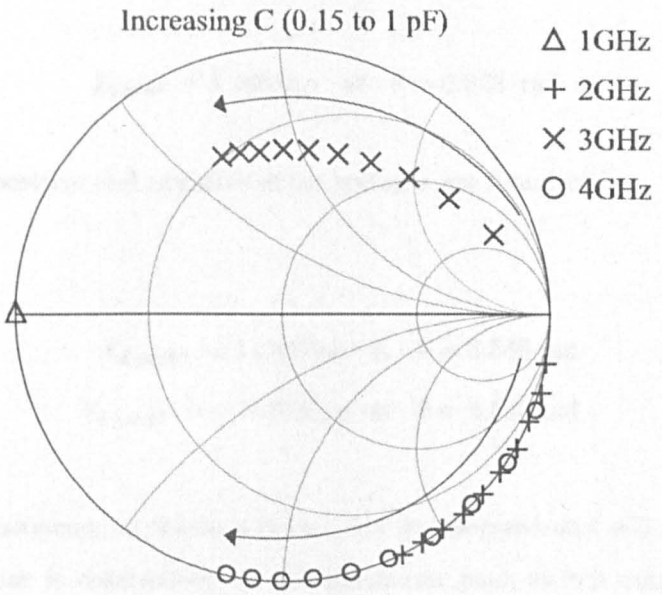


Figure 2.15: Optimum impedances of the required harmonic at 3 GHz and unwanted harmonics at 1 GHz, 2 GHz, and 4 GHz as a function of output shunt capacitance C in the load network for the novel class E tripler.

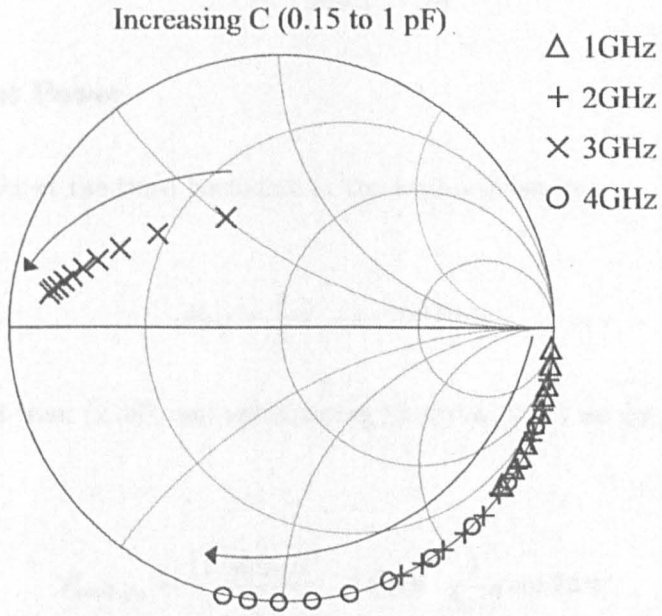


Figure 2.16: Optimum impedances of the required harmonic at 3 GHz and unwanted harmonics at 1 GHz, 2 GHz, and 4 GHz as a function of output shunt capacitance C in the load network of the conventional class E tripler.

2.6.4 Waveform Parameters

Peak switch current is found by equating the second derivative of (2.30) to zero, and is given as,

$$I_{d,peak} = 3.288 I_{DC} \quad \text{at} \quad \theta = 0.873 \text{ rad} \tag{2.37}$$

Similarly, peak positive and negative drain voltages are found to be,

$$V_{d,peak+} = 11.89 V_{DD} \quad \text{at} \quad \theta = 3.549 \text{ rad} \tag{2.38}$$

$$V_{d,peak-} = -11.05 V_{DD} \quad \text{at} \quad \theta = 4.533 \text{ rad} \tag{2.39}$$

The maximum frequency at which a device can be operated and still obtain optimum Class E behaviour is determined by the maximum peak switch current that it can support. From (2.37) and (2.33),

$$f_{max} = \frac{I_{max}}{584.1 C V_{DD}} \tag{2.40}$$

2.6.5 Output Power

Output RF power at the third harmonic at the load is given by,

$$P_{out} = \frac{1}{2} I_{0,peak}^2 \cdot Re(Z_L). \tag{2.41}$$

$I_{0,peak}$ is derived from (2.35), and substituting (2.33) in (2.41) we get,

$$\begin{aligned} P_{out|3f_0} &= \frac{(1.34 I_{DC})^2}{2} \cdot 0.4118 \cdot \frac{1}{3\omega C} \cos 73.3^\circ \\ &= 9\pi\omega C V_{DD}^2 \end{aligned} \tag{2.42}$$

The above derived expression for output power is equivalent to that of the conventional case with an optimal duty cycle of 16.7%. (2.42) demonstrates that operating the novel tripler at 50% duty cycle does not result in a reduction of output power as is in the case of a conventional tripler (Figure 1.18).

The total DC power is the product of I_{DC} and V_{DD},

$$P_{DC} = 9\pi\omega C V_{DD}^2,$$

and is equivalent to (2.42), thus implying 100% DC-to-RF efficiency.

Output power at the third harmonic, given in (2.42), is inversely proportional to both shunt capacitance, C and drain bias voltage, V_{DD}. V_{DD}, in turn, determines the peak switch voltage as given in (2.38) and (2.39), and is set following practical limitations imposed by the active device. Output power is then controlled by shunt capacitance C, and is limited by the maximum frequency the device can be operated at for optimum class E behaviour, as given in (2.40). These limitations are discussed in chapter 3.

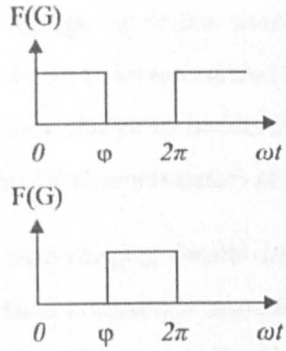
2.7 Analysis of General Switching circuit operating at any Duty cycle

The quantitative analysis has been demonstrated for both class E amplifiers and frequency multipliers. Its usefulness in devising novel circuit topologies and quick evaluation of circuit performance has also been established with the design of a novel class E tripler in Section 2.6. The adaptability of this analysis is evident and implies that it can be applied to any ideal switching circuit operating at any duty cycle to determine closed-form design equations for the load network for 100% $\eta_{DC/RF}$.

Equations relating the currents in the various branches of a specified circuit are first obtained using Kirchoff's law, and then the currents expressed according to their harmonic content. The analysis can then be performed as detailed in Sections 2.2 and 2.6, and utilising expressions shown in Figure 2.17 for a general duty cycle of $\frac{\phi}{2\pi}$.

2.8 Conclusions

A novel approach to class E circuit analysis has been presented in this chapter. The results of this analysis are definitive closed-form design equations which are directly related to actual design components of the load network, and lend themselves to immediate design of class E circuits. It was shown to be easily adaptable to variable



$$= \frac{\phi}{2\pi} + \sum_{n=1}^{\infty} \left(\frac{\sin n\phi}{n\pi} \cos n\omega t - \frac{1-\cos n\phi}{n\pi} \sin n\omega t \right)$$

$$= 1 - \frac{\phi}{2\pi} + \sum_{n=1}^{\infty} \left(\frac{-\sin n\phi}{n\pi} \cos n\omega t - \frac{\cos n\phi - 1}{n\pi} \sin n\omega t \right)$$

Figure 2.17: Harmonic composition of any switching function with a duty of $\frac{\phi}{2\pi}$.

parameters such as drive duty cycle and circuit topology. The first-order analysis was applied to the case of class E amplifiers in order to validate the analysis. It was experimentally demonstrated in the successful design of a 100 MHz class E amplifier, thus establishing the usefulness of the analysis in providing an intelligent and accurate starting point for the design of class E circuits.

The analysis was then used in the mathematical description of conventional class E triplers, and the waveforms obtained highlight the potential problems with the practical implementation of conventional higher order class E multipliers. The smaller duty cycles associated with higher order multipliers for optimum operation, pose a problem with practical implementation of the drive to the device. It is shown that obtaining sufficient turn-off of the device will result in potential forward gate conduction of the device, with higher order multipliers posing a greater risk. A more suitable duty cycle drive of 50% is shown to be sub-optimal, with the required complex load purely reactive. Also shown, is that although the switch waveforms of the conventional circuit theoretically provide high efficiency, they may not necessarily be the optimum waveforms for practical high efficiency operation, as shown in Figure 2.10. The derived waveforms also indicate that a sinusoidal drive will not be optimum to support the switch current waveform as three peaks exist throughout the on period. A rectangular waveform is needed; however, it is more difficult to obtain and can result in higher complexity of the drive circuitry.

A novel class E tripler was proposed to mitigate the problems associated with the conventional circuit. The tripler incorporates a fundamental short circuit termination in the load network to allow the circuit to operate with a 50% duty cycle drive. Closed-

form design equations were derived for the novel tripler, and the optimum load angle was shown to be realisable (73°). The associated switch waveforms were also determined and were shown to be ideally suited for practical high efficiency operation with regards to the IV characteristics of a FET.

The next chapter details design considerations for the proposed class E tripler based on practical limitations imposed by a non-ideal device in a real world environment. These considerations are derived *a priori* with the aid of predicted circuit behaviour from the analysis together with practical measurement of the non-linear active device to be used for the design. The design of three microstrip triplers at 3 GHz is then presented along with simulated performance.

Chapter 3

Novel Class E Tripler - Design Techniques

3.1 Introduction

The quantitative analysis presented in the preceding chapter provided a rapid and in-depth evaluation of class E circuit performance. A firm establishment of expected circuit behaviour and a good preliminary design was obtained for the novel class E tripler that is proposed in this work. The techniques and design considerations involved in translating the ideal circuit design to a practical implementation are addressed in this chapter.

Harmonic balance is predominately used for nonlinear analysis of the triplers, with harmonic balance lending credence to the analysis described in Chapter 2, and the analysis equally certifying the harmonic balance result for improved level of confidence in the simulation [81]. As discussed previously, a detailed analytical treatment involving fewer idealised assumptions may provide more device-specific, accurate results than a first order analysis. However, the numerical iterations and complex Fourier analysis involved makes this approach both expensive and time consuming. Moreover, since advanced harmonic balance algorithms are incorporated into most nonlinear simulation packages, an initial design developed using idealising factors can be refined to a real device solution.

An accurate and verified large-signal device model is an essential requisite for the above approach. The model chosen to represent the device must incorporate all nonlinear mechanisms that strongly affect circuit performance. This chapter includes an assessment of the device and associated large signal model, along with validation of the model

through measurement of the device.

Important design considerations for the input and output matching networks are also examined in this chapter, along with bias selection and bias feedline design for successful implementation of a microstrip tripler. Finally, three different microstrip circuit implementations with detailed design techniques for a 3 GHz tripler on RT/Duroid 5880 are presented. This is the first reported demonstration of a microwave class E frequency tripler, and involves unique microstrip design techniques for the design of class E circuits.

3.2 Active Device and Nonlinear Model

As previously discussed, the chosen active device must operate as a switch for Class E operation. This requires a low-loss device capable of high speed switching times at the fundamental frequency of operation. The device must also be bi-directional in order to support the positive and negative swing of the switch voltage as shown in Figure 2.9. Taking these criteria into consideration, pHEMT technology was chosen to implement the switch. This is particularly attractive due to their fast achievable switching times, low insertion loss and low phase noise owing to the improved carrier transport properties of the 2DEG layer in the device structure [1]. Additionally, this technology has the capacity to support both positive and negative drain voltage with negligible current drawn for high efficiency operation. Contrary to that reported in [47, 51], FET devices are capable of supporting both positive and negative drain voltage with no catastrophic damage to the device, provided adequate gate bias is provided. As discussed in Chapter 2, many circuits such as FET resistive mixers and switches are often biased near $V_{DS} = 0$ hence promoting a negative drain voltage swing [1]. However, contrary to reports made in [1], the DC characteristics of a FET are not symmetrical, and therefore simply reversing the first quadrant characteristic to obtain the third quadrant response is not accurate, as will be explained and proven by measured results presented later in this section.

A second critical design parameter is the gate width of the active device. The ideal switch model assumes zero on-resistance and infinite transconductance. A pHEMT

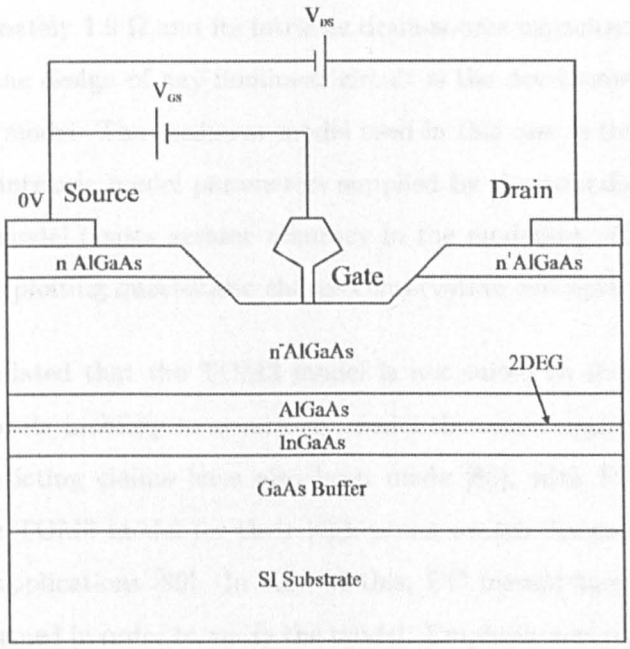


Figure 3.1: Cross section of a typical pHEMT device (not to scale).

device with a larger overall gate width provides a smaller on-resistance [82] and consequently higher efficiency, but also results in a larger intrinsic drain-source capacitance, C_{ds}, which, as predicted in (2.40), can limit the maximum frequency for optimum class E operation. A larger shunt capacitance also leads to a lower optimum load impedance and hence higher current flow, with subsequent higher power dissipation due to resistive losses in the matching networks. Additionally, although a large device may provide higher output power, it also requires a larger input drive in order to charge and discharge the larger input capacitance C_{gs}, which compromises the achievable conversion gain. Conversely, whilst a smaller device may provide more gain, the lower transconductance and higher on-resistance result in lower output power and drain efficiency [83]. The gate length of the device determines the switching speed achievable, with shorter lengths providing higher cut-off frequencies [84].

The active device used in this work is the Filtronic FPD750 pHEMT, with a gate length of 0.25 μm and a gate width of 750 μm, displaying maximum stable gain up to 12 GHz. The datasheet for this device is provided in Appendix B. This AlGaAs/InGaAs device incorporates a recessed gate structure for lower parasitic gate resistance, which is offset towards the source for lower parasitic source resistance [82]. The on-resistance of this

device is approximately 1.9 Ω and its intrinsic drain-source capacitance is 0.15 pF. An essential step in the design of any nonlinear circuit is the development of an accurate non-linear device model. The nonlinear model used in this case is the TriQuint TOM3 model [85], with intrinsic model parameters supplied by the manufacturer (Appendix C). The TOM3 model boasts greater accuracy in the modelling of gate capacitances C_{gs} and C_{gd} by exploiting quasi-static charge conservation concepts [86].

It has been speculated that the TOM3 model is not suited to the design of switching circuits due to its inability to accurately model the ohmic region around $V_{DS} = 0$ [51, 87]. Contradicting claims have also been made [88], with Filtronic plc. regularly utilising the TOM3 model for their high power switch designs for handsets and WiMax/WLAN applications [89]. In view of this, DC measurements of the pHEMT device were performed in order to verify the model. Emphasis was placed on the region around $V_{DS} = 0$, and also negative values of V_{DS} in order to accurately model device behaviour during the negative excursion of the drain voltage waveform during the off period, as shown in Figure 2.9. A packaged FPD750SOT343 was embedded into a 50 Ω test fixture to ensure stability of the circuit. If DC measurements across a bias plane are performed in a circuit environment that produces gate and drain terminations within unstable regions of the stability circles of the device, then oscillations can occur resulting in inaccurate measurements. A programmable DC supply (HP6626A) was used to perform automated measurements by sweeping V_{GS} and V_{DS} and recording the corresponding values of I_{DS}. A spectrum analyser (HP8593E) was also used to monitor stability.

Modelled versus measured I-V curves of the active device are given in Figure 3.2, and show good agreement, especially in the third quadrant. The I-V curves are not symmetrical, and it can be seen that, for gate voltage bias much lower than the pinch-off voltage of -1.0 V, a further negative excursion of the drain voltage is possible with minimal draw of drain current. However, for a certain gate bias level, negative drain current begins to be drawn for a drain voltage level beyond a certain threshold, V_{on}.

This occurs because with increasing values of negative V_{DS}, the gate-drain voltage V_{GD} approaches the pinch-off voltage and increasingly becomes the control voltage in place of V_{GS}. The value of V_{DS} at the beginning of conduction in the third quadrant, V_{on},

can be derived from,

$$V_{DS} = V_{GS} - V_{GD} \tag{3.1}$$

and is therefore given by,

$$V_{on} = V_{GS} - V_p. \tag{3.2}$$

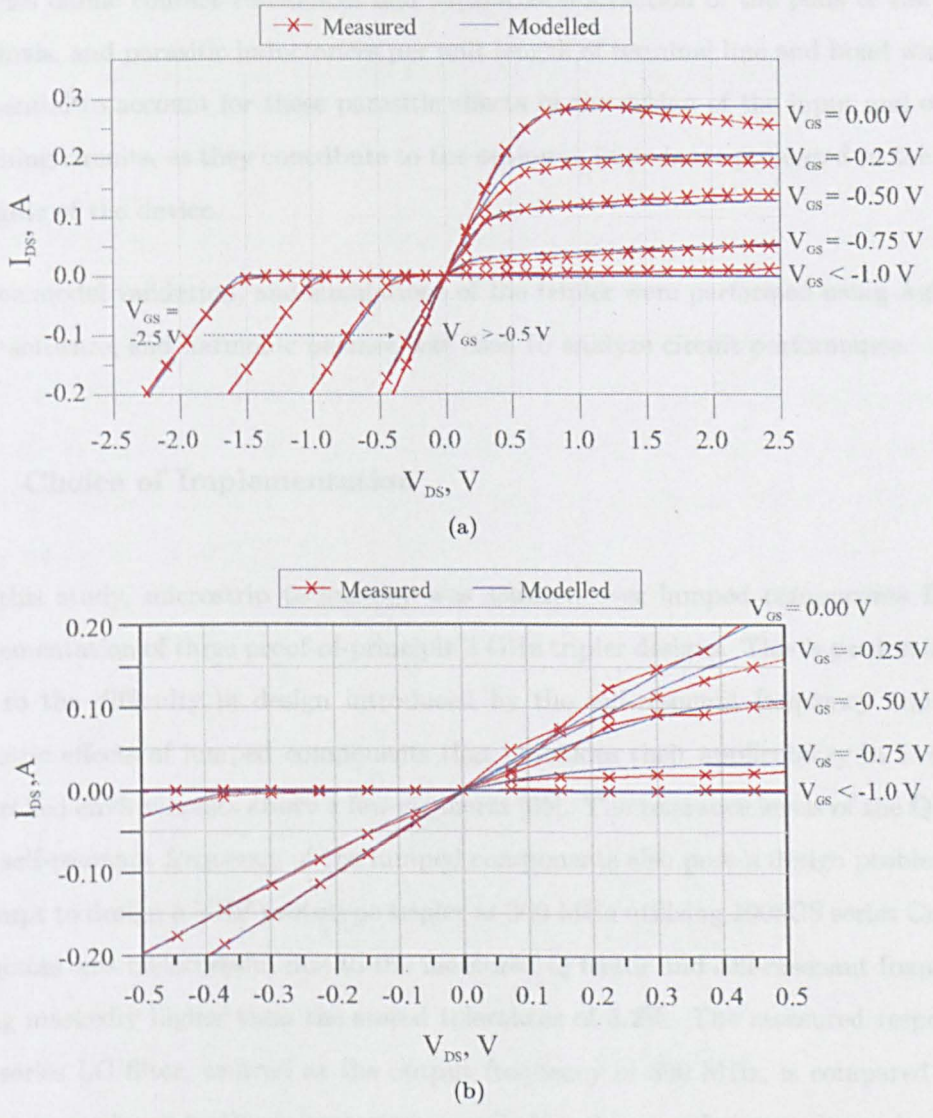


Figure 3.2: (a) Measured and modelled DC I-V curves and (b) detailed measured and modelled DC I-V curves around $V_{DS} = 0$ for a Filtronic FPD750 pHEMT device.

The knee voltage of the FPD750 is also shown in Figure 3.2 to be approximately 0.8 V. The drain must therefore ideally be biased above this value in order to ensure maximum possible $I_{ds,peak}$ for maximum output power. Drain bias is also controlled by the maximum possible $V_{ds,peak}$ given by (2.39), which in turn is dependent on the maximum negative swing of gate voltage, V_{gs}. Hence, a compromise must be reached between output power, efficiency and conversion gain.

The intrinsic TOM3 model is embedded in an extrinsic parasitic equivalent circuit, given in Appendix C, in order to model the effects of interconnect parasitics. This includes ohmic contact resistances and capacitive interaction of the pads of the three terminals, and parasitic inductances per unit length of terminal line and bond wires. It is essential to account for these parasitic effects in the design of the input and output matching circuits, as they contribute to the optimum impedance presented to the drain and gate of the device.

Device model validation, and simulations of the tripler were performed using Agilent's ADS software, and harmonic balance was used to analyze circuit performance.

3.3 Choice of Implementation

For this study, microstrip technology was selected over lumped components for the implementation of three proof-of-principle 3 GHz tripler designs. This is predominantly due to the difficulty in design introduced by the self-resonant frequency and other parasitic effects of lumped components that precludes their applicability in harmonic controlled environments above a few gigahertz [65]. The tolerance levels of the Q factor and self-resonant frequency of the lumped components also pose a design problem. An attempt to design a VHF prototype tripler at 300 MHz utilising 1008CS series Coilcraft inductors was unsuccessful due to the measured Q factor and self-resonant frequencies being markedly higher than the stated tolerances of 5.2%. The measured response of the series LC filter, centred at the output frequency of 300 MHz, is compared to the response produced by the s-parameters supplied by the manufacturer. It can be seen in Figure 3.3 that vital multi-harmonic control, especially at higher frequencies (e.g. $4f_0$) is not easily achieved.

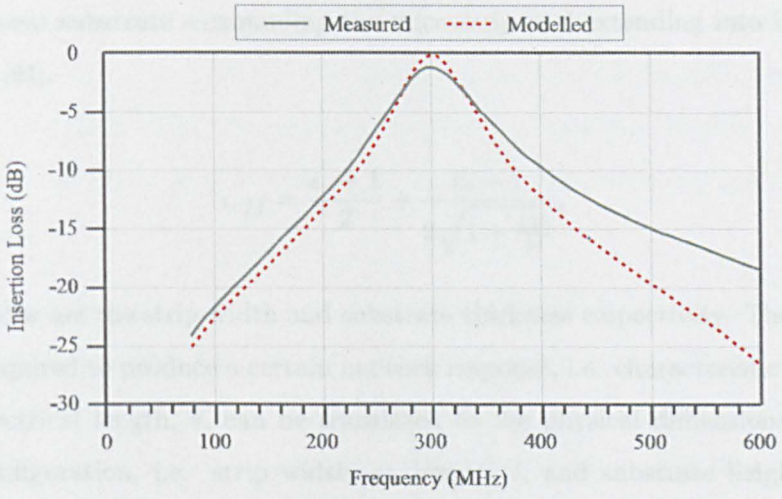


Figure 3.3: Measured (solid) and modelled [supplied by manufacturer] (dashed) insertion loss of the series LC filter, centred at 300 MHz.

Microstrip networks are more accurately modelled and controlled with predictable behaviour described by closed-form equations, offering high accuracy well into the millimetrewave region [90]. Microstrip was therefore chosen as the method of implementation at 3 GHz, with the added motivation of applicability to higher frequency circuits ranging into the millimetrewave region. Microstrip consists of a metallic conductor strip separated from a metallic ground plane by a dielectric substrate of relative permittivity ϵ_r, as shown in Figure 3.4.

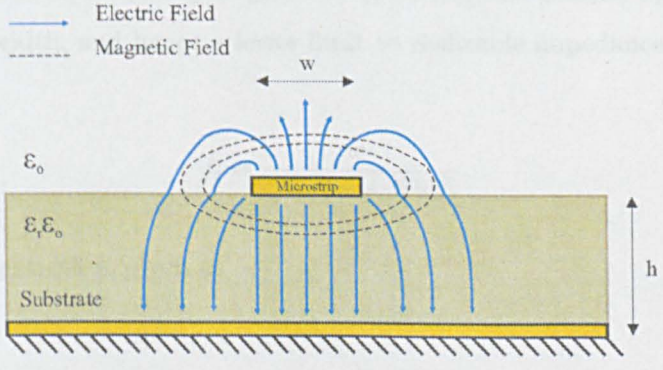


Figure 3.4: Microstrip geometry showing electric and magnetic field lines traversing both $\epsilon_o\epsilon_r$ (dielectric permittivity) and ϵ_o (free space permittivity).

There are two distinct dielectric regions involved: $\epsilon_o\epsilon_r$ of the dielectric material and ϵ_o of air. These may be combined into a relative effective permittivity, ϵ_{eff}, which defines

a homogeneous substrate surrounding the microstrip and extending into infinity, and is given by [91],

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2\sqrt{1 + \frac{12h}{w}}}, \tag{3.3}$$

where h and w are the strip width and substrate thickness respectively. The design parameters required to produce a certain network response, i.e. characteristic impedance, Z_0, and electrical length, θ, can be translated to the physical dimensions of the microstrip configuration, i.e. strip width, w, length, l, and substrate height, h, using equations (3.4)-(3.7). The characteristic impedance of the microstrip line for a geometry where $\frac{w}{h} \geq 1$, can be calculated from,

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_{eff}}[(w/h) + 1.393 + 0.667\ln((w/h) + 1.44)}. \tag{3.4}$$

However, it must be ensured that the width of the stripline does not exceed a limit beyond which a transverse-resonant mode can be excited [90] and couple with the quasi-TEM mode of the microstrip structure within the operating frequency range of the circuit. This is especially pertinent in the design of multi-harmonic controlled circuits such as class E, where the cut-off frequency must be above the highest controlled harmonic. The cut-off frequency is given by (3.5) [92] and sets an upper limit to the realisable strip width, and hence a lower limit to realisable impedance.

$$f_t = \frac{c}{\sqrt{\epsilon_r}(2w + 0.8h)}. \tag{3.5}$$

The guided wavelength is given as,

$$\lambda_g = \frac{\lambda_0}{\sqrt{\epsilon_{eff}}}, \tag{3.6}$$

where λ_0 is the wavelength in free space. Strip length, l, is then given by,

$$l = \frac{\lambda_g \theta}{2\pi}. \tag{3.7}$$

The above equations (3.3 - 3.7) are utilised in the following circuit designs to obtain initial design values of w and l of the striplines, and are subsequently refined using more accurate models incorporated in the Eesof ADS Simulator. Sophisticated models incorporating the parasitic behaviour of discontinuities in microstrip line [93], [92] are also included.

Hybrid MIC technology provides a simple and low cost fabrication technique that is ideal for realising low frequency prototype circuits for purposes of validation. It consists of individual discrete devices, such as FETs and diodes, along with passive elements that are integrated onto a common substrate board through bonding, soldering or conductive silver epoxy. These circuits can operate with relatively good performance from 1 GHz up to around 30 GHz, beyond which parasitics associated with bondwires, interconnects and device packages begin to have a significant impact on circuit performance.

Reliability and reproducibility of hybrid circuits may be poor due to the manual attachment of components, however it also provides the freedom to tune the circuit parameters, for example, by shortening lengths of transmission lines or adding transmission line stubs. Parasitic effects introduced by connections between devices and components to the microstrip must be accounted for and de-embedded in the design of the input and output matching circuits. Bond wires, for example, can be modelled as inductors with the free-space inductance given by [93],

$$L = 5.08 \times 10^{-3} \cdot l[\ln(\frac{4l}{d}) - 1], \tag{3.8}$$

where l and d are the length and diameter of the bondwire measured in mils, and L is inductance in nH. Further models that incorporate the effect of the ground plane on the effective inductance of the bondwire, along with capacitive effects introduced by the height of the bondwire are also available [94].

3.4 Design Considerations

Multiharmonic-controlled circuits come with a degree of complexity and sensitivity, due to the requirement to provide simultaneous optimum impedance at several harmonics of

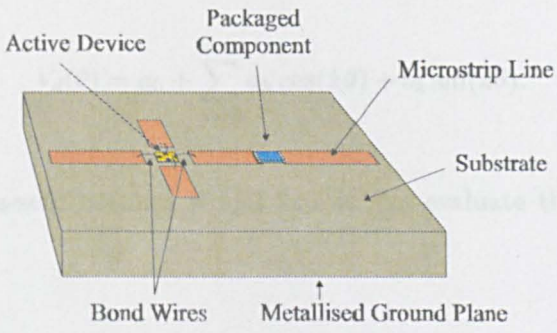


Figure 3.5: Example of a MIC circuit demonstrating device and component attachment.

the fundamental frequency. Prudent design involves arriving at a compromise between circuit performance, complexity and sensitivity, with optimum modules adopting simple designs with reduced complexity for fewer possible points of failure, and yet providing optimum performance. The techniques involved in assessing circuit design with these concepts taken into consideration are detailed in this section.

3.4.1 Number of Harmonics

The quantitative analysis in Section 2.6 takes a large number of harmonics into consideration to produce the ideal switch waveforms shown in Figure 2.9. However, for the purposes of practical implementation of the tripler, it is desirable to limit the number of harmonics that are effectively controlled in the design of the matching networks in order to reduce circuit complexity. It is often the case that the benefits obtained by the control of a larger number of harmonics do not justify the increase in complexity. For a real circuit, the output power decreases at each increasing harmonic, whilst the corresponding improvement in efficiency gained by harmonic control becomes more negligible [95, 96]. In order to evaluate the trade-off between circuit performance and number of harmonics, it is instructive to determine the number of harmonics that are required to reproduce the salient form of the ideal switch waveforms. This is achieved by analysing the switch voltage and current using Fourier series analysis and reconstructing the waveforms with a limited number of harmonics.

The Fourier series of the switch voltage given by (2.32) is,

$$V_d(\theta) = a_0 + \sum_{k=0}^{k=n} a_k \cos(k\theta) + b_k \sin(k\theta). \tag{3.9}$$

Since V_d is only non-zero between π and 2π, we can evaluate the coefficients in this interval as:

$$a_0 = \frac{I_{DC}}{9\pi\omega C} \tag{3.10}$$

$$a_n = \frac{I_{DC}}{\pi\omega C} \times \begin{cases} \frac{2}{n^2} & \text{for } n \text{ odd, } n \neq 1,3 \\ \frac{2}{n^2} - \frac{1.2732\pi}{2} & \text{for } n = 1 \\ \frac{2}{n^2} - \frac{0.2975\pi}{2} & \text{for } n = 3 \\ \frac{2}{6(n+3)} - \frac{2}{6(n-3)} & \text{for } n \text{ even} \end{cases} \tag{3.11}$$

$$b_n = \frac{I_{DC}}{\pi\omega C} \times \begin{cases} 0 & \text{for } n \text{ odd, } n \neq 3 \\ -\frac{\pi}{6} & \text{for } n = 3 \\ \frac{2.5464n}{(n^2-1)} + \frac{0.595n}{(n^2+9)} - \frac{\pi}{n} & \text{for } n \text{ even.} \end{cases} \tag{3.12}$$

Equivalent expressions for the harmonic composition of the switch current are obtained in the same way, and hence expressions for any harmonic component can be derived individually. The Fourier series of the switch current given by (2.30) is,

$$I_d(\theta) = a_0 + \sum_{k=0}^{k=n} a_k \cos(k\theta) + b_k \sin(k\theta). \tag{3.13}$$

With I_d only non-zero between 0 and π, we can evaluate the coefficients as:

$$a_0 = 1 \tag{3.14}$$

$$a_n = \frac{I_{DC}}{\pi} \times \begin{cases} 0 & \text{for } n \text{ odd}, n \neq 3 \\ \frac{-\pi}{2} & \text{for } n = 3 \\ \frac{1.2732}{(n+1)} - \frac{1.2732}{(n-1)} + \frac{0.8926}{(n+3)} - \frac{0.8926}{(n-3)} & \text{for } n \text{ even} \end{cases} \tag{3.15}$$

$$b_n = \frac{I_{DC}}{\pi} \times \begin{cases} \frac{2}{n} & \text{for } n \text{ odd}, n \neq 1, 3 \\ \frac{2}{n} + \frac{1.2732\pi}{2} & \text{for } n = 1 \\ \frac{2}{n} + \frac{0.8926\pi}{2} & \text{for } n = 3 \\ -\frac{1}{(n+3)} - \frac{1}{(n-3)} & \text{for } n \text{ even.} \end{cases} \tag{3.16}$$

It can be seen in Figure 3.6 that four harmonics are sufficient to produce a good approximation to the ideal switch waveforms and is a suitable compromise. Significant improvement is not achieved by the inclusion of additional harmonic control, and the variation in finite fall time of the current waveform is insignificant with the incorporation of higher harmonics. Simulations of an ideal circuit were performed in order to quantify the impact of limiting the number of controlled harmonics on DC/RF efficiency. The results, given in Table 3.4.1, show that significant improvement in efficiency is achieved with control up to the fourth harmonic.[1] Control of subsequent harmonics beyond $4f_0$, however, provides only small improvements in efficiency which are deemed insufficient to offset the corresponding increase in circuit complexity.

The expressions given in (3.11) and (3.12) can also be used to derive the harmonic content at the output of the tripler for a non-ideal output series filter. A perfect filter resonant at $3f_0$ is assumed in the analysis in Section 2.6, giving a sinusoidal output

[1]The remaining unwanted harmonics are terminated in a short-circuit to represent the worst case scenario.

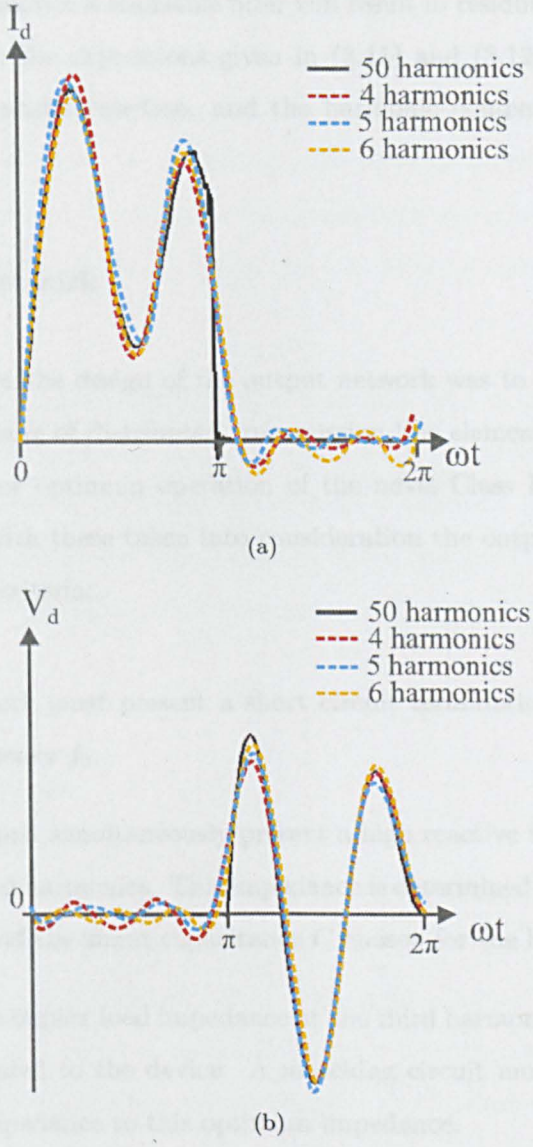


Figure 3.6: Ideal (solid) and 4, 5 and 6-harmonic approximation (dashed) of the drain (a) current and (b) voltage waveforms of the proposed Class E tripler.

No. of controlled harmonics	DC/RF Efficiency
50	99.4 %
6	99.1 %
5	97.5 %
4	95.9 %
3	22.9 %

Table 3.1: The impact of limiting the number of controlled harmonics on DC/RF efficiency of the novel class E tripler.

signal. However, in practice a realisable filter will result in residual unwanted harmonic content at the load. The expressions given in (3.11) and (3.12) can be transformed through any filter transfer function, and the harmonic content at the load can be computed.

3.4.2 Output Network

The main objective in the design of the output network was to realise a narrow-band load network comprising of distributed transmission line elements. The harmonic terminations required for optimum operation of the novel Class E tripler were derived in Section 2.6, and with these taken into consideration the output load network must satisfy the following criteria:

1. The load network must present a short circuit termination at the fundamental switching frequency f_0.
2. The network must simultaneously present a high reactive termination at $2f_0$ and higher unwanted harmonics. This impedance is determined by the resonant circuit tuned to $3f_0$ and the shunt capacitance C chosen for the load network.
3. The optimum complex load impedance at the third harmonic $3f_0$, given by (2.36), must be presented to the device. A matching circuit must transform the 50 Ω terminating impedance to this optimum impedance.
4. All unwanted harmonics must be suppressed to a low level at the output load termination - typically to 20 dBc.
5. The peak switch voltage and current must not exceed the device specifications.
6. The topology should be easily realisable in microstrip technology and contain as few points as possible of potential failure.

The total shunt capacitance of the load network can be provided by the parasitic capacitance, C_{ds} of the device, along with additional external shunt capacitance for a higher output power. Output power was shown to be inversely proportional to drain

bias level, V_{DD} and shunt capacitance, C (2.41). V_{DD} is chosen to maximise the swing of the switch voltage and is limited by the device breakdown voltage at the positive excursion, and by eventual draw of drain current during the negative excursion. A value of C is then chosen according to the output power required, whilst ensuring that the peak drain current does not exceed the maximum current rating of the device ((2.33) and (2.37)), and that the maximum frequency for optimum class E operation (2.40) is not exceeded.

It was shown in Section 3.4.1, that limiting harmonic control to the fourth harmonic provides a good approximation to the drain voltage and current waveforms required for high efficiency operation. The design of the output networks in the following section were accordingly limited to the manipulation of the harmonic impedances up to the fourth harmonic to avoid unnecessary complexity of the tripler.

3.4.3 Input Network

Several strategies have been reported for the optimum design of input matching networks for frequency multipliers. These include choosing the correct gate bias voltage and input power level for a particular load angle in the case of classical multipliers [2], or for particular clipping effect of the drain current to maximise the required harmonic [29, 30]. Large signal input conjugate matching at the fundamental frequency has also been reported with the remaining unwanted harmonics terminated in a short-circuit [1, 20, 38, 97, 98, 99]. Shorting of the unwanted harmonics is a popular choice to overcome distortion of the drive signal due to the nonlinear intrinsic capacitance of the device, C_{gs}. The nonlinearity of C_{gs} for the FPD750 pHEMT with intrinsic gate voltage, V_{gsi}, and drain voltage, V_{dsi}, is plotted in Figure 3.7. Nonlinear compensation of C_{gs} has also been reported by incorporating a diode at the input of the device in order to retrieve the sinusoidal drive waveform [53]. Reflective networks have also proven to be successful in maximising conversion gain. This technique reflects the unwanted harmonics back into the input of the transistor for reamplification and augmentation of the power at the required harmonic through constructive interference at the output. This has been reported for both doublers [5, 100, 101, 102, 103] and triplers [31, 41, 59, 60].

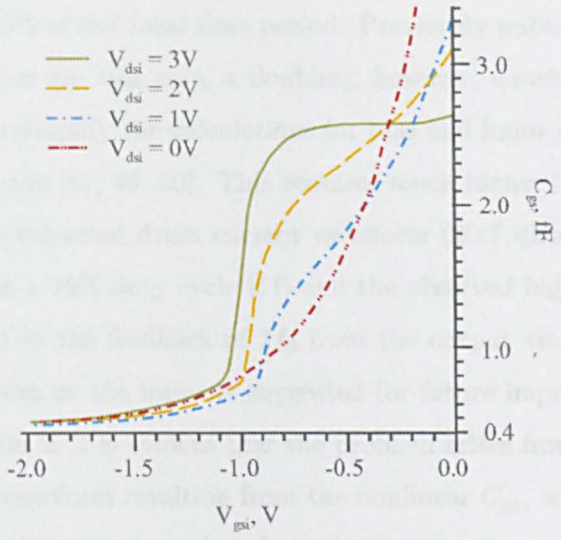


Figure 3.7: Nonlinear intrinsic input capacitance, C_{gs}, of the FPD750 pHEMT device plotted as a function of intrinsic gate-source voltage, V_{gsi}, and drain-source voltage, V_{dsi} (as obtained from the TOM3 model).

In the case of class E circuits however, it is the switching of the device that is of paramount importance for peak circuit performance. The onus is therefore placed on the *shaping* of the drive waveform in order to obtain optimal switching of the device, rather than the reflective nature of harmonics for supplementary augmentation at the output. A square drive waveform is ideal and is popularly implemented as a Class F circuit as the driver stage to a Class E amplifier [104, 105, 106]. This, however, results in a larger number of FET devices and a larger circuit area which are both undesirable when attempting to minimise cost. However, a more promising drive network has been proposed for Class F amplifiers [52]. It was shown that significant signal distortion at the gate of the device is caused by the nonlinearity of the input capacitance with applied input voltage. This, in turn, causes the duty cycle to deviate from the optimum 50 % with corresponding degradation in performance. However, instead of shorting the unwanted harmonics to recover the original sinusoidal drive, the nonlinearity is used instead to *shape* the drive waveform into a square waveform. An approximation to a square waveform is achieved if the input network presents a short circuit at $2f_0$ and $4f_0$ to the input of the device.

As shown in section 2.4, conventional class E triplers require a rectangular drive waveform in order to sustain the three consecutive peaks in I_{ds} throughout the on-period

which accounts for 83% of the total time period. Previously published reports of class E frequency multipliers (in this case, a doubler), however, assume a sinusoidal drive waveform in order to simplify the calculations for bias and input power to achieve the required 75% duty cycle [47, 49, 50]. This requires much higher input power levels in order to support the expected drain current waveform (20.7 dBm - 23.5 dBm). The difficulty in achieving a 75% duty cycle [51] and the observed high $2f_0$ content at the input, are attributed to the feedback of $2f_0$ from the output via C_{gd}. Consequently, a reflective $2f_0$ network at the input is suggested for future improvements. However, as discussed in chapter 2, it is evident that the problem arises from the significant distortion of the drive waveform resulting from the nonlinear C_{gs}, which causes the duty cycle to deviate from its optimum value. Indeed, this is re-iterated in the fact that the optimum operation of the doubler reported in [49, 50] was achieved for a duty cycle of 4%, suggesting that non-linear mechanisms other than the switching of the device were the dominant harmonic generator.

In this work, it is recognised that the input network must be designed not only to provide a fundamental conjugate match to 50 Ω at the supplied input power level for maximum gain, but also to overcome the significant distortion of the input drive signal resulting from the nonlinear intrinsic input capacitance, C_{gs}, of the device. The input network must be designed to shape the input drive into a square waveform in order to drive the transistor efficiently as a switch with 50% duty cycle. A further requirement is to ensure that the gradient of the rising edge of the input square drive must be sharp enough to follow the steep rise in drain current up to its peak value at the beginning of the on period. Failure to meet this requirement results in the drain current and voltage waveforms deviating from their ideal shape, resulting in suboptimal operation.

In addition, referring to Figure 3.2, it can be seen that the input waveform must be designed to drive the gate to a sufficiently negative voltage to ensure maximum negative excursion of V_{ds} whilst avoiding forward biasing the gate-drain diode, and also to a sufficiently positive voltage to provide maximum excursion of the drain current without forward biasing the gate-source diode. This can be realised through careful selection of input power level and gate bias point, along with the degree of conjugate match achieved at the fundamental switching frequency.

3.4.4 Bias Point and Bias Network

Gate bias voltage, V_{GG}, is chosen such that the active device is biased at or near pinch-off so that, coupled with the input wave-shaping network and input power level, a square drive with appropriate amplitude is provided to the input of the device to turn it sufficiently on and off. Drain bias, V_{DD}, is chosen to ensure that adequate output power at the third harmonic is delivered to the load according to (2.42), and also to ensure that V_{ds} does not swing beyond the zero-current region of the negative quadrant of the I-V curve. The design of the gate and drain bias circuitry must ensure a constant supply of V_{GG} and V_{DD}, as well as provide gate current, I_{GS}, and sufficient drain current, I_{DS}, pertaining to the design of the circuit. The gate, in particular, must be protected by limiting the gate current if the device goes into forward conduction or suffers voltage spikes from the power supplies. The bias circuitry can also be designed to ensure stability of the circuit, and also provide isolation from feedback between the gate and drain of the device.

A typical bias circuit design consists of a high impedance, quarter-wavelength line at the operating frequency with a broadband shunt radial stub at its apex. However, this structure re-resonates at harmonics of the operating frequency and is unsuitable in the design of multi-harmonic controlled circuits. Several methods to implement the bias circuitry for class E networks to overcome this problem have been reported. One such method is to provide the bias through a large inductor acting as an RF choke [77]. At higher frequencies however, it becomes increasingly difficult to implement a large enough inductor for RF isolation with a sufficiently high self-resonant frequency. In such cases, the load impedance and harmonic impedances presented to the device must be tuned to account for the finite RF choke. Another popular method is to implement the bias feedlines in microstrip and to include these lines as part of the matching networks [107][62].

This technique was used in a first iteration of the fabricated novel triplers, which incorporated a bias network that consisted of a length of transmission line terminated with decoupling capacitors, as shown in Figure 3.8. The impedance presented by the bias line was used to tune the output load impedance and hence contribute to the overall optimum impedance presented to the device. However, it can be seen that the inter-

action of the decoupling capacitors caused the response of the load network to deviate from its required characteristic, especially at the higher harmonics. This was due to the self-resonant frequency of the individual capacitors interacting to produce a response much removed from that expected.

For the purposes of practical tuning it was therefore deemed prudent to isolate the bias circuitry from the matching networks at all the considered harmonics. To achieve this, a network of high impedance lines and radial stubs was designed to provide sufficient isolation from the matching networks at the fundamental and at each subsequent harmonic up to $4f_0$. This was achieved by ensuring a return loss of at least -20 dB at each harmonic. A schematic of the bias network with simulated insertion loss and return loss profile is provided in Figure 3.9. A 1 kΩ resistor was additionally included in the gate bias to provide a degree of gate protection.

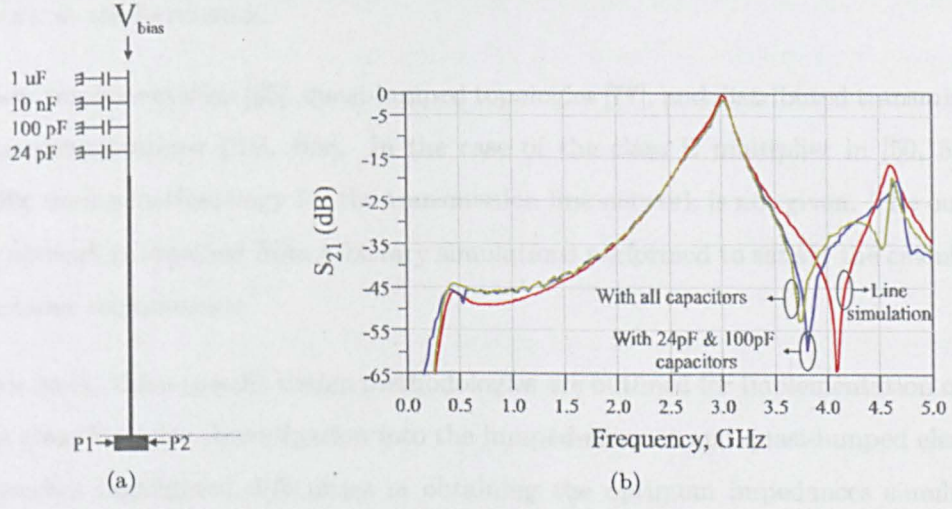


Figure 3.8: (a) Schematic representation of the bias network implemented for the input and output networks of the first generation triplers and (b) simulated insertion loss (red) and measured insertion loss of the output load network with all decoupling capacitors in place (blue) and with only the 24 pF and 100 pF decoupling capacitors in place (green), clearly showing variation of the load network response with capacitors.

3.5 Circuit Implementation

Several techniques to realise the multi-harmonic impedances of a microwave class E amplifier in microstrip have been published. These include straightforward lumped-

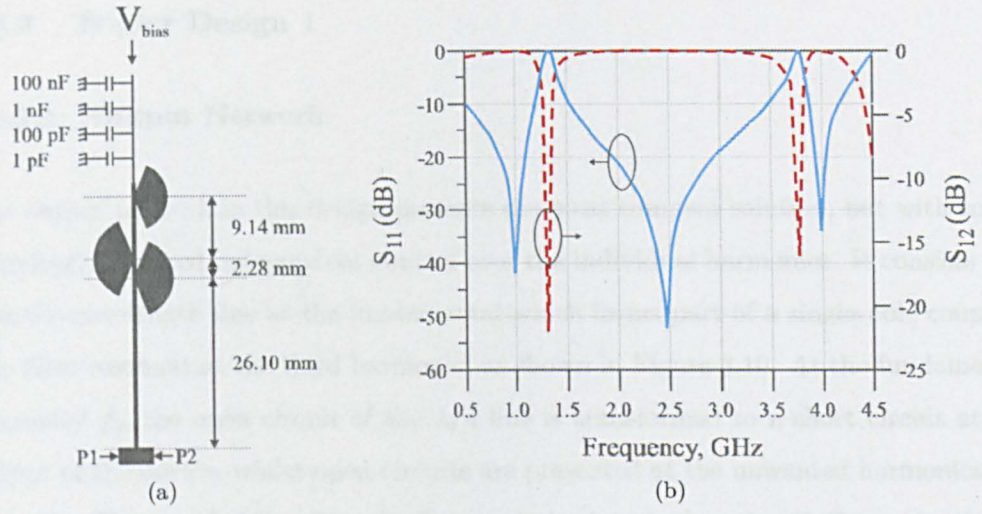


Figure 3.9: (a) Schematic representation of the bias network implemented for the input and output networks of the tripler and (b) simulated return loss (solid) and insertion loss (dotted) of the bias network in 50 Ω showing isolation of the bias from the matching network at the harmonics.

element implementation [65], quasi-lumped topologies [77], and distributed transmission line implementations [108, 109]. In the case of the class E multiplier in [50, 51], a specific design methodology for the transmission line network is not given. The output load network is obtained from arbitrary simulations performed to satisfy the calculated impedance requirements.

In this work, three specific design methodologies are outlined for implementation of the novel class E tripler. Investigation into the lumped-element and quasi-lumped element approaches highlighted difficulties in obtaining the optimum impedances simultaneously at multiple harmonics due to the self-resonant frequency inherent in the former case, and the narrowband nature of the latter. Hence, distributed transmission line implementation of the output and input load networks was chosen.

3.5.1 Tripler Design 1

3.5.1.1 Output Network

The output network in this design presents the most compact solution, but with correspondingly reduced independent control over the individual harmonics. It consists of a quarter-wavelength line at the fundamental which forms part of a single-pole coupled-line filter resonant at the third harmonic, as shown in Figure 3.10. At the fundamental frequency f_0, the open circuit of the $\lambda/4$ line is transformed to a short circuit at the output of the device, whilst open-circuits are presented at the unwanted harmonics $2f_0$ and $4f_0$. The coupled-line filter is then optimised such that the 50 Ω termination is translated through the filter and the quarter-wavelength line to the optimum class E impedance at the third harmonic, $3f_0$. This achieves simultaneous harmonic filtering and optimum $3f_0$ load termination in a single structure, thus benefiting circuit size as well as matching network insertion loss, leading to improved efficiency. The coupled-line filter also functions as a DC block, therefore eliminating the need for a DC blocking capacitor in the output matching circuit.

The resulting harmonic impedances presented to the output of the device are shown in Figure 3.11(a), and the S-parameters of the structure are shown in Figure 3.11(b). At $3f_0$, an insertion loss of 1.2 dB is achieved with a return loss of -12.5 dB. The bond wire inductances and bond pad parasitics are accounted for in the design of the network, and the drain bias line is placed at an optimised distance from the device along TL1 to produce minimal interference with the matching circuit.

3.5.1.2 Input Network

Short circuit terminations at $2f_0$ and $4f_0$ are required to be presented to the input of the device, with a complex conjugate match at f_0, as discussed in Section 3.4.3. This requirement can potentially be met by the compact input structure shown in Figure 3.12. A $\lambda/4$ line at f_0 is terminated in a parallel resonant circuit tuned at f_0. The $\lambda/4$ line translates the short-circuit termination provided by this resonant circuit at $2f_0$ and $4f_0$ to the input of the device, whilst being optimised to provide a conjugate match at f_0. However, an initial iteration of the combined input and output circuit

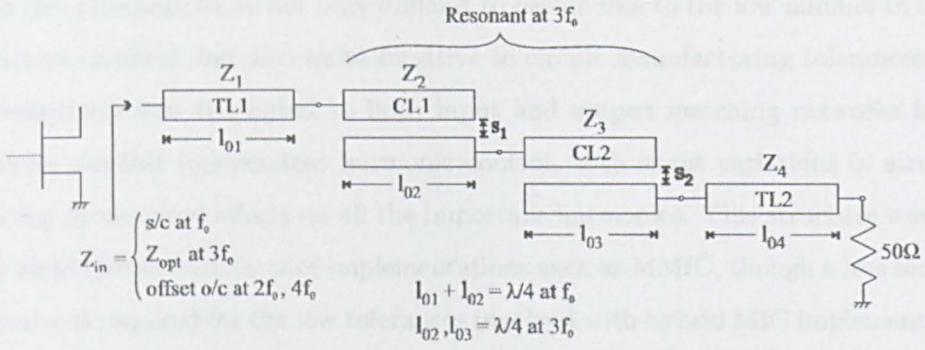


Figure 3.10: Schematic of the output matching network for tripler design 1.

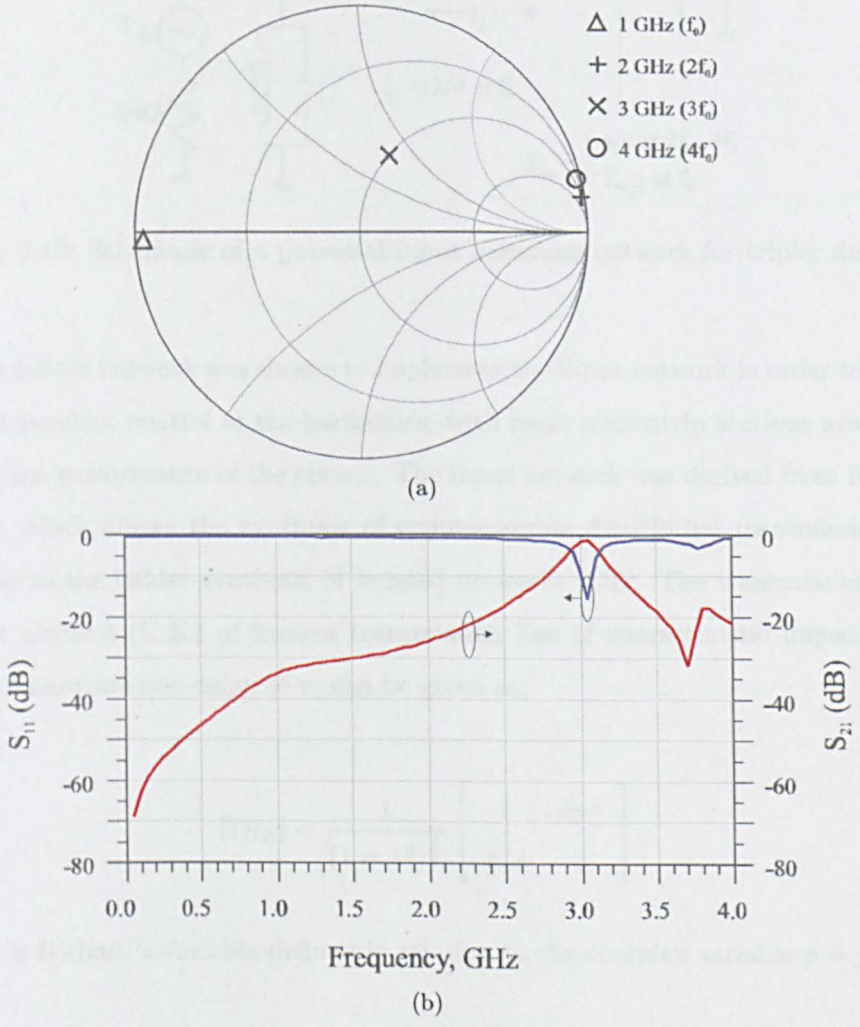


Figure 3.11: (a) Simulated harmonic impedances presented to the drain terminal of the device by the output matching network, and (b) simulated S-parameters of the the output matching network of tripler design 1.

proved this structure to be not only difficult to design due to the low number of design parameters involved, but also quite sensitive to circuit manufacturing tolerances. The high sensitivity was attributed to both input and output matching networks having the lowest possible independent harmonic control, with slight variations in structure producing pronounced effects on all the important harmonics. This structure would be highly suited for strict tolerance implementations such as MMIC, though a less sensitive alternative is required for the low tolerances involved with hybrid MIC implementation.

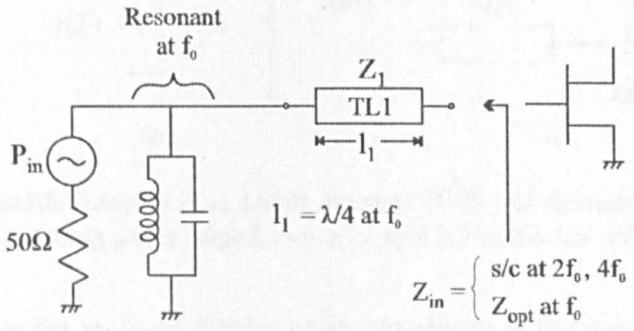


Figure 3.12: Schematic of a potential input matching network for tripler design 1.

Instead a ladder network was chosen to implement the input network in order to provide more independent control of the harmonics, with more microstrip sections available to optimise the performance of the circuit. The input network was derived from Richard's theorem, which allows the synthesis of commensurate distributed transmission lines, analogous to the ladder synthesis of lumped networks [110]. The transmission matrix of a unit element (U.E.) of lossless transmission line of characteristic impedance Z_0, and commensurate one delay of τ, can be given as,

$$[T_{UE}] = \frac{1}{(1-\lambda^2)^{\frac{1}{2}}} \begin{bmatrix} 1 & Z_0\lambda \\ Y_o\lambda & 1 \end{bmatrix}, \tag{3.17}$$

where λ is Richard's variable defined in relation to the complex variable $p = j\omega$,

$$\lambda = \tanh \tau p = j \tan \theta. \tag{3.18}$$

Hence, if $z(\lambda)$ is a positive, real driving impedance, then a U.E. of characteristic

impedance $z(1)$ can always be extracted in cascade from $z(\lambda)$ (as shown in Figure 3.13), leaving a remainder of,

$$z_1(\lambda) = z(1)\frac{z(\lambda) - \lambda z(1)}{z(1) - \lambda z(\lambda)}. \tag{3.19}$$

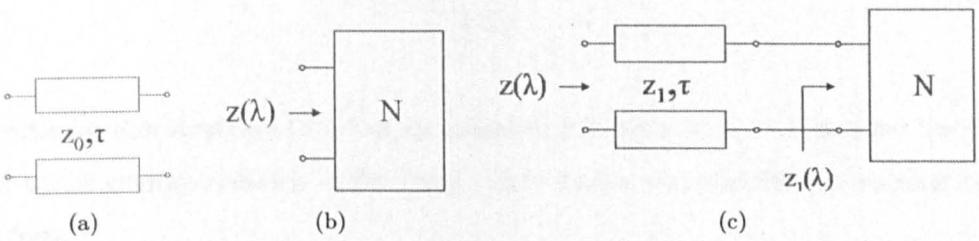


Figure 3.13: Richards theorem: (a) a unit element (U.E.) of characteristic impedance z_0 and delay τ, (b) driving point impedance $z(\lambda)$ and (c) extraction of U.E.s in cascade.

The polynomial for the required driving point impedance of the input network is constructed by placing the harmonics to be shorted (e.g. $2f_0$) as zeroes, and those to be open-circuited (e.g. $3f_0$) as poles. It is given by,

$$z(\lambda) = \frac{\lambda(\lambda^2 + \tan^2 2\theta)}{(\lambda^2 + \tan^2 \theta)(\lambda^2 + \tan^2 3\theta)}, \tag{3.20}$$

where a term relating to the fourth harmonic, $4f_0$, has had to be excluded in order to obtain a solution pertaining to realisable widths of the lines within the limits of manufacturing tolerances and the limit imposed by (3.5). The characteristic impedances for U.E.s are derived for an electrical length of 20° at the fundamental frequency, to obtain realisable line widths. The short-circuit normalized impedances are computed to be,

$$z_1 = 0.3762 \quad z_2 = 0.4528$$

$$z_3 = 0.3052 \quad z_4 = 0.6355.$$

These impedances are de-normalized with respect to 50 Ω, and initial values for the linewidths are calculated using (3.4), with final optimisation performed in ADS once

the complete input circuit is constructed. The transfer matrix of the complete cascade structure is computed by expressing each of the U.E.s in the form given by (3.17) and performing matrix multiplication. This gives,

$$\left[T \right] = \begin{bmatrix} 0.234 & 0.408j \\ 2.45j & 0 \end{bmatrix}. \tag{3.21}$$

In order for this structure to act as an impedance inverter at f_0 to transform the 50 Ω load to the conjugate match at the input of the device, the transfer matrix must be of the form,

$$\left[T \right] = \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix}, \tag{3.22}$$

where Z_0 is the characteristic impedance of the impedance inverter. Therefore, a capacitor is required in cascade with the structure,

$$\left[T_{total} \right] = \begin{bmatrix} 0.234 & 0.408j \\ 2.45j & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ C_{inv}p & 1 \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix} \tag{3.23}$$

The shunt capacitance, C_{inv}, is denormalised with respect to 50 Ω and frequency 1 GHz, to give 0.75 pF so that the overall transfer matrix of the complete cascade structure at f_0 is of the form given in (3.22). In order for C_{inv} to only be presented at f_0, with a short-circuit termination presented to the remaining harmonics, a parallel resonant circuit at f_0 is implemented, as shown in Figure 3.14. The impedance transforming capacitor, C_{inv}, can be absorbed into the parallel resonant circuit, and in this design an 8 pF capacitance replaces the parallel resonant circuit to realize a low pass filter at the fundamental. The open circuit stubs that are implemented to realise this capacitance are also optimised to provide enhanced suppression of the unwanted harmonics by selecting the lengths to be quarter wavelengths at $2f_0$ and $3f_0$ to provide a short-circuit to ground. A schematic of the input matching network is given in Figure 3.14.

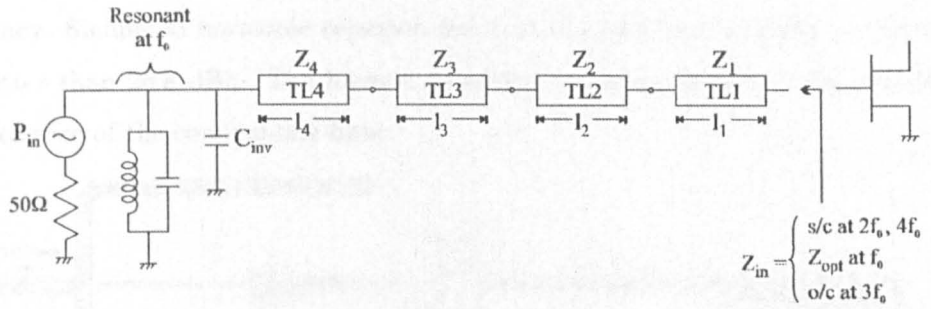


Figure 3.14: Schematic of the input matching network for tripler design 1.

3.5.1.3 Complete microstrip circuit

EM simulations of the input and output sections along with the bias circuit are performed for the final optimisation of the tripler, and the complete layout of the design is given in Figure 3.15. Details of the line dimensions of the matching networks are given in Appendix E. Optimum operation of the tripler is achieved at a gate bias of -1.9 V and a drain bias of 0.4 V, and a plot of simulated circuit performance with input power level is given in Figure 3.16. Switched-mode operation of the multiplier is clearly evident at an input power level of 1.1 dBm, where the output power, conversion gain and drain efficiency begin to increase rapidly. Further increase is seen at a power level of 4 dBm, where optimum switching of the device is achieved and conversion gain (above 0 dB) is observed.

A maximum drain efficiency of 63 % , 28.9 % PAE and 2.7 dB conversion gain at an input power level of 4.6 dBm is expected with a draw of 21 mA of DC drain current. The corresponding drain voltage and current waveforms along with the input voltage driving waveform at this operating point are shown in Figure 3.16. [2] It can be seen that the requisite square drive is achieved for efficient switching of the device at a 50 % duty cycle. A sufficient negative gate drive is also obtained to allow for maximum negative swing of V_{ds}, with minimal draw of I_{ds}, as discussed in Section 3.4.3. The drain voltage and current waveforms are seen to be displaced in time such that I_{ds} is a maximum when V_{ds} is a minimum, and vice-versa, therefore ensuring a high drain

[2] It must be noted that I_{ds} (and V_{ds}) is measured at the terminals of the device. Hence, referring to Figure 2.1, this current is essentially I_0+I_i, which leads to the characteristic 'bump' in the current in the region where the device is off, as seen in Figure 3.16. This effect is more pronounced in designs that implement a larger proportion of the required shunt capacitance, C, as the parasitic capacitance, C_{ds}, of the device.

efficiency. Simulated harmonic rejection levels at the load of the tripler are shown to be better than 26.8 dBc. The highest unwanted harmonic occurs at $9f_0$ due to the re-resonance of the coupled-line filter.

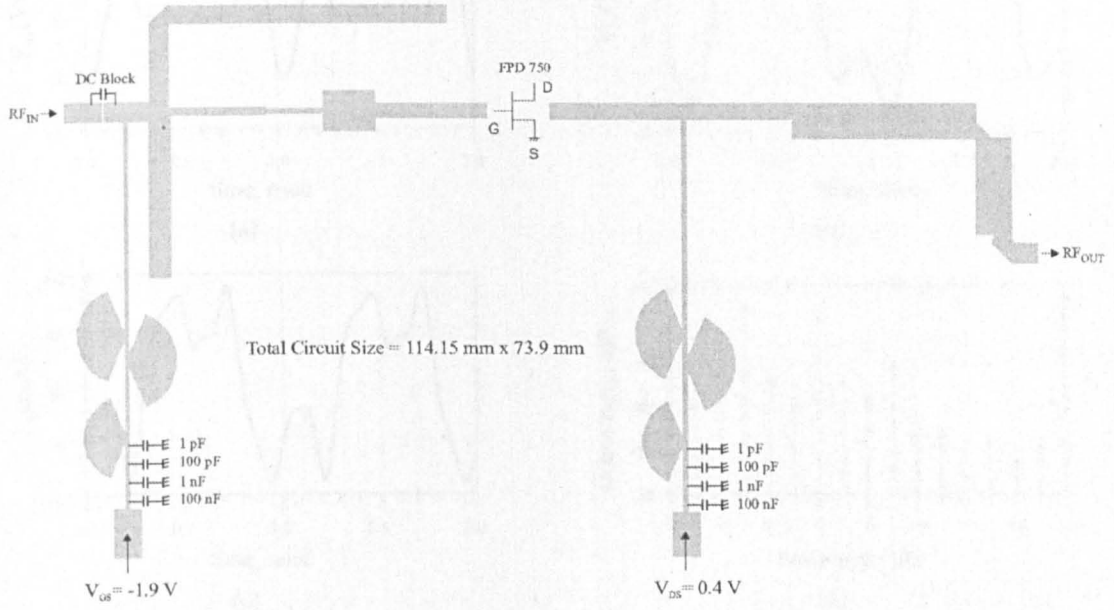


Figure 3.15: Complete Microstrip layout of tripler design 1 (not to scale).

3.5.2 Tripler Design 2

3.5.2.1 Output Network

This design provides an added degree of independent harmonic control by implementing the input as well as the output networks as commensurate transmission lines using Richard's theorem. The input network is designed as described for the previous topology. The polynomial for the driving point impedance for the output network is given by,

$$z(\lambda) = \frac{(\lambda^2 + \tan^2\theta)(\lambda^2 + \tan^2 3\theta)}{\lambda(\lambda^2 + \tan^2 2\theta)(\lambda^2 + \tan^2 4\theta)}. \tag{3.24}$$

The characteristic impedances for the U.E.s are derived for an electrical length of 15° at the fundamental frequency, to obtain widths of the lines that are practically realisable. The open-circuit normalised impedances are,

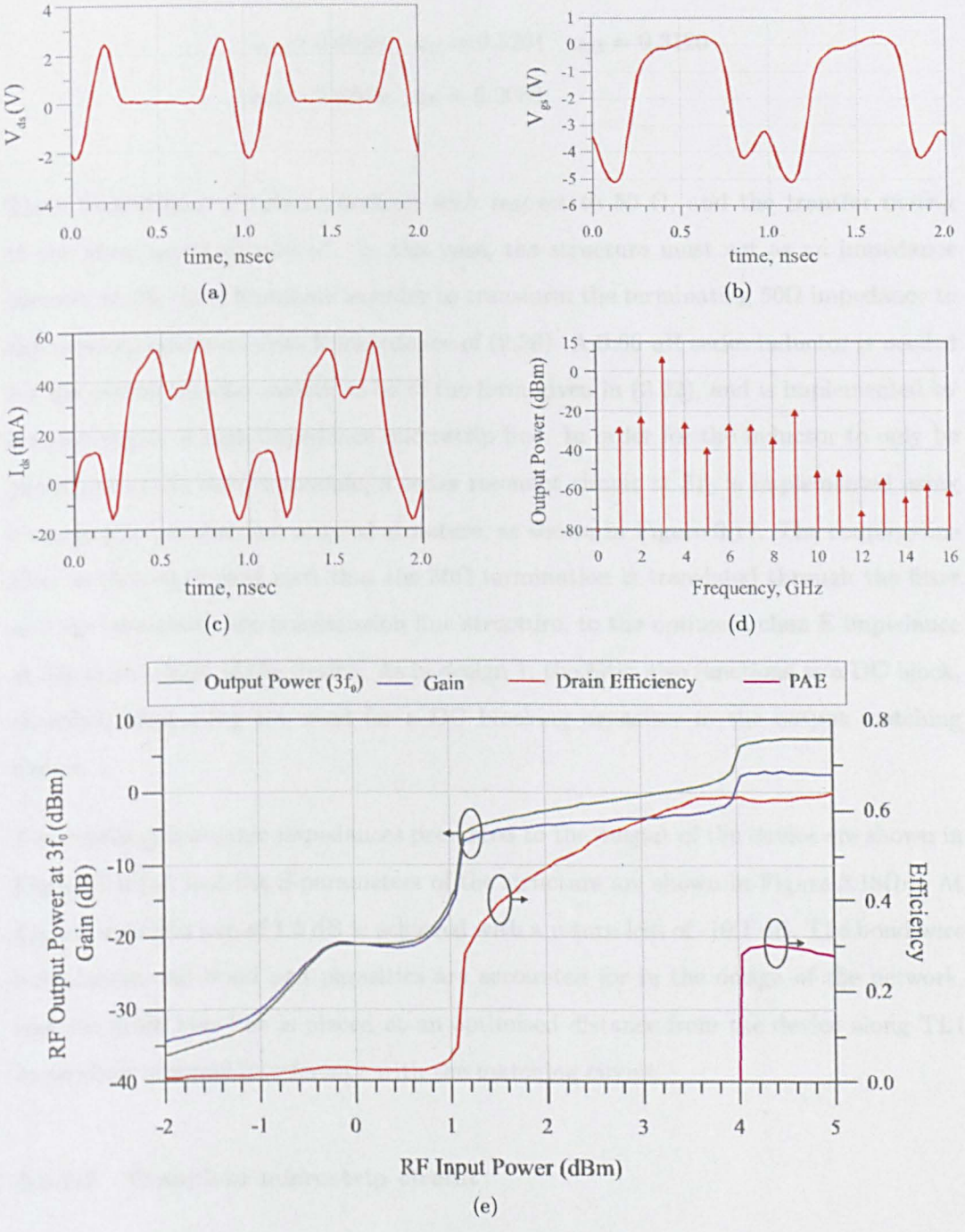


Figure 3.16: Time domain simulations of (a) drain voltage waveform (b) input drive waveform (c) drain current waveform and (d) output power spectrum of tripler design 1, biased at V_{GG}=-1.9 V and V_{DD}=0.4 V, and (e) output power at $3f_0$, conversion gain, drain efficiency and PAE as a function of input power level.

$$z_{01} = 0.4019 \quad z_{02} = 0.5261 \quad z_{03} = 0.3126$$
$$z_{04} = 0.6844 \quad z_{05} = 0.2089.$$

These impedances are de-normalized with respect to 50 Ω, and the transfer matrix of the structure is calculated. In this case, the structure must act as an impedance inverter at the third harmonic in order to transform the terminating 50Ω impedance to the required optimum class E impedance of (2.36). A 0.66 nH series inductor is needed for the overall transfer matrix to be of the form given in (3.22), and is implemented by a short length of high impedance microstrip line. In order for the inductor to only be presented to the third harmonic, a series resonant circuit at $3f_0$ is implemented using a single-pole parallel-line coupled structure, as shown in Figure 3.17. The coupled-line filter is then optimised such that the 50Ω termination is translated through the filter and the commensurate transmission line structure, to the optimum class E impedance at $3f_0$ at the drain of the device. As in design 1, the filter also functions as a DC block, therefore eliminating the need for a DC blocking capacitor in the output matching circuit.

The resulting harmonic impedances presented to the output of the device are shown in Figure 3.18(a), and the S-parameters of the structure are shown in Figure 3.18(b). At $3f_0$, an insertion loss of 1.5 dB is achieved with a return loss of -10.1 dB. The bond wire inductances and bond pad parasitics are accounted for in the design of the network, and the drain bias line is placed at an optimised distance from the device along TL1 to produce minimal interference with the matching circuit.

3.5.2.2 Complete microstrip circuit

Final EM optimisation of the tripler is performed, and the complete layout of the design including input, output and bias networks, is shown in Figure 3.19. Details of the line dimensions of the matching networks are given in Appendix E. In this case, optimum operation of the tripler is achieved at a gate bias of -1.57 V and a drain bias of 0.8 V. A plot of simulated circuit performance with input power level is given in Figure 3.20.

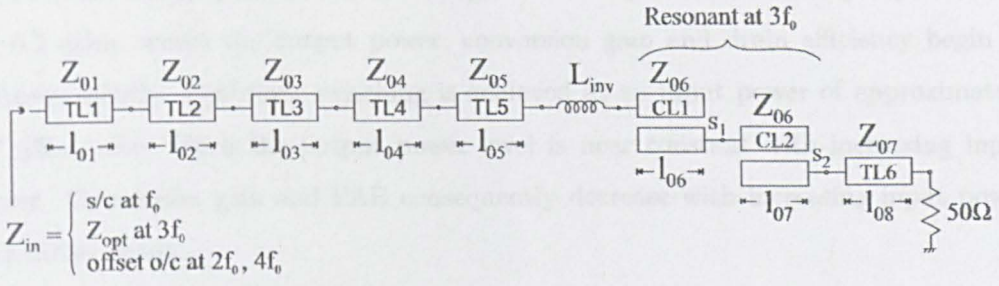


Figure 3.17: Schematic of the output matching network for tripler design 2.

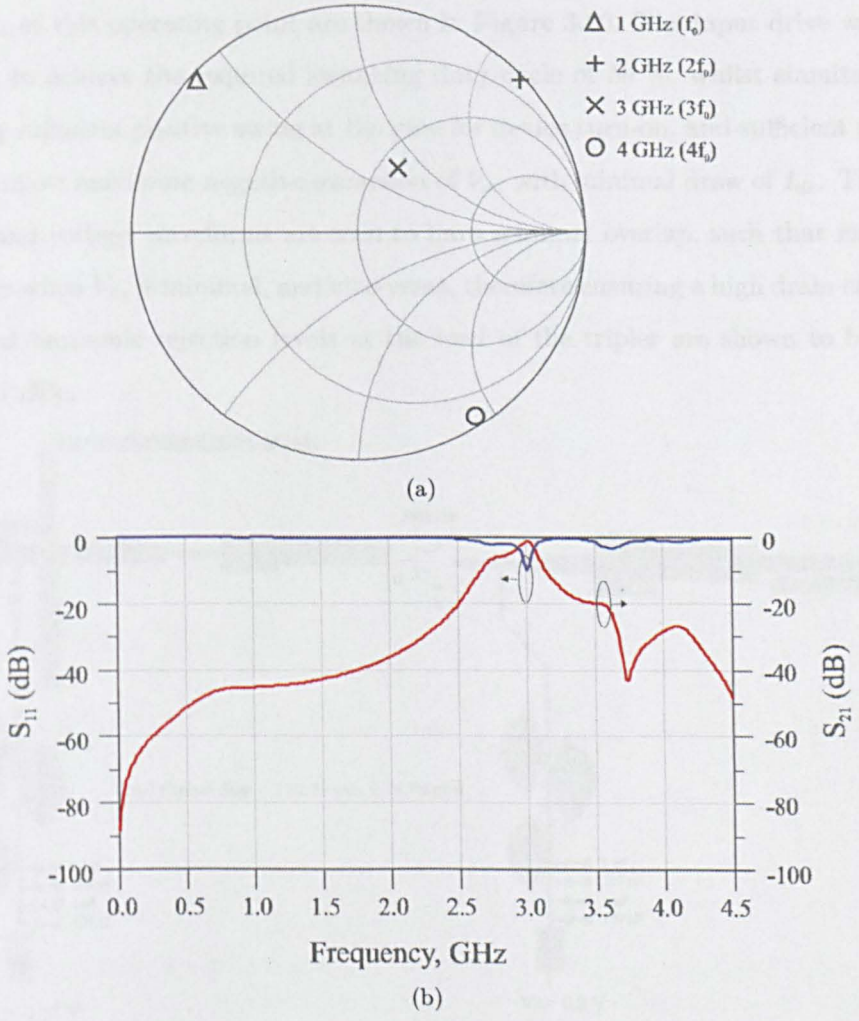


Figure 3.18: (a) Simulated harmonic impedances presented to the drain terminal of the device by the output matching network, and (b) simulated S-parameters of the the output matching network of tripler design 2.

Onset of switching operation of the multiplier is clearly evident at an input power level of -0.2 dBm, where the output power, conversion gain and drain efficiency begin to increase rapidly. Optimum switching is achieved at an input power of approximately 0.7 dBm, after which the output power level is near constant with increasing input power. Conversion gain and PAE consequently decrease with increasing input power as a direct result.

A maximum drain efficiency of 63.5 % , 56.1 % PAE and 8.6 dB conversion gain at an input power level of 0.7 dBm is expected with a draw of 17 mA of DC drain current. The corresponding drain voltage and current waveforms along with the input voltage driving waveform at this operating point are shown in Figure 3.20. The input drive waveform is shown to achieve the required switching duty cycle of 50 %, whilst simultaneously achieving sufficient positive swing at the gate for device turn-on, and sufficient negative swing to allow maximum negative excursion of V_{ds} with minimal draw of I_{ds}. The drain current and voltage waveforms are seen to have minimal overlap, such that maximum I_{ds} occurs when V_{ds} is minimal, and vice-versa, therefore ensuring a high drain efficiency. Simulated harmonic rejection levels at the load of the tripler are shown to be better than 36.7 dBc.

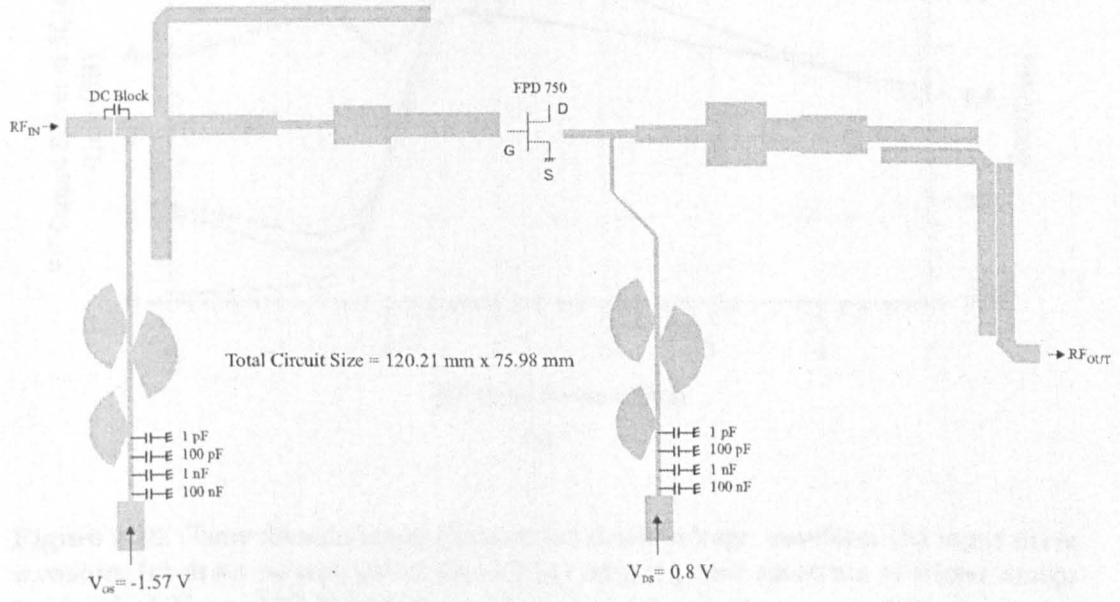


Figure 3.19: Complete Microstrip layout of tripler design 2 (not to scale).

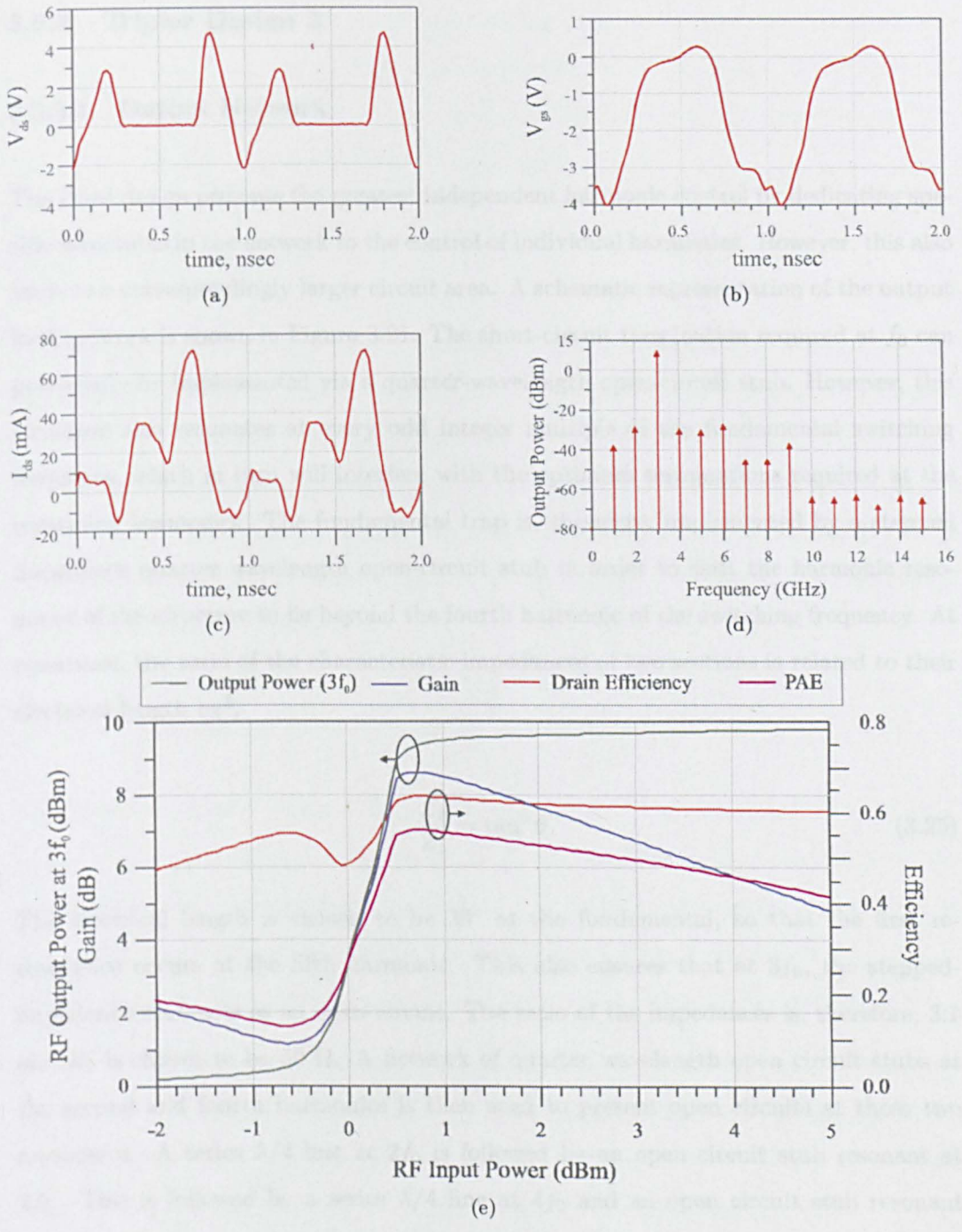


Figure 3.20: Time domain simulations of (a) drain voltage waveform (b) input drive waveform (c) drain current waveform and (d) output power spectrum of tripler design 2, biased at V_{GG}=-1.57 V and V_{DD}=0.8 V, and (e) output power at $3f_0$, conversion gain, drain efficiency and PAE as a function of input power level.

3.5.3 Tripler Design 3

3.5.3.1 Output Network

The third design presents the greatest independent harmonic control by dedicating specific structures in the network to the control of individual harmonics. However, this also leads to a correspondingly larger circuit area. A schematic representation of the output load network is shown in Figure 3.21. The short-circuit termination required at f_0 can potentially be implemented via a quarter-wavelength open-circuit stub. However, this structure also resonates at every odd integer multiple of the fundamental switching frequency, which in turn will interfere with the optimum terminations required at the remaining harmonics. The fundamental trap is, therefore, implemented by a stepped impedance quarter wavelength open-circuit stub in order to shift the harmonic resonance of the structure to lie beyond the fourth harmonic of the switching frequency. At resonance, the ratio of the characteristic impedances of two sections is related to their electrical length by[3],

$$\frac{Z_2}{Z_1} = \tan^2\theta. \tag{3.25}$$

The electrical length is chosen to be 30° at the fundamental, so that the first re-resonance occurs at the fifth harmonic. This also ensures that at $3f_0$, the stepped-impedance stub acts as an open-circuit. The ratio of the impedances is, therefore, 3:1 and Z_1 is chosen to be 50 Ω. A network of quarter wavelength open circuit stubs at the second and fourth harmonics is then used to present open circuits at these two harmonics. A series $\lambda/4$ line at $2f_0$ is followed by an open circuit stub resonant at $2f_0$. This is followed by a series $\lambda/4$ line at $4f_0$ and an open circuit stub resonant at $4f_0$. The impedance looking into this structure is therefore an open circuit at the second and fourth harmonics. A matching network beyond this is used to transform the terminating 50 Ω impedance to the optimum impedance given by (2.36).

The resulting harmonic impedances presented to the output of the device are shown in Figure 3.22(a), and the S-parameters of the structure are shown in Figure 3.22(b). At

[3]This relationship is derived in Appendix D

$3f_0$, an insertion loss of 0.6 dB is achieved with a return loss of -12.1 dB. The bond wire inductances and bond pad parasitics are accounted for in the design of the network, and the drain bias line is placed at an optimised distance from the device along TL1 to produce minimal interference with the matching circuit.

3.5.3.2 Input Network

The input network is also implemented with a network of open-circuit stubs, as shown in Figure 3.23, in order to provide short-circuit terminations at the second and fourth harmonics. A series line of $\lambda/2$ at $2f_0$ is followed by an open-circuit stub of length $\lambda/2$ at $2f_0$. This is followed by a series line of $\lambda/2$ at $4f_0$ and an open-circuit stub of length $\lambda/2$ at $4f_0$. A matching network is implemented beyond this to transform the 50 Ω internal impedance of the power generator to the conjugate match of the fundamental at the gate terminal of the device.

3.5.3.3 Complete microstrip circuit

The input and output sections along with the bias circuit are combined, and the complete layout of the design is shown in Figure 3.24. Details of the line dimensions of the matching networks are given in Appendix E. For this design, optimum operation of the tripler is achieved at a gate bias of -1.48 V and a drain bias of 0.75 V. A plot of simulated circuit performance with input power level is shown in Figure 3.25.

Switched-mode operation of the multiplier is clearly evident for input power levels above 0.3 dBm, where the output power and conversion gain begin to increase rapidly. Above an input power level of approximately 2 dBm, the rate of increase of output power begins to decline, with corresponding decrease in conversion gain and PAE.

From the simulations, a maximum drain efficiency of 68.3 % , 55.4 % PAE and 6.67 dB conversion gain at an input power level of 4.05 dBm is expected, with a DC drain supply current of 23 mA. The drain voltage and current waveforms along with the input voltage driving waveform at this operating point are shown in Figure 3.25. The drive waveform achieved resembles the requisite square-wave for optimum switching of the device with a 50 % duty cycle. It also provides adequate turn-on voltage at the gate,

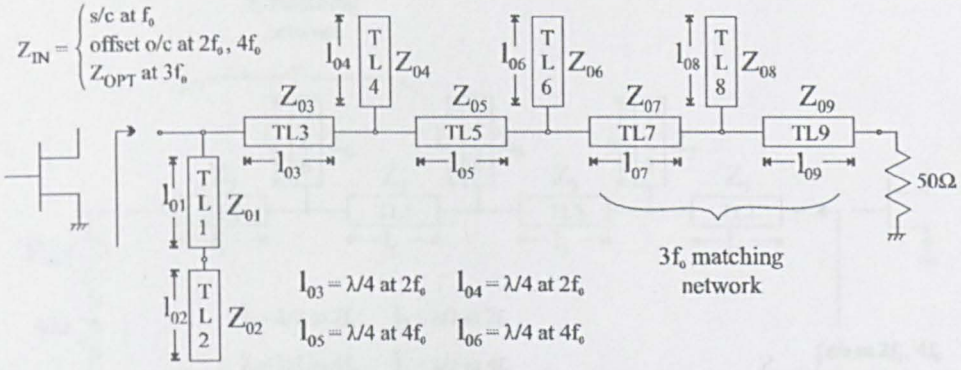


Figure 3.21: Schematic of the output matching network for tripler design 3.

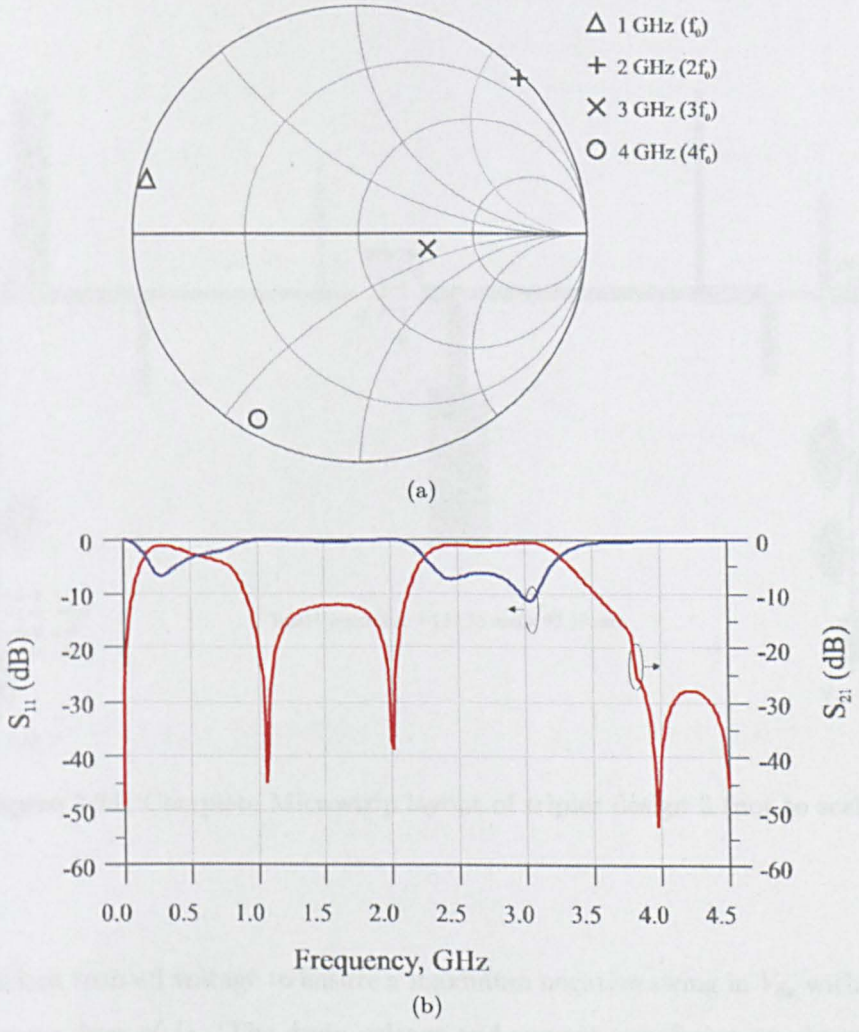


Figure 3.22: (a) Simulated harmonic impedances presented to the drain terminal of the device by the output matching network, and (b) simulated S-parameters of the the output matching network of tripler design 3.

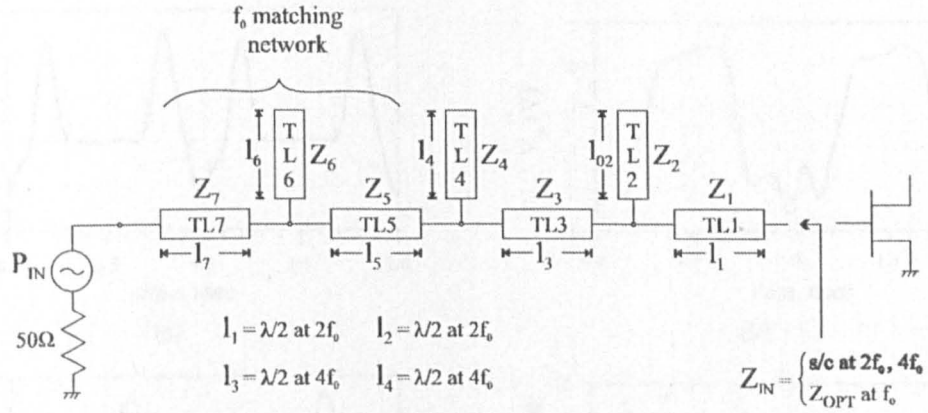


Figure 3.23: Schematic of the input matching network for tripler design 3.

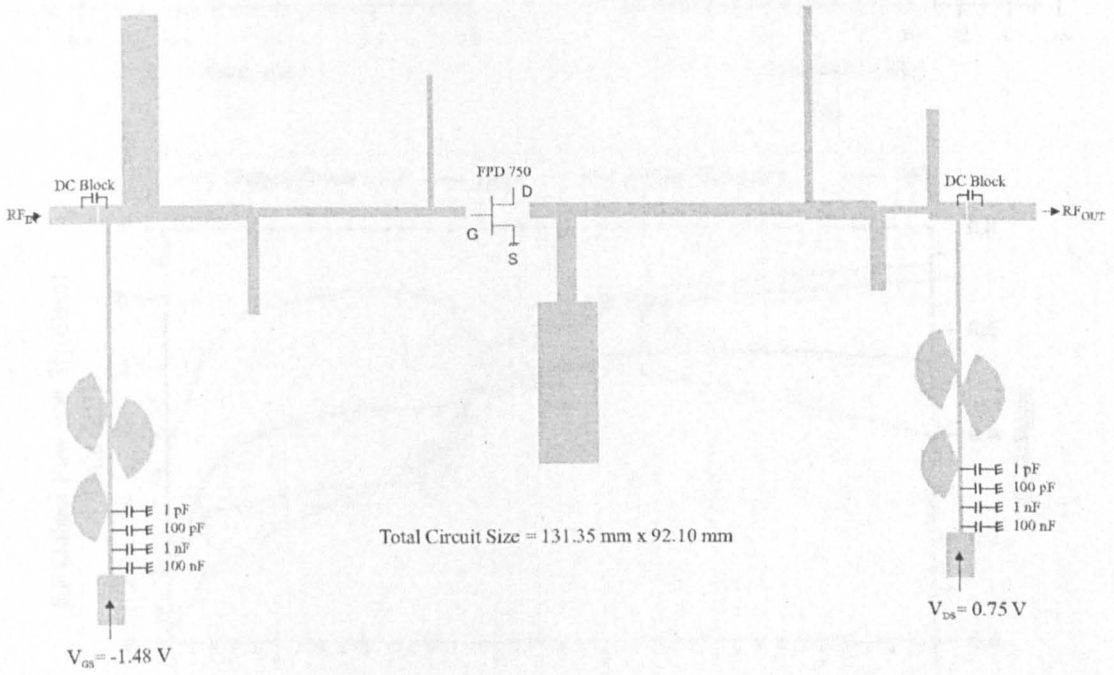


Figure 3.24: Complete Microstrip layout of tripler design 3 (not to scale).

and sufficient turn-off voltage to ensure a maximum negative swing in V_{ds} with minimal simultaneous draw of I_{ds}. The drain voltage and current waveforms are shown to have minimal overlap in time, with maximum I_{ds} occuring at a time when V_{ds} is minimal, and vice-versa, therefore ensuring a high drain efficiency. Harmonic rejection levels at the output of the tripler are shown to be better than 19.2 dBc.

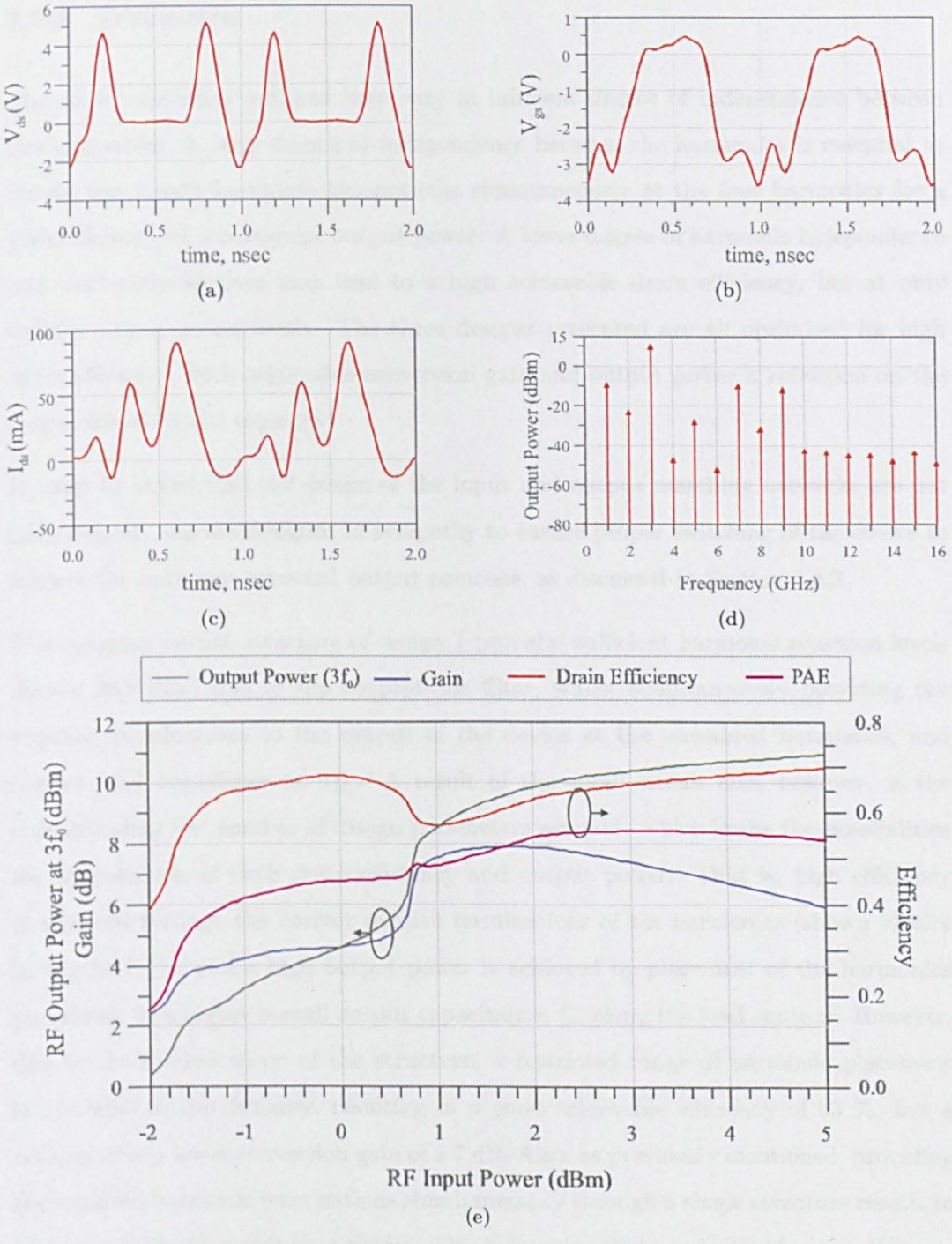


Figure 3.25: Time domain simulations of (a) drain voltage waveform (b) input drive waveform (c) drain current waveform and (d) output power spectrum of tripler design 3, biased at V_{GG}=-1.48 V and V_{DD}=0.75 V, and (e) output power at $3f_0$, conversion gain, drain efficiency and PAE as a function of input power level.

3.5.4 Discussion

The three topologies outlined here vary in inherent degree of independence between the harmonics. A large degree of independence between the harmonics is essential to obtain the correct harmonic terminations simultaneously at the four harmonics for a high efficiency at a particular output power. A lower degree of harmonic independence and microstrip sections may lead to a high achievable drain efficiency, but at only certain output power levels. The three designs presented are all optimised for high drain efficiency, with achievable conversion gain and output power a reflection on the scope offered by the topology.

It must be noted that the design of the input and output matching networks are not independent, and are designed in sympathy to ensure proper switching of the device to achieve the optimum expected output response, as discussed in Section 3.4.3.

The compact output structure of design 1 provides sufficient harmonic rejection levels (below 26.8 dBc) due to the coupled-line filter, whilst simultaneously providing the required terminations to the output of the device at the unwanted harmonics, and correct load impedance at $3f_0$. A result of the small circuit size, however, is the corresponding low number of design parameters available which limits the possibilities for optimisation of both drain efficiency and output power. That is, high efficiency is achieved through the correct relative terminations of the harmonics (shown ideally in Figure 2.15), and a high output power is achieved by placement of the harmonics pertaining to a higher overall output capacitance, C, along the load contour. However, due to the limited scope of the structure, a restricted range of harmonic placement is available to the designer, resulting in a good achievable efficiency of 63 %, but a comparatively lower conversion gain of 2.7 dB. Also, as previously mentioned, providing the required harmonic terminations simultaneously through a single structure results in high sensitivity to circuit parameters. This is because slight variation due to tolerances has a combined effect on all the harmonics, thus departing quite significantly from the design.

An improved degree of harmonic independence is offered by the load network of design 2, but with a correspondingly larger circuit size and complexity. Adequate harmonic rejection levels of 36.7 dBc is achieved with the coupled-line structure, and a high drain

efficiency of 63.5 % is expected. The improved harmonic independence, however, is evident in the much improved expected conversion gain of 8.6 dB at an input power level of 0.7 dBm, with the circuit capable of being optimised for both a high drain efficiency and output power.

The network topology of design 3 provides individual structures to the control of each of the harmonics, therefore providing the most harmonic independence with improved scope of simultaneous high achievable drain efficiency and output power. A maximum drain efficiency of 68.3 % is expected with a corresponding conversion gain of 6.67 dB at an input power level of 4.05 dBm. The harmonic rejection levels, however, are compromised at 19.2 dBc, mainly due to the presence of high fundamental and seventh harmonic components at the load termination. The rejection levels provided by the stepped impedance quarter-wavelength line is not sufficient, and can be enhanced by providing a greater impedance ratio given in (3.25), and is demonstrated in an improved circuit presented in the next chapter. The insertion loss of the output network at $3f_0$, however, is much improved at 0.6 dB compared to 1.2 dB and 1.5 dB of designs 1 and 2 respectively, due to the absence of a coupled-line structure.

A sensitivity analysis was performed for all three designs, in order to predict the percentage change in tripler performance from the optimum cases with a 1 % change in design variables. The results are summarised in Table 3.5.4. It is seen that the most sensitive structure for both designs 1 and 2 is the coupled-line filter. In design 1, the first section of the filter (l_{02} in Figure 3.10) produces the most change in circuit performance, resulting in a 23 % reduction in drain efficiency, with the second section of the filter (l_3 in Figure 3.10) resulting in a 10.5 % reduction. As expected, design 2 is comparatively less sensitive, with the first section of the filter (l_{06} in Figure 3.17) resulting in a 2.7 % reduction in drain efficiency, and the second section (l_{07} in Figure 3.17) producing a 5.2 % reduction. As expected, design 3 provides the least sensitive alternative with the most harmonic independence, with the $4f_0$ stub (l_{06} in Figure 3.21) producing a 0.47 % decrease in drain efficiency, and the $3f_0$ matching stub (l_{08} in Figure 3.21) producing a 1.1 % reduction.

It must also be noted that the unwanted output harmonic terminations presented by all three designs are independent of the terminating 50 Ω load. This implies that any

	Drain Efficiency	Output Power	Gain
Design 1			
l_{02}	23.4 %	10.5 %	15.7 %
l_{03}	10.5 %	6.8 %	10.2 %
Design 2			
l_{06}	2.7 %	5.5 %	2.6 %
l_{07}	5.2 %	13.8 %	6.5 %
Design 3			
l_{06}	0.47 %	3.6 %	2.0 %
l_{08}	1.1 %	1.6 %	0.9 %

Table 3.2: Sensitivity Analysis of the Tripler Designs - percentage change in tripler performance with 1 % change in the most sensitive circuit parameters.

circuit that immediately follows the tripler (for e.g. a mixer) needs only be matched at $3f_0$, thus easing the requirements for the interstage matching circuitry.

3.6 Conclusions

This chapter has provided a comprehensive discussion of all design aspects for the proposed class E triplers. Measurements of the chosen pHEMT device demonstrate the suitability of the TOM3 model in the design of class E triplers. The impact of device size on circuit performance is discussed and the corresponding compromises in drain efficiency, conversion gain and output power are identified.

Subsequent assessment of potential circuit technologies favours microstrip implementation of the tripler over lumped element or quasi-lumped alternatives, due to the self-resonant properties of the former and narrow-band nature of the latter.

Design consideration for the microstrip tripler are then presented, with an evaluation of the trade-offs involved by limiting the number of controlled harmonics. It is shown that control of the first four harmonics provides a sufficient compromise between tripler performance and circuit complexity.

A study into the requirements of the input and output matching networks and the bias networks is included, and with these taken into consideration, three microstrip tripler designs are proposed. Simulations of the three designs demonstrate their potential to achieve high drain efficiencies and adequate harmonic rejection levels. With the circuits optimised for maximum drain efficiency, the achievable output powers and conversion

gains of the three designs are shown to be dependent on the degree of harmonic independence inherent in the load networks. The greater the harmonic independence, the greater the possibility for simultaneous high output power and drain efficiency; however as shown, this also leads to an increase in circuit size and complexity.

The following chapter details the practical demonstration of the three 3 GHz triplers, including circuit fabrication techniques and measured results.

Chapter 4

Realisation and Evaluation of the Novel Frequency Triplers

4.1 Introduction

Simulations of the three proof-of-concept 3 GHz class E tripler designs presented in Chapter 3 demonstrated their potential for high achievable drain efficiency, output power and conversion gain with suitable harmonic rejection levels. This chapter details the practical implementation of the triplers, including circuit fabrication procedures, measurement set-up and experimental characterisation. This is the first reported demonstration of class E frequency triplers, with all three designs achieving better than the previous highest reported drain efficiency, and two designs also bettering the highest reported conversion gain for microwave frequency triplers.

4.2 Circuit Fabrication

The input and output matching circuits of the three tripler designs described in Chapter 3, were realised on 31 mil RT/Duroid 5880, with a dielectric constant (ϵ_r) of 2.2 and metallisation thickness of 0.017 mm. The circuits were mounted on an aluminium block for mechanical support and to provide grounding.

For the first iteration of the circuits, a bare-die FPD750 device was mounted onto a thin vertical microstrip line between the input and output matching circuits, and screws were used to ground the copper strip to the aluminium block beneath. The source of the device was then wire-bonded to the microstrip line. However, a degradation in

performance of these circuits was observed, and attributed in part to the unforeseen additional inductance introduced by the threads of the screws. Additional source inductance is detrimental to the tripler performance, as the optimum multiharmonic impedances presented to both input and output of the device are altered.

In view of this, an improved structure for die attachment and grounding was designed. An elevated ridge in the aluminium ground block was introduced (as shown in Figure 4.1), which incorporates a small platform to which the device is attached using silver epoxy. The input and output matching circuits are positioned on either side of the ridge, and the gate and drain of the device are wire-bonded to these respectively. The source is grounded by wire-bonding to gold discs that are mounted on the ground ridge and attached using conductive silver epoxy. This arrangement, shown in Figure 4.2, provides a more direct connection of the source to the ground. This not only reduces the parasitic source inductance but allows more accurate modelling of the connection to ensure optimum impedance is presented to the device. Wire-bonding was performed using a Kulicke and Soffa Industries wedge-bonding station, with 17 μm diameter gold wire that is ultrasonically fused at each end to form a low resistance electrical connection between the device and microstrip circuit. Bondwire inductance is estimated to be 0.9 nH/mm, according to (3.8).

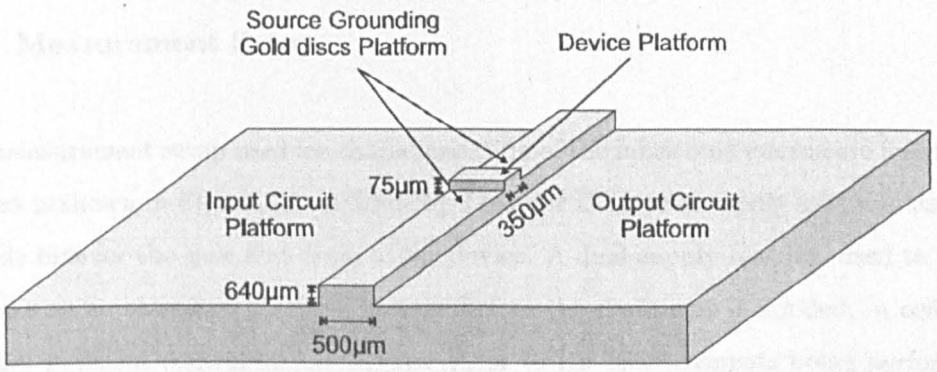


Figure 4.1: Aluminium ground block designed to house a bare-die FPD750 pHEMT device and the fabricated RT/Duroid input and output matching circuits, in order to minimise the parasitic effects introduced through interconnections between the circuit and device (not to scale).

Passive components, including the decoupling capacitors of 1 pF, 100 pF, 1 nF and 100 nF, and DC blocking capacitors are soldered to the microstrip. ATC Broadband 520L

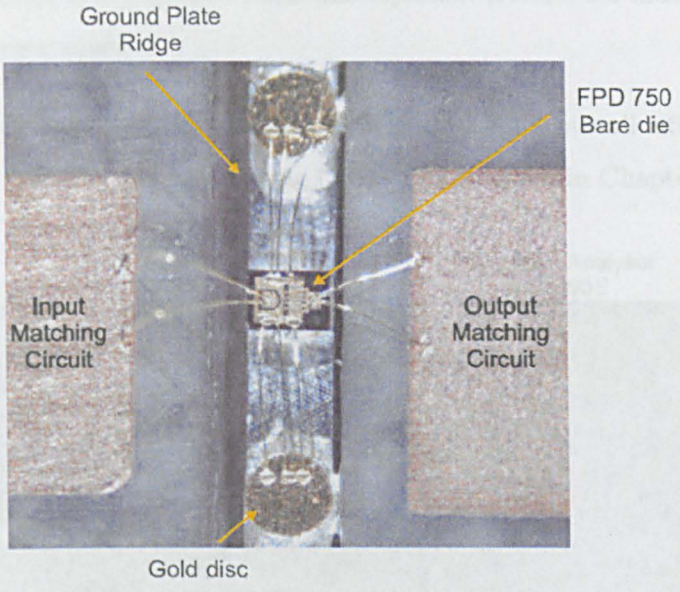


Figure 4.2: Photograph of the FPD750 bare-die pHEMT device bonded to the external matching networks and aluminium ground block.

10 nF capacitors are used as DC blocks, and exhibit an insertion loss of better than 0.6 dB up to 10 GHz. SMA connectors are used to connect RF measurement ports to the input and output ports of the circuits.

4.3 Measurement Setup

The measurement setup used for characterisation of the fabricated microwave frequency triplers is shown in Figure 4.3. A Thurlby-Thandar DC power supply unit was used to provide bias for the gate and drain of the device. A dual-supply bias was used to allow the gate to be biased at pinch-off voltage before the drain bias is applied, in order to exercise sufficient control on the device. Prior to RF measurements being performed, the stability of the device was ensured by terminating the input with a 50 Ω load and monitoring the output of the circuit with the HP8593E spectrum analyser. A sweep of gate and drain bias over the expected range of voltages affirmed the stability of the device.

For RF measurements, an HP8340A signal generator was used to provide the input RF signal at the fundamental frequency of 1 GHz. The output power of the tripler at the

third harmonic and the unwanted harmonic rejection levels were measured using the HP8593E spectrum analyser.

DC/RF efficiency ($\eta_{DC/RF}$), Power-added-efficiency (PAE), overall efficiency ($\eta_{overall}$) and conversion gain are calculated using (1.8) - (1.11), given in Chapter 1.

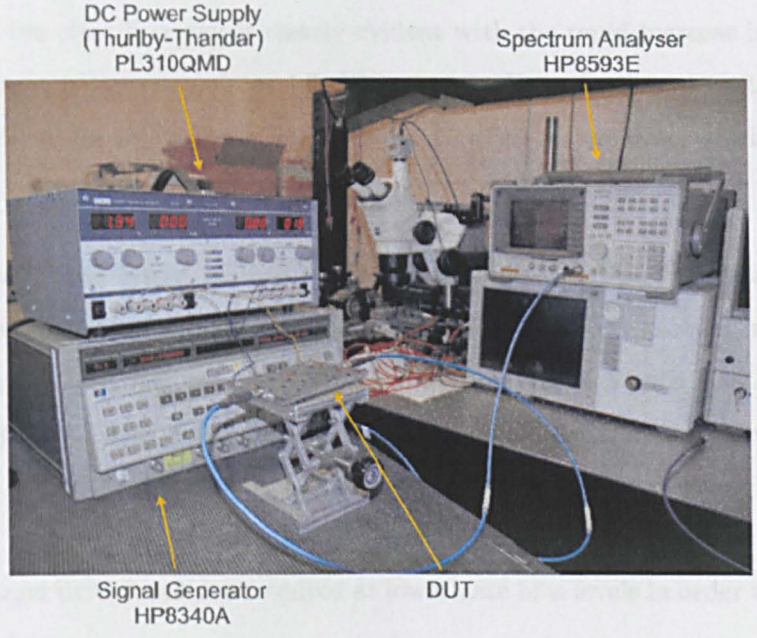


Figure 4.3: Measurement setup of the hybrid MIC class E frequency triplers.

4.4 Experimental Characterisation

4.4.1 Tripler Design 1

A photograph of the fabricated hybrid MIC tripler is shown in Figure 4.4, detailing the complete construction of the test circuit including the aluminium mounting block, RT/Duroid 5880 input and output matching circuits, gate and drain biasing networks and the RF SMA connectors for connection to the measurement ports. DC/RF efficiency of the tripler was measured as a function of RF input power, drain bias voltage, V_{DS} and gate bias voltage, V_{GG}.

Preliminary measurements of the tripler indicated that optimum performance occurs at a switching frequency of 990 MHz, an offset of 10 MHz from the design value. Initial

measurements also revealed that optimum operation is achieved at $V_{GG} = -1.9$ V, which is in excellent agreement with that predicted. With the gate first biased at -1.9 V, $\eta_{DC/RF}$ was measured as a function of input power level and V_{DD}, and the results are shown in Figure 4.5. It can be seen that maximum $\eta_{DC/RF}$ is achieved at $V_{DD} = 0.5$ V, which agrees relatively well with the predicted value of 0.4 V. The onset of switching behaviour of the class E tripler is clearly evident with the rapid increase in $\eta_{DC/RF}$ as the input power is increased from 1.7 dBm to 2.7 dBm. Optimum switching of the device is achieved for input power levels above 3.2 dBm, where drain efficiency reaches a peak value of 29 %.

The circuit was then biased at $V_{DD} = 0.5$ V, and drain efficiency was measured for a range of input power levels and values of V_{GG}. The results are plotted in Figure 4.6, where it can be seen that maximum $\eta_{DC/RF}$ is achieved at a gate bias level of -1.9 V. At this operating bias point, optimum switching of the circuit is achieved for input power levels above 2.7 dBm. Also apparent is that as V_{GG} is decreased, higher input power levels are required for the onset of switched-mode operation of the tripler. This is because larger drive levels are required at lower gate bias levels in order to sufficiently turn on the device.

A cross-section of the optimum $\eta_{DC/RF}$, PAE and conversion gain performance achieved for the operating point of $V_{DD} = 0.5$ V and $V_{GG} = -1.9$ V, is shown in Figure 4.7(a). A rapid rise in conversion gain and PAE is observed for input levels above 2.7 dBm, indicating switched-mode operation of the tripler. A clear distinction between off and on states is demonstrated, with PAE and conversion gain achieving positive values for input power levels above 2.7 dBm. A maximum unprecedented $\eta_{DC/RF}$ of 29 % is achieved, with a conversion gain of 1.8 dB at an input power level of 3.2 dBm, with a simultaneous PAE of 9.6 %. The overall efficiency is measured to be 24 %, and a low DC drain current of 22 mA is drawn at this optimum operating point.

Figure 4.7(b) depicts the measured output power levels at the load at the desired harmonic $3f_0$, and the unwanted harmonics f_0, $2f_0$ and $4f_0$, as a function of input power level. The rapid increase in output power at $3f_0$ as input power is increased above 2.7 dBm indicates optimum switched-mode operation of the device, as expected from the previous measurements. Above 2.7 dBm, the unwanted harmonic rejection

levels are shown to be better than 23 dBc. Further increases in input power beyond 3.2 dBm do not result in an increase in output power as expected, due to switched-mode operation being achieved and the maximum output power deliverable from the load network being obtained. This results in a decrease in conversion gain and PAE beyond an input power level of 3.2 dBm, as seen in Figure 4.7(a).

The output power spectrum of the tripler at the optimum operating point of $V_{DD} = 0.5$ V, $V_{GG} = -1.9$ V and input power of 3.2 dBm, is shown in Figure 4.8. Unwanted harmonic rejection levels are shown up to the fifth harmonic, and are better than 23 dBc.

The fabricated tripler presented in this section is the first ever demonstration of a class E frequency tripler, and achieves the highest reported drain efficiency to date for a microwave tripler (see Table 4.1, Section 4.5). The low featured drain supply voltage of 0.5 V, a DC current consumption of 22 mA, and a low required input power level of 3.2 dBm makes it particularly suitable for power-critical systems in wireless applications (as discussed in chapter 1). The tripler also features a high output power at the third harmonic with sufficient rejection of the unwanted harmonics.

As predicted in chapter 3, however, the performance of the tripler is quite sensitive to circuit parameters, resulting in a deviation from expected performance. A measured offset of 10 MHz in fundamental frequency of operation can be seen to be partly due to the mismatch in measured and modelled S-parameters of the output matching circuit at the relevant harmonics, as shown in Figure 4.9. It can be seen that 990 MHz provides a closer match to the required terminations, especially at $3f_0$ and $4f_0$. Variations in device characteristics can also contribute to the shift from expected performance, with a measured pinch-off voltage of -0.85 V compared to a modelled value of -1.0 V, leading to a lower than expected input power for switched-mode operation. Additionally, where a DC drain current, I_{DS}, of 219 mA is expected at $V_{DD} = 0.5$ V and $V_{GG} = 0$ V, a current of only 197 mA was obtained, indicating a higher than expected on-resistance, with subsequent reduction in drain efficiency and output power.

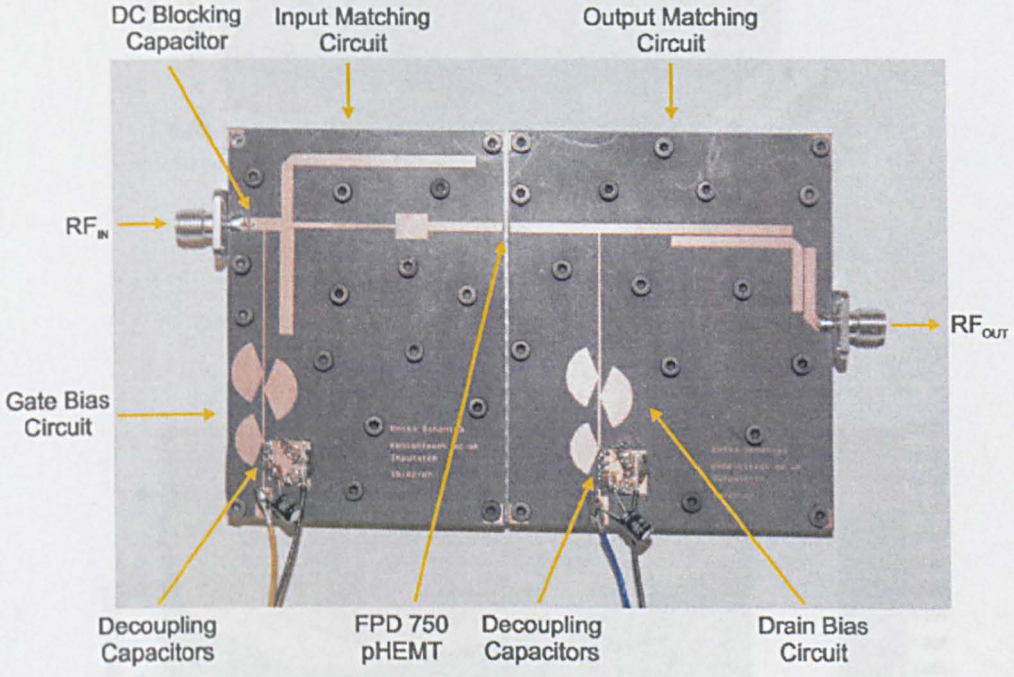
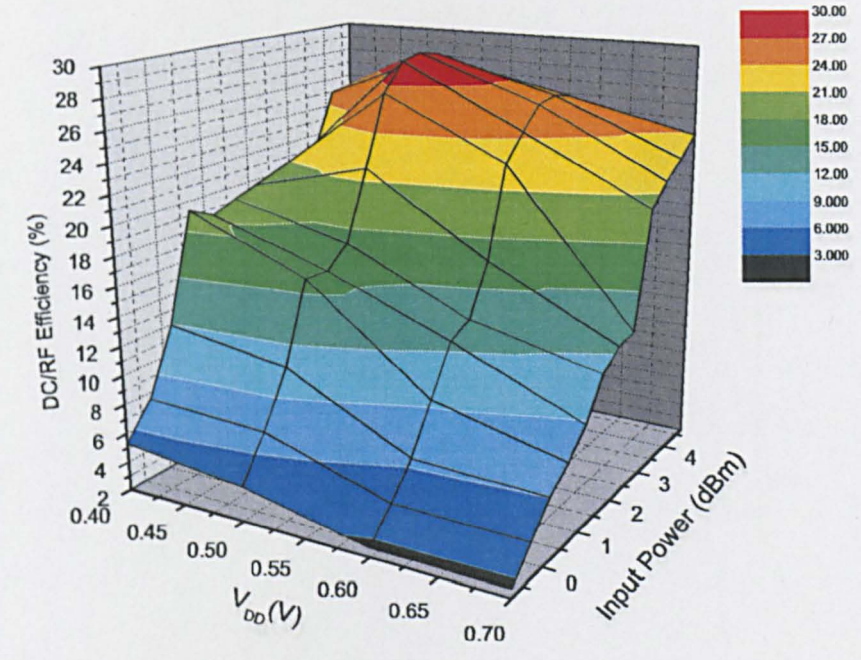
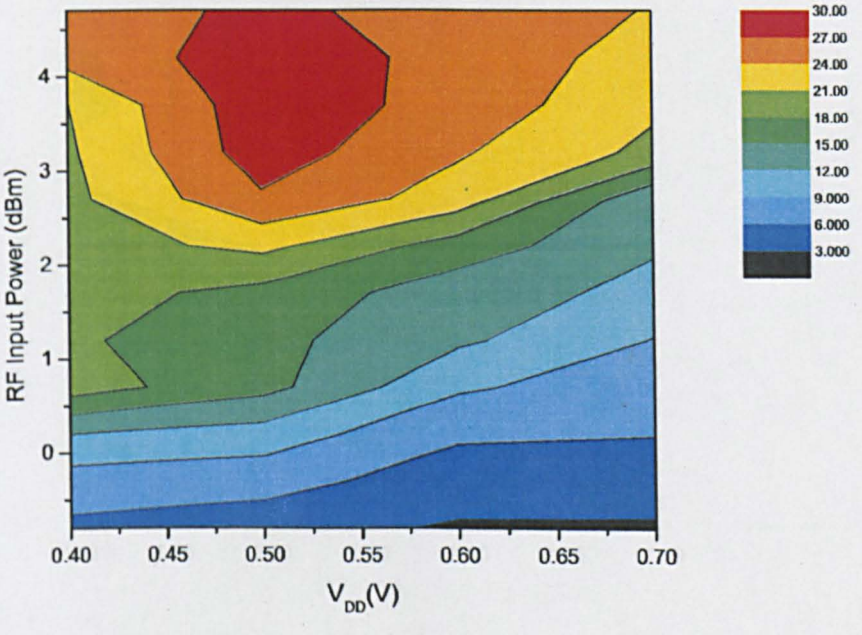


Figure 4.4: Photograph of the fabricated hybrid MIC implementation of Frequency Tripler Design 1. The circuit measures 7.5 cm by 11.5 cm.

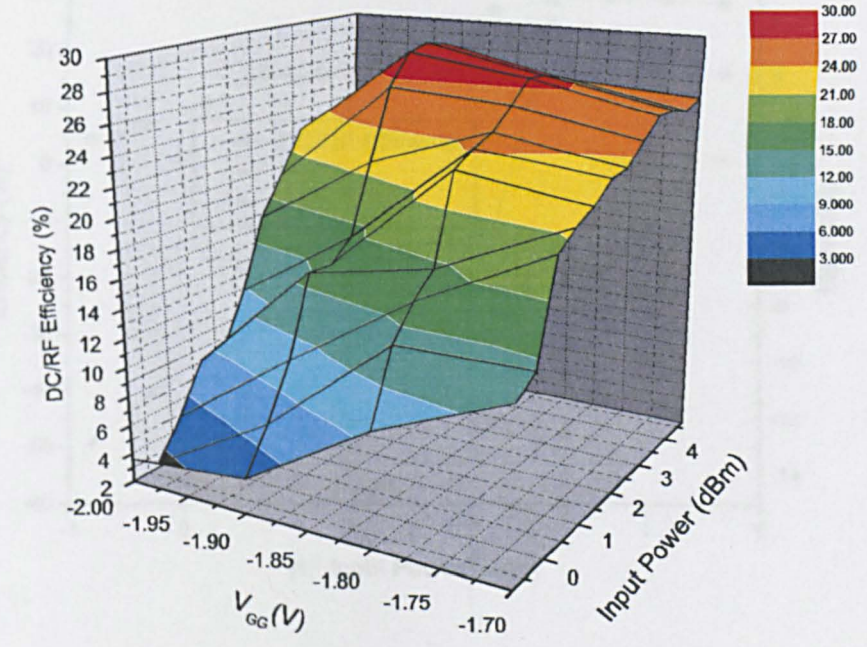


(a)

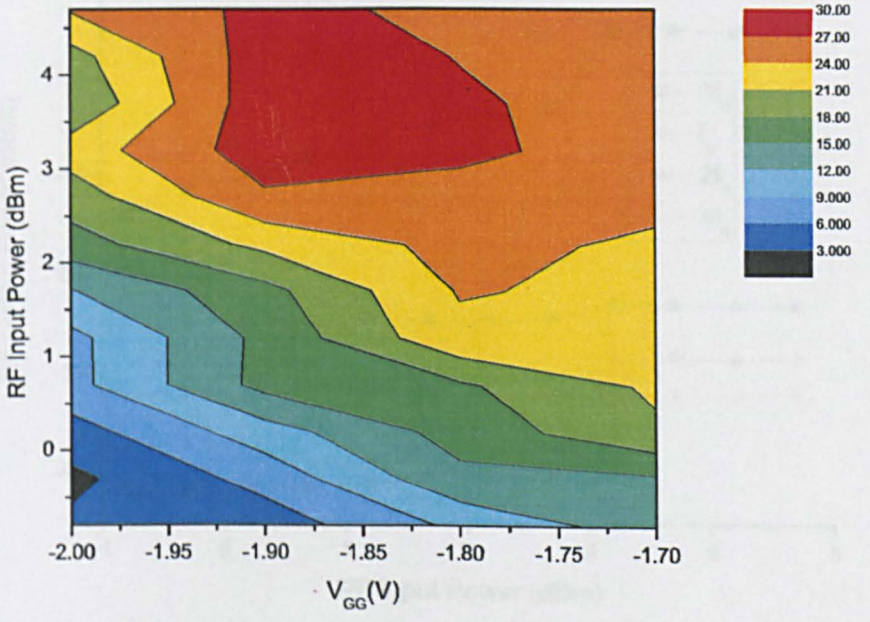


(b)

Figure 4.5: Tripler Design 1: Measured (a) Drain efficiency vs. drain bias (V_{DD}) and input power level for $V_{GG} = -1.9$ V, and (b) contour plot of the same. Maximum efficiency is achieved at $V_{DD} = 0.5$ V at an input power level of 3.2 dBm.

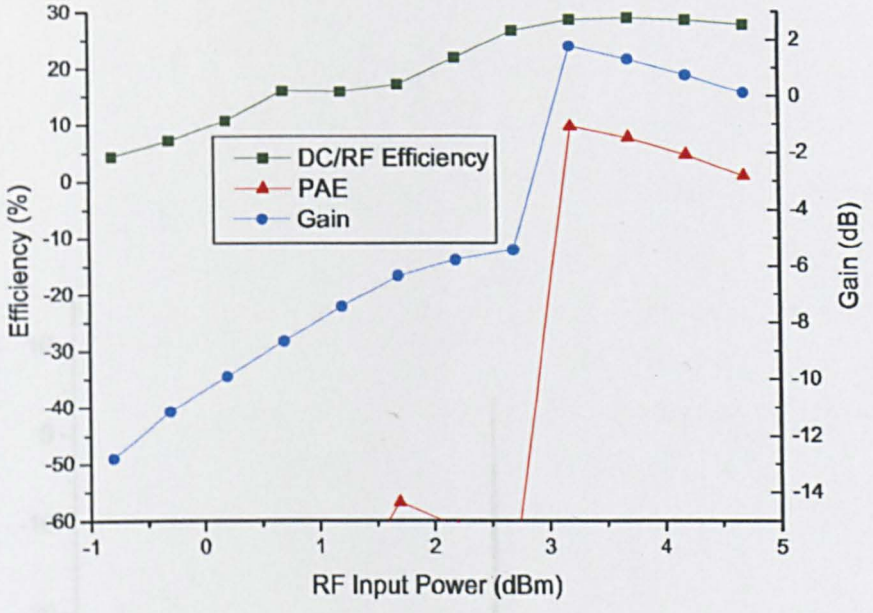


(a)

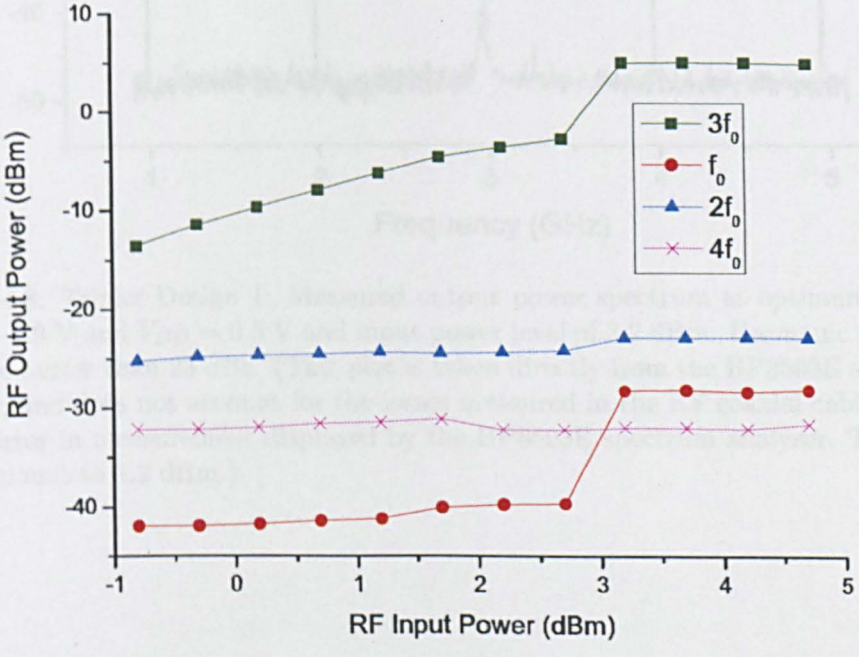


(b)

Figure 4.6: Tripler Design 1: Measured (a) Drain efficiency vs. gate bias (V_{GG}) and input power level for $V_{DD} = 0.5$ V, and (b) contour plot of the same. Maximum efficiency is achieved at $V_{GG} = -1.9$ V at an input power level of 3.2 dBm.



(a)



(b)

Figure 4.7: Tripler Design 1: Measured (a) Drain efficiency, Power-Added-Efficiency and Gain vs. Input power and (b) Output power at $3f_0$ and unwanted harmonic rejection levels at optimum bias levels of $V_{GG} = -1.9$ V and $V_{DD} = 0.5$ V.

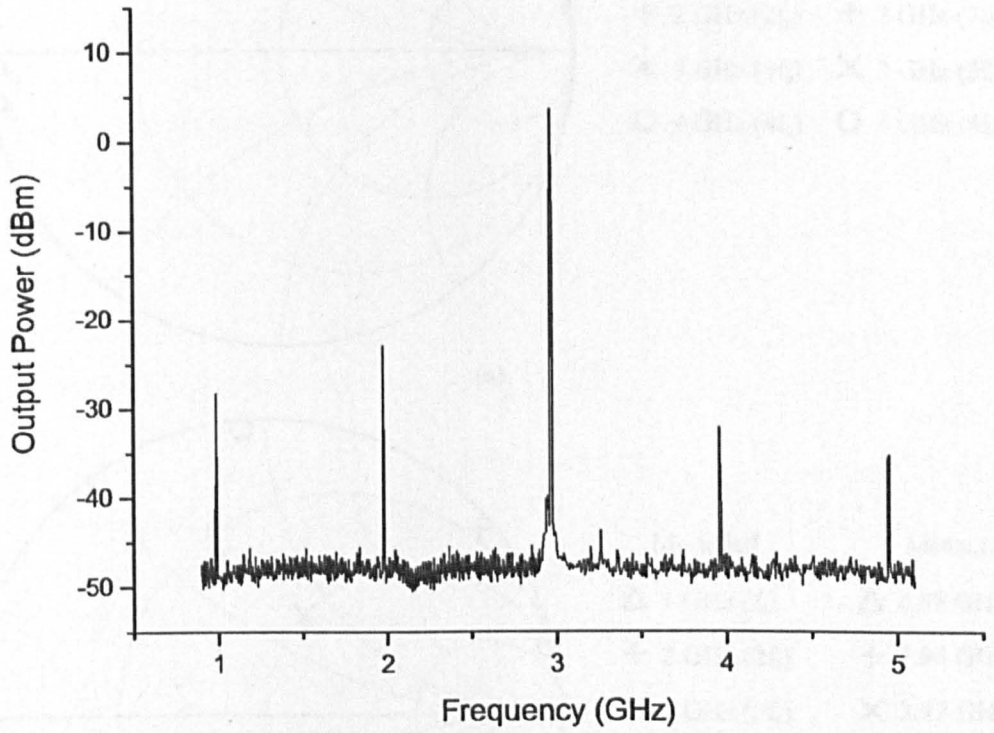


Figure 4.8: Tripler Design 1: Measured output power spectrum at optimum bias of $V_{GG} = -1.9$ V and $V_{DD} = 0.5$ V and input power level of 3.2 dBm. Harmonic rejection levels are better than 23 dBc. (This plot is taken directly from the HP8593E spectrum analyser, and does not account for the losses measured in the RF coaxial cables and a known error in measurement displayed by the HP8593E spectrum analyser. The total losses amount to 1.2 dBm.)

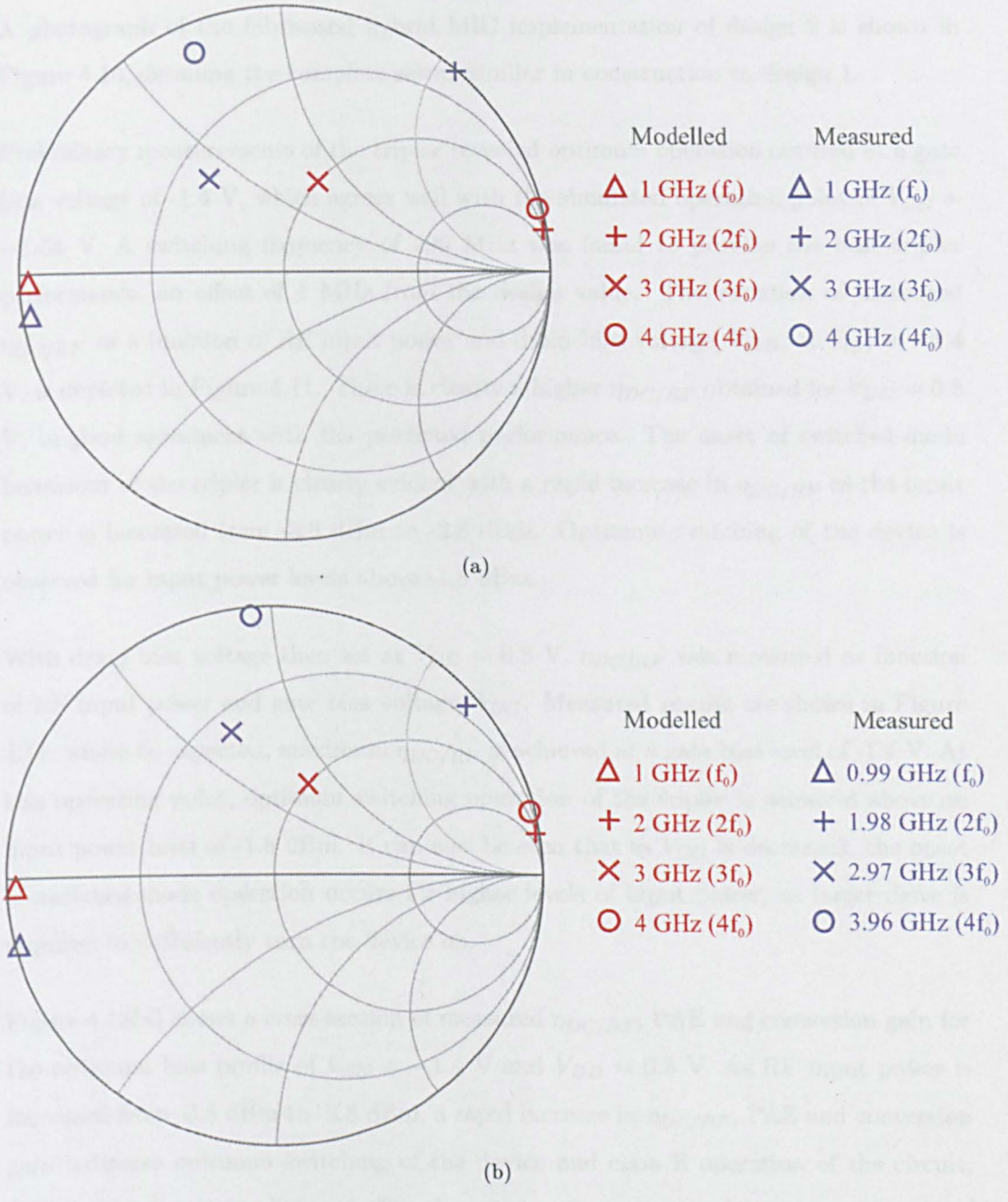


Figure 4.9: (a) Measured and modelled impedances presented to the device by the output matching network at the required harmonic, $3f_0$, and unwanted harmonics, f_0, $2f_0$ and $4f_0$ at $f_0 = 1$ GHz and (b) measured at $f_0 = 0.99$ GHz and modelled at $f_0 = 1$ GHz.

4.4.2 Tripler Design 2

A photograph of the fabricated hybrid MIC implementation of design 2 is shown in Figure 4.10, detailing the complete setup, similar in construction to design 1.

Preliminary measurements of the tripler revealed optimum operation occured at a gate bias voltage of -1.4 V, which agrees well with the simulated operating point of $V_{GG} = -1.54$ V. A switching frequency of 999 MHz was found to provide the best tripler performance, an offset of 1 MHz from the design value. The variation of measured $\eta_{DC/RF}$ as a function of RF input power and drain bias voltage, V_{DD}, at $V_{GG} = -1.4$ V, is depicted in Figure 4.11. There is clearly a higher $\eta_{DC/RF}$ obtained for $V_{DD} = 0.8$ V, in good agreement with the predicted performance. The onset of switched-mode behaviour of the tripler is clearly evident with a rapid increase in $\eta_{DC/RF}$ as the input power is increased from -3.8 dBm to -2.8 dBm. Optimum switching of the device is observed for input power levels above -1.8 dBm.

With drain bias voltage then set at $V_{DD} = 0.8$ V, $\eta_{DC/RF}$ was measured as function of RF input power and gate bias voltage, V_{GG}. Measured results are shown in Figure 4.11, where as expected, maximum $\eta_{DC/RF}$ is achieved at a gate bias level of -1.4 V. At this operating point, optimum switching operation of the tripler is achieved above an input power level of -1.8 dBm. It can also be seen that as V_{GG} is decreased, the onset of switched-mode operation occurs for higher levels of input power, as larger drive is required to sufficiently turn the device on.

Figure 4.13(a) shows a cross-section of measured $\eta_{DC/RF}$, PAE and conversion gain for the optimum bias profile of $V_{GG} = -1.4$ V and $V_{DD} = 0.8$ V. As RF input power is increased from -3.8 dBm to -2.8 dBm, a rapid increase in $\eta_{DC/RF}$, PAE and conversion gain indicates optimum switching of the device and class E operation of the circuit, with a clear distinction between off and on states. An exceptional maximum $\eta_{DC/RF}$ of 47 % is achieved at an input power level of -0.3 dBm, with a simultaneous PAE of 37.2 % and conversion gain of 6.8 dB. The overall efficiency at this optimum operating point is measured to be 42.8 %, with a DC drain current of 12 mA. A maximum conversion gain of 8.6 dB is obtained at an input power level of -2.8 dB, with a corresponding drain efficiency of 43 % and PAE of 37 %.

Figure 4.13(b) depicts measured output power at the load at the required harmonic, $3f_0$, and the unwanted harmonics, f_0, $2f_0$ and $4f_0$, as a function of input power level. The sharp increase in output power at $3f_0$ as the input power is increased from -3.8 dBm to -3.3 dBm is in accordance with the efficiency and gain trends seen in Figure 4.13(a), and suggests that switching of the device is achieved at these power levels. Above -2.8 dBm the output power is nearly constant and corresponds to the optimum output power that the load network is designed to provide. Harmonic rejection levels are shown to be better than 34 dBc above an input power level of -2.8 dBm.

The output power spectrum of the tripler at the optimum operating profile of $V_{GG} = -1.4$ V and $V_{DD} = 0.8$ V at an input power of -0.3 dBm, is shown in Figure 4.14. Unwanted harmonic rejection levels are shown up to the fifth harmonic, and are better than 34.1 dBc.

The tripler presented is one of the first reported demonstrations of a class E frequency tripler. It achieves an unprecedented drain efficiency of 47 %, with the next most efficient tripler reported at 16 % (see Table 4.1, Section 4.5). It simultaneously achieves a high conversion gain of 6.8 dB, with a maximum achievable conversion gain of 8.6 dB, the highest reported conversion gain figures for a microwave frequency tripler. With a low required drain supply bias of 0.8 V, a DC consumption of 12 mA, and a low required input power level of -0.3 dBm, this design clearly demonstrates its advantages in power-critical systems (such as wireless applications). The tripler also achieves exceptional unwanted harmonic rejection at 34.1 dBc, with a high third harmonic output power level of 6.5 dBm.

Measured and modelled S-parameters of the output matching circuit at the relevant harmonics are shown in Figure 4.15, where it can be seen that a satisfactory correlation is achieved up to the third harmonic. A resonance in the drain bias structure at the fourth harmonic was tuned out during EM optimisation of the output matching circuit; however, from Figure 4.15 it is evident that more accurate simulations are required to provide a better match at $4f_0$. Variations in device performance were also noted, with a lower than expected pinch-off voltage of -0.8 V, leading to a reduced input power level for the onset of switched-mode behaviour.

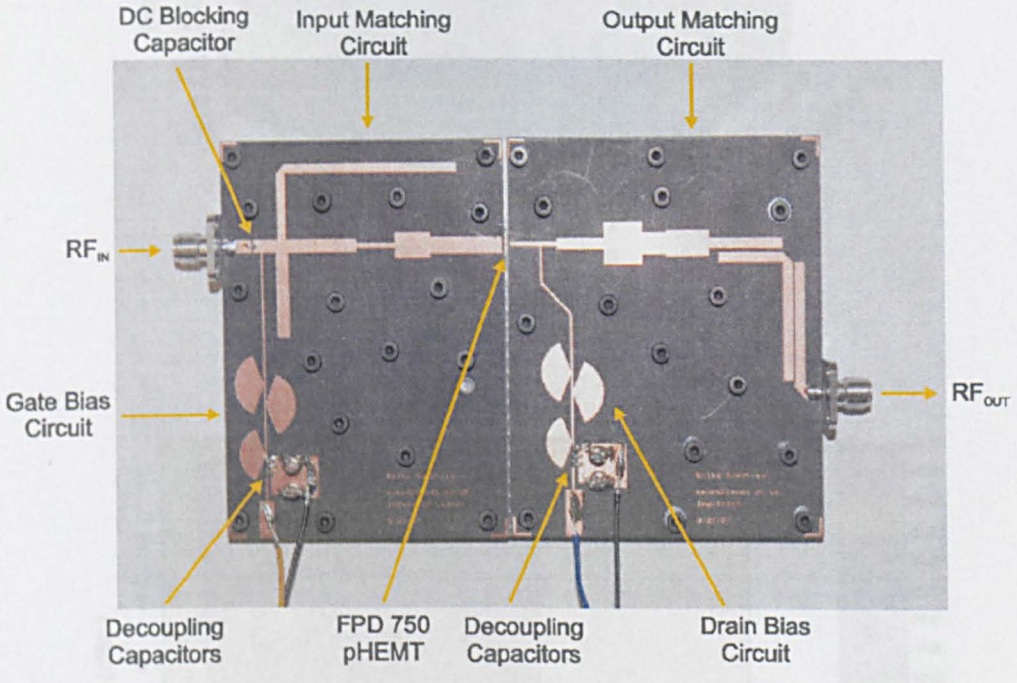
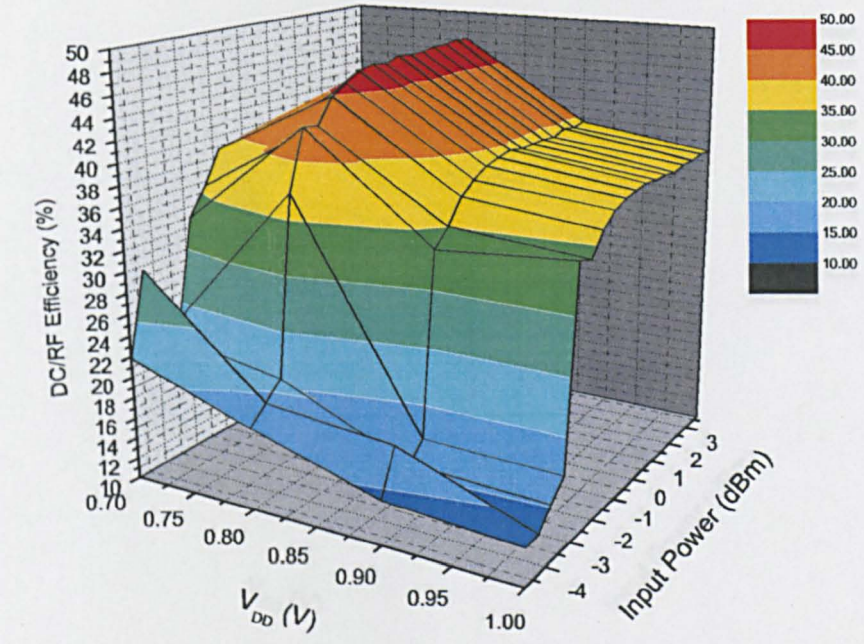
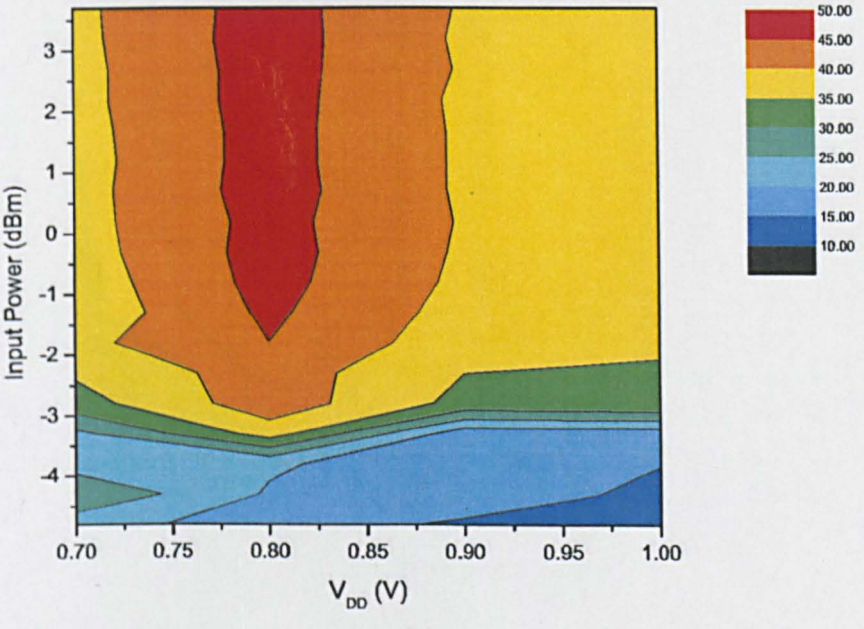


Figure 4.10: Photograph of the fabricated hybrid MIC implementation of Frequency Tripler Design 2. The circuit measures 7.5 cm by 12.1 cm.

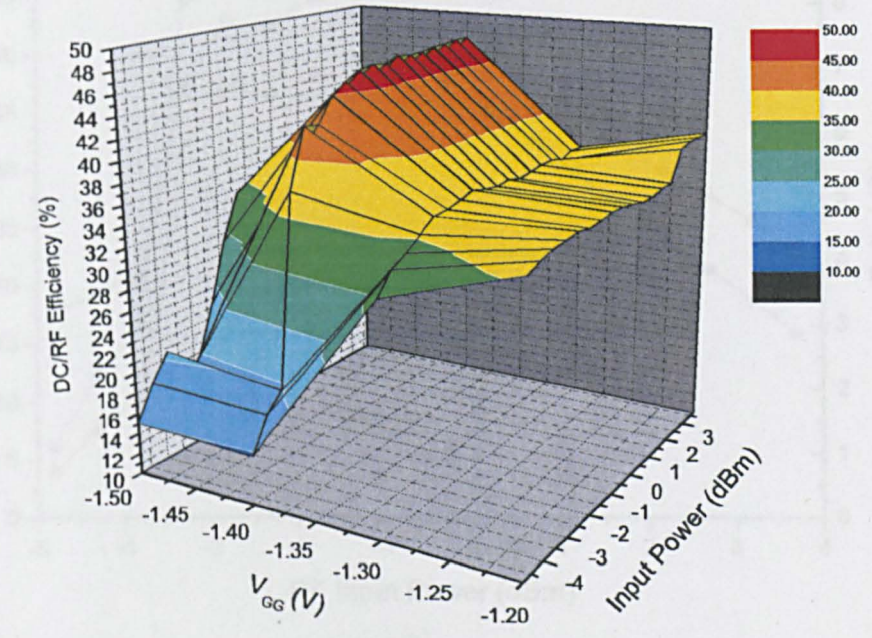


(a)

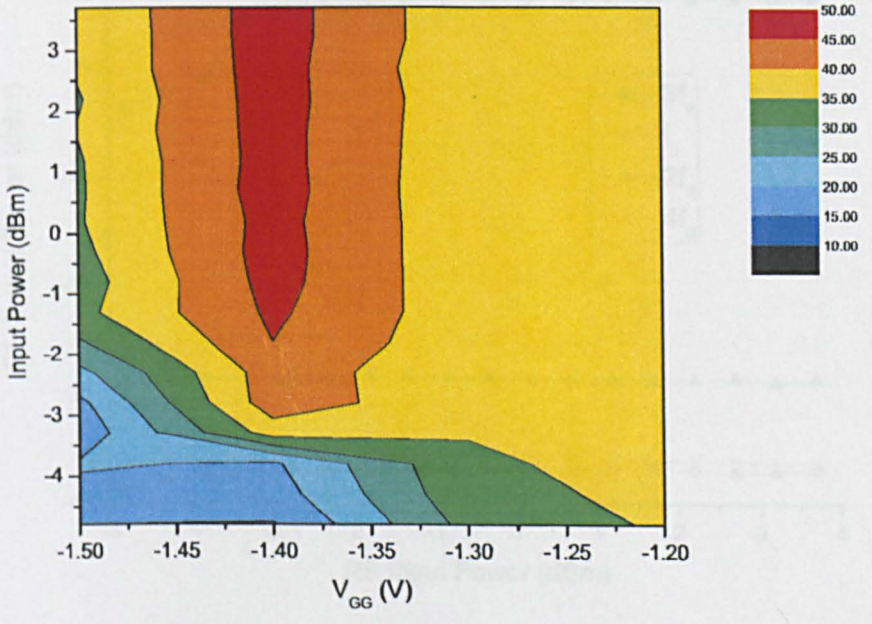


(b)

Figure 4.11: Tripler Design 2: Measured (a) Drain efficiency vs. drain bias (V_{DD}) and input power level for $V_{GG} = -1.4$ V, and (b) contour plot of the same. Maximum efficiency is achieved at $V_{DD} = 0.8$ V at an input power level of -0.3 dBm.

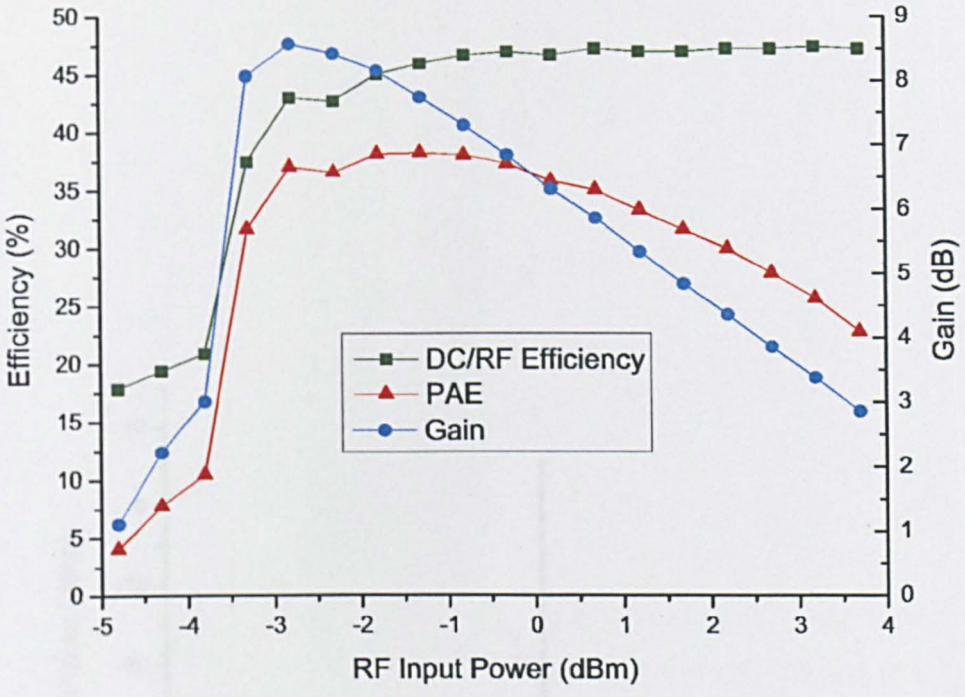


(a)

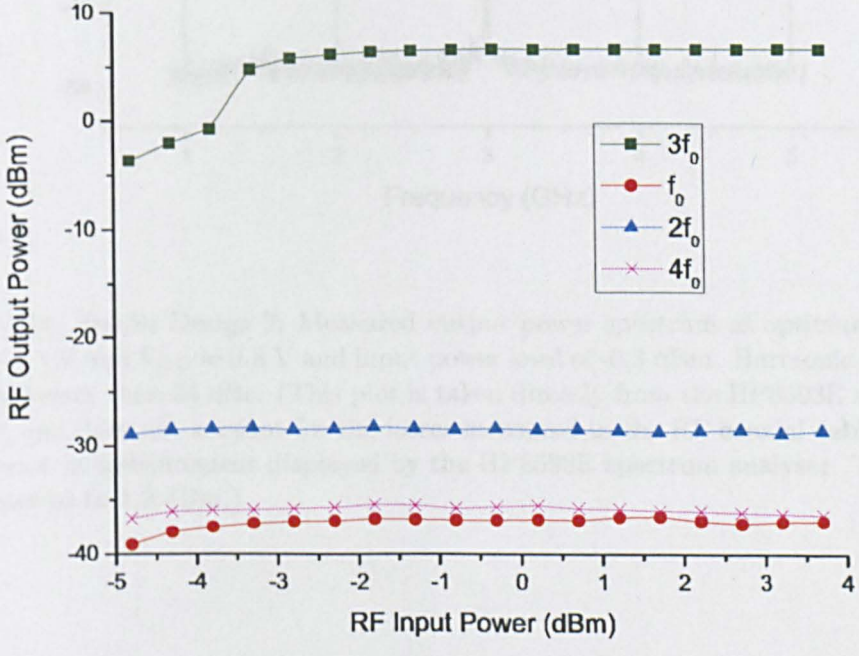


(b)

Figure 4.12: Tripler Design 2: Measured (a) Drain efficiency vs. gate bias (V_{GG}) and input power level for $V_{DD} = 0.8$ V, and (b) contour plot of the same. Maximum efficiency is achieved at $V_{GG} = -1.4$ V at an input power level of -0.3 dBm.



(a)



(b)

Figure 4.13: Tripler Design 2: Measured (a) Drain efficiency, Power-Added-Efficiency and Gain vs. Input power, and (b) Output power at $3f_0$ and unwanted harmonic rejection levels at optimum bias levels of $V_{GG} = -1.4$ V and $V_{DD} = 0.8$ V.

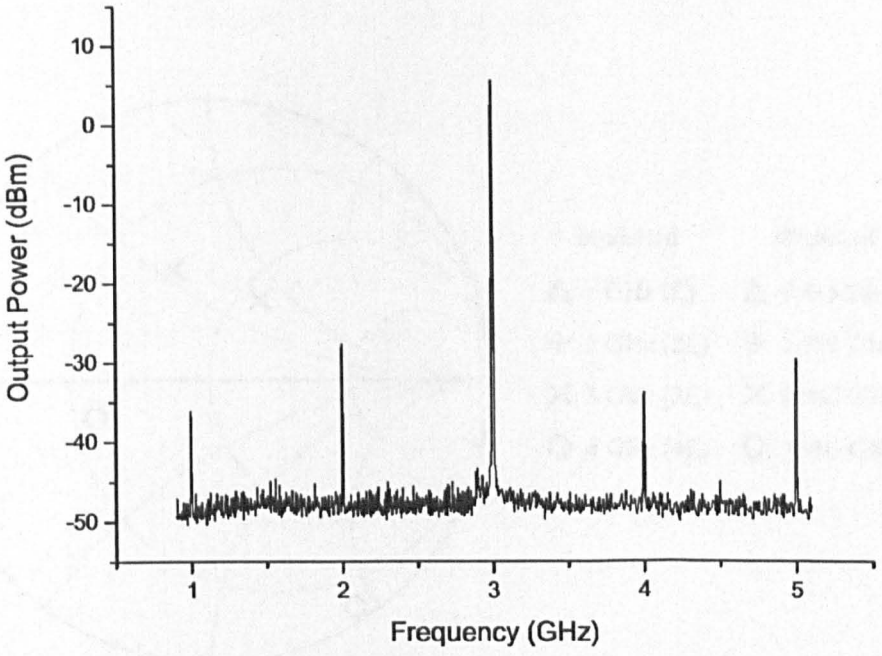


Figure 4.14: Tripler Design 2: Measured output power spectrum at optimum bias of $V_{GG} = -1.4$ V and $V_{DD} = 0.8$ V and input power level of -0.3 dBm. Harmonic rejection levels are better than 34 dBc. (This plot is taken directly from the HP8593E spectrum analyser, and does not account for the losses measured in the RF coaxial cables and a known error in measurement displayed by the HP8593E spectrum analyser. The total losses amount to 1.2 dBm.)

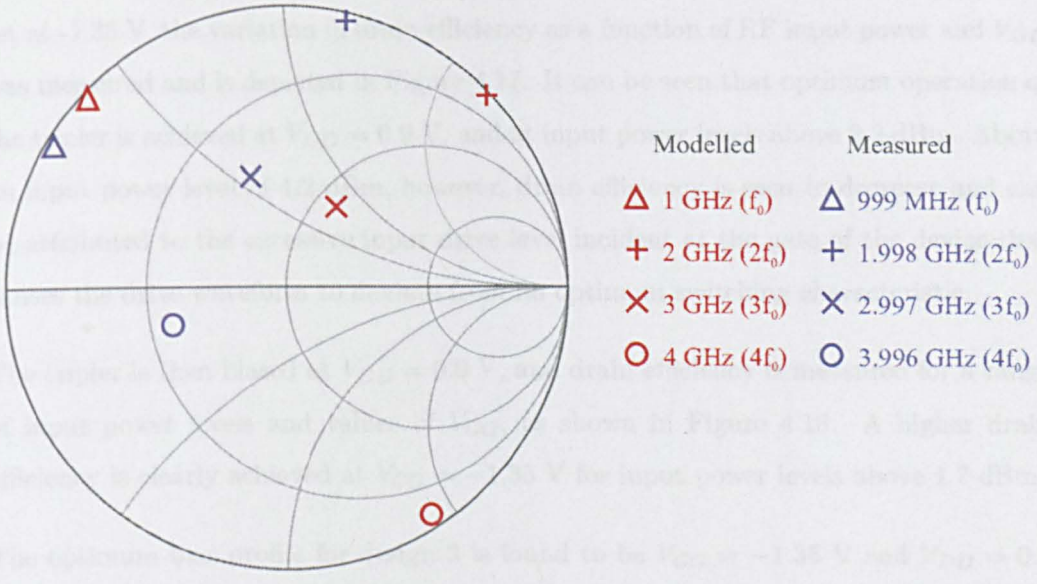


Figure 4.15: Tripler Design 2: Modelled and measured impedances presented to the device by the output matching network at the required harmonic, $3f_0$, and unwanted harmonics, f_0, $2f_0$ and $4f_0$.

4.4.3 Tripler Design 3

The fabricated hybrid MIC implementation of design 3 is shown in Figure 4.16, and is similar in construction to the two designs discussed previously. Characterisation of the tripler involved measuring the drain efficiency as a function of RF input power, drain bias, V_{DD} and gate bias, V_{GG}, along with output power levels at the wanted and unwanted harmonics.

Initial indications showed that a gate bias voltage of -1.35 V provided optimum tripler performance, and agrees relatively well with the predicted value of -1.48 V. With V_{GG} set at -1.35 V, the variation in drain efficiency as a function of RF input power and V_{DD} was measured and is depicted in Figure 4.17. It can be seen that optimum operation of the tripler is achieved at $V_{DD} = 0.9$ V, and at input power levels above 2.2 dBm. Above an input power level of 4.2 dBm, however, drain efficiency is seen to decrease and can be attributed to the excessive input drive level incident at the gate of the device that causes the drive waveform to deviate from its optimum switching characteristic.

The tripler is then biased at $V_{DD} = 0.9$ V, and drain efficiency is measured for a range of input power levels and values of V_{GG}, as shown in Figure 4.18. A higher drain efficiency is clearly achieved at $V_{GG} = -1.35$ V for input power levels above 1.7 dBm.

The optimum bias profile for design 3 is found to be $V_{GG} = -1.35$ V and $V_{DD} = 0.9$ V, and the performance of the tripler in terms of drain efficiency, PAE and conversion gain at this operating point is shown in Figure 4.19(a). A maximum drain efficiency of 59.7% is measured at an input power level of 3.7 dBm, with a simultaneous PAE of 48.4 % and a conversion gain of 7.22 dB. Overall efficiency at this optimum operating point is measured to be 53.6 % , with a DC drain current of 23 mA. A maximum conversion gain of 8.6 dB is achieved at an input power level of -0.8 dBm with 38.5 % drain efficiency.

The output power measured at the required harmonic, $3f_0$, and unwanted harmonics, f_0, $2f_0$ and $4f_0$ as a function of input power at the optimum bias profile, is shown in Figure 4.19(b). The output power at $3f_0$ is relatively constant with input power, indicating switching operation of the class E circuit. Harmonic rejection levels are shown to be better than 19.5 dBc. Figure 4.20 shows the output spectrum of the

tripler at the optimum input power level of 3.7 dBm. Harmonic rejection at f_0 is 19.5 dBc, and is the least suppressed of the unwanted harmonics, as expected from the simulations. Improved harmonic suppression of the fundamental could potentially be achieved by choosing a larger impedance ratio of, $\frac{Z_1}{Z_2}$, of the stepped impedance stub.

Tripler design 3 simultaneously achieves the highest reported drain efficiency and conversion gain to date for a microwave frequency tripler. A peak performance of 59.7 % drain efficiency and conversion gain of 7.22 dB is achieved at an output power of 10.92 dBm, with a maximum conversion gain of 8.6 dB obtained with 38 % drain efficiency at an output power of 7.8 dBm. Peak performance is achieved at a low drain supply voltage of 0.9 V and a DC consumption of 23 mA at a low input power level of 3.7 dBm, proving it to be a particularly advantageous solution in power-critical systems such as wireless communications, as discussed in Chapter 1. A comparison of measured and modelled S-parameters of the output matching circuit is shown in Figure 4.21, where a relatively good correlation is achieved. The circuit is, as expected, less sensitive to circuit variations, with errors caused by manufacturing tolerances or inaccurate EM simulations for a part of the matching network pertaining to one harmonic, having a low repercussion on the terminations of the remaining harmonics.

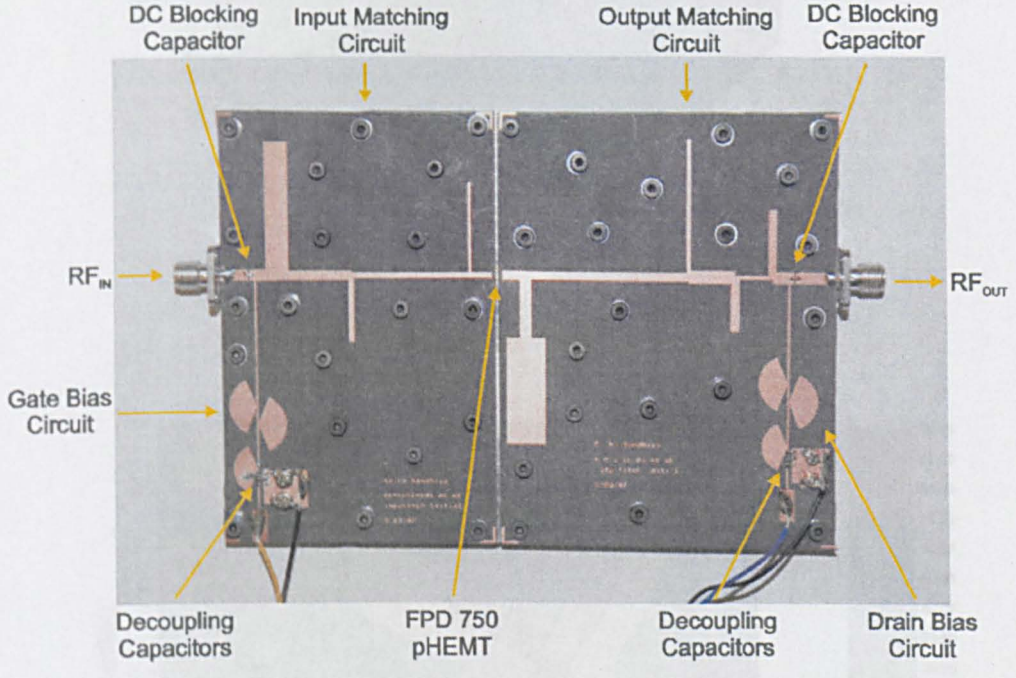
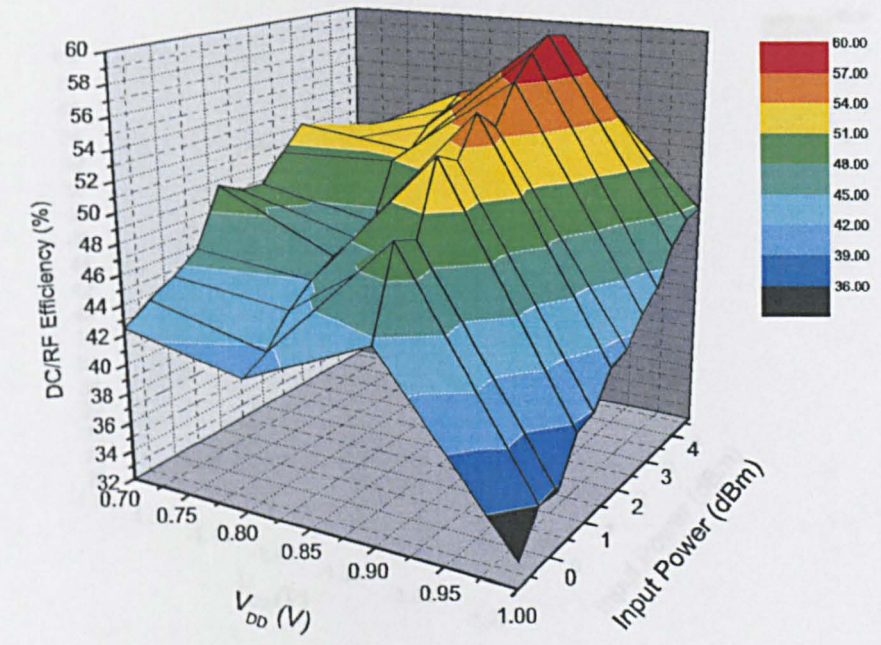
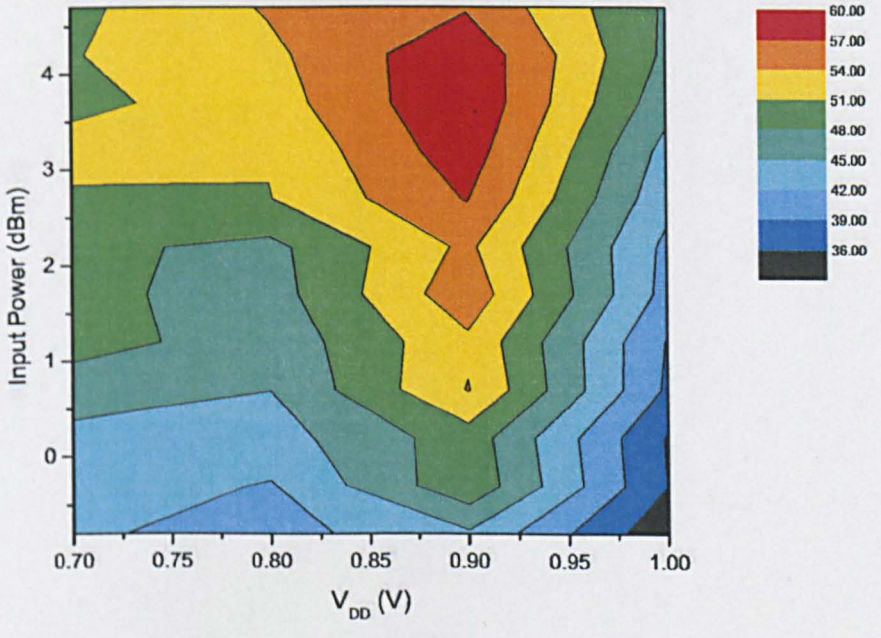


Figure 4.16: Photograph of the fabricated hybrid MIC implementation of Frequency Tripler Design 3. The circuit measures 9.1 cm by 13.2 cm.

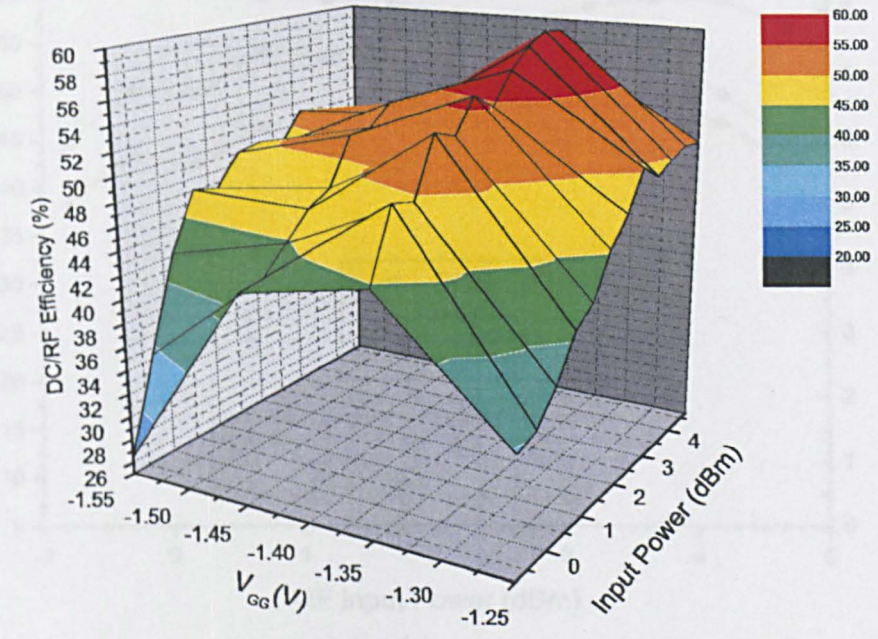


(a)

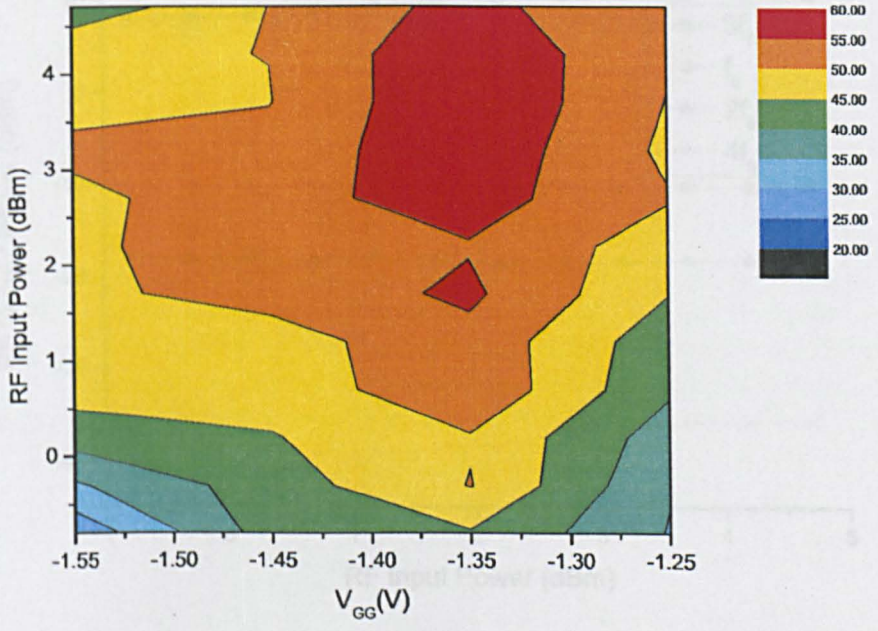


(b)

Figure 4.17: Tripler Design 3: Measured (a) Drain efficiency vs. drain bias (V_{DD}) and input power level for $V_{GG} = -1.35$ V, and (b) contour plot of the same. Maximum efficiency is achieved at $V_{DD} = 0.9$ V at an input power level of 3.7 dBm.

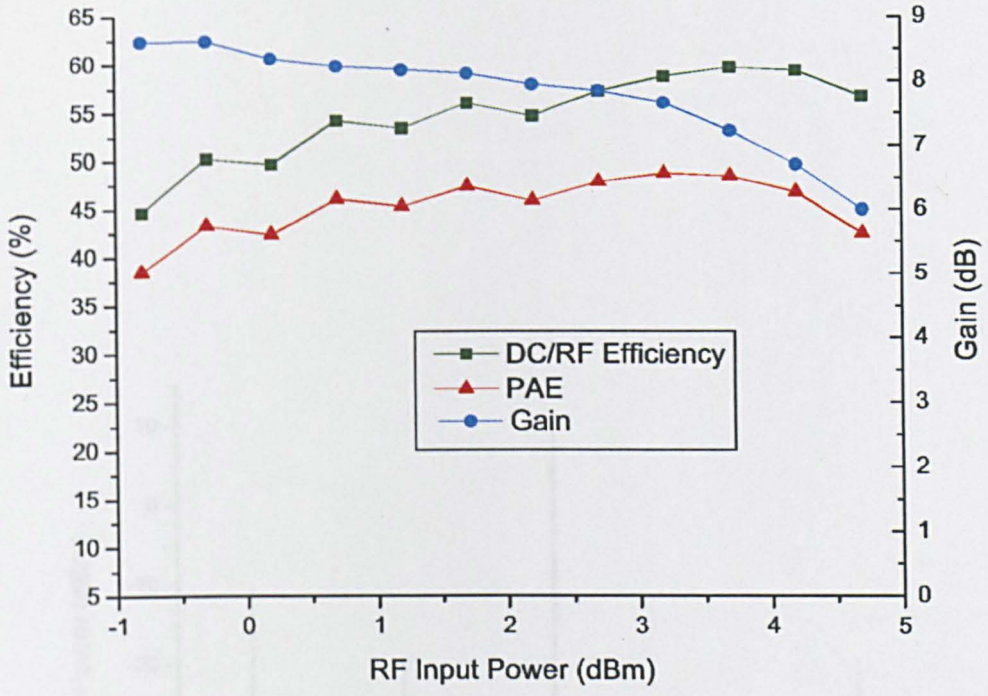


(a)

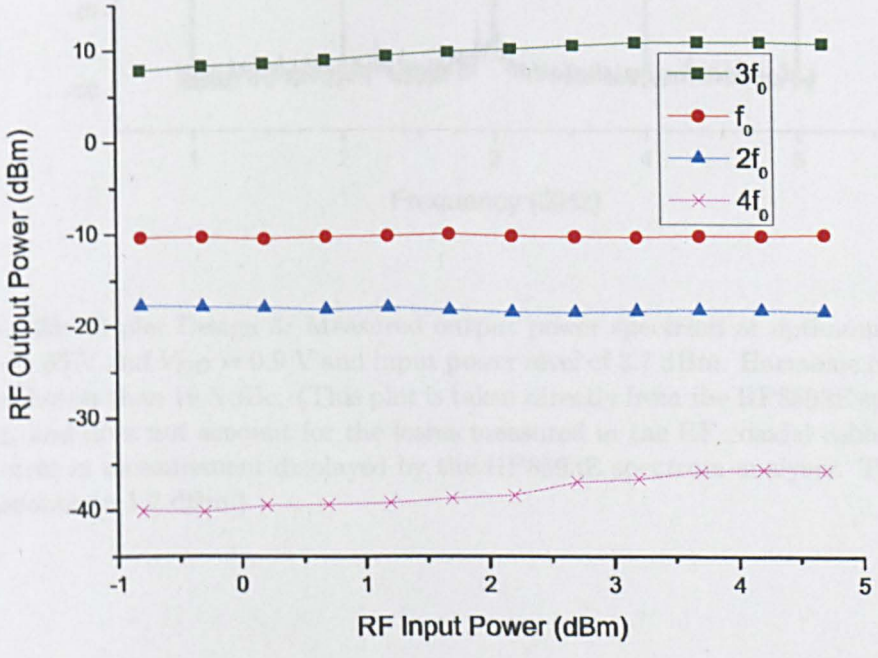


(b)

Figure 4.18: Tripler Design 3: Measured (a) Drain efficiency vs. gate bias (V_{GG}) and input power level for $V_{DD} = 0.9$ V, and (b) contour plot of the same. Maximum efficiency is achieved at $V_{GG} = -1.35$ V at an input power level of 3.7 dBm.



(a)



(b)

Figure 4.19: Tripler Design 3: Measured (a) Drain efficiency, Power-Added-Efficiency and Gain vs. Input power, and (b) Output power at $3f_0$ and unwanted harmonic rejection levels at optimum bias levels of $V_{GG} = -1.35$ V and $V_{DD} = 0.9$ V.

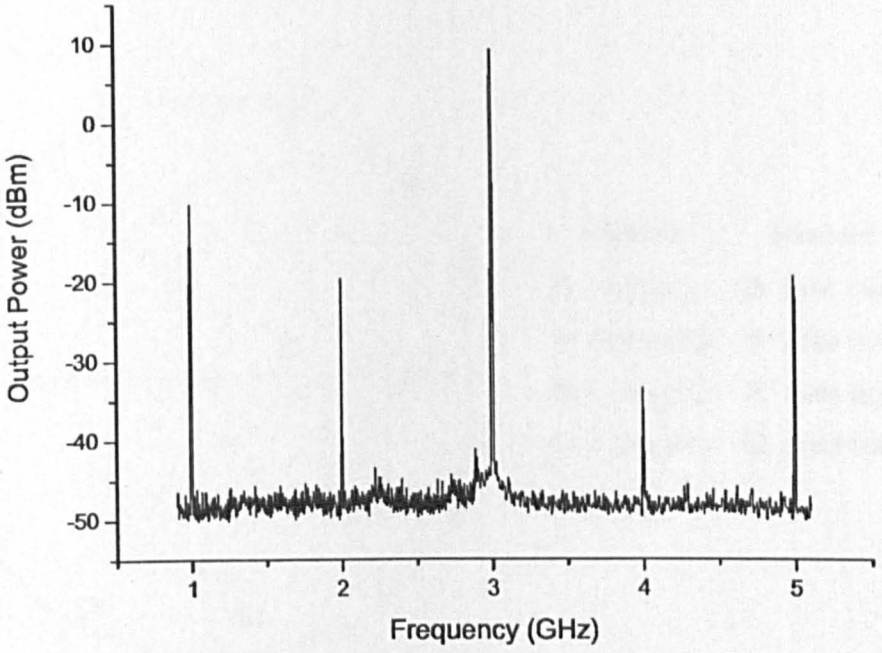


Figure 4.20: Tripler Design 3: Measured output power spectrum at optimum bias of $V_{GG} = -1.35$ V and $V_{DD} = 0.9$ V and input power level of 3.7 dBm. Harmonic rejection levels are better than 19.5 dBc. (This plot is taken directly from the HP8593E spectrum analyser, and does not account for the losses measured in the RF coaxial cables and a known error in measurement displayed by the HP8593E spectrum analyser. The total losses amount to 1.2 dBm.)

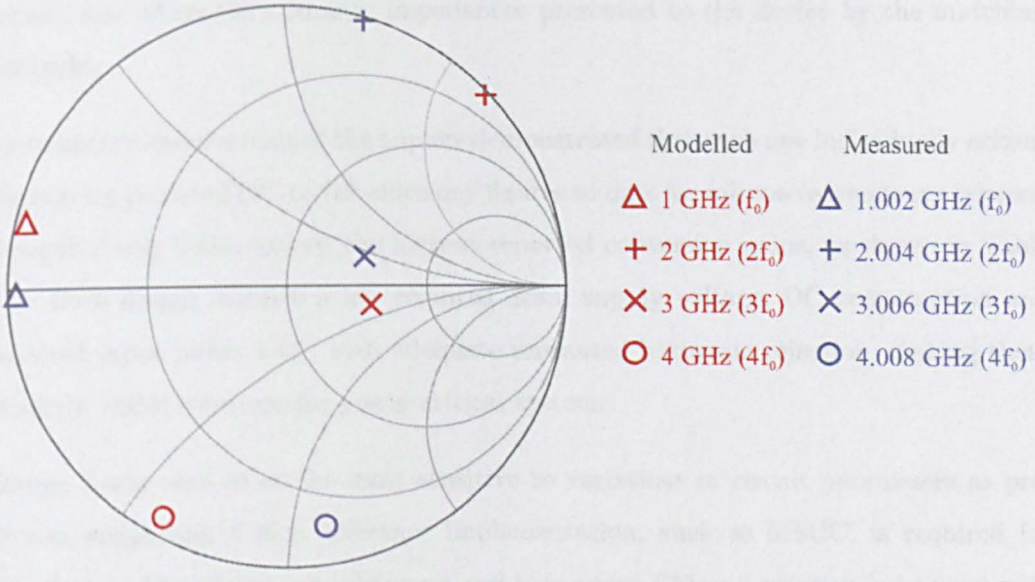


Figure 4.21: Tripler Design 3: Modelled and measured impedances presented to the device by the output matching network at the required harmonic, $3f_0$ and unwanted harmonics, f_0, $2f_0$ and $4f_0$.

4.5 Conclusions

The three designed 3 GHz proof-of-concept triplers were successfully fabricated as hybrid MICs on RT/Duroid 5880. Aluminium mounting blocks were designed specifically to minimise and allow accurate modelling of the parasitic effects of the interconnects between the discrete FPD750 pHEMT device and the input and output matching circuits. The parasitic inductance associated with the interconnect between source and ground was found to be a critical factor in performance degradation of the triplers, as it provides an additional feedback mechanism between the input and output of the tripler, and alters the optimum impedances presented to the device by the matching networks.

Systematic measurements of the triplers demonstrated that each one individually achieve the highest reported DC-to-RF efficiency figures to date for microwve frequency triplers. Designs 2 and 3 also exceed the highest reported conversion gains, as shown in Table 4.1. Each design features a low required drain supply voltage, DC consumption and required input power level, with adequate unwanted harmonic rejection, making them strongly viable solutions for power-critical systems.

Design 1 was seen to be the most sensitive to variations in circuit parameters as predicted, suggesting a high tolerance implementation, such as MMIC, is required for this design. Manufacturing tolerances and inaccurate EM optimisation led to a significant mismatch in measured and modelled S-parameters of the output matching circuit, causing a deviation from expected tripler performance. A better match in measured and modelled output network S-parameters was achieved with designs 2 and 3, with a higher degree of independence between the significant harmonics, resulting in a less pronounced deviation from the expected performance. Variations in device performance were also noted, with a lower than expected pinch-off voltage and higher on-resistance also causing a departure from expected performance.

Triplers	Device	f_0 /GHz	P_{input} /dBm	P_{output} /dBm	Conversion Gain /dB	$\eta_{DC/RF}$	Year
Le [42]	GaAs FET	2.5	+4	+1.6	-2.4	13 %	1992
Henkus [55]	MESFET	2.8-3.5	+10	-0.4	-10.4	1.5 %	1993
Zhao [38]	MESFET	5	+10.2	+3.7	-6.5	2 %	1995
Zhang [31]	pHEMT	11.5	0	-6	-6		1996
Von Stein [56]	GaAs MESFET	2	+6	+2.4	-3.64		1996
Fudem [29]	GaAs FET	14	+23.6	+12.5	-11.1		1998
Thibaud [57]	pHEMT	11.5-13		+10			1999
O'Ciardha [30]	pHEMT	18.7	+17.5	+3.5	-14.0		2000
Mima [40]	pHEMT	2.95	+0.1	+3	+2.9		2000
Beaulieu [44]	HBT	9.5	+15	+10	-5	5 %	2000
Madriz [58]	pHEMT	2.125	-1	+3.1	+4.1	10 %	2000
Boudiaf [59]	pHEMT	12.6	+6.5	+3.1	-3.4	11 %	2000
Penn [43]	MESFET	2.3	+8	+7.3	-0.7	4 %	2001
Allen [27]	pHEMT	24.3	+17	0	-17		2003
Bunz [60]	HEMT	1.78-2.25	+3.0	+3.5	+0.5		2004
Johnson [41]	pHEMT	2.94	+4	+7.67	+3.67		2005
Chiu [61]	pHEMT	12.0	+14	+5	-9	16 %	2006
This work							
Design 1	pHEMT	1.0	+3.2	+5.0	**+1.8**	**29 %**	2007
Design 2	pHEMT	1.0	-0.3	+6.5	**+6.8**	**47 %**	2007
Design 3	pHEMT	1.0	+3.7	+10.9	**+7.22**	**59.7 %**	2007

Table 4.1: A comparison of previously published results for frequency triplers and the results obtained in this work.

Chapter 5

Conclusions and Future Work

5.1 Summary and Conclusions

The main objective of this work was to investigate and develop circuit techniques that lead to the successful implementation of high efficiency class E frequency multipliers. With extensive research carried out into design techniques for high efficiency operation of power amplifiers, frequency multipliers have seen relatively little investigation in terms of optimum design procedures. Investigation of higher order multipliers (>x2) in particular have been relatively limited, with doublers being favoured in terms of simpler design and lower circuit complexity. Prevalent design techniques involve load-pull optimisation, which provide an improvement in conversion gain on the classical approach introduced by Maas [2], by providing alternative harmonic terminations to maximise the power at the required harmonic. However, as discussed in Chapter 1, this procedure is dependent on trial and error iterations with no set systematic procedure to obtain the optimum design, making it a time-consuming and costly process. In addition, it has been shown to be quite sensitive to the device used, the adopted procedure and sequence of harmonic impedance optimisation.

With a shift in focus from achieving high conversion gain and output power to high drain efficiency in the design of frequency multipliers, Class E designs were seen to offer a viable alternative with explicit closed-form design equations for high achievable efficiency, allowing a useful initial design and a definite design plan offered for the harmonic terminations. The optimum duty cycle, D, of an N^{th} harmonic multiplier is given as,

$$D = \frac{1}{2N}, \tag{5.1}$$

As discussed in Chapter 2, for higher multiplication factors, the duty cycle required becomes progressively smaller, implying a larger input drive is required for sufficient switching of the device. This not only compromises the conversion gain but also increases the chances of undesirable forward conduction, therefore limiting most commercially available devices to not more than doubler operation. Achieving the correct fractional duty cycle is also complicated by the distortion of the drive signal caused by the the nonlinear input capacitance, C_{gs}, of the device. Locating the optimum bias and input drive levels can provide a good operating condition, however, the shape of the drive waveform is not controlled and optimum conditions for efficient switching of the device may not be achieved. Additionally, a rectangular drive waveform is required to switch the device at a small duty cycle, resulting in increased complexity of the drive circuitry as a rectangular drive is not easily achieved.

The limitations imposed by the drive requirements of the conventional class E tripler can be alleviated with a 50 % duty cycle drive that is more easily implemented. However, it was shown to lead to sub-optimal tripler operation, with a required load angle approaching 90° for 100 % drain efficiency.

An innovative class E circuit configuration has been proposed in this work that provides a solution to this problem by allowing a 50 % duty cycle drive with a realisable load angle for a theoretical 100 % efficiency operation of a frequency tripler. The load network is modified to include a fundamental harmonic trap to provide a short-circuit termination at f_0. A result of this modification is to provide a load impedance that is not purely reactive. A simple yet accurate quantitative analysis of class E networks is first developed in Chapter 2 to aid in the effective evaluation of circuit performance. The novel first-order analysis was proven to be a more tangible treatment of circuit behaviour, providing a more intuitive description of class E operation and the harmonic content of the output waveforms. The analysis was shown to be adaptable to both class E amplifiers and multipliers, of any circuit configuration and operating at any duty cycle. Closed-form equations for the load network are obtained providing a useful initial design, with the intuitive insights developed in the analysis serving well for

the final design optimisation. The analysis was verified with the successful design and implementation of a prototype lumped class E amplifier at 100 MHz, achieving a $\eta_{DC/RF}$ of 78 % and PAE of 73 % with a gain of 12.6 dB.

The novel class E tripler configuration was then quantitatively analysed for a 50 % duty cycle, and a realisable load impedance angle of 73.3° was obtained, with no degradation of the output power from the conventional case with an optimal duty cycle of 16.7 %. Also shown was that, for the conventional case, the optimum harmonic impedance at $3f_0$ more rapidly approaches a short-circuit termination for larger values of shunt capacitance, C, compared to that of the novel tripler. A more easily achievable match at $3f_0$ at the output of the device is, therefore, offered by the proposed configuration. The output waveforms of the novel tripler were also shown to be more suited for high efficiency operation when considering the practical IV characteristics of a FET. The switch current is non-negative throughout the on-period, and its total amplitude is smaller than that of the conventional case, resulting in a lower power dissipation through the on-resistance of the FET.

Chapter 3 details the design considerations involved in translating the ideal circuit design to a practical implementation of the novel tripler. The effects of choice of active device to implement the switch on circuit performance are discussed, and performance trade-offs are evaluated in terms of device size. The Filtronic FPD750 pHEMT device was chosen for this work, and the associated TOM3 model was evaluated for its suitability in the design of the switching frequency tripler. The measurements of the DC characteristics of the device were performed and confirmed the validity of the model specifically in the regions of expected operation. Microstrip implementation was chosen for circuit realisation due to the specific multi-harmonic control that can be accurately modelled. The effect of limiting the number of controlled harmonic terminations in the design of the tripler was evaluated in order to reduce circuit complexity whilst maintaining good circuit performance. It was shown that control up to the fourth harmonic is necessary to avoid a large degradation in efficiency; however, beyond this the improvement in efficiency gained is minimal and does not justify the associated increase in circuit complexity. Considerations in the design of the input and output matching circuits, the bias level and bias network are then discussed. In this work, it is proposed to exploit the distortion caused by the nonlinear input capacitance, C_{gs} of the device,

rather than circumvent it by shorting all unwanted harmonics. The nonlinearity is used to shape the drive signal to a square waveform by providing a short-circuit termination to $2f_0$ and $4f_0$. This, in conjunction with a conjugate match at f_0, provides efficient and optimum switching of the device.

Three microstrip implementations of the novel tripler are then presented, each employing innovative input and output network microstrip solutions to realise the required harmonic terminations. A comprehensive design procedure is provided for each circuit, and simulated performance of all three designs confirm their strong potential to achieve simultaneous high drain efficiency and conversion gain, with sufficient harmonic rejection at the load. It was observed that, with the designs optimised for maximum drain efficiency, the output power and conversion gain obtained is dependent on the degree of inter-harmonic independence achieved by the particular design. A larger degree of independence between the harmonics leads to more possible solutions where high efficiency and high output power can be achieved. However, this also leads to increased circuit size and complexity, with individual circuit structures being dedicated to the manipulation of one harmonic. A smaller circuit size is demonstrated with a more compact structure offering multi-harmonic optimal terminations; however, as made evident from the sensitivity analysis, this also leads to an increase in sensitivity to variations in circuit parameters, as a small pertubation in line dimension can cause all the harmonic terminations to deviate from their optimum values.

Details of the practical demonstration of the triplers along with measured results are given in Chapter 4. The three circuits achieve the highest reported figures for both drain efficiency and conversion gain for microwave frequency triplers. They present low drain supply voltage and input power level requirements, and feature low DC power consumption with sufficient unwanted harmonic rejection. Design 1 presents the most compact but sensitive circuit, with a minimum number of microstrip line structures providing the optimal output harmonic terminations to the device. The circuit achieves an exceptional maximum drain efficiency of 29 %, with a conversion gain of 1.8 dBm and overall efficiency of 24 %. Deviation from the expected results is attributed to the sensitivity of the circuit to variations in circuit parameters, such as device performance, fabrication tolerance and limitations in simulation. The circuit would, therefore, benefit a high tolerance environment such as MMIC implementation,

and better device characterisation in terms of C_{gs}. Design 2 achieves an unprecedented drain efficiency of 47 % and simultaneously achieves the highest reported conversion gain of 6.8 dB. A maximum conversion gain of 8.6 dB is also achieved with 43 % drain efficiency, which are the highest figures reported for microwave frequency triplers. Design 3 achieves the highest drain efficiency of the three proposed designs, achieving 59.7 % of drain efficiency and a conversion gain of 7.22 dB. A peak conversion gain of 8.6 dB is also obtained with a drain efficiency of 38 %. These successful designs clearly demonstrate their strong suitability and applicability to power-critical systems.

5.2 Recommendations for Future Work

5.2.1 Higher Frequency Tripler

A natural progression of this work will be to extend the frequency of operation of the triplers to a higher band of operation. Although applications involving low frequency multipliers can benefit from these designs, for e.g. extending the phase control range of a phase shifter for a WLAN phased array antenna (see Chapter 1), extension into the X or Ka-band region would benefit space-borne applications.

Investigation into the impact of feedback capacitance, C_{gd} can be carried out in order to assess its effect on the optimum impedances presented to the input and output of the device. The degradation in performance by operating a device beyond the calculated maximum frequency for ideal class E operation (given by (2.40)) can be quantified in order to assess design trade-offs in terms of choice of device and tripler performance.

Preliminary simulations of a 12 GHz tripler that adopts the topology of design 3 were carried out, and the results are shown in Figure 5.1. It must be noted here that the I_{ds} depicted in this figure is, in fact, I_0+I_i and not the instrinsic drain-source current, and therefore deviates from the expected waveform. Since the operating frequency of this circuit is quite close to the maximum frequency for ideal class E operation for the FPD750 device, the total shunt capacitance is realised by C_{ds} of the device, therefore exaggerating this effect. Promising results of 69 % efficiency and 4 dB conversion gain at 1.16 V drain supply voltage with unwanted harmonic rejection levels of 16 dBc,

demonstrate the strong potential for the successful implementation of the novel tripler at high frequencies.

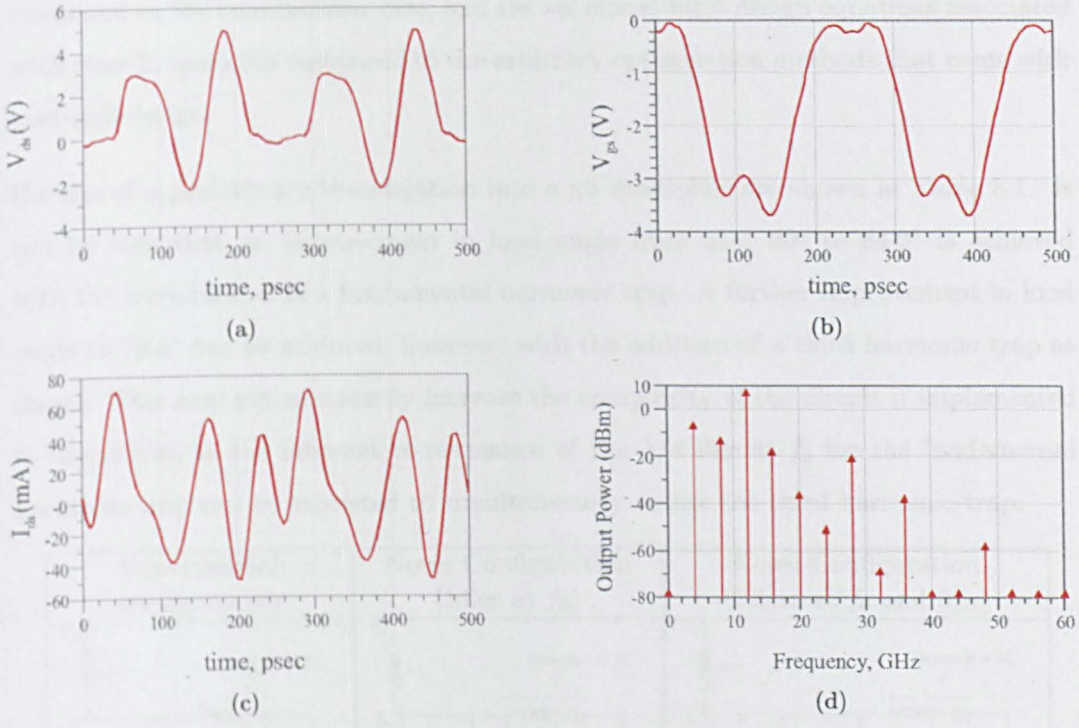


Figure 5.1: Time domain simulations of (a) drain voltage waveform (b) input drive waveform (c) drain current waveform and (d) output power spectrum of a 12 GHz tripler adopting design 3, biased at V_{GG}=-1.7V and V_{DD}=1.16V.

5.2.2 Broadband Design

The experimental class E triplers presented in this work were designed for narrowband operation. Modifications of the input and output matching networks to achieve a more broadband operation would be an interesting line of investigation. The matching networks will have to provide the optimum impedance termination not only in the band of interest, but at the harmonics of the frequency band.

5.2.3 Higher Order Multiplication Factors

The problems associated with the design and implementation of conventional class E multipliers, as discussed above and in Chapter 2, become more pronounced the higher

the order of multiplication factor. Class E higher order multipliers that are implemented with a 50 % duty cycle are an attractive prospect in terms of ease of implementation compared to the conventional case, and the set closed-form design equations associated with class E operation compared to the arbitrary optimisation methods that come with load-pull design.

Results of a preliminary investigation into a x5 multiplier are shown in Table 5.1. It can be seen that an improvement in load angle from near 90° to 84.9° is achieved with the introduction of a fundamental harmonic trap. A further improvement in load angle to 79.8° can be achieved, however, with the addition of a third harmonic trap as shown. This may not necessarily increase the complexity of the circuit if implemented in microstrip, as the inherent re-resonance of the $\lambda/4$ line at f_0 for the fundamental harmonic trap can be exploited to simultaneously realise the third harmonic trap.

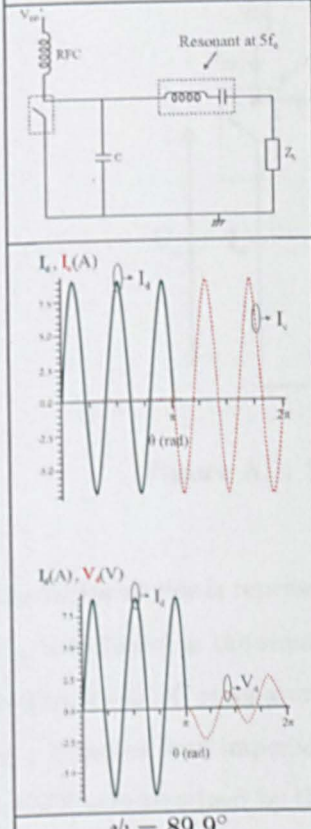
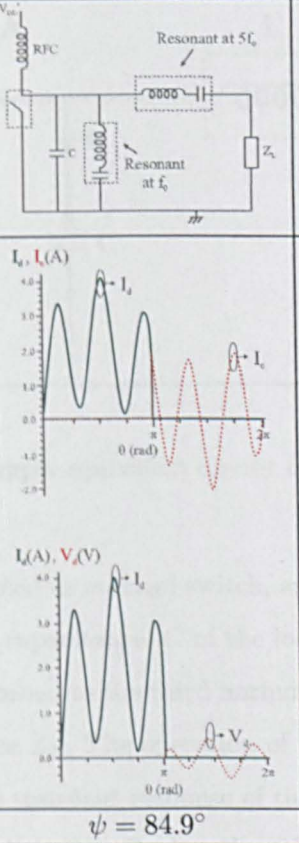
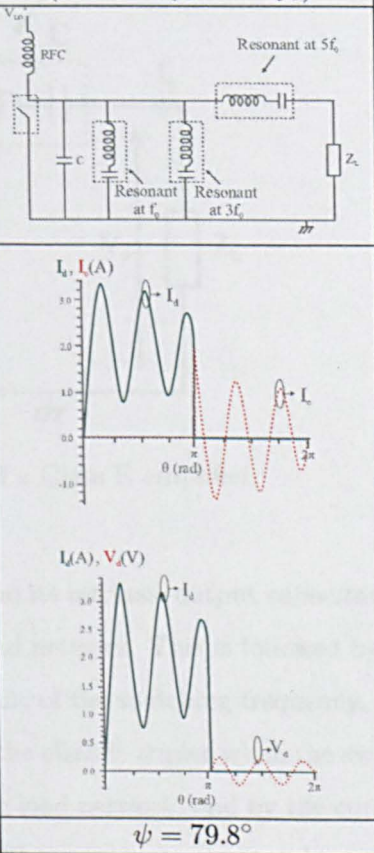
Conventional configuration	Novel Configuration (Idler at f_0)	Novel Configuration (Idlers at f_0 and $3f_0$)
		
$\psi = 89.9°$	$\psi = 84.9°$	$\psi = 79.8°$

Table 5.1: x5 Multiplier: Switch waveforms and associated load angles for the conventional class E configuration and two novel configurations.

Appendix A

Analysis of Conventional Class E Tripler

A simplified schematic of a conventional Class E tripler is shown in Figure A.1.

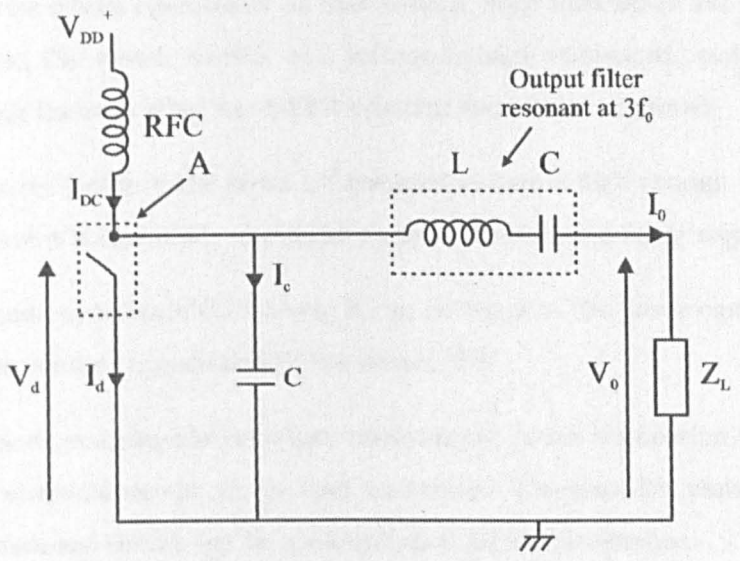


Figure A.1: Simple equivalent circuit of a Class E amplifier.

The active device is represented as an ideal switch, and its intrinsic output capacitance, C_{ds} is included in the shunt capacitance, C of the load network. This is followed by an output series LC resonator tuned to the third harmonic of the switching frequency, and by a complex load impedance Z_L. The operation of the class E tripler when the switch is OFF is determined by the transient response of the load network, and by the current flowing in the switch when it is ON. During the OFF interval, the current I_{DC} splits between the capacitor current I_c, and load current I_0. The capacitor C charges up and a voltage is produced across the capacitor and switch. The load network is designed

to ensure that at the end of the OFF period, the voltage across the switch returns to zero with zero gradient. This ensures that at the ON transition, when the current I_{DC} is split between I_0 and drain current I_d, the switch voltage and current do not overlap and no charge is left stored in C to dissipate into the switch.

A.0.4 Assumptions

The assumptions are as follows:

1. An infinite impedance RF choke is provided at the bias feed. This implies only DC flows through the bias line.

2. The active device operates as an ideal switch, with sufficiently low on-resistance such that the switch current and voltage remain unchanged, and fast enough switching times to allow the OFF-transition time to be neglected.

3. The quality factor of the series LC resonant circuit is high enough such that the load current is essentially sinusoidal at the harmonic frequency required.

4. The shunt capacitance C, is ideal. It can be equal to the linear equivalent of the nonlinear output capacitance of the device [79].

5. The circuit components are ideal, implying no power dissipation occurs in the circuit elements except at the load resistance. The parasitic resistances of the series resonant circuit can be absorbed into the load resistance.

A.0.5 Derivation of Switch Current and Voltage Waveforms

The currents in the various branches of the circuit, namely drain current I_d, capacitor current I_c, and load current I_0 are described according to their harmonic content. From Figure A.1, and the assumptions above, the following statements can be derived about the harmonic composition of the branch currents:

1. I_d contains all harmonics.

2. I_c does not contain any DC component.

3. I_0 contains only third harmonic components.

Nodal analysis is then performed at node A, and the following expression relating the branch currents is obtained,

$$I_{DC} = I_d + I_c + I_0. \tag{A.1}$$

If the fourth and higher harmonic components are represented by $G_4(\theta)$ (as a function of ωt), then I_d can be expressed as,

$$\begin{aligned} I_d = I_{DC} &+ A_1 \sin \omega t + A_2 \cos \omega t + A_3 \sin 2\omega t \\ &+ A_4 \cos 2\omega t + B_1 \sin 3\omega t + B_2 \cos 3\omega t \\ &+ G_4(\theta) \end{aligned} \tag{A.2}$$

and,

$$\begin{aligned} I_c = &- A_1 \sin 2\omega t - A_2 \cos 2\omega t - A_3 \sin 2\omega t - A_4 \cos 2\omega t \\ &+ B_3 \sin 3\omega t + B_4 \cos 3\omega t - G_4(\theta) \end{aligned} \tag{A.3}$$

where, ω is the switching frequency in rads^{-1}, A_1 and A_2 are the coefficients of the fundamental component in the switch current, A_3 and A_4 are the coefficients of the second harmonic and B_1 and B_2 are the coefficients of the third harmonic. B_3 and B_4 are coefficients of the third harmonic in the current through the capacitor. Substituting (A.2) and (A.3) into (A.1), and evaluating at the third harmonic we obtain:

$$I_0 = -B_1 \sin 3\omega t - B_2 \cos 3\omega t - B_3 \sin 3\omega t - B_4 \cos 3\omega t \tag{A.4}$$

For a theoretical efficiency of 100%, the switch current and voltage are required to be displaced in time with no overlap for minimum dissipation of power at the device. This implies that the following conditions must be satisfied:

Switch ON: $I_c = 0$, for $0 \leq \theta \leq \frac{5\pi}{3}$

Switch OFF: $I_d = 0$, for $\frac{5\pi}{3} \leq \theta \leq 2\pi$

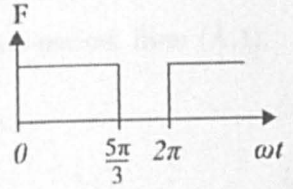
where $\theta = \omega t$. Therefore, from (A.2) and (A.3), during switch ON,

$$G_4(\theta) = -A_1 \sin \omega t - A_2 \cos \omega t - A_3 \sin 2\omega t - A_4 \cos 2\omega t + B_3 \sin 3\omega t + B_4 \cos 3\omega t$$

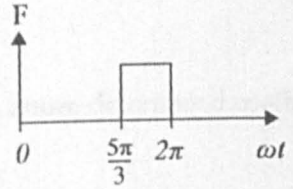
and during switch OFF:

$$\begin{aligned} G_4(\theta) = -I_{DC} &- A_1 \sin \omega t - A_2 \cos \omega t - A_3 \sin 2\omega t \\ &- A_4 \cos 2\omega t - B_1 \sin 3\omega t - B_2 \cos 3\omega t. \end{aligned}$$

The above expressions for $G_4(\theta)$ are relevant when the switch is on and off respectively, and can be combined by multiplying by the corresponding rectangular wave functions shown in Figure A.2 to produce a single expression for $G_4(\theta)$.



$$= \frac{1}{6} + \sum_{n=1}^{\infty} \left(\frac{\sin \frac{n\pi}{3}}{n\pi} \cos n\omega t - \frac{1 - \cos \frac{n\pi}{3}}{n\pi} \sin n\omega t \right)$$



$$= \frac{5}{6} + \sum_{n=1}^{\infty} \left(-\frac{\sin \frac{n\pi}{3}}{n\pi} \cos n\omega t - \frac{\cos \frac{n\pi}{3} - 1}{n\pi} \sin n\omega t \right)$$

Figure A.2: Harmonic composition of rectangular waveforms in order to determine $G_4(\theta)$.

This gives,

$$
\begin{aligned}
G_4(\theta) = & \\
& (-A_1 \sin\omega t - A_2 \cos\omega t - A_3 \sin 2\omega t - A_4 \cos 2\omega t + B_3 \sin 3\omega t + B_4 \cos 3\omega t) \\
& \cdot \left[\frac{5}{6} + \sum_{n=1}^{\infty} \left(-\frac{\sin\frac{n\pi}{3}}{n\pi} \cos n\omega t - \frac{\cos\frac{n\pi}{3} - 1}{n\pi} \sin n\omega t \right) \right] + \\
& (-I_{DC} - A_1 \sin\omega t - A_2 \cos\omega t - A_3 \sin 2\omega t - A_4 \cos 2\omega t - B_1 \sin 3\omega t - B_2 \cos 3\omega t) \\
& \cdot \left[\frac{1}{6} + \sum_{n=1}^{\infty} \left(\frac{\sin\frac{n\pi}{3}}{n\pi} \cos n\omega t - \frac{1 - \cos\frac{n\pi}{3}}{n\pi} \sin n\omega t \right) \right]
\end{aligned}
$$

The above expression for $G_4(\theta)$ cannot contain any DC, fundamental, second harmonic or third harmonic components, as $G_4(\theta)$ represents the fourth and higher harmonic content. Therefore the cosine and sine terms of these components in $G_4(\theta)$ are equated to zero to determine the coefficients. An eighth relationship is obtained by considering the continuity of $G_4(\theta)$ at $t = 0$ and equating the two expressions for $\lim_{t\to 0} G_4(\theta)$. The coefficients are then solved in terms of I_{DC}, and are given as,

$$
\begin{aligned}
A_1 &= 0.05646 I_{DC}, \quad A_2 = 0.04 I_{DC}, \quad A_3 = 0.04259 I_{DC}, \quad A_4 = 0.12243 I_{DC} \\
B_1 &= 1.5212 I_{DC}, \quad B_2 = -0.8333 I_{DC}, \quad B_3 = 0.04959 I_{DC}, \quad B_4 = -0.16667 I_{DC}
\end{aligned}
$$

Expressions for the switch current and switch voltage can now be determined. During the on-period, from (A.1),

$$
I_d = I_{DC} - I_0 \quad \text{for} \quad 0 < \theta < \frac{5\pi}{3} \tag{A.5}
$$

The above determined coefficients are substituted into (A.5) to give the switch current as:

$$
I_d(\theta) = I_{DC}(1 + 1.57079 \sin 3\theta - \cos 3\theta) \tag{A.6}
$$

During the off-period, from (2.25):

$$I_c = I_{DC} - I_0 \quad \text{for} \quad \frac{5\pi}{3} < \theta < 2\pi \tag{A.7}$$

The switch voltage, V_d, across the shunt capacitance, C is given by,

$$V_d(\theta) = \frac{1}{\omega C}\int_{\pi}^{\theta}(I_{DC} - I_0)d\theta$$

Expanding the integral and substituting in the coefficients gives,

$$V_d(\theta) = \frac{1}{\omega C}\left(I_{DC}\theta - 0.5236I_{DC}\cos 3\theta - \frac{I_{DC}}{3}\sin 3\theta - 5.7596I_{DC}\right) \tag{A.8}$$

The switch waveforms are depicted in Fig. 2.14.

The switch bias voltage V_{DD}, is the average of the switch voltage and is found from the DC component of the Fourier series of the switch voltage from (A.8), and is given by,

$$V_{DD} = \frac{I_{DC}}{9\pi\omega C} \tag{A.9}$$

A.0.6 Derivation of Load Impedance, Z_L

At the third harmonic, the voltage across the switch, V_d, is equal to the voltage across the load impedance, V_0, therefore,

$$\begin{aligned} V_d|_{3f_0} = V_0 &= \frac{1}{C}\int(B_3\sin 3\theta + B_4\cos 3\theta)d\theta \\ &= -\frac{1}{3\omega C}(0.16667I_{DC}\sin 3\theta + 0.04959I_{DC}\cos 3\theta) \end{aligned} \tag{A.10}$$

The third harmonic current, I_0 is given by,

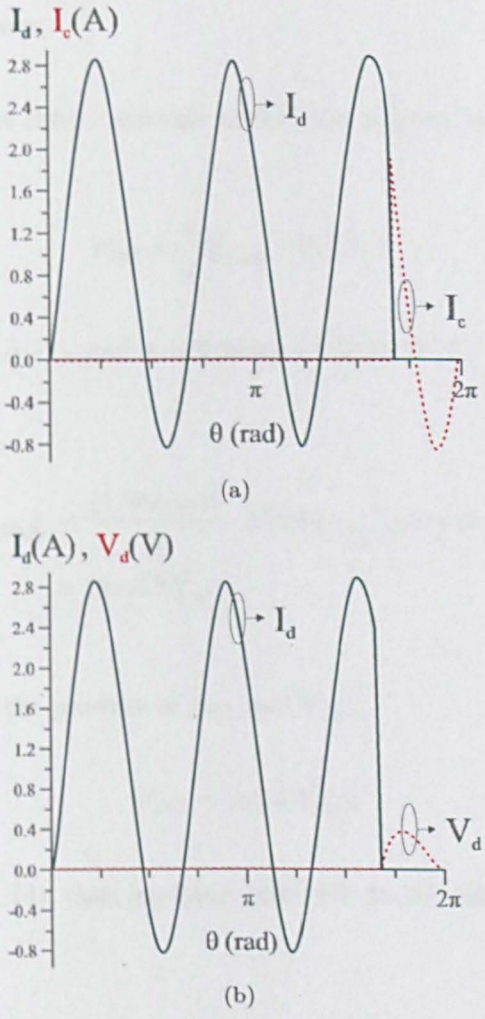


Figure A.3: (a) Switch current I_d (solid), and capacitor current I_c (dashed) and (b) switch current I_d (solid), and switch voltage V_d (dashed) of the conventional class E tripler. (Normalised to $I_{DC} = 1$, $\omega C = 1$).

$$I_0 = \cos 3\theta - 1.5708 \sin 3\theta \tag{A.11}$$

Therefore, the optimum third harmonic impedance required for 100% efficiency can be found by the ratio of (A.10) and (A.11), and is given by,

$$Z_L = \frac{1}{3\omega C} 0.0934 e^{j49.05^\circ} \tag{A.12}$$

A.0.7 Output Power

Output RF power at the third harmonic at the load is given by,

$$P_{out} = \frac{1}{2} I_{0,peak}^2 \cdot Re(Z_L). \tag{A.13}$$

$I_{0,peak}$ is derived from (A.11), and substituting (A.9) in (A.13) we get,

$$\begin{aligned} P_{out|3f_0} &= \frac{(1.86 I_{DC})^2}{2} \cdot 0.0934 \cdot \frac{1}{3\omega C} \cos 49.05^\circ \\ &= 9\pi\omega C V_{DD}^2 \end{aligned} \tag{A.14}$$

The total DC power is the product of I_{DC} and V_{DD},

$$P_{DC} = 9\pi\omega C V_{DD}^2,$$

and is equivalent to (A.14), thus implying 100% DC-to-RF efficiency.

Appendix B

Data Sheet - FPD750 pHEMT device

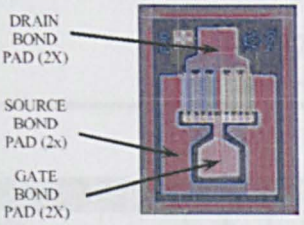
For the convenience of the reader, this appendix provides the technical datasheet for the Filtronic FPD750 pHEMT bare-die device.

Filtronic

FPD750

0.5W POWER PHEMT

- FEATURES
  - 27 dBm Linear Output Power at 12 GHz
  - 11.5 dB Power Gain at 12 GHz
  - 14.5 dB Maximum Stable Gain at 12 GHz
  - 38 dBm Output IP3
  - 50% Power-Added Efficiency



DIE SIZE (µm): 340 x 470
DIE THICKNESS: 75 µm
BONDING PADS (µm): >60 x 60

- DESCRIPTION AND APPLICATIONS

The FPD750 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25 µm by 750 µm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD750 also features Si_3N_4 passivation and is available in a P100 flanged ceramic package and in the low cost plastic SOT89 and SOT343 plastic packages.

Typical applications include commercial and other narrowband and broadband high-performance amplifiers, including SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT f = 12 GHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}	26.5	27.0		dBm
Maximum Stable Gain (S_{21}/S_{12})	SSG	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}	13.5	14.5		dB
Power Gain at P_{1dB}	G_{1dB}	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}	10.5	11.5		dB
Power-Added Efficiency	PAE	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}; P_{OUT} = P_{1dB}		45		%
Output Third-Order Intercept Point (from 15 to 5 dB below P_{1dB})	IP3	V_{DS} = 10V; I_{DS} = 50% I_{DSS} Matched for optimal power Tuned for best IP3		 38 40		dBm
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	185	230	280	mA
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		370		mA
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		200		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -5 V		10		µA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 0.75 mA		1.0		V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 0.75 mA	12.0	14.0		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 0.75 mA	14.5	16.0		V
Thermal Resistivity (see Notes)	θ_{JC}	V_{DS} > 6V		65		°C/W

Filtronic

FPD750

0.5W POWER PHEMT

• ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		8	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward or reverse current		7.5	mA
RF Input Power	P_{IN}	Under any acceptable bias state		175	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	°C
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	°C
Total Power Dissipation	P_{TOT}	See De-Rating Note below		2.3	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits**		2 or more Max. Limits		80	%

*$T_{Ambient}$ = 22°C unless otherwise noted **Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Thermal Resitivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.
- Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 22°C:
  $P_{TOT} = 2.3W - (0.015W/°C) \times T_{HS}$
  where T_{HS} = heatsink or ambient temperature above 22°C

Example: For a 85°C heatsink temperature: $P_{TOT} = 2.3W - (0.015 \times (85 - 22)) = 1.4W$

• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

• ASSEMBLY INSTRUCTIONS

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

• APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

Phone: +1 408 850-5790
Fax: +1 408 850-5766
http://www.filtronic.co.uk/semis
Revised: 11/17/04
Email: sales@filcsi.com

Appendix C

TOM3 Model for FPD750 pHEMT device

This appendix provides the TOM3 modelling report for the Filtronic FPD750 pHEMT bare-die device, provided by Filtronic plc. This includes model parameters for the intrinsic and extrinsic elements.

The values provided for the external parasitics were adjusted to account for the bond-wire length arising from the fixtures used for the hybrid MICs in this project. The values used are given below in Table C.

The external parasitics presented here are bias-independent. $IdExt$, $IgExt$ and $IsExt$ are parasitic inductances arising from the connecting bondwires. $CgGround1$, $CdGround1$ and $CsGround1$ are the parasitic capacitances to ground arising from the bondwires. Ig, Id and Is account for the parasitic inductances due to the metallisation of the gate, drain and source contact pads. $CgGround2$, $CdGround2$ and $CdsExt$ account for the parasitic capacitances formed between gate fingers and between ohmic contact pads. Rs and Rd represent the contact resistance of the ohmic contacts, with Rs also accounting for any bulk resistance leading up to the active channel. Rg represents the mettalisation resistance of the gate Schottky contact.

CdGround1	8.22 fF	Ig	0.155 nH
CdGround2	8.22 fF	IsExt	0.04 nH
CgGround1	51.24 fF	Is	0.03655 nH
CgGround2	21.96 fF	Rd	0.8608 Ω
IdExt	0.54 nH	Rs	0.7481 Ω
Id	0.055 nH	Rg	1.145 Ω
IgExt	0.45 nH	CdsExt	0.156 fF

Table C.1: External parasitic values of the FPD750 pHEMT device.

Modelling Report
FPD750 TOM3 and TOM2 Models

Version 1.0

Device Design and Modelling Group
Filtronic Compound Semiconductor Ltd.

Introduction

This report describes the models for the FPD750 discrete p-HEMT device. The models coupled with package models (given elsewhere). The model describes the device and the inbuilt inductance provided by the connecting bond wires. The metal fixture up until the connecting bond wires has been de-embedded.

Models

Two models are provided for different simulators these are as follows:

TOM3

This model provides a good fit to the measured data and has an advanced charge form. This allows the TOM3 model to accurately model the device over a wide range of operating conditions.

This model is recommended for use in most simulators

TOM2

This model is provided for the simulators that do not include TOM3 within there component set. This model employs a similar charge from to the TOM3 but only has a simple charge model. Consequently I recommend this model only be used when the TOM3 component is not present.

TOM3 Model

The TOM3 model was extracted for the FPD750 discrete part is shown below:

External Parasitics

The following network shows the external parasitics present in the device model:

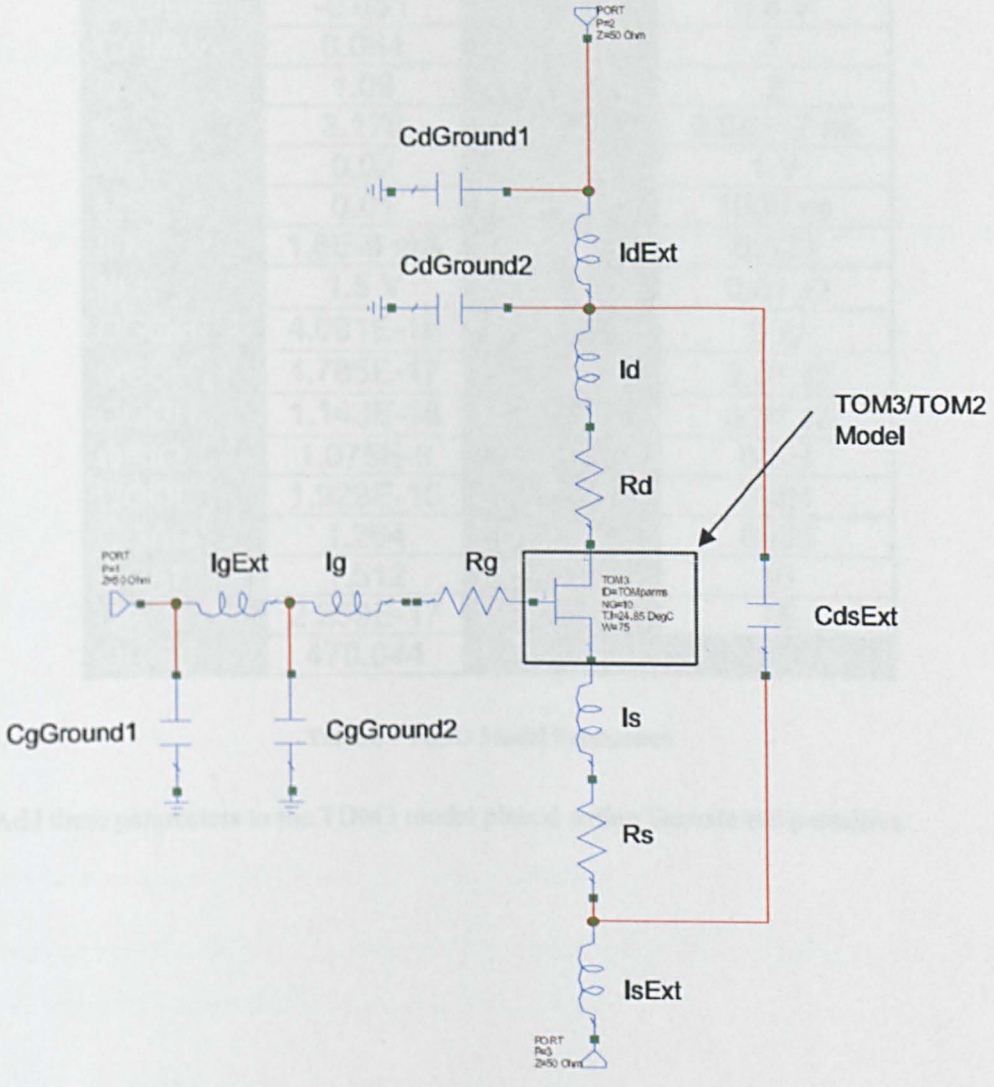


Figure 1 – Schematic of fitted model including external parasitics

TOM3 Model Parameters

The TOM3 model employs an excellent form for the charge relation within the p-HEMT discrete. Shown below are the extracted parameters for the FPD750 device:

VTO	-0.85 V	QGG0	1.936E-16
ALPHA	5.5	CDS	0.000234 pF
BETA	0.00062	IS	1E-11 mA
LAMBDA	-0.051	EG	0.8 V
GAMMA	0.064	N	1
Q	1.09	XTI	2
K	3.178	TAU	0.00117 ns
VST	0.02	VBI	1 V
MST	0.01	TAU_GD	1000 ns
ILK	1.8E-6 mA	KGAMMA	0.023
PLK	1.5 V	RG	0.01 Ω
QGQH	4.001E-16	RGSH	0 Ω
QGSH	4.785E-17	RD	0.01 Ω
QGDH	1.143E-16	RS	0.01 Ω
QGIO	1.075E-6	LS	0 nH
QGQL	1.929E-15	LG	0 nH
QGAG	1.264	LD	0 nH
QGAD	1.512	NG	10
QGCL	2.359E-17	W	75
QGGB	470.044		

Table 2 – TOM3 Model Parameters

Add these parameters to the TOM3 model placed within the external parasitics.

Appendix D

Stepped Impedance Stub

The ABCD matrix of a transmission line of electrical length θ, terminated in a load impedance Z_L is given by,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_0 \sin(\theta) \\ \frac{j \sin(\theta)}{Z_0} & \cos(\theta) \end{bmatrix}, \tag{D.1}$$

where Z_0 is the characteristic impedance of the line.

The input impedance of the line then is given by,

$$Z_{in} = \frac{AZ_L + B}{CZ_L + D} \tag{D.2}$$

The stepped impedance resonator, shown in Figure D.1, is composed of two sections of characteristic impedance Z_1 and Z_2, each of length l.

The input impedance, Z_{in2}, looking into the length of line of characteristic impedance Z_2, is found by applying (D.2) with $Z_L = \infty$, giving,

$$Z_{in2} = \frac{-jZ_2}{\tan(\theta)} \tag{D.3}$$

The impedance given in (D.3) is now the terminating impedance for the second length of line of characteristic impedance Z_1. Therefore, the total input impedance of the stepped impedance stub, $Z_{in(total)}$, can be computed by applying (D.2) with Z_L set to (D.3),

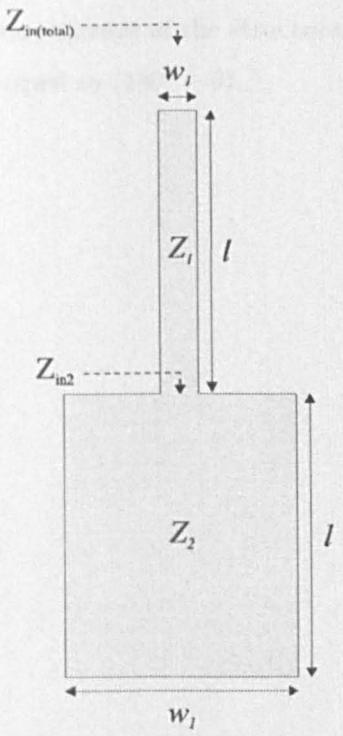


Figure D.1: Schematic of the stepped impedance resonator of characteristic impedances Z_1 and Z_2, with each section of length l.

$$Z_{in(total)} = \frac{\frac{-jZ_2\cos\theta}{\tan\theta} + jZ_1\sin\theta}{\frac{Z_2\sin\theta}{Z_1\tan\theta} + \cos\theta} \tag{D.4}$$

$$= \frac{\frac{-jZ_2\cos^2\theta}{\sin\theta} + jZ_1\sin\theta}{\frac{Z_2}{Z_1}\cos\theta + \cos\theta} \tag{D.5}$$

At resonance, the structure acts as a short circuit, resulting in $Z_{in(total)} = 0$. From (D.5) this gives,

$$Z_1\sin^2\theta = Z_2\cos^2\theta, \tag{D.6}$$

$$\therefore \frac{Z_2}{Z_1} = \tan^2\theta. \tag{D.7}$$

The impedance ratio, $Z_2 : Z_1$, can then be chosen to generate an electrical length, θ, which is equal for both sections of the stepped impedance stub. The ratio chosen

will depend on the required re-resonance of the structure, which occurs at a frequency where the electrical length is equal to $(180^\circ - \theta)$.

Appendix E

Circuit Dimensions

Optimised dimensions of the input and output matching networks of tripler designs 1, 2 and 3 are provided in this Appendix.

OUTPUT	L (mm)	W (mm)	S (mm)	INPUT	L (mm)	W (mm)
TL1	29.85	2.0		TL1	14.18	1.8
CL1	22.82	2.0	0.3	TL2	6.16	4.88
CL2	11.83	2.0	0.31	TL3	7.68	0.67
TL2	4.2	2.4		TL4	12.06	0.99
-	-	-	-	C_{inv} &	45.3	2.1
-	-	-	-	Tank Circuit	20.42	2.59

Table E.1: Dimensions of the transmission lines constituting the matching networks of Tripler design 1.

OUTPUT	L (mm)	W (mm)	S (mm)	INPUT	L (mm)	W (mm)
TL1	8.31	1.52	-	TL1	14.54	3.18
TL2	9.52	2.22	-	TL2	7.39	4.89
TL3	7.26	12.17	-	TL3	7.71	0.88
TL4	6.81	4.87	-	TL4	14.28	2.5
TL5	10.36	6.6	-	C_{inv} &	49.06	1.74
L_{inv}	2.0	2.0	-	Tank Circuit	17.25	2.5
CL1	12.02	2.0	0.51	-	-	-
CL2	23.18	2.0	0.4	-	-	-
TL6	4.2	2.4	-	-	-	-

Table E.2: Dimensions of the transmission lines constituting the matching networks of Tripler design 2.

OUTPUT	L (mm)	W (mm)	INPUT	L (mm)	W (mm)
TL1	13.34	2.34	TL1	4.53	1.2
TL2	8.41	23.33	TL2	18.10	0.6
TL3	33.36	2.3	TL3	24.48	1.18
TL4	27.70	0.6	TL4	14.06	1.36
TL5	9.07	2.59	TL5	12.82	2.01
TL6	9.78	1.81	TL6	7.1	5.0
TL7	5.72	0.58	TL7	4.0	2.4
TL8	13.78	1.46	-	-	-
TL9	2.5	2.4	-	-	-

Table E.3: Dimensions of the transmission lines constituting the matching networks of Tripler design 3.

Appendix F

Publications

1. E.Sandhiya, D. Denis and I.C. Hunter, "Novel Design Methodology for High Efficiency Class E Microwave Frequency Triplers," IEEE MTT-S International Microwave Symposium Digest, pp 1825-1828, June 2006.

2. E.Sandhiya, D. Denis and I.C. Hunter, "Class E Microwave Frequency Triplers," Filtronic Engineering Symposium, Ilkley UK, September 2006.

3. E.Sandhiya, I.C. Hunter and R.D. Pollard, "Analysis and Design of Novel High Efficiency Class E Microwave Frequency Triplers," (submitted to the IEEE Transactions).

References

[1] S. Maas, *Nonlinear Microwave and RF Circuits*, Artech House, Norwood, 2nd edition, 2003.

[2] S. A. Maas, *Nonlinear Microwave Circuits*, Artech House, Norwood, 1988.

[3] James Wong, "High performance active mixer overcomes RF transmitter design challenges", *High Frequency Electronics*, vol. 5, no. 5, pp. 38–42, May 2006.

[4] S. Ohmagari and O. Yamamoto, *Dual Conversion Transmitter*, US Patent No. 5,41,747, 1995.

[5] E. Camargo, *Design of FET Frequency Multipliers and Harmonic Oscillators*, Artech House, Norwood, 1998.

[6] W. S. Hahn, *Transceiver with Frequency Multiplier Tracked to Frequency Generator*, U.S. Patent No. 6,985,702 B2, 2006.

[7] I. Kang, *Wireless Transceiver and Frequency Plan*, U.S. Patent No. 6,028,850, 2000.

[8] T. Kawahara and T. Suetsugu, "Class E frequency multiplier driving class E amplifier", *19th International Telecommunications Energy Conference*, pp. 617–621, 1997.

[9] F. Ellinger and W. Bachtold, "Compact and low power consuming frequency/phase multiplier MMICs for wireless LAN at S-band and C-band", *IEE Proceedings on Circuits, Devices and Systems*, vol. 150, no. 3, pp. 199–204, 2003.

[10] D. M. Klymyshyn, S. Kumar, and A. Mohammadi, "A 360 degrees linear microwave phase shifter with FET frequency/phase multiplier", *Microwave Journal*, pp. 132–137, July 1997.

[11] D. M. Klymyshyn, S. Kumar, and A. Mohammadi, "Frequency stabilized direct GMSK modulator", *9th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, vol. 3, pp. 1319–1324, 1998.

[12] Michael J. Gans, *Phased Array Antennas using Ferquency Multiplication for reduced numbers of phase shifters*, US Patent No. 4,388,626, 1983.

[13] M.T. Faber, J Chramiec, and M Adamski, *Microwave and Millimeter-wave Diode Frequency Multipliers*, Artech House, Norwood, 1995.

[14] S. Maas, *The RF and Microwave Circuit Design Cookbook*, Artech House, Norwood, 1998.

[15] K.M. Johnson, "A high-performance integrated microwave circuit frequency quadrupler", *IEEE Transactions on Electron Devices*, vol. 15, no. 7, pp. 482–486, 1968.

[16] *Harmonic Generation using Step Recovery Diodes and SRD Modules*, Application Note AN-920, Hewlett-Packard, 1984.

[17] J. Zhang and A.V. Raisanen, "Computer-aided design of step recovery diode frequency multipliers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 12, pp. 2612–2616, 1996.

[18] A.V. Raisanen, "Frequency multipliers for millimeter and submillimeter wavelengths", *Proceedings of the IEEE*, vol. 80, no. 11, pp. 1842–1852, 1992.

[19] M. Albulet and R.E. Zulinski, "Effect of switch duty ratio on the performance of class E amplifiers and frequency multipliers", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 45, no. 4, pp. 325–335, 1998.

[20] D. M. Klymyshyn and M. Zhen, "Active frequency-multiplier design using CAD", *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 4, pp. 1377–1385, 2003.

[21] *Agilent ADS Circuit Simulation Manual, Chapter 7 Harmonic Balance*, 2006.

[22] J.J. Pan, "Wideband MESFET microwave frequency multiplier", *IEEE MTT-S International Microwave Symposium Digest*, vol. 78, no. 1, pp. 306–308, 1978.

[23] P. T. Chen, C. Li, and P. H. Wang, "Dual-gate GaAs FET as a frequency multiplier at Ku-band", *IEEE MTT-S International Microwave Symposium Digest*, vol. 78, pp. 309–311, 1978.

[24] A. Gopinath, A.J Seeds, and J.B. Rankin, "Comparison of single- and dual-gate FET frequency doublers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 82, no. 6, pp. 919–920, 1982.

[25] A. Gopinath and J.B. Rankin, "Single-gate MESFET frequency doublers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 82, no. 6, pp. 869–875, 1982.

[26] E. Camargo, R. Soares, R.A. Perichon, and M. Goloubkoff, "Sources of non-linearity in GaAs MESFET frequency multipliers", *IEEE MTT-S International Microwave Symposium Digest*, vol. 83, no. 1, pp. 343–345, 1983.

[27] D. Allen, D. Bryant, and W. Gaiewski, "25.5 to 76.5 GHz active frequency tripler for automotive radar applications", *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 2233–2236, 2003.

[28] C. Rauscher, "High-frequency doubler operation of GaAs field-effect transistors", *IEEE Transactions on Microwave Theory and Techniques*, vol. 83, no. 6, pp. 462–473, 1983.

[29] H. Fudem and E.C. Niehenke, "Novel millimeter wave active MMIC triplers", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 387–390, 1998.

[30] E. O'Ciardha, S.U. Lidholm, and B. Lyons, "Generic-device frequency-multiplier analysis - A unified approach", *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 7, pp. 1134–1141, 2000.

[31] Guohao Zhang, R.D. Pollard, and C.M. Snowden, "A novel technique for HEMT tripler design", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 663–666, 1996.

[32] S. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, Norwood, MA., 1999.

[33] R. Gilmore, "Concepts in the design of frequency multipliers", *Microwave Journal*, vol. 30, pp. 129–132, 1987.

[34] R. Stancliff, "Balanced dual gate GaAs FET frequency doublers", *IEEE MTT-S International Microwave Symposium Digest*, vol. 81, pp. 143–145, 1981.

[35] G. S Dow and L.S. Rosenheck, "A new approach for mm-wave generation", *Microwave Journal*, vol. 26, pp. 147, 1983.

[36] R. Larose, F.M. Ghannouchi, and R.G. Bosisio, "Multi-harmonic load-pull: a method for designing MESFET frequency multipliers", *IEEE Military Communications Conference, MILCOM '90*, pp. 466–469 vol.1, 1990.

[37] Jr. Thomas, D.G. and G.R. Branner, "Optimization of active microwave frequency multiplier performance utilizing harmonic terminating impedances", *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 12, pp. 2617–2624, 1996.

[38] G. Zhao, S. El-Rabaie, and F.M. Ghannouchi, "The effects of biasing and harmonic loading on MESFET tripler performance", *Microwave and Optical Technology Letters*, vol. 9, no. 4, pp. 189–194, 1995.

[39] J. P. Mima and G. R. Branner, "Microwave frequency tripling utilizing active devices", *42nd Midwest Symposium on Circuits and Systems*, vol. 2, pp. 1048–1051, 1999.

[40] J.P. Mima and G.R. Branner, "Synthesis of active microwave frequency triplers", *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, vol. 1, pp. 20–22, 2000.

[41] J.E. Johnson, G.R. Branner, and J.-P. Mima, "Design and optimization of large conversion gain active microwave frequency triplers", *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 7, pp. 457–459, 2005.

[42] D.L. Le, F.M. Ghannouchi, and R.G. Bosisio, "A novel approach for designing GaAs FET frequency mutipliers with optimum conversion gain and power efficiency", *Microwave and Optical Technology Letters*, vol. 5, no. 9, pp. 403–408, 1992.

[43] J. E. Penn, "Power efficienct MMIC frequency triplers", *Microwave Journal*, vol. 44, no. 6, pp. 70–84, 2001.

[44] C. Beaulieu, "Millimeter wave broadband frequency tripler in GaAs/InGaP HBT technology", *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1581–1584, 2000.

[45] H. J. De Los Santos, D. D. Nardi, K. L. Hargrove, M. Hafizi, and W. E. Stanchina, "High-efficiency InP-based DHBT active frequency multipliers for wireless communications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 7, pp. 1165–1167, 1996.

[46] A Adahl and H. Zirath, "A novel high purity, highly efficiency, broadband MMIC frequency multiplier implemented in metamorphic HEMT technology", *Proceedings of the 1st European Microwave Integrated Circuits Conference*, pp. 273–276, 2006.

[47] R. Zulinski and J. Steadman, "Idealized operation of class E frequency multipliers", *IEEE Transactions on Circuits and Systems*, vol. 33, no. 12, pp. 1209–1218, 1986.

[48] R. Zulinski, *Class E Frequency Multipliers*, PhD Thesis, University of Wyoming USA, 1985.

[49] M.D. Weiss, M.H. Crites, E.W. Bryerton, J.F. Whitaker, and Z. Popovic, "Time-domain optical sampling of switched-mode microwave amplifiers and multipliers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2599–2604, 1999.

[50] Manoja D. Weiss, "An X/K-band class-E high-efficiency frequency doubler", *31st European Microwave Conference, London*, pp. 225–228, 2001.

[51] M.D. Weiss, *Switched-Mode Microwave Circuits for High-Efficiency Transmitters*, PhD thesis, University of Colorado, 2001.

[52] M. Akkul, M. Roberts, V. Walker, and W. Bosch, "High efficiency power amplifier input/output circuit topologies for base station and WLAN applications", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 843–846, 2004.

[53] Kye-Ik Jeon, Young-Se Kwon, and Song-Cheol Hong, "Input harmonics control using non-linear capacitor in GaAs FET power amplifier", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 817–820, 1997.

[54] M. Albulet, "Analysis and design of the class E frequency multipliers with RF choke", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 2, pp. 95–104, 1995.

[55] J.C Henkus, R Overduin, and P.J Koomen, "A wideband tripler for X-band in microstrip", *Microwave Journal*, vol. 35, no. 3, pp. 106–111, 1993.

[56] O. Von Stein and J. Sherman, "Odd order MESFET multipliers with broadband, efficient, low spurious response", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 667–670, 1996.

[57] B. Thibaud, D. Barataud, M. Campovecchio, J. M. Nebus, S. Tranchant, P. Quentin, and D. Floriot, "CAD oriented design methods of frequency multipliers - application to a millimeterwave MMIC PHEMT tripler and a microwave HBT doubler", *IEEE MTT-S International Microwave Symposium Digest*, vol. 4, pp. 1747–1750, 1999.

[58] Francisco Madriz, George Vendelin, Jake Goldstein, Masoud Mostafavi, and David Chipman, "Design of pHEMT frequency triplers with conversion gain at 6 GHz", *Applied Microwave & Wireless*, vol. 12, no. 4, pp. 42–48, 2000.

[59] A. Boudiaf, D. Bachelet, and C. Rumelhard, "A high-efficiency and low-phase-noise 38-GHz pHEMT MMIC tripler", *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2546–2553, 2000.

[60] B. Bunz and G. Kompa, "A stability ensuring design approach for frequency

triplers", in *IEEE MTT-S International Microwave Symposium Digest*, 2001, vol. 1, pp. 111–114.

[61] Jui-Chieh Chiu, Chieh-Pin Chang, Mau-Phon Houng, and Yeong-Her Wang, "A 12-36 GHz pHEMT MMIC balanced frequency tripler", *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 1, pp. 19–21, 2006.

[62] I.D. Robertson and S. Lucyszyn, *RFIC and MMIC design and technology*, The Institution of Electrical Engineers, London, 2001.

[63] N.O. Sokal and A.D. Sokal, "Class E - a new class of high-efficiency tuned single-ended switching power amplifiers", *IEEE Journal of Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, 1975.

[64] A.D. Sokal, *High-efficiency tuned switching power amplifier*, US Patent No. 3,919,656, 1975.

[65] R. Negra and W. Bachtold, "Lumped-element load-network design for class-E power amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 6, pp. 2684–2690, 2006.

[66] F. Raab, "Idealized operation of the class E tuned power amplifier", *IEEE Transactions on Circuits and Systems*, vol. 24, no. 12, pp. 725–735, 1977.

[67] F.H. Raab, "Effects of circuit variations on the class E tuned power amplifier", *IEEE Journal of Solid-State Circuits*, vol. 13, no. 2, pp. 239–247, 1978.

[68] R. Zulinski and J. Steadman, "Class E power amplifiers and frequency multipliers with finite DC-feed inductance", *IEEE Transactions on Circuits and Systems*, vol. 34, no. 9, pp. 1074–1087, 1987.

[69] C.P. Avratoglou and N.C. Voulgaris, "A class E tuned amplifier configuration with finite DC-feed inductance and no capacitance in parallel with switch", *IEEE Transactions on Circuits and Systems*, vol. 35, no. 4, pp. 416–422, 1988.

[70] D.K. Choi and S.I. Long, "Finite DC feed inductor in class E power amplifiers - a simplified approach", in *IEEE MTT-S International Microwave Symposium Digest*, 2002, vol. 3, pp. 1643–1646.

[71] J.C. Mandojana, K.J. Herman, and R.E. Zulinski, "A discrete/continuous time-domain analysis of a generalized class E amplifier", *IEEE Transactions on Circuits and Systems*, vol. 37, no. 8, pp. 1057–1060, 1990.

[72] M. Kazimierczuk and K. Puczko, "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle", *IEEE Transactions on Circuits and Systems*, vol. 34, no. 2, pp. 149–159, 1987.

[73] M. K. Kazimierczuk, "Class E tuned power amplifier with nonsinusoidal output voltage", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 4, pp. 575–581, 1986.

[74] M.K. Kazimierczuk and K. Puczko, "Power-output capability of class E amplifier at any loaded Q and switch duty cycle", *IEEE Transactions on Circuits and Systems*, vol. 36, no. 8, pp. 1142–1143, 1989.

[75] P. Alinikula, K. Choi, and S.I. Long, "Design of Class E power amplifier with nonlinear parasitic output capacitance", *IEEE Transactions on Circuits and Systems II*, vol. 46, no. 2, pp. 114–119, 1999.

[76] M.J. Chudobiak, "The use of parasitic nonlinear capacitors in class E amplifiers", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, no. 12, pp. 941–944, 1994.

[77] A.J. Wilkinson and J.K.A. Everard, "Transmission-line load-network topology for class-E power amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 6, pp. 1202–1210, 2001.

[78] T. Mader, *Quasi-Optical Class E Power Amplifiers*, PhD thesis, Univeristy of Colorado, 1995.

[79] T. Suetsugu and M.K. Kazimierczuk, "Comparison of class-E amplifier with nonlinear and linear shunt capacitance", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 8, pp. 1089–1097, 2003.

[80] Y. Ayasli, A. Platzker, J. L. Vorhaus, and L. D. Reynolds, "A monolithic X-band four-bit phase shifter", *IEEE MTT-S International Microwave Symposium Digest*, vol. 82, pp. 486–488, 1982.

[81] E Carey and S. Lidholm, *Millimeter-Wave Integrated Circuits*, Springer Science and Buisness Media Inc., Boston, 1 edition, 2005.

[82] P. H. Ladbrooke, *MMIC Design: GaAs FETs and HEMTs*, Artech House, Norwood, MA, 1989.

[83] D.K. Choi and S.I. Long, "A physically based analytic model of FET class-E power amplifiers-designing for maximum PAE", *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 9, pp. 1712–1720, 1999.

[84] J.L.B. Walker, *High-Power GaAs FET Amplifiers*, Artech House, Norwood, 1993.

[85] R.B. Hallgren and P.H. Litzenberg, "TOM3 capacitance model: linking large and small signal MESFET models in SPICE", *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 5, pp. 556–561, 1999.

[86] A. Balijepalli, R. Vijayaraghavan, J. Ervin, J. Yang, S.K. Islam, and T.J. Thornton, "Large-signal modeling of SOI MESFETs", *Solid-State Electronics*, vol. 50, no. 6, pp. 943–950, 2006.

[87] M. A. Holm and D. M. Brookbanks, "Advanced meander gate p-HEMT model for accurate harmonic modeling of switch MMIC designs", in *Gallium Arsenide and Other Semiconductor Application Symposium (EGAAS)*, 2005, pp. 317–320.

[88] Rob Christ, *Foundry Update Letter*, TriQuint Semiconductor, May 1998.

[89] "Filtronic company profile", *www.filtronic.co.uk/products*.

[90] T.C. Edwards and M.B Steer, *Foundations of Interconnect and Microstrip Design*, John Wiley and Sons, third edition, 2000.

[91] D. M. Pozar, *Microwave Engineering*, John Wiley, second edition, 1997.

[92] Jia-Sheng Hong and M.J. Lancaster, *Microstrip Filters for RF/Microwave Applications*, John Wiley and Sons, Inc., 2001.

[93] M. S. Gupta, R. W. Laton, and T. T. Lee, "Frequency multiplication with high-power microwave field-effect transistors", *IEEE MTT-S International Microwave Symposium Digest*, vol. 79, pp. 498–500, 1979.

[94] D. Jahn, R. Reuter, Yi Yin, and J. Feige, "Characterization and modeling of wire bond interconnects up to 100 ghz", *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 111–114, 2006.

[95] F.H. Raab, "Class-E, class-C, and class-F power amplifiers based upon a finite number of harmonics", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 8, pp. 1462–1468, 2001.

[96] J.D. Rhodes, "Output universality in maximum efficiency linear power amplifiers", *International Journal of Circuit Theory and Applications*, vol. 31, no. 4, pp. 385–405, 2003.

[97] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, "Non-linear design of active frequency doublers", *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 9, no. 2, pp. 117–128, 1999.

[98] J. E. Johnson, A. Silva, and G.R. Branner, "Analysis of nonlinear input impedance matching in active frequency multipliers", *IEICE Transactions on Information and Systems*, vol. E88-D, pp. 1409–1416, 2005.

[99] P.M. White, "Effect of input harmonic terminations on high efficiency class-B and class-F operation of pHEMT devices", *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1611–1614, 1998.

[100] Jr. Thomas, D.G. and G.R. Branner, "Single-ended HEMT multiplier design using reflector networks", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 5, pp. 990–993, 2001.

[101] J. E. Johnson and G. R. Branner, "Fundamental analysis of harmonic reflection in microwave frequency triplers", *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 16, no. 5, pp. 483–495, 2006.

[102] Y. Iyama, A. Iida, T. Takagi, and S. Urasaki, "Second-harmonic reflector type high-gain FET frequency doubler operating in K-band", *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1291–1294, 1989.

[103] Younkyu Chung, "Optimization of second harmonic input impedance for high

conversation gain frequency doubler", *IEEE Asia-Pacific Microwave Conference*, 2003.

[104] T. Sowlati, Y. Greshishchev, C. Andre, and T. Salama, "1.8 GHz class E power amplifier for wireless communications", *Electronics Letters*, vol. 32, no. 20, pp. 1846–1848, 1996.

[105] T. Sowlati, C. A. T. Salama, J. Sitch, G. Rabjohn, and D. Smith, "Low voltage, high efficiency class E GaAs power amplifiers for mobile communications", in *16th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium Technical Digest*, 1994, pp. 171–174.

[106] Ho Chien-Chih, Kuo Chin-Wei, Hsiao Chao-Chih, and Chan Yi-Jen, "A fully integrated class-E CMOS amplifier with a class-F driver stage", 2003, pp. 211–214.

[107] J. K. A. Everard and A. J. King, "Broad-band power efficient class-E amplifiers with a nonlinear CAD model of the active MOS device", *Journal of the Institution of Electronic and Radio Engineers*, vol. 57, no. 2, pp. 52–58, 1987.

[108] T. Mader, M. Markovic, Z. B. Popovic, and R. Tayrani, "High-efficiency amplifiers for portable handsets", *Sixth IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, vol. 3, pp. 1242, 1995.

[109] T.B. Mader and Z.B. Popovic, "The transmission-line high-efficiency class-E amplifier", *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 9, pp. 290–292, 1995.

[110] H. Baher, *Synthesis of Electrical Networks*, Wiley and sons, 1984.