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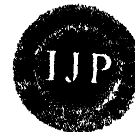

Futuristic memory device : a theoretical modeling

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Abstract The paper presents a theoretical modeling of a memory device that may be treated as an alternative to conventional flash memory devices based on the principle that proximity induces electric field modulation leading to a high ON-OFF current ratio, which can be used to distinguish betweent the two binary states 0 and 1 The present device is expected to operate with synthetic bilayer membrane opening up the possibility of a biocompatible memory device for the future A first order calculation of parameters, relevant fabrication steps and challenges in commercialization of this device are also presented The device has an edge over other flash and quantum-dot memories with respect to non-volatility and endurance

Keywords Flash-memory, synthetic bilayer membrane, charge storage, large on-off ratio

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Conventional flash memory devices [1] base their operation on the storage of charges in a floating gate layer and the modulation of the electric field because of the stored charges leading to a threshold voltage shift that results in a distinction between the two binary states. Most devices use a poly-Si layer as the floating gate. However this enhances charge leakage and degradation of the oxide layer with repeated use. The problem occurs because the charge that is stored on the gate can leak away because of the presence of local defects in the oxide layer. To overcome this problem, it was proposed that the charge could be stored in localized quantum dots embedded in an oxide layer [2]. But it was found that even such a quantum dot memory device failed to solve the problem of

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charge retention satisfactorily [3]. With shrinking device sizes, scaling of these devices has also become a problem due to easy tunneling with reduced tunnel barriers. The most logical step to overcome charge leakage from the storage node of a memory device is to cut out the leakage path which can be done by replacing a conventional floating gate by a suspended floating gate, similar to a MEMs structure. Application of silicon micromachining technologies to the nonvolatile memory device by using mechanical bistability of the object was proposed by Peterson [4] and later developed by Hälg [5]. They are expected to be compatible to conventional Si-technology and at the same time yield high-speed operation [6]. Tsuchiya *et al* were first to show that Nano Electro-mechanical systems based memory devices are viable with a layer of Si-nanocrystals as suspended floating gate and they are compitable with existing Si-micro-fabrication techniques [7].

However, with organic/biological nano-systems being continuously investigated for their potential MEMs application as sensors or in nanoelectronics [8,9], the need of the day is to fabricate a device, which can dwell with Silicon and with other technologies as well Based on the idea of a suspended membrane memory device [7], in this letter, we present a realistic theoretical modeling of such a structure using MATLAB that is expected to be more versatile in its application. This would also throw light on solving the long-standing issues of flash or quantum-dot memories.

The schematic of the device is shown in Figure 1. The device consists of a thin membrane capable of storing charges suspended over a conventional Si-MOSFET structure and the memory operation is subject to the two positions of the charged membrane and it is important that the membrane be adequately charged (explained later in text). The likely candidates for the purpose are a poly-silicon layer or a layer of nano-crystalline dots [2,10]. There are several reports which claim that nano-crystalline dots embedded in a matrix behave as effective charge storage centers and they can be easily charged by contact Atomic Force Microscope (AFM) [11,12]. However, there are quite a few issues, which should be addressed in the context of nano-crystalline quantum dots as charge storage centers. First, charging in quantum dots is self-limiting due to the Coulomb blockade effect [13] and they may not store adequate charge for successful operation of the device. Second, the charging of nano-crystalline dots is very sensitive to humidity and charge

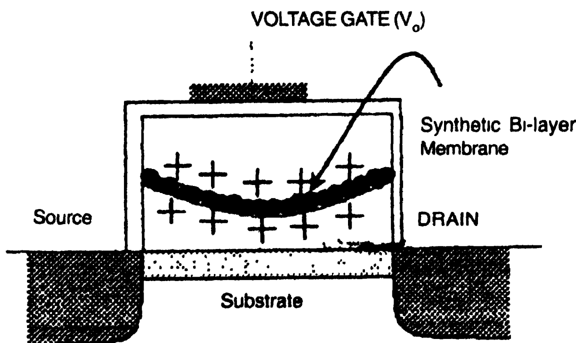

Figure 1. Schematic representation of the memory device.

leakage is enhanced in moist condition [12]. And finally, other charging methods such as application of large gate voltage as prescribed by Tsuchiya *et al* [7] are not user friendly The alternative would be to use synthetic bilayer membranes such as lipid bilayers as they are easily available in various charged states depending on their structure [14] It has three-fold advantages : (1) As synthetic bilayers are available in charged state, there is no need for additional charging ; (2) The total charge contained in a typical a 100 nm × 100 nm × 50 nm synthetic bilayer membrane is much above the threshold value needed for switching operation of the device [15] and, (3) The bilayers can be made to bend on application of electric field much more easily than a layer containing nanocrystalline quantum dots to achieve bistability [16].

The fabrication process involves deposition of an oxide/nitride layer on top of the substrate followed by the deposition of a photo-resist by spinning Etch windows are then defined on the resist. A combination of anisotropic and isotropic dry etching in proper sequence is then carried out to provide the release of the structure as suggested by Cleland and Roukes [17]. Figure 2 depicts the Scanning Electron Micrograph image of a SiO_2 structure in floating condition

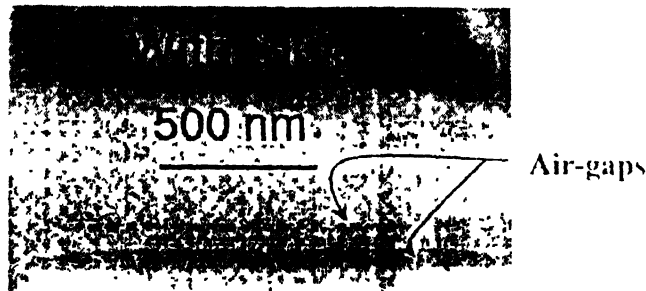

Figure 2. Air gaps are clearly observed in a SiO_2 structure indicated by arrows

Instead of conventional memory devices, which differentiate between the two binary states based on a threshold voltage shift between the two states, here we use the ratio of the ON current (strong inversion) and the OFF current (weak inversion) to separate the two states. This is achieved by having the membrane in two stable states (bi-stability, shown in Figure 3) wherein state 1 is a rest state (stable equilibrium) whereas the second one is that of unstable equilibrium wherein an external electric field has to be applied to hold the membrane in this position. The proximity of the membrane to the substrate leads to electric field modulation in the substrate resulting in strong and weak inversion respectively that can be differentiated by the currents in the two cases.

The electric field in an MOS structure is given by

$$\xi = (-\delta\psi/\delta x) = \left(\sqrt{2}\,kT/qL_D\right) F\left(\beta\psi, n_{po}/p_{po}\right) \tag{1}$$

where

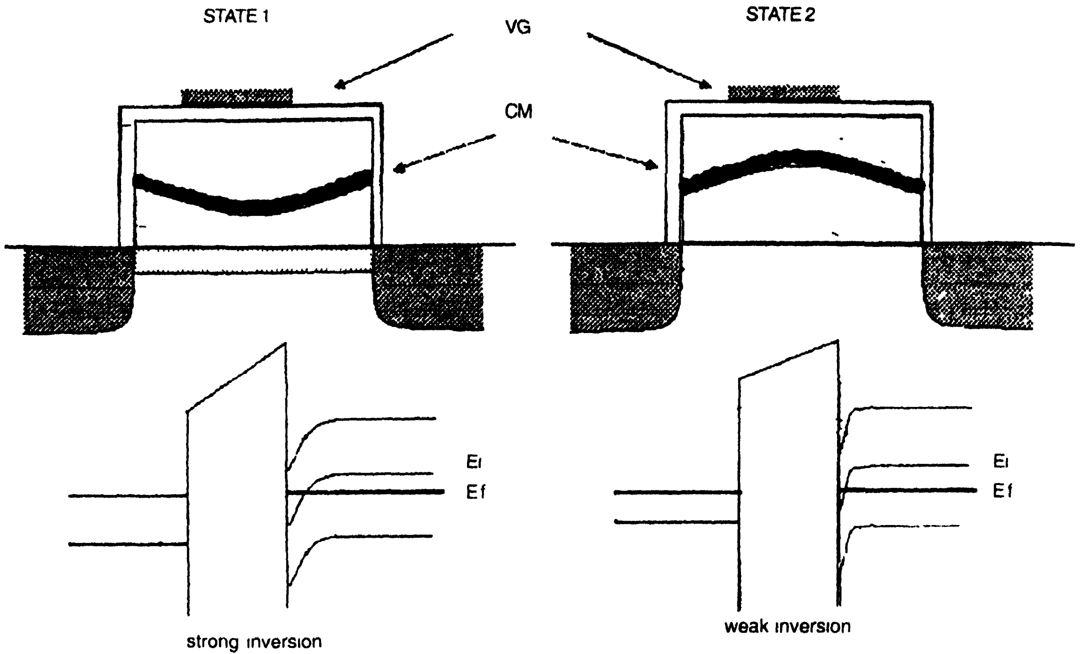

Figure 3. The two stable states of the device (CM = charged Membrane; V_G = Gate Voltage, E_f = Fermi Level; E_i = Intrinsic Energy Level).

ψ : defined as zero in the bulk and measured with respect to the intrinsic Fermi level, n_{po}, p_{po} : equilibrium carrier densities in the bulk, L_D : extrinsic Debye length, k Boltzmann constant, T : Absolute temperature

$$F(\beta\psi, n_{po}/p_{po}) = \left[\left(e^{-\beta\psi} + \beta\psi - 1\right) + n_{po}/p_{po}\, e^{\beta\psi} - \beta\psi - 1\right]^{1/2}. \qquad (2)$$

Considering

Strong inversion : $\psi_s = 2\psi_F$,

Weak inversion : $\psi_s = 05\psi_F$,

and 100% ionization $\left(p_{po} = N_a,\ n_{po} = n_i^2/N_a\right)$ in the bulk.

Considering the background concentration to be variable, we plot the charge on membrane required for strong and weak inversion as a function of the substrate concentration (Figure 4). The difference in the electric field leads to the high ratio between the ON/OFF current, which can be detected.

One can also get an estimate about the Ion/Ioff ratio using similar plots of I_d (drain current) *vs.* V_{DS} (Source-to-drain voltage) for MOSFET operation [1] in the normal and in the sub-threshold regions of operation. As weak inversion lies in the sub-threshold region

of operation, an intuitive feel of the order of magnitude of difference between the two currents can be obtained. As is illustrated by the graphs, this has an order of magnitude difference of at least 3 (normal MOSFET current having values around mA whereas sub-threshold currents falling in the μA region) [1].

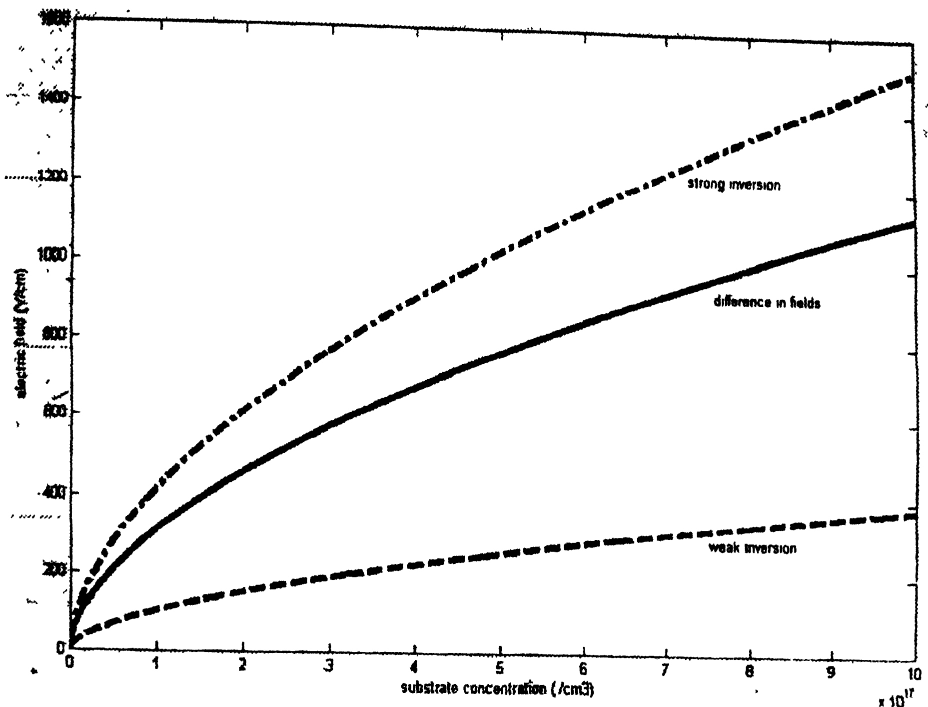

Figure 4. Electric field required for strong and weak inversion with respect to the substrate concentration

Assuming the membrane is located at a distance, *d* from the substrate, we can estimate the charge required on the membrane by Coulomb's models using a first order approximation. Even if the membrane is of nano-dimension, the classical Coulomb model, which is purely electrostatic in nature, remains valid for further calculations and has been used by several authors [7]. Three such values of *d* (10nm, 50 nm, 100 nm) are assumed and the charges required for bi-stable memory operation has been plotted as a function of the substrate concentration (Figure 5).

Knowing the field required to cause weak inversion, we can again use Coulomb's model to get the value of distance d_2, where d_2 represents the distance between the membrane and the substrate for the second bi-stable state. For the same three values of d_1, the plots of the bi-stable distances *vs.* the substrate concentration are obtained and they are shown in Figure 6.

As is evident from the plots, a high substrate concentration leads to a higher difference between the two field values but requires considerably higher charge values. Therefore the

design of the membrane involves a tradeoff between factors such as electric field separation and charging of the membrane Moreover, as argued before, a thin suspended membrane

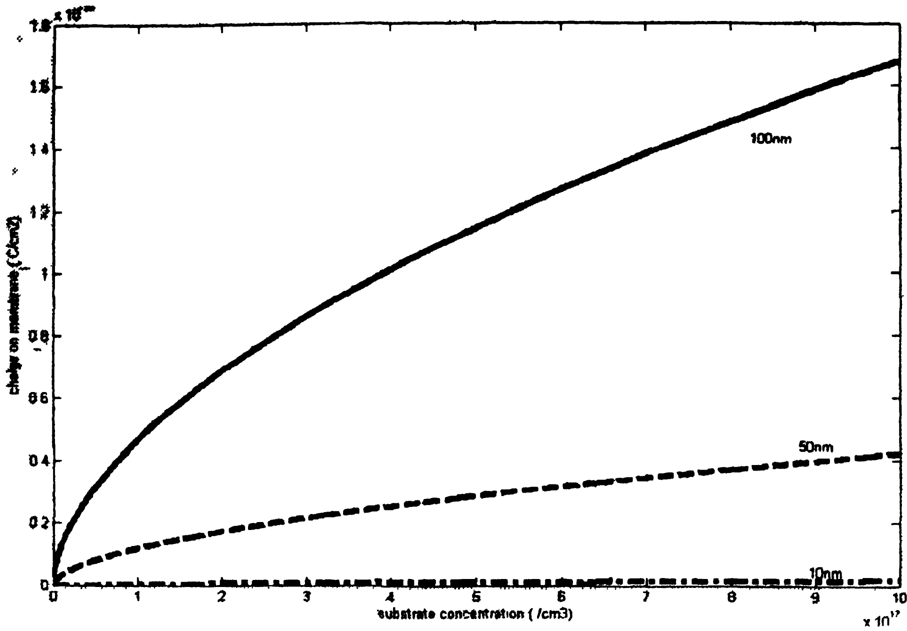

Figure 5 Substrate concentration vs charge on membrane for different d values

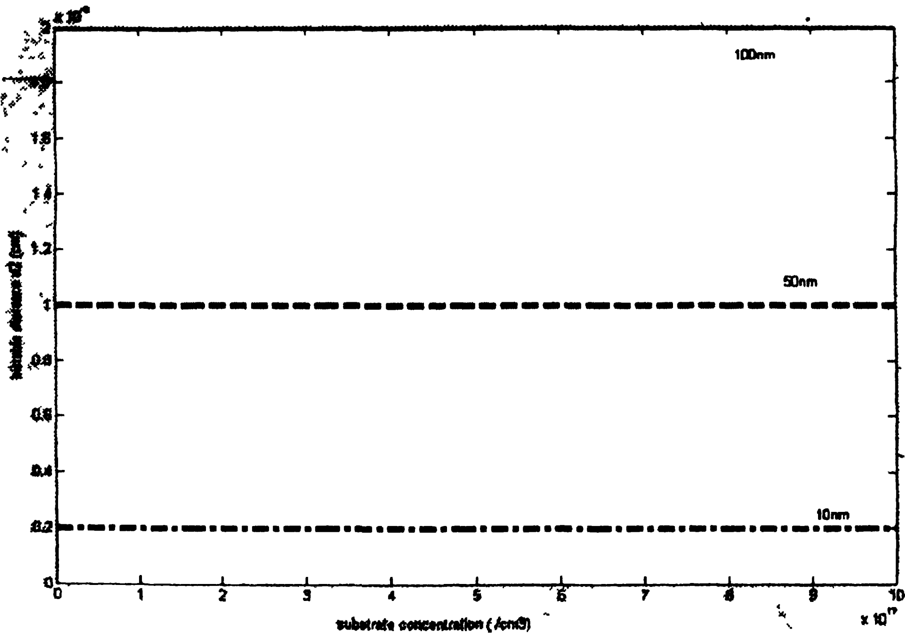

Figure 6. Plot of bi-stable distance 'd_2' as a function of substrate concentration

with enhanced charge trapping capabilities would be more appropriate for the purpose However, the mechanism to get the membrane into the second bi-stable state could be through an application of an electric field The calculation of the field is a simple force balance equation between the force exerted by the electric field on the membrane and gravity This may be used as a suitable starting point for more refined calculations

As estimate of the frequency of operation of the membrane has been done by calculating the resonance frequency of the beams, which are given as [17]

$$\omega = 2 * \pi * \left(w/L^2\right) * \sqrt{(E/\rho)}$$

where

ω -resonance frequency,

E - Young's Modulus

ρ - density

w - beam width in the direction of motion and

L - beam length

Taking beam dimensions being (100 nm x 100 nm x 50 nm), we arrive at a value greater than 25 GHz that is close to the value obtained for a nanometer-scale mechanical resonator [17] Though it establishes the suitability of this memory for high frequency applications there are several problems still persisting associated with the fabrication of the device and integrating it into Si-IC manufacturing processes The fabrication steps involved to arrive at the memory structure are intricate and challenging The mechanical and the elastic properties of the membrane should also be thoroughly investigated for a successful operation the device It is to be noted that the resonance frequency for a charged membrane is different from that of an uncharged one and hence suitability of a charged membrane for high frequency operations needs to be reassessed

If we compare the two memory structures, conventional flash memory and the theoretically modeled memory that is expected to operate with organic/biological system, we find that in case we use the new structure as a random access memory (RAM), it is expected to provide much faster writing time as compared to flash memories where both 0 and 1 need to be written with suitable voltage application between the source and the gate Also this process provides a lesser power consumption especially if the data is biased towards one bit and we exploit this fact Problems before commercialization involve the fabrication of several membranes on a chip, pre-charging them, determining the ideal combination of substrate concentration, membrane distance and the electric field for bi-stability Investigations are already underway to address the above-mentioned issues as a suspended floating gate memory device may solve many long-standing problems of a flash memory

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