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Copper Electrodeposition in Mesoscale Through-Silicon-Vias

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COPPER ELECTRODEPOSITION IN MESOSCALE THROUGH-SILICON-VIAS

BY

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DEDICATION

This work is dedicated to my beautiful wife, Shelley, who through her endless love and profound positivity has pushed me to pursue my dreams.

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I am thrilled to have the opportunity to thank a few of the many people who have helped to make this possible. First, my mentor and advisor, Sang M. Han, guided me during a crucial time in my development as a student and engineer. It was initially through Prof. Han's extraordinarily precise and clear classroom instruction that I developed a true understanding of the incredible work ethic that it takes to excel as a scientist or engineer. In addition, Prof. Han allowed me to join his research group, where I gained the hands-on experience that ultimately culminated in my accepting an internship with Sandia National Laboratories. To Prof. Han, I sincerely thank you for your generosity of spirit, kindness, and for always pushing me to live up to your exemplary standards.

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Finally, I want to thank my brother, Sean, my mom, Judy, my Dad, Randy and Stepmom, Pearl for too many things to even begin to name. I'll never be able to repay you for all the love and support you have given me.

Lastly, I want to thank my incredible wife, Shelley, whose face is in my dictionary, next to the word "perfection".

Thank you everyone!

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ABSTRACT

Copper (Cu) electrodeposition (ECD) in through-silicon-vias (TSVs) is an essential technique required for high-density 3-D integration of complex semiconductor devices. The importance of Cu ECD in damascene interconnects has led to a natural development towards copper electrodeposition in TSVs. Cu ECD is preferred over alternative approaches like the chemical vapor deposition (CVD) of tungsten (W) or aluminum (Al) because Cu ECD films have lower film stress, lower processing temperatures, and more optimal thermal and electrical properties as compared with CVD W or Al.

Via filling with electroplated Cu on substrates that have undergone atomic layer deposition of a conformal platinum seed metal is investigated herein. These mesoscale vias (600 μm depth, 5:1 aspect ratio) will be utilized in ultra-high-vacuum systems and thus require a uniform, void-free Cu deposit of sufficient thickness to prevent device degradation due to skin effects when RF frequencies as high as 100 V at 100 MHz are used. Conformally Cu-lined TSVs are achieved through the implementation of a complex ECD parameter scheme, and these results are compared with computational finite element modeling (FEM) outcomes. A novel, single additive chemistry is also developed and implemented to achieve fully filled void-free mesoscale TSVs within 6 hours of plating time, which represents an extraordinarily fast and controllable plating rate (100 μm/hour) for interconnect (IC) feature filling.

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Chapter 1: Introduction

1.1 Chapter Overview

In Chapter 1, the unique feature geometry and application is addressed in detail. This section highlights the particularly large depth of the TSVs investigated and the extreme environment under which they must operate. In addition, the thickness and film quality requirements of the electrodeposited Cu are discussed.

In Chapter 2, the fundamentals of acid sulfate copper electrodeposition are outlined. This information is gleaned from a thorough literature survey, which is both a deep and wide pool from which to search, as copper ECD has been thoroughly explored over the last century. In particular, this literature survey was focused on the chemical kinetics and transport phenomena associated with via and trench filling in the microelectronics industry.

In Chapter 3, the detailed experimental methods utilized in this research are discussed in order to provide the reader with the necessary detail to understand how the work outlined in this writing was conducted. In addition, specific issues and challenges related to the various experiments are presented.

In Chapter 4, a conformal Cu ECD process is outlined. In particular, several techniques for achieving a sufficiently thick Cu lining of these mesoscale TSVs is described. In addition, potential further improvements to the existing experimental work is highlighted for the reader.

In Chapter 5, a novel approach to TSV filling is presented. This approach utilizes a finely tuned combination of chemistry, convection, and electrochemical parameter optimization

to achieve localized deposition, largely dependent on a concentration gradient of large chain polymeric suppressor molecules.

In Chapter 6, a summary of the relevant results and potential for future experimental investigation is outlined. Specifically, this chapter reestablishes the important progress made in developing multiple methods for conformally coating these mesoscale TSVs with Cu. Additionally, this chapter highlights promising results and the potential for future improvement of the S-shaped negative differential resistance (S-NDR) technique for fully filling TSVs or trenches of varying geometries.

1.2 Background

1.2.1 Copper Electrodeposition in Microelectronics

Copper has been a ubiquitous metal in semiconductor interconnects since 1997, when IBM developed a method to replace aluminum (Al) chemical vapor deposition (CVD) with wet chemical Cu ECD to form interconnect structures essential to many devices that the semiconductor industry relied on at the time and continues to rely on today, only at much smaller size scales.[8] Andricacos et. al. introduced a Cu ECD process that significantly improved upon the Al CVD process that had been almost exclusively used in industry up to that point.

There are many obvious advantages and a few small disadvantages when comparing the efficacy of Cu ECD compared with Al CVD in forming interconnects for the microelectronics/semiconductor industry. First, Cu ECD is generally less expensive and greatly improves throughput compared to Al CVD. Secondly, the material properties of bulk Cu are far superior to Al for device performance, as shown in Table 1 below. [9-11]

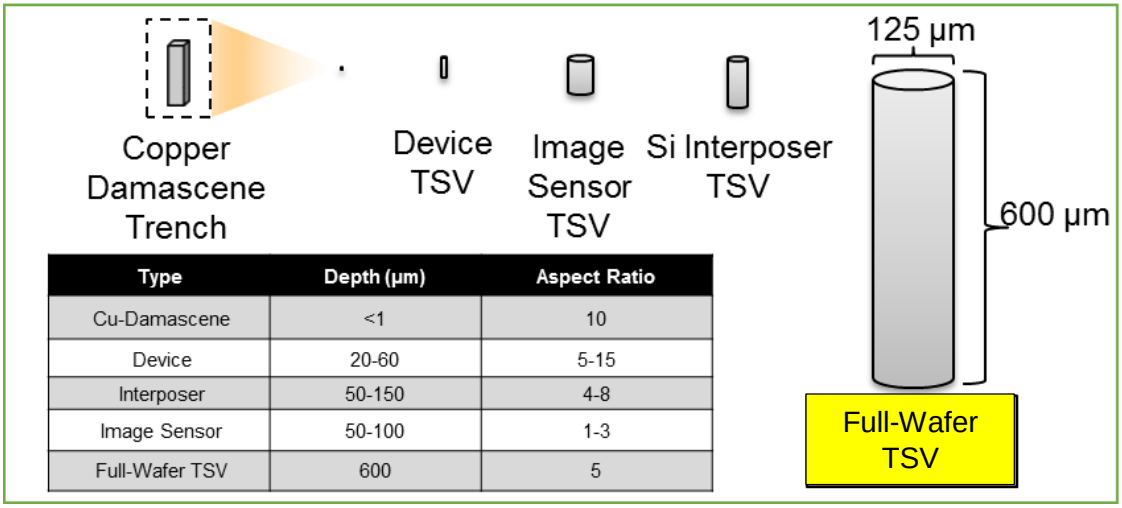
Material properties of pure Copper and Aluminum				
Material property	**Dimension**	**Copper**	**Aluminum**	**Tungsten**
Density (@20°C)	$g \cdot cm^{-3}$	8.94	2.7	19.3
Electrical resistivity (@20°C)	$n\Omega \cdot m$	16.8	28.2	52.8
Thermal expansion (@25°C)	$\mu m \cdot m^{-1} \cdot K^{-1}$	16.5	23.1	4.5
Thermal Conductivity	$W \cdot m^{-1} \cdot K^{-1}$	385	205	173
Typical Tensile Stress	Mpa	10-100	200	1150

Table 1: Pure Cu and Al material properties comparison [9-11]

Third, Cu is a far better conductor of heat and electricity than Al, therefore Cu can be used more effectively as a heat sink or current flow path in any microelectronic device. In Table 1, one can see that Cu has a thermal conductivity value (385 $W \cdot m^{-1} \cdot K^{-1}$) about twice as large as that of Al (205 $W \cdot m^{-1} \cdot K^{-1}$) and W (173 $W \cdot m^{-1} \cdot K^{-1}$) and Cu has an electrical resistivity value (16.8 $n\Omega \cdot m$) about half that of Al (28.2 $n\Omega \cdot m$) and three times that of W (52.8 $n\Omega \cdot m$). Finally, just like Al CVD, Cu ECD allows for non-directional deposition, so the workpiece (working electrode or cathode in an ECD cell) being electroplated can have vertical sidewalls orthogonal to the counter electrode (or anode) and still be uniformly plated in Cu. This compares positively with Al CVD, which is also non-directionally conformal, but this process that is far more time consuming, and generally not advisable for laying down films thicker that ~1 µm. In addition to the advantages Cu ECD has over Al CVD, tungsten (W) CVD has also be utilized to conformally coat interconnects in microelectronics. However, W CVD leads to films with much higher stress (1150 Mpa) than films deposited through Cu ECD (10-100 Mpa), and, similarly to Al, W CVD is not a suitable technique for deposition of sufficiently thick films in mesoscale features.

The final ECD advantage above is of merit when considering the device scale utilized in this work. There are two common device geometries that are widely used in industry,

namely ‘trenches’ and ‘vias’. Trenches tend to exist below 5:1 aspect ratios, while vias



Type	Depth (µm)	Aspect Ratio
Cu-Damascene	<1	10
Device	20-60	5-15
Interposer	50-150	4-8
Image Sensor	50-100	1-3
Full-Wafer TSV	600	5

Figure 1: Scaled-up sketch of common Cu interconnects comparing their depths and aspect ratios[1]

can reach aspect ratios as large as 10:1. A ‘trench’ is effectively confined in only 2 dimensions, width and depth, whereas a ‘via’ is confined in all 3 dimensions, width, depth, and length. This difference is immensely important in terms of the ability for fluid and ion replenishment to occur down the feature depth during the ECD and/or CVD process.

In general, these features are anywhere between 10 nm – 50 µm in diameter, where the forefront of the current technology has recently dipped below 10 nm feature diameters or channel widths. The unique feature geometry investigated in this work is in a ‘mesoscale’ size regime, which is a catch-all term for features larger than 100 µm in diameter or height and smaller than 1 mm. A to-scale comparison between typical feature sizes and the features investigated herein can be seen in Figure 1. Filling features of this mesoscale geometry is unique. This work was able to leverage the understanding that has come out of semiconductor industries and sub-100 µm features as well as microelectrics printed circuit board manufacturing which has much larger features than the mesoscale TSVs

discussed here but novel investigation was required as literature has not focused on these mesoscale geometries.

1.2.2 Interconnects for High Voltage, RF, and UHV Applications

A significant amount of development has been achieved integrating TSVs with standard silicon (Si) substrates; however, very little development has been made integrating this technology with silicon-on-insulator (SOI) substrates.[12] Certain MEMS applications

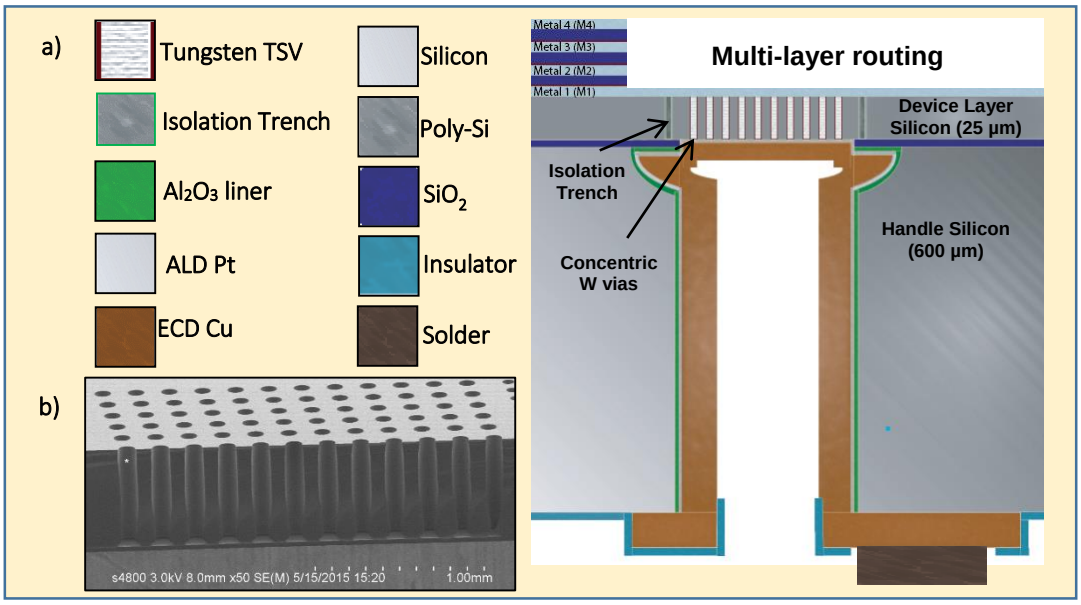


Figure 2: a) Schematic diagram showing TSV and surrounding integration scheme and b) SEM image of TSV arrays

take advantage of the use of SOI wafers with relatively thick device layer silicon, however the integration of TSVs with these unique SOI substrates (e.g., 600 µm handle, 1 µm buried oxide, and 25 µm thick device layer) presents distinct challenges when making electrical contact through the device layer Si, buried oxide (BOX), and the handle Si. This is particularly true for cases in which the handle Si is not thinned, as is commonly done is a 'TSV reveal' approach[13-15] where the TSVs are fabricated before the bulk Si is thinned using chemical mechanical planarization (CMP) to reveal the vias. In this work, we present a novel TSV integration approach which is neither a TSV-first or

TSV-last approach but instead a hybrid, W-TSV-first connected to a Cu-TSV-last approach. Electrochemical deposition (ECD) is ultimately used to connect mesoscale copper (Cu) vias filled in the handle of the substrate to microscale tungsten (W) vias filled by chemical vapor deposition (CVD) in the device layer of a SOI substrate. The novel aspect of these two integration approaches is the mating of metal TSVs across a (thick) SOI substrate dielectric layer. A sketch of the fundamental layout surrounding a single TSV interconnect is shown in Figure 2.

As shown in Figure 2, the Cu vias are electrically connected to W vias filled in the handle layer of the SOI substrate. These deep reactive ion-etched (DRIE) CVD-W filled vias are in the form of concentric circles where each group of self-terminating W trenches is electrically isolated from adjacent groups as well as from the device Si layer using an oxide filled isolation trench, where the oxide serves as a mechanical support for the via. A closer look at this integration scheme is shown in Figure 3. As shown in this figure, there exists a CVD deposited, conformally lined W TSV utilized for electrical connection through the device Si with an oxide filled isolation trench surrounding the W TSVs.

DRIE has become the most accepted process for creating TSVs when working with semiconductor materials. An insulating material for electrical isolation, a barrier layer to prevent diffusion, and a conductive material for electrical connection are all necessary components of a via. CVD is typically used for all three of these purposes if the film thicknesses and aspect ratios are relatively small and the geometries are not overly complex. In relation to Figure 3, ALD is utilized for both the insulating layer and the diffusion barrier because CVD is not capable of conformally coating the notched feature

at the bottom of the backside TSV. More detailed images of the ideal W via and isolation trench layout and the resulting deposition result can also be seen in Figure 4.

ECD is used to fill the vias with a conductive material when via dimensions are too large for CVD, which is common in MEMS applications. When features are particularly large like the Cu TSVs examined in this work, evaporative techniques are not capable of completely filling the features.

After the device layer W vias and isolation trenches (the isolation trench is filled with undoped polysilicon as a mechanical support for the insulating SiN_x layer) are filled, multiple metal layers are used to route the electrical signals of the device. After all of the topside processing is complete the substrate is flipped over and DRIE is used to etch the backside TSV using the buried oxide layer as an etch stop for the deep Si etch. Etch non-uniformity across the wafer requires a significant amount of over etch when performing this deep Si etch in order to ensure that every backside TSV is well landed across the 6 in. wafer. Because of the over etch ion reflection occurs and causes the notched feature in the Si at the bottom of the via that is apparent in Figure 3. A directional RIE is then used to etch the buried oxide at the bottom of the TSV and reveal the bottom of the W vias. The notched feature at the bottom of the backside TSVs requires the use of ALD for the insulating liner and the ECD seed metal. ALD is used to deposit a conformal layer of Al_2O_3 to insulate the Cu-TSVs from the handle Si. A spacer etch is performed to remove the Al_2O_3 from horizontal surfaces, (the backside of the substrate and the layer coating the bottom of the W vias), revealing the W TSVs previously fabricated in the device layer

After the device layer W vias and isolation trenches (the isolation trench is filled with undoped polysilicon as a mechanical support for the insulating SiN_x layer) are filled,

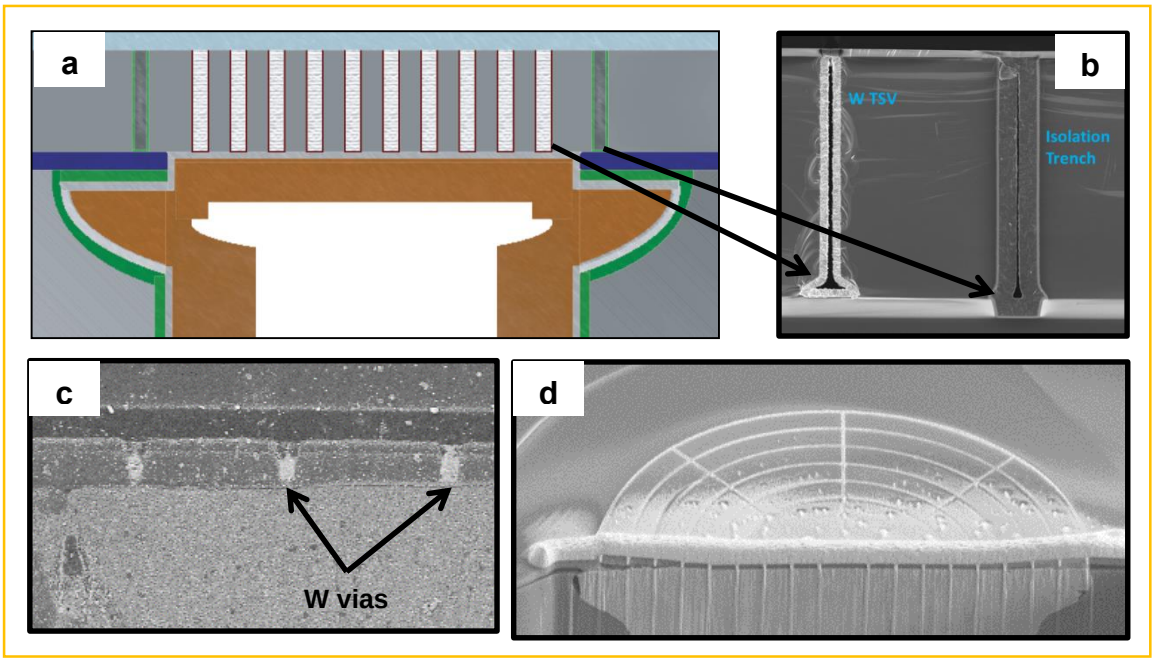


Figure 3: a) Close-up sketch of Cu TSV bottom focusing on W vias and oxide isolation trench b) SEM images of cross sectioned W via and isolation trench c)cross section of W vias d) FIB cut image of Cu TSV underside showing concentric W via layout for electrical connection through device layer Si

multiple metal layers are used to route the electrical signals of the device. After all of the topside processing is complete the substrate is flipped over and DRIE is used to etch the backside TSV using the buried oxide layer as an etch stop for the deep Si etch. Etch non-uniformity across the wafer requires a significant amount of over etch when performing this deep Si etch. Because of the over etch ion reflection occurs and causes the notched feature in the Si at the bottom of the via that is apparent in Figure 3. A directional RIE is then used to etch the buried oxide at the bottom of the TSV and reveal the bottom of the W vias. The notched feature at the bottom of the backside TSVs requires the use of ALD for the insulating liner and the ECD seed metal. ALD is used to deposit a conformal layer of Al_2O_3 to insulate the TSVs from the handle Si. A spacer etch is performed to remove

the Al_2O_3 from horfizontal surfaces, (the backside of the substrate and the layer coating the bottom of the W vias), revealing the W TSVs previously fabricated in the device layer Si.

The application of the features investigated herein is for the integration of TSVs with devices utilized for ion trapping. Specifically, with regards to the ion traps themselves, the operation of these devices adds several significant constraints on the TSVs that are to be developed. Previous iterations of these microfabricated surface electrode ion traps have used gold wire bonds as interconnects. However, wire bonds reduce optical access for cooling lasers that are required when manipulating ions above the surface of the electrodes. In addition, wire bonds limit the maximum input/output (I/O) on a chip

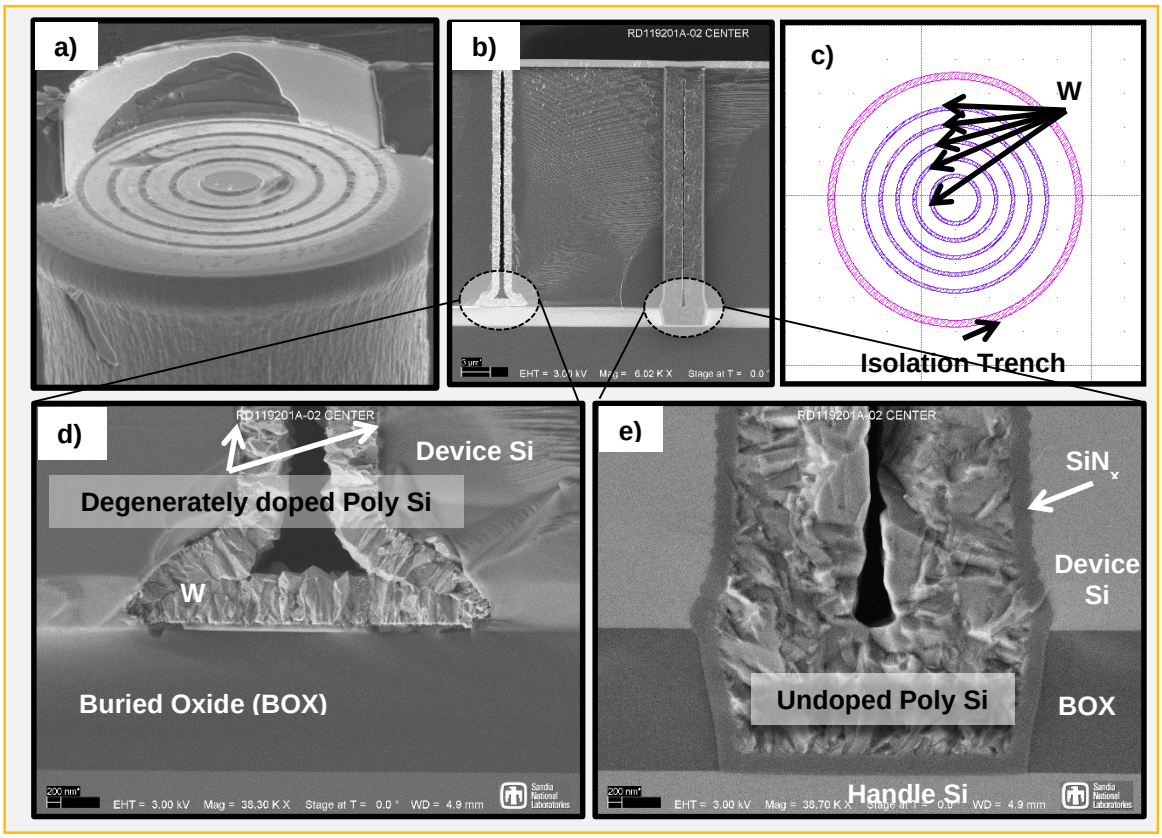


Figure 4: a) Underside view of concentric W vias and isolation trench b) Cross-sectional image of single W via and isolation trench c) Schematic layout of W and isolation trench concentric circles d) Close-up SEM image of W via bottom e) Close-up image of isolation trench bottom

because they are restricted to the perimeter of the die. TSVs allow a greater I/O density because they can utilize the entire area of the die as opposed to the perimeter of the die. In addition to increasing electrical I/O density, these TSVs increases thermal dissipation for pulling away heat generated from high voltage RF signals as compared to depending on the thermal conductivity of the SOI substrate. In Figure 5, one can see sketches and an optical image of these surface ion traps both with wire bonds and TSVs. Specifically, in Figure 5 a) the cross-sectional sketch of the original ion trap assembly package is shown which relies on wire bonds for integration and in Figure 5 b) an optical image of a fabricated surface ion trap with original wire bonds is shown in Figure 5 c) a simplified schematic with the improved, TSV-integrated package is shown where the TSVs are hidden as they connect through the SOI substrate beneath the device and Figure 5 d) an

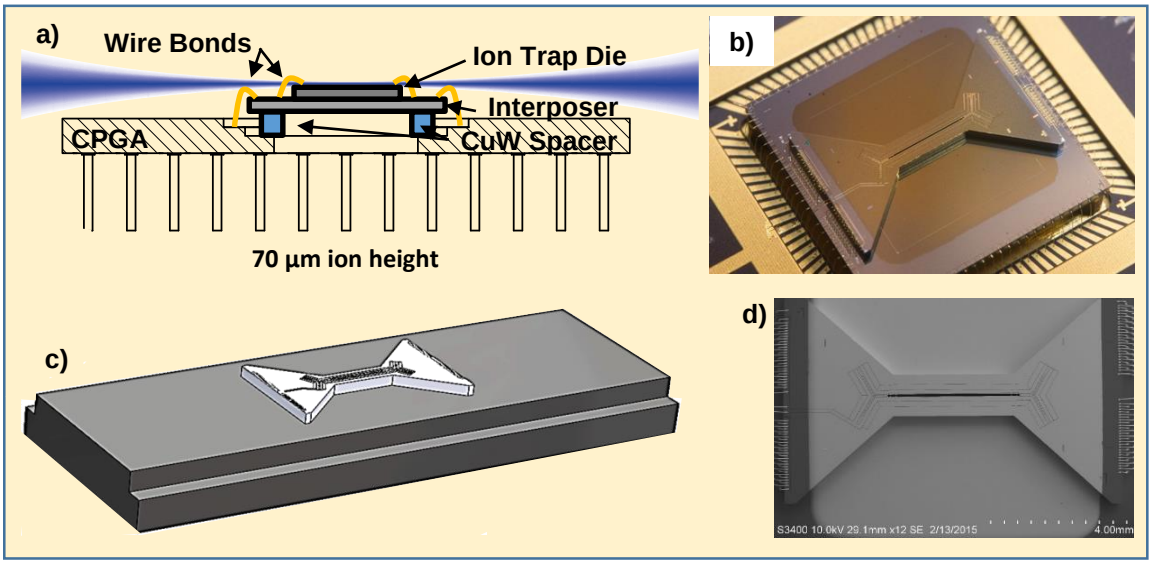


Figure 5: a) Schematic of original surface ion trap iteration relying on wire bonds for integration b) Optical image of completed surface ion trap with wire bonds c) Simplified schematic where TSVs are not seen as they connect through the SOI substrate beneath the device d) SEM image of original surface ion trap layout

SEM image of the top side of the original surface ion trap is shown.

These ion traps are operated under ultra-high-vacuum (UHV ~ 10^{-12} torr) conditions, so any voids within the electrodeposited copper have the potential of outgassing and

disrupting the UHV environment or creating a virtual leak in the UHV chamber. Voids can also lead to either immediate or eventual interconnect failure as trapped electrolyte slowly etches away at the electrical contact. As described in more detail in the sections to follow, the avoidance of forming voids is the main motivator our integration approach and creates unique restrictions for this work.

In addition to the void concern highlighted above, the fact that these ion traps are operated at extremely low temperatures (4 K) provides an argument for the uniquely large mesoscale size, as several amperes of current will be flowing through the features at any given time during device operation. Thus, joule heating is another major concern which influences the momentum of the trapped ion, so the high thermal conductivity of Cu and large thermal flux surface area of this mesoscale interconnects proves an ideal combination for use as an effective heat sink as well as electrical interconnect. The final item of concern with regard to these features relates to the electrical potential (100 V) and RF signal frequency (100 MHz) that will be applied across these features. This combination of potential and frequency leads to a significant Cu 'skin effect' where leakage between adjacent devices, or crosstalk, can occur if the Cu is too thin. From the breakdown voltage of the Al_2O_3 insulating layer between the ECD Cu and the Si handle, shown in Figure 6, a copper thickness (or 'skin depth') of greater than 6.52 μm is required, as the Al_2O_3 is easily broken down at low voltages. Most importantly, if the Cu isn't thick enough the RF field will partially couple to the Si, causing higher capacitance and a short to the handle Si. If this were to occur, it would be a catastrophic failure of the device. The Cu skin depth value, 6.52 μm, was found using Equation 1, where the

standard bulk Cu resistivity (ρ), frequency applied across the interconnect (f), and absolute magnetic permeability of Cu (μ) are the underlying variables that define the skin depth (δ). The ultimate thickness of ECD Cu needs to be at least 2X the 'skin depth', thus a plating process for conformally lining these TSVs with 15 µm thick of Cu is developed in this work.

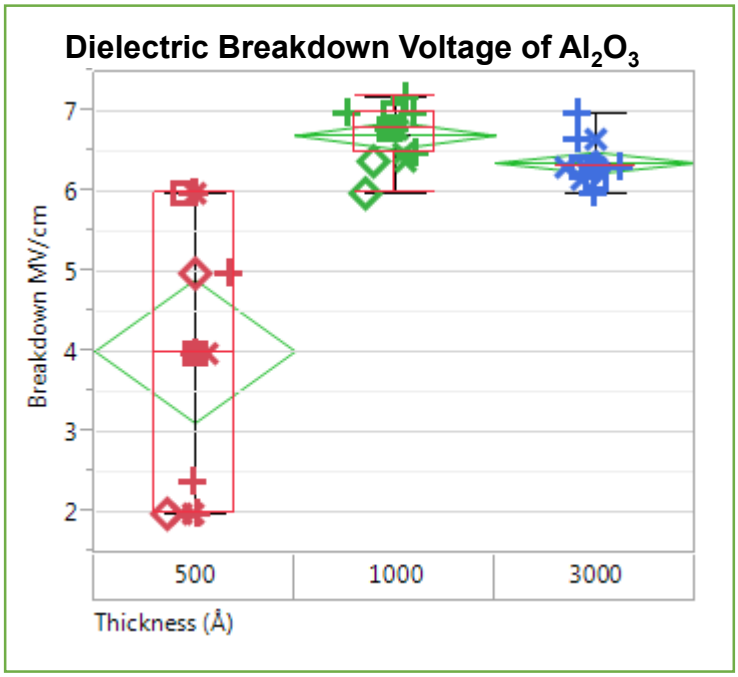


Figure 6: Graph showing estimated breakdown voltage for the insulating Al_2O_3 layer at various thicknesses

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \qquad (1)$$

As discussed above, these TSVs are to be utilized as through-substrate interconnects in order to improve the package simplicity and optical access for devices used to trap and manipulate ions. Due to the mesoscale nature of these vias, with approximately 600 µm depths and 125 µm widths, there are certain unique geometric issues that arise. The two most important features of these TSVs for Cu ECD purposes are their size and the unique profile of the notched feature at the bottom of the vias caused by ion reflection from the buried oxide etch stop. The conformality of the ALD Al_2O_3 is shown in Figure 7 highlighting how uniformly this deposition is able to coat the hard mask undercut feature as well as the notched features at the via bottoms. Specifically, in Figure 7 a) the Al_2O_3

sidewall thickness measurement using an SEM image is shown, b) an SEM image of the Al_2O_3 hardmask undercut thickness, c) an SEM image of the Al_2O_3 via-bottom notch

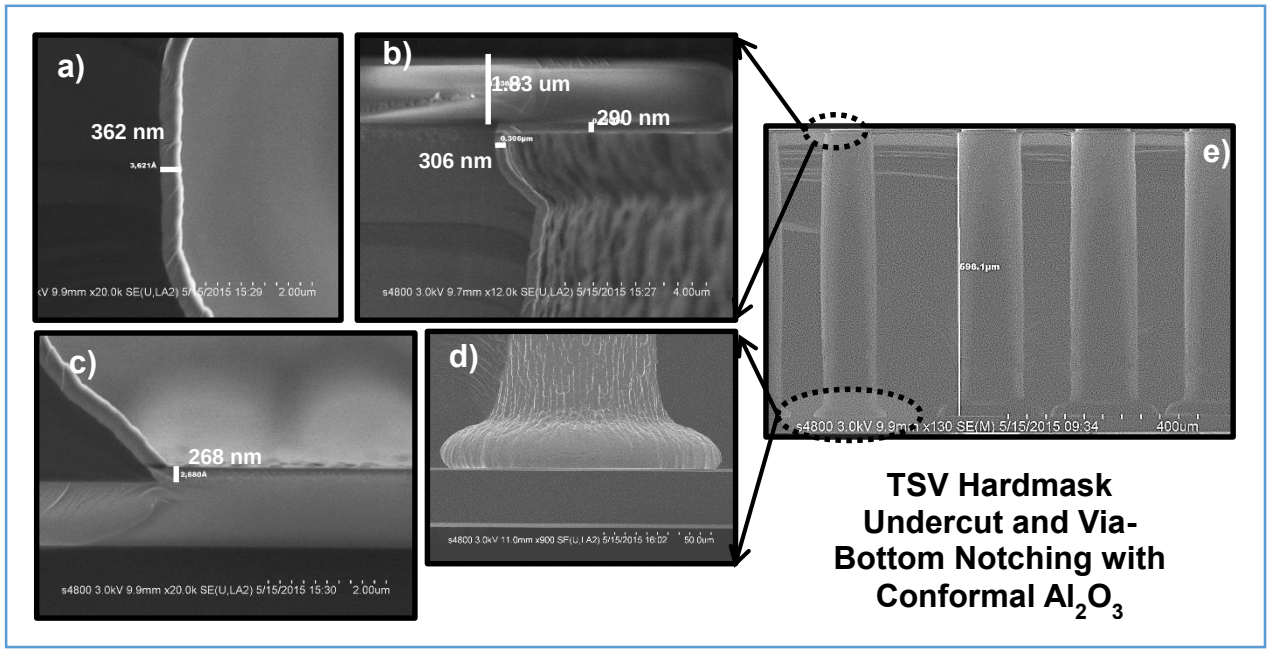


Figure 7: a) Al_2O_3 sidewall thickness b) Al_2O_3 hardmask undercut thickness c) Al_2O_3 bottom notch thickness d) Full SEM image of DRIE caused notching at via bottom e) SEM cross-sectional view of via array

thickness, and d) an SEM image of DRIE-caused notching at via bottom. Lastly e) an SEM cross-sectional view of a via array. These images make a clear-cut case for the use of ALD Pt as a seed material prior to Cu ECD as ALD will allow for conformal Pt film formation into those undercut and notched areas down the length of the TSV.

Chapter 2: Copper Electrodeposition in Mesoscale Interconnects - Fundamentals and Challenges

2.1 Introduction

Copper electrodeposition has been studied extensively over the last century[16, 17], and the kinetic mechanism by which the reduction of copper ions in a sulfate acid chemistry occurs is well established. A sketch of a Cu ECD process is shown in Figure 8 below.

In Figure 8, one can see that in electrolytic ECD cell, the working electrode or cathode is the workpiece to be plated and is connected to a negative power source, while the counter electrode or anode is connected to the positive terminal of the power source. Power sources commonly used for ECD vary greatly in complexity, from simple DC power sources to complex programmable pulse power sources controlled by external software. Non-replenishing chemistries use anodes that consist of inert metals like platinum or platinized titanium, and these baths are manually replenished with copper as they age over time. In contrast, the most common copper plating chemistries rely on a solid Cu anode that replenishes the chemistry with copper as deposition occurs, keeping an equilibrium saturation of Cu in solution. The Cu

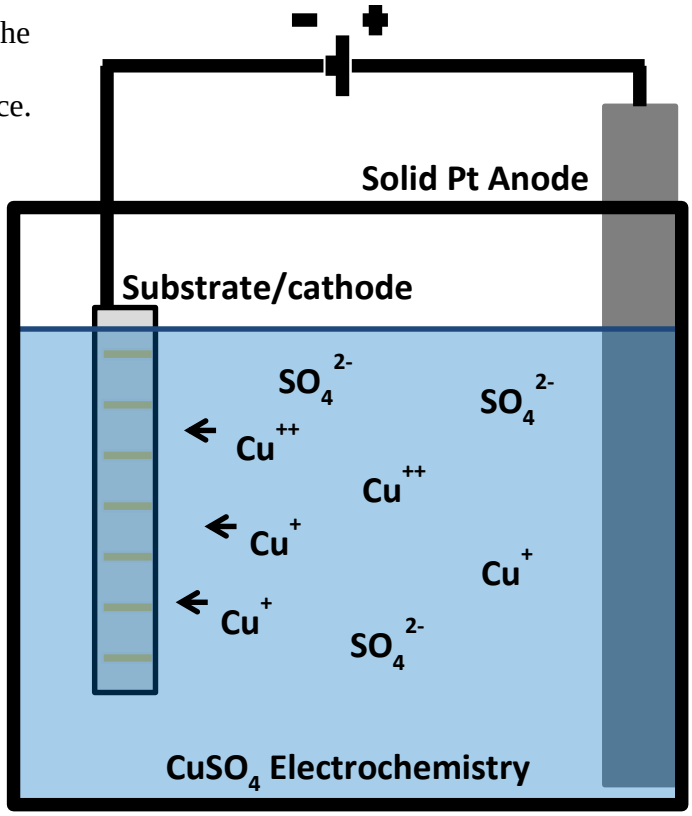


Figure 8: Schematic of simple Cu ECD cell

content is dependent on acid concentration and on the type of acid used in the aqueous solution. A reference electrode is not shown in Figure 8, as they are not commonly utilized in industrial plating tanks relying on galvanostatic control, but reference electrodes are used in R&D environments typically or any situation when high resolution potentiostatic control is desired. For clarity, the additive-free chemical set commonly utilized for acid sulfate Cu ECD chemistries is shown in Table 2.

Additive-free Acid Sulfate Copper Electrolyte			
Constituent	**Form**	Concentration	**Purpose**
Copper Sulfate Pentahydrate	Solid (salt)	1-1.3 M	Metal ion source
Sulfuric Acid Or Methane Sulfonic Acid	Liquid	0.25-1.0 M	Cu reduction & bath stability aid
Sodium Chloride Or Hydrochloric Acid	Solid (salt) Or Liquid	50-100 ppm	Complexing agent for additives

Table 2: Typical Cu acid sulfate electrolyte components

Table 2 shows the acid sulfate Cu electrolyte bath components and their typical respective concentrations and purposes. The Cu that is ultimately deposited on the working electrode surface is dissolved into a DI water/acid solution. This Cu comes in the form of a cupric sulfate salt, which readily dissolves into highly acidic solutions. Sulfuric and methane sulfonic acid both improve bath stability. These two acids prevent Cu from reacting with oxygen, allow for an energetically favorable Cu reduction, improve film quality, and improve bath stability. The NaCl or HCl serves as a source of Cl^- ions, which competitively complex with inhibitor and catalyst additive molecules when they are added to the electrolyte. This Cl^- source is sometimes considered an 'additive', although when existing alone in an electrolyte without any other additives it

doesn't have a significant effect on plating conformality, grain size, or other film quality measurements.

2.2 Reaction Kinetics and Additives in Copper Electrodeposition

The two fundamental copper reduction steps are shown in Equation 2 and 3 below.

$$Cu^{++} + e^{-} \rightarrow Cu^{+} \qquad (2)$$

$$Cu^{+} + e^{-} \rightarrow Cu \qquad (3)$$

Equation 1 above is the rate limiting step of this mechanism. Most importantly, the Cu^{+} intermediate can readily complex with various additives, which is of particular importance when attempting to achieve superconformal Cu growth or refined grain structures on planar surfaces. This Cu^{+} intermediate is solvated in the aqueous chemistry, and because the first step has been shown to have a kinetic rate constant three orders of magnitude smaller than that of the second reduction step,[6] sufficient time and chemical potential exists for competitive adsorption and desorption to occur, which is advantageous in interconnect ECD for several important reasons discussed below.

The purpose of the specific additives in Cu TSV ECD are discussed in Section 2.2.1, but there are a few simple tenets that these additives follow. First, each of the additives rely on the presence of chloride within the bath to competitively adsorb and desorb at the Cu reduction interface. Second, the additives fall under one of two main types; a suppressor (or inhibitor), which serves as a passivating or blocking layer against full Cu reduction onto the electrode and; second, an accelerator (or Cu reduction catalyst) which increases the plating rate particularly in recessed areas, thus smoothing the plated Cu and improving overall conformality.

The chemistry used in this work consists of a copper sulfate solution with either sulfuric acid (H2SO4) or methane sulfonic acid (MSA) as the electrolyte. This baseline solution, or makeup chemistry, is typically modified through the use of a three or four-additive system, in order to manipulate and control the grain size, surface roughness, and deposition rate of electrodeposited copper. These four additives are described below:

Accelerator - Surfactant molecule that adsorbs on the surface and, by coverage increase with area loss, preferentially increases the plating rate as a function of surface coverage which is desired for filling the concave bottom of a given high aspect ratio feature

Suppressor - Large chain polymer (1k-20k mW) which inhibits deposition. When a concentration gradient is achieved throughout the depth of the feature this additive can be used to create a gradient in the deposition rate throughout the depth of the feature (slower deposition higher in via where there is a larger concentration of suppressor molecules).

Leveler - Competes with the accelerator, disabling it at convex surfaces and is commonly used to reduce overburden thickness when filling features; also behaves as a grain refiner.

Chloride - Competitively complexes with suppressor and accelerator species at the surface of the cathode and is required for the suppressor to function.

The specific accelerator, suppressor, and leveler species shown in Figure 9 are not the only species that can be used for their described purposes, but the named species have been the most widely and consistently used in industry.

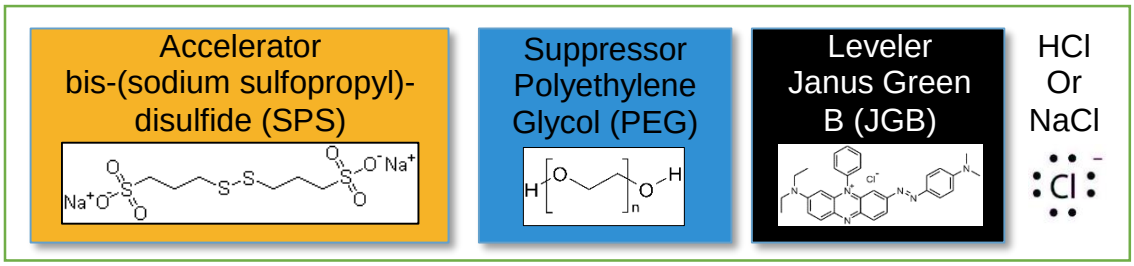


Figure 9: Molecular structures of common additives in Cu electroplating

For Cu suppression to be effective, a tuned polyether species, like PEG is a common constituent, for accelerated Cu deposition, SPS is common for Cu reduction catalysis, and JGB, a nitrogen-containing dye species, is common for leveling. The 'leveler' species can be left out, however, as the suppressor, accelerator, and chloride species have been shown to be sufficient for highly refined, conformal Cu.[6, 18-23] The common concentrations of SPS, PEG, and Cl^- in an acid sulfate electrolyte are shown in Table 3.[6, 19]

Component	Concentration
NaCl	1.0 mmol/L
PEG (MW 3,000)	100 µmol/L
SPS	0-500 µmol/L

Table 3: Typical additive concentrations in Cl- PEG-SPS electrolyte

The additives in Table 3 produce a distinct kinetic change in an acid sulfate electrolyte. Equations 3 and 4 encapsulate the change in current with respect to the surface coverage of SPS (θ_{SPS}), overpotential (η), copper concentration at the surface (C_{Cu}^{++}), bulk copper concentration ($C^{bulk}{}_{Cu}^{++}$), PEG kinetic coefficient (k_{PEG}), SPS kinetic coefficient (k_{SPS}), exchange current density (i^0) for the rate determining, ($Cu^{++} + e^- \rightarrow Cu^+$) step, transfer coefficient (α_{SPS} and α_{PEG}), Faraday's constant (F), the gas constant (R), and the temperature (T).

$$i(\theta_{SPS}, \eta) = \frac{C_{Cu^{++}}}{C^{\infty}_{Cu^{++}}}\left[k_{PEG}(1-\theta_{SPS}) + k_{SPS}\theta_{SPS}\right] \quad (4)$$

$$k_j = \exp\left(\frac{-\alpha_j F \eta}{RT}\right) - \exp\left(\frac{(1-\alpha_j) F \eta}{RT}\right) \quad (5)$$

From Equations 4-5, one can see that SPS and PEG are extremely influential as to the

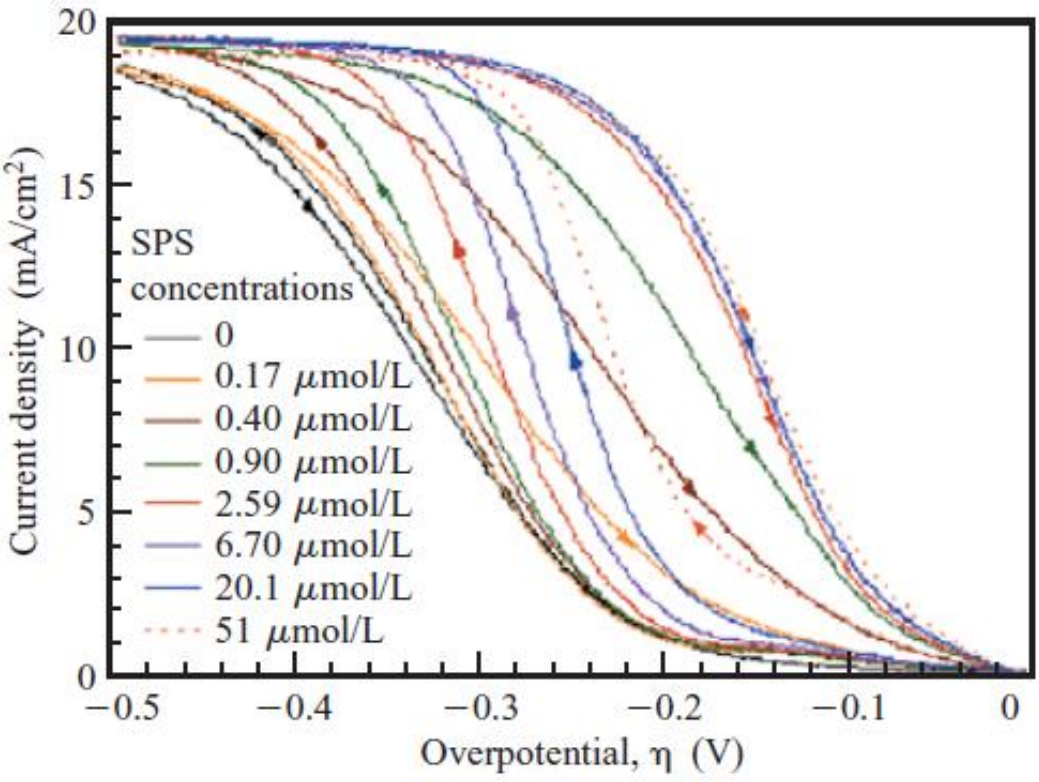


Figure 10: iV curves representative of the desorption of PEG–Cl species by adsorption of SPS at different SPS concentrations onto a planar stationary working electrode[6]

current at a given overpotential, and one example of these equations in action can be seen in Figure 10, where sweeping across negative overpotentials on a planar electrode were conducted at a PEG concentration of 88 µmol/L and chloride concentration of 1 mmol/L of NaCl in a 0.24 mol/L $CuSO_4$ and 1.8 mol/L H_2SO_4 electrolyte. From these curves, one observes that as the concentration of catalyzing SPS increases, the rate at which Cu reduction occurs during the reductive sweep also increases. At the 2.59 µmol/L SPS concentration, the electrode becomes saturated with SPS, so the positive sweep is almost identical at each subsequent increase in SPS concentration. This feature shows that there is a limiting amount of these additives, and that is the point where the electrode is fully saturated with one component or the other, and the effective surface coverage is equal to

1. This clear representation of the competitive adsorption/desorption dynamic at play in a Cl-SPS-PEG electrolyte allows for the curvature-enhanced-accelerator-coverage (CEAC) mechanism to be understood in Section 2.2.1.[6]

In addition to improving the fill profile of high aspect ratio features, these additives are also used to modify the grain size and surface roughness of the plated film. A demonstration of the affect of additives on surface roughness is shown in Figure 11. In general, proper concentrations of suppressor, leveler, and accelerator are used to optimize the electroplated Cu quality, which can be measured in terms of a simple visual inspection and through the use of various surface characterization methods. In particular, atomic force microscopy (AFM) or simple surface profilometry can be implemented to develop a comparison between the plated Cu from different chemistries. By keeping the plating parameters constant between samples while modifying the additive concentrations, one can hone in on the optimal concentration of each constituent. This was conducted in Figure 11, although only a non-additive containing electrolyte was compared with an electrolyte with the supplier reccomended concentration of the additive components of this Intervia 8502 formulation. As one can see in Figure 11, the traditional Cu ECD additives have an enormous impact on the quality of electrodeposited Cu even on planar substrates. In Figure 11 a), the quality of electroplated Cu without any of the additives descibed above is particularly poor in that it is non-uniform in thickness and matte in its coloration. As shown in Figure 11 a), the center-to-edge uniformity difference across the wafer varies from 8% - 100%, depending on the particular sample. In addition, in Figure 11 c), the surface roughness across the sample is significant, as the thickness of plated Cu varies by up to about 0.5 μm within 1 μm of lateral distance across

the wafer. This compares poorly to Figure 11 b) and c), where the Cu quality from the additive-containing bath is bright, uniform (< 5% center-edge uniformity variation), and

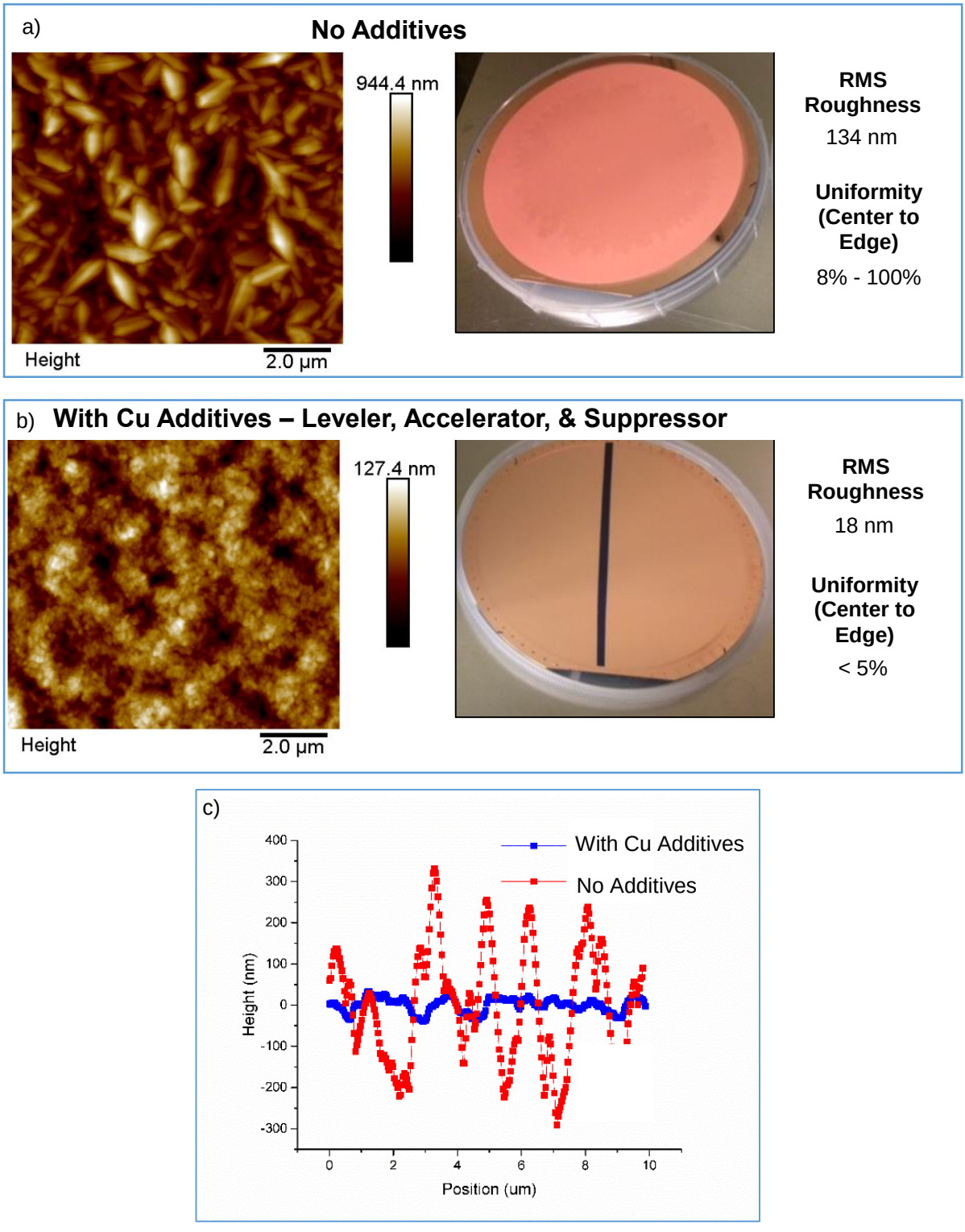


Figure 11: a) AFM and optical image of Cu ECD using additive-free electrolyte b) AFM and optical image of Cu ECD result using three-additive electrolyte c) Underlying AFM data comparing wafers shown in a) and b)

smooth (< 100 nm thickness varaition per µm).

This presents a clear example of the benefits of utilizing traditional Cu ECD additives, as a combination of these additives are necesarry to achieve a void free Cu fill in TSVs from a conformal seed metal, and the additives greatly improve the quality of the plated Cu.

2.2.1 Traditional Acid Sulfate Additives and the Curvature-Enhanced Accelerator Coverage (CEAC) Mechanism

In order to achieve a void-free fill in high aspect ratio features, the filling profile must

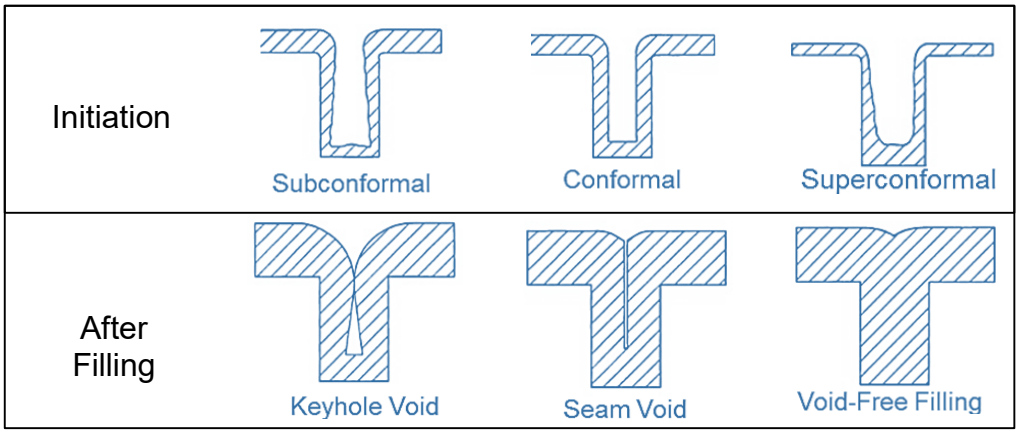


Figure 12: Common fill profiles in vias or trenches. Superconformal initiation typically results in void-free filling when vias are finished with the ECD process[3]

evolve 'superconformally'. The different fill profile possibilities are shown in Figure 12.[3] As shown in Figure 12 the certain method for achieving superfilled features is to initialize deposition more rapidly at the bottom corners of the features in order to prevent seam or keyhole voids as shown in the figure above, which result from conformal and subconformal plating, respectively. There are other methods for achieving fully filled, void-free features and these are as discussed at length in Chapter 5.

The additives discussed above have a specific method of interacting with one another, which is presented in Figure 13. In Figure 13 a), the Cu reduction catalyst (accelerator)

species adsorb or float above the concave surface near via bottom as the large chain polymer (suppressor) species establish a Cu reduction blocking gradient beginning at the convex via entrance and down the via sidewalls. In Figure 13 b), rapid area change continues to improve plating superconformality as the more strongly adsorbed accelerator species catalyze Cu reduction at highly concave surfaces until Figure 13 c) when the via is almost fully filled with Cu at the via entrance as accelerated deposition in concave areas continue. Next, in Figure 13 d), the plating 'momentum' leads to initial overburden growth above the via entrance and then in Figure 13 e), Cu reduction continues as accelerator species is ejected from convex surfaces. Next, in Figure 13 f), the accelerator species is replaced with leveler species prior to Figure 13 g), when polymeric suppressor species readsorb to the convex via entrance and large planar surface on field, severely slowing or halting plating entirely at these locations and thus reducing the overburden thickness.

2.3 Transport Phenomena in Blind Mesoscale Through-Silicon-Vias

The transport phenomena parameters within an aqueous electrolyte are enormously important as to the availability of the different bath constituents within the electrolyte. Typical boundary layer thicknesses have recently been estimated to exist at values from10 μm[1, 24] - 150 μm[25] in a typical ECD system. This obviously depends entirely on the convection mechanism, whether that be by rotation of the electrode, movement of the fluid, or a combination of the two, as is common to 'fountain plating' techniques utilized commonly in the semiconductor manufacturing industry. Fountain plating is a technique wherein fluid is pumped towards the sample and the sample is rotated in a manner to ensure a uniform boundary layer thickness across the wafer is

achieved. In Chapter 5, a lengthy discussion of the importance of the boundary layer thickness on diffusing Cu and a polyether additive is presented. In Table 4, diffusion coefficients for the two additives are provided.[1]

Using the information in Table 4 and inserting these coefficients along with the via depth (z), and boundary layer thickness (δ), one can determine the amount of time required for

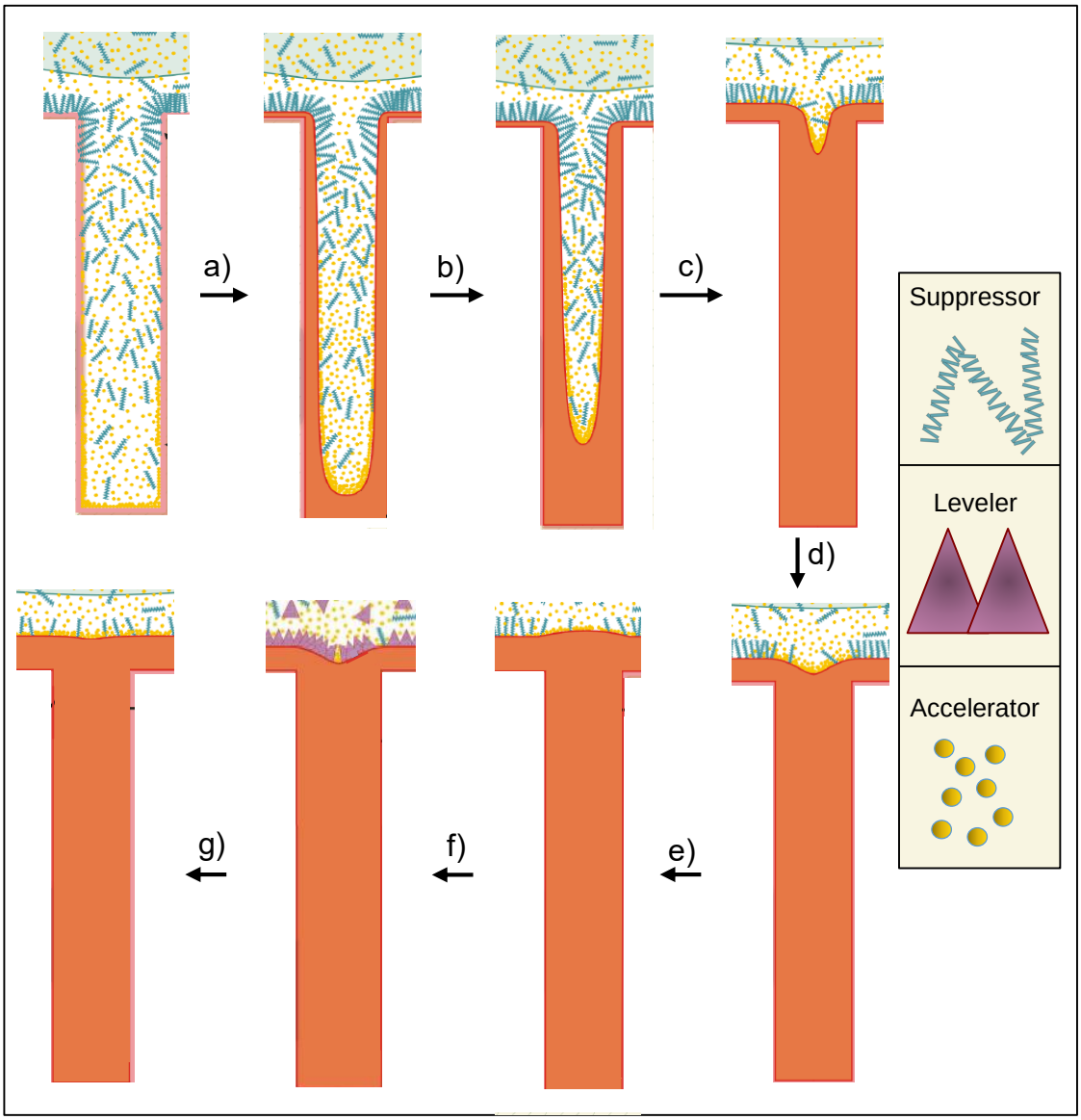


Figure 13: a)Initiation of superconformal CEAC growth front propagation where Cu reduction catalyst (accelerator) species adsorb or float above concave surface near via bottom b) Rapid area change continues to improve plating superconformality c)Via is almost fully filled with Cu at the via entrance d)Plating momentum leads to initial overburden growth e) Cu reduction continues as accelerator species is ejected and f)Replaced with leveler species prior to g) Suppressor species adsorbing to large planar surface on field including above via entrance, severely slowing plating rate

Component	Reported Diffusion Coefficient (μm²/sec)
PEG (MW 1k - 10k)	50
SPS	1000

Table 4: Typical diffusion coefficients of suppressor (PEG) and accelerator (SPS) in acid sulfate electrolytes

a particular additive to diffuse through the boundary layer and adsorb onto the electrode surface. One can also determine the amount of time required for diffusion and adsorption to occur for a given species in these 600 μm deep features, estimating the boundary layer thickness to be 100 μm.[1]

$$\tau_{Diffusion} = \frac{(z+\delta)}{D_s} \qquad (6)$$

From Equation 6, the time required for diffusion of the SPS and PEG molecules to the bottom of the mesoscale TSV discussed herein are 14 and 0.7 seconds, respectively. This would help to explain the presence of the Cu reducing SPS species in the via bottoms rather than the PEG molecules, as they win the 'race' to the bottom surface and are strongly adsorbed to sufficiently prevent themselves from being desorbed by competing polyether suppressor molecules from the electrode surface at the via bottoms.

Chapter 3: Sample Preparation, Experimental Methods, and Characterization for Through-Silicon-Via Electrodeposition

3.1 Introduction

The work discussed herein required a great deal of hands-on laboratory work, where much of the experimentation relied on novel approaches and design of custom apparatuses for each of the required steps involved plating in these features. The aim of this chapter is to clearly present the intricacies behind each of the techniques involved in the ECD process and these techniques have on the Cu conformality throughout the depth of the via. In addition, this chapter focuses on the intricacies behind each of the steps of the experiment including sample preparation to wet the electrolyte down the entire TSV, plate in the via, and characterize the plated film.

3.2 Planar Cyclic Voltammetry with Rotating Disk Electrode Apparatus

One of the most important fundamental tools in any electrochemistry laboratory is a rotating disk electrode (RDE) or rotating ring disk electrode (RRDE) apparatus. For the work discussed here, a Pine Research MSR RDE tool was utilized. This piece of equipment consists of a rotating shaft, the speed of which is controlled externally by the user in order to modify the convection contribution to the ECD process. In addition, a planar Pt working electrode along with a Pt wire counter electrode and a Hg/Hg_2SO_4, K_2SO_4 (sat) reference electrode was used. The sulfate-based reference was used to be consistent with the sulfate electrolyte and mitigate any leached contamination from the electrode. For instance, if a chloride-based reference electrode like Ag/AgCl was used

there would a concern for Cl leaching into the base electrolyte and changing the concentration of Cl in the solution modifying the analysis of the effects of different

Figure 14 a) Controller for managing to rotation speed of the b) Planar Pt working electrode countered by c) The Pt wire counter electrode adjacent e) The mercury/murcurous sulfate reference electrode which is a part of d) the combined Pine RDE apparatus[4]

additive concentrations. In acid sulfate Cu ECD, chloride concentration fluctuations as small as ppm can lead to large changes in plating rates and quality, so the sulfate

reference is optimal to mitigate this issue. The RDE apparatus used in this work is shown in Figure 14.[4]

A Biologic SP-200 potentiostat was used to control and monitor the applied current and potential during the RDE experiments. This instrument is ideal for highly sensitive current, voltage, frequency, and duty cycle control, particularly like the process outlined in Chapter 5 to follow. By using an RDE/three electrode/potentiostat setup, I was able to achieve precise control the fluid flow across a planar working electrode while also carefully controlling and monitoring the electrochemical kinetics and metallization process in both anodic and cathodic regimes.

3.3 TSV Wetting

Prior to electrodeposition of any high aspect ratio feature, the first obstacle to overcome is ensuring the features are properly wet with fluid as opposed to trapping air pockets in the feature preventing deposition. Wetting a surface or a feature is directly related to the hydrophobicity or hydrophilicity of the surface, as well as the fluid properties, such as the viscosity and diffusivity, of the ECD electrolyte. One common method of determining the

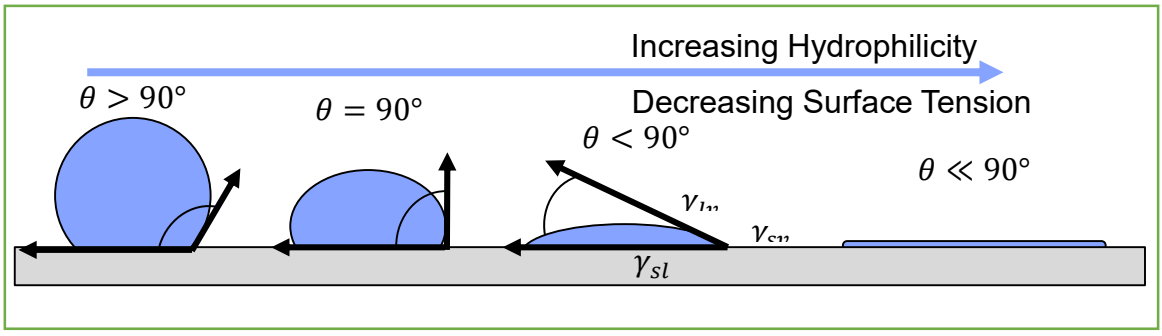


Figure 15: Sketch showing water droplet contact angle experimental technique for determining substrate hydrophilicity

wettability of a particular substrate is to examine the contact angle between a water droplet and a planar surface made of the same material as that of the feature surface.[26]

An illustration showing how the angle of the water droplet with respect to the surface is related to the surface tension and that fluid and thereby the hydrophilicity of the surface is shown in Figure 15. Equation 7 presents the underlying equation presented in Figure 15, where γ_{lv}, γ_{sv}, γ_{sl} represent the liquid-vapor, solid-vapor, solid-liquid interfacial tensions, respectively.

$$\gamma_{lv}cos\theta = \gamma_{sv} - \gamma_{sl} \qquad (7)$$

Typically, a goniometer is used to image the water droplet on the surface and measure the corresponding angle. In this work, a variable angle Keyence VHX-6000 optical microscope was utilized to image the water droplet at 90 degrees with respect to the

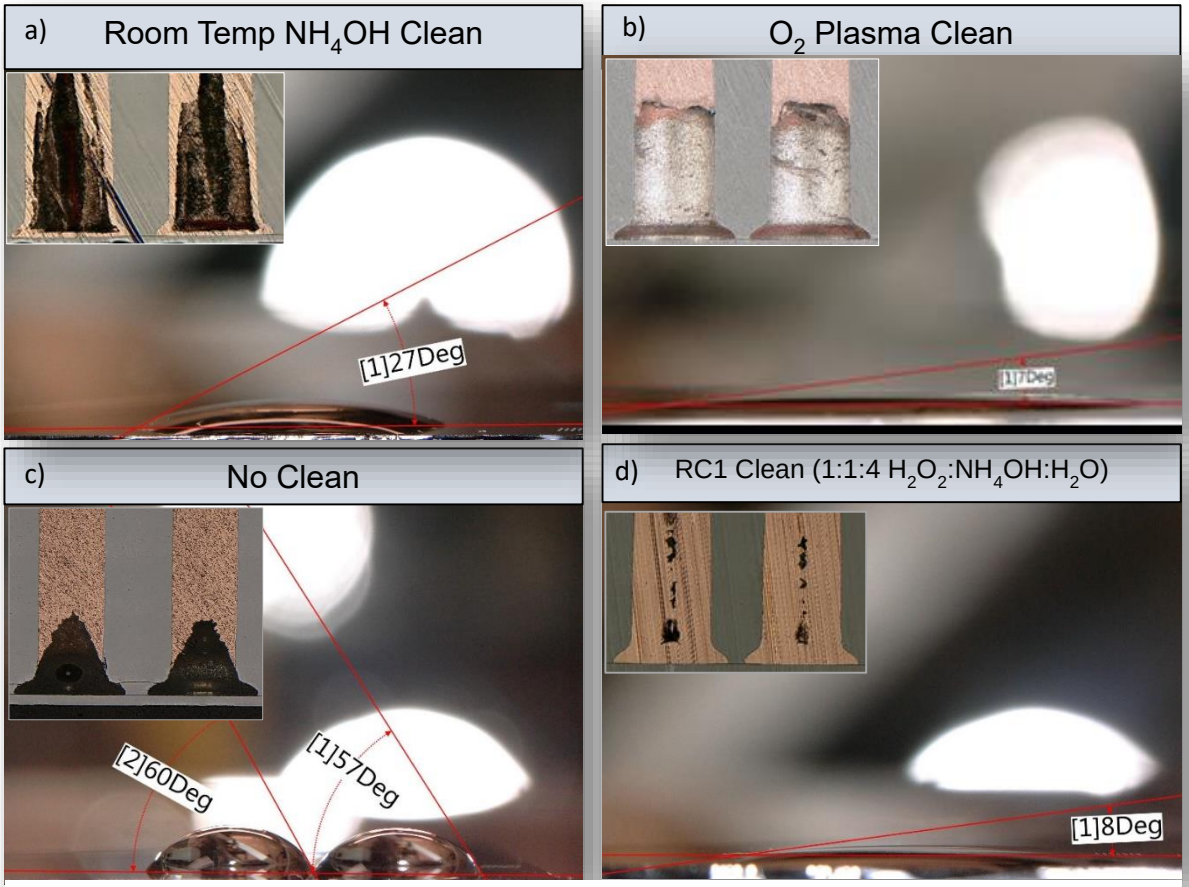


Figure 16: a) Ammonium hydroxide clean effect on planar DI water wetting b) Oxygen plasma clean effect on planar DI water wetting c) Wetting without any Pt substrate preparation d) Aggressive RC1 clean effect on substrate wetting

sample and the measurement software on the digital microscope was used to measure the angle between the surface of the sample and the line tangle to the edge of the water droplet. There are a few degrees of error in the angle measurement but this technique was used qualitatively to determine which sample preparation technique rendered the surf surface the most hydrophilic. The technique discussed above was utilized along with various substrate preparation or cleaning techniques to determine the optimal method for achieving full wetting of the ECD electrolyte. The results of these experiments are presented in Figure 16.

The seed metal used for plating in these vias is an ALD Pt film. Pt has a high affinity to collecting carbon which renders the surface hydrophobic.[27] Once the carbon is removed the surface becomes hydrophilic. Figure 16 a) shows a plating result where full depth via wetting was achieved, although the wetting angle for that ammonium hydroxide clean was relatively large to the angles measured in Figure 16 (c) and Figure 16 (d) the 20 degree measurement is still relatively low compared to the 60 degree measured found when no clean was used, shown in Figure 16 (c). Figure 16 b) shows the wetting angle and ECD result, where a very small contact angle was measured. measured. In this experiment wetting did not occur approximately half way down the via but it is believed that this is a result of the plasma clean not reaching that far down the vias and therefore not improving the hydrophilicity of the sidewall of the via halfway down the feature. Figure 16 c) and d) clearly show a correlation between the contact angle and the ability to fully wet the feature with a large contact angle corresponding to no wetting at the via bottom and a small contact angle, for the aggressive RC1 clean, corresponding to full

depth wetting. In this work, the RC1 clean was most frequently utilized, as this method provided consistent full depth wetting of the ECD electrolyte.

In contrast to the approach discussed above, another way to consider this via wetting issue is outlined in the sketch in Figure 17. This figure, alongside equation 6, illustrates the importance of the external pressure, p_0, surface tension (σ) and via radius (R) on the pressure of trapped air pockets within the via, which must not exist if full wetting is to occur. So, by utilizing a vacuum system and a low surface tension wetting agent like ethanol, via wetting may be possible without having to rely on a corrosive cleaning agent like the RC1 discussed above.[28]

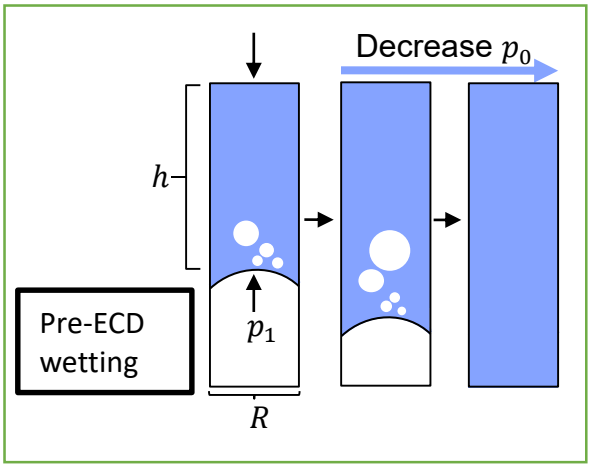


Figure 17: Sketch representing via wetting issue

$$P_1 = P_0 + \rho g h + \sigma\left[\frac{1}{R} + \frac{1}{R}\right] \quad (8)$$

For full via wetting to occur, $P_1 > P_0 + \sigma\left[\frac{1}{R} + \frac{1}{R}\right]$. This can be accomplished by decreasing external pressure or fluid temperature. In addition, there is some notion that the trapped air pockets can be sufficiently shrunk to allow for full wetting the occur by *increasing* the external pressure. Essentially, the entire issue is governed by the ideal gas law, and manipulating the temperature and pressure within the vias can be used to achieve full wetting. Another method for

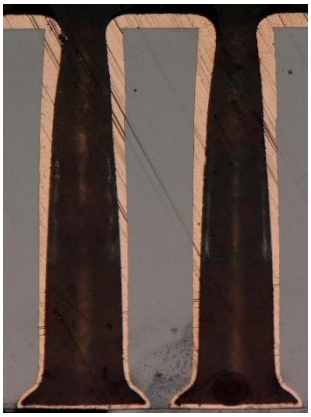


Figure 18: EtOH Pre-Wet Result in 50 µm SPS, 100 µm PEG 3.45k, 1 mM NaCl, 1 M H_2SO_4, at 2.5 mA/cm² for 6 hours

achieving full via wetting is presented in Figure 18, where EtOH was used under vacuum, followed by a water rinse and a quick submersion into the electrolyte. In this figure, one can see that there is indeed full via wetting that occurs, as the Cu in both of the via bottoms in Figure 18 shows.

3.4 Electrodeposition Setup

3.4.1 Beaker-Scale RDE Experiments

In Chapter 5, a novel technique is discussed for filling these mesoscale TSVs with Cu from the bottom-up. With this technique, there is a great deal of importance on the boundary layer thickness above the TSVs, as this technique relies on a finely tuned concentration gradient of polyether suppressor and chloride to complex and passivate the

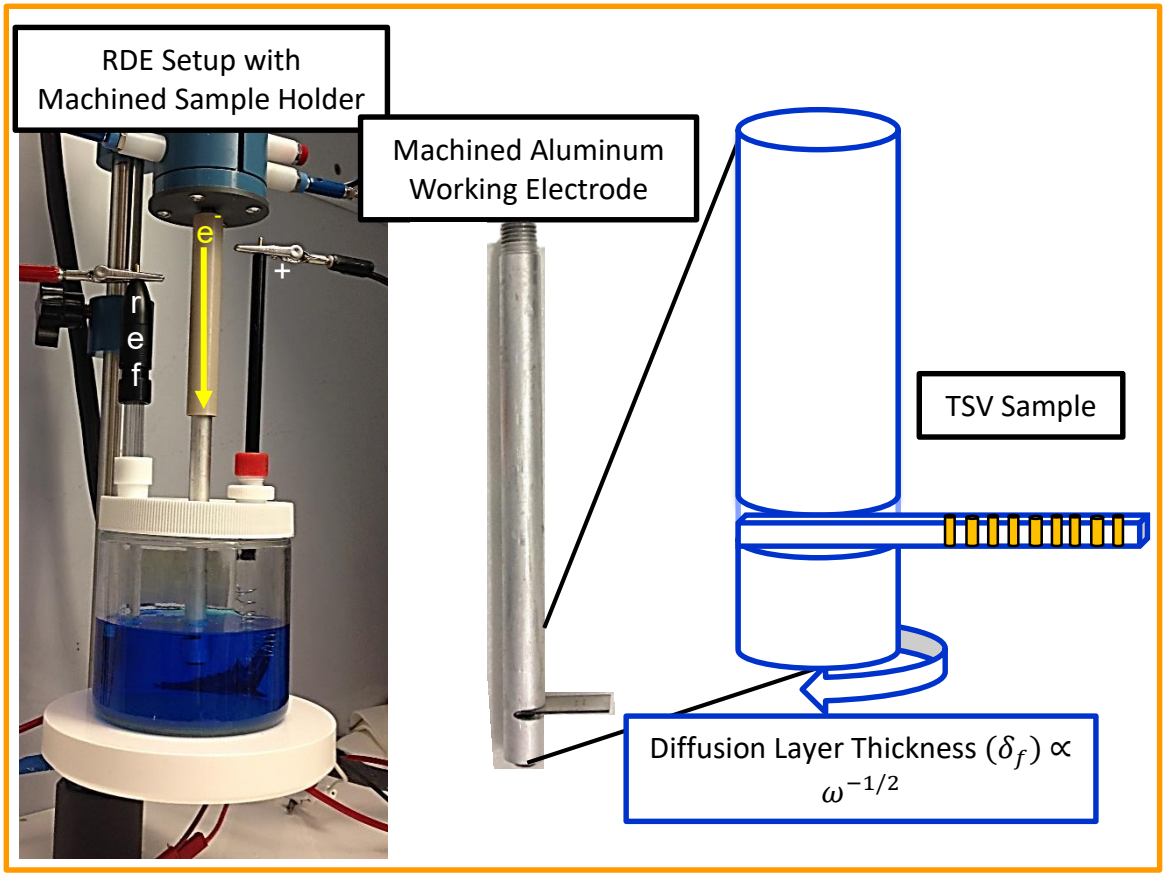


Figure 19: RDE setup with machined aluminum rotating sample holder for controlled boundary layer thickness

electrode surface everywhere other than the TSV bottom. The ECD process for researching this technique relied on an innovative plating setup, shown in Figure 19.

As shown in Figure 19, this setup relied on a rotating working electrode connection rod in order to establish a boundary layer thickness of a known height. The goal of this apparatus was to obtain laminar flow consistently across the TSVs on the sample. This is

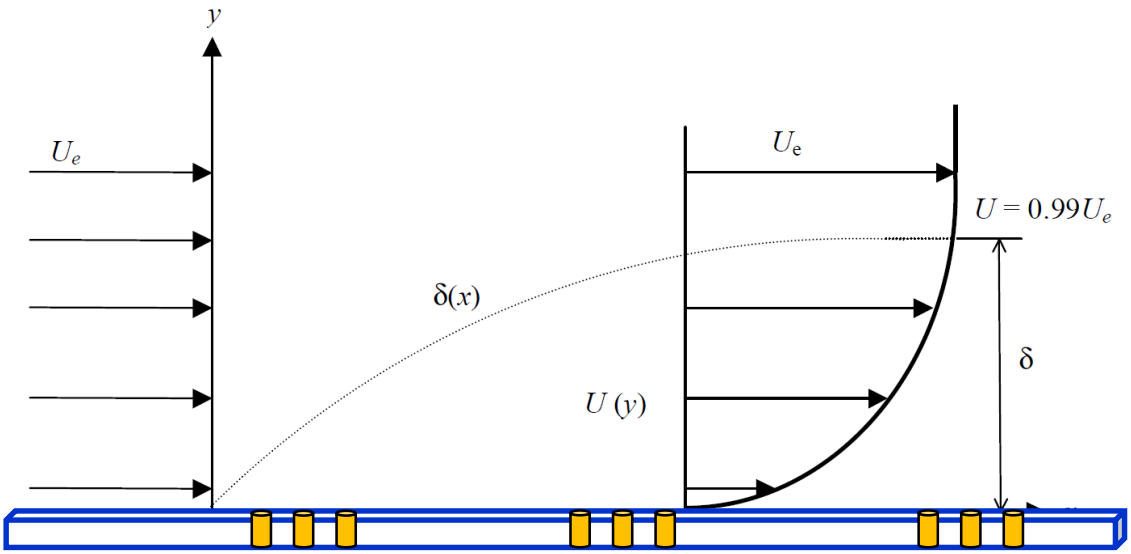


Figure 20: Diagram showing the fluid flow and boundary layer profile across a planar substrate for laminar flow[2]

not a trivial feat however, and the fluid dynamics of laminar flow over a flat plate are presented in Figure 20.

Using Figure 20, one can determine the boundary layer thickness across a sample using a few simple parameters as shown in Equation 9.[29]

$$\delta = \sqrt{\frac{\nu x}{u}} \qquad (9)$$

Where the kinematic viscosity of the chemistry (ν) is slightly greater than that of water at $1.1 \cdot 10^{-6}$ m^2/sec, x is the distance across the sample in the direction of fluid flow, and u is the linear velocity of the fluid. Although the sample is rotating in this case, rather than the fluid being pushed across it, this is analogous to the fluid moving, so the equation above

is appropriate. In order to determine the linear velocity of the fluid, Equation 10 was used.

$$u = 2\pi r \omega_{cyc} \qquad (10)$$

Where r is the radius of rotation from the axis to the set of vias (this is approximately 1 inch or 2.54 centimeters), and ω_{cyc} is the rotation rate (rotations per unit time). So, by solving for the linear speed using Equation 11 and inserting this value into Equation 10, one can determine the boundary layer thickness at any point (x) along the sample. Because these vias are spaced apart at differing intervals, it is of significant importance to determine the average boundary layer thickness, as well as to have an understanding of the rate of change in boundary layer thickness across the sample. To determine the average boundary layer thickness, one must integrate Equation 9 and divide it by the distance (x) in the fashion shown in Equation 11.

$$\delta_{avg} = \frac{1}{x}\sqrt{\frac{\nu}{u}}\int_0^x \sqrt{x}dx \qquad (11)$$

The resulting boundary layer thicknesses for a range of sample rotation rates are shown in Table 5.

ω_{cyc} (rpm)	5	25	50	100	200	400
ν (cm/sec)	1.3	6.6	13.3	26.6	53.2	106.4
Re_{avg}	76.8	383.9	767.7	1535.5	3071.0	6141.9
$\delta_{x=0.1L}$ (μm)	324.1	144.9	102.5	72.5	51.2	36.2
$\delta_{x=0.5L}$ (μm)	724.7	324.1	229.2	162.1	114.6	81.0
$\delta_{x=0.9L}$ (μm)	972.3	434.8	307.5	217.4	153.7	108.7
$\delta_{integral\ avg}$ (μm)	**683.3**	**305.6**	**216.1**	**152.8**	**108.0**	**76.4**

Table 5: Boundary layer thicknesses at various rotation rates for S-NDR approach discussed in Chapter 5

From Table 5, one can see that the boundary layer thicknesses are on the order of the length of the TSVs, which is generally a common theme in Cu TSV or trench filling. Another thing to note here is that the boundary layer thickness varies (from x = 0.1L to x = 0.9L) by about the same amount as the integral average thickness. So, to improve uniformity across a sample, higher rotation rates are desirable. However, rotating the sample at a high rate may cause other issues, as discussed in Chapter 5.

3.4.2 Large Plating Tank

Our electroplating bath has an overall footprint of 18" x 24". It is small enough to be fitted into common depth fume hoods, but large enough to accommodate 6" wafers with moderate throughput before requiring replenishment. The main component of this bath is the reservoir constructed from 3/8" thick PVDF material. Figure 21 shows a side view of the tank. The lid is angled to allow condensed water from evaporation to flow back into the solution during heated plating experiments. This significantly reduces evaporative losses and maintains the appropriate liquid level in the tank. For Cu ECD however, evaporative loss is not of great concern as acid sulfate Cu electrolytes are generally operated at room temperature. The lid on the tank incorporates a quartz window for quick inspections during operation to ensure the liquid level and fluid flow are maintained during operation. The backside of the tank has seven sealed utility ports; one fluid input and output port, four heaters ports, and a small thermocouple port. All plumbing into or out of the bath is run above the standard liquid level to

Figure 21: Side view of custom built electroplating bath reservoir showing graded lid, process viewing window and backside location for fluid input, output, thermocouple and heaters.

eliminate potential leak points. The input and output ports are recessed below the graded lid and are not visible when looking directly at the bath during operation. The fluid input port connects directly into an angled diffuser located in the half hexagonal backside region of the bath. The diffuser is designed to dampen the flow across the heaters and angularly guide the solution over the front side of the working area on one side as well as the front side of the anode simultaneously. The four heaters are 110V Process Technology "V" series connected in pairs to JBN-Duraline quick disconnect industrial/commercial grade waterproof connections, 3MT-20 and 3FT-20. The heaters are controlled by Omega 9001 controllers connected to GFCI protected bench power. To monitor bath operating temperature we use Omega "T" type thermocouples which are coupled into the Omega controllers. The bath has locating groves for the anode and plating fixture to provide fixed locations for repeatability. The anode can be mesh, metal slugs metal sheets. In our set up we use a platinized titanium basket filled with solid Cu slugs. Circulation is provided by Levitronix BPS-200 magnetic levitating centrifugal pump. The fluid lines and fittings are COTS Entegris fluid handling equipment and the filter is a Pall Polypure capsule which filters contaminants larger than 1 µm without interrupting circulation. This filtration is particularly important when plating into photoresist molds which introduce carbon contamination to the chemistry.

3.5 Sample Cross-Sectioning, Polishing, and Microscopy

3.5.1 Scribe and Break Metrology

Initial experimental results relied on 'cleaving' into via samples with the goal of cleaving the sample directly through the middle of rows of vias. However, this method proved to be inaccurate and unreliable as the Cu often did not break down the center but instead the Si cracked and broke around the plated Cu. An example of a cleaved sample is shown in Figure 22. From this figure, orange colored areas are Cu, the green areas are Al_2O_3, and the silver areas are Pt.

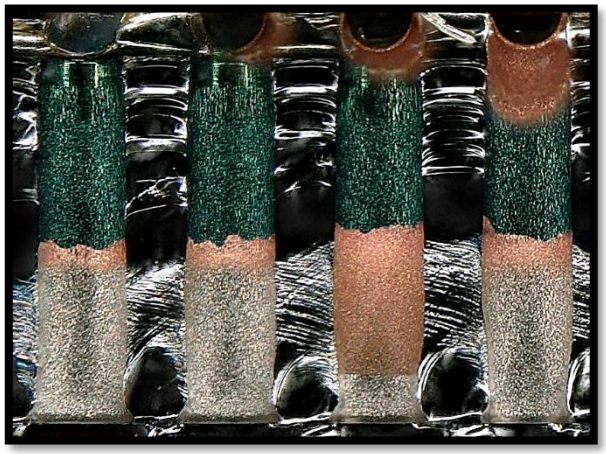


Figure 22: Result of scribe and break metrology

When cleaving a sample, the Cu was often ripped away from the underlying ALD Pt, and even the Pt was sometimes delaminated from the underlying Al_2O_3 insulating layer. In order to better view the vias after plating, a polishing tool was purchase and technique was developed for repeatable cross-sectioning of these samples. The polishing process is outlined in Section 3.5.2.

3.5.2 Polishing

Because the cleaving method was insufficient, a more repeatable method for viewing plated samples was developed. This cross-sectioning method utilized an Allied High Tech Multiprep™ 8" Polishing System for carefully polishing into the middle of via rows. Prior to polishing, the TSVs were infiltrated with epoxy utilizing both vacuum and

positive pressure chambers, and the samples were sandwiched between two glass slides for further support. An example of this polishing apparatus and fixturing is shown in Figure 23.

In Figure 23, one can see the general setup for polishing into these TSVs. This system

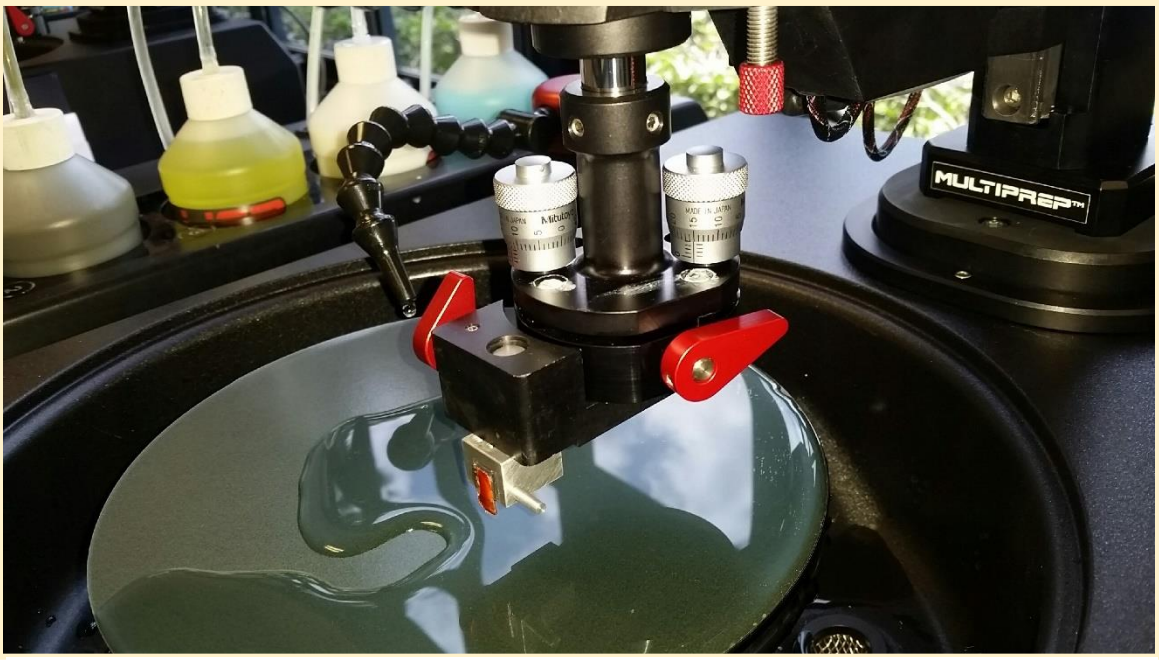


Figure 23: Allied Multiprep™ 8" Polishing system

relies on removable diamond embedded pads ranging from 60 µm to 0.1 µm average impregnated diamond size. This process is typically done by first using a 30 µm high grit film, to polish close (100-200 µm away) to a set of vias, before stepping down in grit size to prevent damage to the vias. Damage from the polishing process is expected to be at 3x of the grit size used so it is important to use a small grit 6 µm – 0.5 µm when inside of the vias and to polish enough to remove at least 3x off the thickness of the previous grit size to remove underlying damage.[30] This system is optimal for achieving scratch-free cross-sectional images of our mesoscale TSVs for subsequent metrology and analysis.

The purpose of infiltrating these features with epoxy and sandwiching between two glass

slides is to provide bulk support of the sample while also preventing the electroplated copper from being smeared or ripped out of the vias if polishing is too aggressive. However, as discussed in Section 3.3, there is an inherent difficulty in forcing any liquid,

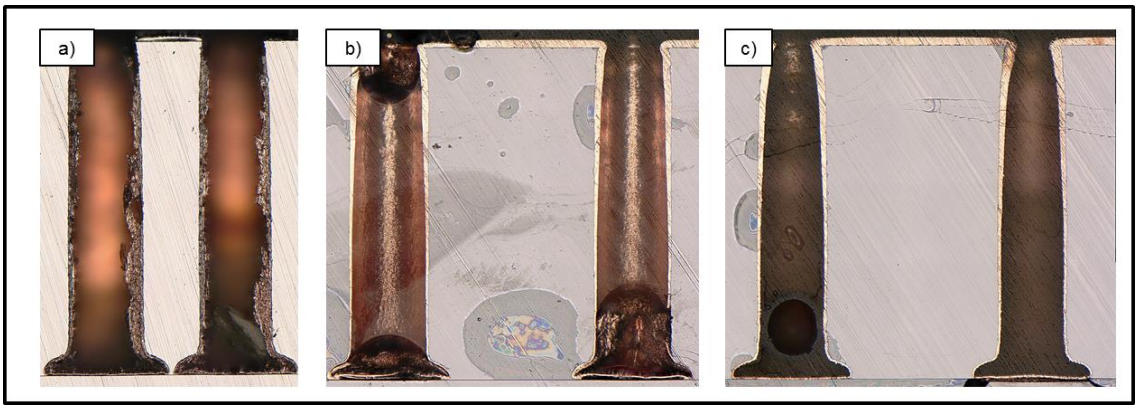


Figure 24: Via samples after ECD, attempted epoxy infiltration and polishing with a) No epoxy infiltration; b) Significant trapped air bubbles near via bottoms harming Cu thickness understanding; c) Full epoxy infiltration with only minor air pockets not affecting polished Cu quality

especially one of significant viscosity, into a high aspect ratio feature. Figure 24 presents examples of incomplete via filling and the result this issue has on the polished result as compared to an example of a fully infiltrated via.

While the method of polishing into these features is clearly much better than the cross-sectioning technique, one can see a few issues that can still arise in Figure 24 above. This information is presented to inform the reader of these issues prior to examining experimental results in sections to follow to clarify ahead of time why some images may appear slightly different than others. As shown in the figure above, the cross sectioning results can be misinterpreted if the epoxy does not adequately infiltrate the via prior to polishing, leading to ambiguity in the plating results. Figure 24 a) has Cu smearing on the sidewall due to a lack of epoxy infiltration, Figure 24 b) has Cu delamination from the via bottom and Figure 24 c) is an example of high quality epoxy filling.

For filling the TSVs with epoxy, mild negative vacuum is pulled at about 10^{-1} torr before pulling in the low viscosity EpoxySet epoxy into the vias, sandwiching between two glass conver slips, and applying 25 psi of positive pressure for 8 hours during the epoxy cure time.

3.5.3 Optical and Scanning Electron Microscopy

For sample preparation, pre and post-plating analysis and general experimental guidance, a Keyence VHX-6000 optical microscope was utilized. This microscope was optimal for the purposes of this work, as this microscope was able to resolve images down to about 1 μm, and distance and angle measurements could be taken within the Keyence interface. This feature was particularly helpful when using the scope to align cross-sectioned samples so as to polish accurately into the center of a given via set.

In addition, for some initial experiments where the exact Cu thickness was measured, scanning electron microscopy was utilized to obtain a more precise Cu thickness measurement down the feature depth. This was not used to great significance, as the optical microscope was able to provide Cu thickness measurements with low enough tolerances to not be of substantial concern.

Chapter 4: Conformal Copper Electrodeposition for Void-Free Through-Silicon-Via Lining

4.1 Introduction

Significant experimentation in this work examined the viability of various ECD plating parameters for conformally plating these features thick enough to accommodate RF voltages at 100V and 100MHz. Improvements in the plated fill profile were made by altering the acid used in the electrolyte, through the use of the two and three additive system discussed in Chapter 2, through modification of the applied potential and current density, and by utilizing 'pulse' plating techniques, rather than DC plating exclusively. The general purpose of this experimentation was to define the optimal Cu ECD chemistry and plating parameters for achieving a conformal Cu fill profile in these mesoscale TSVs. In addition, a stretch goal of this research was to obtain fully filled, void free features, as fully filled features would help to ease the integration scheme for these TSVs downstream from the Cu ECD process.

4.2 Sulfuric Acid vs. Methane Sulfonic Acid

TSV filling has relied mainly on sulfuric acid (H_2SO_4) as the electrolyte constituent for improving $CuSO_4$ dissolution, bath stability, and for use as a Cu reduction aid. The vast majority of proprietary Cu ECD electrolytes designed for high aspect ratio feature filling rely on H_2SO_4. However, these H_2SO_4-containing electrolytes are specifically manufactured for microscale trenches and vias, as

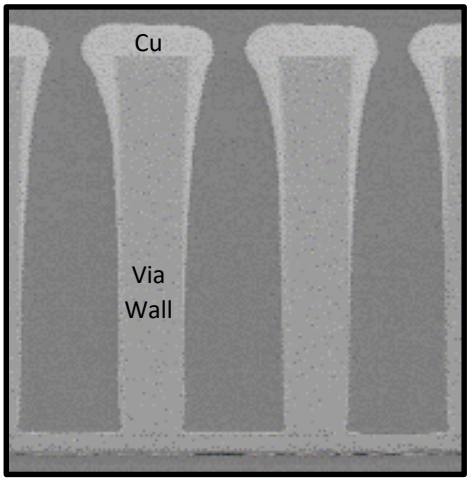


Figure 25: SEM Image of electroplated TSV in proprietary H_2SO_4 electrolyte showing subconformal fill

these size scales are the current industry standard. Mesoscale features are uncommon and have thus not been researched for their ability to be superconformally plated with the typical H_2SO_4 electrolytes. In Figure 25, one can see an SEM of a subconformally plated mesoscale TSV. In the image, the lightest color is the Cu, where it has clearly plated far faster at the via entrance than at the via bottom. This subconformal fill profile is unacceptable, as the Cu will ultimately plate across to the Cu on the adjacent sidewall, thus trapping wet chemistry in large keyhole voids. This image was taken after plating in a proprietary H_2SO_4 electrolyte, which suggested that a large adjustment to the chemistry was required to obtain a conformal or superconformal fill profile thick enough to overcome the skin effect, as discussed in Chapter 1. In order to confirm that the H_2SO_4 electrolyte was the issue, an established chemistry[5] that functioned to superfill microscale features was implemented on these mesoscale TSVs. In Figure 26 a), one can see that the mesoscale full wafer TSVs were subconformally filled using Sun, J.J. Et. Al.'s chemistry while in Figure 26 b) one can see that this chemistry was adequate for the microscale features which are about an order of magnitude more shallow than the mesoscale TSVs. So, in Figure 26, one can see that although Sun, J.J. Et. Al.'s chemistry and plating parameters were sufficient to fully fill features about an order of magnitude

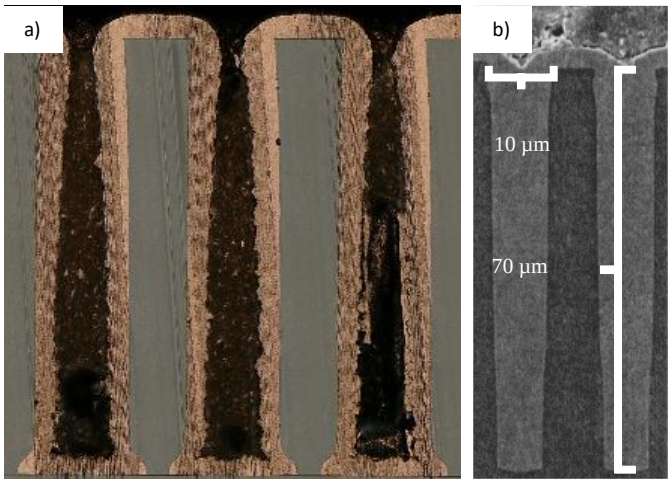


Figure 26: a) Mesoscale TSV and b) Sun, J.J. TSV after Cu ECD in 60 g/L Cu containing, H_2SO_4 electrolyte showing Sun, J.J. Et. Al.'s established method does not translate to the much larger TSVs

smaller that the full-wafer TSVs, this technique was insufficient for fully filling the full-wafer TSVs.

After a literature review, it was understood that methane sulfonic acid (MSA) could be used to replace H_2SO_4 to possibly achieve more optimal results. This was of interest in particular because Cu has a higher solubility in MSA electrolytes compared with H_2SO_4 electrolytes. The higher solubility of Cu in MSA as compared to H_2SO_4 suggests that MSA is the optimal electrolyte for the purpose of filling these TSVs, because more Cu ions available in each via decreases mass transport limited depletion of Cu, leading to increased plating conformality. With more Cu in solution in an MSA electrolyte compared to an H_2SO_4 electrolyte, the propensity for Cu mass transport limited depletion of Cu ions in the via bottoms can be more optimally controlled.[31] This was proven both with a proprietary H_2SO_4 chemistry and with a chemistry and plating parameter set previously used for filling TSVs with a similar aspect ratio.[5] An example of the effect of increased Cu availability down the via depth can be seen in Figure 27. As shown in Figure 27, the availability of Cu ions at the via bottom markedly improves plating conformality, leading to a

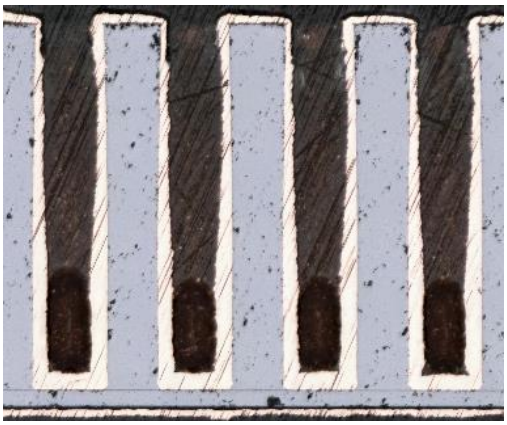


Figure 27: Cu ECD result using 80 g/L Cu electrolyte dissolved in MSA rather than H2SO4

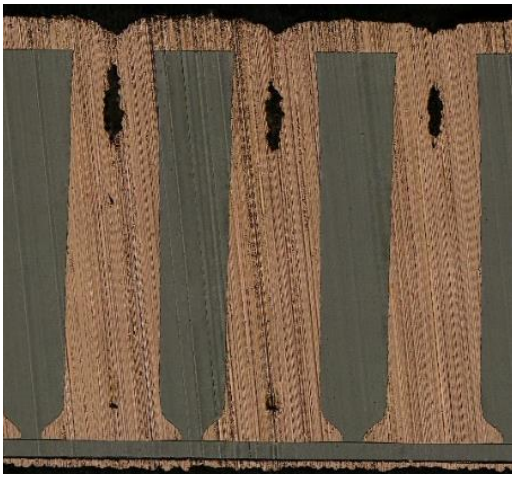


Figure 28: Keyhole void formation after plating proceeds to completion using 80 g/L Cu chemistry

superconformal initiation mechanism. This 'initiation mechanism' does not inherently yield a superfilled via. When plating was allowed to proceed to completion, as evidenced by Figure 28, where the same chemistry utilized for Cu ECD in Figure 27 was used. In Figure 28, one can see that seam or keyhole void formation still ultimately results, even after Cu growth appears faster in the via bottoms during the first 5-10 µm of Cu growth. In order to improve upon the fill profile in Figure 27 to promote full filling not seen in Figure 28, other parameters were investigated. However, the full filling of these TSVs is again a stretch goal, as lining of the TSVs with 15 µm of Cu being the minimum requirement for successful integration of these TSVs into the ion trap fabrication scheme.

4.3 Utilizing organic additives to modify via filling

As discussed in Section 4.2, MSA was deemed as the appropriate *additive free* chemistry to use for achieving a sufficiently thick Cu plating profile, but was not sufficient for fully filling the features. As initially presented in Chapter 2, the correct combination of three additives, suppressor, accelerator, and leveler, has been shown to help increase the plating rate at the bottom of TSVs or trenches relative to the top of these features. In order to utilize the additives discussed in Chapter 2 to achieve a superconformal fill, the filling coefficients of different samples plated after modifying the additive concentration were compared. The technique is presented in Figure 21 and the equation used is shown in Equation 8.[32]

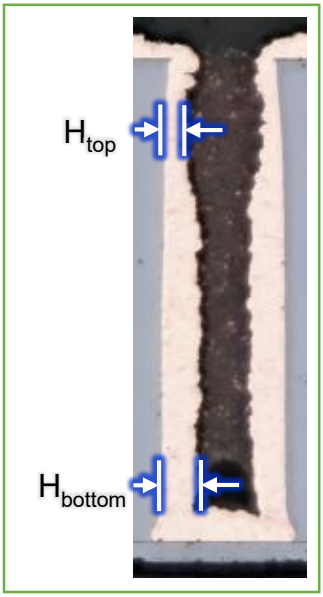


Figure 29: Fill profile characterization

$$k_{fill} = \frac{H_{bottom}}{H_{top}} \quad (8)$$

In order to achieve void-free fill or lining of these TSVs, a filling coefficient (k_{fill}) greater than 1.0 is desired. This statement means that the Cu is plating at a faster rate near at the bottom of the via than it is at the top, and ultimately it would mean that the features could be fully filled with Cu if k_{fill}>>1.0. Utilizing an Enthone GSW Cu chemistry accelerator, leveler, and suppressor (GSW additives B, C, and D, respectively), experiments were conducted in order to understand how affective these additives are at controlling the fill profile in these vias as shown in Figure 30, Figure 31, and Figure 32.

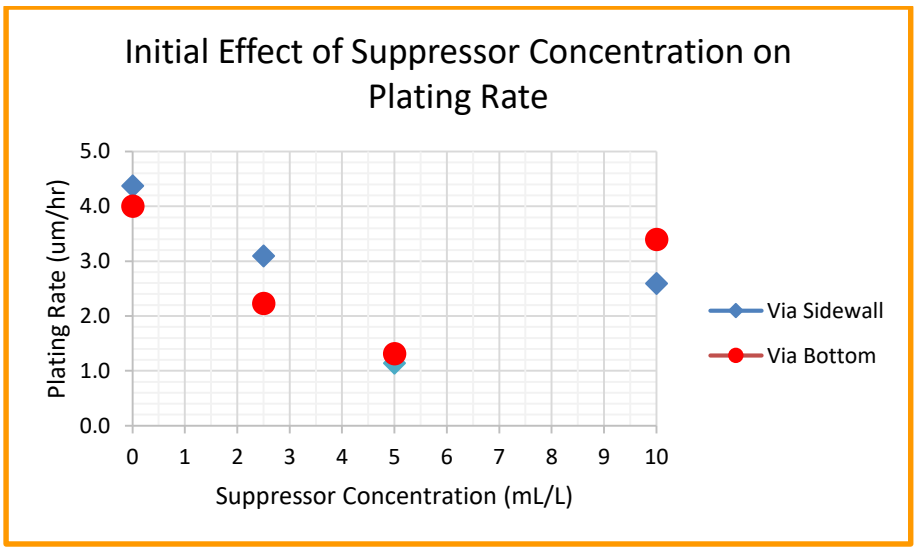


Figure 30: Impact of suppressor concentration on plating rate at via top and bottom

For the plating runs in Figure 30, a known concentration of accelerator and leveler (5 mL/L and 1 mL/L, respectively) was used per the recommended concentration supplied by Enthone Inc., and the concentration of suppressor was increased with each subsequent experiment, from 0-10 mL/L. As shown in in Figure 30, there appears to be an optimal concentration of suppressor at 10 mL/L. This does match up with many of the recommended proprietary recipes, which tend to suggest a suppressor concentration from 2x-4x of the accelerator concentration.[33, 34]

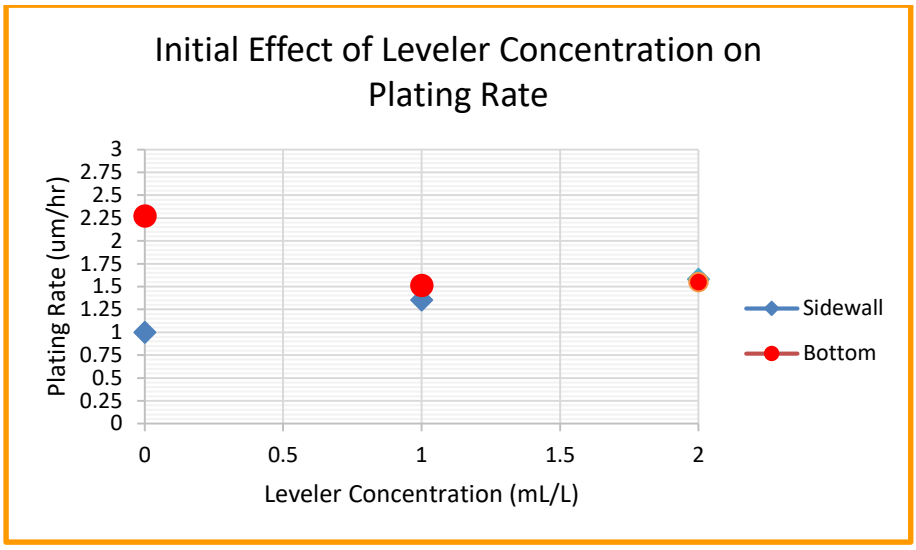


Figure 31: Impact of leveler concentration on plating rate at via top and bottom

The results from the work encompassed in Figure 30 were applied to the next experiment by setting the concentration of the suppressor to 10mL/L and keeping the accelerator at the recommended 5mL/L and modifying the concentration of leveler from 0-2 mL/L. These results are summarized in Figure 31. As shown in in Figure 31, the leveler does not seem to improve the fill profile, as k_{fill} is largest when no leveler is in solution.

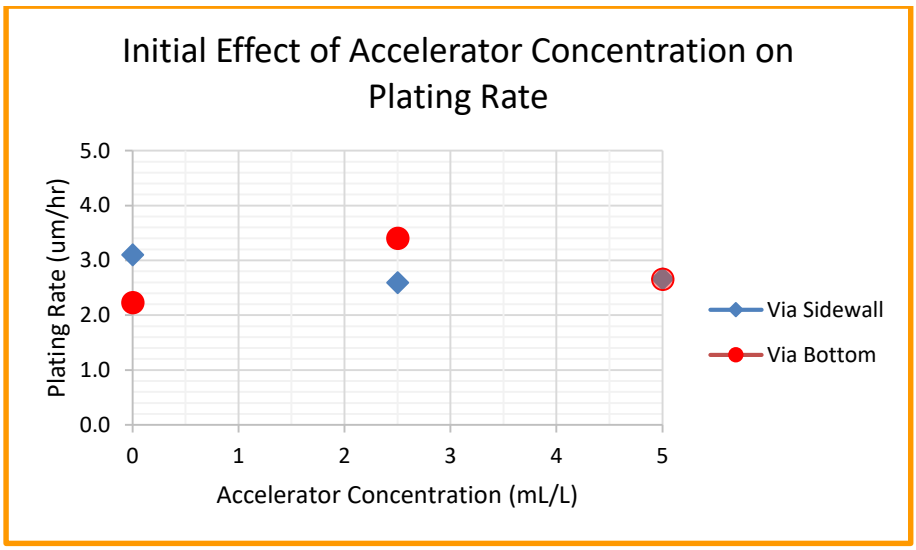


Figure 32: Impact of leveler concentration on plating rate at via top and bottom

For the plating runs in Figure 32, a known concentration of suppressor and leveler (10 mL/L and 1 mL/L, respectively) was used, and the concentration of accelerator was increased with each subsequent experiment, from 0-5 mL/L. As shown in in Figure 32, there appears to be an optimal concentration of accelerator at 2.5 mL/L. This matches up with the typical upper bound of suppressor recommendation (4:1).[33, 34]

As shown in Figure 30, Figure 31, and Figure 32, achieving a faster plating rate at the via bottoms was achieved initially, but one important caveat to this data is that it was taken only at Cu thicknesses around 10 μm. When deposition was allowed to proceed for longer time scales, void free Cu filling was not seen. As mentioned previously, the inability for the CEAC superfilling mechanism to be represented in these features could be because that model was developed for microscale features. In Section 4.3.1, this is examined using Finite Element Modeling, where the Cu growth front was examined in micro- and mesoscale features to confirm the experimental results.

4.3.1 COMSOL Modeling of CEAC Mechanism on Microscale and Mesoscale TSVs

Finite element modeling (FEM) using COMSOL Multiphysics™ software was conducted as a supplement to experimental work with the purpose of comparing the CEAC mechanism's effectiveness at different size scales. The results of this examination into the theoretical effect of the CEAC mechanism on three different geometries can be seen in Figure 33, culminating with the mesoscale TSV geometry. This was of practical interest because the CEAC model has only been shown to be functional for void-free Cu filling from the damascene up to approximately 100 μm length-scale interconnects. Within the COMSOL Multiphysics™ interface, the 'surface reaction kinetics' and 'growth front tracking' modules were combined,

specifically utilizing Equation 9 and 10 below.[25, 35]

$$i_{loc} = -(0.4726\theta + 0.0374)exp\left(-\frac{(0.5+0.25\theta)F}{RT}\eta\right) \quad (9)$$

$$v_n = \frac{i_{loc}M}{2F\rho} \quad (10)$$

Where θ is the local surface coverage of the catalyst, *F* is Faraday's constant, *R* is the gas

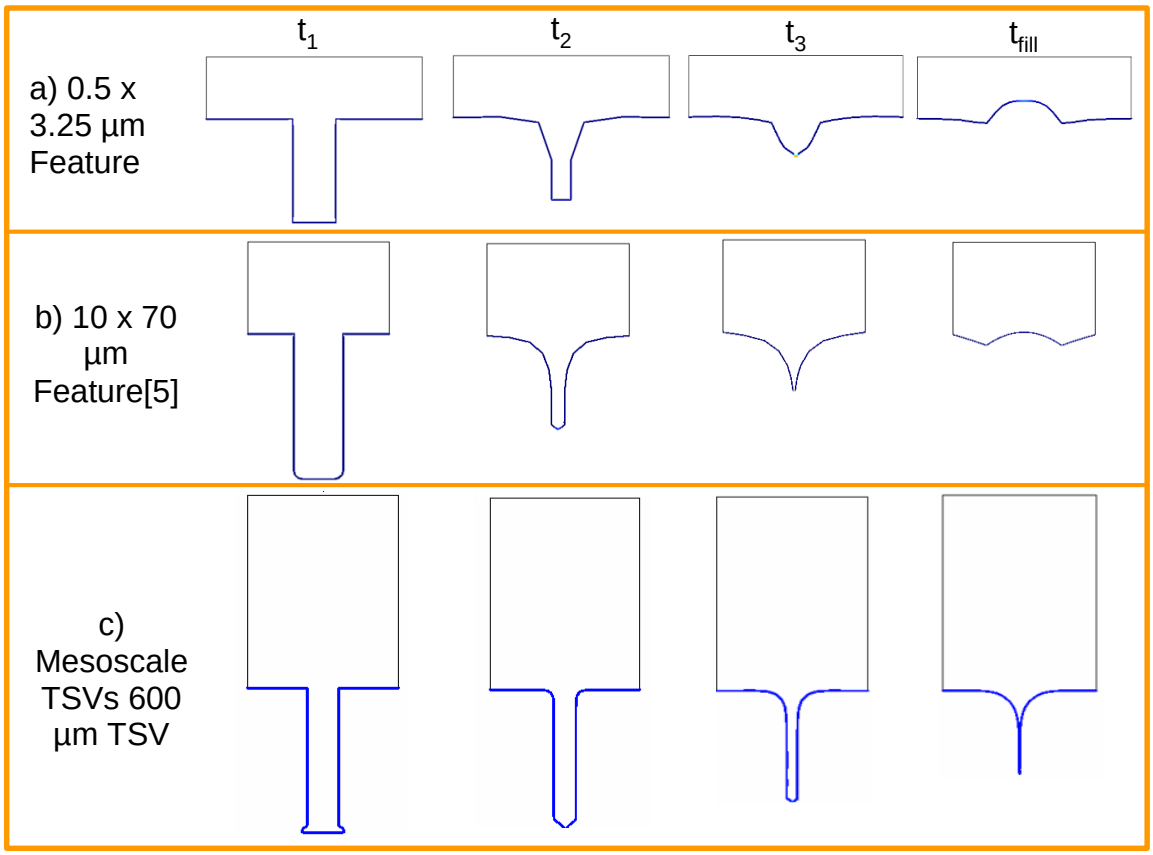


Figure 33: a) Cu growth front tracking showing superfilling evolution profile and b) 10 x 70 µm feature that has been shown to fully full using the CEAC mechanism by Sun et. al. and c) Mesoscale ion trap TSV fill profile showing seam or keyhole void formation to be likely

constant, *T* is the electrolyte temperature, η the overpotential at the cathode, *M* (kg/mol) is the molar mass, ρ is the density of Cu, and v_n is the normal mesh velocity or velocity of Cu at the growth front.

This model represents a simplified version of the CEAC mechanism, where Cu reduces onto the concave regions of the depositing surface more quickly than on planar regions.

A curvature dependent accelerating catalyst is modeled on the depositing surface, where superfilling is achieved in the smaller features due to curvature-enhanced accelerating catalyst concentration change, which is exclusively dependent on the surface curvature during deposition. The model does not account for the effect of suppression on the planar regions of the TSV or for leveling. As you can see at t_{fill} in Figure 33 a) and b), when the via is fully filled, a significant overburden thickness forms, which confirms the lack of leveling species in this model. From the equations, it is clear that the growth front orthogonal to the Cu surface at each point is proportional to the local current density (i_{loc}). In addition, this model does not account for fluid flow or dilute species transport within the electrolyte, which may have significant bearing on the resulting Cu fill profile.

In Figure 33 a), the Cu growth front for a standard damascene scale interconnect is that of a superfilled via, just as is true in Figure 33 b), which is much larger than damascene features, but still approximately an order of magnitude smaller in length and half as wide as the mesoscale TSVs focused on in this work. In summary, the model above establishes a clear fill profile difference when only considering the concavity of a surface as the cause for superconformal fill undergirded by the CEAC mechanism.

4.4 Applied Current Density Optimization

In order to obtain void free conformal deposition, there are a wide variety of variables to manipulate. One of these parameters consists of the current density applied to the substrate. By calculating the area of a given sample and testing a variety of applied current densities, one can optimize the fill profile based upon this applied current density. In Figure 34, one can clearly see that for direct current deposition in additive-free

electrolytes, there is a significant improvement in plating conformality corresponding to a decrease in the applied current density.

As shown in Figure 34, while reducing the current density in additive free baths does improve plating conformality, it may also yield dendritic, large grain structures. This is of particular concern in these large mesoscale vias, as there will be sufficient film thickness and plating time for any dendritic growth to lead to void formation, as shown in the SEM images in Figure 34 b). Despite this, the dendritic growth issue may also be mitigated with a combination of additives discussed in previous sections.

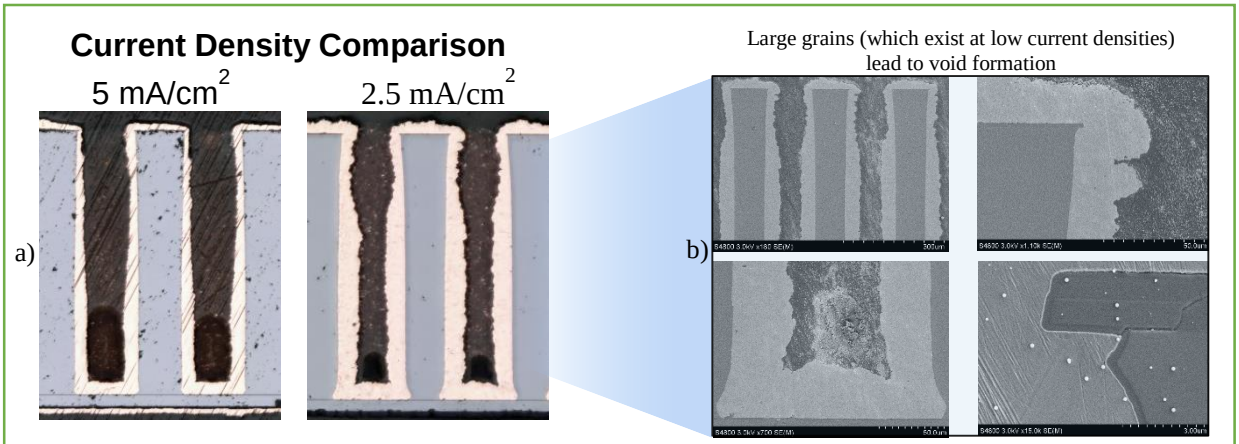


Figure 34: a) Optical microscopy comparing conformality difference caused by varying applied current densities and b) SEM images showing dendritic growth in additive-free baths at low current densities

4.5 Pulse Frequency and Duty Cycle Optimization

Two more parameters that may be manipulated when attempting to improve plating conformality are the applied pulse frequency and duty cycle. The pulse frequency is defined as the number of on cycles per second, while the duty cycle is defined as the percentage of time the applied potential is 'on', or reducing Cu ions at the

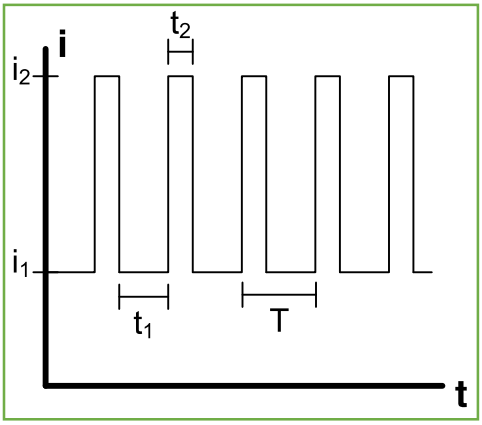


Figure 35: Sketch of applied pulse regime example, where i_2 is the current applied during the 'on' time (t_2), and t_1 is the off time

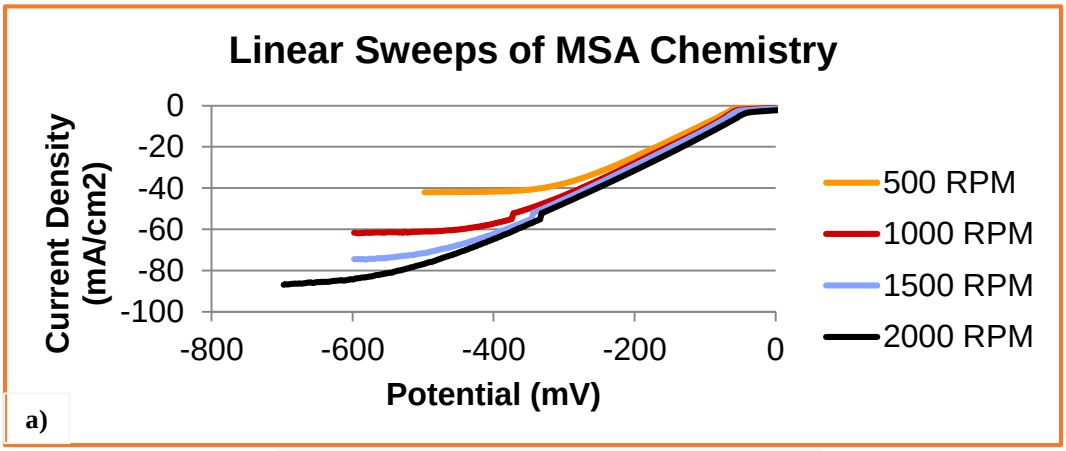
cathode. This concept is presented in Figure 35, where i_2 is the current applied during the 'on' time (t_2), and t_1 is the 'off' time with i_1 set to zero current. One popular method of understanding upper and lower bounds for Cu depletion within a given geometry is to utilize an RDE/potentiostat apparatus discussed above. By altering the rotation rate of the RDE in a known electrolyte, one can determine the diffusion coefficient, the amount of 'on' time, and 'off' time for Cu depletion and replenishment within the TSV geometry. This information can be gleaned using the 'Levich' equation as shown in Equation 11 and 12.

$$I_L = 0.62nFAD^{\frac{2}{3}}\omega^{\frac{1}{2}}\nu^{\frac{-1}{6}}C \tag{11}$$

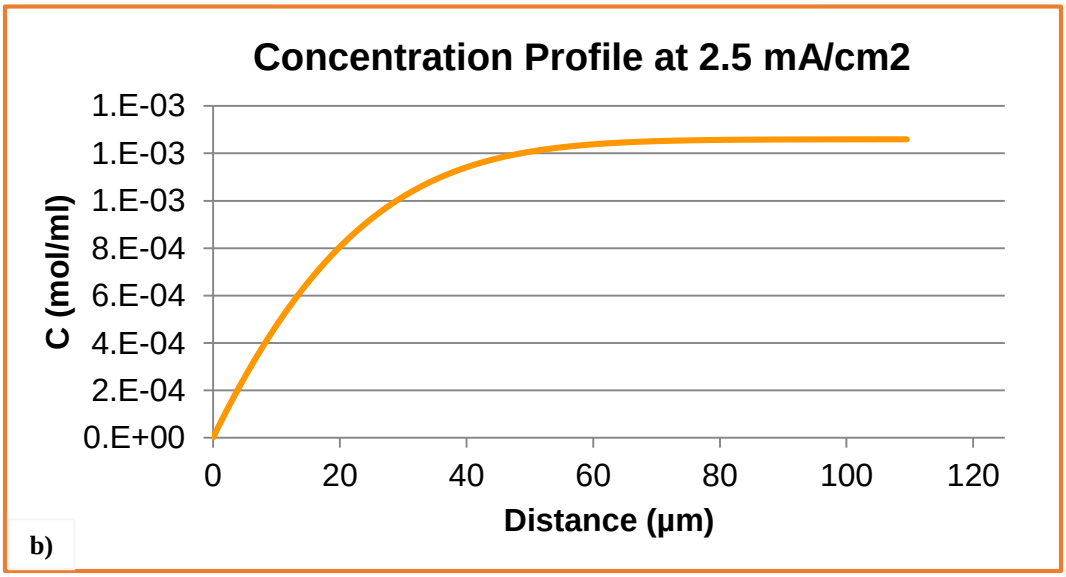
$$C(x,t) = C^* - \frac{i}{nFAD}\left\{2\left(\frac{Dt}{\pi}\right)^{\frac{1}{2}} exp\left(-\frac{x^2}{4Dt}\right) - x\, erfc\left[\frac{x}{2(Dt)^{\frac{1}{2}}}\right]\right\} \tag{12}$$

Where Equation 11 utilizes the electron transfer number (n), Faraday's constant (F), the angular velocity of the working electrode (ω), the kinematic viscosity of the fluid (ν), and the bulk Cu concentration (C), and the current (I_L) to determine the diffusion coefficient of Cu ions in the fluid (D). From there, Equation 12 is utilized to determine the concentration of Cu ions within the via geometry at any position (x) and time (t) to find the amount of time required for the concentration of Cu ions at the interface (C^*) to reach zero when a given electron transfer occurring at that interface. The graphical representation of these equations can be seen in Figure 36. In Figure 36, the potential is swept in the reductive (negative) direction, and each scan is performed at an increasing rotation rate. As discussed in Chapter 3, for any flat plat, the boundary layer thickness (δ) is proportional to the inverse square root of the velocity of the fluid ($u^{-1/2}$) at any position (x) across the surface, which increases the current density relative to a slower

rotation rate and thus larger boundary layer thickness. From this relationship, one can determine the diffusion coefficient using Equation 4 by simultaneously solving for the current (I_L) at each rotation rate (ω). After determining the diffusion coefficient of Cu in the MSA electrolyte, Equation 5 can be used to determine the local Cu concentration



Cu Ion Diffusion Coefficient = 985 µm^2/sec



Cu Diffusion Time for Replenishment in TSV Bottom = 1.6 sec
Applied Potential on Time for Cu Depletion = 0.105 sec

Figure 36: a) iV curve at varying planar electrode rotation rates for diffusion coefficient determination using Equation 3 and b) Concentration profile at known current density down via depth (x)

down the via depth at 2.5 mA/cm^2 and thus the amount of on or off time for Cu depletion and diffusion-caused replenishment, respectively.

Experimentally Determined D_{Cu}	Roha, D. Et. Al. Provided D_{Cu}[13]	Chuan Seng Tan, K.-N. C. Provided D_{Cu}[14]
985 μm^2/sec	800 μm^2/sec	1000 μm^2/sec

Table 6: Comparison between Levich Equation calculated Cu diffusion coefficient versus literature values in similar chemistries[1, 24]

As shown in Figure 36, the upper bound for applied potential for Cu depletion at the via bottom is 105 milliseconds, and the required off time for full bulk Cu replenishment is 1.6 seconds. In addition, the diffusion coefficient calculated from the data in Figure 36 a) was determined to be 985 μm^2/sec, which compares favorably with literature values for Cu in and MSA sulfate Cu ECD electrolyte, as shown in Table 3. After the diffusion

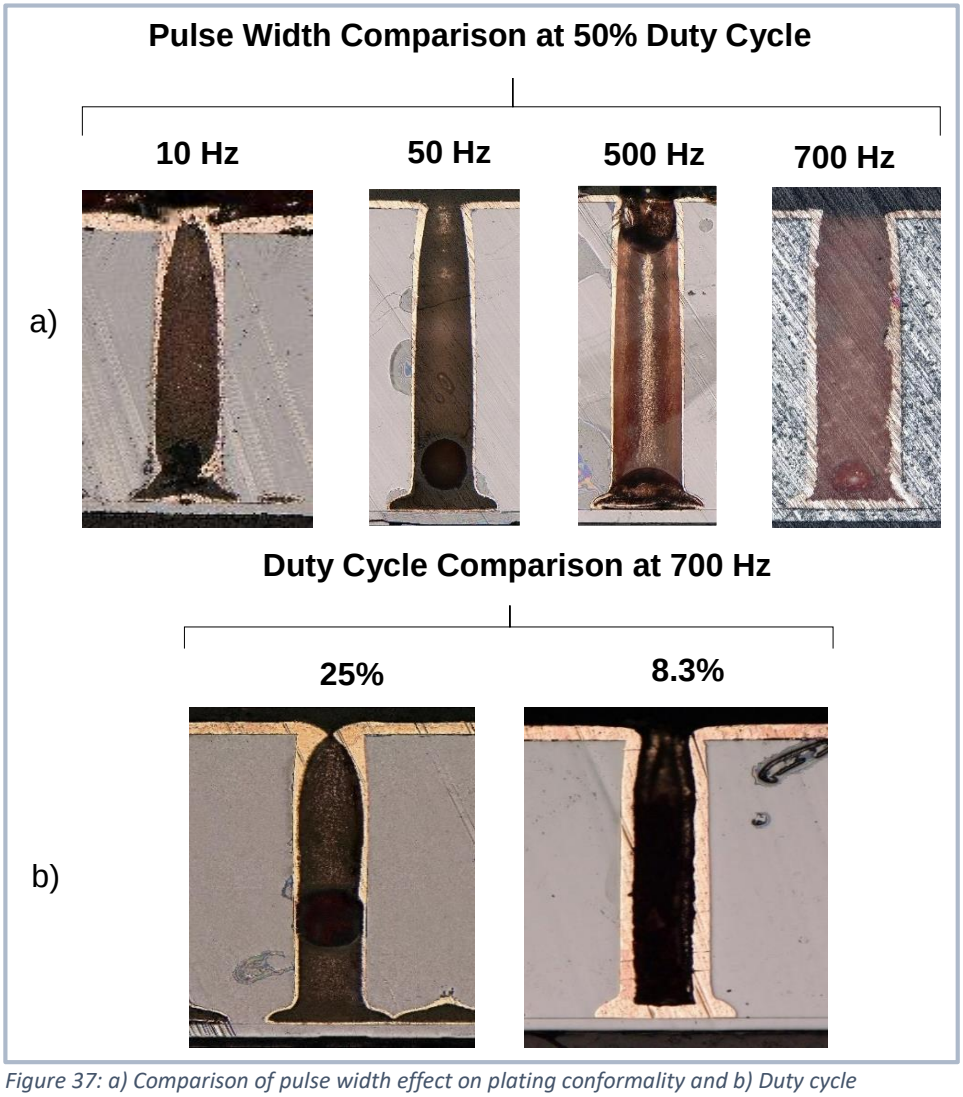


Figure 37: a) Comparison of pulse width effect on plating conformality and b) Duty cycle comparison at optimal (700 Hz) frequency from a). These test runs were all plated at or below 2.5 mA/cm2

coefficient in the MSA electrolyte, following by the on and off times for Cu depletion and replenishment are calculated, they can be effectively used as a guidewire for determining to optimal pulse frequency and duty cycle. A comparison of the effect of several pulse frequencies and duty cycles on the resulting Cu fill profile is shown in Figure 37.

As shown in Figure 37, the higher frequency (shorter on and off pulses) and lower duty cycle (smaller ‘on’ time per cycle) leads to an increase in conformality. This is a somewhat intuitive result, as a longer ‘off’ time will improve Cu replenishment through dissusion at the electrode/electrolyte interface and a decrease in ‘on’ time with each pulse will also decrease the amount of Cu depletion at the interface. This corresponds well to Figure 36, which provided an estimate for the amount of time required for Cu depletion and replenishment to occur during ‘on’ and ‘off’ time, respectively. Using the information gleaned in Figure 36 and Figure 37, one can establish a well-rounded perspective into the appropriate pulse regimes required for maintaining Cu concentrations similar to the bulk concentration throughout the via depth.

4.6 Conclusion

Significant experimentation in this work examined the viability of various ECD plating parameters for conformally plating these features thick enough to accommodate RF voltages at 100V and 100MHz. Improvements in the plated fill profile were attained through the use of a different acid in the additive-free electrolyte. Experimentation, both wet chemical and computational, was conducted into the efficacy of the three additive system discussed in Chapter 2 on these mesoscale features. In addition, the plating parameters, the applied current density, pulse frequency, and duty cycle, were examined

in attempts to optimize each of these parameters for achieving a superconformal Cu profile. The stretch goal of this research was to obtain fully filled, void free features, however this was not attained using the three-additive electrolyte discussed at length in Chapters 2 and 4. This lead to the motivation for the research conducted and experiments performed in Chapter 5.

Chapter 5: S-Shaped Negative Differential Resistance Approach for Bottom-Up Copper Filling[7, 25, 36-40]

5.1 Introduction

An alternative approach[7, 25, 36-40] for Cu TSV filling relies on a single-additive (suppressor or inhibitor) electrolyte rather than the three additive (suppressor, accelerator, and leveler) electrolyte discussed in Chapters 2 and 4. This technique is referred to as S-Shaped because the iV curve, when conducting a linear scan across an appropriate potential range is 'S-shaped', having significant hysteresis from the reductive versus oxidative scan direction. This technique is referred to as a Negative Differential Resistance mechanism because the electrolyte serves as a dynamic resistor which shifts its resistance depending upon the current passing through the electrolyte or potential across it. Specifically, when the input reductive potential increases, the resistance decreases.

The unique aspect to this particular technique for Cu TSV filling is that it enables fully filled TSVs, plating almost exclusively from the bottom up, despite initiating from a conformal conductive seed material which exists on the top field, via sidewalls and via bottoms. This is accomplished through careful control of three variables in this single additive electrolyte; the suppressor concentration; applied reduction potential; and diffusion layer thickness. In addition to these three plating parameters, specific types of suppressors are needed to create this hysteretic CV curve which is a signature for the ability for the plating to initiate only from the bottom of the TSV. In Addition, a novel modification to this technique is introduced, where an MSA electrolyte is utilized rather than an H_2SO_4 electrolyte, which increases the plating rate and decreases the dependency

on Cu ion diffusion due to an increase in the amount of Cu dissolved in solution prior to plating.[31]

5.2 Fundamental Principles

As mentioned in Chapter 2, copper electrodeposition from sulfuric acid electrolytes is described by the speciation of the metal cations. The deposition reaction sequence is re-written below:

$$Cu^{++} + e^{-} \rightarrow Cu^{+}$$

$$Cu^{+} + e^{-} \rightarrow Cu$$

Crucially, each of the Cu cations involved is solvated, or accompanied by water of hydration surrounding it. As the Cu is reduced out onto the electrode surface, the water

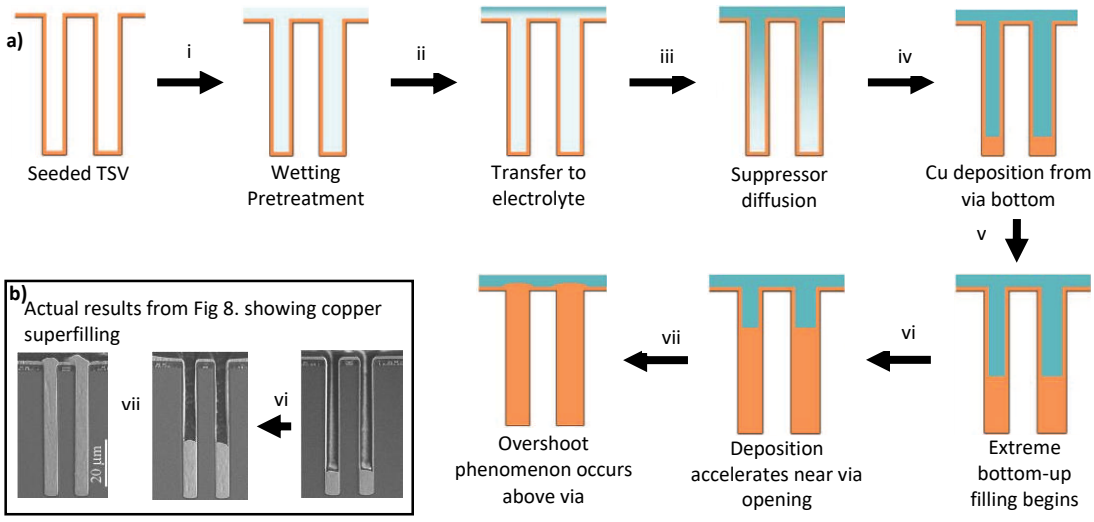


Figure 38: a) Sequence for S-NDR extreme bottom-up superfilling proven by b) experimental results on 56 x 5 .6 µm annular TSVs[7]

sheath is removed, which causes localized hydrophilic areas just above the Cu surface.[7, 25, 40] As the polyether suppressor is hydrophobic, the Cu reduction initiation causes a semi-permanent hydrophilic sheath over the electrode at the via bottom interface. This will only occur when the Cu reduction potential and local suppressor concentration at the

surface are such that the reduction is just energetically favorable to allow for the bottom surface of the TSVs to begin depositing, while the TSV sidewalls and the field retain a large enough concentration of suppressor to prevent deposition from occurring in these areas. Thus, deposition will occur as shown in Figure 38.[7]

As shown in Figure 38 a i), this process begins with a fully conductive seeded TSV. In Figure 38 a ii), the wetting pre-treatment is conducted, which may involve either an RC1 clean or an ethanol pre-wet process as referred to in Josell et. al. In Figure 38 a iii), the TSV sample is transferred to the S-NDR electrolyte without electrical connection. In Figure 38 a iv), the reductive potential is initiated, and if the potential, suppressor concentration, and boundary layer thickness are tuned properly, bottom up deposition begins. In Figure 38 a v), this bottom-up deposition proceeds toward the via opening. In Figure 38 a vi), the bottom up deposition will have approached the opening. In Figure 38 a vii), the bottom-up Cu deposition accelerates beyond the via opening, forming an overshoot that will be polished away subsequently via a chemical mechanical planarization (CMP) or mechanical planarization (MP) process. In Figure 38 b), one can see an experimental result showing this bottom-up fill profile as it proceeds through steps vi – vii, where it fully fills the via and overshoots. Figure 38 b) are images from Josell Et. Al. of an annular 56 μm TSV with an aspect ratio of 10.

Apart from the general plating mechanism resulting from this technique, a representative illustration of this mechanism is shown in Figure 39. In this figure, one observes that as the voltage is linearly scanned in the reductive direction, plating is fully suppressed

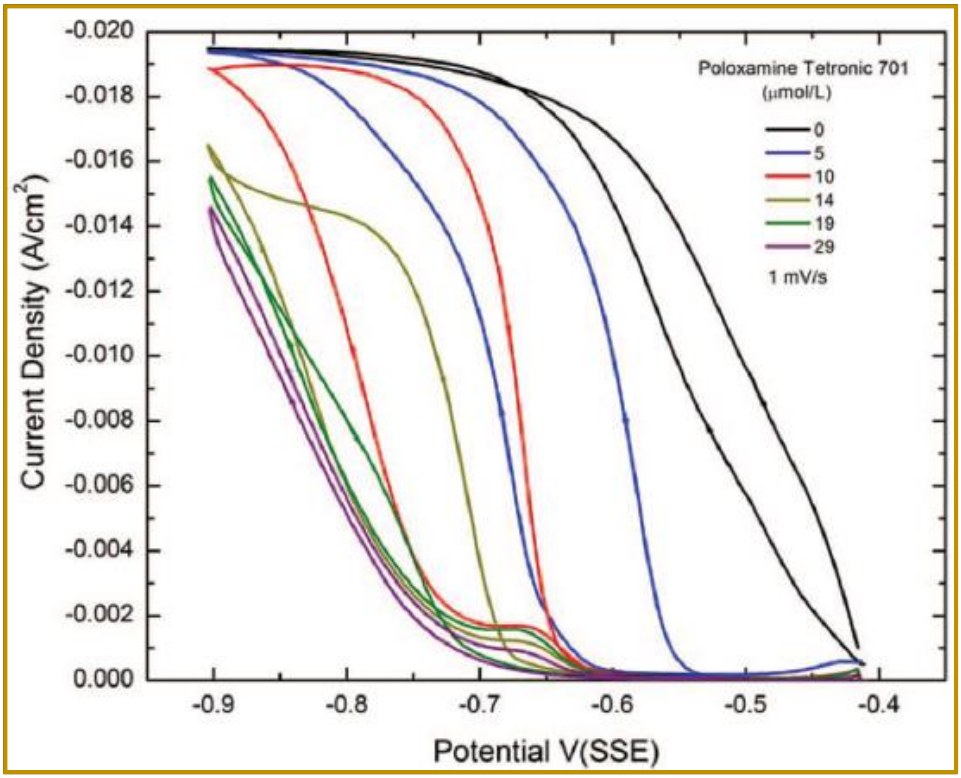


Figure 39: Example of S-NDR mechanism in H_2SO_4 electrolyte with increasing concentrations of poloxamine Tetronic 701 suppressor[6]

everywhere on the electrode due to the polyether suppressor blocking layer, until localized (ideally localized only on the via bottom on an actual sample) occurs, where the current reading quickly climbs. This potential at which the rate of change of current density rapidly increases is the potential where suppressor breakdown occurs. This point can be considered the 'suppressor breakdown potential', as this is the point where the potential is sufficiently negative to cause the

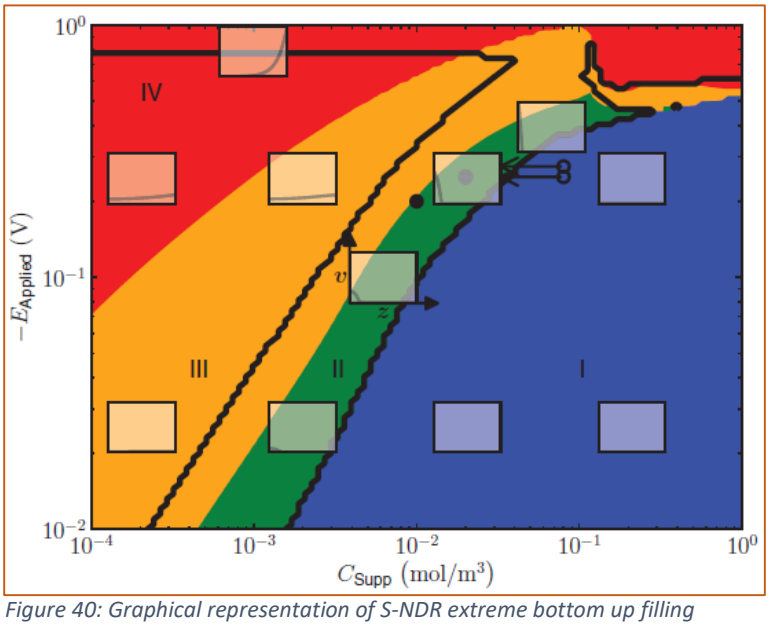


Figure 40: Graphical representation of S-NDR extreme bottom up filling importance on suppressor concentration and applied potential[6]

suppressor to desorb from the surface and allow plating to occur. On the positive return scan, the current reading is different from the reductive scan because the deposition is localized. This is also represented by Figure 41, where a planar electrode was plated in this S-NDR chemistry, and 'Turing-patterns' result. These nucleation-type plating patterns are representative of the localized deposition, which on a planar, abraded electrode occurs only at the bottom of recessed scratches and plates up from there.

As shown in Figure 39, when there is no suppressor in solution, there is little hysteresis, and plating begins immediately upon applying a reductive potential (vs. SSE). With each subsequent scan while increasing the suppressor concentration, the suppressor breakdown, or plating initiation, begins further negative, until what appears to be a limiting concentration around 20 µmol/L of polyether suppressor. These iV scans were conducted on a static planar electrode, and the Turing-pattern plating nucleation can be seen in Figure 41.

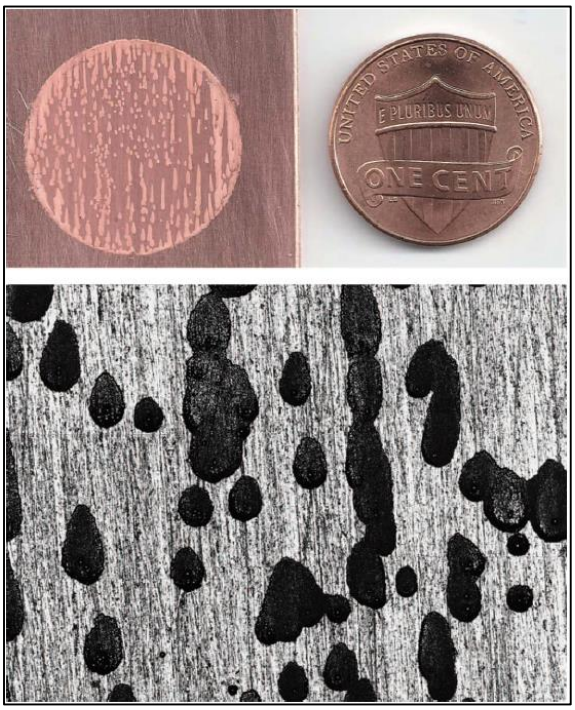


Figure 41: Turing pattern formation corresponding to critical behavior of extreme bottom-up superfilling electrolyte[6]

In addition to Figure 39 and Figure 41, a graphical representation of the importance of the suppressor concentration and applied potential, which was developed and modeled by Josell Et. Al. In Figure 40, one sees the red area, which represents too little suppression, so plating occurs everywhere along the feature and on the field. The yellow zone corresponds to subconformal plating

occurring along the feature and some plating on the field and pinchoff will ultimately occur generating a void in the via. The green zone represents the suppressor concentration/applied potential that is just right for plating to initiate and proceed in a bottom-up fashion, and the blue zone corresponds to too positive of applied potential and/or too much suppressor in solution preventing plating from occuring anywhere on the electrode. This region represents a fully suppressed system where the passivated layer cannot be disrupted in that potential range.

5.3 Annular Microscale TSV Filling

Josell et. al. examined the effectiveness of the S-NDR approach on annular TSVs with a 56 μm depth and aspect ratio of 10. The summary of these plating experiments is shown in Figure 42. In Figure 42, one can see that Moffat, Josell Et. Al. were able to tune the applied potential and suppressor concentration to achieve void-free superfilling at two different potentials and suppressor concentration illustrating the need to balance the applied potential with the diffusion of suppressor throughout the depth of the via. In Figure 42 a), one sees that at -0.6 V (vs. SSE) and 10 μM Tetronic 701 polyether suppressor, full bottom-up superfilling is achieved within 20 minutes of plating time. In Figure 42 b), the reductive potential is pushed 500 mV negative from the example in Figure 42 a), and to compensate for this to remain in the ‘green zone’ from Figure 40, the polyether suppressor concentration is doubled in order to maintain a full bottom-up fill profile. Of particular note in Figure 42 is the speed with which Cu is deposited in these features. These features are approximately 60 μm in depth, so the plating rate looks to be about 200 μm/hour, which fluctuates slightly around the suppressor concentration and applied potential of a given experimental run. This plating rate is extraordinarily large

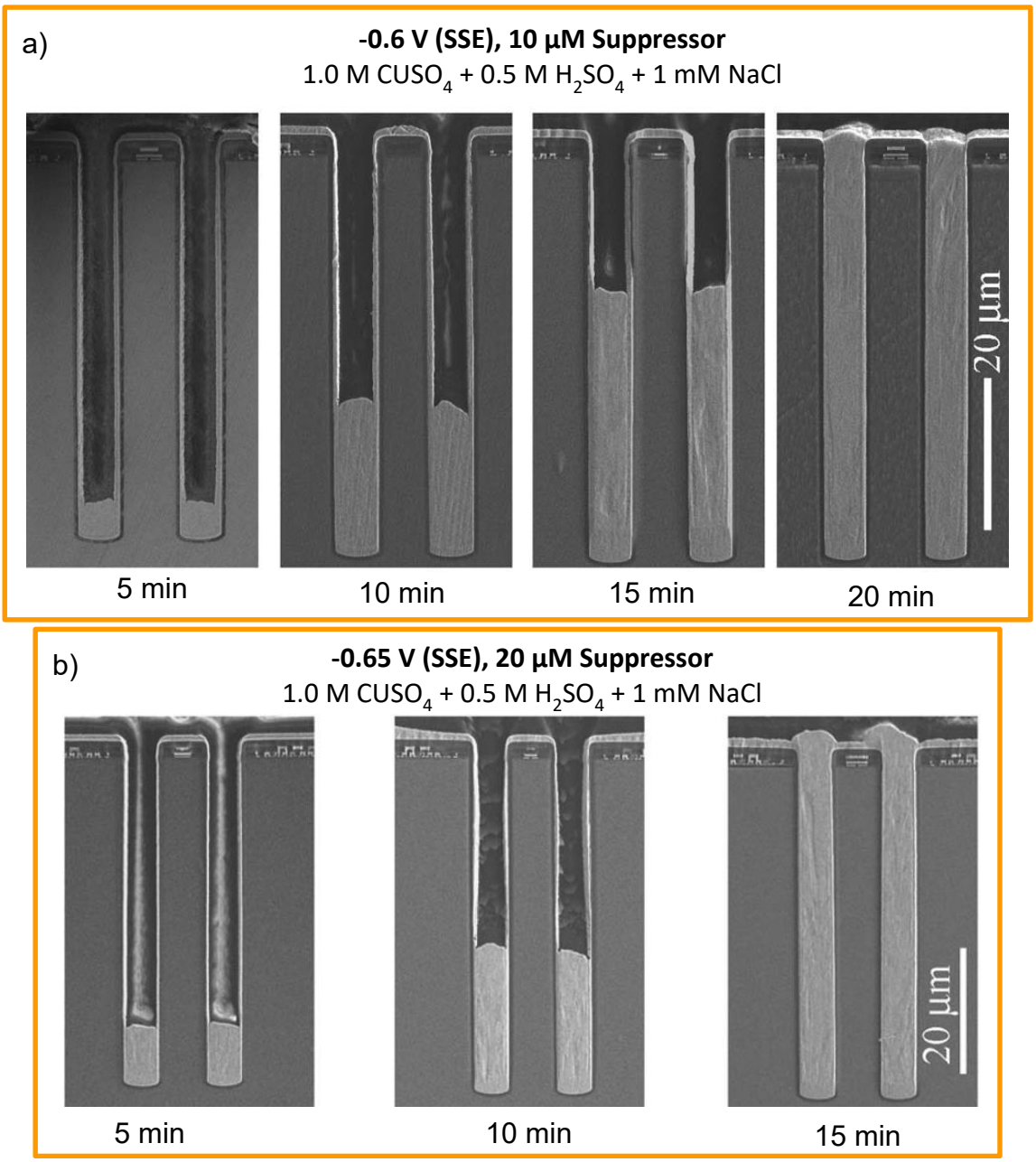


Figure 42: a) Cu growth front tracking with time for 20 minutes at 10 µM suppressor and -0.6 V (SSE) and b) Cu growth front tracking with time for 15 minutes at 20 µM suppressor and -0.65 V (SSE) [6]

relative to typical plating rates in acid Cu plating baths, which tend to exist at less than 50 µm/hour at similar potentials. Additionally, despite this fast plating rate in the bottom-up approach shown in Figure 42, the plated Cu is of particularly high quality.

5.4 Mesoscale H_2SO_4 TSV Filling

The S-NDR extreme bottom up filling technique introduced above is an exciting prospect for mesoscale TSV filling, and some results after implementing this approach on the

mesoscale TSVs are shown in Figure 43. The experiments presented in Figure 43 were all conducted by Daniel Josell, PhD on the NIST, Gaithersburg campus as a courtesy contribution to this work.

In Figure 43, one can see the importance of manipulating the three important variables in these experiments; the applied reductive potential, boundary layer thickness, and

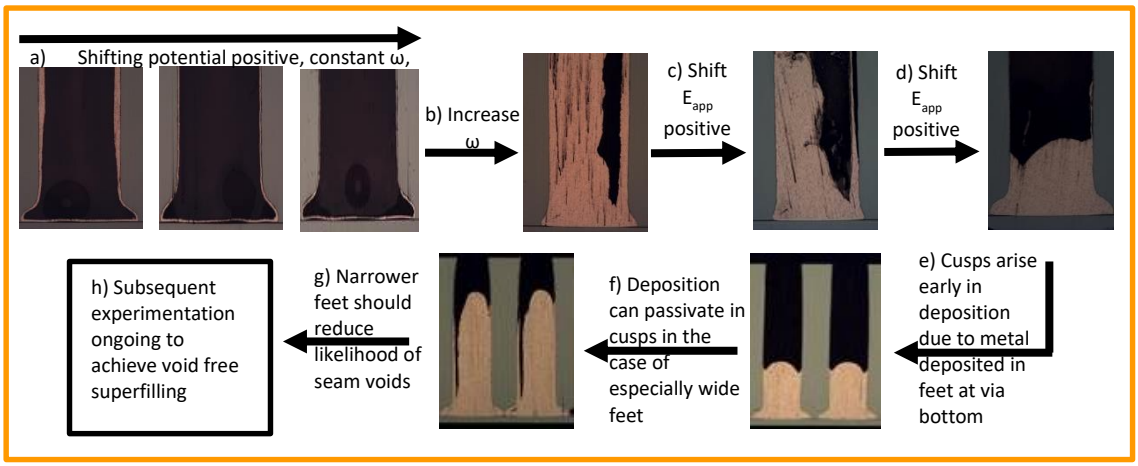


Figure 43: Results of S-NDR approach using 1 M $CuSO_4$, 0.5 M H_2SO_4, 1 mM NaCl, 0-25 µM Tetronic 701 chemistry showing effect of convection, Tetronic 701 concentration, and applied potential contributions on plating results in mesoscale TSVs

suppressor concentration. Refer to Section 3.4.1 for the plating setup for these experiments. Essentially, TSV samples are rotated with the via openings facing in the positive z direction so as to allow for a precisely controlled boundary layer thickness across the substrate. In Figure 43 a), an initial three experiments were conducted, and one can see a very thin Cu layer, which is improving in conformality, before almost bottom-up Cu growth is achieved. In Figure 43 b), the rotation rate was increased to thin the boundary layer and thus thin the distance by which Cu must diffuse from the bulk. In Figure 43 b), there is too much plating occurring too high up the feature, meaning that these plating parameters lead to a 'yellow zone' plating regime from Figure 40. In order to push the plating further down the feature, in Figure 43 c), the potential is shifted

further positive, and this is repeated in Figure 43 d), which achieves bottom-up filling. In Figure 43 e), one can see the result of large etch feet, which lead to cusps forming from passivated areas remaining suppressed in the shape of the Cu growth into those etch feet. In Figure 43 f), one can see that these cusps can be even worse with irregular convection, leading to large seam voids forming up the via length. To correct for this, the fluid flow speed needs to be reduced to prevent turbulent eddy currents from forming irregular suppression breakdown regions within the feature. For clarity, these issues may be mitigated by reducing the rotation rate and thus increasing fluid flow uniformity from one via to the next. One caveat to reducing the rotation rate is that the Cu replenishment will also be reduced. Thus in order to allow a lower rotation rate for reduced eddy current effects a MSA based electrolyte was utilized to increase the concentration of Cu and reduced the dependency on rotation rate for replenishing Cu ion concentrations.

5.5 Novel S-NDR TSV Filling with MSA Electrolyte

As shown in Section 5.4 above, there have been some promising results obtained with respect to filling these mesoscale TSVs using a 0.5 M H_2SO_4, 1 M $CuSO_4$, 1 mM NaCl electrolyte. However, the inconsistent filling results shown in Section 5.4 lead this research in the direction of transitioning to an MSA electrolyte, for similar reasons as discussed in Chapter 4. First, by using an MSA electrolyte, one can dissolve more Cu in solution. This may help to increase bottom-up uniformity between adjacent vias as well. In addition, this may be accomplished by rotating the samples at a slower rate, because there is sufficient Cu in solution to reduce the necessity of such a thin boundary layer thickness. The other benefit this chemistry may have is to increase the plating rate, as an

increase in available Cu at the bottom of the TSVs will allow for bottom-up plating to proceed more rapidly.

As shown in Figure 44, the same critical behavior is evident with an MSA electrolyte as was seen with the H_2SO_4 electrolyte. One can see that as the polyether suppressor compound was added to solution, the suppressor breakdown shifts further negative, and the corresponding hysteresis is similar to that of the H_2SO_4 electrolyte. The scans conducted in 0.25 M MSA, 1.25 M $CuSO_4$, and 1 mM NaCl chemistry. Turing Patterns are also shown in Figure 44 along with a comparison to non-hysteretic plating mechanism's planar plating example. The Turing Pattern formation shown in Figure 44, along with the critical behavior and hysteresis of the plating mechanism are clear evidence that this chemistry will function in the same way as the H_2SO_4 electrolyte, with the only difference being that there is more Cu in solution to increase plating rates and

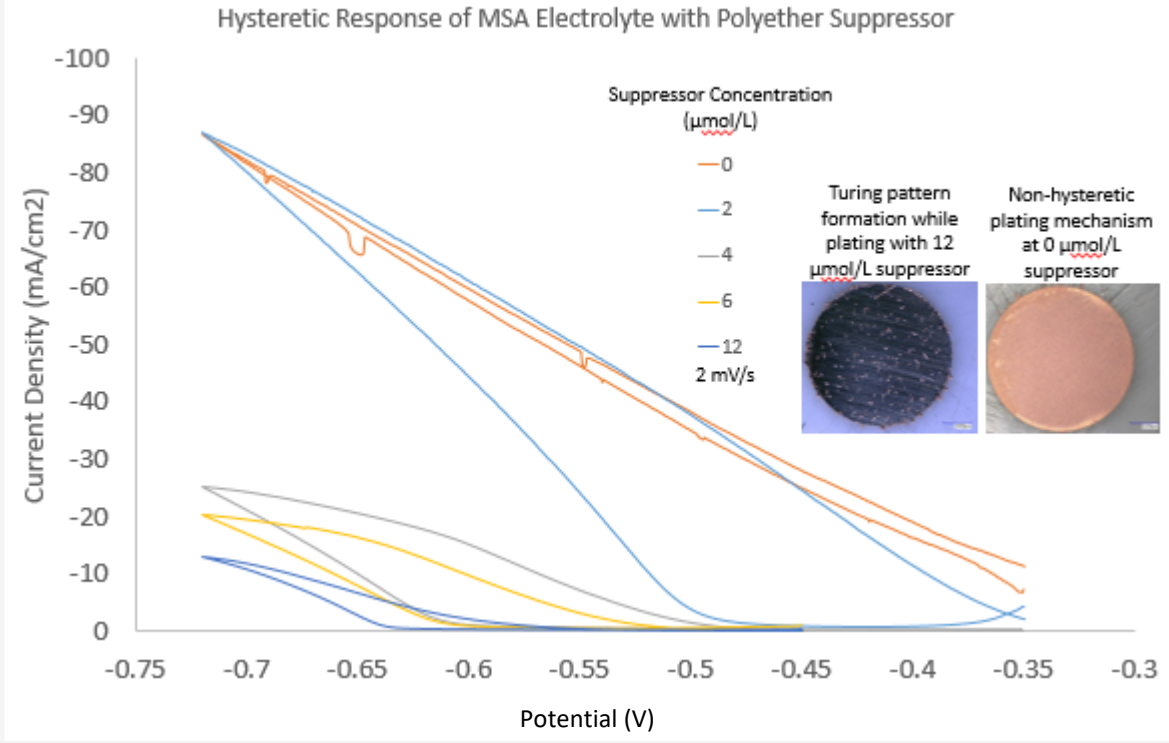


Figure 44: Hysteretic critical behavior of Cu ECD in 0.25 M MSA, 1.25 M $CuSO_4$, and 1 mM NaCl chemistry. Turing patters also shown in comparison to non-hysteretic plating mechanism's planar plating example

improve bottom-up uniformity. Although the MSA may help to maintain a more parallel fill profile with respect to the via bottom, there is still some evidence that the convection is still an important factor, as shown in Figure 45. In Figure 45 a1-a2), the nucleation site Cu deposition looks to have little relation to the 25 rpm rotational fluid flow across the

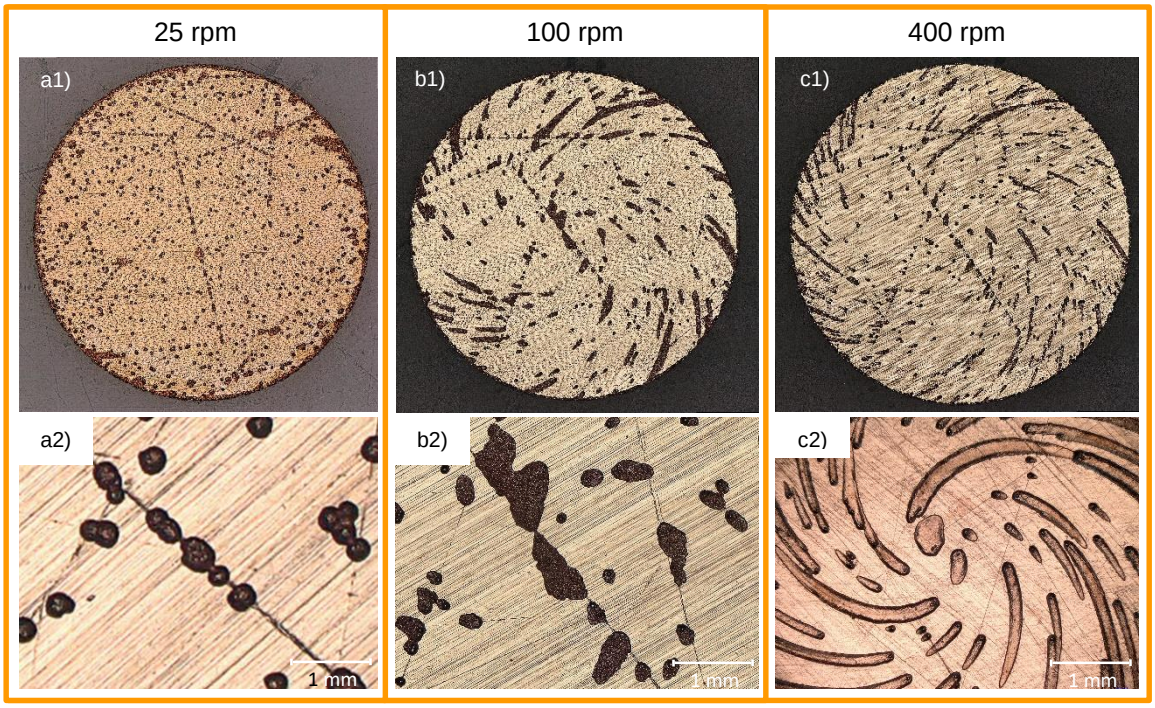


Figure 45: Examples of rotation rate effect on S-NDR mechanism Cu growth profile a1) Full planar electrode view showing vertical nucleation growth at 25 rpm, a2) Closeup of electrode shown in a1), b1) Increased nucleation in rotational pattern at 100 rpm and b2) Closeup of 100 rpm nucleation, c1) Extreme convection driven Cu growth and c2) Close-up of extreme rotational convection-driven growth

planar electrode. In Figure 45 b1-b2), the 100 rpm rotation rate looks to have caused Cu deposition in a pattern effected by the direction of fluid flow. In Figure 45 c1-c2) the 400 rpm rotation rate has caused even more significant rotational Cu growth profiles atop the electrode. From these images, one may consider the boundary layer thickness and fluid flow direction to be particularly impactful as far as the fill uniformity between adjacent vias and the upward Cu growth profile within those features.

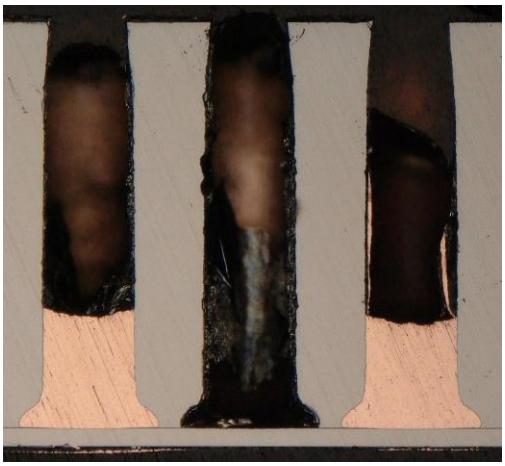


Figure 46: Sample plated in 0.25 M MSA, 1.25 M CuSO4, 1 mM NaCl, 25 µm Tetronic 701, at 400 rpm, -0.6 V(SSE), 400 rpm, for 2 hr

After the MSA chemistry used in Figure 44 was shown to be an effective tool for improving upon the already established S-NDR technique, samples were plated and cross sectioned, and the best results are shown in Figure 46 and Figure 47. In Figure 46, one can see that there is bottom-up initiation in two of the three vias shown. This is a common result of the S-NDR mechanism, where some vias have bottom-up initiation, but it isn't as consistent as is required. When utilizing the identical wetting technique used here with a conformal chemistry, consistent Cu plating was achieved. So, althought consistent bottom-up filling does seem to be aided through the use of a larger concentration of Cu in an MSA electrolyte as compared to an H_2SO_4 electrolyte with less Cu, it is an issue that needs to be investigated further to be entirely eliminated before the technique can be successfully implemented in the ion trap integration scheme. Future work will continue to attempts to improve upon this, mainly through a reduction in convection, as this irregular convection within adjacent vias is thought to be a potential cause of bottom-up irregularity. In Figure 47, one sees almost fully filled features, the cusp formation is thought to exist as a function of both convection and TSV bottom etch stop cusp size. The

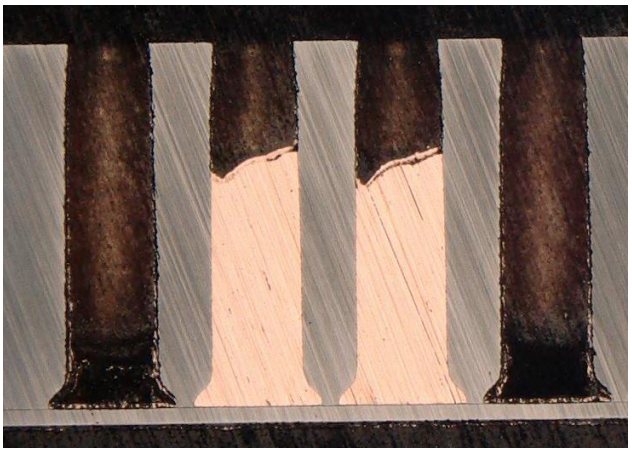


Figure 47: Sample plated in 0.25 M MSA, 1.25 M CuSO4, 1 mM NaCl, 50 µm Tetronic 701, at 400 rpm, -0.6 V(SSE), 400 rpm, for 4.5 hr

sample in Figure 47 was plated in 0.25 M MSA, 1.25 M $CuSO_4$, 1 mM NaCl, 50 µm Tetronic 701, at 400 rpm, -0.6 V(SSE), 400 rpm, for 4.5 hr and is the best result this research has had so far in relation to MSA-electrolyte S-NDR extreme bottom-up superfilling.

Chapter 6: Summary and Future Work

6.1 Summary

This work initially investigated a traditional three additive system as well as an additive-free chemistry for mesoscale TSV Cu ECD lining and full feature filling. Using these techniques, the TSVs were plated sufficiently for a successful conformal lining of these features thick enough to accommodate RF voltages at 100V and 100MHz. However, full feature filling, which has advantages for downstream integration approaches was not accomplished using this technique. Thus, a novel S-NDR extreme bottom-up superfilling electrolyte was investigated, which relied on a single polyether suppressor additive to allow for plating to initiate exclusively from the bottom-up.[7, 25] This method has been implemented with inconsistent success, and so far has proved capable of achieving approximately ¾ full feature fill without consistent uniformity between adjacent vias. An H_2SO_4 electrolyte was investigated, but was unable to achieve consistent full feature filling across hundreds of vias. Current work is being conducted into understanding why filling results have yet to be completely consistent across multiple rows of vias and how to improve upon the bottom-up fill consistency. Most importantly however, the optimal results found herein have relied on an MSA electrolyte, which is a wholly novel approach prior to the work presented herein.

6.2 Future Work

Future work will investigate approaches to accomplish full bottom-up feature filling using 0.25 M MSA, 1.25 M $CuSO_4$, 1 mM NaCL, and 1-100 µM Tetronic 701 chemistry. In particular, high suppressor concentrations and low rotation rates will be thoroughly investigated with the goal of achieving bottom-up approaching 100% uniformity across a

mesoscale TSV substrate. In addition, this technique will be implemented at the 6” and 8” wafer scales with similarly precise bottom-up uniformity across an entire wafer.

References

1. Chuan Seng Tan, K.-N.C., Steven J. Koester, *3D Integration for VLSI Systems*. 2012, Boca Raton: Pan Stanford Publishing.
2. Puttkammer, P.P., *Boundary Layer over a Flat Plate*. 2013, University of Twente: Twente.
3. Jung-Chih Hu, W.-C.G., Ting-Chang Chang, Ming-Shiann Feng, Chun-Lin Cheng, You-Shin Lin, Ying-Hao Li, Lih-Juann Chen. 2005: Germany.
4. Corp., P.R. *MSR Rotator*. Pine Research 2017 June 3; Available from: https://www.pineresearch.com/shop/rotators/standard/msr/.
5. Sun, J.J., et al., *High-aspect-ratio copper via filling used for three-dimensional chip stacking.* Journal of the Electrochemical Society, 2003. **150**(6): p. G355-G358.
6. Moffat, T.P., et al., *Superconformal film growth: Mechanism and quantification.* Ibm Journal of Research and Development, 2005. **49**(1): p. 19-36.
7. Moffat, T.P. and D. Josell, *Extreme Bottom-Up Superfilling of Through-Silicon-Vias by Damascene Processing: Suppressor Disruption, Positive Feedback and Turing Patterns.* Journal of the Electrochemical Society, 2012. **159**(4): p. D208-D216.
8. Andricacos, P.C., et al., *Damascene copper electroplating for chip interconnections.* Ibm Journal of Research and Development, 1998. **42**(5): p. 567-574.
9. Meulenbroeks, D., *Aluminum Versus Copper Conductors*. 2014, Siemens: Switzerland.
10. Huang, R., et al., *Stress, Sheet Resistance, and Microstructure Evolution of Electroplated Cu Films During Self-Annealing.* Ieee Transactions on Device and Materials Reliability, 2010. **10**(1): p. 47-54.
11. Knisely, K., *R&D S&E Electronics Engineering - MESAFab*, A. Hollowell, Editor. 2017.
12. Lau, G.K., et al., *Process Integration and Challenges of Through Silicon Via (TSV) on Silicon-On Insulator (SOI) Substrate for 3D Heterogeneous Applications.* 2015 Ieee 17th Electronics Packaging and Technology Conference (Eptc), 2015.
13. Alvanos, T., et al., *A Novel Methodology for Wafer-Specific Feed-Forward Management of Backside Silicon Removal by Wafer Grinding for Optimized Through Silicon Via Reveal.* 2014 Ieee 64th Electronic Components and Technology Conference (Ectc), 2014: p. 452-458.
14. Huang, B.K., et al., *Integration Challenges of TSV Backside Via Reveal Process.* 2013 Ieee 63rd Electronic Components and Technology Conference (Ectc), 2013: p. 915-917.
15. Liu, C.H., et al., *Integrated Process Characterization and Fabrication Challenges for 2.5D IC Packaging Utilizing Silicon Interposer with Backside Via Reveal Process.* 2014 Ieee 64th Electronic Components and Technology Conference (Ectc), 2014: p. 1628-1634.
16. Bandes, H., *The Electrodeposition of Copper - a Review of Recent Literature.* Transactions of the Electrochemical Society, 1945. **88**: p. 263-279.
17. Brown, O.W. and F.C. Mathers, *Electrodeposition of copper upon iron.* Journal of Physical Chemistry, 1906. **10**(1): p. 39-51.
18. Moffat, T.P., et al., *Superconformal electrodeposition of copper (vol 4, pg C26, 2001).* Electrochemical and Solid State Letters, 2001. **4**(8): p. L5-L5.
19. Moffat, T.P., D. Wheeler, and D. Josell, *Electrodeposition of copper in the SPS-PEG-Cl additive system - I. Kinetic measurements: Influence of SPS.* Journal of the Electrochemical Society, 2004. **151**(4): p. C262-C271.
20. Yokoi, M., S. Konishi, and T. Hayashi, *Mechanism of the Electrodeposition and Dissolution of Copper in an Acid Copper-Sulfate Bath .1. The Behavior of Intermediate, Cu+.* Denki Kagaku, 1983. **51**(3): p. 310-316.

21. Yokoi, M., S. Konishi, and T. Hayashi, *Mechanism of the Electrodeposition and Dissolution of Copper in an Acid Copper-Sulfate Bath .3. Effect of Cl- Ions.* Denki Kagaku, 1983. **51**(6): p. 456-459.
22. Yokoi, M., S. Konishi, and T. Hayashi, *Mechanism of the Electrodeposition and Dissolution of Copper in an Acid Copper-Sulfate Bath .5. Acceleration Mechanism in the Presence of Cl- Ions.* Denki Kagaku, 1983. **51**(6): p. 460-464.
23. Yokoi, M., S. Konishi, and T. Hayashi, *Mechanism of Electrodeposition and Dissolution of Copper in an Acid Copper-Sulfate Bath .2. Mixed Controlled Reaction Model.* Denki Kagaku, 1982. **50**(12): p. 941-945.
24. Roha, D. and U. Landau, *Mass-Transport of Leveling Agents in Plating - Steady-State Model for Blocking Additives.* Journal of the Electrochemical Society, 1990. **137**(3): p. 824-834.
25. Josell, D., D. Wheeler, and T.P. Moffat, *Modeling Extreme Bottom-Up Filling of Through Silicon Vias.* Journal of the Electrochemical Society, 2012. **159**(10): p. D570-D576.
26. Lee, Y.Y.a.T.R., *Contact Angle and Wetting Properties*, in *Surface Science Techniques*. 2013, Springer: Verlag. p. 3-34.
27. Wagner, F.T., T.E. Moylan, and S.J. Schmieg, *Hydrophilic Vs Hydrophobic Coadsorption - Carbon-Monoxide and Water on Rhodium(111) Vs Platinum(111).* Abstracts of Papers of the American Chemical Society, 1987. **194**: p. 2-Coll.
28. Zhang, J.H., et al., *Wetting process of copper filling in through silicon vias.* Applied Surface Science, 2015. **359**: p. 736-741.
29. James Welty, C.W., Robert Wilson, Gregory Rorrer, *Fundamnetals of Momentum, Heat, and Mass Transfer*. 2008, Danvers: John Wiley and Sons, Inc.
30. Tech, A.H., *8" Multiprep Polishing Tool On-Site Training*. 2016: San Diego.
31. Cho, S.K., M.J. Kim, and J.J. Kim, *MSA as a Supporting Electrolyte in Copper Electroplating for Filling of Damascene Trenches and Through Silicon Vias.* Electrochemical and Solid State Letters, 2011. **14**(5): p. D52-D56.
32. Yazhou Zhang, G.D., Hong Wang, Ping Cheng and Rui Liu, *Optimization of innovative approaches to the shortening of filling times in 3D integrated throuh-silicon-vias (TSVs).* Journal of Micromechanics and Microengineering, 2015: p. 1-11.
33. *Intervia 8500,8501,8502 Technical Data Sheet*, in *Intervia Cu 8540 TDS*. 2017, MicroChem.
34. *Cu-M Technical Data Sheet*, in *Cu-Bath M TDS*. 2016, Enthone.
35. Moffat, T.P., et al., *Superconformal electrodeposition of copper.* Electrochemical and Solid State Letters, 2001. **4**(4): p. C26-C29.
36. Josell, D. and T.P. Moffat, *Bottom-up Copper Deposition in Alkaline Electrolytes.* 2014 Ieee International Interconnect Technology Conference / Advanced Metallization Conference (Iitc/Amc), 2014: p. 281-283.
37. Josell, D. and T.P. Moffat, *Superfilling Damascene Trenches with Gold in a Sulfite Electrolyte.* Journal of the Electrochemical Society, 2013. **160**(12): p. D3009-D3014.
38. Josell, D. and T.P. Moffat, *Bottom-Up Electrodeposition of Zinc in Through Silicon Vias.* Journal of the Electrochemical Society, 2015. **162**(3): p. D129-D135.
39. Josell, D., M. Silva, and T.P. Moffat, *Superconformal Bottom-Up Cobalt Deposition in High Aspect Ratio Through Silicon Vias.* Journal of the Electrochemical Society, 2016. **163**(14): p. D809-D817.
40. Wheeler, D., T.P. Moffat, and D. Josell, *Spatial-Temporal Modeling of Extreme Bottom-up Filling of Through-Silicon-Vias.* Journal of the Electrochemical Society, 2013. **160**(12): p. D3260-D3265.