FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

CMOS Phase Modulator for Polar Transmitters

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Abstract

The Internet of Things (IoT) is an emerging and promising technology which will revolutionize the global world through connecting objects every day. IoT deals with low-power devices which interact with each other through the Internet. To ensure the connection with this massive devices and services it is used the next generation 5G mobile networks that requires a high data rate communication and use spectral efficient modulators. Thus, a great solution is the orthogonal frequency-division multiplexing (OFDM) since it divides the entire channel into many narrow-band sub-channels, which are transmitted in parallel to maintain high-data-rate transmission.

An important part of the wireless device is the radio transceiver. It consists of a receiver and a transmitter. It is important to develop a transmitter with a high efficiency and linearity, and with a low system complexity. Also, standards like OFDM present high peak to average power ratio (PAPR), which decreases the transmitter efficiency by forcing large power back-off operation. So, one suitable solution is the use of polar and outphasing transmitters which increases the efficiency. A polar transmitter is mainly constituted by two blocks which one is responsible for the phase modulation and the other one for the amplitude modulation.

The aim of this dissertation is building a phase modulator for a polar transmitter in (complementary metal-oxide-semiconductor (CMOS) 180nm technology. The CMOS technology is adequate for the digital domain and has a low efficiency in RF, however it is a low-cost technology which is ideal to be applied in circuits fabricated in a large scale. The proposed modulator is composed by three main blocks: a phase interpolator, a phase signal divider and a sign bit. The crucial cell of this project is the phase interpolator, which is responsible for performing the final RF phase modulation. An important aspect to have in count in this work is the high power consumption, since the RF interface consumes a lot of power, in any device. Thus, this modulator must not be fully digital because those architectures have a great power consumption due to the use of multiplexers with a significative number of inputs. Based on this, we decided to follow a mixed signal approach.It receives two digital differential orthogonal signals, thus those signals define which quadrant of unit-circle will be performed. Also, it receives a baseband signal which will select the output phase in the desired quadrant. To select the desired quadrant to perform it was developed a sign bit cell which is responsible for select the input signals of the interpolator. To obtain those four input RF signals it was used a frequency signal divider composed by latches which receive a signal with a frequency two times greater than the required.

A high performance phase modulator must have a low phase noise , which implies an increase of power consumption. Based on this, the goal of this project was achieved a great phase resolution with a better power consumption without damaging the output phase per quadrant. In this project, it was achieved a 5-bit resolution, per quadrant, for 2.53mW power consumption.

Resumo

A Internet das coisas (IoT) é uma tecnologia promissora que está em desenvolvimento, e promete revolucionar o mundo da tecnologia com a conexão de todos os objetos que usamos no dia-a-dia. IoT usa dispositivos de baixa potência que interagem uns com os outros através da internet. Para garantir a conexão com esses dispositivos e serviços, é necessário o uso da nova geração de redes móveis 5G, que requer uma elevada taxa de transmissão de dados senso assim necessários moduladores eficientes em todo o espectro. Uma solução poderia ser a multiplicação ortogonal por divisão de frequência (OFDM), uma vez que esta divide todo o canal em múltiplos sub-canais de banda estreita, que são transmitidos em paralelo de modo a manter a alta transmissão de taxa de dados.

Uma parte importante de um dispositivo sem fios é o transmissor de rádio que consiste num receptor e num transmissor. Um transmissor deve ser desenvolvido com alta eficiência e linearidade e com baixa complexidade do sistema. Além disso, padrões como OFDM apresentam uma relação de potência entre pico e média alta, que diminui a eficiência do transmissor. Assim, uma solução adequada a estas condições, é o uso de transmissores polares e outphasing devido ao aumento de eficiência. Um transmissor polar é constituído principalmente por dois blocos, sendo um deles responsável pela modulação de fase e o outro pela modulação de amplitude.

O objetivo desta dissertação é a construção de um modulador de fase para um transmissor polar em tecnologia de 180nm (CMOS). Esta é adequada para o domínio digital e tem baixa eficiência no domínio RF, no entanto, é uma tecnologia de baixo custo, o que é ideal para ser aplicada em circuitos fabricados em grande massa. Um aspeto importante a ter em conta neste trabalho é o grande consumo de energia, uma vez que a interface RF consome muita energia em qualquer dispositivo que a utilize. Assim, o modulador deste trabalho não deve ser totalmente digital devido ao elevado consumo de energia , uma vez que são arquiteturas que recorrem a multiplexadores com um número significativo de entradas. Mediante estes requisitos, foi decidido seguir uma abordagem mixed-signal. O modulador proposto é composto por três blocos principais: um interpolador de fase, um divisor de fase de um sinal de relógio e um seletor de sinal. O bloco mais sensível deste projeto é o interpolador de fase, que é responsável por realizar a modulação de fase. Este intepolador recebe dois sinais RF defasados de 90 graus que definem qual quadrante de círculo unitário será executado. Além disso, recebe um sinal de banda base que selecionará a fase de saída no quadrante desejado. Para selecionar o quadrante desejado, foi desenvolvida uma célula que é responsável por selecionar os sinais de entrada do interpolador. Além disso, para obter os quatro sinais RF de entrada, foi utilizado um divisor de sinal de frequência composto por latches que recebem um sinal com frequência duas vezes maior do que a requerida.

Um modulador de fase com um bom desempenho deve ter um baixo ruído de fase, o que implica um aumento do consumo de energia. Com base nisso, o objetivo deste projeto foi alcançar uma ótima resolução de fase com um melhor consumo de energia sem danificar a fase de saída por quadrante. Neste projeto, foi obtida uma resolução de 5 bits, por cada quadrante do círculo unitário, para consumo de energia de 2,53mW.

Acknowledgments

Sometimes our health prank on us and changes our plans, our future, and our mental well being, so am extremely grateful to my advisor Prof. Cândido Duarte, and to my co-advisor Eng. Rui Gomes for believing in me, for motivating me, and for the good advices. Without them, this thesis could not been written.

I want to thanks to my parents for supporting me all these years, and specially to Juliana Azevedo and Mafalda Azevedo who are the best that I have in my life. Also, I want to thanks to Mauro Rodrigues for being always on my side during these years, but specially in this semester. Without them I could not overcome my mental health, and recover the happiness and motivation that I always had.

I am grateful to the doctors and nurses who helped me and gave their best to my quick recover, without them I could not do this thesis in this semester.

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Finally, I am grateful to the professors who supported me, contributing to my graduation.

Ília Azevedo

"É a vida que segue
E não espera pela gente
Cada passo que dermos em frente
Caminhando sem medo de errar
Sei que o melhor de mim
Está para chegar "

Mariza

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Abbreviations And Acronyms

ADPLL	All-Digital Phase-Locked Loop
CMOS	Complementary Metal-Oxide Semiconductor
CP	Charge Pump
DAC	Digital-to-Analog Converter
DLL	Delay-Locked Loop
DNL	Differential Non-Linearity
DPA	Digitally Modulated Power Simplifier
DSM	Delta-Sigma Modulator
DSP	Digital Signal Processing
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
EVM	Error Vector Magnitude
IC	Integrated Circuit
INL	Integral Non-Linearity
IoT	Internet of Things
LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look-Up Table
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PA	Power Amplifier
PCW	Phase Code Word
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
PM	Phase modulator
SoC	System-on-Chip

Chapter 1

Introduction

The concept of the IoT [1], [2] has drawn the attention of the research community with the end goal of ensuring that wearables, sensors, smart appliances, washing machines, tablets, smartphones, smart transportation system, and other entities are connected to a common interface with the ability to communicate with each other [3]. The IoT paradigm does not set any constraint on the type of technology used to connect the end devices to the Internet, it is a fact that wireless communication is the only feasible solution for many IoT applications and services. To ensure a low cost implementation of these systems a good approach would be the CMOS technology. However, this technology is proper for the digital domain but for RF it has a lower efficiency. Thus, several wireless communication systems [4],[5] can be applied, such as Near Field Communications (NFC) [6], Short-range passive and active Radio Frequency Identification (RFID) systems [7], Bluetooth-based systems, including Bluetooth Low Energy (BLE) [6],[8], systems based on the family of IEEE 802.15.4 standards like ZigBee [6],[8], 6LoWPAN [9], and Thread-based systems [10]. To ensure the connection with this massive devices and services it is used the next generation 5G mobile networks [3], such as enhanced Mobile Broadband (eMBB) [11], massive Machine Type Communications (mMTC) [12], Critical Communications and Network Operations. It is important to emphasize that these 5G mobile network can support the basic communication requirements, such as high throughput, low latency in terms of data delivery, high scalability to enable massive number of devices, efficient energy consumption technique and the provision of ubiquitous connectivity solution for end-users.

1.1 Problems Context

The use of 5G mobile network increases the search for higher data rates transmission over mobile or wireless channels. To ensure an efficient transmission it it is necessary a type of modulation with higher bit rate to support the multiple devices. Also, it is fundamental to reduces the symbol interference, once the symbol duration reduces with the increase of the data rate, and dispersive fading of the wireless channels will cause more severe intersymbol interference (ISI) if single-carrier modulation, such as in time-division multiple access (TDMA) or Global System for Mobile

Communications(GSM).

Thus, in OFDM [13],[14],[15] the entire channel is divided into many narrow-band sub-channels, which are transmitted in parallel to maintain high-data-rate transmission and, at the same time, to increase the symbol duration to combat ISI. However, OFDM has high peak to average power ratio which decreases the transmitter efficiency.

A crucial part of the wireless device is the radio transceiver. It consists of a receiver and a transmitter. In transmitter systems an important requirement is the efficiency [16]. For example, increasing battery life in portable devices and decreasing dissipated power in base stations are the driving forces in developing efficient systems. Architectures like envelope tracking (ET), which utilizes linear power amplifiers, and envelope elimination and restoration (EER), that utilizes switched-mode power amplifiers are now of great interest. The reason for this is that both of these can improve the efficiency of the transmitter system in power back-off.

Thus, a great solution to this problem are polar transmitters [17]. More specifically, the design of digitally modulated power amplifiers (DPAs) which brings many benefits over the counterpart approach (i.e. analog centric design), such as enhanced reconfigurability, multi-mode operation, lower complexity and higher system efficiency by integrating in advanced CMOS nodes both the baseband and RF front-end.

1.2 Motivation

Polar architecture [18], represented in Fig. 1.1, is a good candidate to mitigate the compromise between linearity, efficiency and system complexity. Such architectures require phase and envelope modulator with wider bandwidths than their Cartesian counterparts.

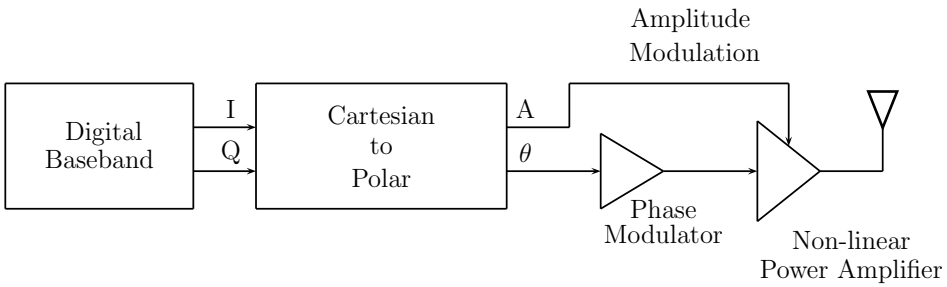

Figure 1.1: System Level Representation of a Polar Transmitter

Polar transmission utilizes envelope and phase component to represent the digital symbols instead of the conventional I/Q format. The baseband signal *V(t)* is split into the envelope signal *A(t)* and the phase signal θ(t).

$$V(t) = I + jQ \tag{1.1}$$

$$A(t) = \sqrt{I^2 + Q^2} \tag{1.2}$$

$$\theta(t) = tan^{-1}\left(\frac{Q}{I}\right) \tag{1.3}$$

From these equations, is possible to conclude that the original complex signal V(t) can be restored from a phase-only signal multiplied with its envelope at the PA. This polar modulation process is also known as EER. However, polar architectures cause significant challenges in the design of the transmitter. Namely, the delay mismatch between the envelope and phase paths can cause significant spectral re-growth as well as an EVM increase in the transmitted signal. Therefore, a way to calibrate the delays in both paths is required to cover inevitable variations over process such as voltage and temperature (PVT). Another important drawback is the significant bandwidth extension caused by the non-linear Cartesian to polar transformation, which imposes severe operational constraints on the DPA.

Digitally modulated transmitters are currently being exploited in CMOS technology. Contrasting with analog (i.e. traditional) approach, digitally intensive techniques can resort to improve capabilities of smaller CMOS nodes, which permits the integration on the RF front-end with the digital signal processing (DSP) block in a single low-cost technology. To take advantage of increased CMOS switching speed, polar transmitter can be adopted. In this sense research and development of phase modulators in CMOS can take advantage of digitally-assisted techniques.

1.3 Problem Statement

There are several architectures that allow us to perform phase modulation. One of the possibilities is the usage of an all-digital phase-locked (ADPLL) [19]. However, in highly integrated system-on-chip (SoC), it is preferable to have a single ADPLL providing a global clock to the different blocks. This, in turn, automatically increments the system complexity due to a variety of very well-known problems, such as oscillator injection locking, increased substrate noise, and area overhead. Thus, the carrier phase modulation should be performed on a single self-contained block. This block is an RF phase modulator that receives the digital phase part from the decomposition of digital I and Q signals in their polar representation. Then it gives an output with the phase carrier modulated.

There are mainly two different approaches, the fully-digital and the mixed-signal. The topology based on fully-digital phase modulator can lead to a high power consumption and could be necessary the implementation of additional components leading to an increasing of system complexity. The topology mixed-signal that are composed essentially by DACs and mixers suffers from gain and delay mismatches, a huge occupied area, and could have a power phase resolution. Also, there are problems about parasitic capacitances and resistances which can cause an undesirable signal output.

1.4 Thesis Objectives

The main goal of this project is to study and design a dedicated digitally-controlled phase modulator block for polar transmitters. Due to the importance of power consumption in the whole system, the block has to be a mixed-signal. The architecture has to be designed in order to have a high resolution, occupy the smallest area as possible, and the most important, have a low power consumption. After deciding the ideal architecture in order to satisfy those requirements, a design must be performed in order to execute a phase modulator. To accomplish this, it is necessary to understand the main goal of a phase modulator, get familiar with the most common typologies of RF phase modulators.

In short, the main objectives are:

- The phase modulator should support 1GHz operation.
- The system has to have a 5 bit resolution.
- The work must consume the lower power consumption possible.
- Implement and design the phase interpolator for this work with an acceptable power consumption.
- Implement a quadrature clock divider and a signal selector.
- Implement the layout of the phase modulator.

1.5 Document Outline

The chapter 2 describes various architectures to perform phase modulation in a transmitter. Their advantages and disadvantages are in considered, and their properties are summed and compared on a table.

The chapter 3 clarifies the phase modulator concept concept that will be adopted to this work. Also, details the working principle of the phase modulator where it is included a mathematical approach and its results. Still, it is explained how the fundamental cell of the phase interpolator was designed and implemented, and its results from Virtuoso Simulator.

The chapter 4 includes the phase modulator implementation at transistors level. First, it describes the design and the implementation final phase interpolator, including its results. Also, considerate some parameters of the phase interpolator which contributes to the improvement of the output phase. After that, shows the architectures that implements the differential quadrature clocks and its results, and shows the design of the signal selector and its results. In the end, there are represented the results of the phase modulator obtained, such as its output phase in 360 degrees, its power consumption and linearity measurements.

Finally, the chapter 5 concludes the thesis with some discussion of the future work.

Chapter 2

Phase Modulator Architectures

The phase modulation (PM) [20] is a crucial component of today's highly efficient polar DPAs, since it provides the necessary generation of a phase modulated RF carrier encoded with the base-band data.

A phase modulator [21] must handle a signal that is significantly bandwidth expanded due to the nonlinear transformation from an I/Q representation to amplitude/phase. Therefore, many architectures have been published in the literature in order to respond to such requirements.

This chapter briefly overviews some of the main approaches to implement phase modulators, which will serve as the bases for the solution to be investigated in this dissertation. It will be focused only the phase component, due to the fact that the desired design will be integrated with an amplifier that reform the amplitude component.

2.1 Cartesian Phase Modulator

The core component of Cartesian phase modulator [22], in Fig. 2.1, is the high-resolution I/Q phase interpolator. It corresponds to the two DACs and the mixers, where, after signal summation obtains the desired phase modulated signal.

The quadrature inputs are generated by the carrier frequency sine-wave. Then the differential current DACs, which are controlled by 8 bits, will determinate the differential current in order to implement the I/Q weight. Then, to obtain a signal phase modulated the signals I/Q-LO that has a 90 degrees difference, are summed.

Although quite simple, this architecture suffers from gain and phase mismatches. Also, improving the phase resolution provided by the mixers implies doubling the number of elements in the current DAC and therefore the power required will be higher. Also, due the harmonics arising from the nonlinear switching actions in the Gilbert core, the phase linearity is degraded.

It operates from 1.2/1 V supplies, delivers 16.8dBm average power, and 247mW of power consumption.

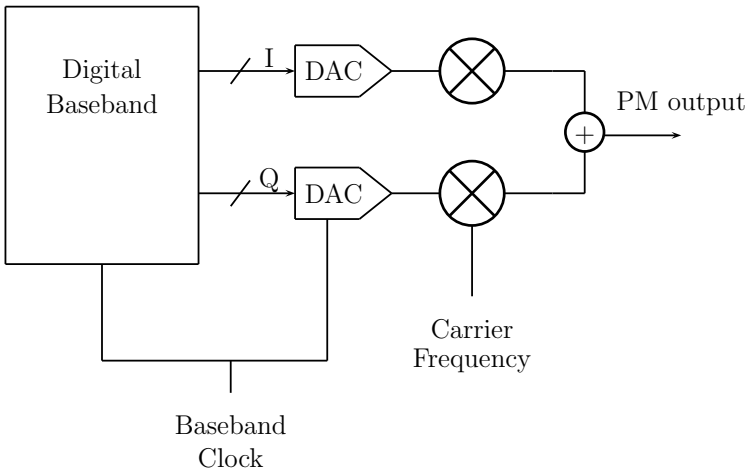

Figure 2.1: Cartesian Phase Modulator

2.2 Phase Modulator with Discrete Carrier Pre-Rotation

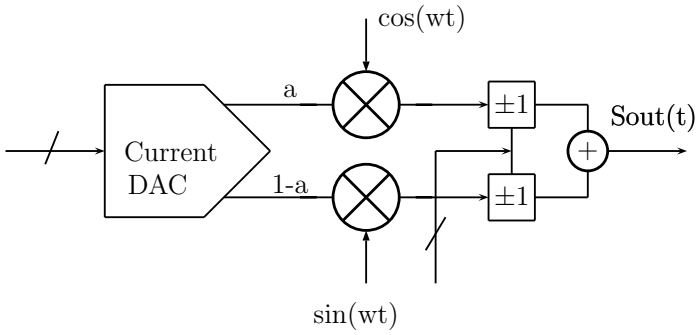

Figure 2.2: Block Diagram for Single DAC

This architecture, in Fig. 2.2, presents a digital-to-RF phase modulator [23]. This approach is related to those used in [24] and [25] to reduce the number of required current cells over the more conventional approach of [26].

The principle of working is similar to the Cartesian phase modulator, but it only has one DAC,

which means that it occupies less area. It works on the principle of vector addition, where the output is generated by summing weighted components of sine and cosine. This functionality can be represented as *Sout(t)* = $\pm$*acos(wt)*$\pm$ *bsin(wt)*. To perform the *a* and *1-a* values, a current-steering DAC is used, which is controlled by digital input ϕ [1:9] that will select the corresponding current-steering to provide them. Then the multiplication of *a*cos*(wt)* and (1-*a*)sin*(wt)* is performed. After that a phase quadrant is chosen by multiply the previous results by +1 or -1. Hence the output signal is performed.

Compared to the previous, this approach provides a higher phase resolution.

This architecture was designed to a 2.5GHz carrier frequency, a 200MSPS sample rate, 12 bits phase resolution and a 65nm CMOS technology.

2.3 Phase Modulator using resonant low-Q

This proposed architecture for phase modulator is represented in Fig. 2.3. This approach, which is an improvement of [27], is known as a fast settling phase modulator [28] which targeted a outphasing system and was implemented in 65nm CMOS.

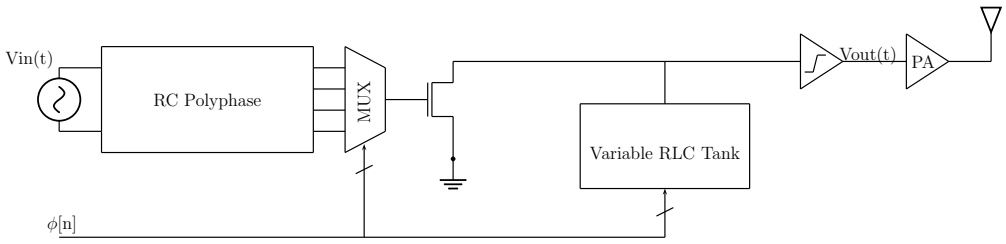

Figure 2.3: Phase Modulator Using Resonant Low-Q

It is a simple architecture composed by two-stage RF polyphase filter [29], a multiplexer and an RLC tank. In order to perform the phase modulation, a differential RF signal is divided into four quadrants using a two-stage polyphase filter. One of those phases will be selected using the 4:1 multiplexer, and then the signal will be phase shifted by a desired amount thought the use of a varying switched capacitor bank acting as part of a resonant RLC tank. The relevant component of this architecture is the RLC tank [30], in Fig. 2.4, which receives the carrier phase positioned in one of the four quadrants.

The capacitor value for the center frequency is fixed, and then is defined a minimum and a maximum value which depends on the tank's factor quality, which in turn depends on the carrier frequency. Thus, by adjusting this parameter a phase coverage of 90 degrees is guaranteed. Therefore, the output signal has a phase offset in relation to the input signal, that proportionally varies with the capacitor value, and the desired phase modulation is performed. The quality factor determines the inclination of its response, in this way is required only a small change in absolute capacitance value to cover the entire quadrant.

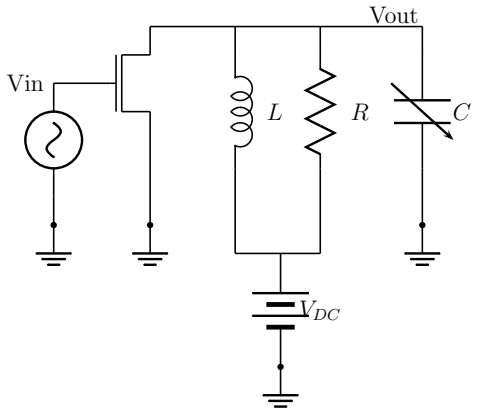

Figure 2.4: RLC Tank

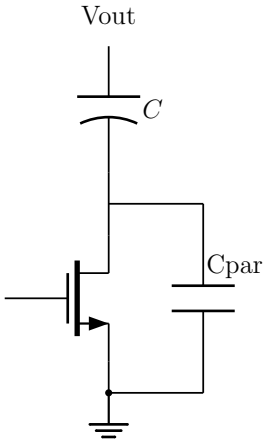

Figure 2.5: Switched Capacitor Element Cell

The system, has a switched capacitor, in Fig. 2.5, which allows varying the capacitance value. It consists of a fixed capacitance, which needs to be controlled, and also of a variable capacitance, which will generate the desired phase modulation. To control the values of both capacitance has used an array of values where each element represents an effective capacitance depending on the control voltage, which opens or closes the NMOS switch.

For this system, there is no need for high frequency selectivity, so it has not a high power consumption. However, there are some inconveniences about the carrier frequency. For lower

frequencies, the component large size will be prohibitive for integration in silicon, however, for very high frequencies, it is possible to encounter the problem of very low required component values overshadowed by the circuit intrinsic parasitic value, and there is another limiting factor which is the unit size of a reliable switched capacitor unit cell, that requires a balance with the number of resolution bits for a specific application.

Also, there are several second-order effects due to non-linearity and non-idealities. The most important is the increasing of parasitic capacitances and resistances, the smaller the quality factor. This aspect causes distortion in the output signal. Another problem is the fact that ideally the desire input carrier frequency has to be a pure sine wave, and in reality that signal has harmonics. This, will result in a different phase shift at different frequencies, however, this effect is not important since the tank itself provides some attenuation, and the receiver operates around the center frequency.

This design a 80MSamples per second, is controlled by 12 bits, has a -27dB EVM, 5mW power composition, occupy a 0.22mm^{2}of area, and has a 65ηm technology.

2.4 Open Loop Phase Modulator

The open-loop phase modulator [31] consists in a phase generator, a multiplexer and a digital control logic. The phase generator receives a signal at the carrier frequency from a phase-locked loop (PLL) and generates multiple sub-phases, and then, with the control of digital logic, which decodes transmission data ϕ[n] at the clock frequency, a sub-phase is selected to get the desired phase modulated output signal.

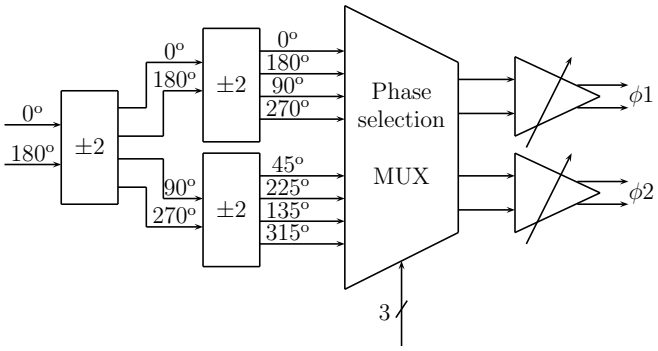

Figure 2.6: Octant Phase Interpolator

In this architecture, represented by Fig. 2.6, the phase generator is divided in an octant phase interpolator and a sub-octant phase interpolator. The first one is generated by dividing the carrier signal by two-stage CML dividers. Then, the multiplexer selects two differential signals in 45 degrees phase difference to provide the input to 9 bit sub-octant interpolator [32].

The sub-octant interpolator is composed by a phase interpolator, represented in Fig. 2.7, whose output varies from the two input differential phases in 45 degrees as the current weight differs on M1 and M2 transistors, which is handled by a digital control current weight and should be updated at the clock frequency. The shared source of the two NMOS improves the speed of current switching which is fundamental to avoid a phase offset and non-linearity.

The sub-octant interpolator is composed by a phase interpolator based on current summation [33], whose output phase varies accordingly to the weighted current sum of two 45 degrees phase off-setted RF carriers.

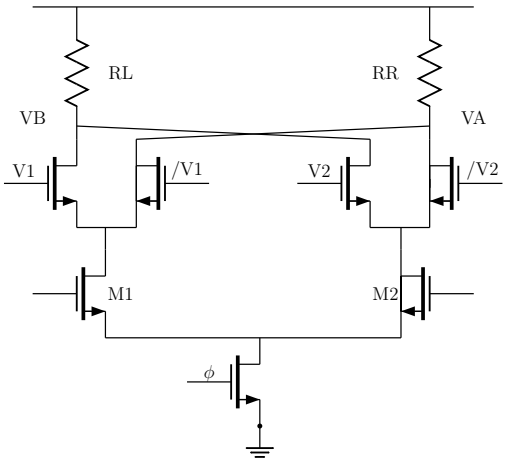

Figure 2.7: Sub-Octant Interpolator

The input differential signals at the interpolator are responsible for the phase resolution of this architecture. Since the output phase is swept from 45 degrees phase difference, because of dividing the carrier phase in 8 sub-phases, a better phase resolution is provided, instead of dividing only in 4 sub-phases, i.e. classical quadrature approach.

This system is crucial when it comes with the current font sizing, because it is inversely proportional with the non-linearity in output. Thus, to have a low DNL (Differential Non-Linearity) it is necessary a greater area.

This design has a 150MHz bandwith, a 2.5GHz carrier frequency, and a 300MHz switching frequency. It was implemented in a 65ηm technology and has a 12 bit control where 3 of them controls the phase selection, and 9 controls the phase interpolator.

The simulation results to 2.5GHz carrier frequency and 12-bit, reveal that the phase modulator consumes 14mA from 1.0V supply. Its DNL is in between -0.55 and 0.32 when 1 LSB is 167fs. The jitter is 178fs, rms (-54dBc) which is 8-7-bit ENOB. And the area consumption is 0.9mm^2.

2.5 Closed-Loop tapped delay line phase modulator

The following architecture, represented in Fig. 2.8, is a new fully digital architecture [34] for an RF phase modulator with significantly improved phase resolution. It is mainly composed by a delay-locked loop (DLL), a delta-sigma modulator (DSM) which is built by N delay elements and a local oscillator, a phase frequency detector (PFD), a charge pump (CP), a LPF, and a multiplexer N to 1.

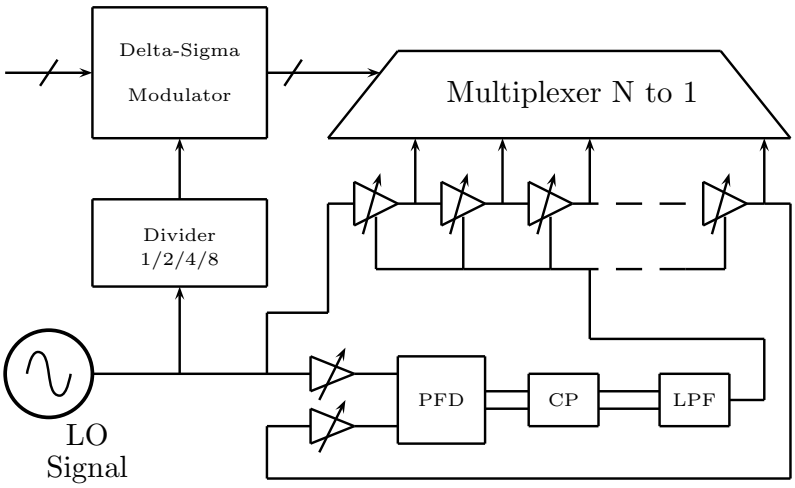

Figure 2.8: Closed Loop Tapped Delay Line Phase Modulator

The input phase comes from the baseband processor with 10-bit resolution at the carrier frequency. The output of the DSM corresponds to five output bits with higher rate than the input data, which will be as a controller to the multiplexer. In this way, the multiplexer will select different taps according to high speed data that is given. Thus, the DSM block is responsible for increasing the effective phase resolution of the phase modulator.

The 32 to 1 multiplexer is used to select different values of the DLL according to the baseband digital phase data to achieve the desired phase modulated signal at the output. To avoid phase distortion, it is necessary to have the same delay from each input tap to the multiplexer.

The DLL maintains 2π phase difference at the input of PFD, with two variable delay lines with two external controls, to provide a phase difference between the input of the first and the output of the last delay elements remains exactly 2π across the whole carrier frequency band. This difference is measured by the PDF. Then, the CP is used to provide appropriate control voltage for the variable delay chain over the whole carrier frequency range.

Thus, since the delay chain provides N discrete phase steps, and the DLL forces 2π phase shift across the delay chain, the phase resolution equals 2π/N. An important detail is that without the PFD the DLL does not guarantee 2π across the all delay lines or equivalently 360^o/N phase shift for each delay tap.

Since a phase modulator requires a wide bandwidth, this topology has a good advantage because it performs in a bandwidth between 1GHz and 3GHz.

The innovator block of this architecture is the DSM block which improves the system performance, and consume less than 5% of the whole chip DC power consumption.

Also a disadvantage is that since the DPM chip works at frequencies up to 3GHz, and since it includes many digital gates, particularly in the delay chain and multiplexer which use large devices, generating higher power consumption. The design has a 45nm technology, an RF frequency between 1 and 3GHz, the area occupied was 0.15 mm^2 , the signal bandwidth is 20Mb/s, a -33.5dB EVM , and a 34mW of power consumption.

This architecture offers a better phase modulation bandwidth, and offers the lowest power consumption compared with the other designs.

2.6 Phase Interpolators

There are some recent projects that use the phase interpolator to implement a phase modulator, such as [35] where it is designed only one basic cell which is replicated N times, where N is the bit resolution. This approach occupies a large amount of area, since the number of the replicated cells in each quadrant is equal to the number of bits of control. In referring article there are 9 control bits and four quadrants, which lead us to conclude that there are 36 unit cells replicated. The approach in [36] has a different design avoiding the LO feedthrough, but also the unit cell is multiplied. Also in [37] the concept is the same. Although these solutions have a good concept, the replication of the unit cells will consume a high power due to the parasitic capacitors in layout.

2.7 Conclusions

To provide optimum signal reconstruction the phase modulator must manage wide bandwidth signals while keeping at a minimum both the complexity and power consumption. Also, it is necessary a fast settling time for use in high data-rate outphasing transmitters.

The cartesian phase modulator [22] suffers from the gain and phase mismatches as well as increased power consumption for a higher phase resolution. Also, the phase linearity is degraded.

To phase modulator with discrete carrier pre-rotation [23], the problems are the same, but this architecture has an advantage by improving the occupied area, since it is composed by only one DAC.

An interesting architecture is the phase modulator using resonant low-Q [28], however, it has problems in fabrication when it comes with too small or too large frequencies. Also, due to a low quality factor there are a among of parasitic capacitances and parasitic resistances that will affect the phase modulation. Another issue is that it is designed for pure sine wave input, and in reality there are harmonics in input signal which will cause a different phase shift at different frequencies. Also, the advantage of this approach is that it is possible to adjust the capacitor size according to the desired carrier frequency. Despite being an interesting approach, it will not be a reference to this work, since the RLC tank has a coil which contributes to the increasing of the area.

The open loop phase modulator [31] whose non-linearity in the output is inversely proportional to the current font size. Thus, having a low DNL implies a great area. The disadvantages from this architecture when applied to this work, are the phase selector which is a multiplexer 8:1 which means a great power consumption, and its 10Gb/s clock generator.

The last architecture is a fully digital topology [34] which does not correspond to the desired design. Despite having a DSM block which has a low power consumption, the switching in N-1 multiplexer will increase it. Also, this architecture uses a PLL whose components have to be carefully designed, implying an extra work and time to this project.

Despite of these disadvantages, a proper topology for this polar transmitter is the open loop phase modulator, which provides a good phase resolution, and a low non-linearity, and has an ideal power consumption.

Table 2.1: Architectures comparison

Phase Modulator Architectures	Carrier Frequency (GHz)	Sample Rate (MHz)	Phase Resolution (bits)	Power (mW)	Area $(mm)^2$	Supply Voltage (V)	Technology
Cartesian - 2013 [22]	1	200	9	9	N.A	1.2	65nm
Discrete carrier - 2011 [23]	2.5	200	10	1.9	0.26	1	65nm
Resonant Low-Q - 2014 [28]	0.416	80	9	5	0.22	1	65nm
Open Loop - 2013 [31]	2.5	150	9	14	0.9	1	65ηm
Digital Closed Loop - 2017 [34]	2.4	200	5	34	0.15	1	45nm

The table 5.1 shows an overview of the different architectures from the literature.

Chapter 3

Phase Modulator Architecture

3.1 Phase Modulator Concept

The approach chosen for this work was the open loop phase modulator [31], but with a different architecture since the aim of this design is to implement a phase modulator with a good trade-off between power consumption and resolution.

The fig.3.1 is the architecture of this work which consists in three main blocks, the quadrature signal generator, two signal selectors, and the phase interpolator. It was decided that the phase interpolator will receive two signals in quadrature allowing the use of only one clock generator. The differential multiplexer 8:1, from the open loop phase modulator, will be substituted by two differential multiplexers 2:1 to avoid the need to switch between eight RF signals and the use of a high number of transmission gates. Thus, this solution will use a lower number of transmission gates, because it only needs to switch two RF signals in each differential multiplexer. In this way, the power consumption of the phase modulator can be reduced.

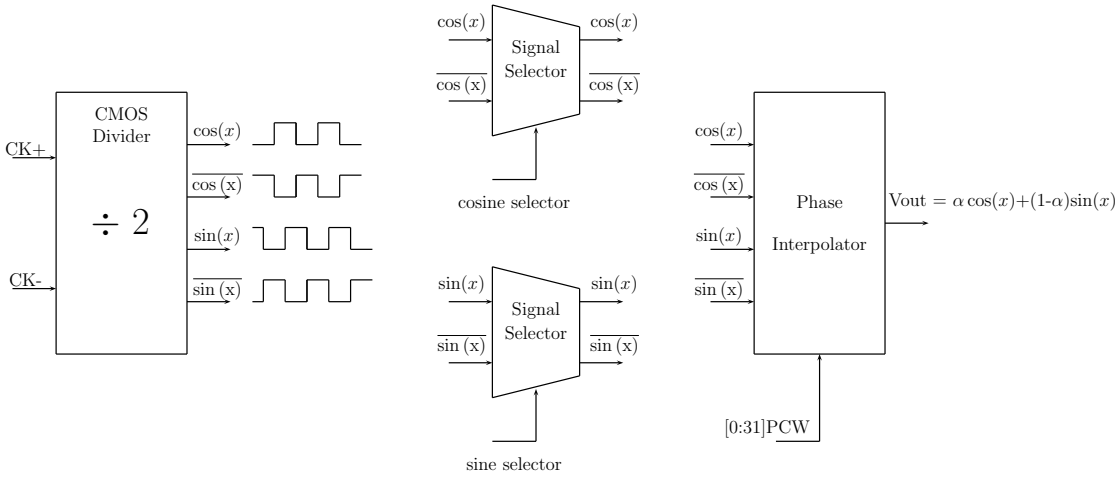

Figure 3.1: Phase modulator architecture

3.2 Phase Interpolator: Working Principle

The main block of this architecture is the phase interpolator once the performance of the phase modulator depends on it. So, it is important to size it with suitable values to get a good performance, and good values of static performance metrics, such as the linearity.

A general idea of how this phase interpolator works, can be interpreted with an unit circle, represented in Fig. 3.2. Initially, it receives two quadrature signals, which are used to select one quadrant from the unit circle, then the imposed current weight, represented by α, will represent the angle between the input signals to select the desired output phase. In this way, the resulting output signal will be the sum of those input signals whose both magnitude and phase depends on the current weight, $\alpha\cos(x)+(1-\alpha)\sin(x)$

With the Fig. 3.3 it is possible to verify the relation between the input signals and the current weight. Each signal has its own phase, $\phi 1$ and $\phi 2$ which have a 90 degrees difference, and depending of the α the resulting signal will be between these two signals.

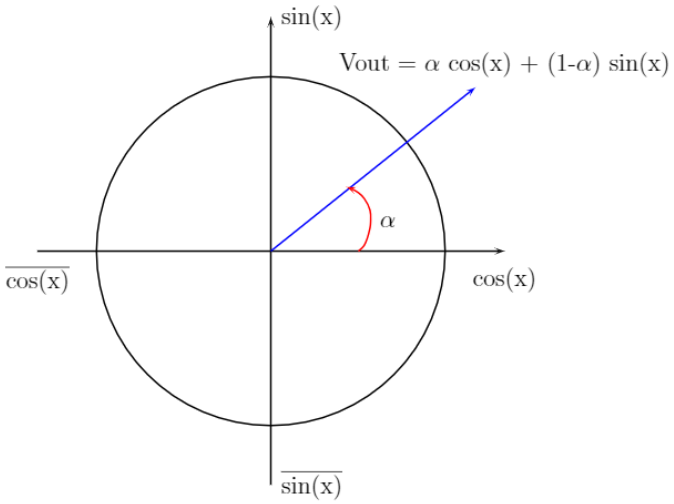

Figure 3.2: General concept of phase modulation by the summing of two out-of-phase signs

As the phase interpolator receives four differential quadrature clock signals, the range to choose an output phase with a current weigh value is 90 degrees, which is equivalent to one quadrant of the unit circle. With this approach it is possible to select a desired quadrant by inverting the received signals, allowing a phase modulation over the unit circle, in 360 degrees.

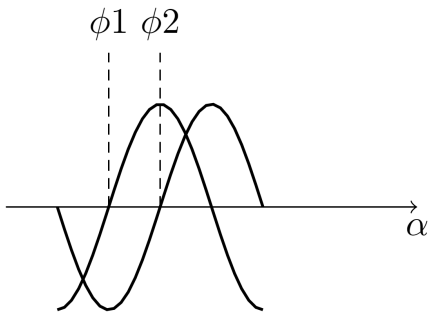

Figure 3.3: Current Shifting

3.2.1 Schematic Level Concept

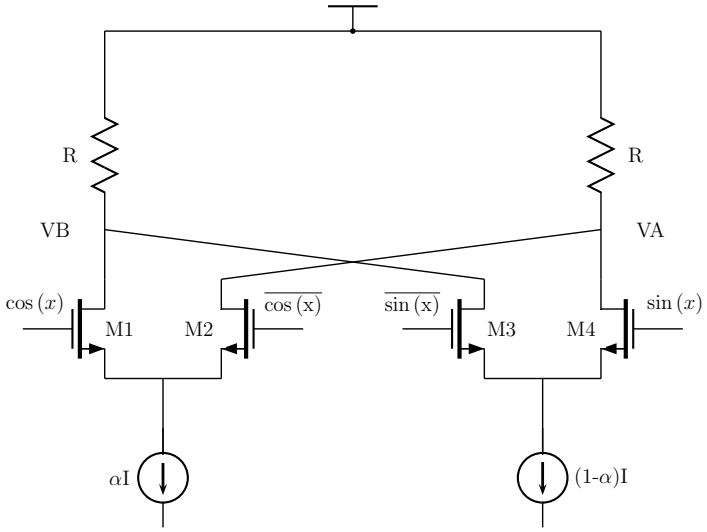

Figure 3.4: Phase Interpolator Concept

The idea of the phase interpolator is represented Fig. 3.4, where it is possible to verify the two differential pairs which will receive the four input RF signals. It is important to emphasize that each differential pair does not receive two quadrature input signals, but receives two signals with the same phase but with different polarities. To sink the current weighted to the differential pairs an NMOS transistor will act like a current bias which is represented in the figure.

The four differential quadrature RF signals are responsible for switching the transistors M1, M2, M3 and M4, represented in Fig. 3.4 between ON or OFF, causing four different performing situations. The Fig. 3.5 represents those signals, and all possible situations which can determinate the output signal of the phase interpolator.

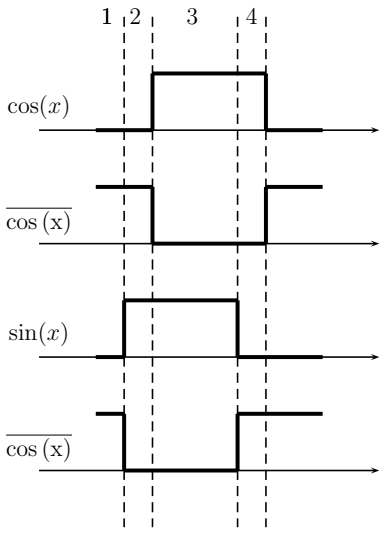

Figure 3.5: Four situations caused by the four differential input RF Signals

To estimate the output amplitude and phase output resulted from this interpolator, it is necessary to use trigonometric identities to find an expression which depends on the current weight, represented by α and on the $\sin(x)$ and $\cos(x)$ which represents the RF quadrature input signals.

$$a\sin x + b\cos x = c.\sin(x+\phi) \tag{3.1}$$

$$where: \quad c = \sqrt{a^2+b^2} \tag{3.2}$$

$$\phi = \arctan(b,a) \tag{3.3}$$

So, with (3.2) and (3.3), it is possible to determinate the desired expressions, but first, it is necessary to obtain the output signal expression according to (3.1).

$$\overline{\sin(x)} = \sin(x+180) \tag{3.4}$$

$$\cos(x) = \sin\left(x+\frac{\pi}{2}\right) \tag{3.5}$$

$$\overline{\sin(\mathrm{x})} = \cos\left(x + \frac{\pi}{2}\right) \tag{3.6}$$

Another important trigonometric properties, to achieve an output expression with the format (3.1), are (3.4), (3.5), and (3.6).

Also, is it important to mentioned that the output signal results of the difference of the output from the differential pairs output, (3.7).

$$Vout = VA - VB \tag{3.7}$$

According to the four situations referred in fig.3.5, it is possible to detach the circuit in fig.3.4 to help to estimate the output signal expression.

The Fig. 3.6 represents the first situation caused by the input signals, where there the transistor M2 and M3 from Fig. 3.4 are ON, since the input signals $\overline{\cos(\mathrm{x})}$ and $\overline{\sin(\mathrm{x})}$ are high. Analyzing this figure, the VA voltage can be estimated by (3.8) and the VB voltage by (3.9), after that, using (3.7), the output signal can be estimated achieving the result in (3.10).

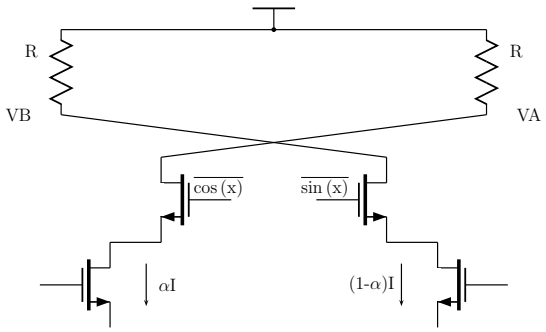

Figure 3.6: First situation

$$VA = VDD - \alpha IR\overline{\cos(\mathrm{x})} \tag{3.8}$$

$$VB = VDD - (1-\alpha)IR\overline{\sin(\mathrm{x})} \tag{3.9}$$

$$Vout = (1-\alpha)IR\overline{\sin(\mathrm{x})} - \alpha IR\overline{\cos(\mathrm{x})} \tag{3.10}$$

The Fig. 3.7 represents the second situation, where the cosine and negative sine signals are high, turning the transistors M1 and M3 ON.

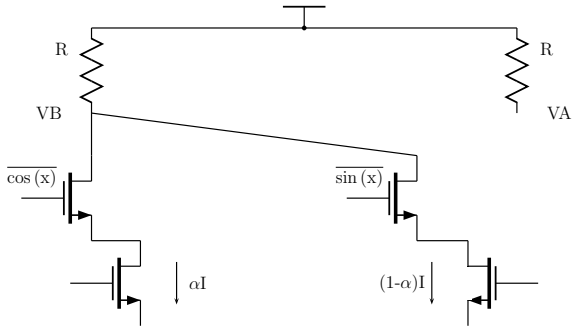

Figure 3.7: Second situation

Such as in the previous approach, the output signal can be estimated in the same way. The results (3.11), (3.12) and the most important, (3.13) are the expressions achieved in this situation.

$$VA = VDD \tag{3.11}$$

$$VB = VDD - [\alpha IR\cos(x) + (1-\alpha)IR\overline{\sin(x)}] \tag{3.12}$$

$$Vout = \alpha IR\cos(x) + (1-\alpha)IR\overline{\sin(x)} \tag{3.13}$$

The Fig. 3.8 represents the third, when the cosine and sine signals are high turning the transistors M1 and M4 ON and the transistors M2 and M3 OFF.

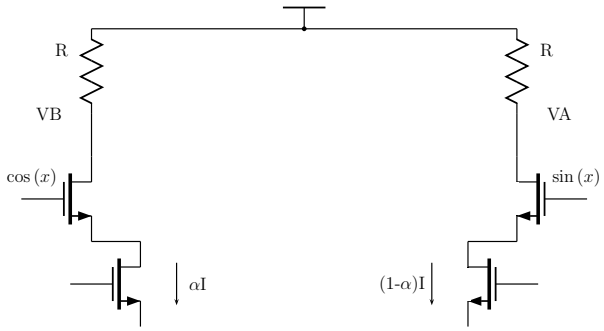

Figure 3.8: Third situation

In this case it was used the trigonometric property (3.17) to manipulate the resulting output signal expression (3.16) from (3.14) and (3.15) to get the desired result represented in (3.18).

$$VA = VDD - (1-\alpha)IR\sin(x) \tag{3.14}$$
$$VB = VDD - \alpha IR\cos(x) \tag{3.15}$$
$$Vout = \alpha IR\cos(x) - (1-\alpha)IR\sin(x) \tag{3.16}$$
$$-\sin(x) = \overline{\sin(x)} \tag{3.17}$$
$$Vout = \alpha IR\cos(x) + (1-\alpha)IR\overline{\sin(x)} \tag{3.18}$$

The Fig. 3.9 represents the final possible performing situation of this interpolator. In this case, the negative cosine a sine signals are high, turning the M2 and M4 transistors ON.

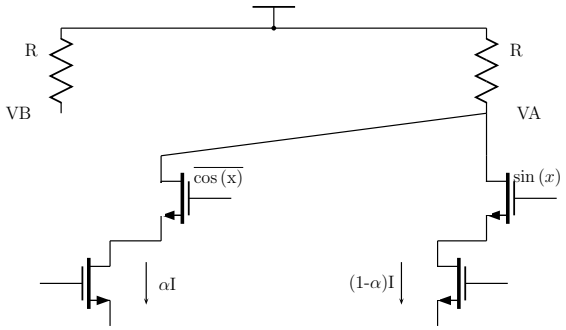

Figure 3.9: Fourth situation

It was estimated the output signal in the same way but using the properties (3.22) and (3.23). Thus, the final result obtained was (3.24).

$$VA = VDD - [\alpha IR\overline{\cos(x)} + (1-\alpha)IR\sin(x)] \tag{3.19}$$
$$VB = VDD \tag{3.20}$$
$$Vout = -\alpha IR\overline{\cos(x)} - (1-\alpha)IR\sin(x) \tag{3.21}$$
$$-\sin(x) = \overline{\sin(x)} \tag{3.22}$$
$$-\overline{\cos(x)} = \cos(x) \tag{3.23}$$
$$Vout = \alpha IR\cos(x) + (1-\alpha)IR\overline{\sin(x)} \tag{3.24}$$

If all final results are compared, it is concluded that in all situations the output signal expression is the same. So, to this formula, will be applied following trigonometric identities to achieve the signal magnitude and phase.

$$\overline{\sin(x)} = \sin(x+\pi) \tag{3.25}$$

$$\cos(x) = \sin\left(x+\frac{\pi}{2}\right) \tag{3.26}$$

It is possible to conclude that

$$Vout = \sqrt{(\alpha IR)^2 + ((1-\alpha)IR)^2}\arctan\left(\frac{\alpha}{1-\alpha}\right) \tag{3.27}$$

Based on (3.27), it can be verified that the signal amplitude will vary according to the current weight. Also, as expected, the output signal phase will be depend on the current weight values. Thus, applying these formulas, it is possible to estimate the dependency of phase and magnitude to the current weight. To get this dependency, it was simulated in MATLAB software these expressions and Fig. 3.10 was obtained, which indicates, how can output phase vary with the current weight. Also, it can be concluded that the output phase vary in a specific range with the current weight.

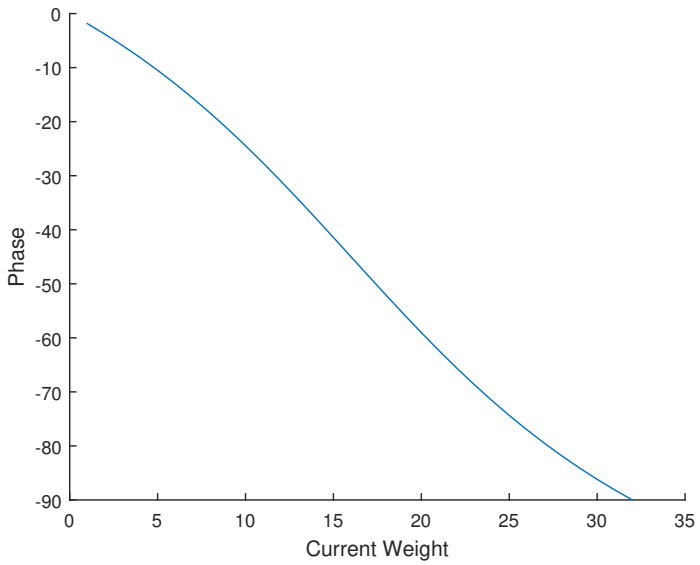

Figure 3.10: Phase vs Current weight

Also, it was obtained the Fig. 3.11 where it is possible to confirm a little amplitude variance with the current weight. As expected from (3.27) the amplitude is maximum for the maximum and minimum current weight values, and is minimum for the average value of the current weight.

In Fig. 3.12 is represented the theoretical output signals from phase interpolator, assuming all higher order harmonics are short-circuited. Here, it is possible to observe the phase shift of the output signals, which evidence that the output signal phase will be between the phase of the input

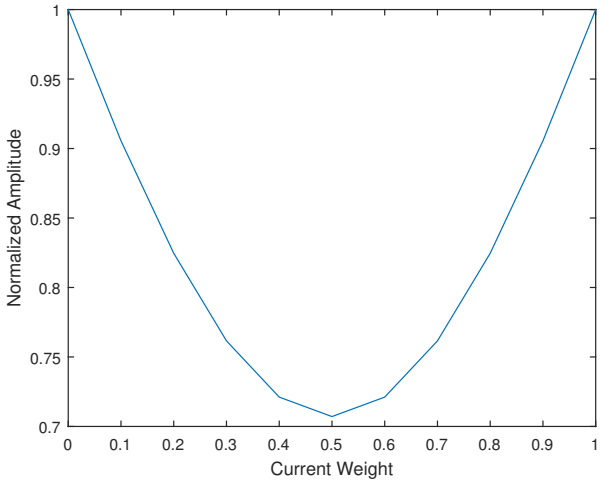

Figure 3.11: Amplitude variation

signals has mentioned previously. Also, it can be seen signals with different amplitude, which confirms the previous result.

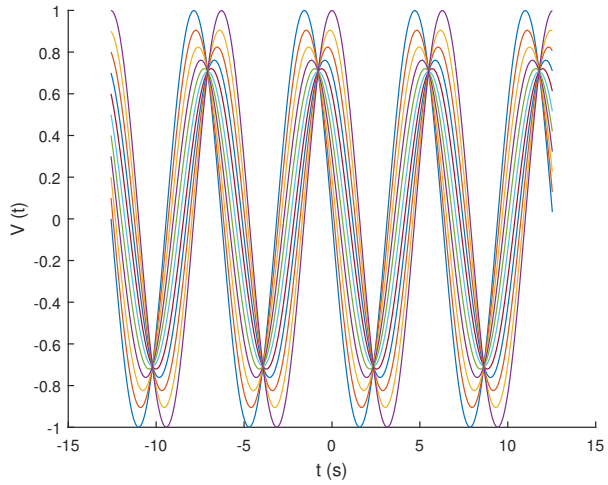

Figure 3.12: Output Signals to all Current Weight Values

By analyzing the way the phase interpolator performs, it can be concluded that there are four possible working conditions of this circuit, due to the different voltages of the input signals at a time. Thus, the output signal expression for each situation was estimated to know if the result is always the same or not. After comparing all results obtained it was concluded that the output signal phase and amplitude varies with the current weight. These results are useful to know the results expected from the phase interpolator which will be implemented with a 180nm CMOS technology, in Cadence Virtuoso IDE. Also, these results will be compared to future results from schematic and layout simulations, in order to understand the limitations that this circuit can impose.

3.2.2 Fundamental Phase Interpolator

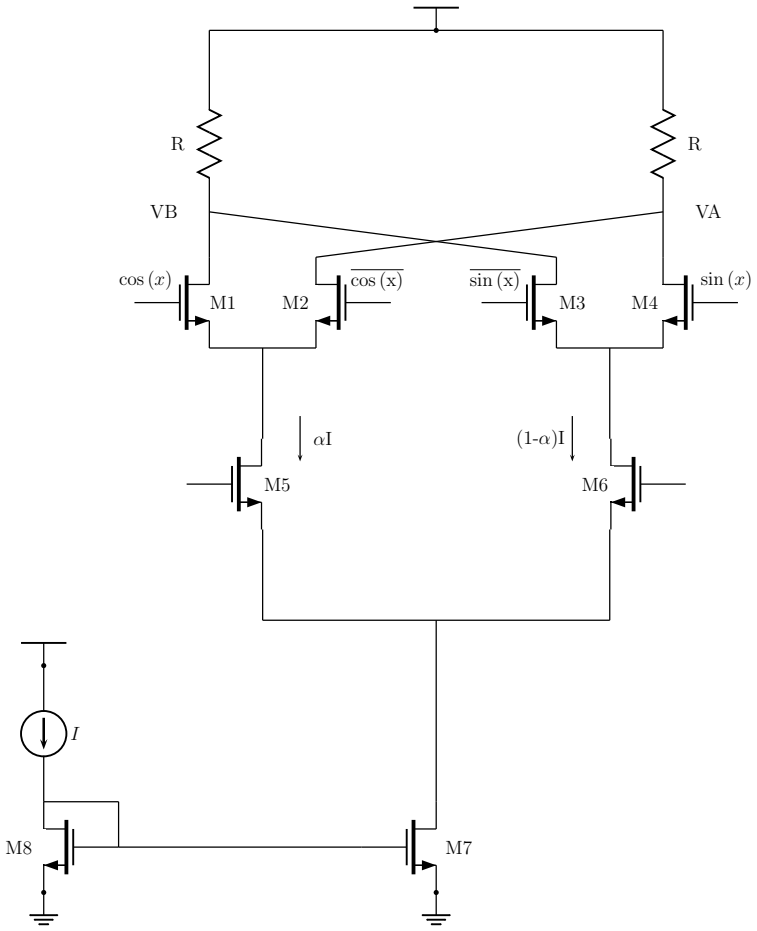

Figure 3.13: Phase Interpolator

The fundamental phase interpolator architecture [38], represented in Fig. 3.13 is composed by a differential pair composed by the transistors M1 and M2, and another differential pair composed by the transistors M3 and M4. These differential pairs receives the RF signal at 1GHz, and has an NMOS transistor in common drain, which will provide a constant weighted current, and receives a digital signal at 500MHz. These transistors are the M5 and M6 in Fig. 3.13. Also, there is a basic current mirror implemented using two MOSFET which behaves as a current bias to sink a constant current to the circuit. The two differential pairs are connected to the same output, terminated by resistors R.

As the differential pairs receives high frequency signals on its gates, so, it is necessary a fast NMOS switching. Thus, they must operate in triode region which means that the $V_{GS} < V_{th}$, and consequently, $V_{DS} < V_{GS} - V_{th}$, and also, as V_{th} = 0.5V, the drain voltage of M1 (V_{DM1}), M2 (V_{DM2}), M3 (V_{DM3}) and M4 (V_{DM4}) must be less than 1.3V. Also, to act as a fast switch the channel length of these transistors has to be the minimum size of this technology, since this technology has a great size.

The transistors M5 and M6 will receive the digital information in baseband frequency, 500MHz, and will be a current bias to the differential pairs, as mentioned before. Therefore, they must operate in saturation region, which means that to these transistors, its $V_{GS} > V_{th}$, and its $V_{DS} > V_{GS} - V_{th}$, so the drain voltage of M5 (V_{DM5}) and M6 (V_{DM6}) must be greater than 1.3V. Also, to act like a current bias, these transistors has to be its channel length greater than the minimum of this technology. Because in saturation, the current increases slightly with V_{DS}, but with a larger channel length the current is the same for all V_{DS} values

As the transistors M1, M2, M3 and M4 operate in triode region to act like a switch, they will work as a resistance which ideally is zero, so the V_{DM5} and the V_{DM6} must be enough to M5 and M6 work in saturation. However, due to the internal resistance of the transistors, there is a voltage drop between V_{DM1} and V_{DM5}, for example, which prevents having the necessary voltage to M5 and M6 achieve the saturation region. Thus, since the increasing of channel width decreases the NMOS internal resistance, the solution for this problem was increasing the channel width of the M5 and M6 transistors. With this approach the M5 and M6 transistors can achieve the saturation region for a value, lower than 1.3V, which allow a V_{DS} of M1 transistor greater than the V_{th}.

$$r_o = \frac{1 + \lambda V_{DS}}{\lambda I_D} \tag{3.28}$$

$$r_o = \frac{1}{I_D}\left(\frac{1}{\lambda} + V_{DS}\right) \tag{3.29}$$

$$where: \quad \lambda = \frac{\delta L}{V_E L} \tag{3.30}$$

According to the Schichman-Hodges model, the MOSFET output resistance is given as (3.28) or (3.29), where λ is the channel-length modulation parameter. It can be concluded that with a higher channel length the output resistance will increase affecting the current mirror performance. To avoid this issue, it is necessary a high channel width to increase the width-to-length ratio, allowing an output resistance decrease and a higher current flow to provide to interpolator the same current as the current supply.

In the first approach, the circuit was designed to ensure a correct differential pairs and current mirror performances, according to the theoretical concepts mentioned. Then the transistors where sized according to their respective regions of operation.

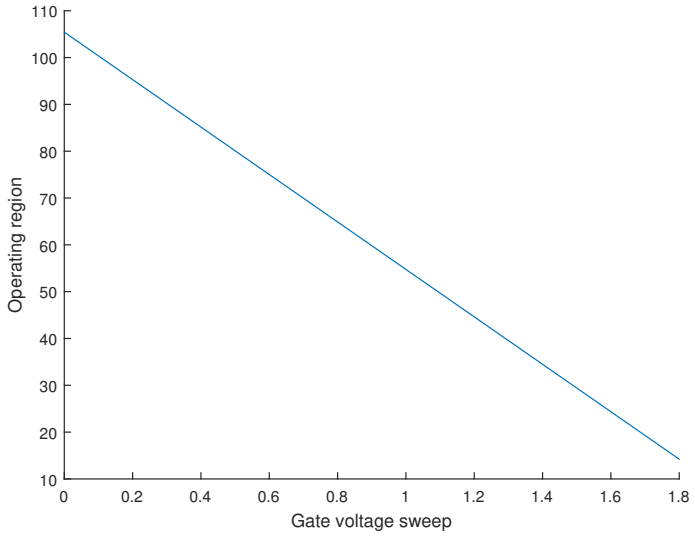

Figure 3.14: Output Phase

The Fig. 3.14 shows the output phase obtained when the gate of M5 transistor receives 1.8V and the gate of M6 transistor receives 0V, and vice-verse. Here, it is possible to verify the 90 degrees between the PCW equals to 0 and 31. Thus, the desired aim and performance of this circuito was achieved.

The next step of this work is apply this circuit concept to achieve a phase interpolator with a 5 bit resolution.

Chapter 4

Transistor Level Implementation for the Phase Modulator

Having already sized a basic phase interpolator it is necessary to decide the design to get a better resolution possible for this work. As mentioned in 2 there are various approaches of the use of this block. Although these solutions have a good concept, it was discussed a new solution, which in a previous analysis, it was concluded that it could occupy a lower area.

To avoid these problems, and to try to implement a better approach in context of this work, it was implemented a new design which consists in having five transistors in parallel, as in Fig. 4.1. The transistors in parallel will receive in its gate a digital value at the baseband signal frequency, allowing the control of the current weight by a digital value.

Their channel-width is scaled in 2^n, such that, the M5 and M10 width is the minimum for the technology used, the next ones will have a channel width two times greater than the previous, and so one.

$$I_D = \frac{u_n C_{\text{ox}}}{2} \frac{W}{L} [V_{\text{GS}} - V_{\text{th}}]^2 [1 + \lambda (V_{\text{DS}} - V_{\text{DSAT}})] \tag{4.1}$$

Therefore, according to the equality for MOSFET in the saturation region (4.1), it is concluded each transistor has a binary weight on current allowing 32 possible output phase values with 5 transistors in parallel, at each side.

To achieve the current weight on each side of the circuit it is necessary provide a digital value to the gate of the transistors in parallel to turn them ON or OFF. So it was implemented a control block in Verilog-A, which according to a received Phase Code Word (PCW), which is a number between 0 and 31, it provides digital values to the gates of the transistors in parallel. For example, if the PCW is 12 which is 11000 in binary it means that BB16 and BB8 are 1.8V and BB4, BB2 and BB1 are 0V and also, $\overline{BB16}$ and $\overline{BB8}$ are 0V and $\overline{BB4}$, $\overline{BB2}$ and $\overline{BB1}$ are 1.8V.

However, to get the same performance as the previous phase interpolator, it is necessary to estimate the ratio between the sum of the channel width from the transistors in parallel of one side

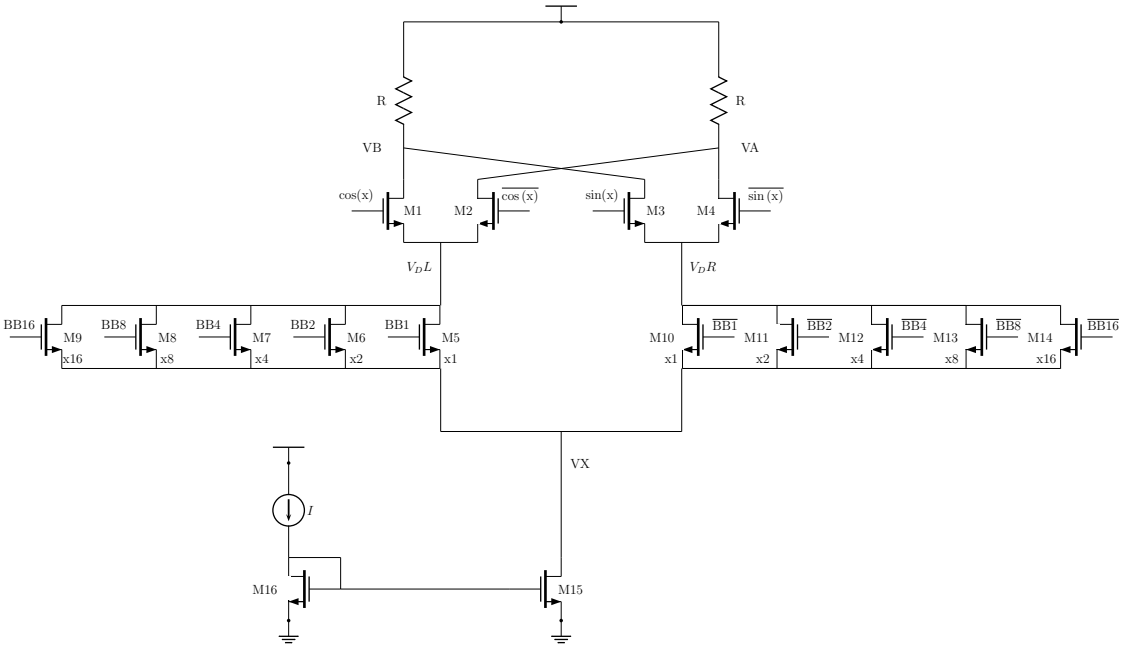

Figure 4.1: 5-bit Phase Interpolator

and the channel width of M6 or M5 from Fig. 3.13 in 3. Then it is necessary increase the channel width from the other transistors and the current bias value in the same ratio. So, the channel width for M5 and M10 is 240nm, for the M6 and M11 are 480nm, for M7 and M12 is 960nm, for M8 and M13 is 1920nm and for M9 and M14 is 3840nm, then it is achieved a total channel width of 7440nm, which means that the ratio is 7.44, so the current supply value for this new design will be 744um and both resistors are 670Ω, and also, the M1, M2, M3 and M4 channel widths must be 40um.

With the Fig. 4.2 and Fig 4.3 it is possible to see that the desired V_DL and V_DR values were achieved in this new configuration. In the simulation it was set a PCW equal to zero, which means that the right side is ON, that is, all the transistors in parallel are conducting, and the left side is OFF. The Fig. 4.2 represents the signal on V_DL and V_DR nodes, when PCW is 0. It is possible to verify that the side of the node V_DL is OFF, since its voltage is about 1.6V. The V_DL is not 1.8V, as expected due to the internal resistance of the transistors M1 and M2. Also, with the signal in V_DR, can be seen that the maximum voltage is about 1.22V, which is enough to let the transistors in parallel perform in saturation region.

With parametric DC simulation it is possible to verify the working regions of each trasistors. In Virtuoso it is possible to map the five transistors regions as, 0 is cutoff, 1 is triode, 2 is saturation, 3 is sub-threshold and 4 is breakdown. In Fig. 4.3 it is represented the operation region of the transistors parallel on both sides of the phase interpolator. It can be seen that the working region of the transistors switches between saturation and sub-threshold region, according if the transistors

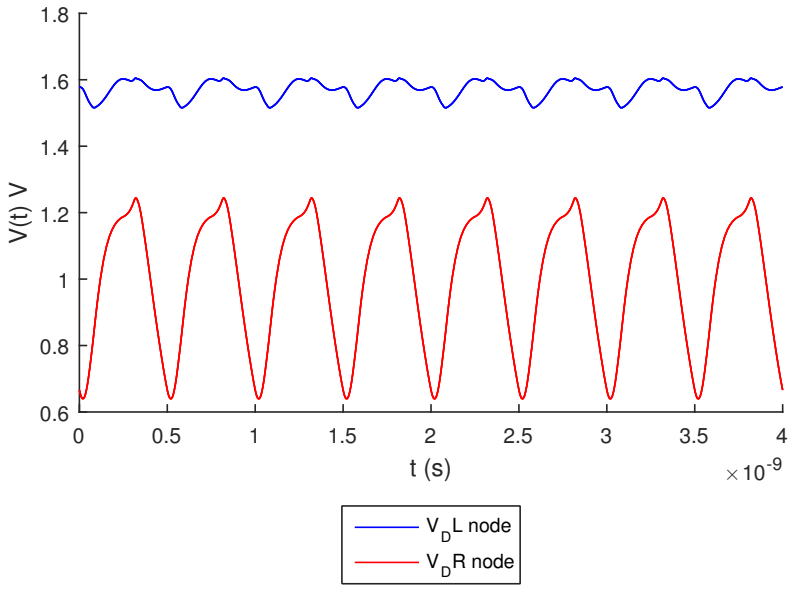

Figure 4.2: Signals in V_DL and V_DR When Current Bias is 744uA

are ON or OFF. The operation region of the M1, M2, M3 and M4 transistors were measured and it was possible to verify that it works at triode region.

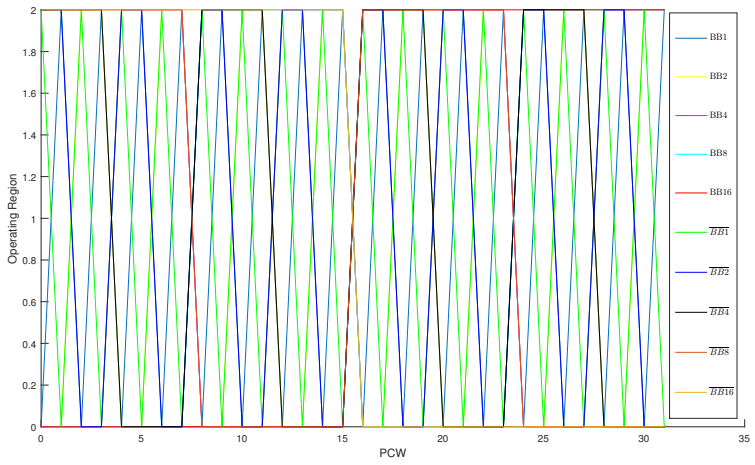

Figure 4.3: Parallel transistors operation region

To this approach it was measured the output phase for each PCW value, the result can be seen in Fig. 4.4. The output phase obtained is not so linear as expected, but it is necessary a current bias with 744uA, which means that this circuit will have a great power consumption. So, instead of improving its linearity, it was important to find a solution to reduce the current bias value and

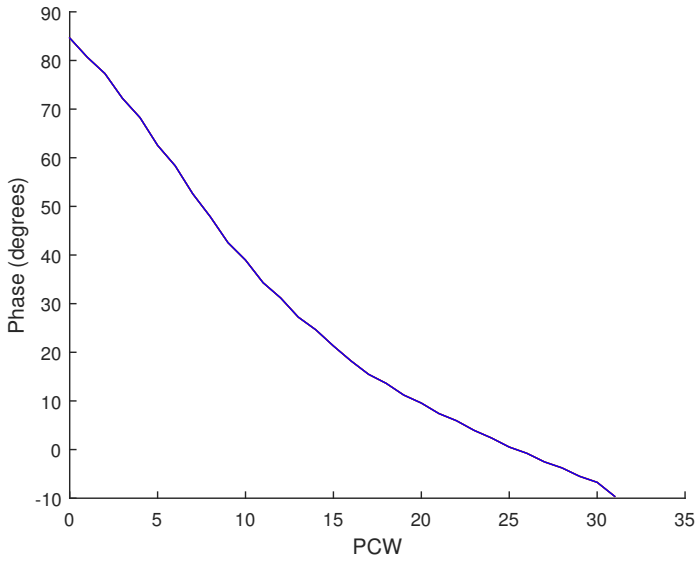

Figure 4.4: Output Phase When Current Bias Value is 744uA

consequently the power consumption.

Thus, since the first approach consumes a 100uA current bias, and this approach which has an area 7,4 greater, consumes 744uA, it is possible to conclude that the increasing of the parallel channel width meant the current increase and consequently the power consumption. So, it was concluded that this way of design is not proper to the aim of this work.

However, with this way of design it is possible to decrease the current supply, increase R resistors values and decrease M1, M2, M3 and M4 transistors channel width to achieve the same voltage values to get the correct transistors region of operation, but, doing that, the phase output becomes non-linear.

Thus, the channel width of the transistors in parallel was resized with the fact that a transistor with a size $\frac{W}{L}$ is equivalent to have N transistors in parallel, where each transistor have the size $\frac{\frac{W}{N}}{L}$. In this way, the sum of the channel width of the transistor in parallel can be reduced.

Initially, to turn 1um total width channel in 2^n scaled, the width channel of M10 must be 32um, for M11 is 64um, for M12 is 128um, for M13 is 256um, and for M14 is 512um. However, it is necessary to multiply the channel width and channel length by a factor to achieve the minimum channel width allowed bu this CMOS technology, 240um, to achieve the same W/L ratio than the previous.

Simulating with those values, the M10 and M11 transistors achieve the saturation region only when V_RD is 1.4V, so it will never reach this region of the same V_RD voltage of the previous approach. This fact happens due to its lower channel width which increases its the internal resistance. Then, the circuit was resized to increase the V_RD voltage to attain the target region.

For a ratio of 128nm/540nm it was possible to achieve the saturation region with an acceptable V_RD voltage, so the minimum channel width of the transistors in parallel had to be 128nm. Thus,

the total channel width was four times greater than basic circuit, which is less than the previous approach.

With these changes all components had to be sized again, but not in proportion total channel width increment of the transistors in parallel. So, to achieve a drain voltage about 1.3V in M1, M2, M3 and M4, their channel width had to be decreased to 5um and the resistors R were increased to 4kΩ to adjust the VA and VB voltages. The digital value received by the gates of the transistors in parallel has to decrease from 1.8V to 1.4V, to decrease the V_DL and V_DR voltages, allowing all transistors to perform in saturation operation. Besides that, the current supply value was increased to 210uA to adjust the suitable drain voltage off all transistors in phase interpolator.

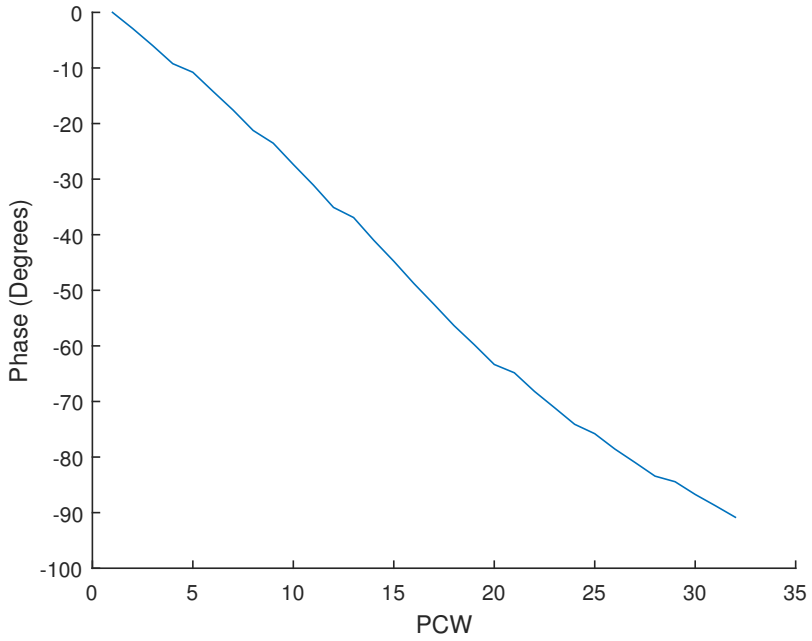

Figure 4.5: Output Phase for each PCW

The Fig. 4.5 shows the output phase shift for all PCW values with two RF input signals in quadrature. It is possible to check that the phase difference from two signals in which PCW is 0 and 31 is 90 degrees. It is possible to see that this approach with a low power consumption has a better linearity than the previous, which means that this solution is the better suited to the aim of this work.

Since the transistors in parallel were resided, the necessary V_DL and V_DR voltages, from Fig. 4.1, to achieve the correct operating region is not the same as in the first scaling for reduce the power consumption. In the Fig. 4.6 it is possible to conclude that the necessary V_DR value to achieve the saturation region is about 1.2V and the V_DL voltage value is higher because the M1 and M2 transistors are in cutoff region. It is fundamental to mention that these values are lower than the previous approach since the current value is lower, the channel width of M1, M2, M3 and

M4 transistors is lower too, as the W/L ratio of the parallel transistors, thus allowing a lower V_{DS} voltage.

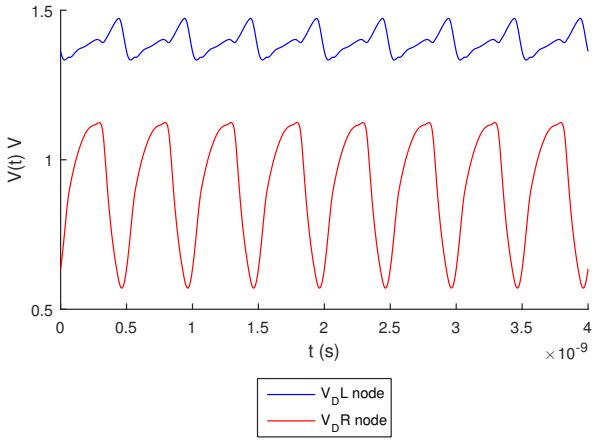

Figure 4.6: Signals in V_DL and V_DR Nodes When Current Bias is 200uA

Also, it was measured the operating region of each transistor such as in the previous approach, and all transistors perform as desired.

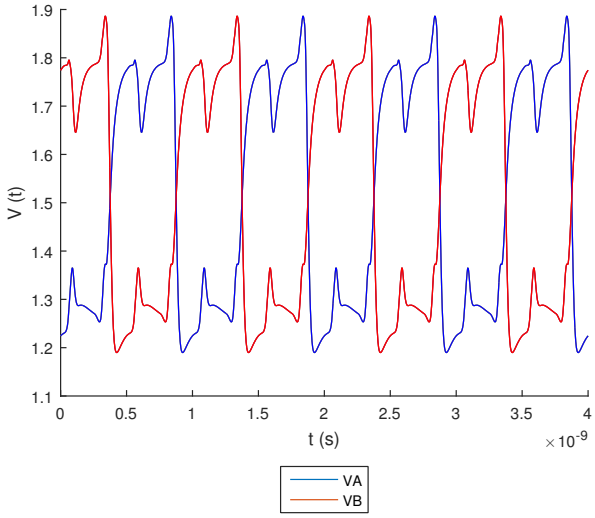

Figure 4.7: Output Signal in VA and VB when PCW is 0 and 31

The Fig. 4.7 indicates the output signal of this approach when PCW is 0 and 31, and it is possible to observe that the format of the output signal has a format of a square wave, but with the high frequency harmonics. However its amplitude varies between 1.2V and 1.8V, as expected

because the VA and VB are the drain voltages of the transistors M1, M2, M3, M4, and this voltage can not be greater than 1.3V

In conclusion, it is possible to design this phase interpolator according to the requirements of this work. Initially it was implemented a circuit which was easy to design, but it consumes a lot of power consumption due to the increase of channel width of the transistors in parallel which lead to a current bias value of 744uA. To decrease the high power consumption it was necessary decrease the channel width of transistors in parallel keeping the same ratio W/L of previous approach. This new approach which was harder to design, due to its instability. However the correct performance of the transistors were achieved, and the 90 degrees difference of the output phase for all PCW was obtained with a better linearity. However, it is important to improve the output phase linearity to approach it with the theoretical result, by changing some determinant parameters of this circuit.

4.1 Phase Output Improvements

Initially the circuit was sized only to achieve a 90 degrees phase sweep in the correct transistors operating regions. After that it was necessary to validate this result, comparing it with the theoretical value. This result is in Fig. 4.8, and although being a suitable approach, it can be possible to improve this result. So, this circuit was simulated with various values of current bias and values of channel width of M1, M2, M3 and M3 transistors, which could be responsible for a simulated phase output closer than the theoretical.

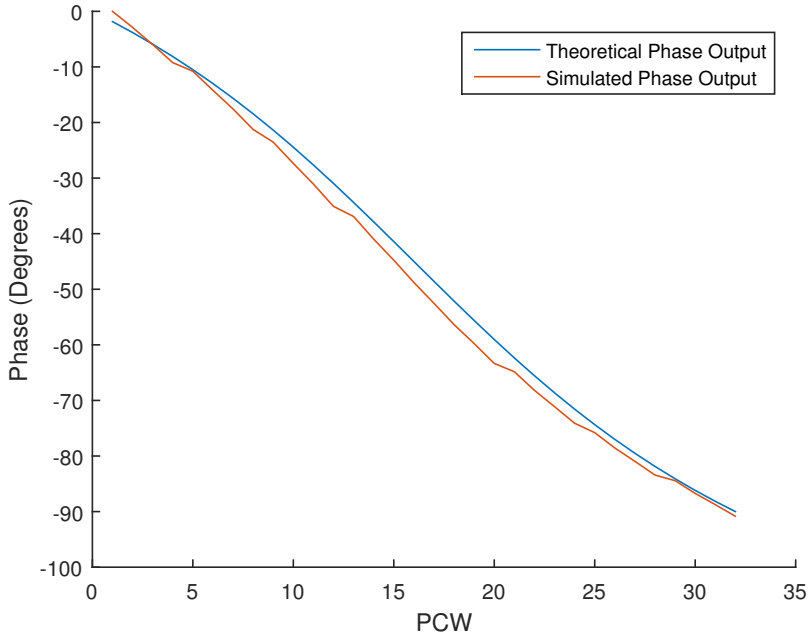

Figure 4.8: Theoretical and Simulated Phase Output in Previous Approach

An important parameter is the current bias value which can be changed with an adjust on resistors values at the same time, to maintain the same transistors operating region. Once the power consumption value is crucial in this work, decreasing the current value could yield a good solution as well.

In the Fig. 4.9 there is represented a simulation of the phase shift for all PCW for three possible current bias values, with the corresponding resistors values.

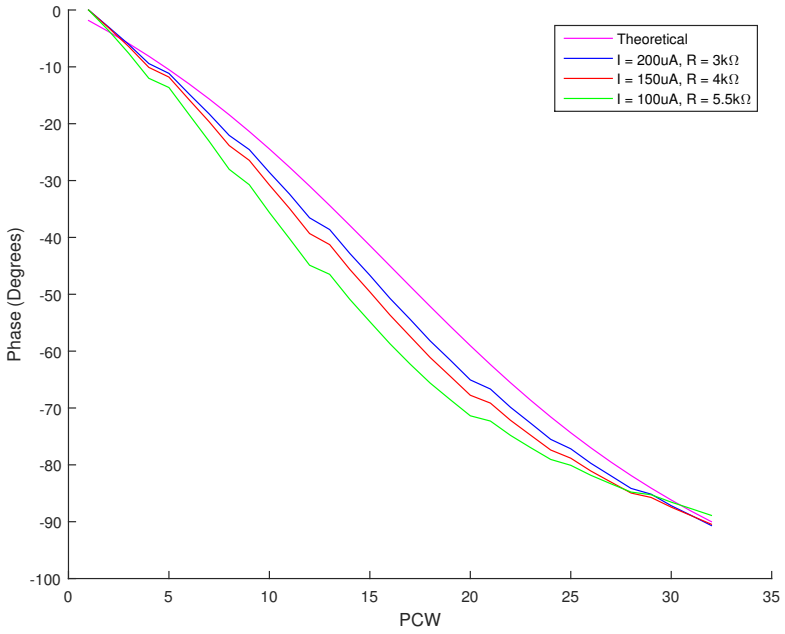

Figure 4.9: Phase Output for Different Current Bias Values

There are another parameter in this circuit which can be changed to achieve a better approach to the theoretical output phase, the channel width from M1, M2, M3, and M4 transistors. It was noticed noticed a great improvement of the output phase with the decrease of this value, but it is necessary at the same time to adjust the current and the two resistors. In Fig. 4.10 it is possible to verify an approach to the theoretical value with the decrease of the channel width.

The current bias value was changed for the final approach because, despite being a better solution according to the previous image, when the channel width values were changed , the current had to be decreased to get the correct operating region.

This linearity improvement is possible because in the previous solution the transistors were operating at the threshold of its operating regions. So, with the adjust of the transistors channel width, the current and the two resistors value, the drain voltages changed and it was reached a well-defined operating region to all transistors of this circuit.

The Fig. 4.11 shows the final result of this size adjustment compared with the theoretical, where it is possible to see that they are very close. This result, was achieved with a 250uA current bias, with a M1, M2, M3 and M4 channel width of 3um, two resistors with $3k\Omega$.

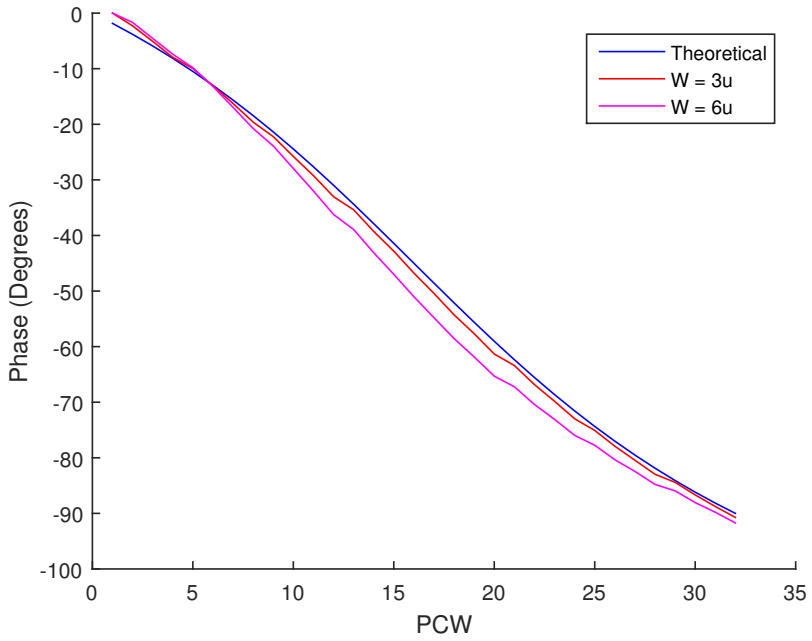

Figure 4.10: Phase Output for Different M1, M2, M3 and M4 Channel Width

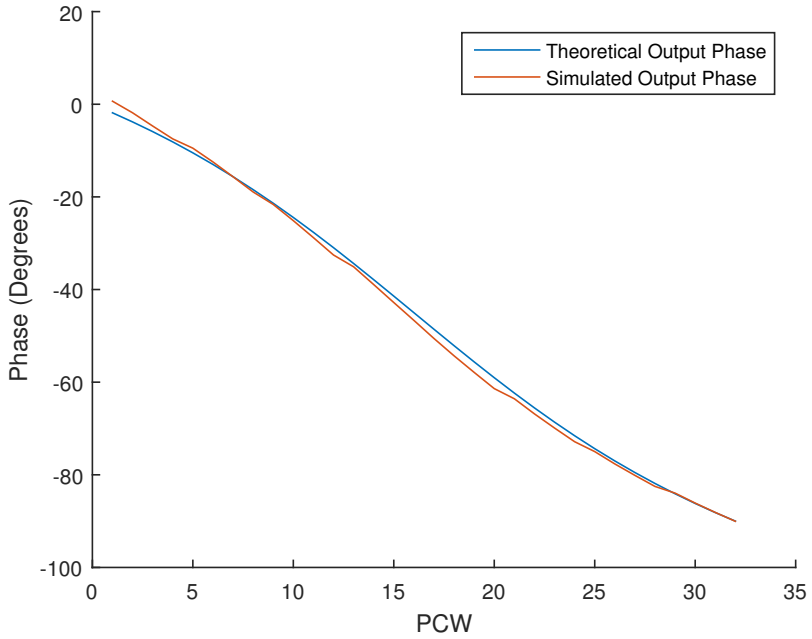

Figure 4.11: Simulated Phase Output Compared With Theoretical Phase Output with Improvements

The Fig. 4.12 represents the signal output, in VA and VB nodes from Fig. 4.1, to a 0 PCW and to a 31 PCW. It is possible to conclude that these signals are in a 90 degrees difference phase,

and also it can be verified that its amplitude voltage varies between 1.2V and 1.8V, as the previous results. These values can confirm the correct operation of this circuit.

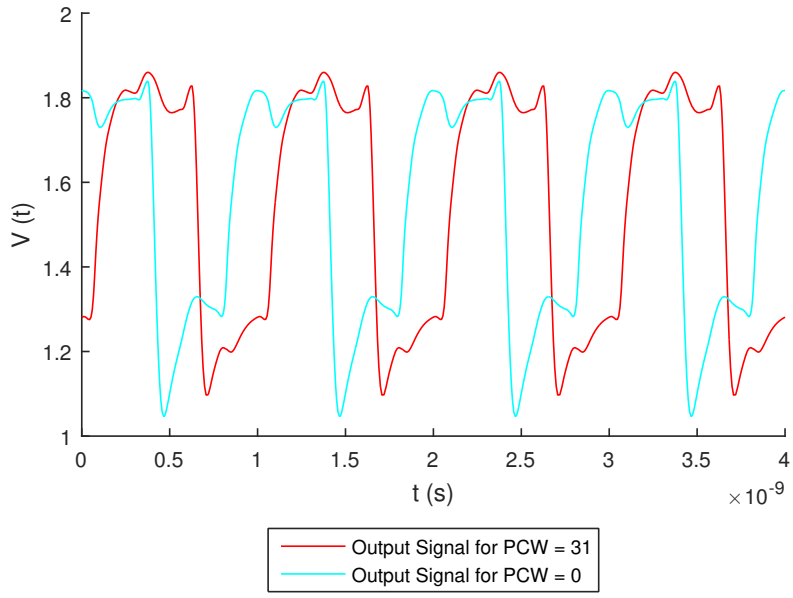

Figure 4.12: Output Signal

This last solution is the final design, consuming 450uW of power. It accomplishes all requirements in agreement with the theory. It achieve a 90 degrees output phase for all PCW and has a moderate power consumption.

4.2 Differential Quadrature Clock Signals

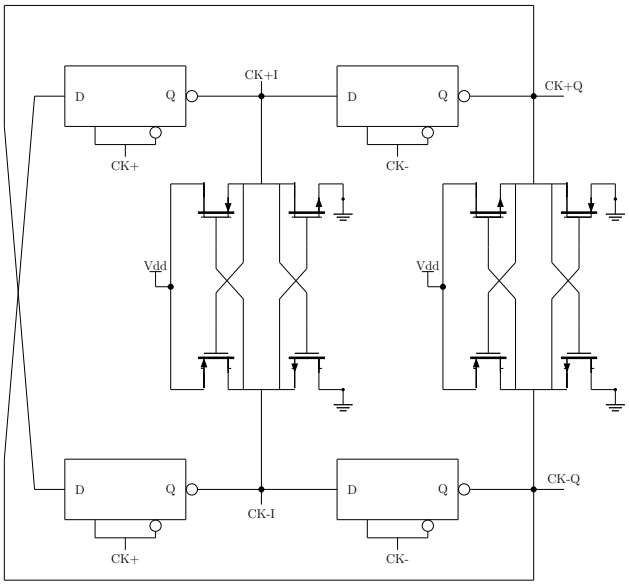

Figure 4.13: Clock Divider

The next aim is the design of two blocks, one of them has to divide the received RF signal in four quadrature signals, and the other has to act like a multiplexer allowing the exchange of the phase interpolator inputs in order to reach the 360 degrees.

In this section the architecture used to perform a signal divider and its simulation results will be explained and demonstrated. This architecture was chosen according to the most important requirement for this work, the power consumption.

The Fig. 4.13 represents the architecture chosen, the clock divider [39], which seems to be a great solution to this problems. It only use four latches and eight inverters, avoiding components which occupy great areas such as resistors or coils.

This clock divider is used to produce four differential quadrature clock signals CK_{I+}, CK_{I-}, CK_{Q+} and CK_{Q-}.

The differential 2*f0 clock, CK_{+}/CK_{-}, is applied to one clock divider to generate the desired carrier LO at f0. It is implemented as a flip-flop based frequency divider which consists of four C2MOS latches, arranged in a loop. The back-to-back inverters ensure that no illegal

states will occur, and guarantee 180º. They also align differential clock phases (CK_{I+}/CK_{I-} and CK_{Q+}/CK_{Q-}). The input and output nodes of C^2MOS latches, represented in Fig. 4.14, experience rail-to-rail voltage swing. Consequently, they exhibit a superior noise performance over the low-swing current-mode logic (CML) latches. In this approach , the data and clock inputs of C^2MOS are swapped. By doing so, the D-to-Q delay of the latch and, subsequently, the overall loop time period of the divider, decreases.

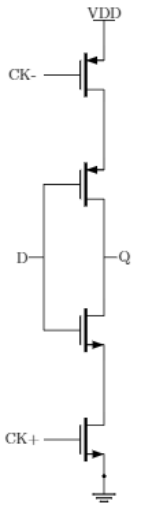

Figure 4.14: CMOS latch

The transistor sizing is adjusted based on its operating frequency, so to this technology the channel width and channel length of NMOS and PMOS transistors must have the same value. So, it was decided that the channel length has the minimum value, 180n, and the channel width must be, at least, 1440nm to obtain a good signal amplitude, once for values under this the signal amplitude becoming decrease, obtaining a digital signal to the minimum channel width. Also, the values for the back-to-back were set according to the optimal width size of an inverter of this technology to acquire equals rise and fall times, so the PMOS channel width has to be three times greater than the NMOS, so, the channel length is the minimum to all transistors, 180n, and the channel width of PMOS is 720nm and of NMOS is 240nm.

The Fig. 4.15 and the Fig. 4.16 are the result of a simulation where it is possible to verify the four differential quadrature clock signals, CK_{I+}, CK_{I+}, CK_{Q+} and CK_{Q-}, obtained at the output.

However, it is necessary to add inverters, to the input signals, ck+ and ck-, and in the outputs of this block to obtain output signals with a proper amplitude. These inverters have the NMOS and PMOS channel length of 180nm, and the channel length of PMOS is 720um and the channel length of NMOS is 240nm.

This block consumes a 797.345uW power, measured with the inverters included.

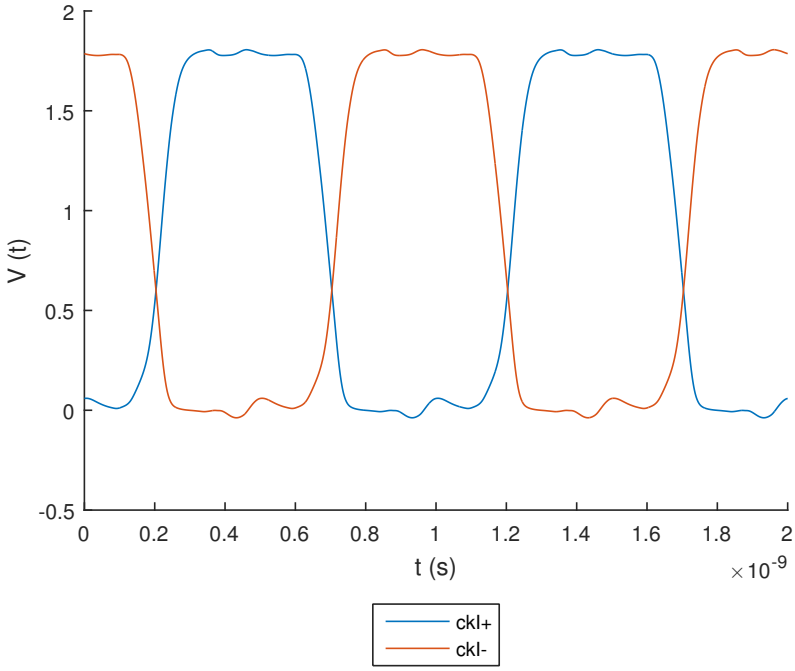

Figure 4.15: CK_{I+} and CK_{I+} signals

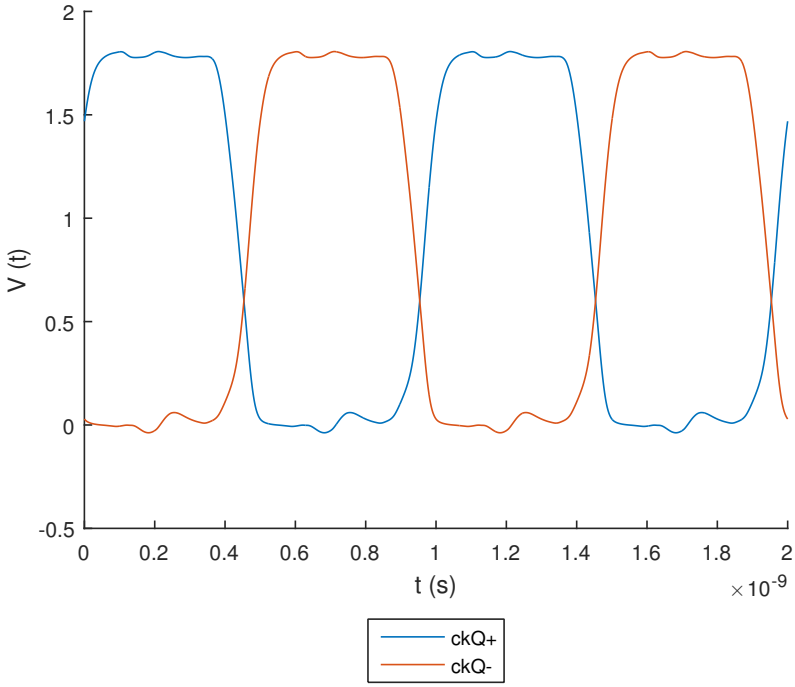

Figure 4.16: CMOS latch

4.3 Quadrature Signal Selector

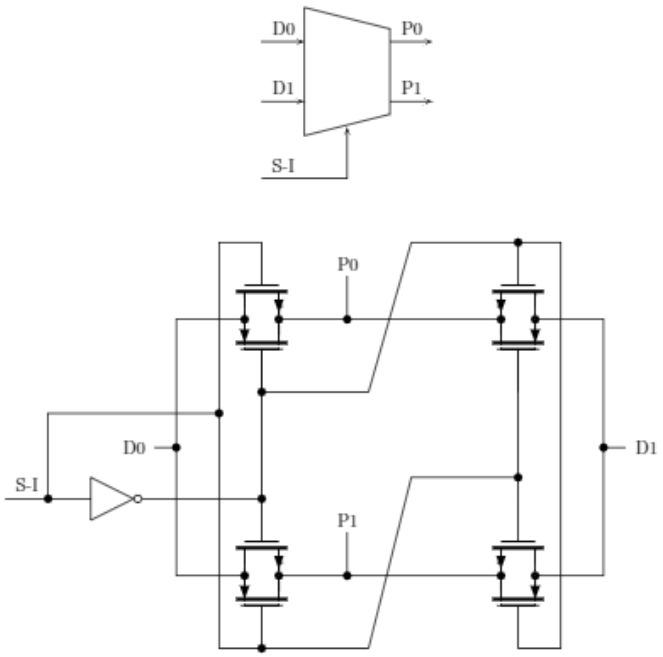

Figure 4.17: Quadrature Signal Selector

The Fig. 4.17 shows the quadrature sign bit [40], is for the two quadrature clock signals, which turns out to be a multiplexer. When the sign bit is high, then D0 and D1 directly pass through the transmission gate switches to the P0 and P1 nodes. When the sign bit is low, the inputs D0 and D1 cross each other through the pass-gate switches to reach the P1 and P0 nodes, respectively.

In the context of this work, it is necessary two differential multiplexers, one which receives CK_{I+} and CK_{I-} as input, the other receives the CK_{Q+} and CK_{Q-} signals, and their outputs will be the phase interpolator signal inputs. In this way, according to the value of the selector, each input of the differential pair of the phase interpolator can receive two possible values, allowing a modulation to span the full 360 degrees.

The transmission gates were sized according the PMOS channel width will be three times greater than the NMOS, so the PMOS channel width is 720nm and the NMOS channel width is 240nm. Also, the PMOS and NMOS channel length is the minimum value, 180nm.

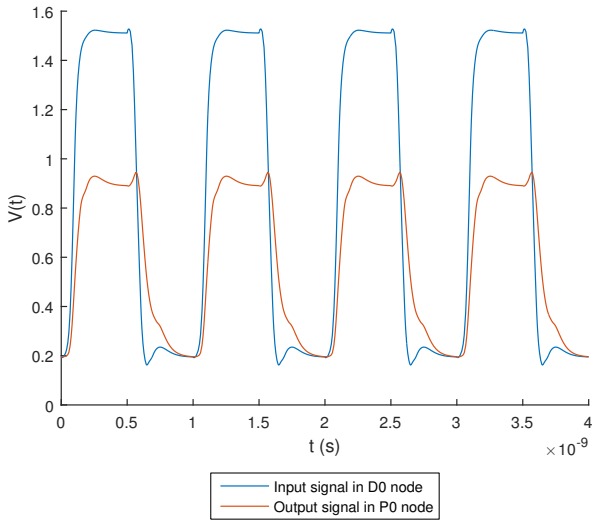

Figure 4.18: Input Signal at the D0 Node and Output Signal of P0 node

The Fig. 4.18 represents a simulation of this circuit, where it is possible to see the the output signal in P0 node, and after the inverter. Analysing these signals it can be seen that the output signal suffered from a voltage down scale, which is not fixed with the increase of transistors channel width. This attenuation is caused by the ON-resistance on transmission gates, which increases with the supply voltage as can be seen in [41]. Despite this, in time domain, the signals are in phase.

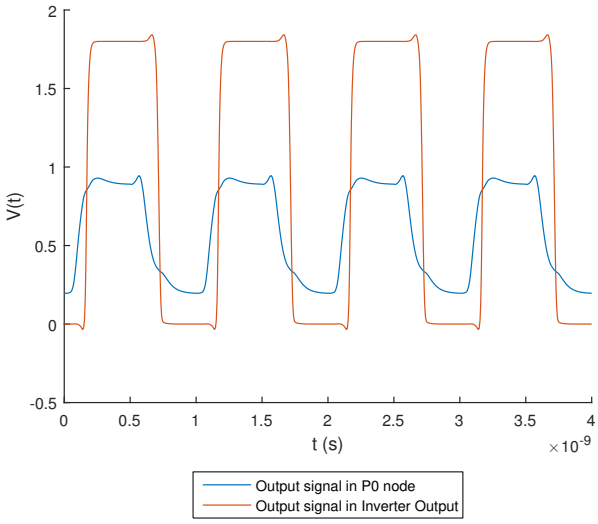

Figure 4.19: Output Signal at P0 Node and Output Signal at Inverter Output

To resolve the signal voltage down scale, it was added two inverters, acting like active loads, in the two circuit outputs, to restore it. In Fig. 4.19 it is possible to see the difference of the signals before and after the inverters.

So, it was obtained the Fig. 4.20 which represents the input signal in D0 and the output signal in P0, when the selector is 1.8V. In this result, it was noticed that the input signal also suffers from an attenuation due to the the switch ON-resistance, and there is a delay between the input and the output due to the charging and discharging of parasitic capacitors. Despite this, it is possible to conclude that the signals are the same.

The Fig. 4.21 represents the input and output signal, in the same node than the previous, but when the signal selector is 0V. It is possible to see the same delay and attenuation.

The power consumption of this block is 138.75uW. Since this block uses transmission gates which means a great power consumption, so this value is expected. Despite the use of transmission gates, this block consumes less energy than the other two. So, it is verified that the power consumption of this block can not be significant to the phase modulator.

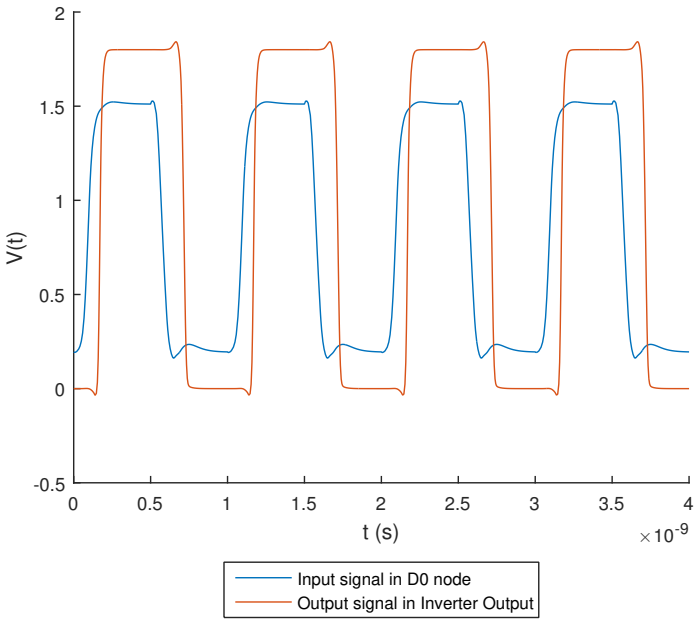

Figure 4.20: Input and Output signals when selector is 1.8V

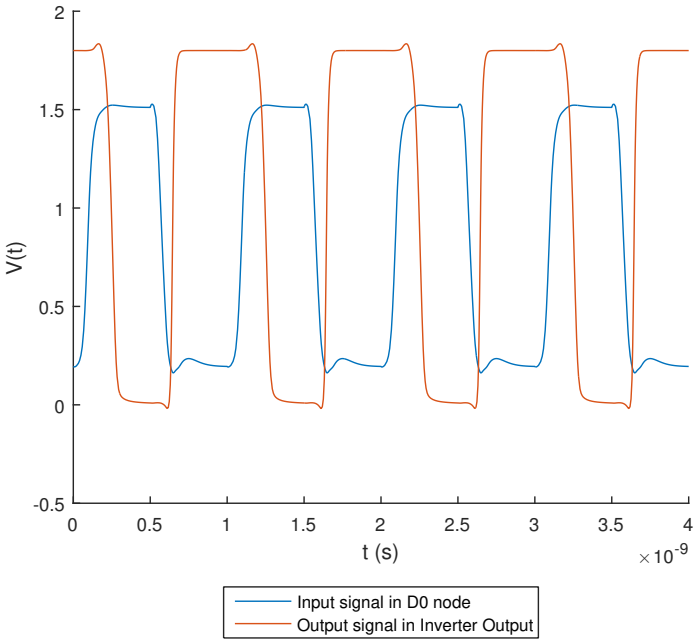

Figure 4.21: Input and Output signals when Signal Selector is 0V

4.4 Phase Modulator

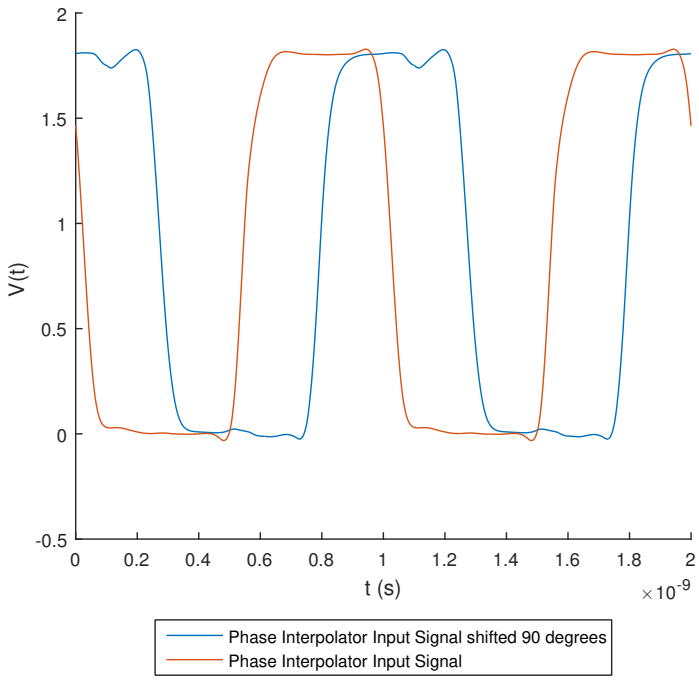

Figure 4.22: Interpolator Clock Inputs Generated in Phase Modulator

After being sure that all blocks were acting correctly, with the minimum sizes, all were connected to implement the complete phase modulator. Many problems emerged because of the parasitic capacitance presented on the transistors, which contributed to the loss of amplitude, and consequently, to the distortion of the signals.

Thus, on the input and on the output of these blocks, was added inverters acting as voltage restoring units, sized according to the optimal size of this technology, which is a PMOS channel width with 720nm and 240nm to NMOS, and a PMOS and NMOS channel length with the minimum size. In this way, the signals are recovered over the whole circuit, and so, the phase interpolator receives signals with a better amplitude to achieve a better performance. The Fig. 4.22 represents the improved phase interpolator input signals with these inverters.

In the Fig. 4.23 represents the phase sweep in 360 degrees. It is possible to verify that this phase modulator can cover the entire unit circle presented in chapter 2 in Fig. 3.2

Another important aspect is the output signal which must have the better shape possible to the demodulation. A possible solution could be removing harmonics, at higher frequencies with a differential low pass filter (LPF), which in this case, consists in adding a capacitor between the interpolator outputs.

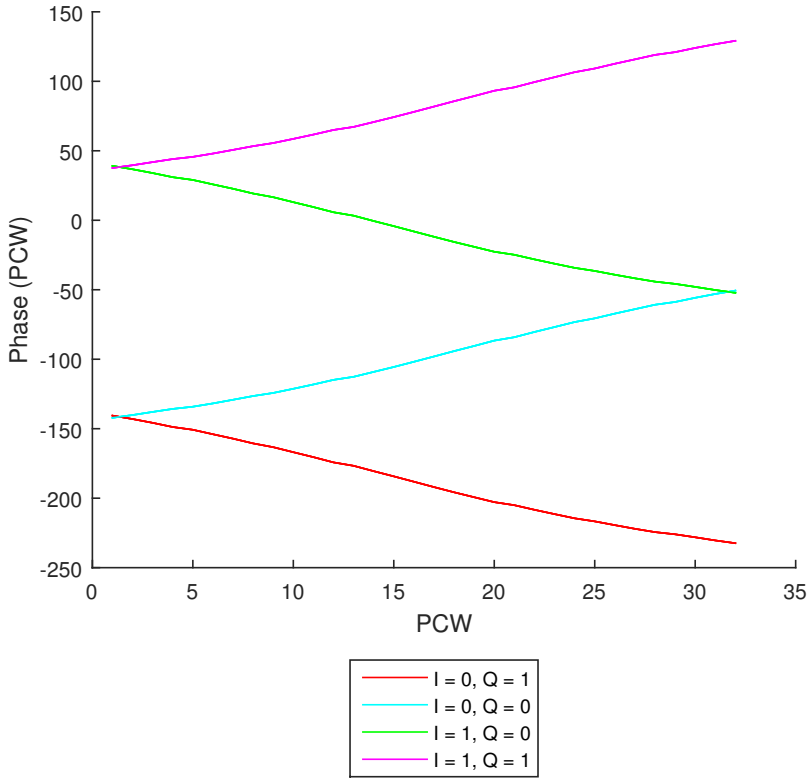

Figure 4.23: Output Phase for All Quadrants

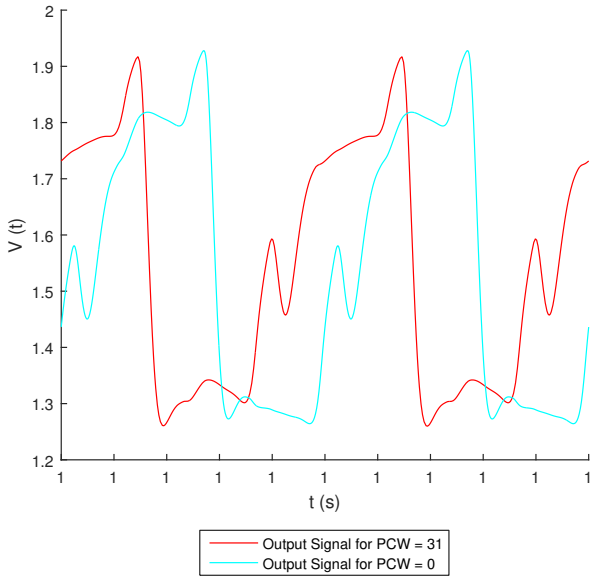

Figure 4.25: Output Signal with LPF

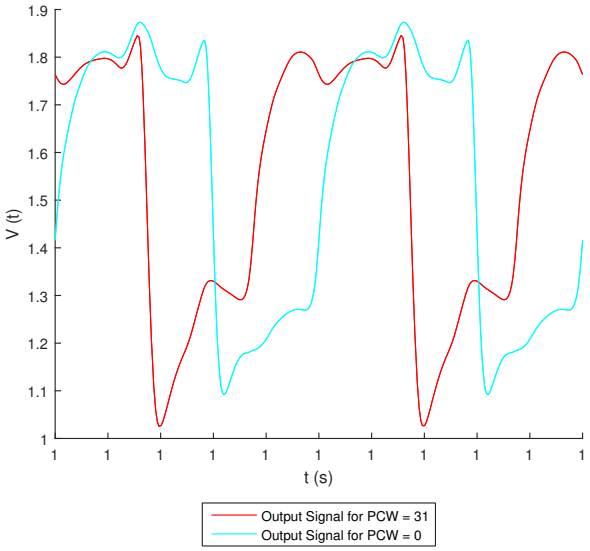

Figure 4.24: Output Signal without LPF

The Fig. 4.24 represents the output signal for a 0 and 31 PCW. By removing the harmonics with the LPF, the output signal obtained is represented in Fig. 4.25.

4.4.1 Power Consumption

The power consumption obtained in this phase modulator is 2.53mW, which is an acceptable value for this work.

The phase interpolator consumes 450uW, the quadrant signal generator consumes 797.3uW and the singal selector consumes 138.75uW, which gives a total of 1.386mW of power consumption. However power consumption for the phase modulator is almost 1mW greater. So, it can be concluded that the inverters used to restore the signals in the phase modulator consumes almost the same amount of the sum of the power of the three block of this system.

Comparing with the others architectures from the literature, in 1, this result is great having in count that this work uses a CMOS 180nm technology.

4.4.2 Linearity

A fundamental parameter of the phase modulators is its linearity. So it was measured some static performance metrics, such as the DNL, the INL, and consequently its monotonicity.

By sweeping the input code word (PCW) and measuring the output phase the DNL of the phase modulator with code was obtained. The measured DNL characteristic of the phase modulator is shown in Fig. 4.26. To estimate the DNL values it was applied the equalities (4.2) and (4.3). In

this context the DNL(i) was obtained using the output phase (out(i)) for the corresponding PCW(i), and since the phase modulator as a 5 bit resolution, the ***b*** value is 5.

By this Fig. 4.26 is possible to see that any DNL value is greater than 1LSB or lower than -1LSB which means that it is non-monotonic.

The estimation of INL for each PCW value is done with the DNL values by summing them, and by the method of using the endpoints. In Fig. 4.27 it is possible to observe the INL estimated with the end-point method. Having an imaginary line connecting the first and the last point, can be concluded it has better linearity for PCW values under 10 than the linearity for PCW values after 10. The maximum absolute INL value obtained was 1.8571.

This phase non-linearity obtained is introduced by using $\alpha\cos(x)$ and $(1-\alpha)\sin(x)$, can be compensate using a simple one-dimensional look-up-table (LUT). Modern transmitters increasingly rely on such digital assistance [26].

$$DNL(i) = \frac{out(i) - out(i-1)}{LSB}, 1 \leq i \leq 2^b - 1 \tag{4.2}$$

$$Where, \quad LSB = \frac{out(2^b - 1) - out(0)}{2^b} \tag{4.3}$$

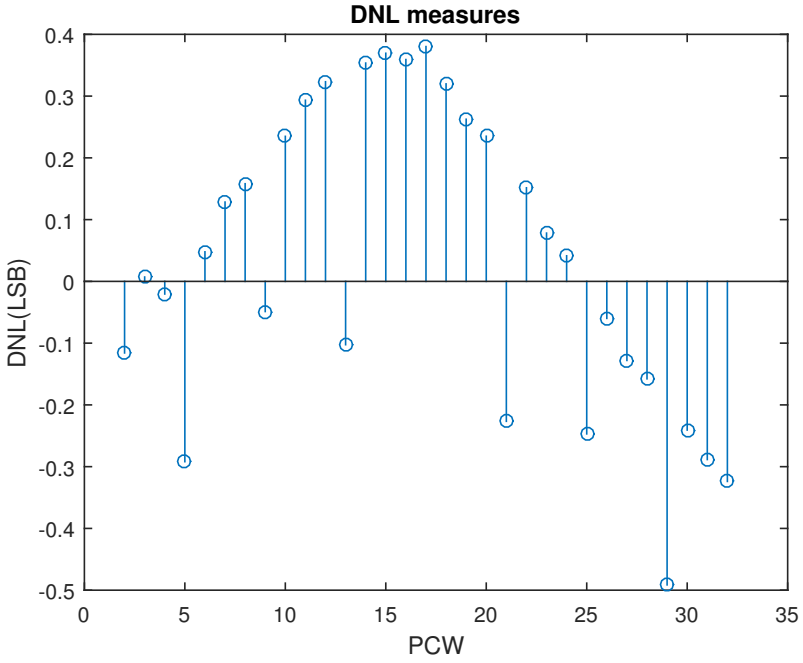

Figure 4.26: DNL

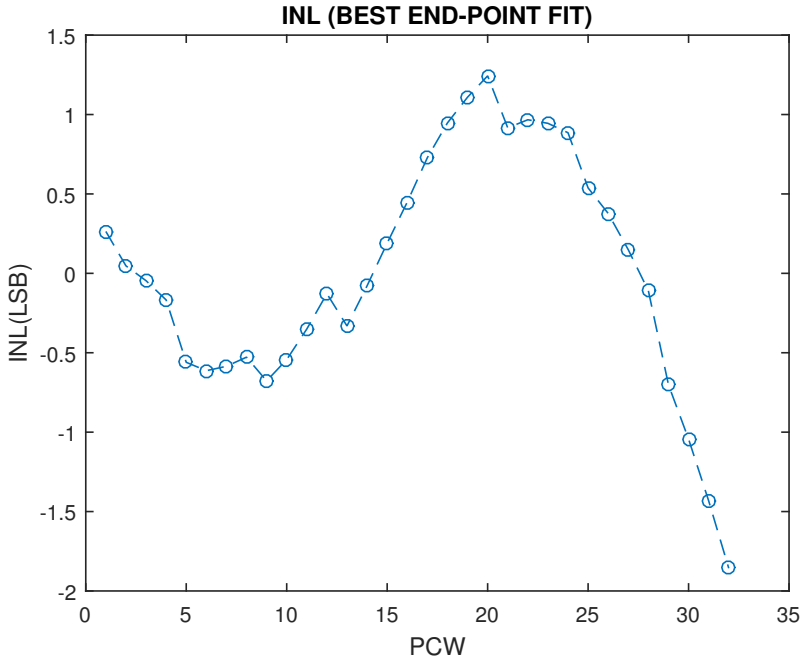

Figure 4.27: INL

4.5 IC Layout

The Fig. 4.28 represents the layout of the quadrature clock divider circuit, the Fig. 4.29 is the circuit which selects the inputs of the phase interpolator which is represented in Fig. 4.30. During the layout implementation some aspect was taken in count to reduce the parasitic resistors and capacitances, such has the use of higher layers and avoiding their overlap, and the use of multiple fingers for transistors with larger channel width and length.

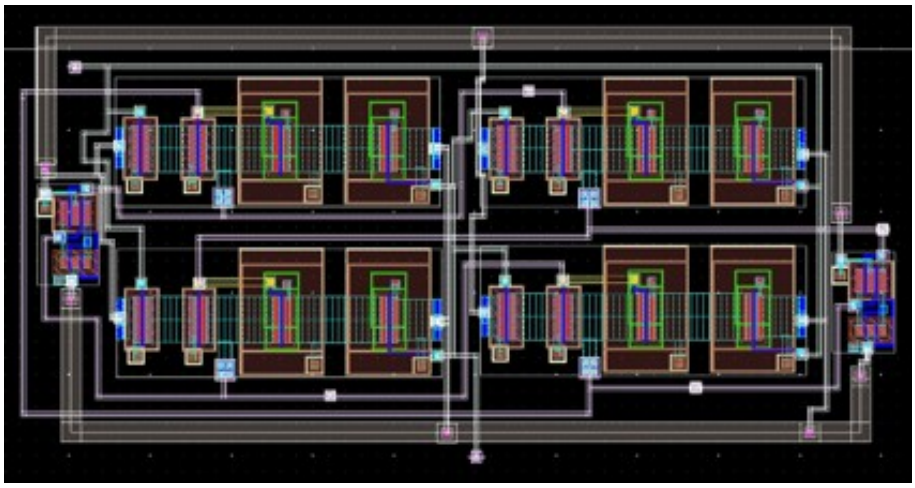

Figure 4.28: Layout of Clock Divider

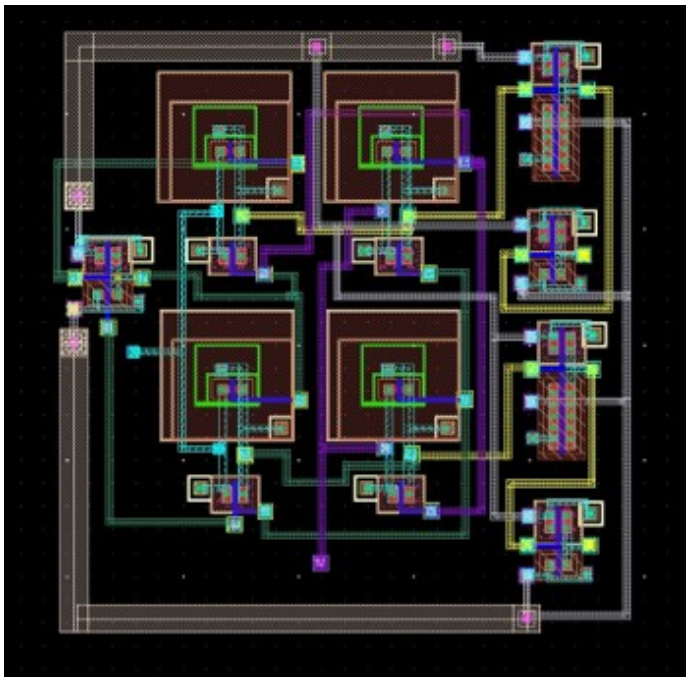

Figure 4.29: Layout of Signal Selector

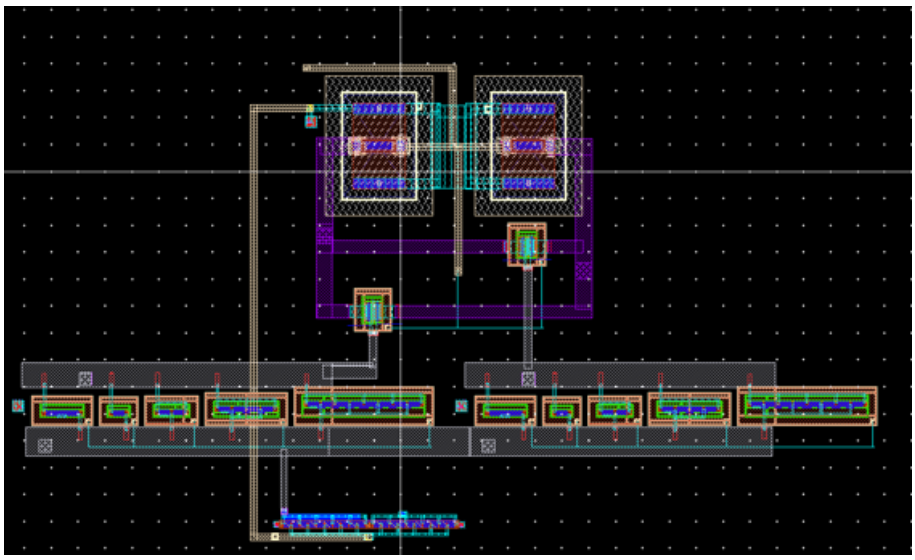

Figure 4.30: Layout of Phase Interpolator

4.5.1 Layout Results

The output phase from layout was obtained, as can be seen in Fig. 4.31. With this result it is possible to compare it with the results from schematic and from the theoretical and analyse their differences. The layout result has a different shape which results from the parasitic capacitances and resistors in transistors in phase interpolator, mainly in the transistors in parallel. These components will contribute to modify the drain to source voltages, turning the operating region of the transistors in parallel in a threshold between the saturation and triode. The Fig. 4.32 shows the phase modulation the 360 degrees from the layout approach. It can be verified that a suitable result was obtained.

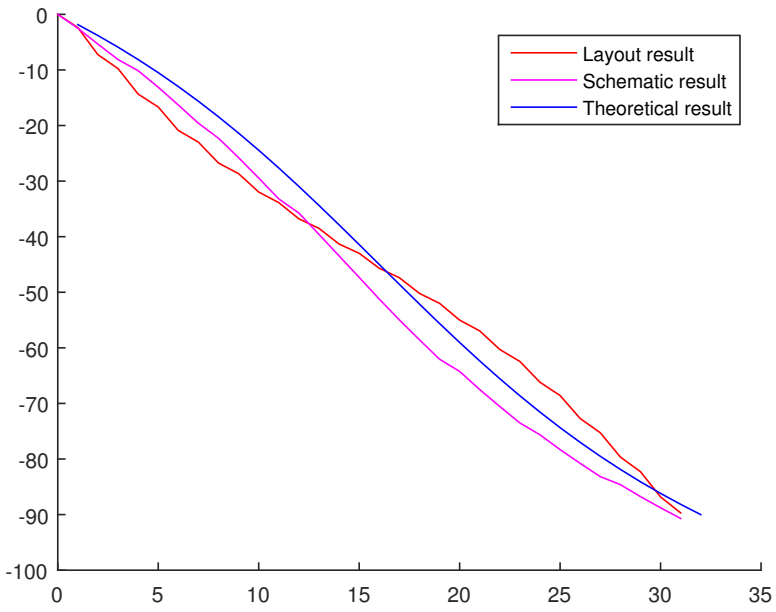

Figure 4.31: Output Phase From Layout, Schematic and Theoretical

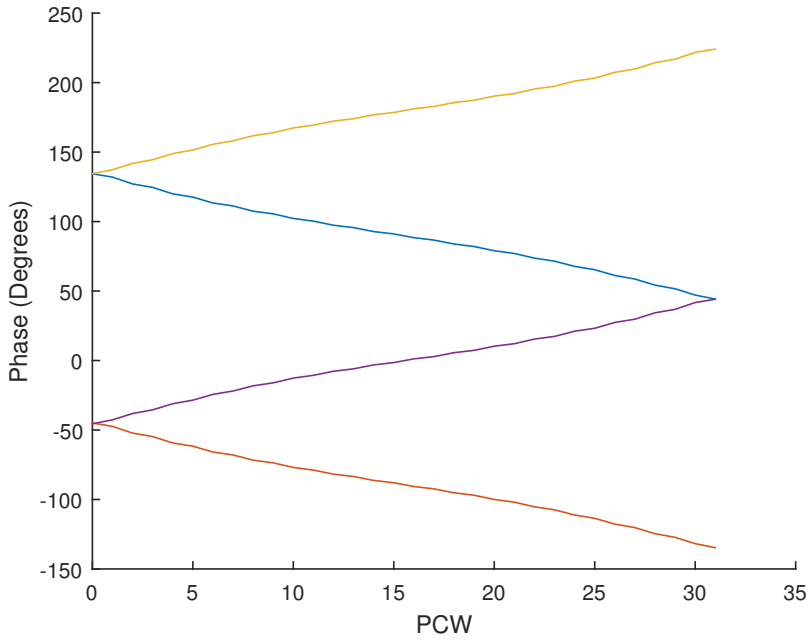

Figure 4.32: Layout Phase Modulation

4.5.2 Linearity Results From Layout

As mentioned before, the linearity is an important parameter in phase modulators and then it was measured to the layout approach. From Fig. 4.33 it is possible to conclude that this circuit has linearity once any DNL value is greater than 1 in module.

In Fig. 4.34 the INL values, obtained from the best end-point algorithm, can be observed.

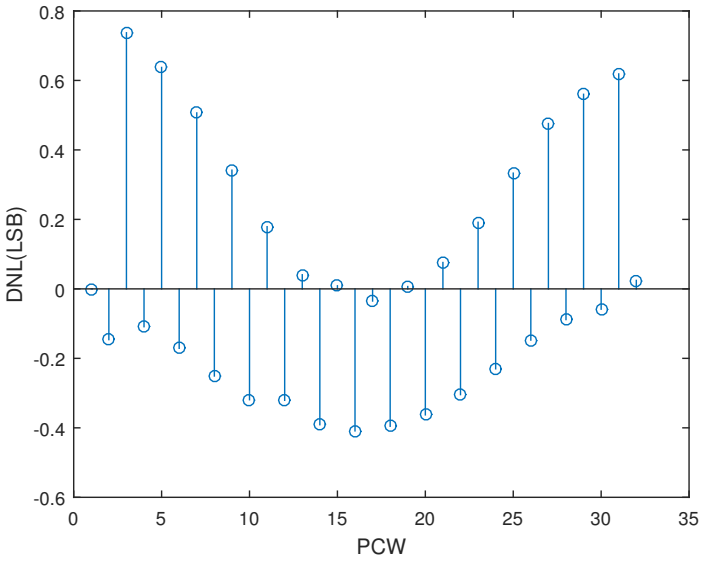

Figure 4.33: DNL of Layout

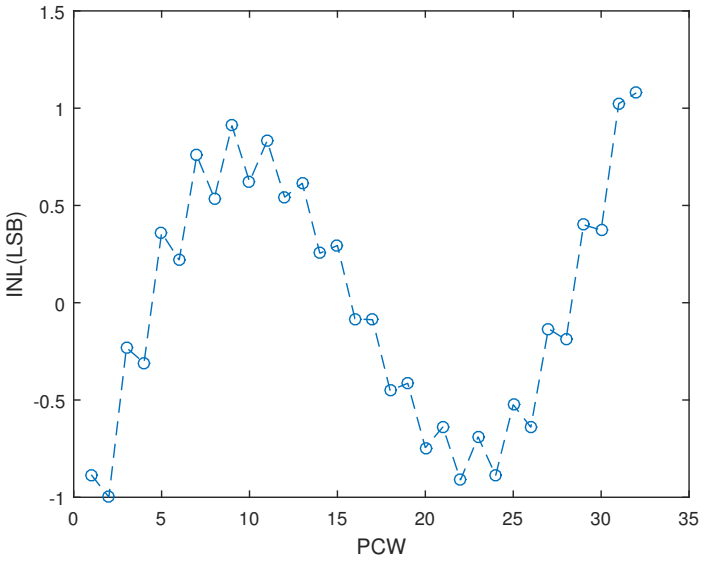

Figure 4.34: INL of Layout

Chapter 5

Conclusions

In this thesis, the phase modulator was designed with the aim of achieving an acceptable phase resolution with a moderate power consumption in CMOS 180nm technology.

The table 5.1 summarizes the properties of this design. Here it is possible to observe the contribution to the power consumption of each block for this phase modulator, concluding that the crucial block is the quadrant signal generator due to its back-to-back inverters. Although the signal selector was designed with the transmission gates, which act as a switch which consume a high power, it is the block which has the lowest power consumption.

However, the total power consumption value is a suitable for this work, once it is almost the double compared to the other architectures from the 5.1, even being a technology higher than the presented in the referred table.

This phase modulator accomplished all requirements, such as the 5 bit resolution, the low power consumption, and the difference of the output phase of 90 degrees to the quadrature RF input signals. Also, a positive aspect of this phase modulator is the possibility to select the RF input signals of the phase interpolator which allows a phase modulation in 360 degrees, as can be seen in 4 in Fig. 4.23. These results show that this architecture is viable for the aim of this work.

Table 5.1: Phase Modulator Performance Summary

Technology	CMOS 180nm
Power Supply	1.8V
Carrier Frequency	1GHz
Baseband Frequency	500MHz
Phase Resolution	5 bits
Phase Interpolator Current	250uA
Quadrant Signal Generator Power Consumption	797.345uW
Signal Selector Power Consumption	138.75uW
Phase Modulator Power Consumption	2.53mW

5.1 Future Work

To conclude the polar transmitter it is necessary fabricate an integrated circuit (IC) to integrate this work in the polar transmitter. Thus, the next step is to do a Monte Carlo analysis to ensure the IC acceptable performance and a good yield.

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