FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

High Power Density DC-DC Converter

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Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

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Resumo

Os conversores CC-CC fazem parte da estrutura base de veículos híbridos e elétricos. A mobilidade elétrica está em crescimento com o desenvolvimento de variados veículos elétricos, desde *skates*, bicicletas e *scooters* a carros, camiões e aviões. Versatilidade e densidade de potência imperam nas necessidades para transferência de energia. Os conversores CC-CC permitem a transferência de energia entre duas fontes de energia (e. g. bateria e barramento de alta tensão). A natureza bi-direcional das transferências supracitadas justifica a necessidade de um conversor bi-direcional de energia.

Tal conversor precisa ainda de ser compacto, de baixo peso e elevada densidade de potência. Os componentes passivos podem ser reduzidos com um aumento de frequência.

Neste documento será proposto uma solução para o problema, cobrindo todos os aspetos relevantes como o desenho, simulação, assemblagem e teste do mesmo, culminando com sugestões de melhorias futuras.

É explorada a tecnologia de semicondutores em Carbureto de Silício (SiC) e um novo circuito de acionamento para os MOSFETs em SiC é desenhado, implementado e testado. O aumento da velocidade de comutação traz complicações que são analisados durante a fase de teste.

O conversor é modelado usando o modelo médio do espaço de estados, linearizado para um ponto de operação com componente dinâmica sobreposta. Perturbações na tensão de entrada e corrente de carga são incluídas no modelo, tais como as principais resistências parasita presentes.

O estudo da solução cobre topologias, métodos de acionamento, comportamento, desenho e tipos de elementos passivos, elementos ativos, circuitos de acionamento, controlo e consequências da operação a frequência elevada.

Embora muito condensado, o autor espera que o documento seja uma boa base de conhecimento para implementação de conversores CC-CC usando tecnologias de semicondutores e métodos de modelação modernos.

Abstract

DC-DC converters are at the core of hybrid and electric vehicles. Electrical mobility is booming with all kinds of electric vehicles, from skates, bicycles and scooters to cars, trucks and planes. Versatility and power density demands for new solutions for power transfer. DC-DC converters enable the transference of energy between two power energy sources (e. g. battery and high voltage bus). The bi-directionality of such energy transfers calls for a bi-directional converter.

Furthermore, and because of the need for compact and low weight solutions, the converter must have high power density. The passive components can be reduced with an increase in frequency.

In this document a DC-DC converter solution will be proposed, covering all relevant aspects from design, simulation, assembly and testing, as well as comments on improvements to be made.

The new SiC semiconductor technology is explored and a new driving circuit is designed, implemented and tested. The increase in commutation speed brings new noise and isolation issues that are addressed during testing phase.

The converter is modelled using a state-space averaging representation, linearised around steady-state duty-cycle and small-signal duty-cycle variations. Input voltage and load current disturbances as well as major parasitic resistances are included in the model.

The study covers topologies, switching methods, passive components operation, design and types, active components, drivers, control and consequences of (high) frequency operation.

Although very condensed, the author hopes this document provides a good insight on DC-DC converter operation using modern semiconductor technologies and modelling techniques.

Acknowledgement

The author would like to thank Prof. Adriano Carvalho for the superior insight on the problem and orientation at all crucial moments.

The AddVolt team went far above all obligations and expectations, supporting and counselling during research, prototyping, testing and writing phases (with special mention to Eng. Miguel Sousa's unconditional mentoring).

Furthermore, the author would like to thank his companion, family and friends for their understanding and support (even when working in weekends and late hours).

José Pedro Fortuna Araújo

"I've found out so much about electricity that I've reached the point where I understand nothing and can explain nothing."

Pieter van Musschenbroek,
describing his experiments with the Leyden jar.

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Abbreviations and Symbols

A	Cross-Section Area
AC	Alternating Current
B	Magnetic Flux Density
BJT	Bipolar Junction Transistor
C	Capacitor or Capacitance
DC	Direct Current
EMI	Electromagnetic Interference
ES	Equivalent-Series
ESR	Equivalent-Series Resistance
f	Frequency
FET	Field-Effect Transistor
GaN	Gallium Nitride
i or I	Current
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
H	Magnetic Line Intensity
JFET	Junction Field-Effect Transistor
L	Inductor or Inductance
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
N	Number of turns on a coil
P	Power
R	Resistor or Resistance
RFI	Radio-Frequency Interference
r	Radius
SBD	Schottky Barrier Diode
SiC	Silicon-Carbide
SJT	"Super-High" Junction Transistor
V	Voltage or Volume
ZVT	Zero Voltage Transition
δ	Skin-Effect
λ	Flux Linkage
μ	Permeability
ϕ	Magnetic Flux
σ	Conductivity

Chapter 1

Scope

1.1 Introduction

This document will provide the basic structure to successfully implementing a high-density DC-DC converter.

In it will be covered what the author proposes to implement, the corresponding state of the art on the subject, the tools intended to be used and a schedule plan.

Given the Thesis will be developed in a company environment, there will be regular meetings with the company's supervisor and less frequent but also periodic meetings with both the company and faculty's supervisor.

In the Thesis dedicated website will be all the relevant content, providing a straightforward way to keep up with the work progress.

1.2 Project Specifications

The project's main objective is developing a 40kW DC-DC Converter able to manage the flow of energy between a battery bank and a regenerative break system.

In a very general sense, the project will consist on the design of the Converter's hardware (electrical circuit) and software (control and microcontroller program), simulation, implementation, testing and improvement solutions.

It is expected a study in new semiconductor technologies that can eventually enable an increase in frequency and consequently increase power density by reducing passive component size.

Chapter 2

State of the Art

2.1 Introduction

A DC-DC converter is in its essence a power transfer system with ideally lossless ratio conversion of voltage/current.

Its typical function is as an intermediary block to transfer energy from an energy supplying system to an energy consuming system.

In order to design a converter, especially one with moderately high-power and density, it is crucial to understand a vast range of concepts and areas. As a direct consequence (and to a point contradictory) the concepts can not be studied with too much depth because of the limited available time in the Master Dissertation.

In this document, the author will try to give an extremely condensed view on the main topics one must grasp to be able to make conscious decisions when designing a DC-DC converter.

2.2 Relevant performance indicators

When analysing the pros and cons of each solution, it is crucial to understand what are the key factors that determine the quality of each solution.

Price The price of the solution is relevant, as is its variation, depending on the massification of the production or the evolution of the technology (specially if it is recent).

Power Density The ratio between power delivery and volume of the converter is relevant on several applications, being the automotive industry one where this is an important factor.

Scalability The scalability of the converter is the ease of adapting the solution to a different power regime.

Weight Closely related to Power Density, the weight of the converter is important on automotive applications as well.

Reliability The reliability of the converter will determine its resistance to failures and its lifetime.

Efficiency The efficiency of the converter is crucial, as it is an intrinsic performance indicator of the converter: its job is to transfer energy, and the efficiency will describe how well the job is done.

Safety Addresses issues such as isolation or rest state of switches (normally-on or normally-off).

Control ease The simplicity of the solution will provide easier manipulation by its users.

Noise and energy quality The power factor and amount of ripple influence the durability of the modules and the delivery of power.

2.3 Topologies

This section will address the different converter topologies. The switches are considered ideal and no device technology will be chosen in the topology analysis (apart from the use of diodes).

The converters presented will be grouped by their isolation characteristics. Because the way energy is transferred through the converter is also relevant, such information will be presented whenever deemed necessary.

The non-isolated topologies are not galvanic-isolated. Consequently, the converter will have less components, simpler analysis and have less failure points. Because it is not isolated, it will not provide a safety guard between input and output of the converter.

The capacitor isolation is a galvanic isolation that blocks DC current.

The transformer isolated converters have an extra degree of freedom associated to the transformer turns ratio $\frac{N_S}{N_P}$. However, a transformer is an additional lossy element, and one with several concerning design aspects: self and mutual inductances, core saturation, isolation (and stray capacitances) and losses. Using a transformer greatly increases size, price, losses and consequently limits power density.

In fact, apart from the converters listed below, and keeping the turns ratio unitary, all the converters studied can only supply an output voltage equal or in some cases double of the input voltage [3].

Because of the issue above, and/or its uni-directionality, all other transformer isolated basic solutions were considered unsuitable by the author.

Among the discarded converters were:

- Forward (simple, two-switch and active clamped) and Isolated Half-bridge- gain is $\frac{N_s}{N_p}D$ [3] (not inherently buck-boost) and are not bi-directional

- Isolated Full-bridge and Push-Pull and Phase Shift ZVT- gain is $2\frac{N_s}{N_p}D$ [3] (not inherently buck-boost) and are also not bi-directional

2.3.1 Basic Buck-Booster

The Buck-Booster is able to provide in its output voltage gains with magnitude both smaller and bigger than 1.

Like most of the converters, the energy storage element is an inductor.

The converter generates relevant input and output disturbance, increasing the importance of the input and output capacitive filters.

The diode and switch can be connected to either positive or negative rail of the input and output.

Replacing the diode with a switch with complementary duty-cycle, the converter becomes synchronous and bi-directional.

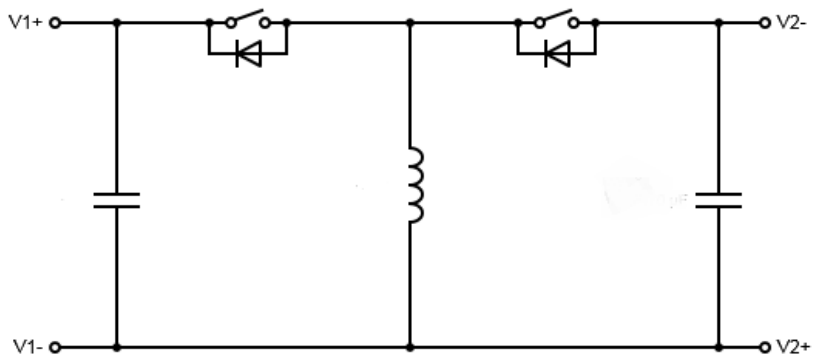


Figure 2.1: Buck-Booster

The energy transfer is of V-I-V type: the input and output sources are treated as voltage sources, and the inductor transfers energy through the form of current.

2.3.2 Ćuk

The Ćuk converter is a fairly recent topology (29th of January, 1980) designed by Slobodan Ćuk.

The input and output noise generated are much smaller than in the buck-booster because the supply of energy is constant (the sources are treated like current sources) instead of being pulsed like in the buck-booster.

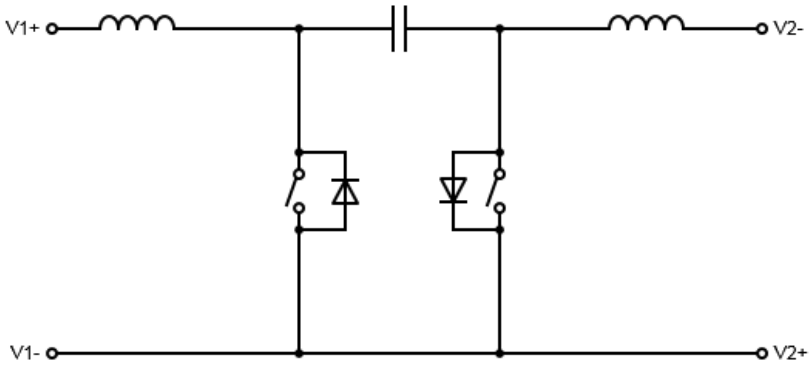
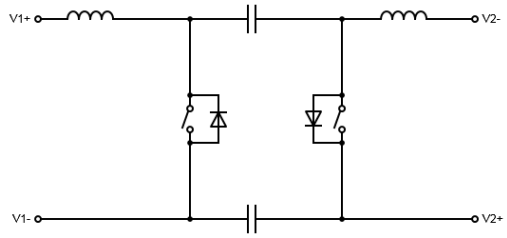
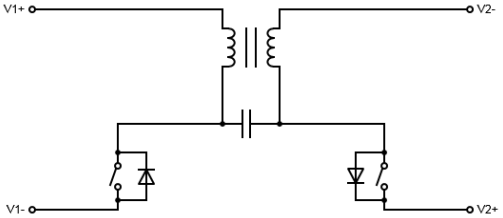


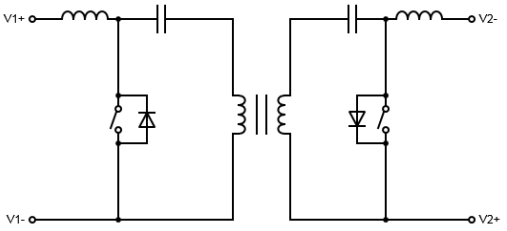
Figure 2.2: Ćuk - Basic topology



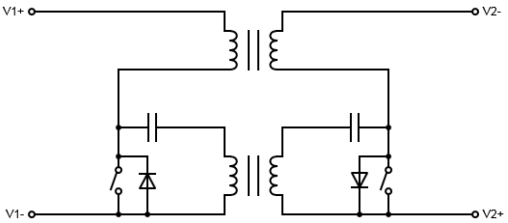
(a) Ćuk - Extra capacitor for isolation



(b) Ćuk - coupled inductors



(c) Ćuk - transformer isolated



(d) Ćuk - Inductor coupled and isolated

Figure 2.3: Ćuk topology variations

The converter can be seen as a boost converter cascaded with a buck converter.

Its distinctive feature is the use of a capacitor as the energy storing passive component instead of an inductor. It is also possible to operate the converter in either current or voltage discontinuous mode.

The energy transfer is of I-V-I type: the input and output sources are treated as continuous current sources, and the capacitor transfers energy through the form of voltage.

Because the inductors have the same waveform (only different average currents), they can be coupled to lower the output ripple even further (b).

A transformer can also be used to isolate input from output (c).

(d) shows a coupled inductor, transformer isolated Ćuk converter.

2.3.3 SEPIC

The Single-Ended Primary-Inductor Converter is a Ćuk variation, where the inductor and Switch are interchanged on one side of the converter [4]. The converter keeps its bidirectional properties, but the output loses the continuous current property.

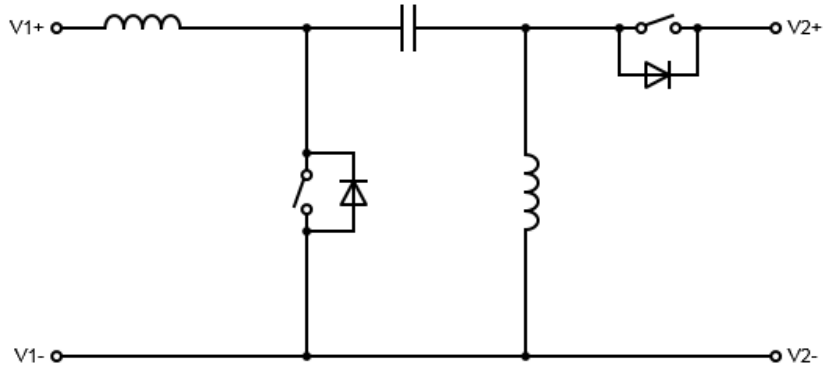


Figure 2.4: SEPIC/Zeta Converter

Just like for the Ćuk converter, the inductors can be coupled and the input isolated from output.

2.3.4 Zeta

In all the topologies the diodes are replaced with controlled switches because of the bi-directionality necessity. Because of this, the Zeta converter is the same as the SEPIC converter, only with the input switched with the output.

Consequently, based on the properties of both sources (e.g. battery power bank and motor/generator), one can choose between the SEPIC or Zeta configurations [4].

2.3.5 FlyBack

The Flyback converter is a Buck-booster where the inductor has been replaced with a transformer. The turns ratio can be tampered with to optimize steady-state operation.

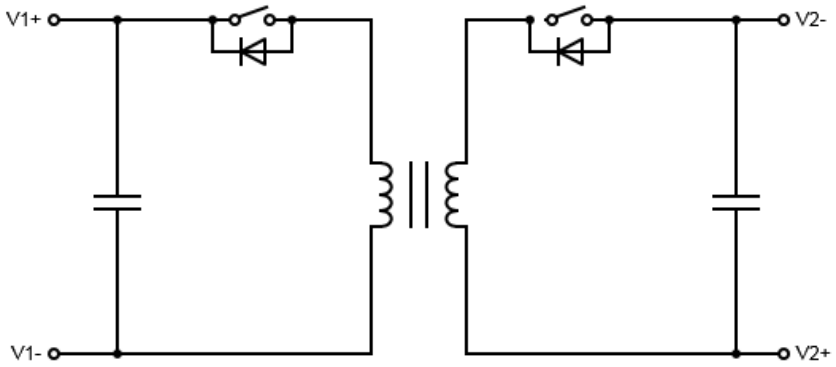


Figure 2.5: Flyback Converter

2.3.6 Split-Pi

The Split-Pi is no more than a mirrored converter: two active buck or boost (which are in fact the same, only input swapped with output) with outputs connected to the same intermediary buffer capacitor. It is the non-inverting Ćuk:

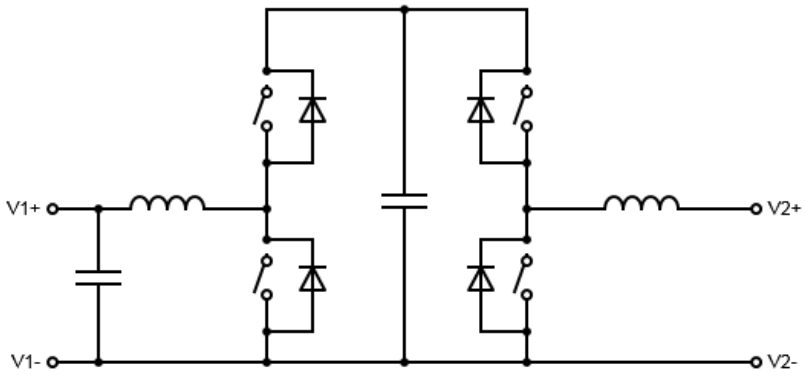


Figure 2.6: Split-Pi Converter

2.3.7 Comparison

The comparison of the converters is based on the arrangement of capacitors, inductors, transformers and switches. Different topologies use different storing elements, e. g., a capacitor able to store the same energy as an inductor will be smaller and lighter. It is based on this assumptions that the table below was created. The comparison of topologies was based on 10 parameters:

- Price - It was used as a rough estimation that transformers and switches were much more expensive than inductors, which in turn were more expensive than capacitors
- Power density - Transformers and extra switches reduce power density

- Scalability (power and size) - Transformers, limit the total power of the converter. Also, more switches in the topology make it more resistance to power scaling
- Weight - Capacitors are lighter than inductors, and transformers are heavier
- Reliability - Capacitors are less reliable than inductors. Adding a transformer adds complexity and reduces reliability
- Efficiency - This issue will be covered with more detail in posterior chapters, but as a rule of thumb, transformers and inductors introduce losses more expressive than those of capacitors.
- Safety - Transformers add isolation and therefore limit the damage in case of converter malfunction.
- Control ease - the lower number of passive elements, the lower order the control plant is.
- Noise - Input and output disturbances. The topologies with input and output inductors filter the current, whereas the other topologies deliver pulsed current.
- Inovation - More recent topologies leave more space for improvement and inovation, a key aspect in the Dissertation.

Topology	Price	Power Dens.	Scalab.	Weight	Reliab.
Buck-boost	/	/	-	/	+
Ćuk	+	+	/	+	-
SEPIC/Zeta	+	+	/	+	-
Flyback	-	-	-	-	/
Split-Pi	-	-	+	-	/

Table 2.1: Topologies' comparison - part 1

Topology	Eff.	Safety	Control	Noise	Inov.
...Buck-boost	/	-	+	-	-
...Ćuk	+	-	-	+	+
...SEPIC/Zeta	+	-	-	/	+
...Flyback	-	+	/	-	-
...Split-Pi	-	+	/	+	-

Table 2.2: Topologies' comparison - part 2

2.4 Soft-switching - Minimizing switching-losses

In a converter, the factors degrading its efficiency are the losses in the active and passive components.

The losses in switches are the most important and can be divided into two categories - conduction and switching losses. The first is a consequence of the on-resistance of the switch, while the latter is caused by delayed action of the switches: when going from off to on, the current rises before the voltage drops and when going from on to off, the voltage rises before the current drops.

Furthermore, there is a direct proportion between the losses in a switch and its necessary power rating.

Soft-switching reduces transient spikes, increasing the reliability and durability of the components.

While the conduction losses are set by the switch, the switching losses can be minimized by several approaches, being the main ones described below.

2.4.1 Quasi-resonant converters

Quasi-resonant converters make use of the discontinuous mode of the converters, when the energy carrier passive element (inductor or capacitor) discharges and the voltage on the switches start oscillating. By turning on the switch during one of the low voltage valleys, the losses can be reduced. However, this method introduces irregularity in the switching times and necessity of monitoring every switch voltage curve.

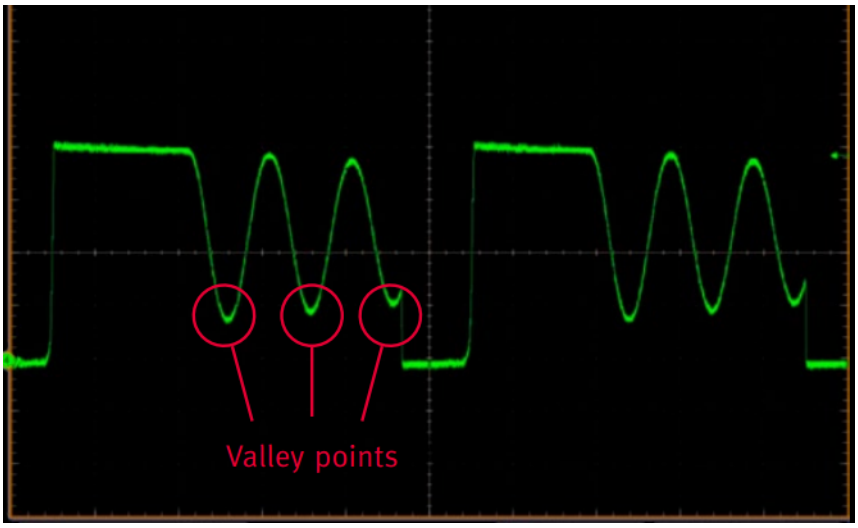


Figure 2.7: Quasi-resonant converter switching voltage

2.4.2 Zero Current and Voltage Switching

As mentioned above, when turning off a switch, the current drop delay is responsible for the power dissipation. Increasing the hard-switching $\frac{dv}{dt}$, while thinning the switch power loss, has several

drawbacks: an increase in driving current, switch stress and transient spikes.

The alternative is providing an alternate path for the flow of current when the switch is turned off.

The most simple and straightforward alternative is adding a small parallel capacitor - when the voltage across the switch starts rising, the previously uncharged capacitor starts drawing current to keep up with the voltage imposed. Ideally, the capacitance should be such that at the $\frac{dv}{dt}$ the capacitor is able to suck the maximum current that can flow through the switch. On the other side, when turning on the switch, the capacitor will gradually short-circuit, discharging through the switch. Thus, this solution is not viable without further alterations.

When turning on the switch, it is then necessary to either discharge the capacitor through another path or alternatively limit the current flow through the capacitor.

The first alternative is implemented differently according to the topology chosen. However, the basic principle behind it implies pulling from the capacitor more current than its branch can supply through an auxiliary switch and some kind of resonant circuit [1] [5] [6] [7]. This means the auxiliary switch will need to take similar current levels to the ones in the main switch, although it is for a shorter period.

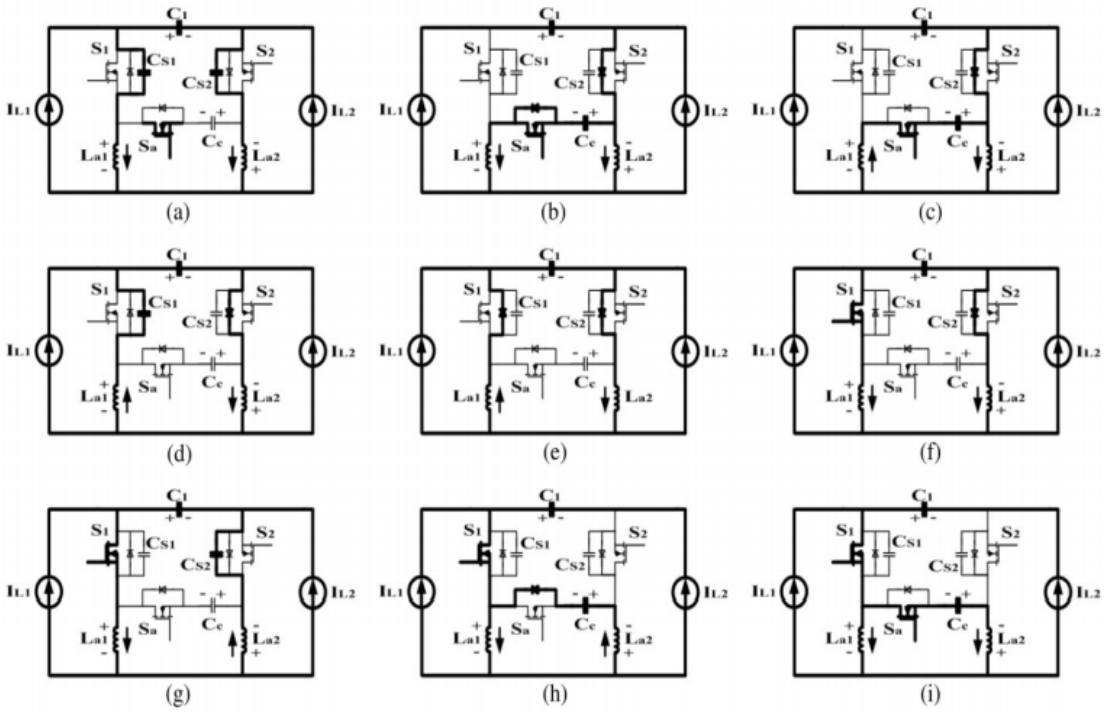
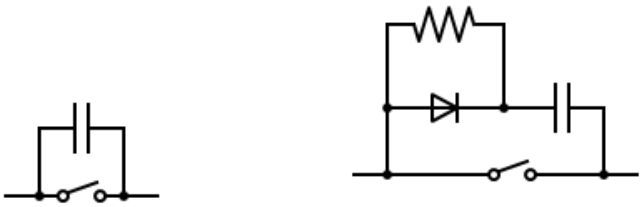


Figure 2.8: Proposed ZVS Ćuk converter in [1] and its switching sequence

The second alternative forces the energy at a slower pace through a different path when discharging the snubber capacitor.

With the RCD snubber the capacitor charges with current supplied by the diode and discharges at the rate imposed by the resistor. Unfortunately, and because the diode has a non-ideal positive drop-voltage, the capacitor will start charging through the resistor until the voltage in the switch is

high enough for the diode to be forward-biased. This leads to increased power loss in the switch on turn-off.



(a) Capacitor snubber (b) RCD snubber

Figure 2.9: Passive snubbers

2.5 Passive components

The passive elements are two-terminal elements unable to introduce net energy into the system. The study will focus on the three most frequent: resistors, capacitors and inductors. The transformers are particular case inductors.

2.5.1 Resistors

A resistor imposes electrical resistance, dissipating energy directly proportional to the instantaneous voltage imposed and current flowing through it. It is a dissipative element, so it must be avoided if the efficiency is a concerning issue.

2.5.2 Capacitors

The capacitor stores energy in an electric field. It has at least two electrical conductors (generally metal plates) and a dielectric between them. Its storage performance depends on the constitution of the dielectric, plate geometry (area) and distance.

Ideally, they are non-dissipative, provide isolation, block DC current and are resilient to voltage changes.

Non-ideally, they have internal leakage and equivalent-series resistance (ESR) and series inductance (ESL) (with increased relevance with frequency increase). With exception of special designed capacitors, at their breakdown voltage the dielectric starts conducting - besides losing their capacitor function, they also fail at providing isolation.

They come in various types, depending on the need of polarity, operating voltage, current, temperature dependence, reliability or other parameters.

2.5.2.1 Capacitor types

- **Electrolytic cathode capacitors** [8] - can have aluminium, tantalum or niobium anode. They are asymmetric and polarized. Because the cathode is an ionic conducting liquid (electrolyte) their volumetric density is higher but the performance is seriously compromised: higher leakage current, limited temperature operating range, higher parasitic resistance and inductance and lower capacitance stability and accuracy. They are susceptible to ageing - either by liquid evaporation or lack of voltage excitation.

  The most common are aluminium - which are more susceptible to ageing due to lack of voltage applied, and tantalum - with higher accuracy and price but more susceptible to breakdown in the event of voltage spikes (sometimes exploding violently).

  Electrolytic capacitors' main advantage is their high volumetric density. Their main application is in high current, low frequency circuits, namely power supply filters. Their use with a paralleled faster, lower ESR and smaller capacitor works particularly well.

- **Ceramic dielectric** [9] Ceramic capacitors have low ESR and ESL, allowing operating frequencies superior to electrolytic capacitors. Depending on the dielectric type (NP0, X7R, X5R or Y5V), there can be voltage and temperature de-rating. The ceramic technology enables fabrication of EMI/RFI supression, X2Y, feed-through and power capacitors.

- **Film dielectric** [10] - Film capacitors have self-healing properties and ability to handle high pulse currents. Thus, a breakdown or short does not destroy the component. This makes film capacitors a good candidate for snubber circuits, where a failure can cause the destruction of the switch. They are also suitable for RFI/EMI suppression.

- **Supercapacitors** [11] - Highest density, polarised, low voltage capacitors. Supercapacitors rely on both double-layer (Helmholtz principle, electrostatic charge) and pseudocapacitor (electro-chemical energy storage through Faradaic current). Because of their low voltage they are not suited for the DC-DC conversion. Instead, energy storage is their market, competing with the ubiquitous batteries.

- **Class X and Y** [12] - Capacitors class X and Y certified provide galvanic isolation, guaranteeing that in breakdown the terminals are isolated.

2.5.2.2 Equivalent model

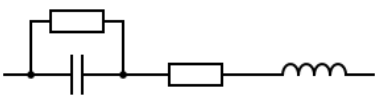


Figure 2.10: Capacitor model

2.5.3 Inductors

The inductor stores energy in a magnetic field. It is made of a conducting wire, usually wound into a coil in various configurations. Its storage performance depends on the geometry of the coil and the material used for the core (to increase the magnetic conductivity and field). Inductors are accepted as the duals of capacitors:

Ideally, they are non-dissipative, are resilient to current variations and have zero DC voltage drop.

Non-ideally, they have an ESR inherent to the wire constitution and core losses. Because of the wire resistance, the turns of the coil have different potentials, creating parasitic capacitances between them. With an increase in frequency, due to skin-effect, the wire resistance increases (and consequently the capacitance of the inductor). If the frequency is increased past its resonating frequency, the inductors behaviour becomes more similar to that of a capacitor.

Their main disadvantages are their sensitive deviation from ideal behaviour, EMI radiation and size.

The main losses in and inductor come from the skin-effect resistance and manifestation of eddy currents on the core (that dissipate the stored magnetic energy through the core's electrical resistance as heat).

In the following sections, an introduction to electromagnetic principles will be covered, as well as a list of cores, inductors and transformer (special case inductor) types.

2.5.4 Electromagnetic principles

To be able to select (or design!) an inductor or transformer, it is crucial to have at the very least a basic understanding on electromagnetism and design of inductors and transformers. Only in the *Passive Components* section will the different types of inductors and transformers be covered.

This section is based on the book on Transformers and Inductors for Power Electronics [13].

In a very simplistic approach, the main phenomena of interest can be introduced as follows:

- A current flow generates a magnetic field.
- Changes in a magnetic field generate electromotive force (i.e. voltage) across the elements under the magnetic field's influence.

Magnetic fields are represented by closed lines. A straight conductor creates a field whose lines are concentric with the conductor and whose direction follows the "right-hand rule". The intensity of the magnetic lines $\mathbf{H}$ is constant for each line. The magnetic flux density $\mathbf{B}$ depends on the medium of permeability μ:

$$\mathbf{B} = \mu \mathbf{H} \tag{2.1}$$

For free space, $\mu_0 = 4\pi \times 10^{-7} H/m$. Magnetic media can have permeabilities 400 (ferrites) to 10 000 (silicon steel) times greater.

For a single conductor with constant flowing current i, the magnitude of $\mathbf{H}$ can be easily deduced geometrically:

$$H(r) = \frac{i}{2\pi r} \tag{2.2}$$

Regarding Electromagnetic induction:

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{2.3}$$

$$\oint_C \mathbf{E} \cdot dl = -\frac{d}{dt} \int_S \mathbf{B} \cdot \mathbf{n} da \tag{2.4}$$

Stating that the electric field intensity $\mathbf{E}$ around the closed loop C is equal to the rate of change of the magnetic flux density. $\mathbf{n}$ is the unit vector normal to the surface.

2.5.4.1 Cores and Windings

Ferromagnetic materials have a magnetic permeability μ superior to free space's (i. e. vacuum) μ_0. Thus, the magnetic permeability of a material is given relative to vacuum's permeability (μ_r):

$$\mu = \mu_r \mu_0 \tag{2.5}$$

Therefore μ_r can be seen as an amplification factor, enabling a greater flux density $\mathbf{B}$ for the same intensity $\mathbf{H}$. However, above the saturation flux density B_{sat}, the material behaves like air ($\mu_r \to 1$).

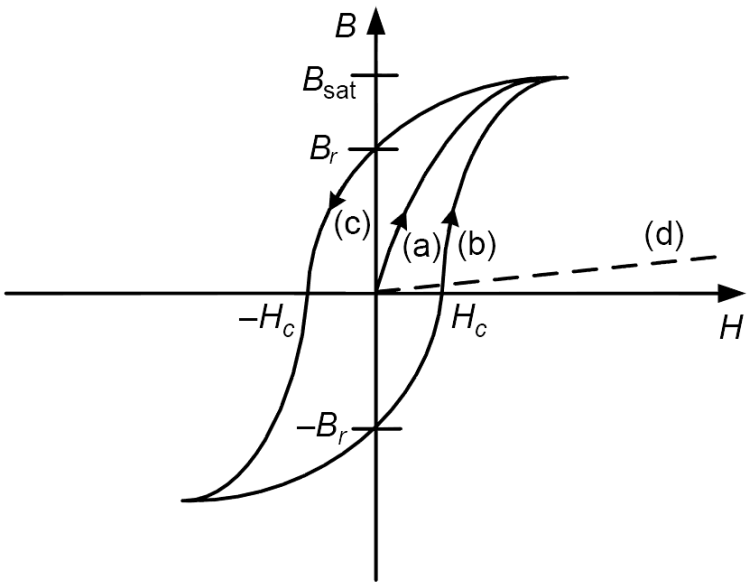


Figure 2.11: B-H Magnetization Curve

The magnetic behaviour of a material can be explained by the magnetization curves:

- (a) - From a resting point, slowly increasing H orients the magnetic domains quasi-linearly until the material starts saturating, consequence of the scarcity of magnetic domains to align.
- (c) - The magnetic domains partially retain their orientation (a magnetic memory), explaining why an inversion in the H polarity results in a positive B (B_r - remnant magnetization) when H crosses zero.
- (b) - This curve depicts the dual of (c). The B_r is negative in this case, for obvious reasons.
- (d) - Line representing vacuum's B-H magnetizing curve

H_C locates **H** magnitude to return **B** to zero (i. e. non-magnetized state).

Hard magnetic materials (magnets) have higher B_r and H_C, logically being harder to demagnetize.

The permeability is sensitive to temperature. When the temperature is high enough, $\mu_r \to 1$ and the material behaves paramagnetically. This is called Curie temperature, and the values for ferrites can be low enough to be relevant (200°C), making this an important design parameter.

Losses in inductors and transformers A first approach is given here, and will be detailed in the chapter dedicated to frequency considerations.

Copper Losses at DC are related to the resistance of the wire R_{DC}. At higher-frequencies, the current is pushed to the surface of the conductor due to the appearance of an AC magnetic field. This is known as skin-effect, and the equivalent thickness of the annulus where the current is flowing is the skin-depth δ, dependent on frequency f, permeability μ and conductivity σ, and given by:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{2.6}$$

The AC resistance R_{AC} of a conductor with radius r_0 can be approximated by:

$$R_{AC} = R_{DC}\left(1 + \frac{(r_0/\delta)^4}{48 + 0.8(r_0/\delta)^4}\right) \tag{2.7}$$

At high frequencies, the magnetic field of a conductor can also influence another, increasing its resistance - known as proximity effect, which is a specific type of crosstalk.

Both copper losses and the proximity effect can be minimized by using individually insulated stranded wire (Litz wire).

Hysteresis Losses are a consequence of the resilience of the magnetic domains to reorientate. The loss in one cycle is equal to the product between the area inside the B-H magnetization curve and the volume V of the core. When the cycle loss is multiplied by the operating frequency f, we get the hysteresis power dissipation:

$$\int H \, \mathrm{d}B \times V \times f \tag{2.8}$$

Eddy Current Losses are consequence of current flow in the cores. This effect is most seen on silicon steel, but at high enough frequency, also ferrite starts conducting. The current flow happens around the core depending on the direction of the magnetic field. The losses are consequence of the resistive path they follow. Splitting the core by laminating it with an insulating material reduces the current path perimeters, thus reducing Eddy Current Losses.

Core materials

- **Ferrites** are the most used in power electronic devices. Amongst the most common types are Mn-Zn and Ni-Zn:
  - Ni-Zn has high electrical resistivity (around $10k\Omega m$), making it suitable for operating frequencies over $1MHz$
  - Mn-Zn has low resistivity (around $1\Omega m$), but higher permeability and saturation flux density

  The low Curie temperature is a challenge when designing for high current applications. When compared to laminated or powdered iron cores, the ferrites' saturation flux density is significantly lower.

- **Laminated Iron Alloys** are used in low to medium frequencies applications (up to $20kHz$), therefore they are out of the scope of this study, where high frequency is mandatory to decrease component size.

- **Powder Cores** are made of a powder mix of iron or iron alloy mixed with and insulation material. The insulation material results in a distributed gap, reducing the effective permeability, thus increasing the maximum DC current the core can handle without saturating. Molybdenum permalloy (MPP) and those with carbonyl iron are among the most common materials used. Powder cores are usefull for applications where an air gap is advantageous, such as energy storage inductors.

- **Amorphous Alloys** have resistivity lower than ferrite but higher than silicon steel. The saturation flux density is higher than ferrites and so is the Curie temperature. They are used in high-power inductors, although sensitive to high-frequency.

- **Nanocrystalline Materials** have high saturation flux density, resistivity and Curie temperature. They are used in applications up to $150kHz$.

Materials	Ferrites	Nanocrystalline	Amorphous
Permeability	2200	15 000	10 000 - 150 000
B_{peak}(T)	0.49	1.2	1.56
$\rho(\mu\Omega m)$	10×10^6	1.15	1.3
Curie Temp (^{o}C)	210	600	399
Power loss (mW/cm^3)	288 @ 0.2T, 50kHz	312 @ 0.2T, 100kHz	294 @ 0.2T, 25kHz

Table 2.3: Soft magnetic materials - part 1

...Materials	Si iron	Ni-Fe (permalloy)	Powdered iron
...Permeability	5000 - 10 000	20 000 - 50 000	75
...B_{peak}(T)	2.0	0.82	0.6 - 1.3
...$\rho(\mu\Omega m)$	0.48	0.57	10^6
...Curie Temp (^{o}C)	745	460	665
...Power loss (mW/cm^3)	5.66 @ 1.5T, 50Hz	12.6 @ 0.2T, 5kHz	1032 @ 0.2T, 10kHz

Table 2.4: Soft magnetic materials - part 2

2.5.4.2 Inductance

When considering a single coil wound up on a basic ring shaped magnetic core, taking l_c and H_c as the average perimeter and magnetic field intensity:

$$H_c l_c = Ni \tag{2.9}$$

where i is the current flowing through the N turns of the coil.

Magnetic flux ϕ is defined as

$$\phi = B_c A_c \tag{2.10}$$

where A_c is the cross-section of the magnetic circuit.

Flux linkage may be seen as the influence of the magnetic flux on a coil:

$$\lambda = N\phi \tag{2.11}$$

The reluctance $\mathscr{R}$ of a magnetic piece is related to its shape and material such that:

$$\mathscr{R} = \frac{l_c}{\mu_0 \mu_r A_c} \tag{2.12}$$

and

$$Ni = \phi \mathscr{R} \tag{2.13}$$

Self and Mutual Inductance A changing magnetic flux produces a voltage e in the coil:

$$e = -N\frac{d\phi}{dt} = -\frac{d\lambda}{dt} \tag{2.14}$$

The voltage produced in a nearby $coil_2$ by a $coil_1$:

$$e_2 = -\frac{d\lambda_2}{dt} = -\frac{d\lambda_2}{di_1}\frac{di_1}{dt} = -M_{21}\frac{di_1}{dt} \tag{2.15}$$

It is proven that the mutual inductance M is the same for both coils: $M_{21} = M_{12} = M$, which yields:

$$M = \frac{d\lambda_2}{di_1} = \frac{d\lambda_1}{di_2} \tag{2.16}$$

Apart from the mutual inductance, the coil's self inductance L is given by:

$$L = \frac{d\lambda}{di} \tag{2.17}$$

Yielding

$$e = \frac{d\lambda}{dt} = L\frac{di}{dt} \tag{2.18}$$

Through some equation manipulation, we can dessicate inductance L:

$$L = \frac{d\lambda}{di} = \frac{Nd\phi}{di} = \frac{N^2BA}{Ni} = \frac{N^2BA}{Hl} = \frac{N^2\mu_0\mu_r A}{l} = \frac{N^2}{\mathscr{R}} \tag{2.19}$$

We can infer that the self inductance is dependent on the number of turns in the coil quadratically and the design of the core.
The power stored in an inductor is given by

$$P = \frac{1}{2}Li^2 \tag{2.20}$$

Inductor design We now have the basic tools to start designing an inductor, aiming for:

- Linear operation for the desired current range (keeping B below B_{SAT})
- Achieving the inductance value needed for the converter
- Minimizing volume and losses
- Reliability at operation

Using an air core (i.e. no core), there would be no field saturation. However, the magnetic field would not be contained and the high air reluctance would affect the coil inductance strongly, forcing the number of turns (and volume) to increase drastically.

Using a low reluctance core would provide higher inductance, but at the cost of a short current range operation.

The design then focuses on the balance between the magnetic gain of the core and the space available to wound up the coil. This is possible because, as we have seen, the H in the coil is linearly dependent on the number of turns, and the inductance is quadratically dependent on it.

The manipulation of the core's reluctance can be achieved by using different core materials, shapes and the introduction of air gaps (which can be loosely seen as a core material).

Transformer design With two coils wound up on a single magnetic core, and assuming the magnetic flux is contained within the core:

$$\frac{v_1}{v_2} = \frac{N_1}{N_2} \tag{2.21}$$

because the variation of flux in the first coil will be entirely felt on the second coil.

The mmf on the system is

$$H_c l_c = N_1 i_1 - N_2 i_2 \tag{2.22}$$

For an ideal core with high permeability:

$$N_1 i_1 = N_2 i_2 \tag{2.23}$$

Such that ratio a is:

$$\frac{v_1}{v_2} = \frac{i_2}{i_1} = \frac{N_1}{N_2} = a \tag{2.24}$$

Because of energy conservation, power is independent of a - $V_1 i_1 = V_2 i_2$. However, impedance as seen from the primary is not:

$$Z_2 = \frac{v_2}{i_2} = \frac{v_1}{i_1} a^{-2} \tag{2.25}$$

It is important to note that there is a part of the coil that produces flux not linking the other coil - it is called the leakage inductance L_l. This effect makes the flux on each coil dependent on its inductance, leakage inductance and mutual inductance.

The mutual inductance M is dependent on L_1 and L_2 (excluding the leakage induction):

$$M = \sqrt{L_1 L_2} \tag{2.26}$$

The coupling coefficient k tells how much of the coil total inductance L_{11} is contributing for the flux in the secondary coil:

$$k_1 = \frac{L_{l1}}{L_{11}} \tag{2.27}$$

And

$$k = \sqrt{k_1 k_2} \tag{2.28}$$

Which yields

$$M = k\sqrt{L_{11} L_{22}} \tag{2.29}$$

Laminated Core They are the most common type of transformers, present in both low voltage and power electronics.

Toroidal As with the toroidal inductors, these transformers have the lowest leakage flux. They can be smaller than the rectangular transformers for the same power rating, but they are more expensive due to the higher complexity in winding.

Autotransformer The autotransformer does not provide isolation. Instead, it is made of a single inductor with tapped point(s) along it.

Planar Transformer Planar transformers have a reduced height and consequent bigger area. They have good heat dissipation characteristics and are mainly used in military and aerospace designs.

2.5.4.3 Inductor types

- Laminated core inductor - Minimizes eddy currents by laminating the steel core into thin sheets parallel to the field.
- Ferrite core inductor - Because the ferrite is non-magnetic, no eddy current flows, making it a suitable solution for high-frequency and density.
- Toroidal core inductor - Shaping the core as a toroid instead of a rod-like shape, the magnetic circuit can be closed, reducing the flux leakage.
- Choke - Designed to block high-frequency AC currents, it has small power losses.
- Ferrite bead - It is a special small choke that dissipates the high frequencies in a ferrite core. It is sometimes used on the gates of semiconductors to reduce switching noise.

2.5.4.4 Equivalent model

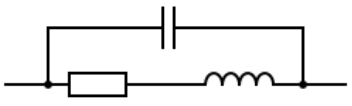


Figure 2.12: Inductor Model

2.5.5 Capacitor and Inductor Comparison

A quick analysis can be made to understand the differences in using a capacitor or inductor as a storing element:

Consider a 50kW converter with input voltage (V_{in}) = 100V and output voltage (V_{out}) = 350V.

In a buck-booster (and Ćuk converter), the duty cycle would be:

$$D = \frac{V_{out}}{V_{out} + V_{in}} = \frac{350}{450} \tag{2.30}$$

The average current going through the inductor would roughly be:

$$\frac{V_{out}}{1 - D} = 650A \tag{2.31}$$

Which yields:

$$E = \frac{1}{2} L I^2 = 211k\, L \tag{2.32}$$

For the Ćuk converter, the voltage in the capacitor is

$$V_{in} + V_{out} = 450V \tag{2.33}$$

which yields

$$E = \frac{1}{2} C V^2 = 101k\, C \tag{2.34}$$

At first sight, it can be seen that for the same application, the operating voltage of the capacitor is much more reasonable than the operating current of the inductor. Furthermore, it is observable that the stored energy in the inductor is approximately twice as big as the capacitor's. However, a capacitor with $C_{capacitor} = 2L_{inductor}$ would be much smaller and inexpensive.

2.6 Semiconductor devices

[14] Semiconductor devices are the main element in electronic circuits and their importance comes from their ability to control (at least to some level) the flow of electricity.

Below will be given a brief introduction of the main semiconducting devices as well as their basic behaviour.

2.6.1 Diode

It is the simplest of the semiconductor devices.

Ideally conducts current from anode to cathode (i.e. when forward-biased) with zero voltage drop the terminals, blocking current from cathode to anode and sustaining arbitrary voltage (i. e. when reverse biased).

Non-ideally, when conducting current from anode to cathode, there is a forward voltage drop V_F, there is a limited breakdown voltage V_B the diode can sustain from cathode to anode before breaking down and starting conducting and there is a residual reverse current I_R when the diode is reverse-biased.

When going from reverse-bias to forward-bias, the current rises before the voltage crosses zero, during a time t_{FR} (forward recovery time).

The reverse recovery time is slightly more complex, because the current goes from positive, crosses zero and continues to negative values, only then recovering back to zero (or close) in a time t_{RR} (reverse recovery time). This timings limit the maximum switching frequency of the device.

The power diode is turned on and off by the power circuit and is therefore not controllable by an external control signal. This is diode's strength and weakness and in the scope of the bi-directional converters, diodes are mainly used in snubber circuits to shape the switching waveforms of other semiconductors.

2.6.2 Thyristor

Thyristors are switches with controlled turn-on (and turn-off, for Gate turn-off thyristors).

Amongst the semiconductor families, they have the slowest commutation speeds, and therefore are not used in DC-DC converters, where higher frequencies are a necessity.

Consequently, their study is not relevant for this scope. However, SIC thyristors are under study, which may prove a viable solution in the future.

2.6.3 Bipolar Junction Transistors

Bipolar Junction transistors (BJT), similarly to thyristors, are current controlled devices. BJTs are faster than thyristors but have an inferior power rating. However, Insolated gate bipolar transistors (IGBT) have superior power rating for the same switching speed ratings, while Field-effect transistors (FET) have superior switching speed for the same power rating. For this reason, and for the vast majority of applications, BJTs can be replaced with IGBTs and FETs for a better performance without any significant trade-off. For this reason, IGBTs and FETs will be the main focus of the switches families study.

2.6.4 Field-effect Transistors - FET

Field-effect transistors enable or disable the conduction of current by using an electrical field to shape the conduction channel. FETs are unipolar devices, meaning the conduction is either through majority carriers or minority carriers (unlike bipolar devices, using both). This means their inherent ability to conduct current is lower.

Unlike bipolar devices, their thermal coefficient is negative (an increase in temperature reduces current conduction), which enables the paralleling of devices, as they will balance the current distribution.

FETs are the fastest family of switching devices, and together with their simple gate control mechanism, they become the main choice for high-frequency applications and a competitive solution in medium to high-power applications.

2.6.5 Power MOSFET

Power MOSFETs are an enhancement of the low power MOSFETs, replacing the lateral with a vertical channel. The gate is isolated from the power circuit, although current can leak because of the layers capacitances.

Its inherent body diode is suitable for bi-directional converters, although its poor performance calls for a parallel external diode in higher power operation.

Besides the capacities between the three terminals (one of which can unintentionally turn-on the device), there is also a parasitic BJT that can also turn-on the device in the presence of a rapid voltage change , debilitating the device.

It is normally-off when no voltage is applied, which is an attractive feature safety-wise.

2.6.6 JFET

JFETs are the simplest FET devices. They do not have an intrinsic body diode, and are typically depletion-mode (inverse logic), becoming a bigger design challenge safety-wise.

2.6.7 IGBT

IGBTs are the most recent switching devices amongst the mentioned above. They are composed of a MOSFET cascaded with a BJT in a Darlington configuration. The IGBT combines the MOSFET voltage control with the good on-state characteristics of the BJT. Although the turn-off tail is shorter than BJT's (and consequently faster), it is still considerable, making it a slower device than MOSFETs, and unsuitable for frequencies above 100kHz. On the other-hand, their current and voltage handling is superior to MOSFETs. The higher-current density makes it the prime choice for medium-high power applications where switching frequencies ranging from $20 - 100kHz$ are at play.

2.6.8 Silicon Carbide enhancements

Silicon Carbide (SiC) technology, as an alternative to Silicon, has changed the perspective on the switching devices [15]. It enables the fabrication of devices with smaller parasitic capacitances and small temperature coefficients.

SiC produces faster and higher power-density devices. Unfortunately, the material is not as versatile as silicon, limiting the devices where it is applicable and currently produced to:

- **SJTs** - a "Super-High" current gain bipolar junction transístors fabricated by GeneSic.
- **JFETs** - fabricated by Infineon and USCi.
- **MOSFETs** - fabricated mainly by Cree, ROHM, ST and several other.
- **Schottky Barrier Diodes - SBD** - fabricated by most of the SiC producers.

For single-packaged devices:

Device	Voltage rating	Current rating	Thermal coefficient	Producer
SJT	600	100	positive	GeneSic
JFET	1200	38	negative	USCi
MOSFET	1200	90	negative	Cree

Table 2.5: New Technology Devices Comparison

MOSFETs, besides their easier and reliable control are the best choice among the three externally controlled devices (SJTs, JFETs and MOSFETs).

2.7 Semiconductor materials

[16] Semiconducting materials stand between conductors and insulators in terms of electrical conductivity. They allow the fabrication of all the semiconductors used, such as diodes and the whole switch family - e.g. MOSFETs, IGBTs, BJTs, JFETs. Several properties are indicators of the behaviour of a material, and amongst those are:

- Band-gap: It is the energy required for a valence electron to be freed into the conduction band. It is quantified in electrons-volt (eV). A wider band-gap enables the fabrication of higher voltage, speed and temperature rated devices.
- Electron Mobility: Characterizes the ease of movement of an electron when subjected to an electric field. It is proportional to conductivity.
- Electron Saturation velocity: It is the saturation of the drift velocity of the electrons.
- Thermal Conductivity: It is the heat transfer rate of the material.

2.7.1 Silicon

Silicon has been the lead material for silicon devices since its replacement over germanium devices (in the late 1960s). There are effective processes for the purification of silicon (necessary to its use as a semiconductor), it is suited for both n-type and p-type junction doping and because of its long life as a semiconductor material, manufacture processes are well studied and developed. Furthermore, silicon is the second most abundant element in the planet (behind oxygen).

2.7.2 Silicon Carbide

Silicon Carbide has been in the electronic market since the 1900s, and was used to produce the frst Ligh-Emitting-Diode (LED). It is a wide band-gap material, with higher electron mobility and thermal conductivity than Silicon, making it a faster and better suited for high power switching devices.

2.7.3 Gallium Nitride

Gallium Nitride has electron mobility even higher than Silicon Carbide but poorer thermal conductivity, making it a better choice for high-speed, low-power applications.

2.7.4 Comparison

Below is a comparison of the materials from the Digikey Whitepaper [16]

Materials Property	Si	SiC-4H	GaN
Band Gap (eV)	1.1	3.2	3.4
Critical Field 10^6 V/cm	0.3	3	3.5
Electron Mobility (cm^2/V-sec)	1450	900	2000
Electron Saturation Velocity (10^6 cm/sec)	10	22	25
Thermal Conductivity (Watts/cm^2 K)	1.5	5	1.3

Table 2.6: Semiconducting Materials

GaN has higher electron mobility (leading to faster switching frequencies) while SiC has higher Thermal Conductivity, making it more suitable for higher power operation.

As such, for the application of concern, SiC MOSFETs are the devices able to switch the high-power involved at high-frequencies.

2.8 Gate Drivers

Semiconductor driving is a vast and complex area. Moreover, the topologies vary with the semiconductor family to drive. Believing SiC MOSFETs are key to the solution, the author has decided to focus only on MOSFET driving, thus reducing wasted effort and distraction studying drivers for all semiconductor families.

It will be assumed that an Integrated Circuit (IC) will provide the basic driving (i. e. shaping the microcontroller waveform to a voltage range appropriate to the MOSFET driving). This way, the IC driver will be a black-box with microcontroller input, voltage supply and output.

The solutions presented below were based on [17] and will cover enhancements to the basic IC drive.

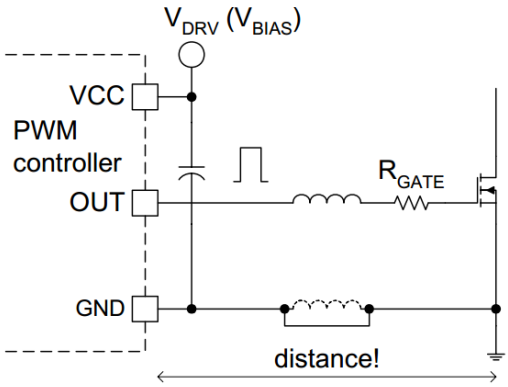


Figure 2.13: Basic driver

The basic driver can operate with minor additions of an external resistor (to reduce internal dissipation of the MOSFET) and a bypass capacitor for the driver supply. This configuration forces the driving current to flow from and into the driver (which is limited and fairly low - about 1A). Besides, the ground return path is long and the parasitic inductance caused by it produces ringing in the switching waveforms.

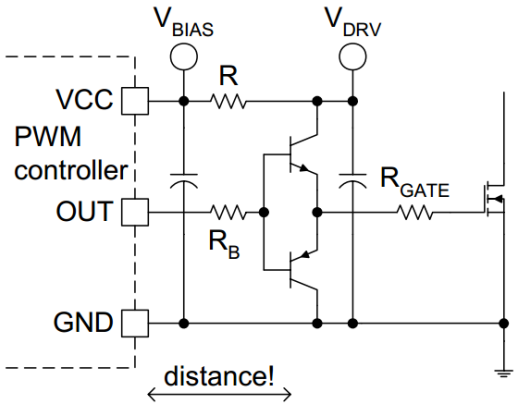


Figure 2.14: Bipolar Totem Driver

The Bipolar Totem Driver is among the most popular and cost effective solutions. The driving current now flows through the transistors directly into the gate, and the current loop is much shorter.

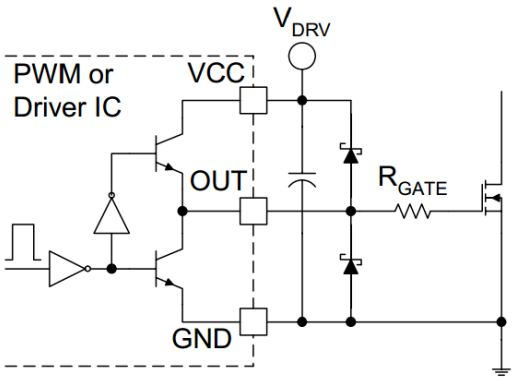


Figure 2.15: Internal Totem Protection

When the IC driver has an internal Totem, the transistors are generally both npn. Because the current flows only in one direction, ringing is prone to happen. Low-voltage Schottky diodes must be placed to provide a current path in the opposite direction.

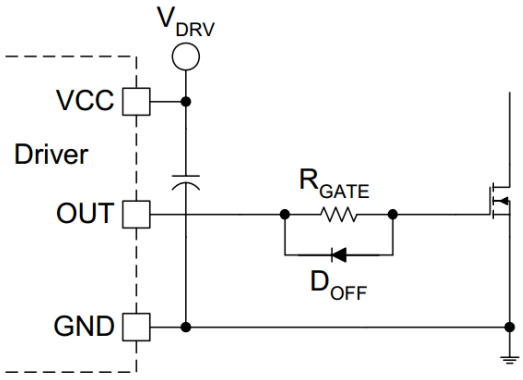


Figure 2.16: Basic speed enhancement

The turn-on of the MOSFET is faster than the turn-off, so generally the efforts to increase speed are focused on the turn-off. The simplest approach is to use a diode to bypass the external gate resistance on turn-off. The help provided by the diode fades away as the current starts falling and the foltage on the resistor approaches the diode's. Although this implementation reduces the turn-off delay, the current still has to flow through the driver.

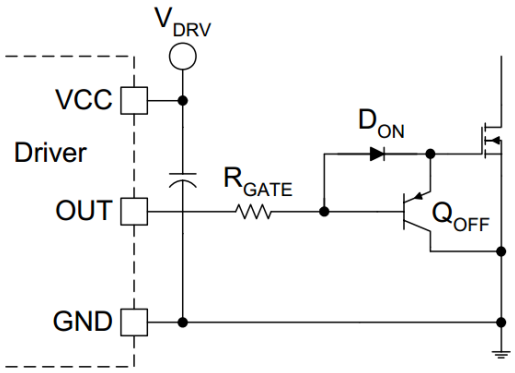


Figure 2.17: Local pnp turn-off

The pnp bipolar transistor is equivalent to the low-side of the Totem topology. The diode protects the transistor from voltage breakdown. The main disadvantage is the incapacity to pull the gate driver all the way to Ground, because of the base-emitter voltage drop. This solution is very common in speed enhancement efforts.

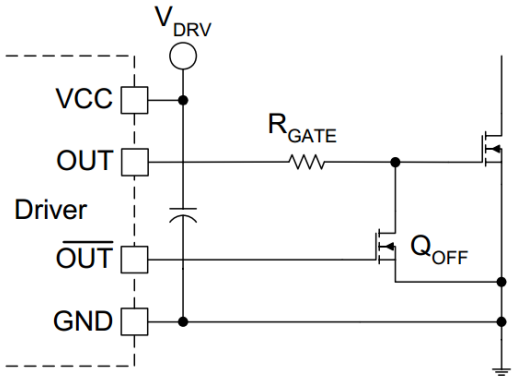


Figure 2.18: Local N MOSFET turn-off

The MOSFET equivalent needs a complementary output from the IC driver (because P MOSFETs are not a viable alternative). The added disadvantage is the drain-source voltage of the auxiliary N MOSFET adds to the gate-source voltage of the main switch, increasing the total charge the driver as to provide.

dV/dt protection will not be covered, as it it even less likely to cause problems on SiC than Si MOSFETs. ROHM claims operation with 50kV/μs without breakdown [18].

Although SiC MOSFETs can be driven from 0-18V, in order to improve the turn-off, they can be driven to -4V. One example of such drive is given by ROHM:

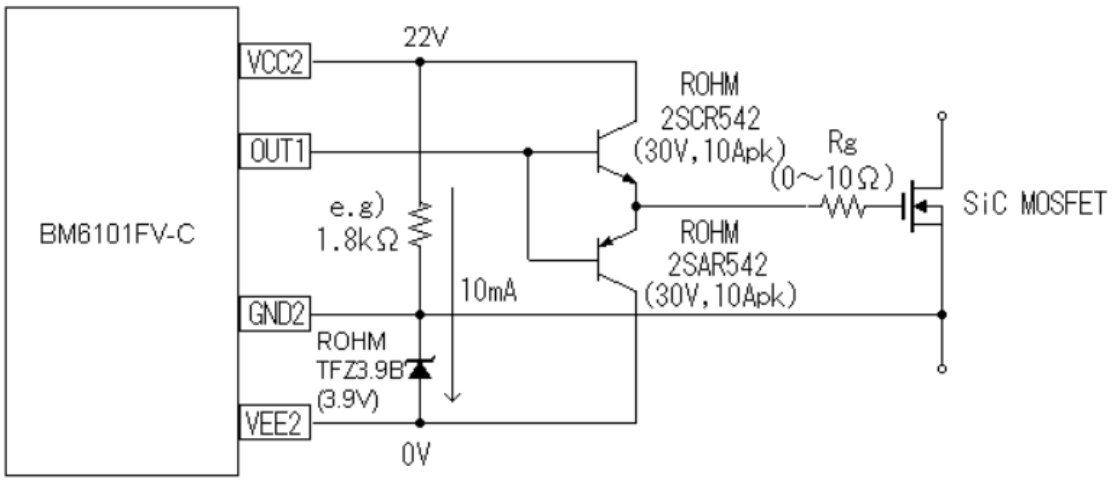


Figure 2.19: Rohm driving solution

2.9 Converter Modelling

2.9.1 The Average Model

A power converter commonly has two states: one with closed and other with open switch. The two states can be combined using a binary control variable that merges both space states into a single one. Furthermore, it is proven that letting the binary control variable become a real number between 0 and 1 (representing the duty cycle of the switch), the space state equations will still describe the converter model - this is only possible because the switch is assumed to always be either open or closed.

Below will be given an example for a Ćuk converter.

The load is assumed to be a paralleled resistor R and capacitor C_o.

When the switch is on ($u = 1$):

$$L_{in}\frac{di_{in}}{dt} = V_{in} \tag{2.35}$$

$$L_o\frac{di_o}{dt} = -(v_{cap} + v_o) \tag{2.36}$$

where v_{cap} is the voltage in the energy transfer capacitor.

$$C_{cap}\frac{dv_{cap}}{dt} = i_o \tag{2.37}$$

$$C_o\frac{dv_o}{dt} = i_o - \frac{v_o}{R} \tag{2.38}$$

When the switch is off ($u = 0$):

$$L_{in}\frac{di_{in}}{dt} = V_{in} - v_{cap} \tag{2.39}$$

$$L_o \frac{di_o}{dt} = -v_o \tag{2.40}$$

$$C_{cap} \frac{dv_{cap}}{dt} = i_{in} \tag{2.41}$$

$$C_o \frac{dv_o}{dt} = i_o - \frac{v_o}{R} \tag{2.42}$$

Combining the two partial models with the control variable u yields:

$$L_{in} \frac{di_{in}}{dt} = V_{in} - (1-u)v_{cap} \tag{2.43}$$

$$L_o \frac{di_o}{dt} = -(v_o + u\, v_{cap}) \tag{2.44}$$

$$C_{cap} \frac{dv_{cap}}{dt} = (1-u)i_{in} + u\, i_o \tag{2.45}$$

$$C_o \frac{dv_o}{dt} = i_o - \frac{v_o}{R} \tag{2.46}$$

2.9.2 Normalization

Normalization makes calculations general and more flexible. Following the previous example, the space state will be normalized by changing current, voltage and time variables as follows:

$$x_1 = \frac{1}{V_{in}} \sqrt{\frac{L_{in}}{C_{cap}}} i_{in} \tag{2.47}$$

$$x_2 = \frac{1}{V_{in}} v_{cap} \tag{2.48}$$

$$x_3 = \frac{1}{V_{in}} \sqrt{\frac{L_{in}}{C_{cap}}} i_o \tag{2.49}$$

$$x_4 = \frac{1}{V_{in}} v_o \tag{2.50}$$

$$\tau = \frac{t}{\sqrt{L_{in} C_{cap}}} \tag{2.51}$$

yielding the normalized model:

$$\dot{x_1} = -(1-u)x_2 + 1 \tag{2.52}$$

$$\dot{x_2} = (1-u)x_1 + u\, x_3 \tag{2.53}$$

$$\alpha_1 \dot{x_3} = -(u x_2 + x_4) \tag{2.54}$$

$$\alpha_2 \dot{x_4} = x_3 - \frac{x_4}{Q} \tag{2.55}$$

where $\dot{x}$ represents the derivation with respect to τ and

$$\alpha_1 = \frac{L_o}{L_{in}} \tag{2.56}$$

$$\alpha_2 = \frac{C_o}{C_{cap}} \tag{2.57}$$

and

$$Q = R\sqrt{\frac{C_{cap}}{L_{in}}} \tag{2.58}$$

2.9.3 Equilibrium Point and Static Transfer Function

When there is no variation in the voltages, currents and control, the steady-state function (or Static Transfer Function) can be obtained. By setting the left side of the last set of equations to zero and solving:

$$\bar{x_1} = \frac{1}{Q}\frac{U^2}{(1-U)^2} \qquad (I_{in}) \tag{2.59}$$

$$\bar{x_2} = \frac{1}{1-U} \qquad (V_{cap}) \tag{2.60}$$

$$\bar{x_3} = -\frac{1}{Q}\frac{U}{(1-U)} \qquad (I_{out}) \tag{2.61}$$

$$\bar{x_4} = -\frac{U}{1-U} \qquad (V_{out}) \tag{2.62}$$

2.9.4 General Model

A very interesting approach to converter system modelling is through its energy dissipation structure. In a converter there are a number of energy transfer processes as well as dissipations. The following model will contemplate all of them in a structured way:

$$A\,\dot{x} = J(u)\,x - R\,x + B\,u + \varepsilon(t); \tag{2.63}$$

In its essence it represents the conservative changes in state through $J(u)$ (skew symmetric matrix that does not take part on stability considerations), its dissipative elements through R (symmetric matrix), B represents the control input channels, and $\varepsilon(t)$ is a vector that represents external input sources.

Again, exemplifying for the Ćuk converter, and taking the normalization equations previously calculated:

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & \alpha_1 & 0 \\ 0 & 0 & 0 & \alpha_2 \end{bmatrix} \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & -(1-u) & 0 & 0 \\ 1-u & 0 & u & 0 \\ 0 & -u & 0 & -1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} - \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{Q} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

2.9.5 Representation of Single Switch Converters

The system can also be modelled as

$$\dot{x} = f(x) + g(x)u,\ y = h(x), \tag{2.64}$$

where x is the state of the system ($\Re^n$), $f(x)$ is the drift vector field ($\Re^n$), $g(x)$ is the input control field ($\Re^n$), u is either 0 or 1, and $h(x)$ is the output function ($\Re$).

Furthermore, the directional derivative of $h(x)$ in the direction of $f(x)$ is denoted as $L_f h(x)$ and in the direction of $g(x)$, $L_g h(x)$.

2.10 Control

If the converter is to manage the voltage and current in both input and output as expected, the system must have feedback. Not all system variables are appropriate for control, either because they do not help stability or because they are physically difficult to measure.

As such, it is of most importance to be able to understand the behaviour of the system and to be able to model it. For that purpose, there will be a big focus on modelling techniques for the converters rather than focusing only on control techniques.

This section is a selection of what the author thought as the most important methods present in [19]. For the sake of information density, a lot of demonstrations are left out, and can be checked by reading the cited document.

Throughout the chapter the Ćuk converter will be used as an example, because of its slightly more complex behaviour and increased system order.

2.10.1 Sliding Mode

Sliding mode is a discontinuous control naturally suited to non-linear systems such as DC-DC power supplies. The nature of the DC-DC switches (2 states: on and off) makes sliding mode

actuation even more adequate. In the following sections, some sliding mode approaches will be taken, and as before, the Ćuk converter will be used to exemplify the concepts.

2.10.1.1 Sliding Surface

A sliding surface is the set of state-vectors where the output function is satisfied. In the power converter context, the sliding surface will usually correspond to the states of the system where the output voltage or current is the one targeted by the controller, i. e, the states x where $h(x) = 0$.

2.10.1.2 Equivalent Control

When x is such that $h(x) \neq 0$, a correctly designed controller will push x in the direction of the sliding surface S. It will collide with S obliquely, and the controller action will have to change to push the straying state in the direction of S again. If we assume the response of the controller to be infinitely fast, we can define u_{eq} as the smooth equivalent control.

In equilibrium, x will be along S, and keeping it there implies:

$$\dot{h}(x) = L_f h(x) + L_g h(x)\, u_{eq} = 0, \tag{2.65}$$

thus

$$u_{eq} = -\frac{L_f h(x)}{L_g h(x)} \tag{2.66}$$

It is proven that if $h(x_0) \neq 0$ the system will converge to S in the direction of $g(x)$.

It is also proven that the control is tolerant to perturbations in the span of $g(x)$, i. e., if there perturbation is in the same direction as $g(x)$.

2.10.1.3 Direct Control

For a Ćuk converter, and taking the output capacitor voltage as the goal of the control:

$$h(x) = x_4 - V_d \tag{2.67}$$

where V_d is the desired output voltage.

For this example we have

$$L_f h(x) = \frac{1}{\alpha_2}\left(x_3 - \frac{x_4}{Q}\right) \tag{2.68}$$

$$L_g h(x) = 0 \tag{2.69}$$

The relative degree of $\frac{L_f h(x)}{L_g h(x)}$ is bigger than 1 and thus u_{eq} can not be defined.

2.10.1.4 Indirect Control

Taking S as the input current necessary to set the output voltage to V_d:

$$h(x) = x_1 - \frac{V_d^2}{Q} \tag{2.70}$$

In this case:

$$L_f h(x) = 1 - x_2 \tag{2.71}$$

$$L_g h(x) = x_2 \tag{2.72}$$

Yielding

$$u_{eq} = 1 - \frac{1}{x_2} \tag{2.73}$$

Using a Lyapunov function, the system is proven to be stable,

hence

$$u = \begin{cases} 1 \; if \; (x_1 - \bar{x}_1) < 0 \\ 0 \; if \; (x_1 - \bar{x}_1) > 0 \end{cases} \tag{2.74}$$

In practical terms, one would need to compute $\bar{x}_1$ such that V_d is the one desired, i. e., find the input current that is necessary to drive the output to the desired voltage.

2.10.2 $\Sigma - \Delta$ modulator

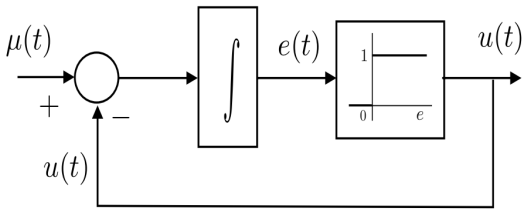


Figure 2.20: $\Sigma - \Delta$ modulator

The $\Sigma - \Delta$ modulator is able to turn a continuous control input $\mu = [0,1]$ into a discontinuous binary input $u = \{0,1\}$, which is appropriate in the DC-DC converter switch actuation. The binary output can be seen as the u_{eq} concept introduced before.

It is also possible to fix the frequency of the modulator by comparing the error integral with a triangular waveform, as shown in the figure below.

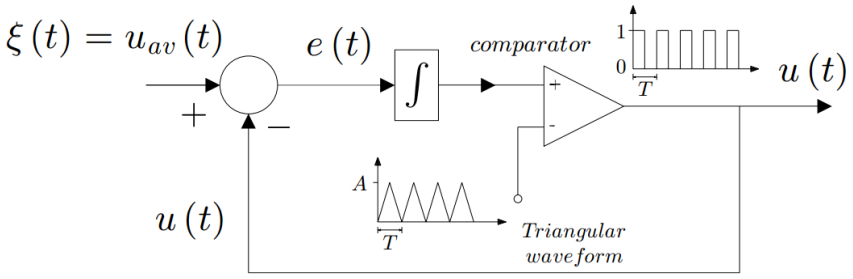


Figure 2.21: $\Sigma - \Delta$ modulator with PWM output

2.10.3 Aproximate Linearization Methods

Linear control methods have been extensively used to control DC-DC converters (albeit their non-linear nature). The basic principle behind this approach consists on linearizing the system around the equilibrium point and guaranteeing the system is always sufficiently close to the control objective to converge.

The linearized state model is of the type:

$$\dot{x}_\delta = Ax_\delta + b\, u_{av,\delta} \tag{2.75}$$

with $x_{i\delta} = x_i - \bar{x}_i$, yielding for the Ćuk model:

$$\dot{x}_{1\delta} = -\frac{1}{1-V_d}x_{2\delta} + (1-V_d)u_{av,\delta} \tag{2.76}$$

$$\dot{x}_{2\delta} = \frac{1}{1-V_d}x_{1\delta} - \frac{V_d}{1-V_d}x_{3\delta} + \frac{V_d(1-V_d)}{Q}u_{av,\delta} \tag{2.77}$$

$$\alpha_1\dot{x}_{3\delta} = \frac{V_d}{1-V_d}x_{2\delta} - x_{4\delta} - (1-V_d)u_{av,\delta} \tag{2.78}$$

$$\alpha_2\dot{x}_{4\delta} = x_{3\delta} - \frac{1}{Q}x_{4\delta} \tag{2.79}$$

2.10.3.1 Pole placement

The linearized state model is of the type:

$$\dot{x}_\delta = Ax_\delta + b\, u_{av,\delta} \tag{2.80}$$

with

$$u_{av,\delta} = -k^T x_\delta \tag{2.81}$$

yielding the closed loop system

$$\dot{x}_\delta = (A - bk^T)x_\delta \tag{2.82}$$

By placing the eigenvalues of $(A - bk^T)$ in the stable region, we assure a stable feedback system, with control:

$$u_{av} = \bar{u}_{av} - k^T x_\delta = U - k^T (x - X) \tag{2.83}$$

2.10.3.2 Observers

Because some of the variables might be more difficult to measure than others (their reference to ground, nature - voltage or current, type of measurement isolation), observers can be an effective way to estimate the variables that are not directly measured.

Taking the incremental output y_δ:

$$y_\delta = c^T x_\delta \tag{2.84}$$

The Luenberger observer estimates the incremental state x_δ as $\hat{x}_\delta$ such that:

$$\dot{\hat{x}}_\delta = A\,\hat{x}_\delta + b\,u_{av,\delta} + l(y_\delta - \hat{y}_\delta) \tag{2.85}$$

$$\hat{y}_\delta = c^T\,\hat{x}_\delta \tag{2.86}$$

The estimation error $\dot{e}_\delta = x_\delta - \hat{x}_\delta$ has dynamics:

$$\dot{e}_\delta = (A - lc^T)\,e_\delta \tag{2.87}$$

In a similar fashion to the system's pole placement, the observer poles must be placed in order to stabilize the observer. As a rule of thumb, the poles of the estimator should be ten times faster than the poles of the controlled system.

2.11 EMI suppression

A DC-DC converter has switching elements commuting power, which produce high frequency noise that can affect nearby circuitry (inside the converter or in the proximities). Furthermore, the converter can also inject noise on its inputs and outputs. The first are mostly caused by unwanted coupling of paths (through induction). The latter are consequence of the supply and demand of power and bad ground planning.

2.11.0.3 Differential Noise Supression

Differential noise is an unwanted variation between two lines (usually source and return of both input and output). The effect can be mitigated by adding bypass capacitors close to the noise source. If necessary, an L-C filter may be used.

2.11.0.4 Common-mode Noise Supression

Common mode noise is an unwanted flow of current in both lines. It can be reduced by adding a capacitor in each line and connecting it to ground.

2.12 Frequency considerations

2.12.1 High-frequency

The need for smaller and cheaper passive components results on a need to increase frequency. However, raising frequency increases losses, a factor that needs to be taken into account in order to achieve a balance in the design.

The main loss mechanisms will be described below, together with the solutions to minimize said losses.

2.12.1.1 Skin Effect

As explained before, the AC current in a wire creates opposing currents, forcing the current to flow in the borders of the conductors.

Below it can be seen the distribution of current on a 2.5mm wire as well as the ratio between wire radius r_0 and the thickness of the conduction area δ:

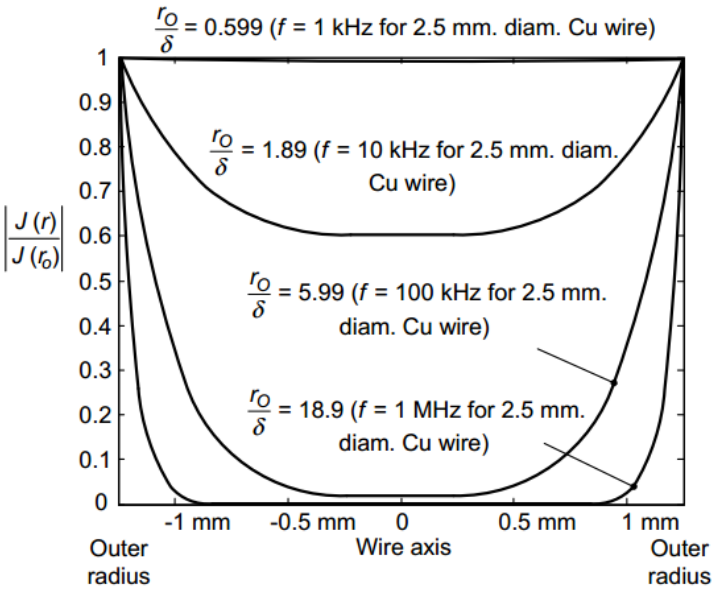


Figure 2.22: Current distribution at different frequencies

2.12.1.2 Proximity Effect

Proximity effect is a consequence of different H fields between layers of conductors. Wounding up a coil in a transformer, for instance, leads to multiple layers of conductor on the core. Between

layers, the NI product is different, as the contour is composed of different number of turns. In, fact, for a constant number of turns per layer, and for layer n:

$$H(r_{n_i}) = (n-1)H_0 \tag{2.88}$$

Showing the H field rising in equal steps.

With the frequency rising such that the skin depth becomes smaller than the conductor thickness, the current will be pushed to the lateral side of the conductor - contrasts with the skin effect, that pushes the current radially away from the conductor center.

For an arbitrary waveform,

$$\frac{R_{eff}}{R_{dc}} = \frac{I_{dc}^2 + \sum_{n=1}^{\infty} k_{p_n} I_n^2}{I_{rms}^2} \tag{2.89}$$

Where

$$k_{p_n} = \Delta_n \left(\frac{sinh(2\Delta_n) + sin(2\Delta_n)}{cosh(2\Delta_n) - cos(2\Delta_n)} + \frac{2(p^2-1)}{3} \frac{sinh(\Delta_n) - sin(\Delta_n)}{cosh(\Delta_n) + cos(\Delta_n)} \right) \tag{2.90}$$

and for the n-th harmonic:

$$\Delta_n = \frac{d}{\delta_n} = \sqrt{n}\frac{d}{\delta_0} \tag{2.91}$$

Where d is the conductor thickness and δ_0 is the skin thickness

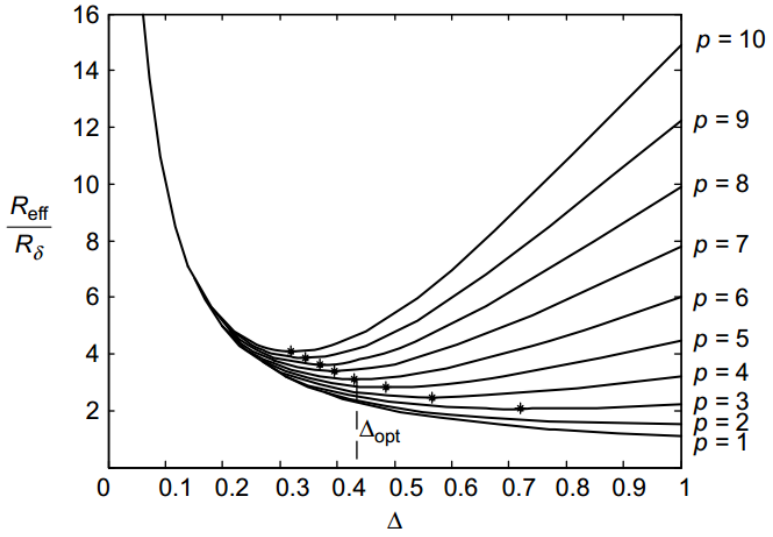


Figure 2.23: Optimum Δ

Showing there is an optimal frequency to minimize the AC resistance.

2.12.1.3 Leakage Inductance

Neglecting fringing effects and magnetic energy stored in the windings:

$$L_{l1} + L_{l2} = \frac{\mu_0 N^2 \ MLT \ b}{3w} I^2 \tag{2.92}$$

Where MLT is the mean length of a turn, b is the distance between inner and outer radii of the windings ($MLT \times b$ = volume of the windings) and w is the length of the winding window.

Consequently, the windings should be spaced in a long and narrow window.

There is a dramatic decrease in leakage inductance for high frequencies at $\Delta > 1$:

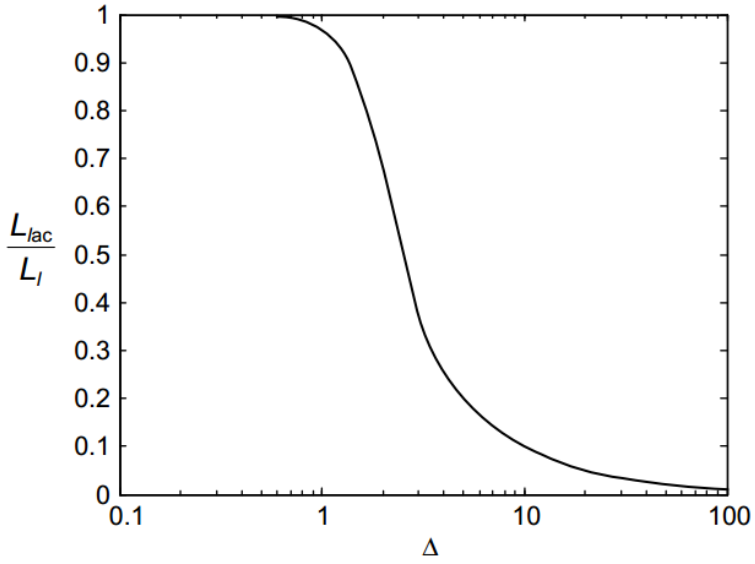


Figure 2.24: Leakage inductance at high frequencies

2.12.2 Spectrum analysis

In an operating DC-DC converter, there are multiple significant frequencies at play (desired and undesired) that must be considered when designing the system.

It is impossible to know beforehand the exact frequencies that will be present. However a rough estimation can be made with regard to the different parts of the system:

- **DC (0 Hz)** - the continuous component at both input and output.
- **10kHz - 100 kHz** - Automotive microcontroller computation time and actuation.
- **100kHz - 1MHz** - the period of the commutation of the switches.
- **up to 50 MHz** - ringing caused by the rise/fall times of the commutations.

Chapter 3

DC-DC Converter design

3.1 Introduction

A 40kW DC-DC Converter capable of stepping up 100V to 350V is a problem with distinct and diverse fronts to tackle.

This chapter will cover the theoretical conception of the DC-DC converter, broken down to its most relevant topics:

- **Topology**, regarding the macro arrangement of active and passive elements of the converter, as well as providing a base model to start from in posterior topics.
- **Passive (inductors and capacitors) and active (switches) power elements** - requirements and choices.
- **Power elements paralleling** if the power rating of the devices is inferior to the converter's.
- **Driver** - requirements and design of a driver to control the switches.
- **Instrumentation** - requirements and choice of sensors necessary to the controller and protection of the converter.
- **Protections** - failure detection and countermeasures, as well as snubbers and soft-switching.
- **GUI** - although not core of the converter, provides a straightforward way to display relevant information.
- **Control** - detailing of the topology model, as well as design of a control scheme for the plant.
- **Software structure** - outline of the code blocks to be implemented in the microcontroller.
- **Top level layout** will display the preliminary concept of the converter.
- **Post design modifications** covers the alterations made to the concept due to posterior design or test results.

3.2 Topology

There are several important factors to consider when choosing the topology for the converter.

The goal is to chose a solution that has high-density, does not overcomplicate the problem (e.g. by having more switches), it is not overly costly (by having extra components, like transformers or extra switches), it is suited for high-frequency and power operation and it is preferably symmetric (because of the need for bi-directionality).

With this in mind (and the list of topologies mentioned in the state of the art), one can immediately exclude the topologies with more than two switches. This is an elimination factor because extra switches have significant negative consequences:

- Total cost - the energy from input to output always goes through the switches. That said, an increased number of switches does not mean that less current will flow through them.
- Increased complexity - increasing the number of switches increases the complexity of the drive circuit. Furthermore, the application is medium to high-power, meaning switch paralleling is a probable solution. As we will see, paralleling devices needs special care - reducing the number of "abstract switches" reduces the number of real devices.

As such, we can eliminate the Split-Pi converter from the solution list.

Isolation by means of a transformer is not part of the specifications and it incurs in additional losses and costs. The Flyback converter can be eliminated.

Because some symmetry is important for versatility, the Zeta and SEPIC converter can be excluded in favour of the Ćuk converter.

The decision narrows down to the Buck-Boost and Ćuk converter.

Although their storage element is different and the topology seems quite different, they are not so far apart. Both have the switches oriented in such way that a half-bridge module can be used. Both have inverting outputs and the same duty-cycle gain.

However, the buck-boost has pulsating input and output, while the Ćuk has them filtered by the inductors.

The Ćuk is actually a boost-buck (unlike the buck-boost), has a snubber capacitor in parallel with the series of the switches and the topology can be manipulated to change the place of the inductors: each side's inductor can be connected to either positive or negative rail.

Furthermore, as detailed in [2], the maximum gain and efficiency of the Ćuk topology vs buck-boost (with an input filter, for components with equal parasitics) are much higher:

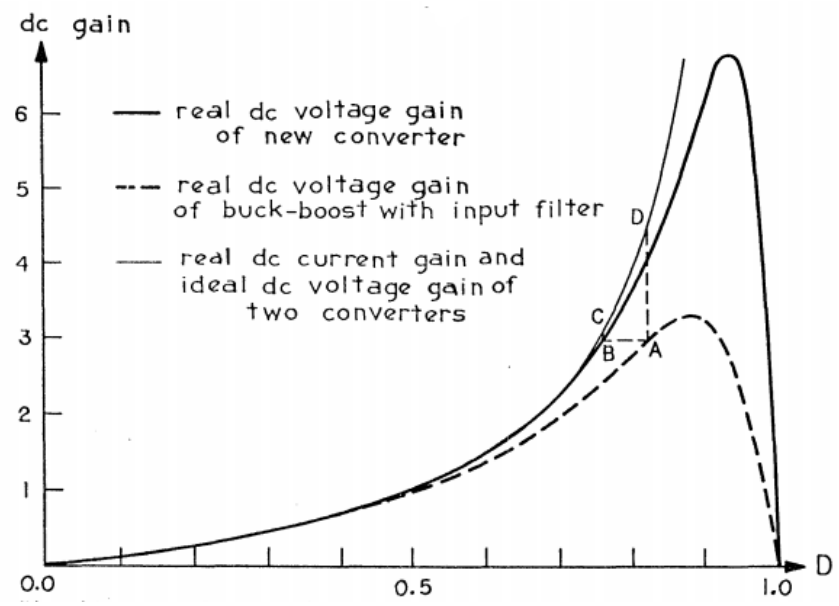


Figure 3.1: Maximum DC gain comparison - Ćuk vs Buck-Booster [2]

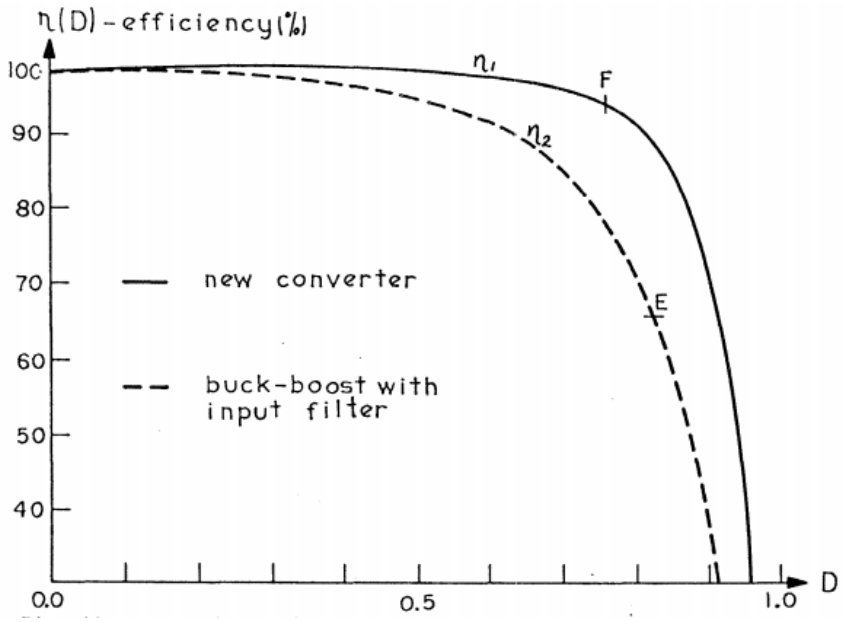


Figure 3.2: Efficiency comparison - Ćuk vs Buck-Booster [2]

For all the reasons above, the Ćuk topology has been chosen.

3.2.1 Model

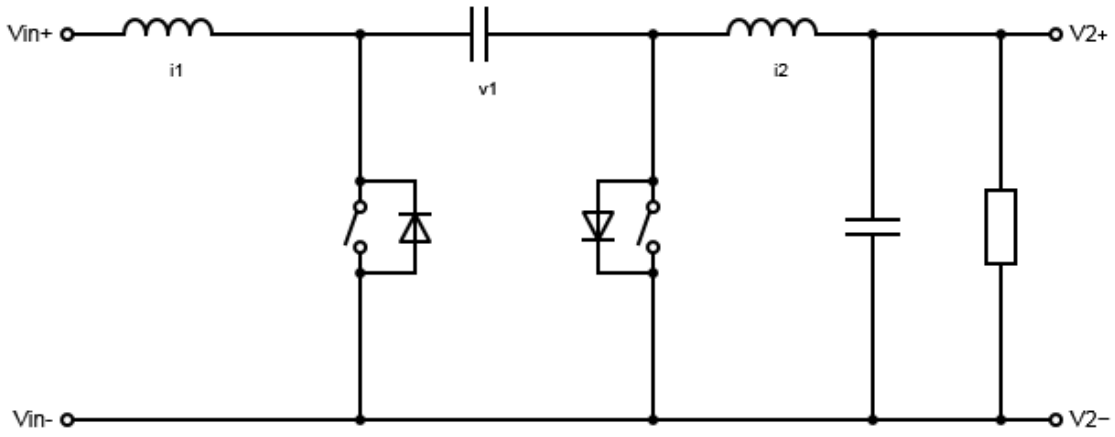


Figure 3.3: Ideal Ćuk converter

The average model of the converter, in the state-space form

$$\dot{x} = A\,x + b\,V_{in} \tag{3.1}$$

$$y = C^T\,x = v_o \tag{3.2}$$

with

$$x = \begin{bmatrix} i_1 \\ v_1 \\ i_2 \\ v_2 \end{bmatrix} \tag{3.3}$$

is

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-u)}{L_1} & 0 & 0 \\ \frac{1-u}{C_1} & 0 & \frac{u}{C_1} & 0 \\ 0 & -\frac{u}{L_2} & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{3.4}$$

The equations above represent the ideal converter for a constant input voltage and duty-cycle. To include variations in the duty-cycle and input voltage (and consequent variations of the state) as well as more realistic models for the passive elements (mainly series resistances), a more complete model has to be derived.

The following modelling techniques are from [2], where Ćuk introduces the Hybrid Model and derives it for his converter.

From the superposition principle, the AC state ($\hat{x}$) caused by input voltage variation can be analysed separately:

$$\dot{\hat{x}} = A\,\hat{x} + b\,\hat{v}_{in} \tag{3.5}$$

and

$$\hat{y} = c^T\,\hat{x} \tag{3.6}$$

yielding the AC transfer functions:

$$\frac{\hat{x}(s)}{\hat{v}_{in}(s)} = (sI - A)^{-1}b \tag{3.7}$$

$$\frac{\hat{y}(s)}{\hat{v}_{in}(s)} = c^T(sI - A)^{-1}b \tag{3.8}$$

Considering the duty-cycle variations $\hat{u}$ over the steady-state duty-cycle U, and ignoring all nonlinear terms by assuming the AC variations are much smaller than the DC value:

$$\dot{\hat{x}} = A\,\hat{x} + b\,\hat{v}_{in} + \big[(A_1 - A_2)X + (b_1 - b_2)V_{in}\big]\hat{u} \tag{3.9}$$

and

$$\hat{y} = c^T\,\hat{x} + (c_1^T - c_2^T)X\,\hat{u} \tag{3.10}$$

With A_1, b_1, c_1^T and A_2, b_2, c_2^T corresponding to the state matrices during on and off time, respectively.

Yielding transfer functions:

$$\frac{\hat{x}(s)}{\hat{u}(s)} = (sI - A)^{-1}b\big[(A_1 - A_2)X + (b_1 - b_2)V_{in}\big] \tag{3.11}$$

$$\frac{\hat{y}(s)}{\hat{u}(s)} = c^T(sI - A)^{-1}b\,\big[(A_1 - A_2)X + (b_1 - b_2)V_{in}\big] + (c_1^T - c_2^T)X \tag{3.12}$$

The main parasitic elements are the resistances in the inductors:

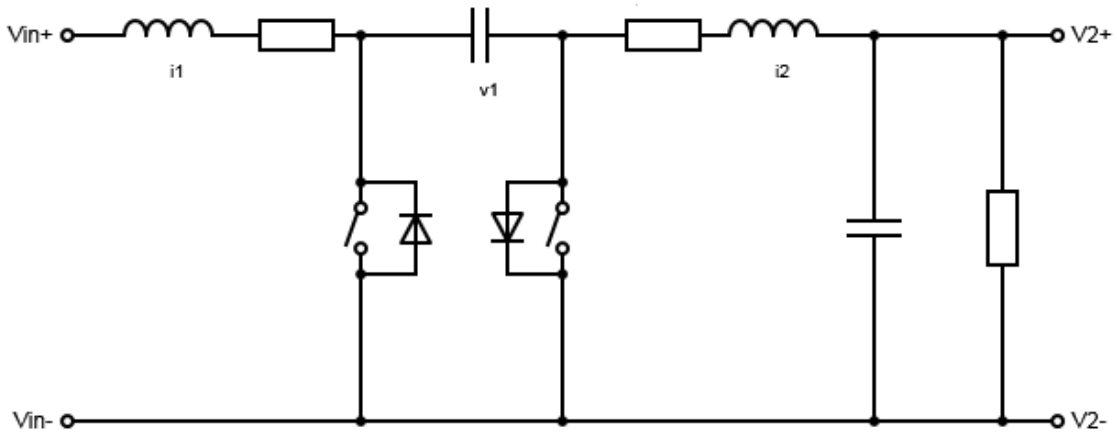


Figure 3.4: Ćuk with inductances' resistances

Then:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{(1-u)}{L_1} & 0 & 0 \\ \frac{1-u}{C_1} & 0 & \frac{u}{C_1} & 0 \\ 0 & -\frac{u}{L_2} & -\frac{R_2}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{3.13}$$

With $R_i = resistance\ of\ inductor\ i$.

It is interesting to observe how the dissipative (negative) elements occupy the diagonal of the state matrix and the energy is transferred between voltage in capacitors and current in inductors through a skew symmetric matrix, as predicted in the general model in 2.9.4.

At DC ($\dot{X} = 0$):

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} \frac{1}{R_1 + (R+R_2)(\frac{1-U}{U})^2} \\ \frac{1}{(1-U) + \frac{R_1}{R+R_2}\frac{U^2}{1-U}} \\ -\frac{1}{R_1 \frac{U}{1-U} + (R+R_2)\frac{1-U}{U}} \\ -\frac{R}{R_1 \frac{U}{1-U} + (R+R_2)\frac{1-U}{U}} \end{bmatrix} V_{in} \tag{3.14}$$

Choosing a correction factor R':

$$R' = \frac{R_1}{R}\left(\frac{U}{1-U}\right)^2 + \frac{R+R_2}{R} \tag{3.15}$$

The DC state becomes:

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} \frac{1}{R}\frac{U^2}{1-U^2} \\ \frac{1}{1-U}\frac{R+R_2}{R} \\ -\frac{1}{R}\frac{U}{1-U} \\ -\frac{U}{1-U} \end{bmatrix} \frac{V_{in}}{R'} \tag{3.16}$$

Doing a quick simulation with equal inductances $L_1 = L_2 = 1.5\mu H$ and resistances $R_1 = R_2 = 0.02\Omega$, a load resistor $R = 3.1\Omega$ and an input voltage source $V_{in} = 100V$, one can see the influence

of the small inductor resistances:

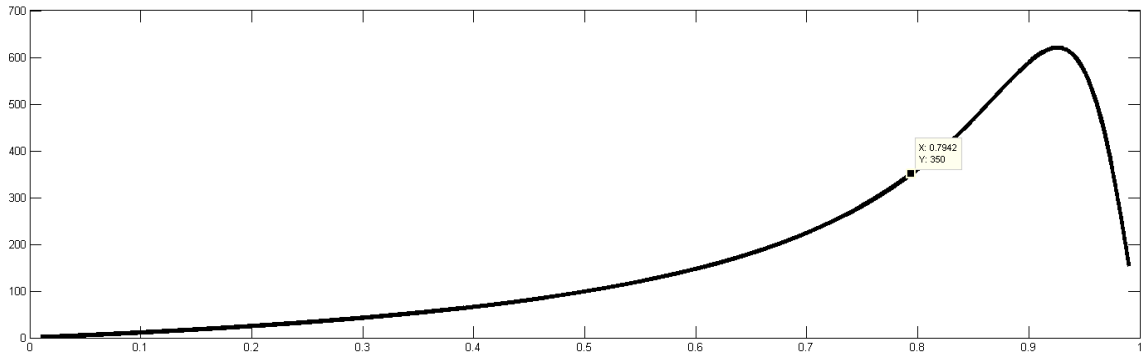


Figure 3.5: Output voltage vs. duty cycle at $(x, y) = (0.7942, 350)$

From the voltage gain plot, the actual duty cycle to achieve a 350 V output voltage is 0.7942 (instead of 0.(7)).

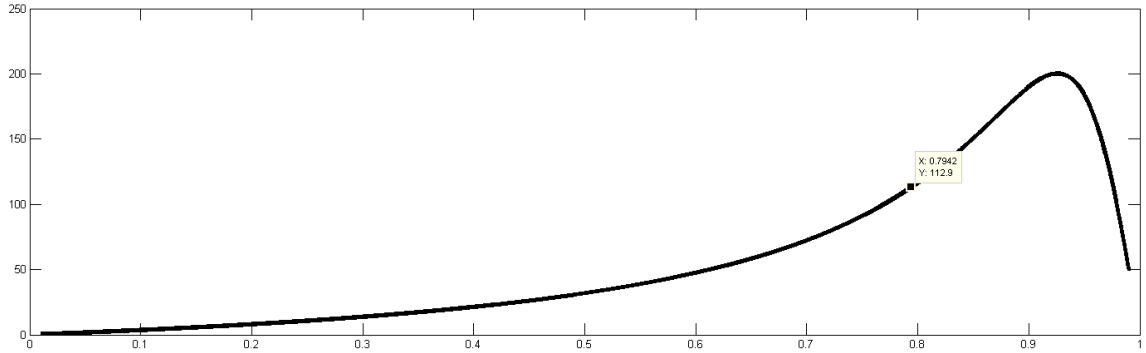


Figure 3.6: Output current vs. duty cycle at $(x, y) = (0.7942, 112.9)$

For the duty cycle observed above and same load, the current is 112.9 A.

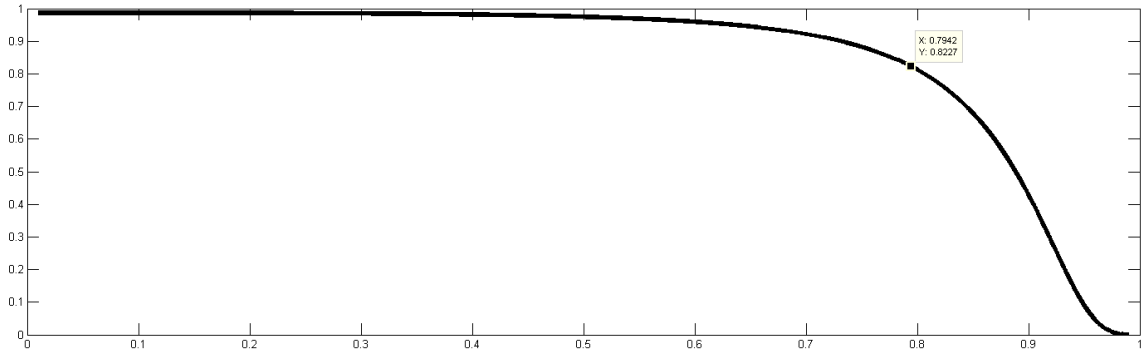


Figure 3.7: Power efficiency at $(x, y) = (0.7942, 0.8227)$

The power efficiency can be plotted as the ratio between lossy voltage and current versus lossless converter voltage and current.

For the duty cycle calculated above, the efficiency has already dropped to 82 %.

Still considering the inductor resistances as the only lossy components, it is important to determine the duty cycle that maximizes the voltage gain for the given resistances:

$$\frac{dx_4}{dU} = 0 \tag{3.17}$$

$$-V_{in}R\frac{d\frac{1}{R_1G+\frac{(R+R_2)}{G}}}{dG}\frac{dG}{dU} = 0,\ G = \frac{U}{1-U} \tag{3.18}$$

$$U_{max} = \frac{1}{\sqrt{\frac{R_1}{R+R_2}}+1} \tag{3.19}$$

The converter should be designed to avoid this point, because it has poor efficiency and because the signal of the derivative of the gain changes at that point, leading to a much more complex control.

3.3 Inductors

As has been explained in the previous chapter, inductors are a very sensitive design topic. In the converter chosen their function will be to smooth the input and output current. Oversimplifying, the goal is reaching an acceptable ripple (that increases with a reduction in inductance) with an inductor that can take the necessary current.

The ripple in current not only degrades the power signal but also puts additional stress on the switch - for the same average current, the switch will need to withstand the average current plus the ripple.

However, inductance is achieved with magnetic cores and conducting wire - translating into increases in space, cost, losses and heat.

3.3.1 Specifications

3.3.1.1 Inductance

As explained before, there is not an absolute optimum value for the inductance. With this in mind, a worst case scenario inductance will be calculated. In the implementation phase, the inductor will need to outperform the specifications given now.

Imagining the frequency can not be raised above 100kHz, with the converter operating at full load, setting a 50A peak-to-peak ripple and assuming constant capacitor voltage:

The duty-cycle D is defined by the relation between input and output voltage:

$$D = \frac{V_{out}}{V_{in}+V_{out}} = 0.(7) \tag{3.20}$$

$$\Delta I = \frac{V\ D}{L\ f} \tag{3.21}$$

with

$$V\ D = V_{in}\ D = (V_{cap} - V_{in})\ (1-D) = V_{out}\ (1-D) \tag{3.22}$$

Proving that for an equal ripple at input and output, the inductors must have the same inductance:

$$L = \frac{V_{in}\ D}{\Delta I\ f} = 15.(5)\mu H \tag{3.23}$$

If the voltage ripple on the capacitor is not negligible, i.e. $V_{cap} \neq V_{in} + V_{out}$, the shape of the current on the inductors will not be triangular (and will not have the same shape).

3.3.1.2 DC resistance

As seen in the state equations in a lossy converter, the inductors' resistance limits the gain and efficiency of the converter.

The theoretical maximum resistance on the inductors is such that the maximum duty cycle translates into the maximum voltage the converter can supply.

For simplicity, both resistances on the inductors were considered equal:

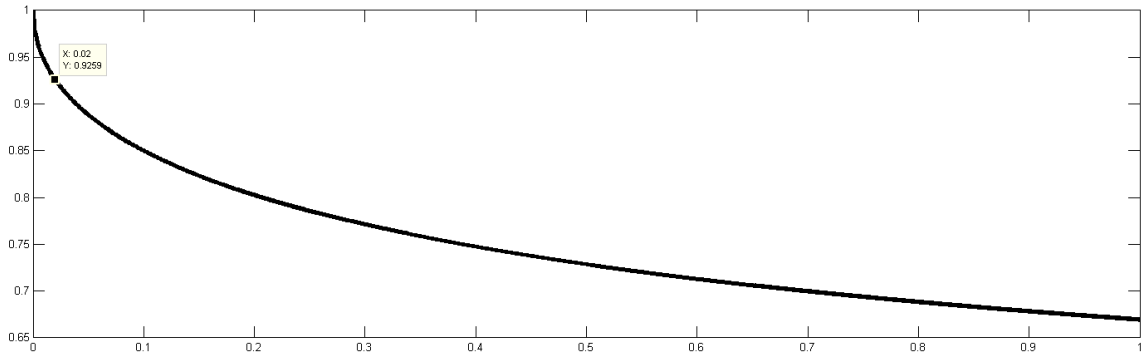


Figure 3.8: Inductor resistance (Ω) vs. maximum duty cycle at $(x, y) = (0.02, 0.9259)$

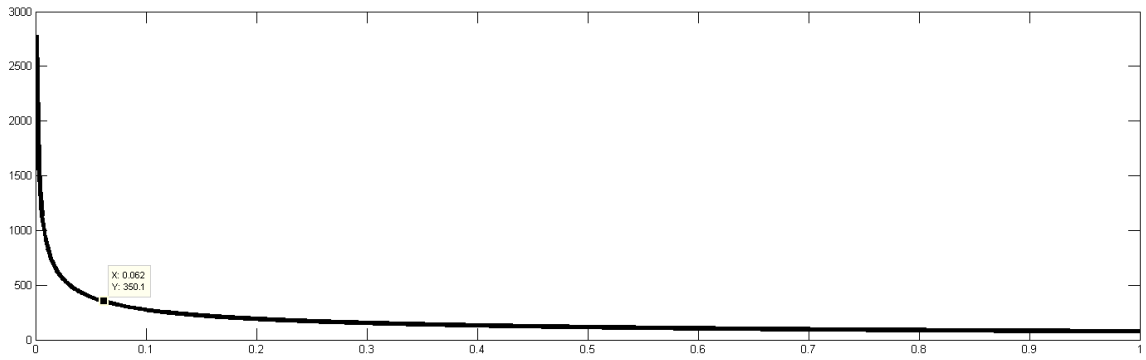


Figure 3.9: Inductor resistance (Ω) vs. maximum voltage (V) at $(x, y) = (0.062, 350.1)$

Yielding 62 $m\Omega$. However, the converter would be operating at a very unstable point: duty cycle variations (positive or negative) would result in a smaller voltage gain. Ideally, the resistance should be as small as possible to keep the voltage gain close to the ideal curve ($\frac{U}{1-U}$). At the very least it should be small enough to keep the duty cycle from reaching the maximizing duty cycle.

3.3.1.3 Self Resonant Frequency

The converter will operate at a maximum frequency of 1 MHz. Therefore, the inductor should have a self-resonant frequency much higher than this value (at least twice).

3.3.1.4 Saturation Current

For the inductor to never saturate, the current through it should never surpass the saturation current of the inductor.

The maximum current through each inductor is equal to the average current (either input current or output current of the converter, depending on the inductor) plus the current ripple.

3.3.1.5 RMS Current

The RMS Current parameter of an inductor is consequence of the maximum temperature rise the inductor can sustain.

Assuming a triangular current waveform, the maximum RMS current will be:

$$I_{RMS} = \sqrt{I_{DC}^2 + (\frac{I_{ripple}}{2\sqrt{3}})^2} \tag{3.24}$$

Where I_{ripple} is the difference between the maximum and minimum current when the maximum DC current is flowing through the inductor.

3.3.2 Choice

The custom made inductor is wound up with Litz wire, has 10.7 μH @ 150 A, 4mOhm DC resistance, with 64W and 88^{o}C temperature rise at 200kHZ and full load.

Figure 3.10: Inductor chosen

3.4 Capacitors

The energy transfer capacitor in the converter (Ćuk capacitor) is the only power capacitor of concern in the topology. The output capacitor present in the figures throughout this document is not part of the topology - it must be accounted for only because it is already present in the rail (load).

The energy transfer capacitor will be parallel to the series of input and output. It will hold the sum of the input and output voltages and will charge and discharge alternating with the input and output currents.

Ripple in the capacitor voltage is not critical itself (only if it affects some other parameter of the capacitor). Circuit-wise, it should have very low inductance and preferably low resistance. Capacitor-wise, it must withstand the DC voltage imposed and the current changes. It must operate in a rough environment and ideally should not short-circuit in case of failure.

3.4.1 Specifications

3.4.1.1 Nominal Capacitance

Contrarily to inductors' inductance, Capacitors' capacitance is technically not as challenging as inductors' inductance. Furthermore, the voltage ripple isn't very relevant, as long as it is not high enough to distort the current wave in the inductors. The voltage ripple will be:

$$\Delta V = \frac{I_{out}\, D}{C\, f} = \frac{I_{in}\, (1-D)}{C\, f} \tag{3.25}$$

For a maximum ripple of 50V:

$$C = \frac{I_{out}\, D}{\Delta V\, f} = 6.(6) uF \tag{3.26}$$

3.4.1.2 Working DC Voltage

The theoretical voltage on the capacitor will be $V_{in} + V_{out} = 450V$. Accounting for a 20% overshoot on the output and a 10% safety margin on that value:

$$V_{max} = 1.1(V_{in} + 1.2V_out) = 572V \tag{3.27}$$

3.4.1.3 RMS Voltage

It will depend on the capacitor's capacitance. Assuming the wave will be triangular with DC offset:

$$V_{RMS} = \sqrt{V_{DC}^2 + \left(\frac{V_{ripple}}{2\sqrt{3}}\right)^2} \tag{3.28}$$

3.4.1.4 RMS Current

The current on the capacitor will be alternating between the current flowing from input during off-state and current flowing from output during on-state. The current wave will be the sum of 2 square waves and a triangular wave with the current ripple (assuming equal input and output ripple):

$$I_{RMS} = \sqrt{(I_{in}\sqrt{1-D})^2 + (I_{out}\sqrt{D})^2 + \left(\frac{I_{ripple}}{2\sqrt{3}}\right)^2} \tag{3.29}$$

3.4.1.5 Working Temperature

The capacitor must withstand moderately high temperatures, considering it will be operating near other power components, such has transistors and inductors. A maximum temperature of 85°C would be ideal.

3.4.1.6 Polarization

The capacitor can be polarized, as both input and output voltage will always be non-negative.

3.4.1.7 Equivalent Series Resistance

The series resistance of the capacitor is always in series with one of the inductors' resistance, adding up. The calculation of max gain does not alter significantly when the capacitor resistance is included, as long as both inductors and capacitor's resistance is kept below the critical resistance value calculated previously.

3.4.1.8 Equivalent Series Inductance

The series inductance of the capacitor should be as small as possible. Any parasitic inductance in the capacitor will resist the variation in current during state changes, forcing the current into the transistor that is trying to close.

3.4.2 Choice

The RMS current running through the capacitor is the parameter bottleneck. The solution is to use parallel capacitors.

Using 3 parallel Kemet C4DEIPQ5680A8TK MKP capacitors, all requirements are met.

- Nominal capacitance: $3 \times 68 \mu H$
- DC Voltage: 800 V
- dV/dt: $35 V/\mu s$
- RMS Current: $3 \times 68 = 204$ @ $65^{o}C$
- Temperature: 85 ^{o}C
- Not polarized
- Equivalent Series Resistance: $0.70 mH/3$
- Equivalent Series Inductance: $25 nH/3$

3.5 Switches

The switches must be able to block current and allow it to pass with as little power dissipation as possible and able to switch at high frequencies (ideally up to 1MHz).

The only switches able to withstand high-power and high-frequencies are the SiC MOSFETs.

3.5.1 Specifications

- On current: $I_{in} + I_{out} + I_{ripple} = 600A$
- Off voltage: $V_{in} + V_{out} + V_{ripple} = 500V$
- On resistance: Similar to the capacitor.

3.5.2 Choice

The highest rated and with higher power/price ratio available is the Cree SiC MOSFET, rated for 70 A @ 80 ^{o}C.

The solution is to build a switch made up of several parallel MOSFETs.

Figure 3.11: Cree's SiC MOSFET

3.5.2.1 Paralleling

A lot of new problems arise when paralleling devices, such as current distribution at on-state and during turn on, heat management, stray inductances, and current loops. It is important to understand and design with regard to this issues.

On-state During on-state (i. e. when all MOSFETs are already turned on), the worst case scenario is when, at full load, all transistors but one have the maximum On-resistance and one has the minimum on-resistance.

The current flowing through the lowest resistance MOSFET is given by

$$I_{MOS\_R\_min} = I_{max} \frac{\frac{R_{on\_max}}{(N_{MOS}-1)}}{\frac{R_{on\_max}}{(N_{MOS}-1)} + R_{on\_min}} \tag{3.30}$$

and the number of MOSFETs:

$$N = \frac{R_{on\_max}}{R_{on\_min}} \left(\frac{I_{max}}{I_{MOS}} - 1 \right) + 1 \tag{3.31}$$

where I_{MOS} is the maximum current the MOSFET can take, I_{max} is the maximum current that can possibly flow through the switch (array of a number N_{MOS} of MOSFETs).

For an unbalanced array, the lowest resistance MOSFET will be at 25°C (25 $m\Omega$) and the others at 80 °C (30 $m\Omega$). The maximum current on the cold MOSFET is 90A, yielding:

$$N = 1.2 \left(\frac{500}{90} - 1 \right) + 1 = 6.5 \tag{3.32}$$

For a balanced array worst case, all MOSFETs are at 80°C (maximum current is 70A):

$$N = 1 \left(\frac{500}{70} - 1 \right) + 1 = 7.1 \tag{3.33}$$

And it is clear that the bottleneck is the average current in all transistors, and different temperatures will never be a problem.

The choice between 7 or 8 transistors per switch depends on the cooling system.

Transient The first MOSFET to turn-on will be the one with the lowest gate threshold voltage. For the same reason, it will also be the last to turn-off. Aggravating this problem is the fact that the threshold voltage lowers with an increase in junction temperature.

In practical terms, the most stressed MOSFET will have a tendency to increase its stress even more.

Fortunately, for the Cree MOSFET the threshold variation is relatively low - $1.8 < V_{th} < 2.4$.

The most stressed MOSFET may eventually run currents superior to its DC rating, as long as it is within a limited time and the temperature does not rise above the case limit.

The other big problem in the transient are the stray inductors: Inductance near the gate limits the current variation going in it, the inductance on the ground return path of the driver limits the drive voltage actually applied. Unbalanced inductances create different voltages and currents on the MOSFETs.

The main aspects to account for are [20]:

- Individual gate resistors - in order to avoid low resistance (and therefore underdamped) paths between different gates and sources, each transistor should have its dedicated gate resistor. Furthermore, this way it is possible to align the switching times of the parallel MOSFETs by introducing slight variations in the gates' resistances.

- Thermal Coupling - temperature rises result in an increase of the on-resistance. This will result in less current flowing through that particular MOSFET (and consequent less power dissipation). However, a rise in temperature also lowers the turn on and off threshold voltage - the higher temperature the transistor, the sooner it will switch on and later will switch off, resulting in an increase in dissipated power.

  To assert if a rise in temperature will be positively feedback (i. e. the temperature will rise even more) or negative, even in a simplified approach, some aspects need to be taken into account:

  - On current
  - Switching energy
  - Switching frequency

  As long as the On losses are bigger than switching losses, the system will be naturally stable. For 25°C, 70A, 150V, 0.8 duty-cycle operation:

  As such:

$$P_{switch} = E_{switch} f_s = 0.00045 f_s \tag{3.34}$$

$$P_{On} = R_{On} I_{On}^2 D = 98W \tag{3.35}$$

  For $P_{On} > P_{switch}$:

$$f_s < \frac{98}{0.00045} = 217.8kHz \tag{3.36}$$

  This calculations are very rough but are enough to understand that the crossing frequency will definitely be near the operating frequency. Extra switching losses when a transistor absorbs a current spike (due to unsynchronized switching) were not accounted for (which would significantly reduce the crossing switching frequency).

  Thermally coupling the switches is consequently imperative, in order to minimize this effect.

- Equalized source common inductance - the presence of inductance in the source-common path will generate a voltage opposing the flow of current when the transistor is switching. Consequently, the effective voltage seen at the gate will be smaller (delaying the switching). Equalizing this inductances is a must to reduce gate signal skew.

- Hard-switching - the steeper the voltage and current transitions, the smaller switching losses, allowing an increase of the switching frequency.

- Symmetrical Layout - Adopting a symmetrical layout will naturally help solve skew and asynchronism issues.

3.6 Driver

The driver is responsible for turning on and off the MOSFETs, supplying the correct voltages, with the right transient currents.

3.6.1 Specifications

The Cree's MOSFETs turn-on ideally at 20V (maximum 25V) and off at -5V (maximum -10V).

The driving circuit should be fast enough to switch the transistors at 1 MHz, handle current high enough to (ideally) drive the transistors without any external gate resistance. It must limit voltage ringing and overshoot on the gates.

3.6.2 Choice

The driving circuit chosen is similar to one shown in the previous chapter. The bipolar totem is made of two MOSFETs able to handle the high switching frequency and current, (represented as normal switches in the figure):

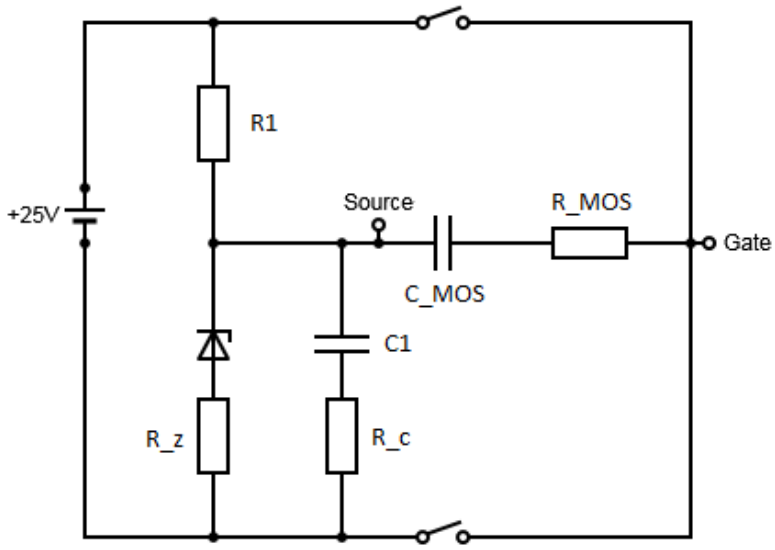


Figure 3.12: MOSFET voltage shift

To analyse the operation of the circuit, it is important to first understand its transient behaviour, without commutation of the MOSFET array (modelled by C_MOS and R_MOS):

C1 charges from 0V to 5V (zener breakdown voltage) through the resistances R1 and R_c. The rise can be considered linear without too much precision loss:

$$t = \frac{5V \times C1 \times (R1 + R\_c)}{25} \tag{3.37}$$

The resistor R1 must be designed to supply enough current for stable voltage regulation by the zener.

When C1 charges to 5V, the zener will start conducting on reverse mode and keep the voltage steady, with current:

$$I_{zener} = \frac{25-5}{R1+R\_z} \tag{3.38}$$

When the switch on the bottom closes, C_MOS will share its charge with C1 (with inverted polarity) through resistors R_c and R_MOS. C1 must be much larger than C_MOS, for the voltage drop due to C_MOS to be neglectible:

$$\frac{1}{2}C_1V_{final}^2 = \frac{1}{2}C_1V_{init}^2 - \frac{1}{2}C_{MOS}(V_{final}+V_{on})^2 \tag{3.39}$$

$$(C_1+C_{MOS})V_{final}^2 + 2C_{MOS}V_{on}V_{final} + (C_{MOS}V_{on}^2 - C_1V_{init}^2) = 0 \tag{3.40}$$

$$V_{final} = \frac{C_{MOS}}{C_1+C_{MOS}}V_{on} \pm \frac{\sqrt{C_{MOS}C_1(v_{init}^2 - V_{on}^2) + C_1^2V_{init}^2}}{C_1+C_{MOS}} \tag{3.41}$$

Where C_MOS was previously charged to V_{on}.

When the switch on the top closes, C_MOS will be paralleled with the series of negative C1 voltage and 25V. While C_MOS is charging, the current will also flow through C1 (charging it as well).

The expressions are similar to the above, leading to the same conclusion: C1 must be significantly bigger than C_MOS.

R_z limits the current in the diode when the voltage surpasses the 5 V. It must be higher than R_c to force the current through the capacitor. some care must be taken to not let the voltage rise too much above the 5 V.

The pre-driver must successfully turn on and off the auxiliary MOSFETs as fast as possible.

To drive 1 pair of MOSFETs, two independent isolated power supplies can be used to feed independent (and input isolated) gate drivers. No bootstrap issues arise, and no additional input isolation is necessary.

Furthermore, the use of this power supplies releases stress on the power supply used to generate the 25 V in the driver stage.

The solution with multiple isolated switching DC converters may have a higher cost but minimizes the number of passives and fail points.

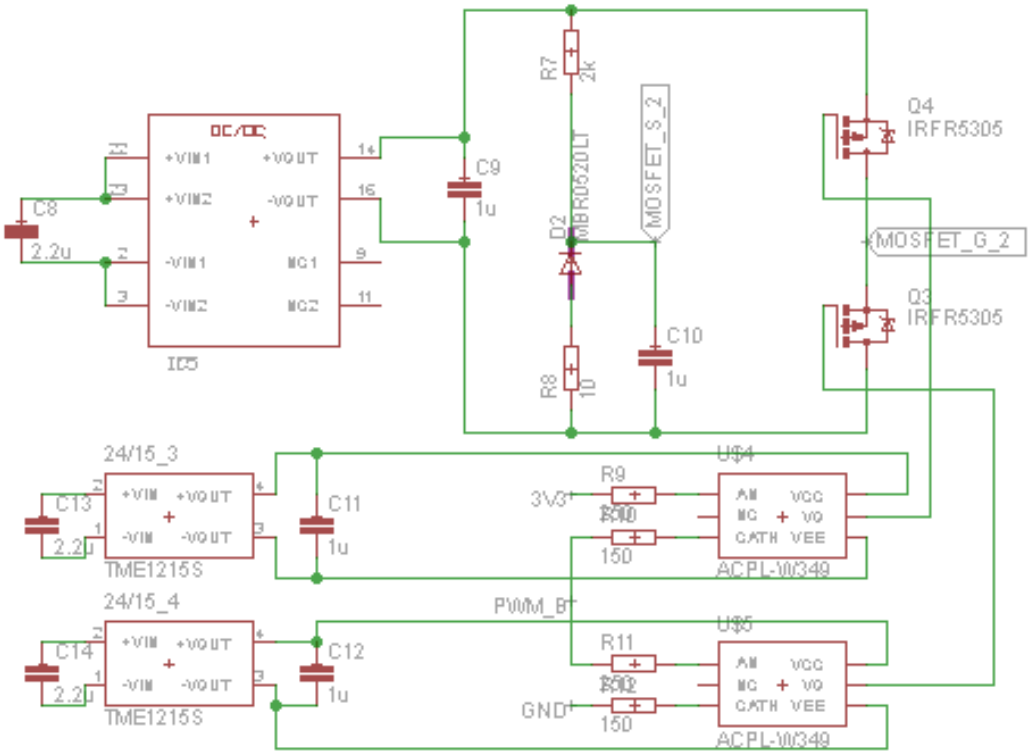


Figure 3.13: Driver schematic

3.7 Instrumentation

The sensors play a vital role in the system feedback - they are responsible for the reliable information of the plant state - mainly currents and voltages.

3.7.1 Specifications

The sensors should be able to measure the currents of both input and output inductors, as well as input and output voltage. Ideally, the sensors should be isolated and as fast and accurate as possible.

- The input current sensor must measure currents from -400 to 400 A
- The output current sensor must measure currents from -150 to 150 A
- The input voltage sensor must measure voltages from 50 to 150 V
- The output voltage sensor must measure voltages from 0 to 400 V

This are rough maximizations of the possible current and voltage values, in order to avoid the sensors going out of range.

3.7.2 Choice

3.7.2.1 Current Sensor

As seen in the control scheme, the currents do not have to be read independently, as their current shapes are parallel, with only different scaling factors. Therefore, a single sensor could measure the sum of both currents, this way reducing the number of components.

To increase reliability, two equal sensors can be placed measuring the same currents. If the sensors' readings differ more than a predefined percentage, then an error must be reported and the converter must shut-down.

Tamura's L06P600S05 is a board mount current sensor up to 600 A (less than the sum of maximum input and output current):

- Primary nominal current: $\pm 600A$
- Supply voltage: 5V
- Offset voltage: 2.5V
- Output voltage range: 1-4V

3.7.2.2 Voltage Sensor

Avagos's HCPL-7520 isolated linear current sensor can be used to measure voltages if combined with a voltage divider.

3.8 Protections

The converter must be able to respond to failure situations. Besides protection against switching voltage and current swings, it is also necessary to have a blocking circuit independent of the microcontroller that is able to inhibit the commutation when the converter starts operating under dangerous conditions, i.e., excessive input or output voltages or currents.

3.8.1 Snubber and soft-switching

Fortunately, the capacitor on the Ćuk converter is itself a snubber (as it provides an alternative flow of current when the switches open.

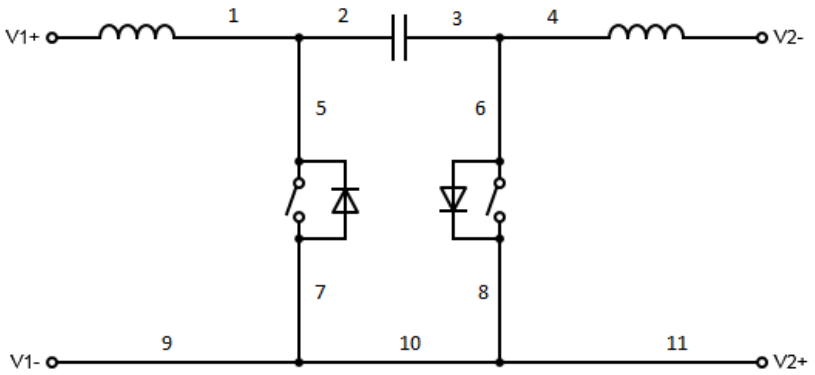


Figure 3.14: Ćuk Converter - paths prone to have stray inductances

Stray inductances on 1, 4, 9 and 11 are not critical at all: they add up to the inductance of the purposely placed inductors of the converter. The most damage they can cause is slightly altering the dynamics of the system.

Stray inductances on 2, 3, 5, 6, 7, 8 and 10 are all equally (and very) destructive. When a state change happens (change of closed switch) any energy stored in the stray inductance will form a resonant circuit with the (small) output capacitance of the opened switch. Not only the current will oscillate but also the voltage on the output capacitance will vary depending on the current going through the stray inductor when the switch closes, its inductance, and the output capacitance of the switch. From an energetic point of view, and in the moment the inductor current reaches zero (i. e. all energy has been transferred to the capacitor), the voltage on the switch capacitor is maximum:

$$V_{capacitor} = \sqrt{L/C}\, I_{inductor} \tag{3.42}$$

Where $I_{inductor}$ is the current on the inductor before the state change.

The effect above was simulated for a 10n inductor, 220pF capacitor and 500A current as shown in Figure 3.15:

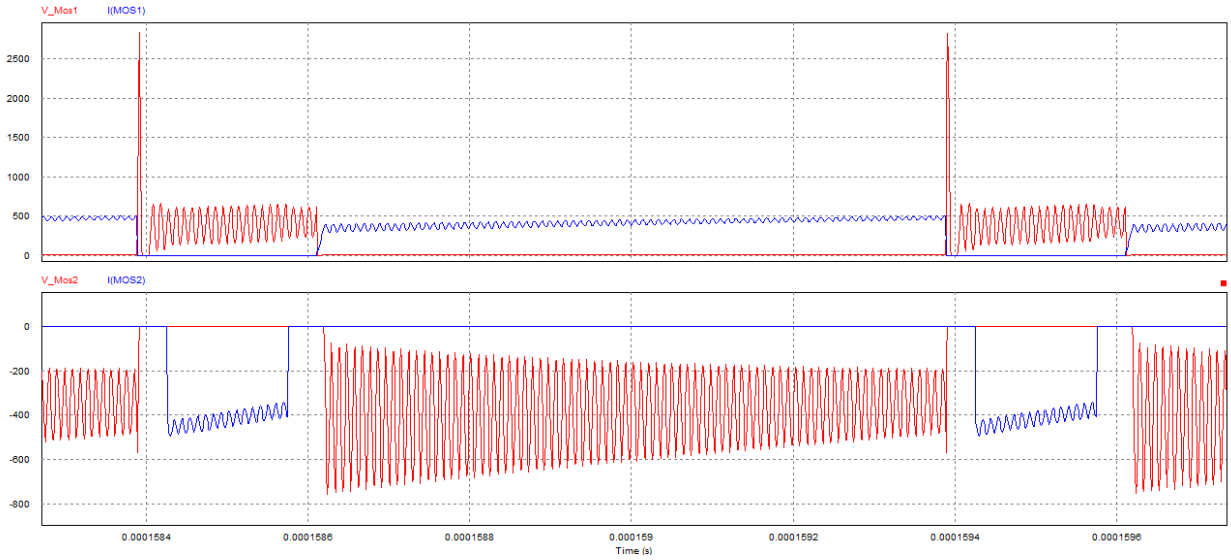


Figure 3.15: Stray inductance causing oscillations

Without digging too deep into all the negative effects, at least two are very obvious: the current and voltage ratings of the switches will need to be much higher unless some measures are taken:

The most straightforward solution is to increase the capacitance on the switch. However, it has to be increased with the square of the current. Furthermore, the energy stored in the capacitor ($\frac{1}{2}CV^2$) during the off switch time, even in ideal conditions, will short-circuit during on time, dissipating in the switch:

$$P_{diss} = \frac{1}{2}CV^2 f \tag{3.43}$$

where V is approximately equal to the sum of input and output voltage.

If the parallel capacitor proves to be insufficient, the RCD circuit described in the state of the art can be implemented:

The capacitor charges through the (ideally) lossless diode and discharges through the resistor and the switch (in series). The resistor must be small enough so the voltage at the transition to off state ($V = R\,I$) does not surpass the device ratings and at the same time big enough to limit the current at the on transition of the switch ($I = \frac{V}{R}$).

Although this solution releases stress on the switch, it does not increase efficiency (it actually slightly reduces it).

3.8.2 Detection

A single error signal is generated by an OR of three optically isolated sensors. The error signal not only disables the microcontroller PWMs but also serves as an input signal to the microcontroller.

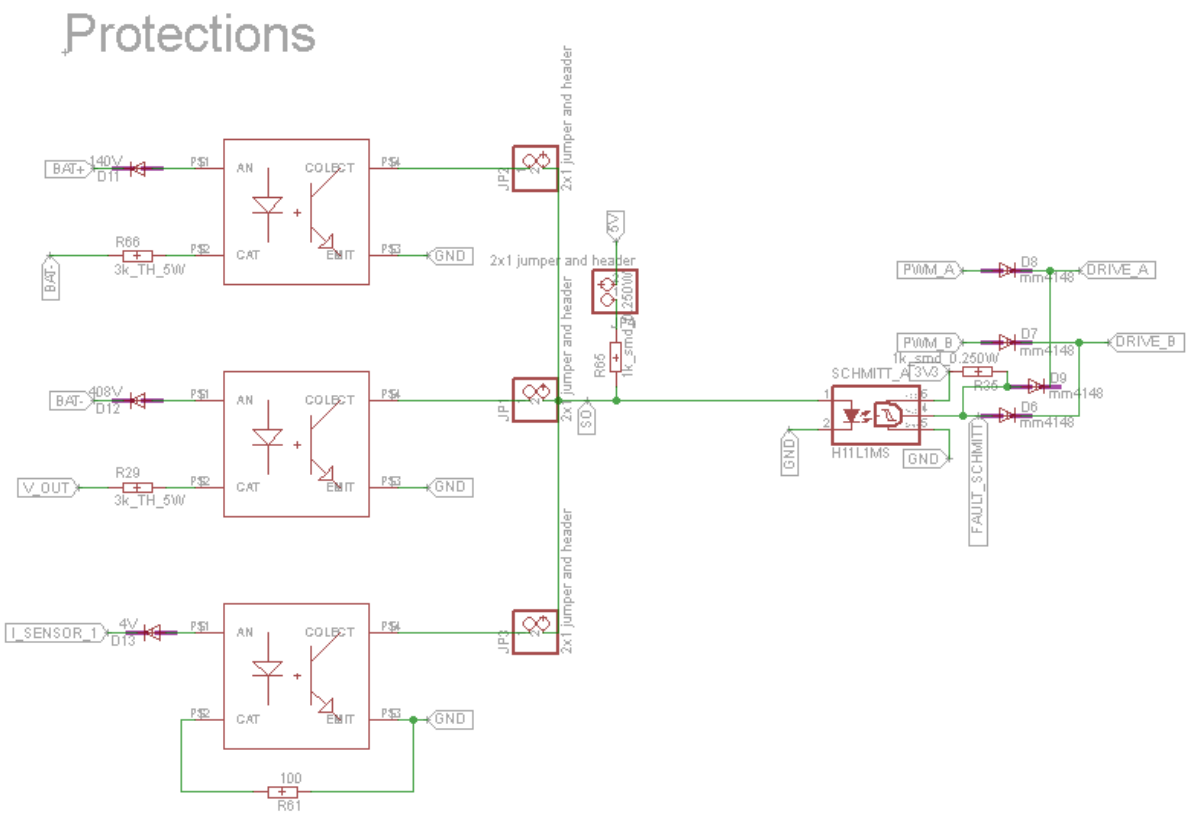


Figure 3.16: Protections concept

In a system with this level of complexity, power and price, it is of utmost importance to protect user, converter parts and even all systems connected to the converter (mainly battery pack and inverter).

The system should ideally react to a failure without need of interference from the microcontroller. Relays are naturally suited for the task for their well defined normally open or closed states.

3.8.3 Over-voltage

The converter must be able to detect a threshold where the input or output voltage becomes unacceptable.

If the input voltage suddenly rises too much (well above the full charge state), it is probably because the battery is fully charged and has stopped receiving energy.

If the output voltage rises too much, the converter has either a control malfunction or it is not able to absorb the energy at a superior rate than the output capacitor is being charged.

Both situations require the converter to shut-down to minimize damage.

3.8.4 Over-current

Excessive current flowing in the converter can damage converter passive components and switches, but can also damage the battery pack.

It is necessary to limit (or stop) the flow of current when it is excessive.

3.8.5 Pre-charge

Before the converter begins operation, it is necessary to pre-charge the Ćuk capacitor to match the input voltage. This will limit the oscillations between the series inductors and capacitors loop when the converter starts.

3.8.6 Discharge

In an event of a failure or when the system is switched-off, no current or voltage can flow or exist in the converter.

Consequently, the Ćuk and output capacitors, as well as both inductors must be discharged.

3.8.7 Protections concept

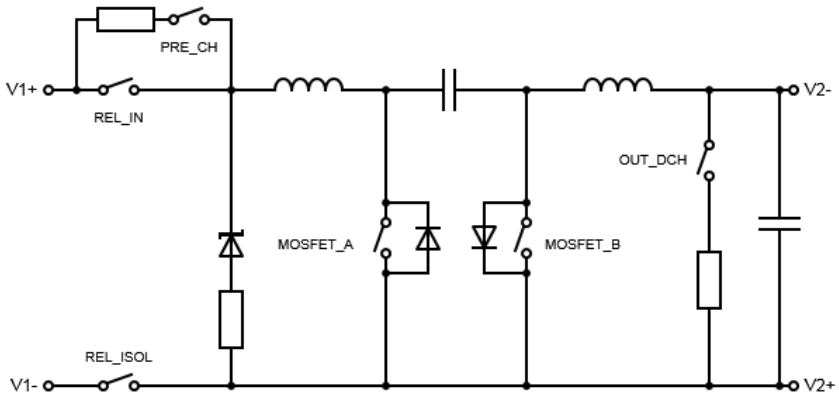


Figure 3.17: Converter protection concept

Defining the relay control vector P(PRE_CH, REL_ISOL, REL_IN, OUT_DCH, MOSFET_A), the relay states can be defined as:

OFF: P(0, 0, 0, 1, -)

ON: P(0, 1, 1, 0, -)

And the control sequences as:

Pre-charge:

- P(0, 0, 0, 1, -) - OFF
- P(0, 0, 0, 1, PWM) - Ćuk capacitor preventive discharge (MOSFET_A driven with PWM to control current flow)
- P(1, 1, 0, 1, 0) - Ćuk capacitor charges through MOSFET_B diodes until stable
- P(1, 1, 1, 1, 0) - intermediate step with REL_IN and PRE_CH overlap
- P(0, 1, 1, 0, -) - ON

Failure:

- P(0, 1, 1, 0, -) - ON
- P(0, 0, 0, 1, 0) - OFF (to discharge inductors)
- P(0, 0, 0, 1, PWM) - Ćuk capacitor preventive discharge (MOSFET_A driven with PWM to control current
- P(0, 0, 0, 1, -) - OFF

Naturally, the OFF state must be the resting state of all relays. As such, PRE_CH, REL_ISOL and REL_IN must be N.O. and OUT_DCH must be N.C.

REL_IN and REL_ISOL must be rated to handle the converter rated current, while PRE_CH and OUT_DCH will handle much smaller currents.

3.9 GUI

A display can provide basic information about the system and prove to be a valuable resource for debuggers and users.

3.9.1 Specifications

The display is not core of the converter. As such:

- It should be as non-invasive as possible
- Have low power consumption
- Consume low resources
- Refresh rate is not critical

Amongst the available protocols, and besides 1-wire, I^2C is the lowest pin consuming protocol. Given the vast availability of displays with this protocol as opposed to 1-wire, makes I^2C the obvious choice. The communication is made with two pins (Data and Clock) which only need 2 pull-up resistors.

The OLED displays are the lowest power and cost displays, available in different sizes.

3.9.2 Choice

0.96" I^2C OLED 128x64 B&W display is controlled by the SSD1306 ASIC. The device comes with all interfaces integrated in a low cost package.

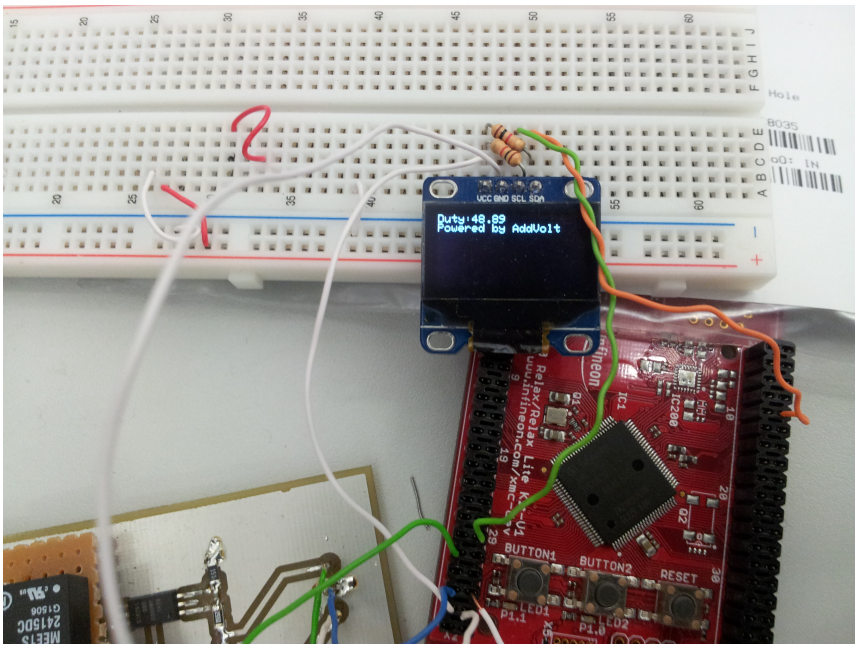


Figure 3.18: LCD chosen

3.9.3 Libraries

To control the display, several libraries had to be created and adapted:

- The I^2C library (available in the microcontroller's developing tools)
- Command and refresh operations' partitioning (to reduce latency and jitter):
  - instead of running the full initialization command array in one call, only one command is sent on each call.
  - instead of refreshing the whole display in one call, only an 8x16 bit block is updated on each call.
- Graphic library and font Sparkfun opensource library, posteriorly edited to allow the print of strings, as well as removal of redundant and unnecessary functions.

Additionally, a Matlab script was created to convert png images to the buffer byte format in the display. This makes possible the use of a background image in the display.

3.10 Control

The control of a DC-DC converter, especially one with medium/high-power is a very critical design aspect. An overshoot or deviation from operating point can mean exceeding the power rating of a component and catastrophically destroy the converter.

Luckily, the converter used in the previous chapter to demonstrate the modelling techniques happened to be the one chosen. As such, direct application of the controlling techniques can be made on the Ćuk converter model.

Besides the basic and intrinsic function of the controller (manipulating the controlled input to produce the desired stable output), it should also limit the outputs to safe levels (e. g. keep the sum of the current in the inductors from going over the nominal current of the switches). Ideally, it should even predict the parameters of the converter elements (e. g. parasitic inductance or series resistance).

3.10.1 Choice

From the ideal model:

$$x_1 = \frac{\dot{x}_2\, C_1}{1-U} - \frac{U}{1-U}(\dot{x}_4\, C_2) + \frac{1}{R}\left(\frac{U}{1-U}\right)^2 (V_{in} - \dot{x}_1\, L_1) + \frac{1}{R}\frac{U}{1-U}(\dot{x}_3\, L_2) \tag{3.44}$$

$$x_2 = \frac{V_{in} - \dot{x}_1\, L_1}{1-U} \tag{3.45}$$

$$x_3 = \dot{x}_4\, C_2 - \frac{1}{R}\left(\frac{U}{1-U}(V_{in} - \dot{x}_1\, L_1) + \dot{x}_3\, L_2\right) \tag{3.46}$$

$$x_4 = \frac{U}{1-U}(\dot{x}_1\, L_1 - V_{in}) - \dot{x}_3\, L_2 \tag{3.47}$$

Given the main goal is to regulate the output voltage and keep the currents in acceptable levels, the output voltage and current in the inductors should be measured directly (hence providing information of x_1, x_3 and x_4 and, with little computational effort, $\dot{x}_1$, $\dot{x}_3$ and $\dot{x}_4$).

If x_2 (the capacitor voltage) is not measured, the equations can be adapted as follows:

$$x_1 = \frac{-\ddot{x}_1\, C_1\, L_1}{(1-U)^2} - \frac{U}{1-U}(\dot{x}_4\, C_2) + \frac{1}{R}\left(\frac{U}{1-U}\right)^2 (V_{in} - \dot{x}_1\, L_1) + \frac{1}{R}\frac{U}{1-U}(\dot{x}_3\, L_2) \tag{3.48}$$

$$\hat{x}_2 = \frac{V_{in} - \dot{x}_1\, L_1}{1-U} \tag{3.49}$$

while x_3 and x_4 remain the same.

x_4 should be kept steady at the desired voltage (-350 V), i. e.,

$$x_4 - ref = 0 \tag{3.50}$$

Given the output voltage will be fixed, so will the steady-state duty-cycle.

However, the load (R) will not be constant. This way, a new state-space can be devised, where our goal is to control the transient duty-cycle of a controller where the load is a disturbance.

The steady-state model is:

$$\dot{X} = A\,X + b\,V_{in} + B_p\,I_L \tag{3.51}$$

where the steady-state A matrix is now:

$$A = \begin{bmatrix} 0 & -\frac{(1-U)}{L_1} & 0 & 0 \\ \frac{1-U}{C_1} & 0 & \frac{U}{C_1} & 0 \\ 0 & -\frac{U}{L_2} & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & 0 \end{bmatrix} \tag{3.52}$$

With the resistor replaced with a current perturbation:

$$B_p\,i_L = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{C_2} \end{bmatrix} i_L \tag{3.53}$$

The load variation is:

$$\dot{\hat{x}} = A\,\hat{x} + B_p\,\hat{i}_L \tag{3.54}$$

And the duty-cycle variation is:

$$\dot{\hat{x}} = (A_1 - A_2)\,X\,\hat{u} \tag{3.55}$$

yielding the superimposed model:

$$\dot{x} = A\,X + b\,V_{in} + B_p\,I_L + A\,\hat{x} + B_p\,\hat{i}_L + (A_1 - A_2)\,X\,\hat{u} \tag{3.56}$$

where

$$A_1 - A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{L_2} & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & 0 \end{bmatrix} - \begin{bmatrix} 0 & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & 0 \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L_1} & 0 & 0 \\ -\frac{1}{C_1} & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.57}$$

and

$$b_1 - b_2 = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.58}$$

yielding the DC model:

$$X = -A^{-1}\,(b\,V_{in} + B_p\,I_L) \tag{3.59}$$

and AC model:

$$\dot{\hat{x}} = A\,\hat{x} + B_p\,\hat{i}_L + (A_1 - A_2)\,X\,\hat{u} \tag{3.60}$$

with transfer function:

$$\frac{\hat{x}(s)}{\hat{u}(s)} = (sI - A)^{-1}\left[(A_1 - A_2)X\right] \tag{3.61}$$

$$\frac{\hat{x}(s)}{\hat{u}(s)} = \begin{bmatrix} s & \frac{1-U}{L_1} & 0 & 0 \\ -\frac{1-U}{C_1} & s & -\frac{U}{C_1} & 0 \\ 0 & \frac{U}{L_2} & s & \frac{1}{L_2} \\ 0 & 0 & -\frac{1}{C_2} & s \end{bmatrix}^{-1} \begin{bmatrix} 0 & \frac{1}{L_1} & 0 & 0 \\ -\frac{1}{C_1} & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{1}{R}\frac{U^2}{(1-U)^2} \\ \frac{1}{1-U} \\ -\frac{1}{R}\frac{U}{1-U} \\ -\frac{U}{1-U} \end{bmatrix} V_{in} \tag{3.62}$$

with det(sI-A) :

$$s^4 + \left(\frac{1}{L_2C_2} + \frac{U^2}{L_2C_1} + \frac{(1-U)^2}{L_1C_1}\right)s^2 + \frac{(1-U)^2}{L_1L_2C_1C_2} \tag{3.63}$$

If instead the input voltage was considered part of the system states (modelled by a big capacitor C_{in} with a series resistance R_{in}), the model would be more accurate, although the input voltage source would still be poorly modelled.

In that scenario:

$$A = \begin{bmatrix} -\frac{R_{in}}{L_1} & -\frac{(1-U)}{L_1} & 0 & 0 & \frac{1}{L_1} \\ \frac{1-U}{C_1} & 0 & \frac{U}{C_1} & 0 & 0 \\ 0 & -\frac{U}{L_2} & 0 & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 \\ -\frac{1}{C_{in}} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.64}$$

$$x = \begin{bmatrix} i_1 \\ v_1 \\ i_2 \\ v_2 \\ v_{in} \end{bmatrix} \tag{3.65}$$

b and V_{in} would not exist as control inputs and would be part of the state.

The difference between A_1 and A_2 would remain the same, only padded with zeros:

$$A_1 - A_2 = \begin{bmatrix} -\frac{R_{in}}{L_1} & 0 & 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 \\ -\frac{1}{C_{in}} & 0 & 0 & 0 & 0 \end{bmatrix} - \begin{bmatrix} -\frac{R_{in}}{L_1} & -\frac{1}{L_1} & 0 & 0 & \frac{1}{L_1} \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 \\ -\frac{1}{C_{in}} & 0 & 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ -\frac{1}{C_1} & 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.66}$$

With the DC model simplifying to:

$$X = -A^{-1} B_p I_L \tag{3.67}$$

And the operating point becoming:

$$X = \begin{bmatrix} I_L \frac{U}{1-U} \\ \frac{V_{in}}{1-U} \\ -I_L \\ -\frac{U}{1-U} V_{in} \\ V_{in} \end{bmatrix} \tag{3.68}$$

$B_u = (A_1 - A_2)X$ is the traditional control column, linearised around a fixed load current and input and output voltage operating point:

$$B_u = (A_1 - A_2)X = \begin{bmatrix} 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ -\frac{1}{C_1} & 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_L \frac{U}{1-U} \\ \frac{V_{in}}{1-U} \\ -I_L \\ -\frac{U}{1-U} V_{in} \\ V_{in} \end{bmatrix} = \begin{bmatrix} \frac{V_{in}}{L_1(1-U)} \\ -\frac{I_L U}{C_1(1-U)} \\ -\frac{V_{in}}{L_2(1-U)} \\ 0 \\ 0 \end{bmatrix} \tag{3.69}$$

with superimposed model:

$$\dot{\hat{x}} = A X + B_p I_L + A \hat{x} + B_p \hat{i}_L + B_u \hat{u} \tag{3.70}$$

However, the effort of increasing the order of the system plus the low relevance of using the input voltage as a capacitor makes it impracticable to use a fifth order model.

As such, the model takes V_{in} as an input (which is yet assumed constant), accounts for input voltage source and inductors' series resistance and a varying load.

Matrix A is very similar to the one that accounts for inductors' resistance. In fact, the input resistance is in series with the resistance of the first inductor. This way, R_1 is simply the sum of input resistance and first inductor resistance:

$$A = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{(1-u)}{L_1} & 0 & 0 \\ \frac{1-u}{C_1} & 0 & \frac{u}{C_1} & 0 \\ 0 & -\frac{u}{L_2} & -\frac{R_2}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & 0 \end{bmatrix} \tag{3.71}$$

And V_{in} as an input is again:

$$B_v\, V_{in} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{3.72}$$

with superimposed model:

$$\dot{\hat{x}} = A\, X + B_v\, V_{in} + B_p\, I_L + A\, \hat{x} + B_p\, \hat{i}_L + B_u\, \hat{u} \tag{3.73}$$

The system is linearised around the rated output voltage and full load point. However, the state matrix does not necessarily need to be static, as long as its change rate is much slower than that of the inner controllers.

This way, the pseudo-static linearisation should help set a more appropriate operation point, while the inner controllers are responsible for rejecting disturbances. This approach allows slow variations of input voltage as well as voltage set-point. A variation in the DC constant of the load current will also reflect in a slow adaptation of the control matrices that will result in a more accurate control.

This way, U can be a slowly varying function of steady-state input voltage and the voltage reference, inducing slow changes in matrix A. Together with the variation of I_L, X will be altered to reflect this changes.

$$X = \begin{bmatrix} I_L \frac{U}{1-U} \\ \frac{1}{1-U}(V_{in} - R_1 I_L \frac{U}{1-U}) \\ -I_L \\ -\frac{U}{1-U} V_{in} + R_1 I_L (\frac{U}{1-U})^2 + R_2 I_L) \end{bmatrix} \tag{3.74}$$

with B_u becoming:

$$B_u = \begin{bmatrix} \frac{1}{L_1}\frac{1}{1-U}(V_{in} - R_1 I_L \frac{U}{1-U}) \\ -\frac{I_L}{C_1}\frac{1}{1-U} \\ -\frac{1}{L_2}\frac{1}{1-U}(V_{in} - R_1 I_L \frac{U}{1-U}) \\ 0 \end{bmatrix} \tag{3.75}$$

The control of the plant consists of an inner control loop with tighter time constraints to avoid overshoots in the current, operating as a current noise rejection controller. The outer controller will reject noises in the output voltage reference.

A parallel computation will adapt the controller depending on the steady-state duty-cycle, state and load.

The inner current control loop exists to protect the transistors from excessive current. Given the current going through the transistors will be the sum of magnitudes of input and output currents, i.e. $X_1 - X_3$, the inner C matrix will be:

$$C_i = \begin{bmatrix} 1 \\ 0 \\ -1 \\ 0 \end{bmatrix}^T \tag{3.76}$$

while the outer controller will be monitoring the output voltage:

$$C_v = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}^T \tag{3.77}$$

3.10.1.1 Block Diagram

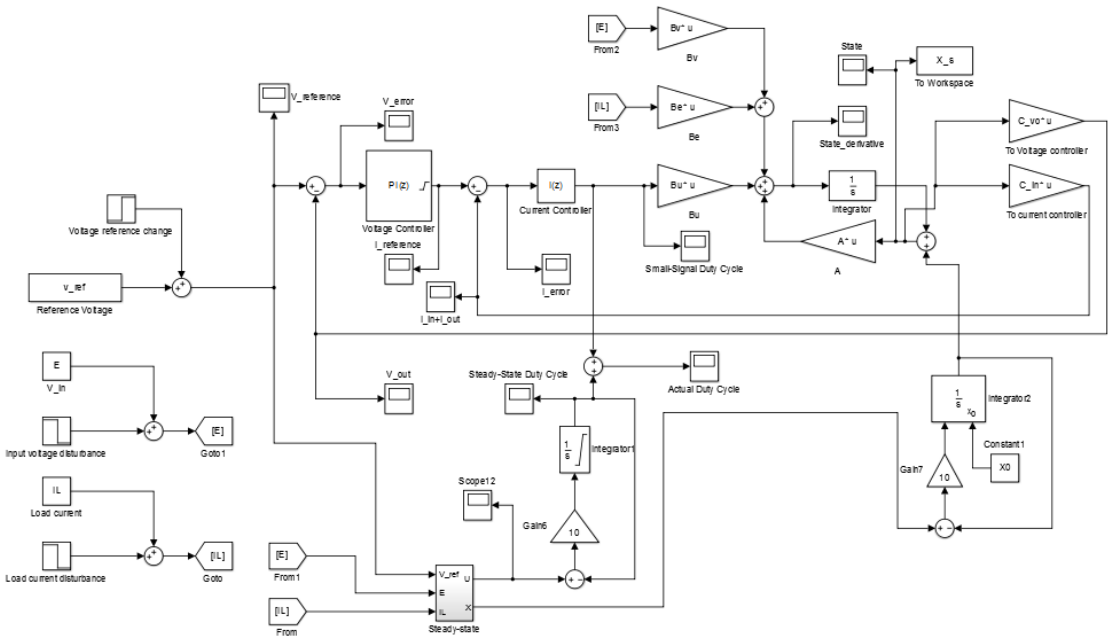


Figure 3.19: Converter model

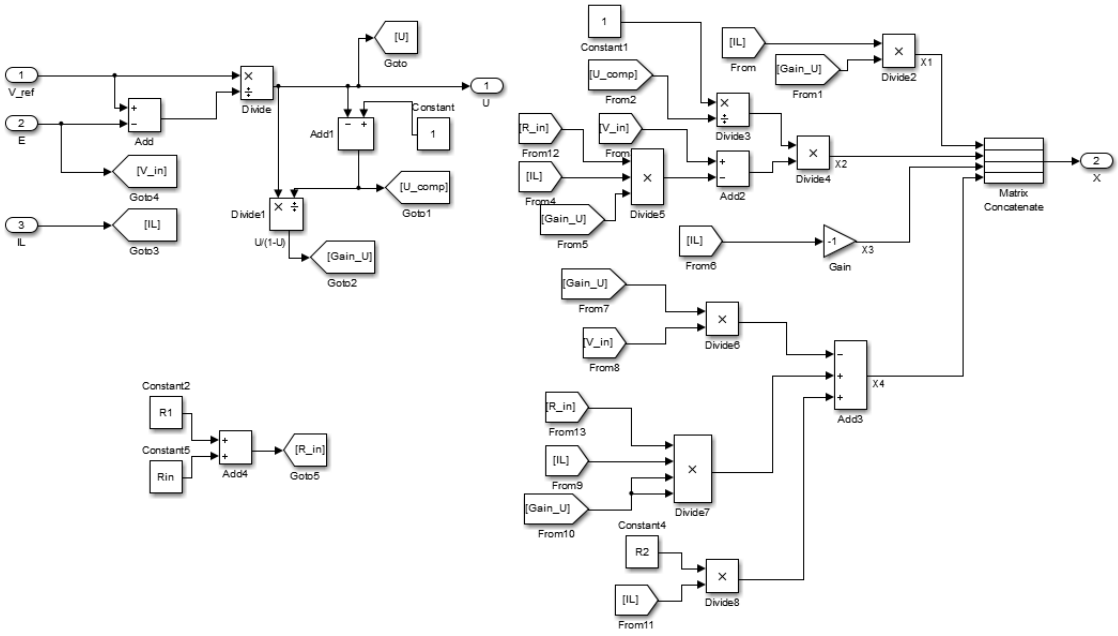


Figure 3.20: Calculation of steady state duty cycle and states

The current controller was tuned to have response time = 1 ms, the voltage controller was tuned with response time = 10 ms. The adaptive steady-state has response time 100 ms.

This way, interference between controllers and state operating point adaptation can be minimized.

3.11 Software Outline

The microcontroller will be responsible for managing and commanding all analogic and digital signals. Its main goal will be assuring the output voltage follows the reference. However, it must be able to provide much more than that:

- Power regulation:
  - Stable voltage output - good transient and steady-state response
  - Controlled current in the system - current peaks must be effectively damped to avoid exceeding components' ratings
  - Startup sequence - pre-charging of the system before start of operation
  - Emergency response - safe interruption of the functioning converter
- Failure prevention and response - Watchdog timer detecting and recovering from program halts/malfunctions
- GUI updating

Figure 3.21 shows the global code architecture designed.

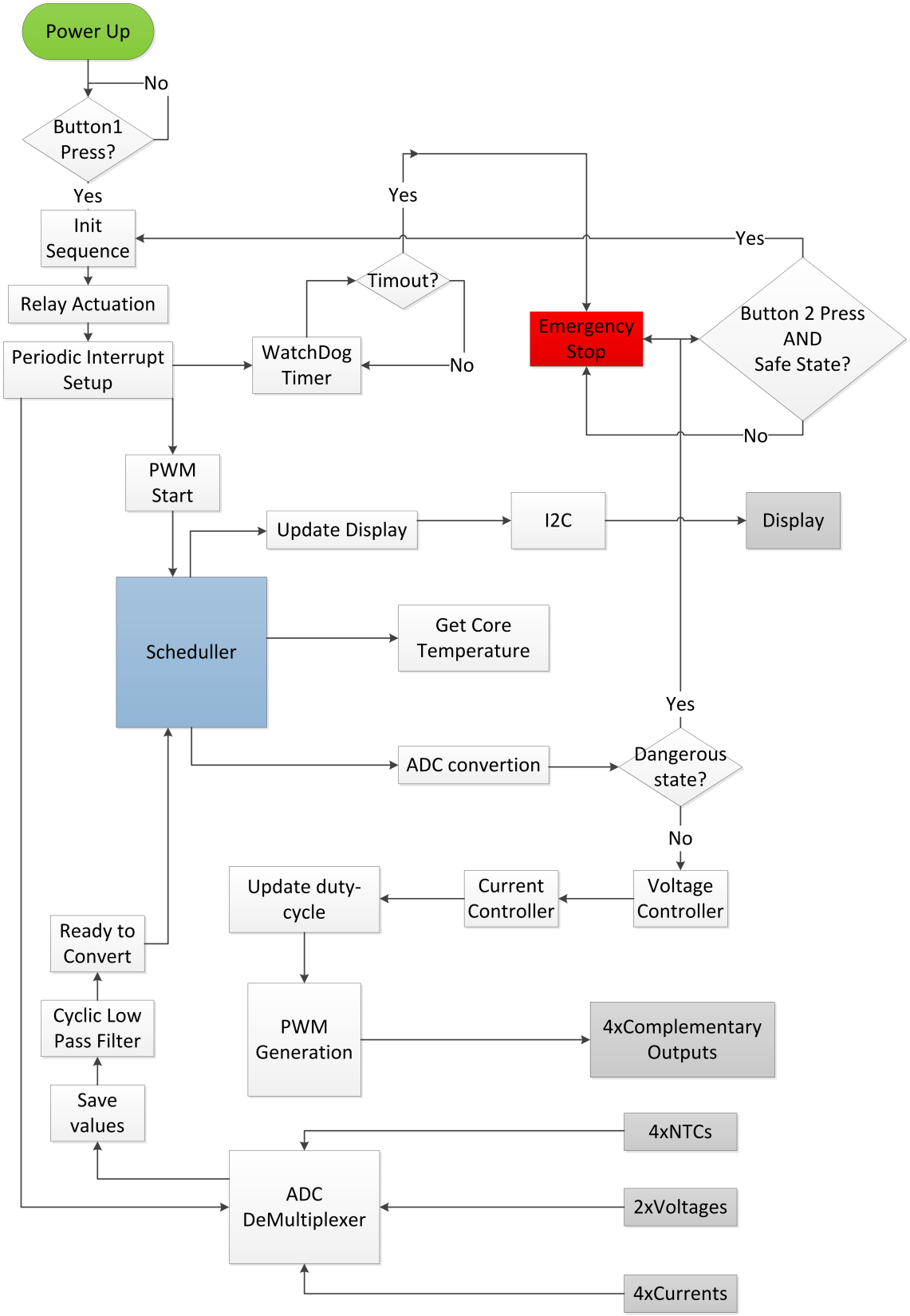


Figure 3.21: Code architecture

3.11.1 Hardware Platform Choice

Infineon's XMC4500 is an automotive grade microcontroller running an ARM Cortex-M4 processor at 120MHz. It has 1MB of FLASH, 4x4 ADCs and supports serial communication (such as I^2C).

The XMC4500 Relax Kit Lite is an evaluation board that suits all the needs necessary for this application.

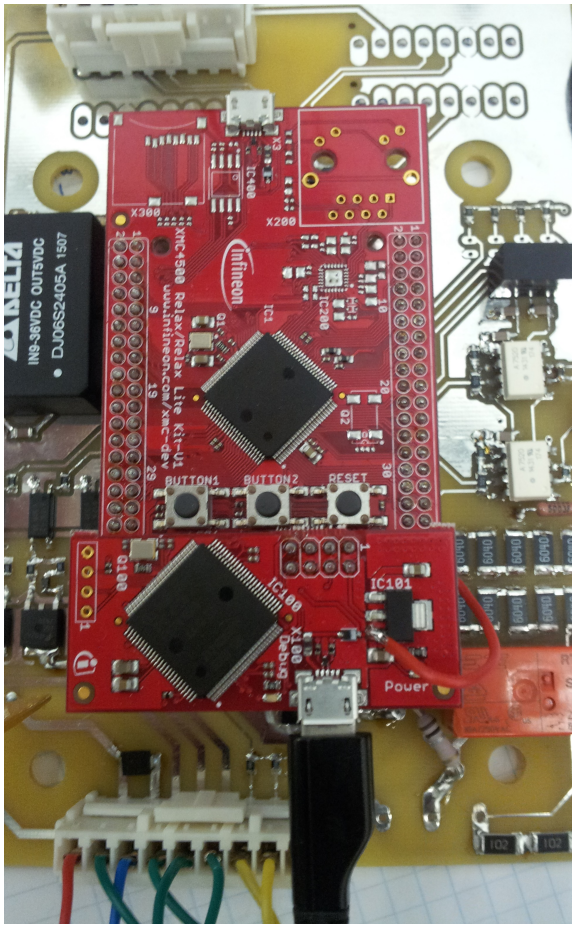


Figure 3.22: Microcontroller board mounted on driver

3.12 Top-level Layout

A good top-level layout can influence the performance of the converter greatly. Namely, the placement of the long paths must be given great thought. Only this way will the stray inductances appear only where they do not affect the performance. Distribution of heat and drive distances and symmetries are also important factors to take into consideration. The converter must also be as compact as possible while still allowing proper cooling of the power components and isolation between signal and power circuits. A concept was designed, that will serve as base for the prototype.

Taking the previous design choices into consideration, i. e.:

- Ćuk topology
- 2 power inductors with powder core and wound on Litz wire
- 3 low-inductance MKP Capacitors
- 16 SiC MOSFETs
- Designed SiC Driver board
- Current, voltage and temperature sensoring
- Failure detection and relay actuation
- Relevant information display
- Voltage and current control

The concept below was idealized:

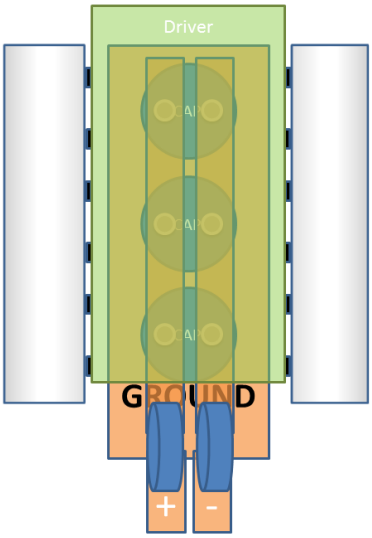


Figure 3.23: Preliminary concept

and 3D modelled in Figure 3.24.

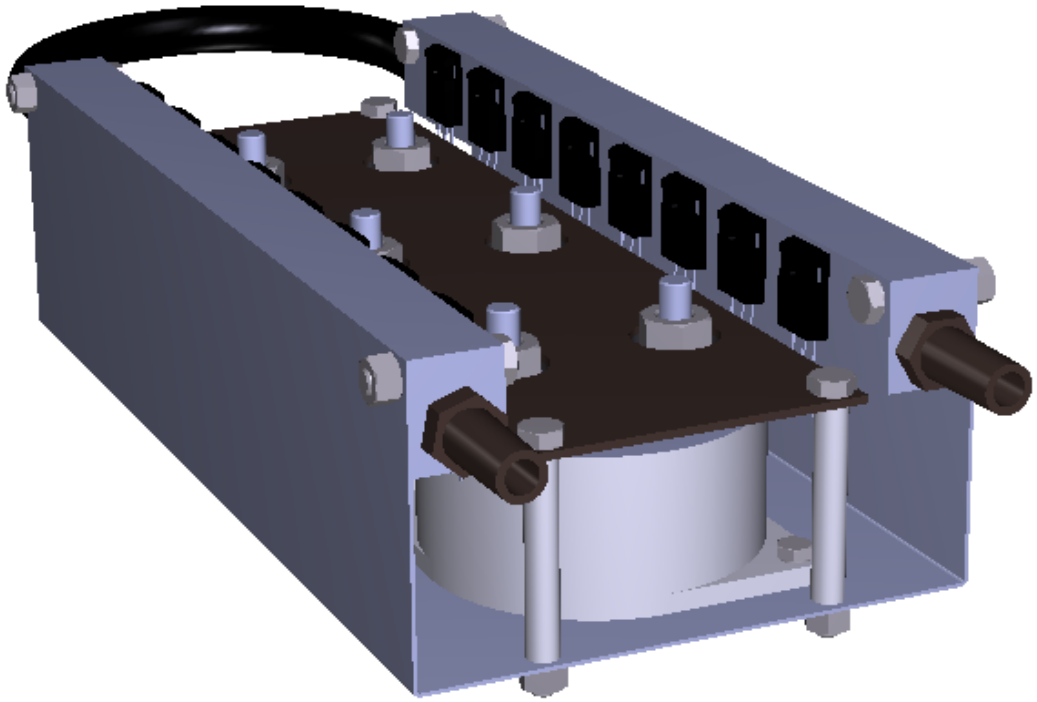


Figure 3.24: Preliminary concept 3D render

The critical inductance paths have been minimized, the inductors have space to grow if there is need to increase the performance of the converter as well. They are also near each other, slightly increasing their inductance.

The driver is right above the MOSFETs and at a reasonable distance from the terminals and inductor, allowing measurement of the currents while not suffering from serious interference from the inductors.

Chapter 4

Computational Analysis of the Behaviour of the DC-DC Converter

4.1 Introduction

This chapter will assess the performance of the models and designs of the previous chapter, through their computational analysis.

- **Topology** - Simulated first in open-loop in PSIM.
- **SiC MOSFET** - Simple simulation using the manufacturer LTSpice model to acess the switching performance of the transistor.
- **Driver** - PSIM testing of the designed driver.
- **Control** - After controller tuning in MATLAB, the closed-loop simulation was made in PSIM. Finally, a test against a PMSM motor simulation with varying torque was made.

4.2 Topology

The Ćuk was simulated in PSIM.

The ideal model with a pre-charged Ćuk capacitor (to the input voltage) and remaining elements with zero initial conditions were set. The duty-cycle was approximated to 0.78.

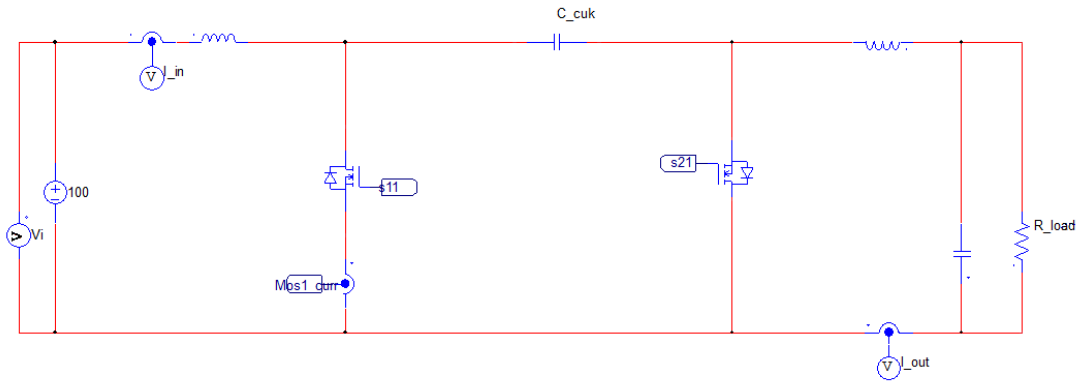


Figure 4.1: Ideal Ćuk

The step response to the 0.78 duty-cycle is shown below.

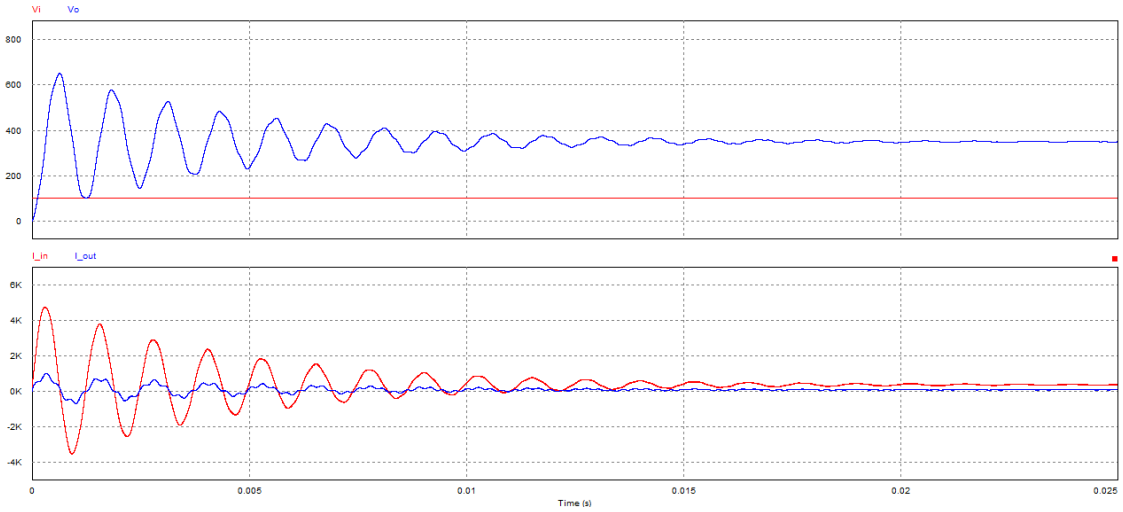


Figure 4.2: Ideal Ćuk step response

Which is clearly unacceptable. The oscillations are mainly caused by the loop formed by the series of input voltage source, both inductors, Ćuk capacitor and output capacitor, which is only damped by the load.

Adding the series resistances and inductances to the model:

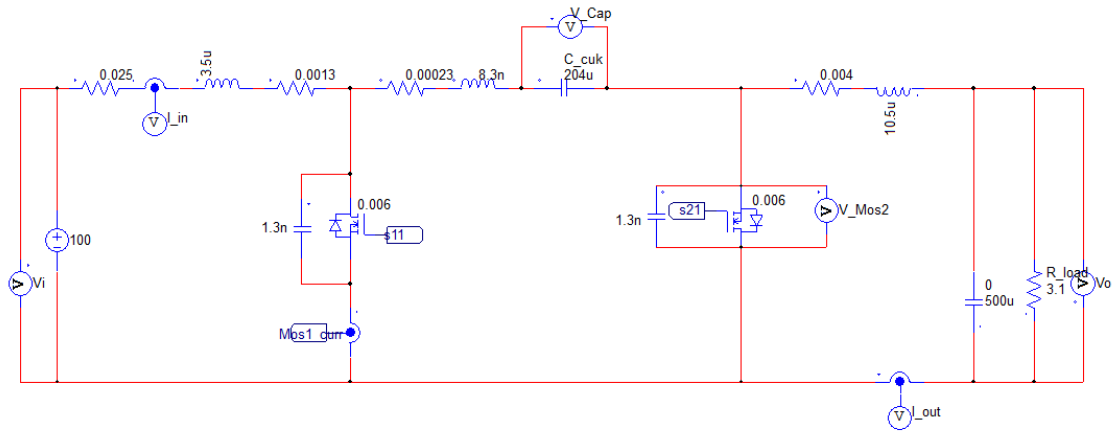


Figure 4.3: Ćuk with passive elements resistances and inductances

Where the response is much more damped, but still unacceptable:

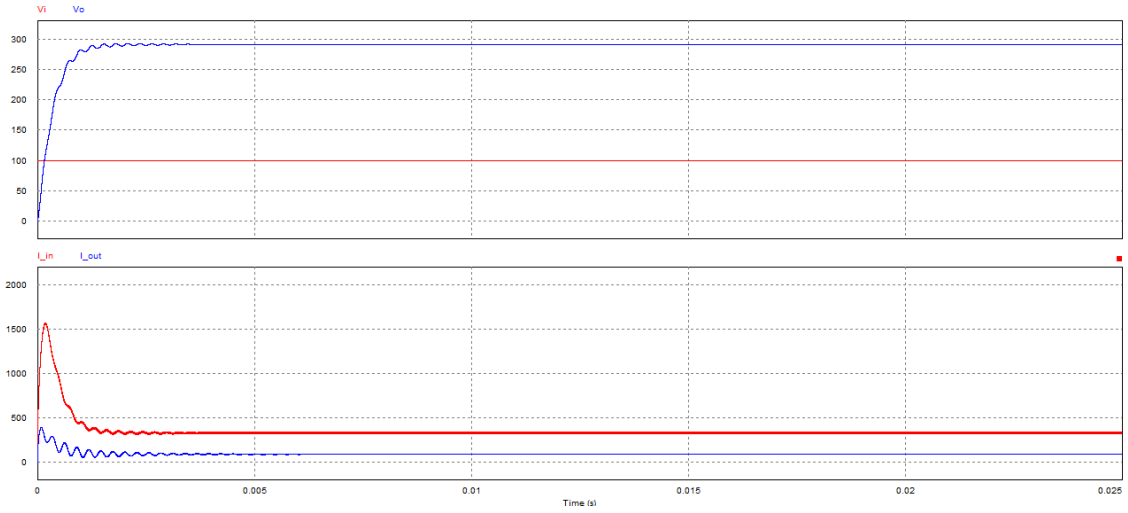


Figure 4.4: Ideal Ćuk step response

Besides the big peak in the inductor currents (that add up in the transistors) the same duty-cycle does not take the voltage to the desired level - which obviously justifies the use of a closed loop controller.

4.2.1 Model

Considering the inductors' and input series resistances as the only non-ideal elements, the system was modelled in MATLAB.

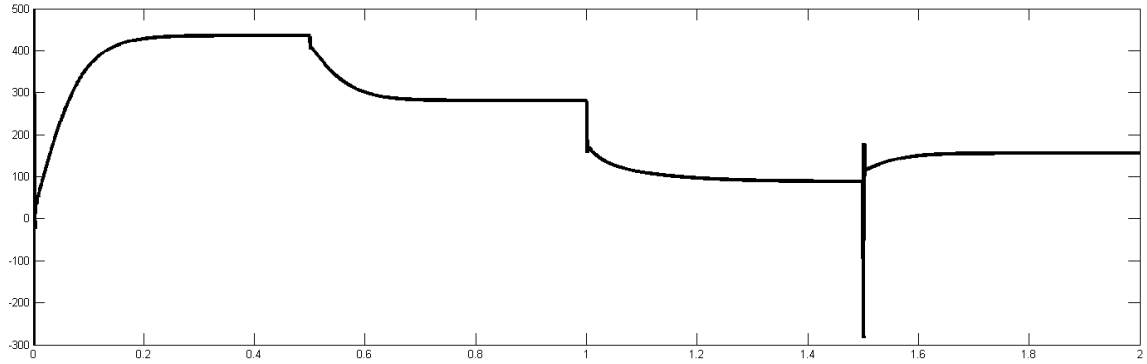
One test was made that shows the response of the converter, controllers and model to several disturbances:

- t=0s to t=0.5s - stabilization after start-up in the middle of full-load operation (because of an unexpected restart, for example). The simulation shows the absolute need for start-up

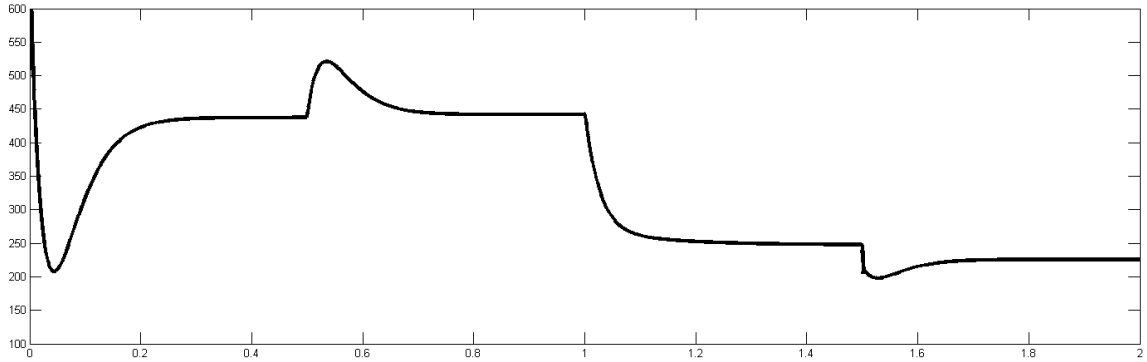
sequences and emergency stops: after a reset, the converter must be in idle state, and only after a start-up sequence must the switches start commutating.

- t=0.5s to t=1s - response to a step load variation of 40A - this perturbation induces a voltage swing on the output voltage. Keeping the current loop critically damped with the same response time, this swing can be reduced with a larger capacitance at output.
- t=1s to t=1.5s - response to a step voltage reference variation of 200V - although not included in the project specifications, the converter shows a good response to a reference voltage variation.
- t=1.5s to t=2s - response for a step variation of input voltage of 20 V - this variation can be caused by a failure in the input energy bank - the abrupt drop in input voltage causes the current in the inductors to swing, leading to potentially catastrophic results.

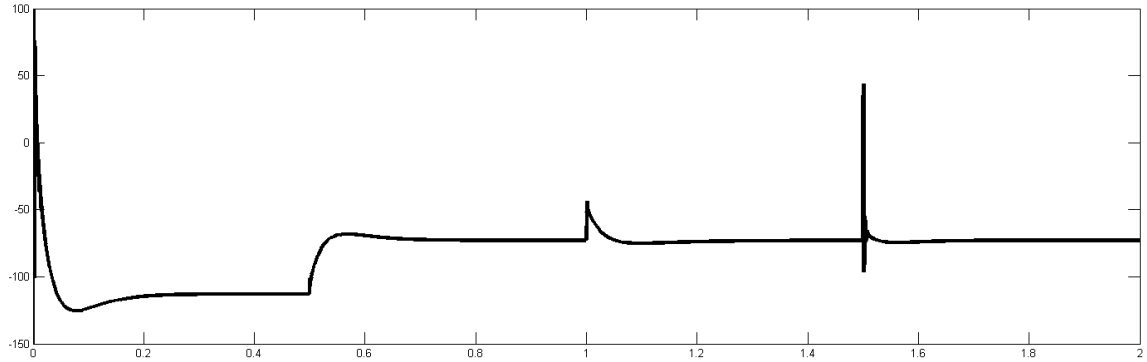
Sampling time of the controller is 0.01 ms. Figures 4.5 and 4.6 show the MATLAB output of the simulation described above.



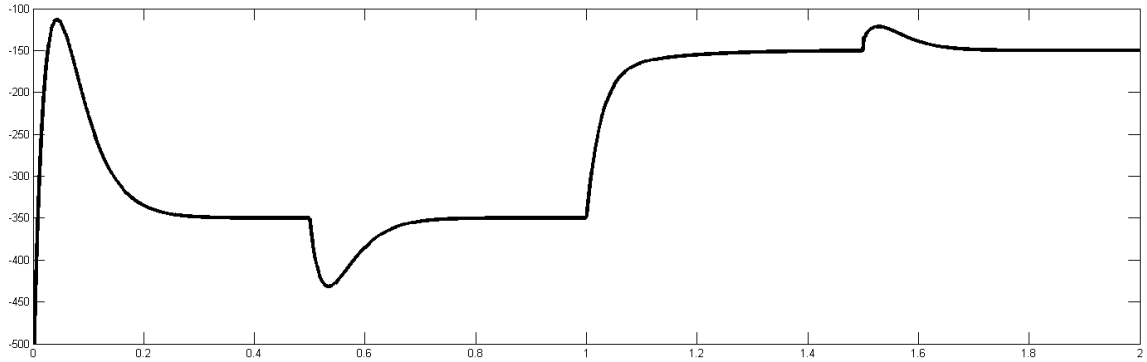
(a) Input current



(b) Ćuk capacitor voltage



(c) Output current



(d) Output voltage

Figure 4.5: Step response to disturbances

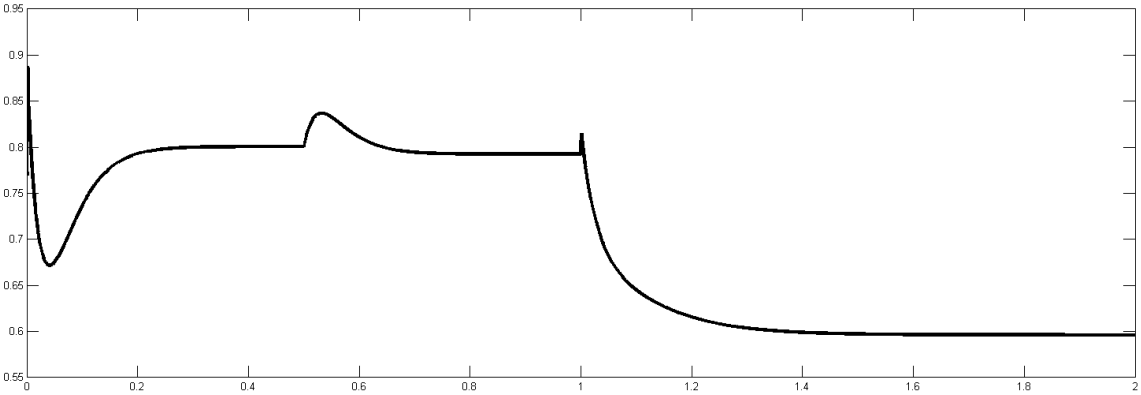
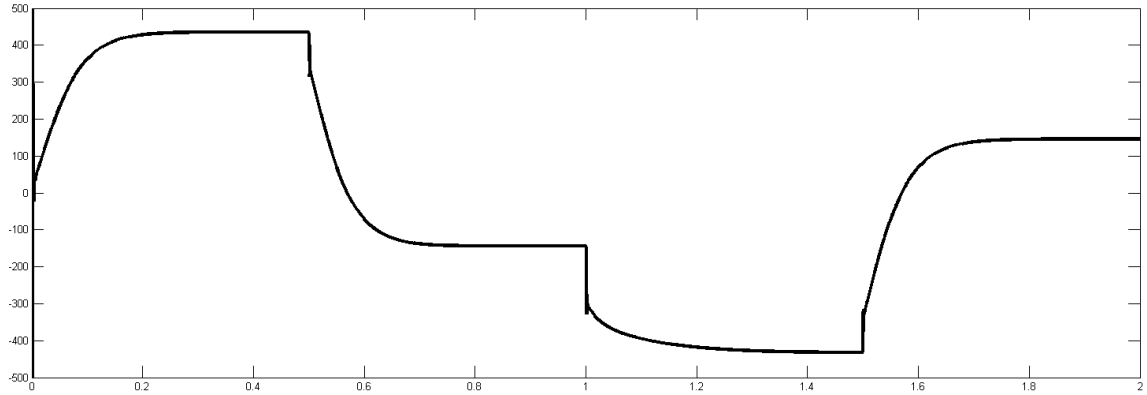


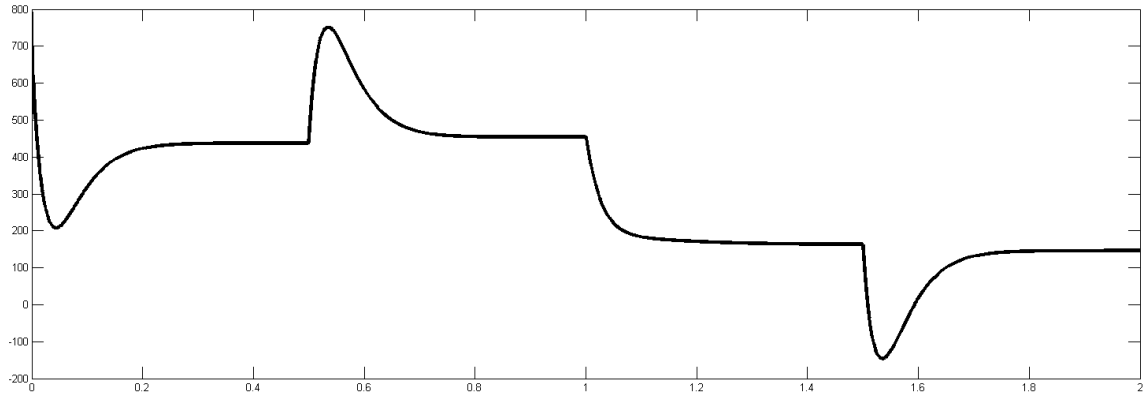
Figure 4.6: Duty Cycle

To test the bi-directionality and buck-boost functionality of the converter, another test was made (Figures 4.7 and 4.8):

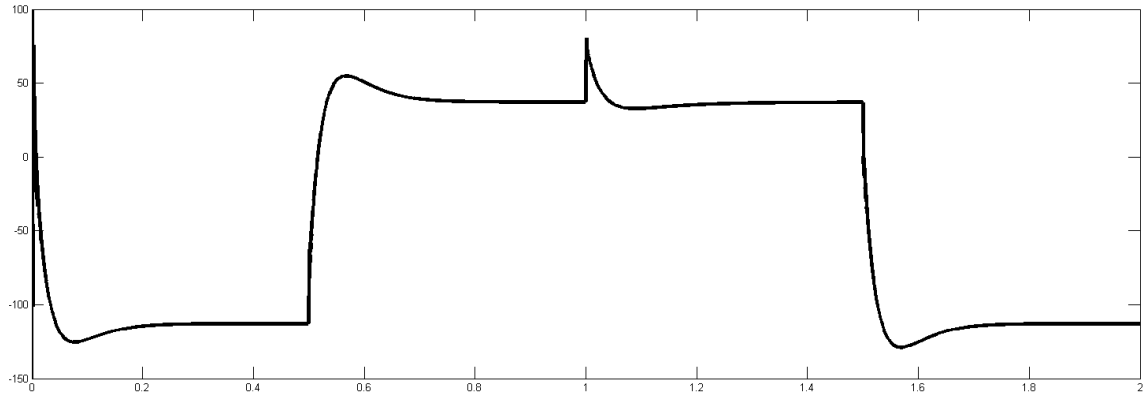
- t=0s to t=0.5s - stabilization after start-up in the middle of full-load operation ()as in the previous test) - the converter is boosting voltage to the output, as well as supplying current.
- t=0.5s to t=1s - response to a step load variation of 150A (resulting in negative load, i. e., regeneration) - the converter is still boosting voltage, but supplying current to the power bank (loosely refered to as input).
- t=1s to t=1.5s - response to a step voltage reference variation of 300V (resulting in a voltage output reference lower than input voltage) - the converter is bucking voltage to the output and still supplying current to the input.
- t=1.5s to t=2s - response to a step load variation of 150A (in order to return the load to its original value, i. e., consuming power) - the converter is now supplying current to the output, finalizing the test of the four combinations of buck-boost bi-directional energy flow.



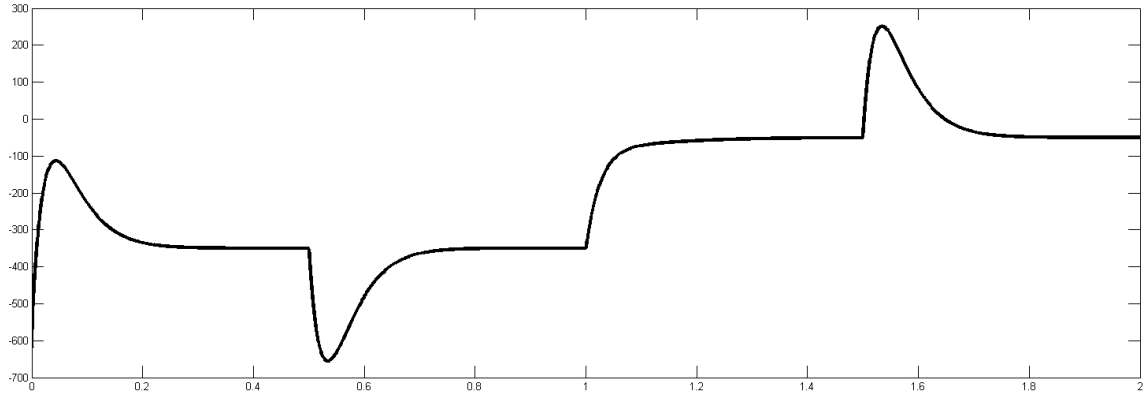
(a) Input current



(b) Ćuk capacitor voltage



(c) Output current



(d) Output voltage

Figure 4.7: Step response to disturbances

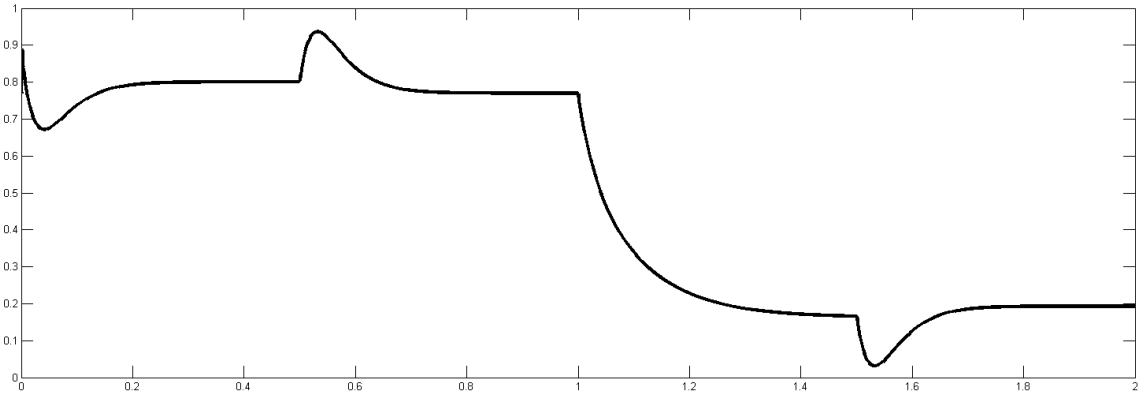


Figure 4.8: Duty Cycle

4.3 Switches

After request of the SPICE model of the SiC MOSFET from the supplier, a simple simulation is made to show the influence of the external gate resistance on commutation (Figures 4.9, 4.10 and 4.11).

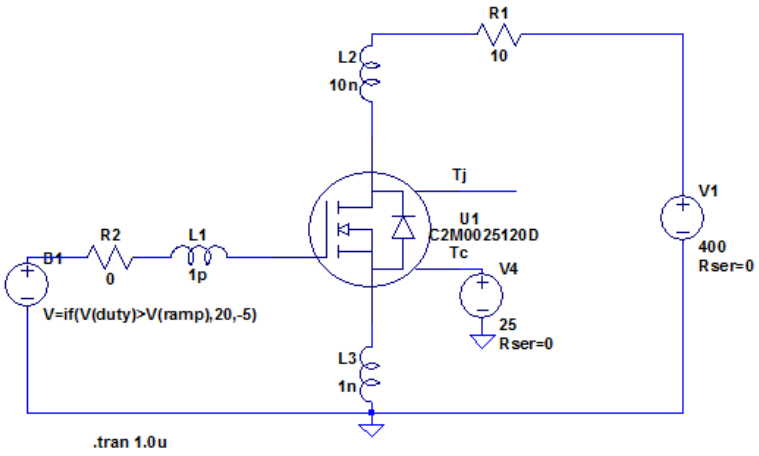
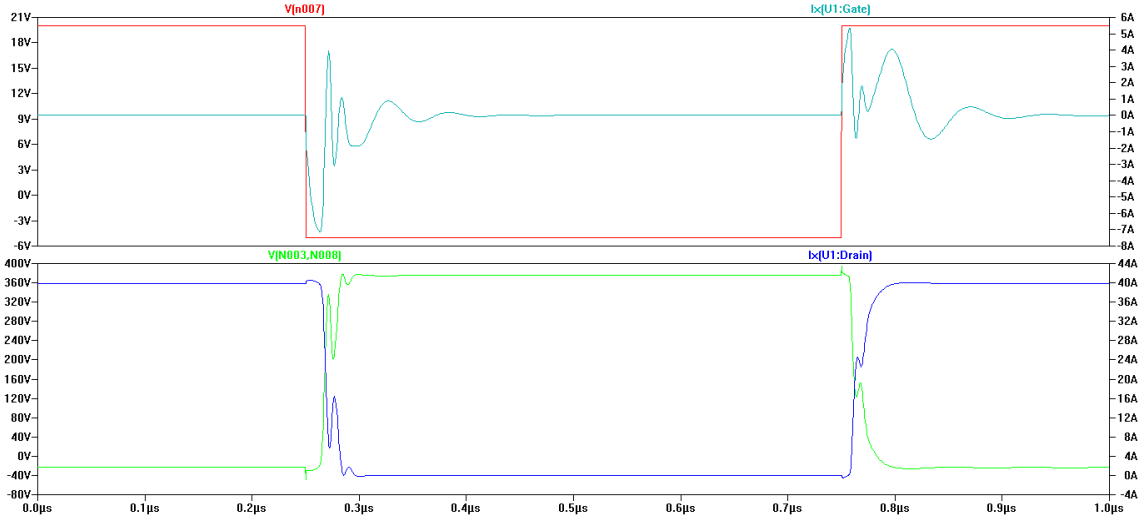
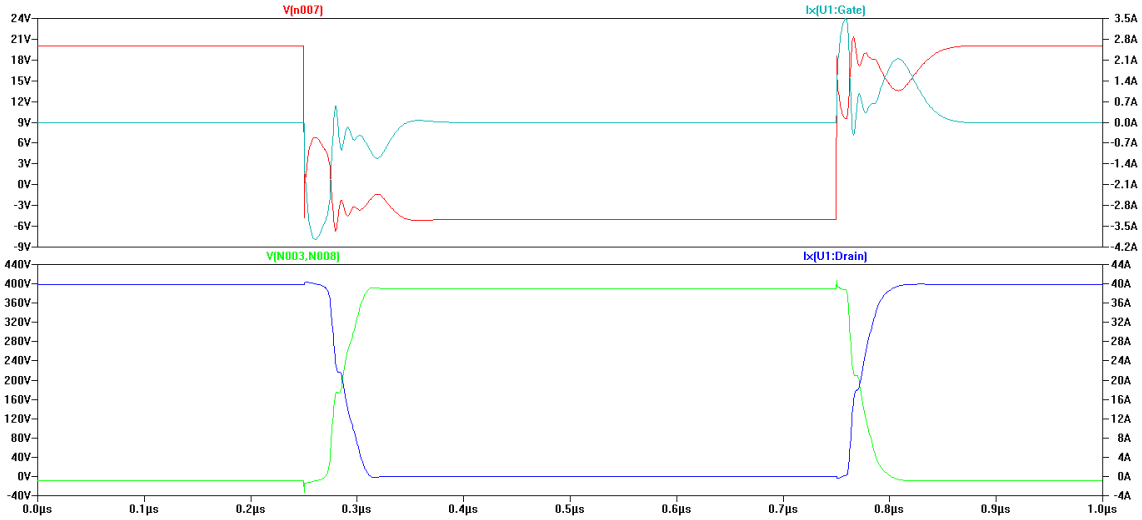


Figure 4.9: Switch test circuit

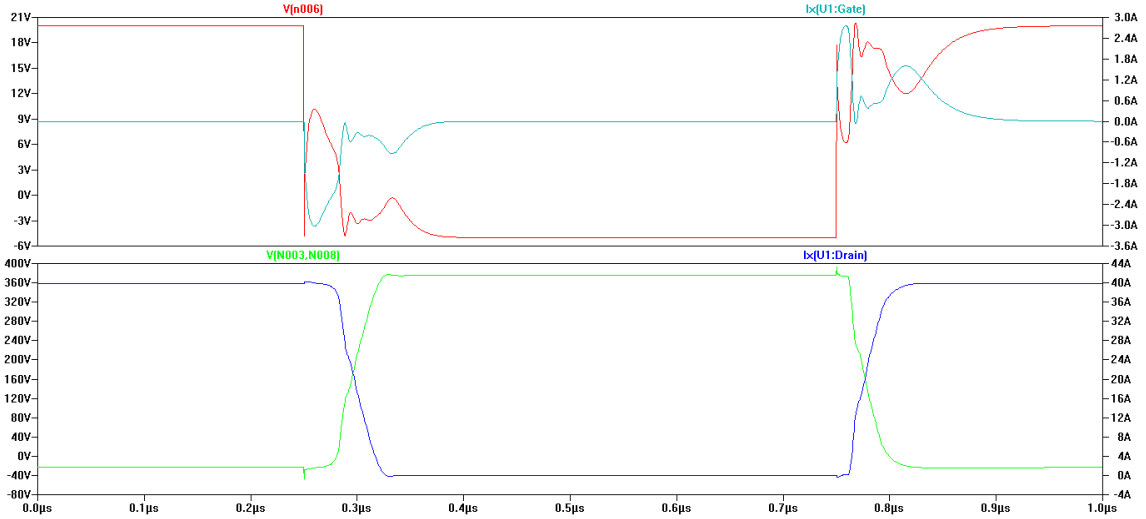


(a) $R_{Gext} = 0\Omega$

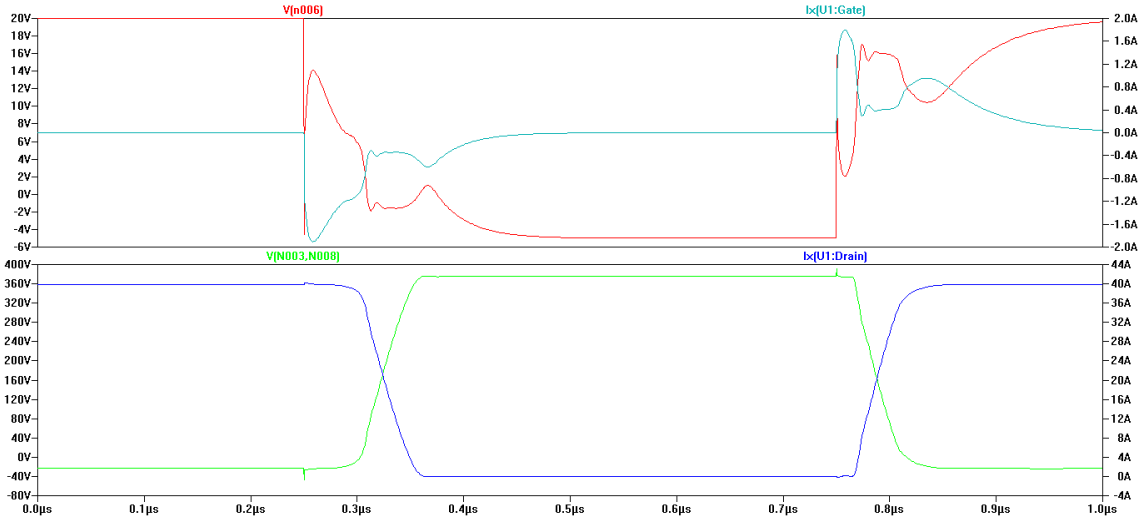


(b) $R_{Gext} = 3\Omega$

Figure 4.10: External gate resistor influence on commutation - $0\Omega - 3\Omega$



(a) $R_{Gext} = 5\Omega$



(b) $R_{Gext} = 10\Omega$

Figure 4.11: External gate resistor influence on commutation - $5\Omega - 10\Omega$

Where only the turn-on and off delays are dependant on the external gate resistance. Because this delay does not contribute to additional losses, the extra effort required when using smaller gate resistance is not worth it.

4.4 Driver

The driver is responsible for turning on and off the MOSFETs, supplying the correct voltages, with the right transient currents.

The voltage shift driver was simulated on PSIM:

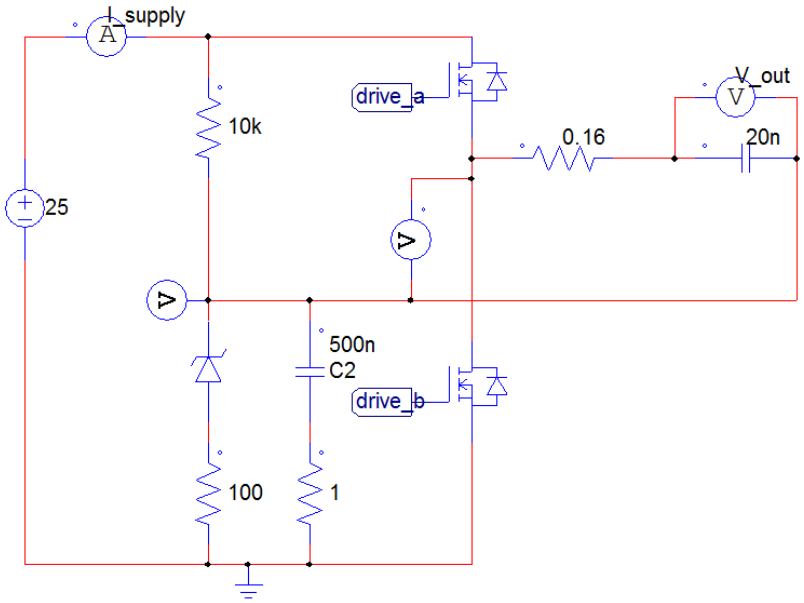


Figure 4.12: Switch test circuit

with steady-state results:

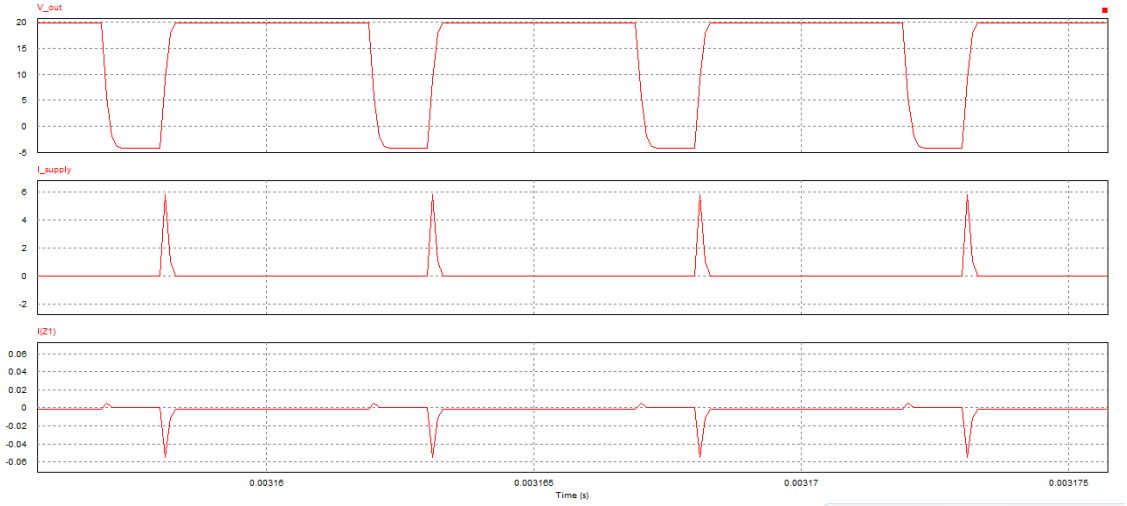


Figure 4.13: Switch test circuit

4.5 Control

Simulating in PSIM the control previously designed in MATLAB, the start-up response (zero-load) with a -100A step at t=0.6s and 100A step at t=1.2s is shown below.

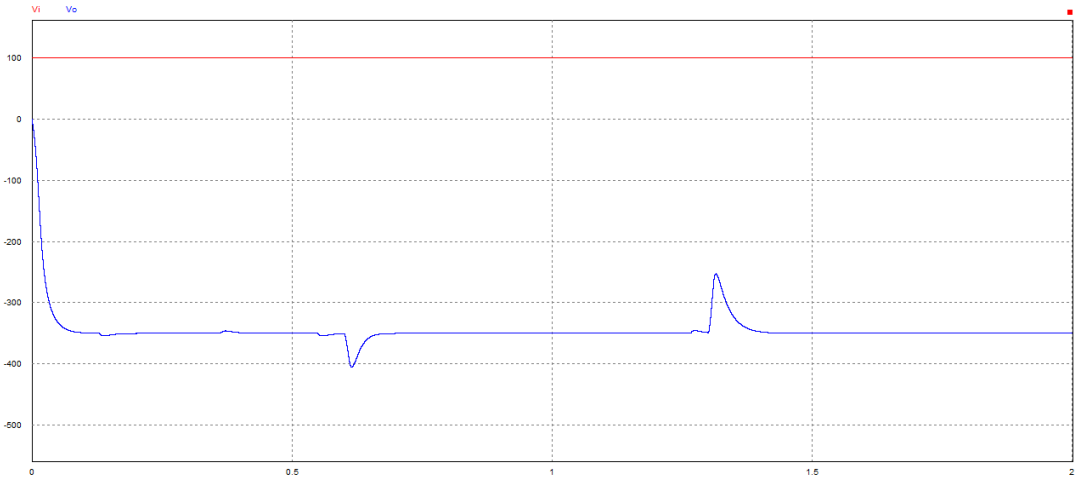


Figure 4.14: Input and Output voltage

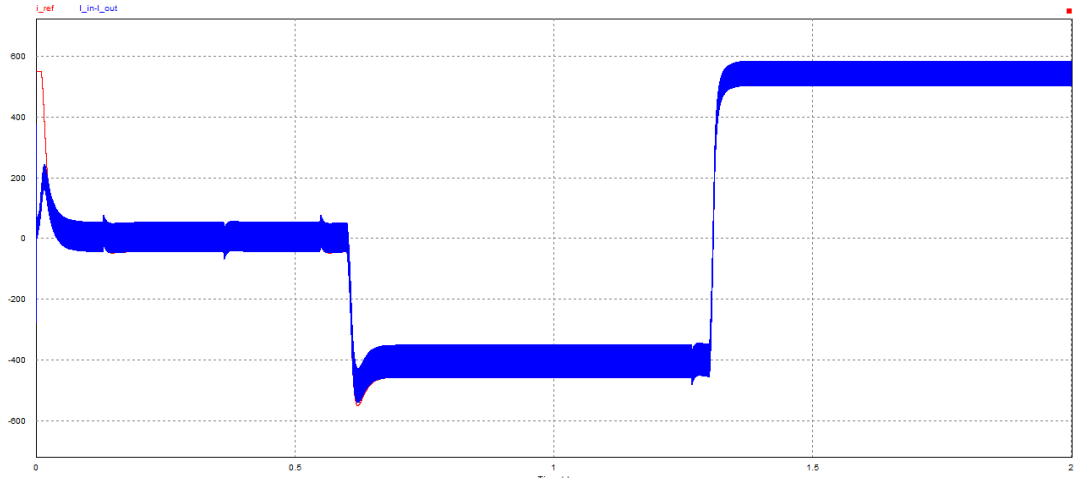


Figure 4.15: Current reference vs current response

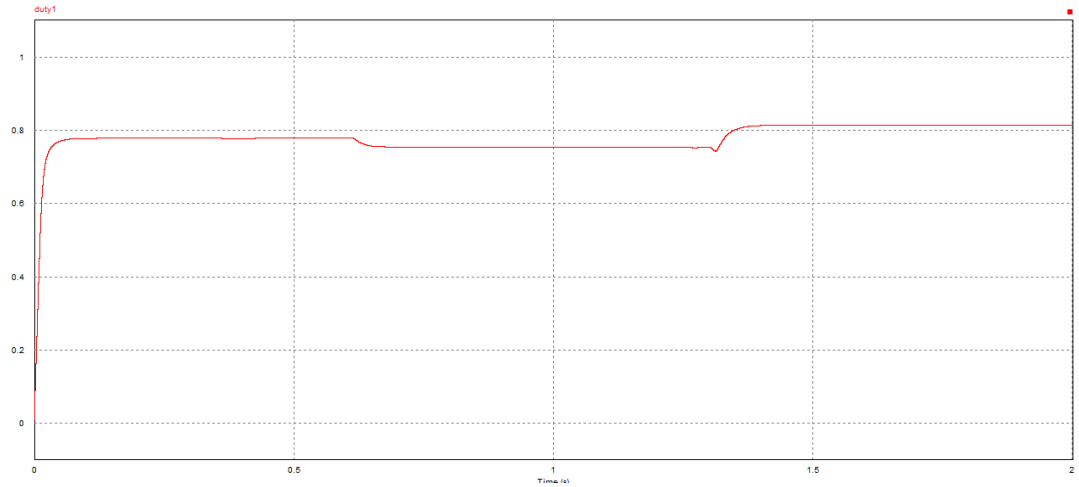


Figure 4.16: Duty Cycle

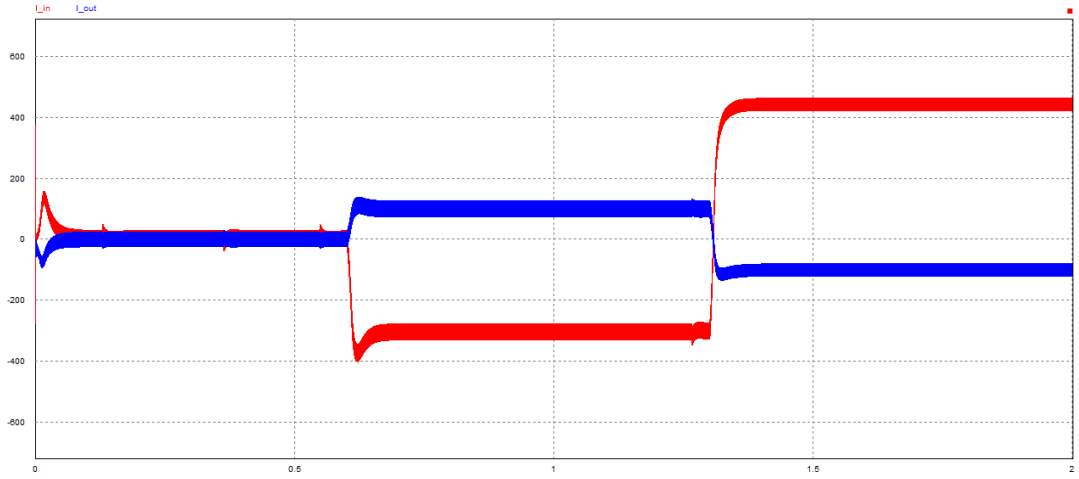


Figure 4.17: Input and Output currents

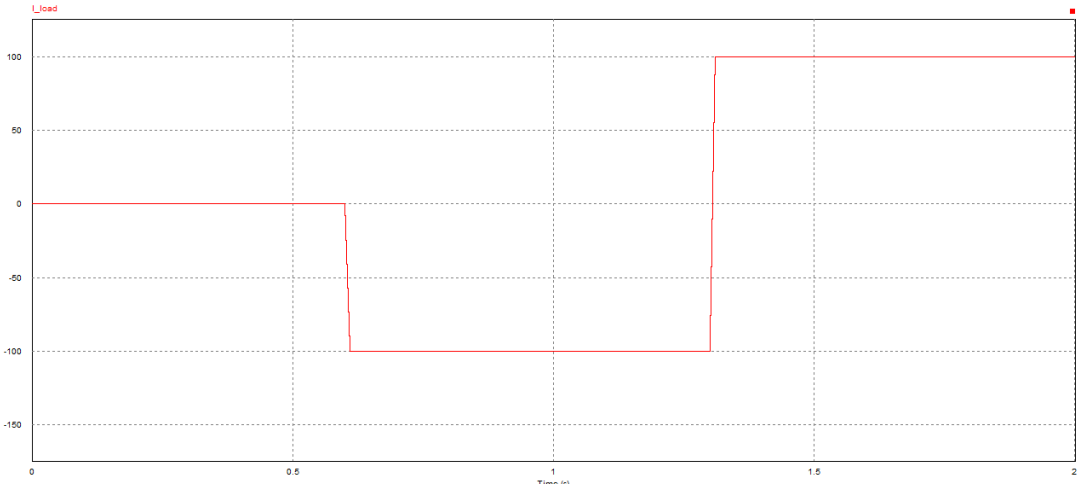


Figure 4.18: Load current

Where the influence of the change of current demand is apparent, but with the controller limiting the current in the converter with almost no overshoot and with the converter behaving as expected.

To simulate a more complex and close to reality load (and application), the converter was connected to a PMSM motor input voltage bus:

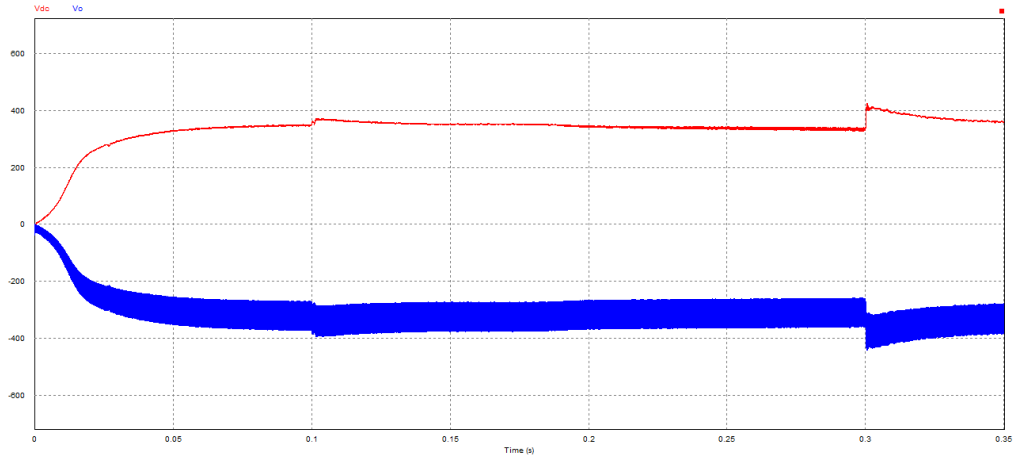


Figure 4.19: Input and Output voltage

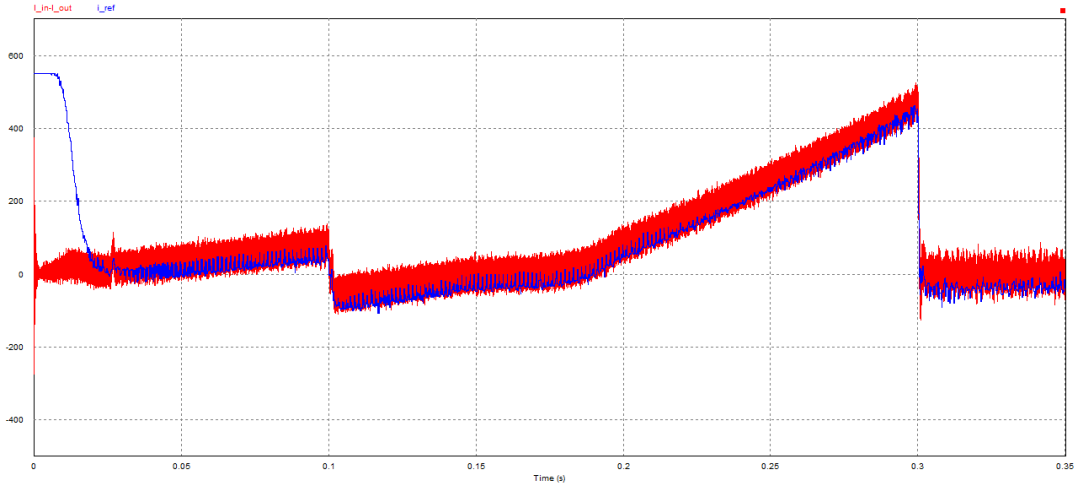


Figure 4.20: Current reference vs current response

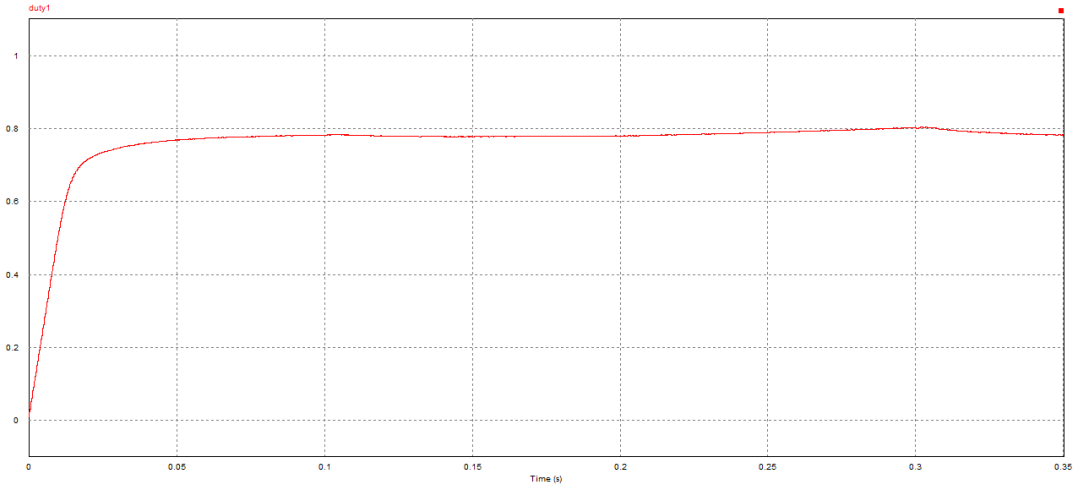


Figure 4.21: Duty Cycle

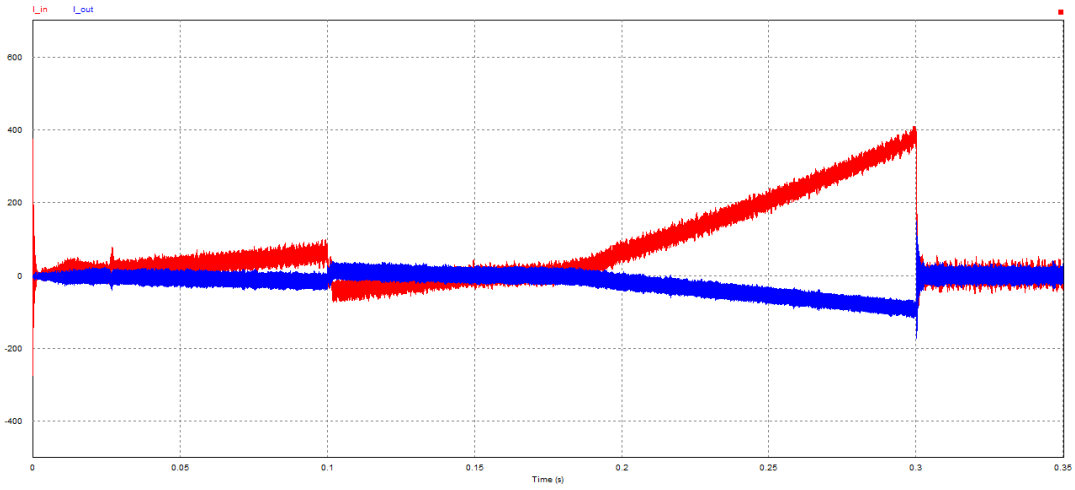


Figure 4.22: Input and Output currents

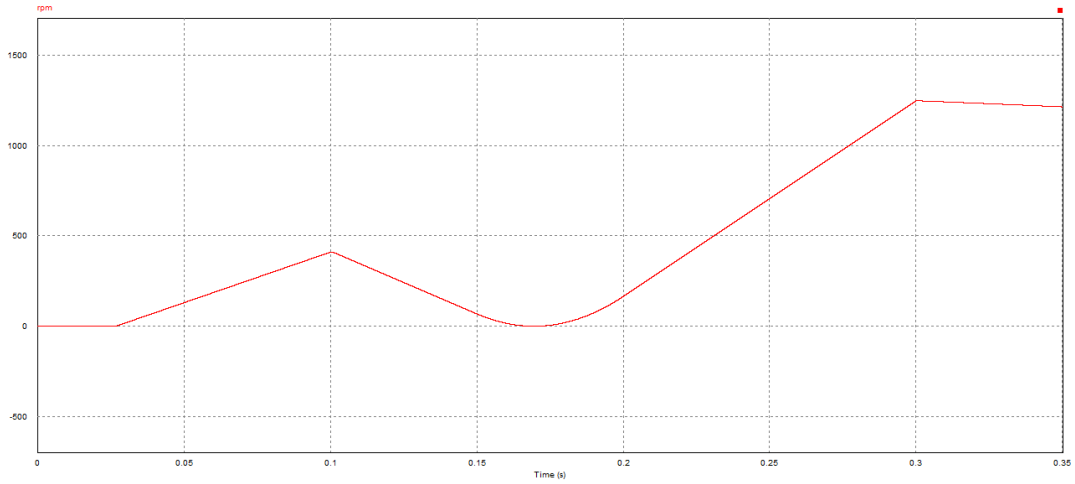


Figure 4.23: Motor speed (rpm)

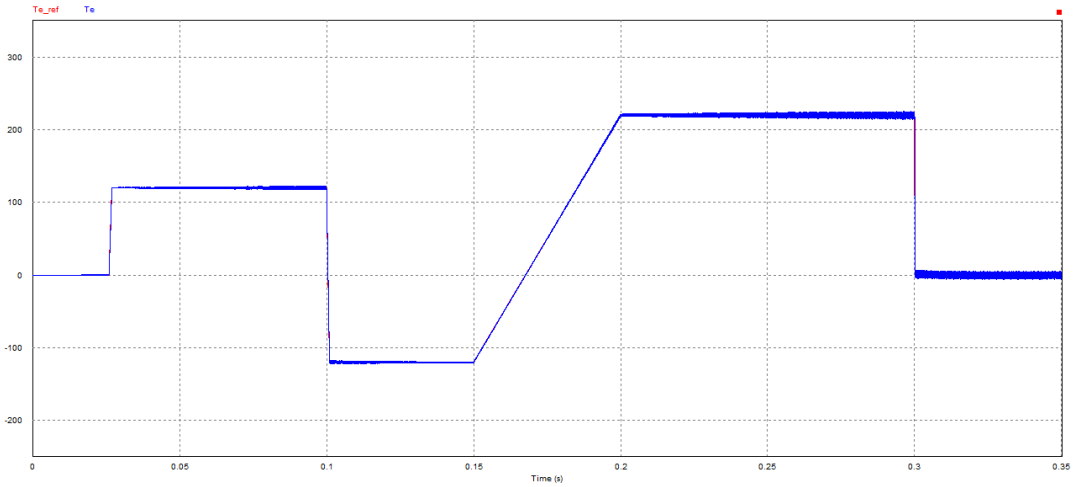


Figure 4.24: Motor torque

4.6 Modifications - converter paralleling

After the preliminary design and computational analysis, it is clear the multitude of converter parts that need paralleling:

- The SiC MOSFETs need paralelling, and the issues associated with it have already been covered.
- A single capacitor isn't capable of handling all the current necessary.
- Making inductors for currents superior than 150A requires a big technological effort, and normally results in inductor paralleling.

By splitting the converter into 2 or more identical topologies, we can achieve the following:

- Massive reduction of parallel switching issues - Isolation between MOSFET groups: the last MOSFET to turn off is only affected by the current running in its group. I. e., the peak current in the MOSFET, in a balanced state, is now $\frac{Total_{current}}{N_{arms}}$
- Each driver is relieved from the stress of switching all the MOSFETs.
- Each isolated SMPS powering the drivers will need less power.
- If the switching waves are interleaved, the input and output ripple frequency multiplies by the number of arms and the magnitude of the ripple divides by the same amount.
- The layout is not radically altered

at the cost of:

- The drivers must be multiplied by the number of arms.
- If an interleaved approach is used, the complexity of the controller increases.
- The total number of components must be a multiple of the number of arms.

4.6.1 Number of arms

Splitting the converter in 3 seems the most sensible answer: There are already 3 capacitors in the design, and there would be 3 inductors on the input as well. At first sight, the number of transistors doesn't seem very compatible with this approach. However, given the peak pulse current the MOSFET can take is 250A, splitting the converter in less than 3 arms would yield a current bigger than a single transistor can take.

4.6.2 Interleaving

If the converter arms were to be switched with the same phase (synchronously), the input and output inductances would be in parallel - and the consequent equivalent inductance would be reduced. If the switching is done with shifted phases, the frequency at output will be multiplied by the number of arms and counter the inductance reduction. This way, input and output will see the same ripple as with inductances equal to the ones in each arm. The switching frequency will be the base frequency in each arm multiplied by the number of arms.

4.6.3 Layout

The adaptations necessary to switch independent arms include de-shunting the Ćuk capacitors, using individual inductors and splitting the drivers. Modularity comes naturally, and each arm should have a connector to pass sensor information and receive supply and control signals.

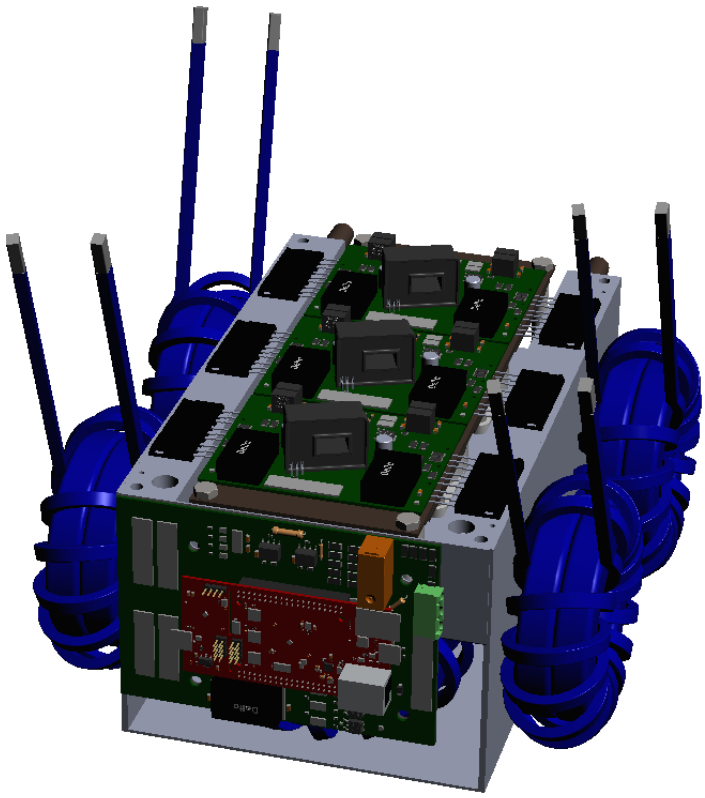


Figure 4.25: Interleaved prototype 3D render

The signal board (vertical) provides power and PWM signals to the half-bridge drivers, and receives the current sensor information from each driving module.

Chapter 5

Tests design and planning

5.1 Introduction

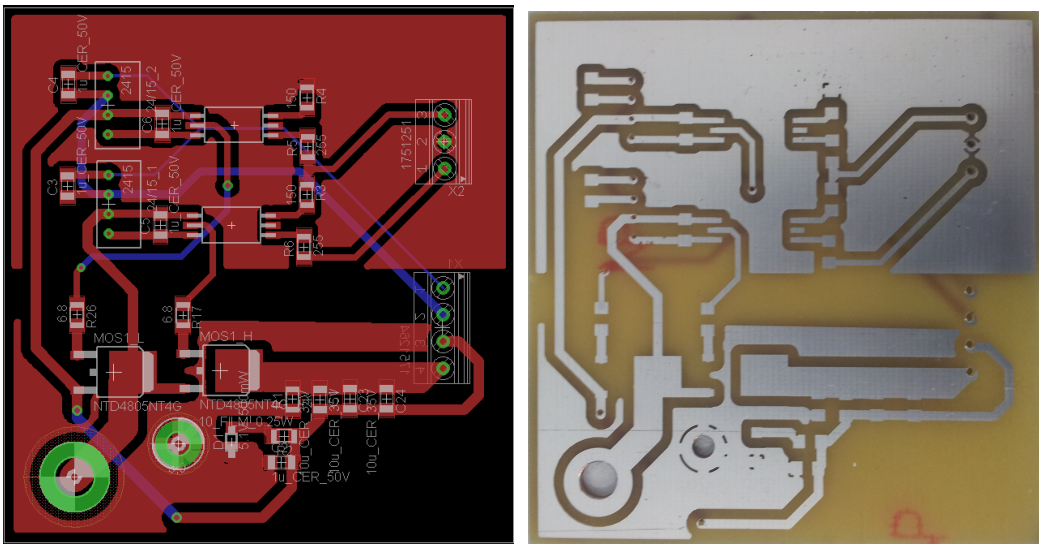
This chapter will describe the tests designed to assess the performance of the converter and its structural parts.

5.2 Driver

The driver section is responsible for translating a PWM signal from the microcontroller into open and close commands for the SiC MOSFETs, while providing isolation between signal and power.

Each SiC MOSFET array is controlled by a single driver block, made up of pre-drivers (isolated integrated circuits), voltage shifter (to provide the positive and negative voltage necessary to switch the SiC MOSFETs) and a last stage MOSFET halfbridge (to provide the necessary current to drive the SiCs).

Each MOSFET in the half-bridge requires a dedicated pre-driver and isolated power-supply.



(a) Eagle Layout (b) Printed Circuit Board

Figure 5.1: Driver preliminary concept

The test plan to assert the functionality of the driver is comprised of distinct phases:

- **Microcontroller correct signal generation** - a benchmark program was created, generating a PWM wave with duty cycle controlled with two buttons.
- **Pre-driver operation** - correct generation of drive signal to the MOSFET buffers.
- **Pre-drivers wave cross** - check if there is crossing in the MOSFET buffers gate waves.
- **Driver output wave** - test of the driver output against a series resistor and capacitor emulating the SiC MOSFET and gate resistor.
- **Single MOSFET commutation** - commutation of a single MOSFET with large external gate resistance and increasing frequency
- **Single MOSFET commutation with load** - Setup with a pull-up power resistor with a parallel flyback diode and increasing rail voltage.
- **Single MOSFET commutation with load** - commutation of the MOSFET with decreasing external gate resistance.
- **Parallel MOSFET commutation with load** - commutation of two MOSFETs to compare gate waveforms.

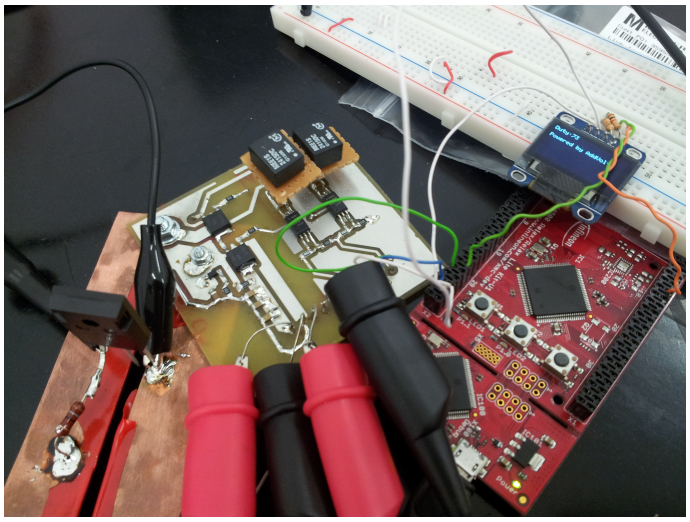


Figure 5.2: Driver setup for the first SiC MOSFET commutation

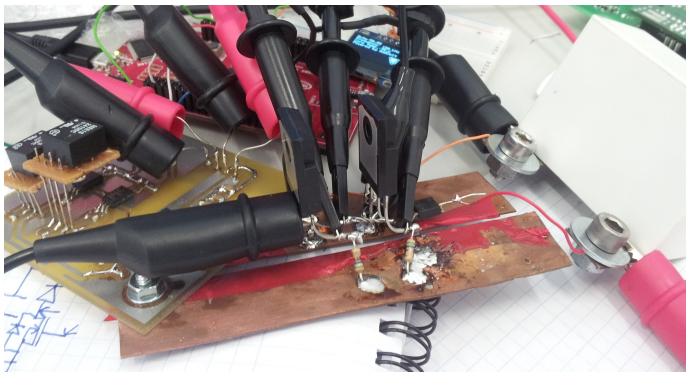


Figure 5.3: Paralleling of two SiC MOSFETs commutation

5.3 Open-loop Converter

The open-loop (fixed duty-cycle) testing of the converter asserts the quality of the electrical signals in the power elements as well as the integration of the driver in the solution. As such, the tests should include:

- In idle-state (both MOSFETs off):
  - Gate voltages
  - Applying an input voltage, measure voltage on Ćuk capacitor
- With low frequency commutation (50kHz) and limited input voltage source:
  - Gate on and off voltages and currents
  - Input voltage and current
  - Output voltage and current

  - MOSFETs Voltage and current
  - Voltage on Ćuk capacitor

- Repeated tests with high frequency (350kHz) commutation and limited input voltage source
- Repeated tests with increased input voltage
- Parallelisation of second MOSFET
- Test with unlimited voltage source

5.4 Display

To test the display interface, a simple breadboard test can be made. The microcontroller will supply and communicate with the display on the breadboard (together with the necessary pull-ups on the communication lines).

5.5 Sensors

The sensoring chain must be tested from analogic input to digital converted value:

- Verify analog input value
- Verify analog output value
- Verify ADC conversion value item Verify conversion from ADC (0-4096) to measurement unit (voltage, current or temperature)

Ultimately, if all steps are generated correctly, the information shown on display should be coherent with the state of the converter.

5.6 Microcontroller

The tasks to be executed by the microcontroller must be timed to ensure there are no relevant delays nor missed deadlines.

Each function can be timed by toggling a port at its beginning and end.

5.7 Protections

A miniature of the protection concept was assembled on veroboard to verify its functionality.

The test consists on passing the voltage limits on each detector (and also both at the same time) to verify if the PWM is inhibited at the output of the protection circuitry.

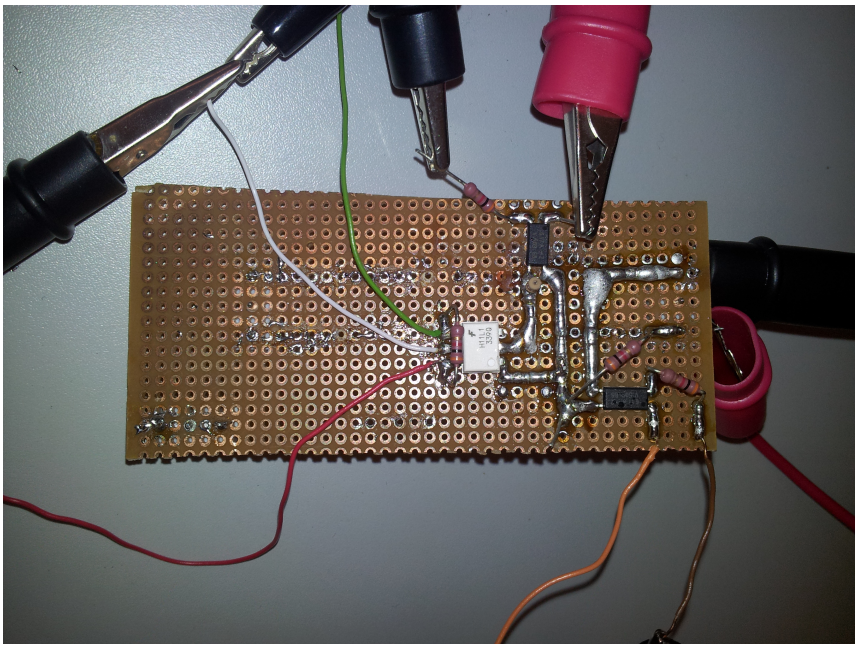


Figure 5.4: PWM disable protection circuit concept

Chapter 6

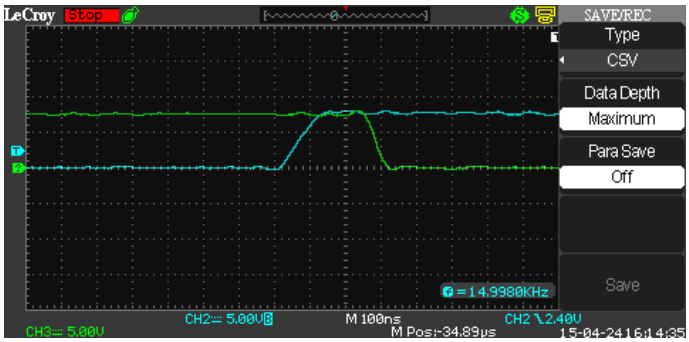
Experimental Validation

6.1 Introduction

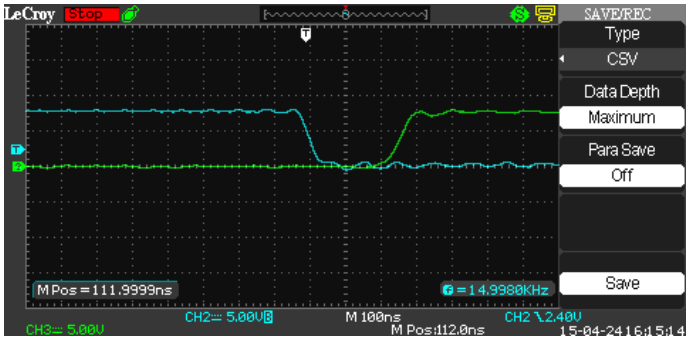
This chapter will assess the results of the tests designed in the previous chapter. Only the most relevant test results will be shown.

6.2 Driver

The first relevant result was observed when verifying the gate voltages from the optically isolated drivers intended to command the buffer MOSFETs. After initial pre-driver testing, it was observed there was superimposition of the gate signals due to the asymmetry between on and off input delay (Figure 6.1):



(a) Pre driver bridge turn-on



(b) Pre-driver bridge turn-off

Figure 6.1: Pre-driver gate waves

After low passing the IC drivers input signal to delay the turn-on (Figure 6.2):

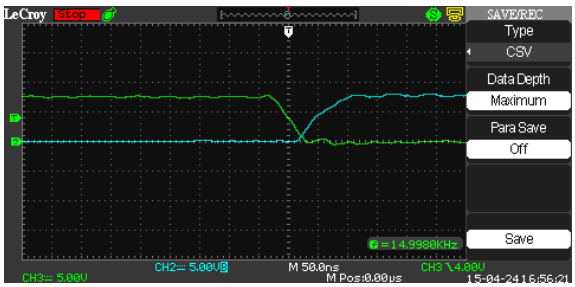


Figure 6.2: Turn-on with corrected timing

Where the superimposition now doesn't exist. It is important to leave enough dead-time to avoid superimposition but also vital to not leave the SiC gate floating (when both buffer MOSFETs off) for too long.

After first setup assembly, the SiC MOSFET was switched with no load and increasing frequency (25kHz, 75kHz, 150kHz, 200kHz) and a large gate resistor ($Rg_{ext} = 17\Omega$) (Figure 6.3).

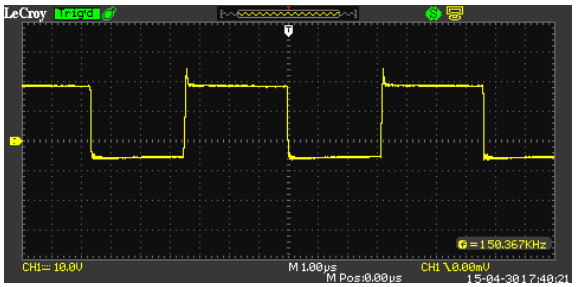
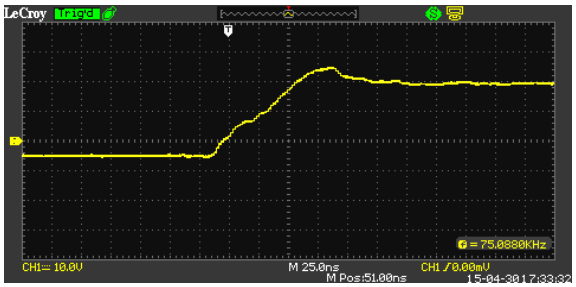
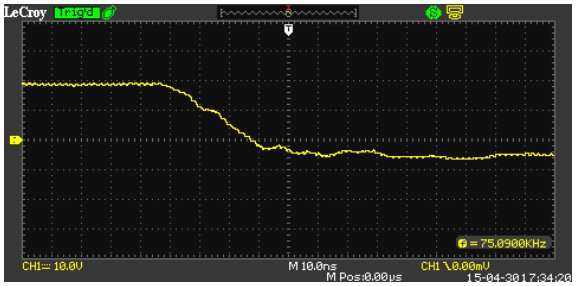


Figure 6.3: 150 kHz commutation

Capturing the detail of the gate voltage turn-on and off waves (Figure 6.4):



(a) Turn-on

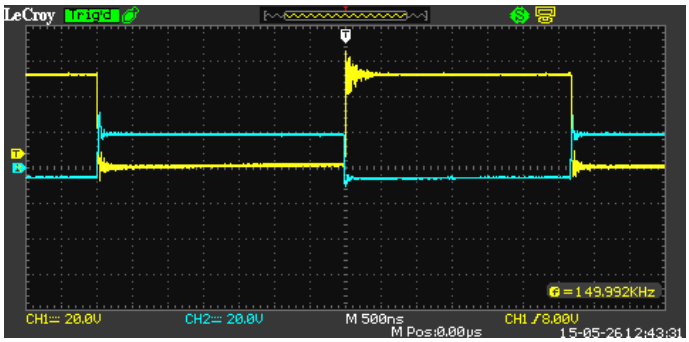


(b) Turn-off

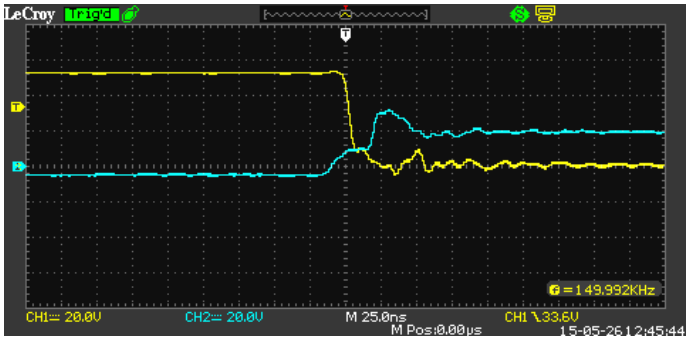
Figure 6.4: Commutation wave

At 200kHz the low MOSFET in the pre-driver buffer over-heated. Both were replaced with higher voltage rating MOSFETs and testing resumed.

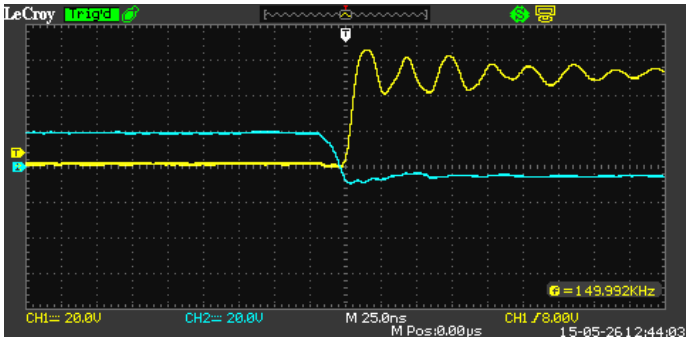
After assembly of the frewheeling diode, load resistance and rail capacitor (Figure 6.5):



(a) Switching



(b) Turn-on

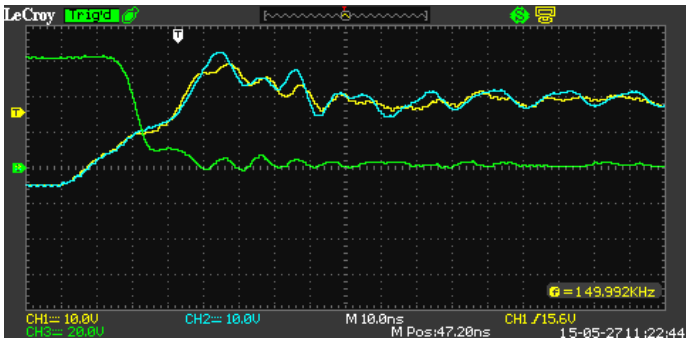


(c) Turn-off

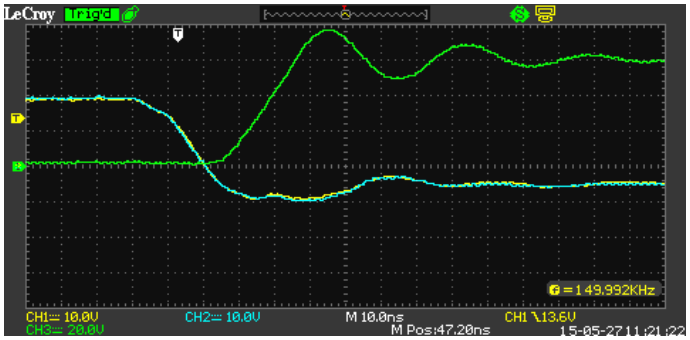
Figure 6.5: Commutation at 50V and average 0.8A

Where there is ringing on the gate at turn-on and a smooth turn-off. However, the drain-source ramp is high on both transitions.

After assembly of the second SiC MOSFET (Figure 6.6):



(a) Turn-on



(b) Turn-off

Figure 6.6: Commutation at 60V and average 0.33A

Where it can be observed the matching in the waveforms of the gate voltage. The Miller-plateau appears clearly on the turn-on gate waveform.

6.3 Converter

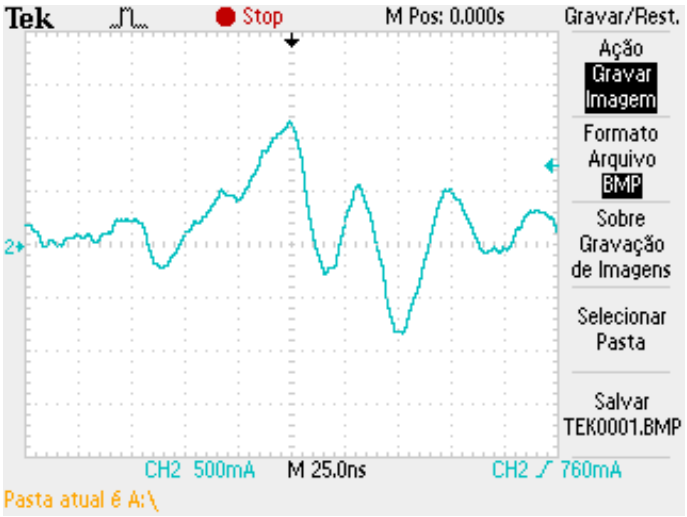
This section is organised by signals and not by test setups. I. e., for each signal, a sequence of test results is shown based on the evolution of the tests and modification of the setup. This way, the influence of converter modifications can be easily analised.

6.3.1 Gate current

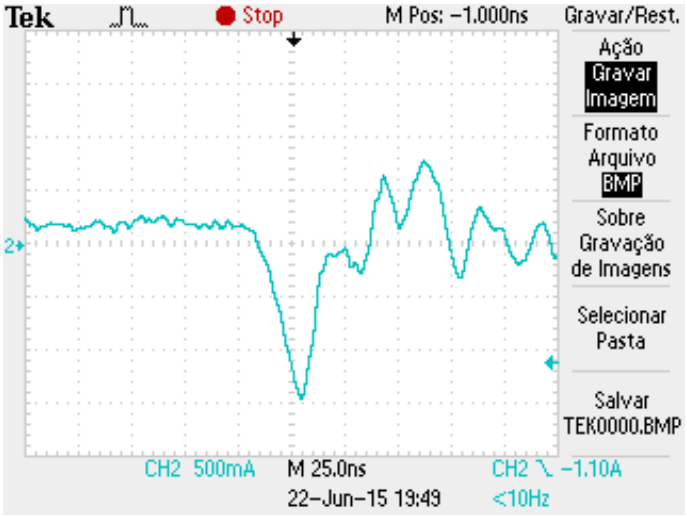
Setup:

- $L_{in} = L_{out} = 50uH$
- $C_{cuk} = 220uF$
- One SiC (160mOhms) per arm with $R_{gate} = 5\Omega$
- Auxiliar power supply (PS23023): 23.5V, 0.20A
- $V_{in} = 5.0V$
- $I_{in} = 0.60A$

- Switching Frequency = 50 kHz
- Duty = 50%
- Load = R (10 Ohm)



(a) Turn-on



(b) Turn-off

Figure 6.7: Gate currents on input side MOSFET

The peak currents indicate the MOSFETs are indeed switching. The oscillation after the switching is of no concern, as it is a consequence of the rapid opening/closing of the switch. However, two major problems are clear:

- The rate of change (and magnitude) of current at turn-on is low.
- At turn-on there is an undesirable oscillation before the actual turn-on.

To counter the first symptom, the resistance can be halved, doubling the peak current.

The second symptom is consequence of the lack of isolation of the isolated DC-DC converters at high-frequencies. The parasitic capacitor from input to output does not block frequencies above 100kHz. The switching times of both pre-driving MOSFETs (30ns) and SiC MOSFETs (10ns) correspond to oscillating frequencies between 3MHz to 10MHz. Because of that, signals at that noise level are not isolated and propagate from driver to auxiliary power supply and power circuitry.

To counter this problem, a low pass LC filter ($f_c \simeq 11kHz$) was inserted between auxilliary supply and remaining circuitry. Because the self-resonant frequency of the inductor was at 2.2MHz, another low pass ($f_c \simeq 40kHz$) was inserted at the driver supply to isolate the high-frequency noise from the signal side of the circuitry, as well as a hand wound copper wire with significant clearance to minimize any stray capacitances in it.

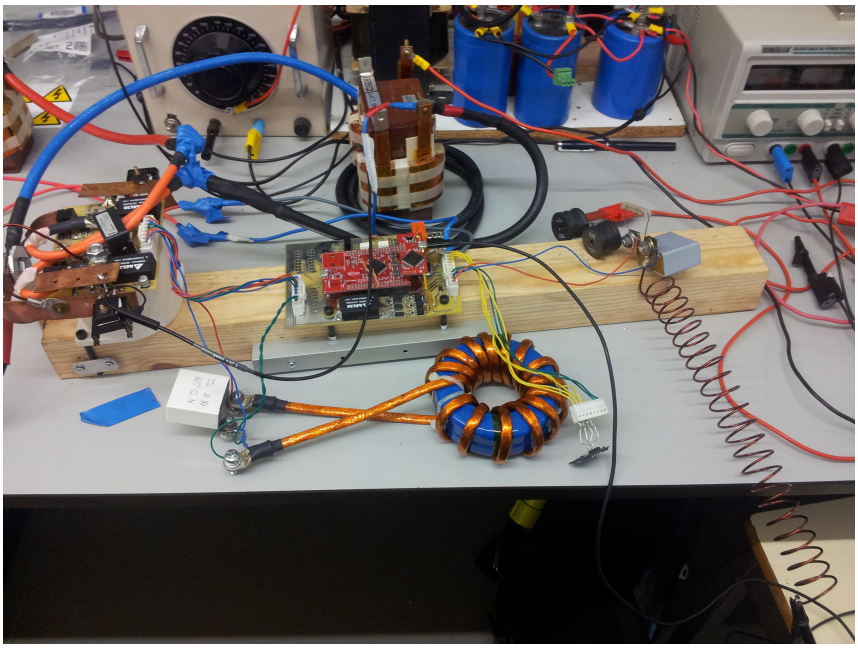
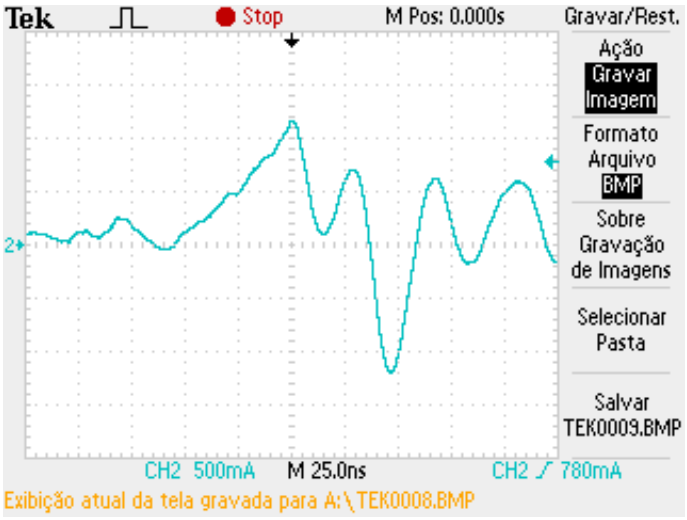
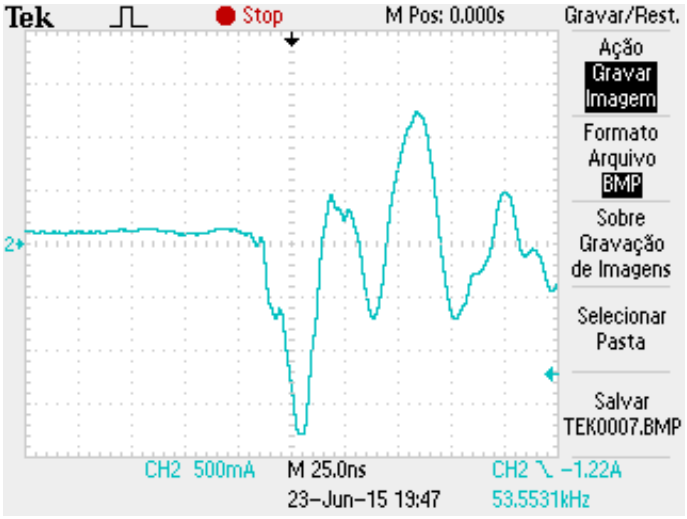


Figure 6.8: Setup with supply filters

After halving resistances and inserting filters:



(a) Turn-on

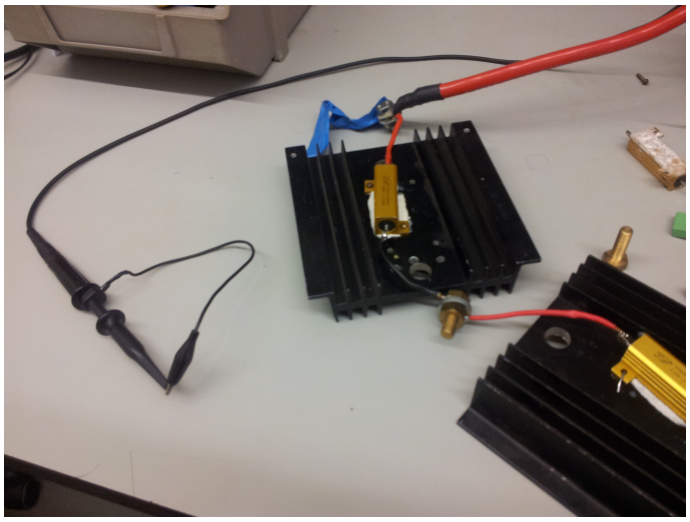


(b) Turn-off

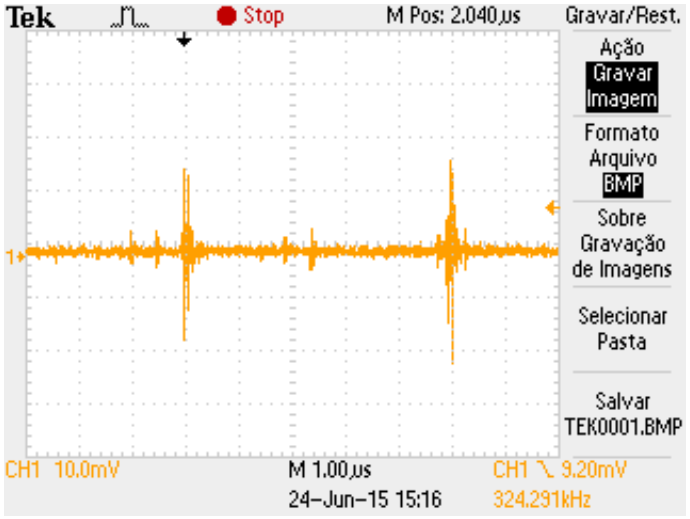
Figure 6.9: Gate currents on input side MOSFET

Where the oscillation after commutation has increased due to an increase in current flow and reduction of damping (caused by halving the gate resistance).

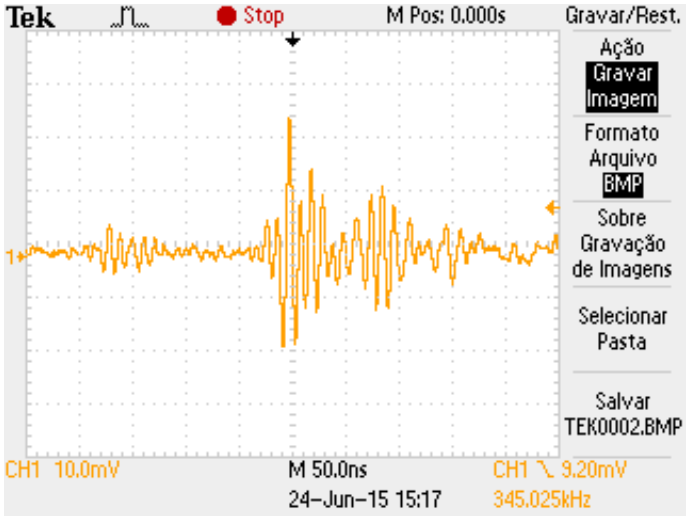
However, even if the driver was supplied from an external battery and the input voltage was left unconnected, the noise could still be picked by the oscilloscope (left in the air):



(a) Oscilloscope probe location



(b) Noise on commutation



(c) Noise detail

Figure 6.10: Airborne electromagnetic noise

The conducting plates in the power inductors act as capacitors at high frequencies. To prevent the high frequency current from running through the inductors (and consequently all the power circuitry), two large clearance inductors were hand-wound in series with the power inductors:

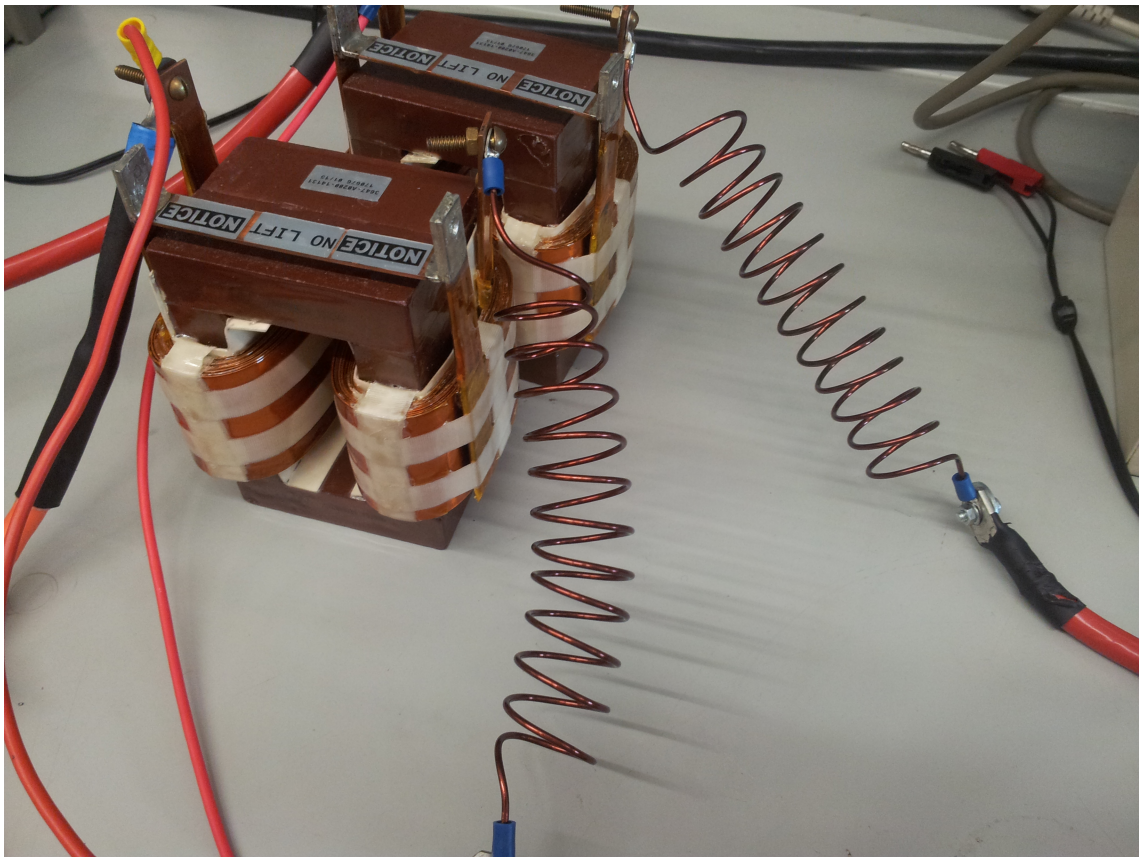
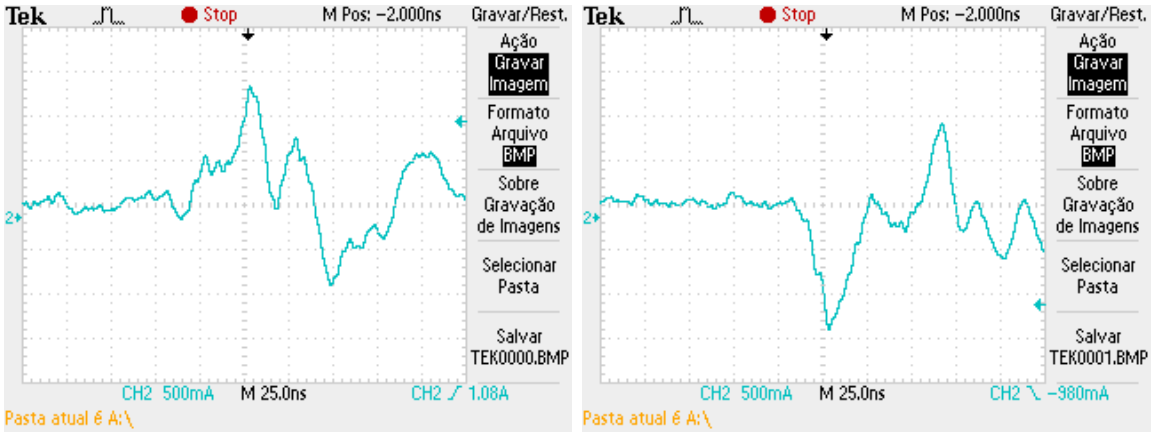


Figure 6.11: Series inductors

After all the filtering done above, and for a 12V input voltage:

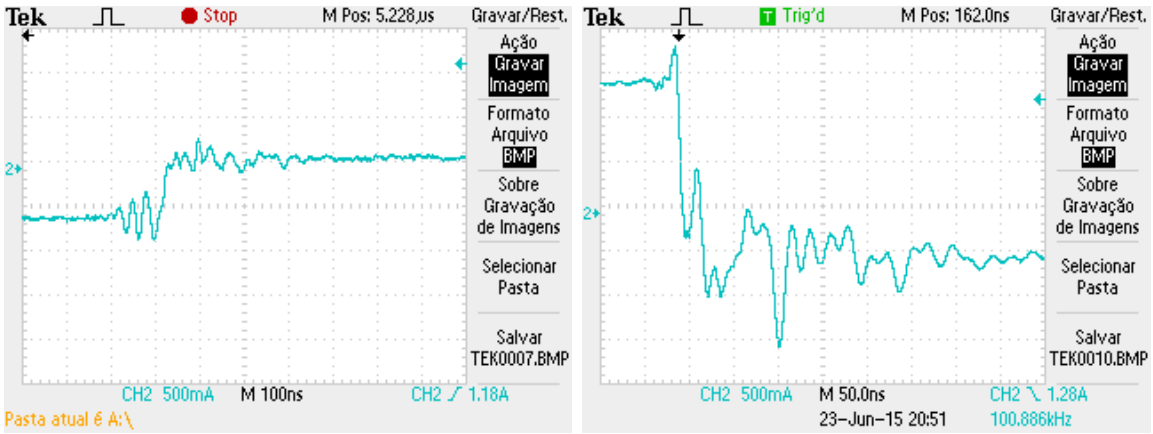


(a) Turn-on (b) Turn-off

Figure 6.12: Gate currents on input side MOSFET

The turn-on is still slower than turn-off. The source of the problem is the lack of high-frequency damping (with ferrite beads), the over-tight dead-time on the pre-driver (where undesired current runs through the low MOSFET, that should already be closed) and driver layout (distant filtering capacitors add inductance to the high-side path). This issues can only be corrected in a new PCB.

The corresponding source currents:

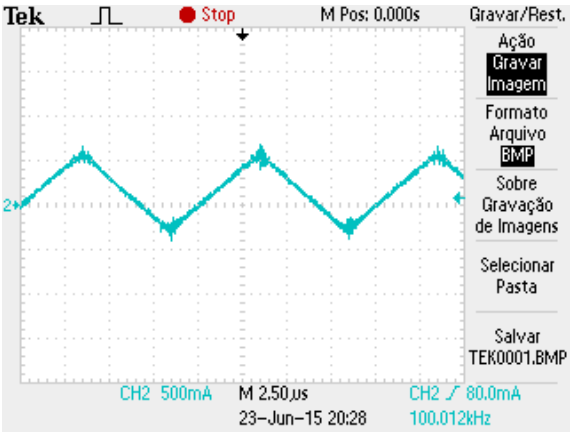


(a) Turn-on (b) Turn-off

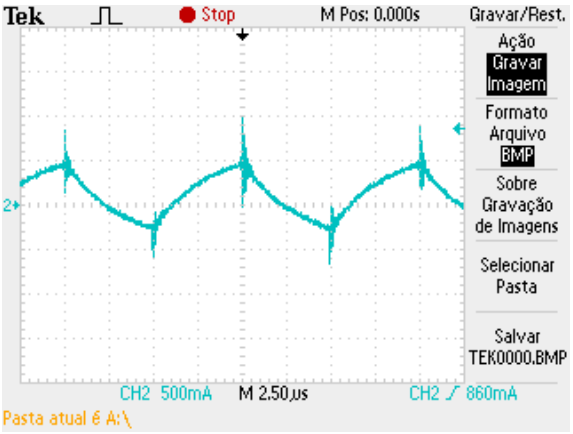
Figure 6.13: Source currents on input side MOSFET

Show fast commutation (near 25ns).

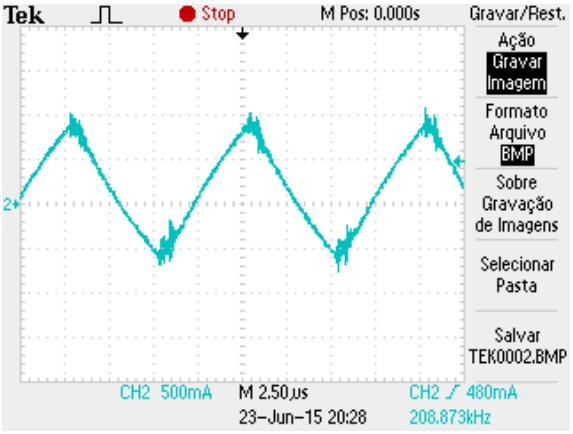
The inductors' currents:



(a) Input current



(b) Output current



(c) $I_{in} + I_{out} = I_{MOS_1} + I_{MOS_2}$

Figure 6.14: Source currents on input side MOSFET

Show the correct operation of the converter, with one of the most importance characteristics of this topology: filtered current output.

6.4 Microcontroller

The measurement of the execution time of the main tasks running in the processor yielded:

- ADC result processing - $75\mu s \sim 100\mu s$, with main subtasks:
  - Conversions (0-4095 ADC values to voltages and currents) - $50\mu s$
  - Voltage and current controller - $25\mu s \sim 35\mu s$
  - Duty Cycle update - $10\mu s$
- Display 8x16 block refresh - $1\mu s \sim 6\mu s$
- Get Microcontroller Core temperature - $1\mu s \sim 3\mu s$
- Filter iteration - $500ns$

6.5 Display

Generating the logo image from the Matlab script, and printing the strings in the I^2C display, updating the duty-cycle information in real-time yields the result below.

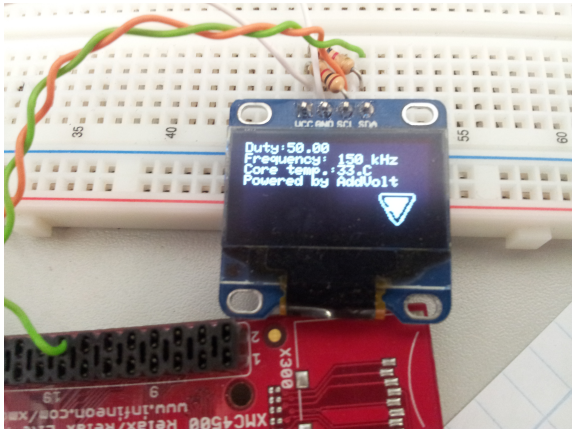


Figure 6.15: Display proof of concept

Chapter 7

Conclusion

The Ćuk converter exhibits promising results, both on simulations and experimental results. Its unusual property of having an output with constant current is advantageous to many applications that need a constant flow of power (such has a motor application). The inductors at input and output make it possible to keep load or energy bank distant from the converter, because the stray inductances will have minimum impact (as shown in the motor simulation). As for the experimental results, even without an ideal setting (because of the hand made filters and inductors), the tests showed good results, with the high-frequency noise being the limiting factor to an increase in switching frequency. The topology's most significant disadvantage is the higher order of the system, which adds some complexity to the modelling and controller.

The converter can also be easily adapted to work as an active boost (commonly refered to as buck-boost), by removing the output inductor and using the Ćuk capacitor as output capacitor.

The Silicon-Carbide technology was studied and tested, proving to be a good alternative to the ubiquitous Silicon. The driver designed had some minor flaws (to be easily corrected in a next design), with its biggest disadvantage being the power consumption at high frequency switching. The SiC manufacturer Cree is now developing transistors with inferior gate voltage thresholds (C3M0065090J switches with -4V to 15V) which will reduce power consumption further.

The modelling techniques used yielded good results, either on MATLAB (where the model was inserted) and when the controller was ported to PSIM. A robust model will give accurate responses, and with accurate responses a reliable controller can be designed.

Working in a start-up helped understanding the working environment of a technological company, taking advantage of all the resources and know-how in it. From negotiating and ordering a custom made inductor from Poland to studying a PCB's manufacturer design rules, the work developed ended up being much more broad and extensive than initially thought. As a direct consequence, it was also extremely satisfying to do so.

The solution developed is only an initial prototype, but it is enough to understand the implications of the design chosen and will allow a more conscious second prototype design.

7.1 Future Work

7.1.1 Control

As the processing power of computers and microcontrollers increases, some techniques used to reduce computation requirements start losing pertinence. Maybe forcing restrictions on the models to be able to linearize it is not the best solution nowadays. Designing a control method for a model as accurate as possible with minimum approximations might be the next step.

As an intermediary step, adapting the (I, PI) controller parameters to the real-time operating point might also be a viable solution.

7.1.2 Electronics

Lower cost of driver, possibly by using independent power sources to positive and negative gate voltage. Improve performance of driver, especially during SiC turn-on.

Ferrite beads in series with gate resistors to reduce ringing. Reformulation of pre-driver to reduce power consumption.

Prepare for next generation SiC MOSFETs (different pins, packages, characteristics and ratings).

Integrated magnetics: use a single core to wind input and output inductor, as well as the transformer for isolation.

Increase frequency further. The effects on the driving circuitry are consequence of the switching time. However, on the power elements, the switching frequency plays the major role. Increasing the frequency will be a great challenge because of the inductors (where at >1MHz the stray capacitances, skin and proximity effect will limit the number of turns), capacitors (increasing the stress caused by the alternating current) and on the MOSFETs (where the switching losses will be higher). However, increasing frequency will bring faster response converters (given the lower inductance and capacitance levels) with smaller components.

Appendix A

Open Loop Transfer Functions

A.1 Current Loop

$$\frac{\hat{y_i(s)}}{\hat{u(s)}} = C_i\,(sI-A)^{-1}\,B_u =$$

$$C_i \frac{1}{s^4+(\frac{R_2}{L_2}+\frac{R_1}{L_1})s^3+(\frac{(1-U)^2}{C_1L_1}+\frac{R_1R_2}{L_1L_2}+\frac{U^2}{C_1L_2}+\frac{1}{C_2L_2})s^2+(\frac{U^2R_1}{C_1L_1L_2}+\frac{(1-U)^2R_2}{C_1L_1L_2}+\frac{R_1}{C_2L_1L_2})s+\frac{(1-U)^2}{C_1C_2L_1L_2}}$$

$$\begin{bmatrix} s^3+\frac{R_2}{L_2}s^2+(\frac{1}{C_2L_2}+\frac{U^2}{C_1L_2})s & -\frac{1-U}{L_1}s^2-\frac{(1-U)R_2}{L_1L_2}s-\frac{(1-U)}{C_2L_1L_2} & -\frac{U(1-U)}{L_1C_1}s & d.c. \\ d.c. & d.c. & d.c. & d.c. \\ -\frac{U(1-U)}{C_1L_2}s & -\frac{U}{L_2}s^2-\frac{R_1U}{L_1L_2}s & s^3+\frac{R_1}{L_1}s^2+\frac{(1-U)^2}{C_1L_1}s & d.c. \\ d.c. & d.c. & d.c. & d.c. \end{bmatrix} B_u =$$

$$\frac{1}{det(sI-A)}X_2\left(\frac{1}{L_1}\left(s^3+\frac{R_2}{L_2}s^2+(\frac{1}{C_2L_2}+\frac{U^2}{C_1L_2}+\frac{U(1-U)}{C_1L_2})s\right)+\frac{1}{L_2}\left(s^3+\frac{R_1}{L_1}s^2+(\frac{(1-U)^2}{C_1L_1}+\frac{U(1-U)}{L_1C_1})s\right)\right)$$

$$-\frac{I_L}{C_1}\frac{1}{1-U}\left((\frac{U}{L_2}-\frac{1-U}{L_1})s^2+(\frac{R_1U}{L_1L_2}-\frac{(1-U)R_2}{L_1L_2})s-\frac{(1-U)}{C_2L_1L_2}\right)=$$

$$\frac{1}{det(sI-A)}\frac{1}{1-U}(V_{in}-R_1I_L\frac{U}{1-U})\left(\frac{L_1+L_2}{L_1L_2}s^3+(\frac{R_1+R_2}{L_1L_2})s^2+(\frac{1}{C_2L_1L_2})s\right)$$

$$-\frac{I_L}{C_1}\frac{1}{1-U}\left((\frac{U}{L_2}-\frac{1-U}{L_1})s^2+(\frac{R_1U}{L_1L_2}-\frac{(1-U)R_2}{L_1L_2})s-\frac{(1-U)}{C_2L_1L_2}\right)=$$

$$\frac{1}{det(sI-A)}$$

$$\frac{1}{1-U}\Bigg(((V_{in}-R_1I_L\frac{U}{1-U})\frac{L_1+L_2}{L_1L_2})s^3+$$

$$((V_{in}-R_1I_L\frac{U}{1-U})\frac{R_1+R_2}{L_1L_2})-\frac{I_L}{C_1}(\frac{U}{L_2}-\frac{1-U}{L_1}))s^2+$$

$$((V_{in}-R_1I_L\frac{U}{1-U})\frac{1}{C_2L_1L_2}-\frac{I_L}{C_1}\frac{R_1U-(1-U)R_2}{L_1L_2})s+$$

$$\frac{I_L}{C_1}\frac{(1-U)}{C_2L_1L_2}\Bigg)$$

(A.1)

A.2 Voltage Loop

$$\frac{y_i\hat{(s)}}{u\hat{(s)}} = C_v\,(sI-A)^{-1}\,B_u =$$

$$C_v \frac{1}{s^4+(\frac{R_2}{L_2}+\frac{R_1}{L_1})s^3+(\frac{(1-U)^2}{C_1L_1}+\frac{R_1R_2}{L_1L_2}+\frac{U^2}{C_1L_2}+\frac{1}{C_2L_2})s^2+(\frac{U^2R_1}{C_1L_1L_2}+\frac{(1-U)^2R_2}{C_1L_1L_2}+\frac{R_1}{C_2L_1L_2})s+\frac{(1-U)^2}{C_1C_2L_1L_2}}$$

$$\begin{bmatrix} d.c. & d.c. & d.c. & d.c. \\ d.c. & d.c. & d.c. & d.c. \\ d.c. & d.c. & d.c. & d.c. \\ \frac{-U(1-U)}{C_1L_2C_2} & -(s+\frac{R_1}{L_1})\frac{U}{L_2C_2} & s(s+\frac{R_1}{L_1})\frac{1}{C_2}+\frac{(1-U)^2}{L_1C_1C_2} & d.c. \end{bmatrix} B_u =$$

$$\frac{1}{det(sI-A)}\left(\frac{\left(R_1I_L\frac{U}{1-U}-V_{in}\right)\left(U(1-U)+sC_1(sL_1+R_1)+(1-U)^2\right)+I_L(SL_1+R_1)U}{(1-U)L_1L_2C_1C_2}\right) =$$

$$\frac{1}{det(sI-A)}\left(\frac{\left(R_1I_L\frac{U}{1-U}-V_{in}\right)\left((1-U)+sC_1(sL_1+R_1)\right)+I_L(SL_1+R_1)U}{(1-U)L_1L_2C_1C_2}\right) =$$

$$\frac{1}{det(sI-A)}\frac{1}{1-U}\left(\frac{\left(R_1I_LU-V_{in}(1-U)\right)+\left(sL_1+R_1\right)\left(sC_1(R_1I_L\frac{U}{1-U}-V_{in})+I_LU\right.}{L_1L_2C_1C_2}\right) \tag{A.2}$$

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