



Flatband voltage control in p-metal gate metal-oxide-semiconductor field effect transistor by insertion of TiO₂ layer

W. J. Maeng, Woo-Hee Kim, Ja Hoon Koo, S. J. Lim, Chang-Soo Lee, Taeyoon Lee, and Hyungjun Kim

Citation: [Applied Physics Letters](#) **96**, 082905 (2010); doi: 10.1063/1.3330929

View online: <http://dx.doi.org/10.1063/1.3330929>

View Table of Contents: <http://scitation.aip.org/content/aip/journal/apl/96/8?ver=pdfcov>

Published by the [AIP Publishing](#)

Articles you may be interested in

[Charge trapping induced drain-induced-barrier-lowering in HfO₂/TiN p-channel metal-oxide-semiconductor-field-effect-transistors under hot carrier stress](#)

Appl. Phys. Lett. **100**, 152102 (2012); 10.1063/1.3697644

[Impact of static and dynamic stress on threshold voltage instability in high-k/metal gate n-channel metal-oxide-semiconductor field-effect transistors](#)

Appl. Phys. Lett. **98**, 092112 (2011); 10.1063/1.3560463

[In 0.53 Ga 0.47 As n-metal-oxide-semiconductor field effect transistors with atomic layer deposited Al₂O₃, HfO₂, and LaAlO₃ gate dielectrics](#)

J. Vac. Sci. Technol. B **27**, 2024 (2009); 10.1116/1.3125284

[On the dc and noise properties of the gate current in epitaxial Ge p-channel metal oxide semiconductor field effect transistors with TiN/TaN/HfO₂/SiO₂ gate stack](#)

Appl. Phys. Lett. **92**, 163508 (2008); 10.1063/1.2916821

[Material and electrical analysis of hafnium titania bilayer dielectric metal-oxide-semiconductor field-effect transistors](#)

J. Vac. Sci. Technol. B **23**, 2561 (2005); 10.1116/1.2126676

Want to publish your paper in the
#1 MOST CITED journal in applied physics?

With *Applied Physics Letters*, you can.

AIP Applied Physics
Letters

THERE'S POWER IN NUMBERS. Reach the world with AIP Publishing.



Flatband voltage control in p-metal gate metal-oxide-semiconductor field effect transistor by insertion of TiO₂ layer

W. J. Maeng,¹ Woo-Hee Kim,¹ Ja Hoon Koo,² S. J. Lim,¹ Chang-Soo Lee,¹ Taeyoon Lee,² and Hyungjun Kim^{2,a)}

¹Department of Materials Science and Engineering, Pohang University of Science and Technology (POSTECH), San 31, Hyoja-Dong, Nam-Gu, Pohang 790-784, Republic of Korea

²School of Electrical and Electronic Engineering, Yonsei University, 262 Seongsanno, Seodaemun-Gu, Seoul 120-749, Republic of Korea

(Received 9 November 2009; accepted 25 January 2010; published online 24 February 2010)

Titanium oxide (TiO₂) layer was used to control the flatband voltage (V_{FB}) of p-type metal-oxide-semiconductor field effect transistors. TiO₂ was deposited by plasma enhanced atomic layer deposition (PE-ALD) on hafnium oxide (HfO₂) gate dielectrics. Comparative studies between TiO₂ and Al₂O₃ as capping layer have shown that improved device properties with lower capacitance equivalent thickness (CET), interface state density (D_{it}), and flatband voltage (V_{FB}) shift were achieved by PE-ALD TiO₂ capping layer. © 2010 American Institute of Physics. [doi:10.1063/1.3330929]

Among various high-k gate oxides, HfO₂ is a front up choice due to stable interface with silicon channel, preferable band offset, and good dielectric properties.¹ However, a large negative shift in the threshold voltage (V_{th}) up to 750 mV is a big concern for p-FETs.^{1,2} The presence of positive fixed charges caused by oxygen vacancy (V_o) in HfO₂ was proposed to be a major cause for this phenomenon.³ Since Al incorporation is supposed to compensate the V_o resulting in V_{th} shift, the use of Al₂O₃ or AlN capping layer or Al incorporation in gate oxides was proposed to suppress the V_{th} shift.⁴⁻⁶ However, compared to rather well-established techniques for V_{th} shift control using capping or alloying the gate oxides with rare earth oxides for n-FET,^{7,8} relatively little study has been reported for controlling V_{th} shift of p-FET.

Meanwhile, recent studies have shown that the SiO₂/high k interface plays a significant role in controlling V_{FB} shift due to dipole layer formation and vertical position of inserted layer is important for several different inserted oxide layers.^{9,10} For n-FET, it was shown that the V_{th} tuning is strongly correlated with the electronegativity of rare earth element.¹¹ Thus, we expect that the insertion layer composed of elements with higher electronegativity than Hf in high-k/Si interface may increase the effective work function (EWF) for p-FETs. Finding additional element to tune the V_{FB} shift besides Al containing layer would be give us more degree of freedom in fabricating high performance metal-oxide-semiconductor field effect transistors (MOSFET) devices. In this article, we investigated the insertion of plasma enhanced atomic layer deposition (PE-ALD) TiO₂ layer for HfO₂ gate oxide for controlling the V_{FB} shift of p-FET and compared the electrical properties with Al₂O₃ insertion layer. TiO₂ was chosen due to the fact that Ti has the same electronegativity ($\cong 1.5$) as Al but with relatively high dielectric constant.¹

HfO₂ and TiO₂ layers were deposited by home-made PE-ALD system. For PE-ALD of TiO₂ and HfO₂ layers, tetrakis(dimethylamino)titanium and tetrakis(dimethylamino)hafnium were used as precursors, respectively, and oxygen

plasma as a reactant. For PE-ALD La₂O₃ and Al₂O₃ layers, lanthanum(isopropyl)cyclopentadienyl [La(iPrCp)₃] and trimethylaluminum was used as La and Al precursors, respectively. The thicknesses of HfO₂ and each inserted layer were approximately 4 and 1 nm, respectively. The thickness was routinely measured using ellipsometry. X-ray photoelectron spectroscopy (XPS) measurements were carried out in Escalab 2201-XL equipped with a Mg K α x-ray source and a hemispherical detector. Postdeposition annealing (PDA) and forming gas annealing (FGA) were carried out at 400 °C for 10 min in N₂ ambient and 400 °C for 30 min in H₂ 5% -N₂ 95%, respectively. Ru was deposited using a dc magnetron sputtering as a metal gate through patterned shadow mask and Au was deposited using thermal evaporation as a backside electrode. Then, high temperature annealing (HTA) was performed at $T_a=550, 700,$ and 800 °C for 10 s in vacuum to manifest the effect of Fermi level pinning (FLP) for each prepared sample. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured using Keithley 4200 semiconductor parameter analyzer and HP4284 LCR meter. The extraction of capacitance equivalent thickness (CET) values and interface state density (D_{it}) is described in our previous reports.^{12,13}

Figure 1(a) shows XPS spectra in Al 2p binding energy region for as-deposited and HTA ($T_a=800$ °C) HfO₂ samples with Al₂O₃ top layer (Si/HfO₂/Al₂O₃). For both samples, Al 2p peak is observed clearly at 75 eV, indicating the presence of Al₂O₃ top layer. However, the intensity of this peak becomes smaller after HTA at 800 °C. Since XPS peak intensity is inversely proportional to the depth of atoms from the surface, we infer that the Al atoms diffused into the dielectric layer.¹⁴ Similarly, Fig. 1(b) shows the XPS spectra of Ti 2p_{3/2} peak for as-deposited and HTA ($T_a=800$ °C) HfO₂ samples with TiO₂ top layer (Si/HfO₂/TiO₂). Similar to Si/HfO₂/Al₂O₃ sample, the intensity of Ti 2p_{3/2} peak at 460 eV decreased after HTA. Although we could not obtain depth profiles of Al or Ti due to its very small thickness ($\approx 4-5$ nm), these results indicate that the HTA produces indiffusion of Al or Ti into the interface layer between high k and Si. Moreover, the deconvoluted XPS spectra in Fig. 1(b)

^{a)}Electronic mail: hyungjun@yonsei.ac.kr.

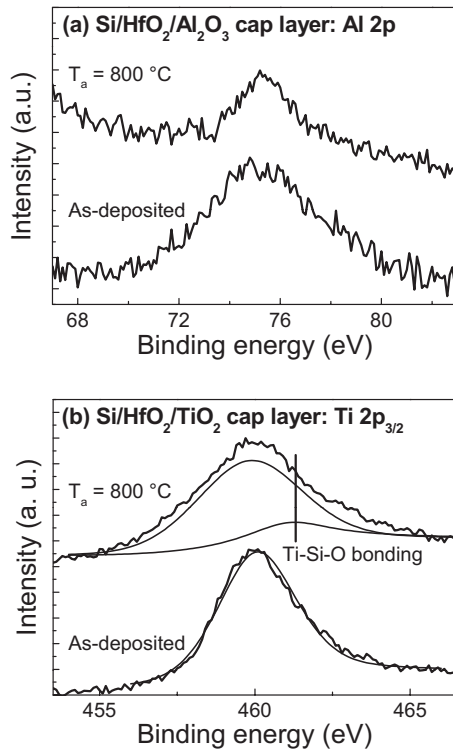


FIG. 1. XPS spectra for as-deposited and HTA ($T_a=800^\circ\text{C}$) HfO_2 samples with Al_2O_3 or TiO_2 capping layer: (a) Al $2p$ and (b) Ti $2p_{3/2}$.

shows the formation of Ti–Si–O bonding, clearly showing the indiffusion of Ti atoms to interface layer.

Figure 2(a) shows C–V curves for a MOS capacitor using HfO_2 as gate dielectric without any inserted layers after PDA and FGA, followed by HTA with varying T_a from 550 to 800 °C. The capacitance value decreases with increasing annealing temperature, due to the interfacial layer formation

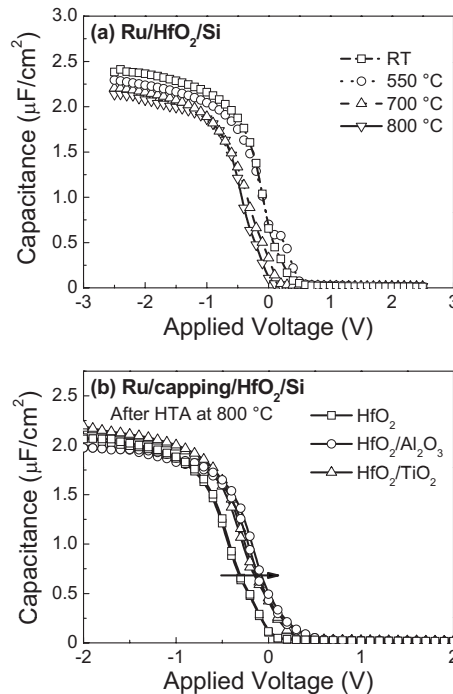


FIG. 2. (a) C–V curves of MOS capacitor with HfO_2 as a gate insulator after HTA from 550 to 800 °C (b) C–V curves of the MOS capacitors with HfO_2 , $\text{HfO}_2/\text{Al}_2\text{O}_3$, and $\text{HfO}_2/\text{TiO}_2$ as a gate insulator after HTA at 800 °C.

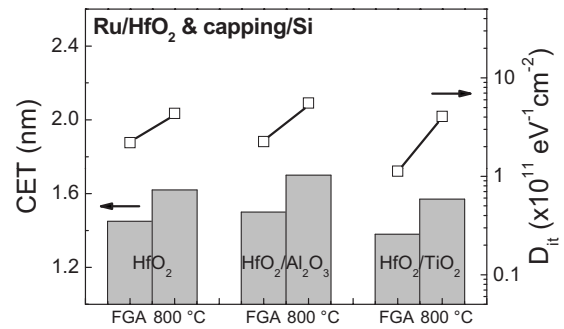


FIG. 3. CETs and D_{it} value of the MOS capacitors with HfO_2 , $\text{HfO}_2/\text{Al}_2\text{O}_3$, and $\text{HfO}_2/\text{TiO}_2$ as a gate insulator after HTA at 800 °C.

at Si/ HfO_2 interface. A shoulder is observed for the sample with $T_a=550^\circ\text{C}$, which is attributed to the formation of interface states originated from Hf diffusion and subsequent interfacial layer mixing.¹⁵ Due to this, the V_{FB} was changed a little bit from 0.02 V to 0.24 eV after HTA at $T_a=550^\circ\text{C}$. However, after HTA at higher temperatures, the V_{FB} shifted to negative direction; -0.14 V at $T_a=700^\circ\text{C}$ and -0.20 V at $T_a=800^\circ\text{C}$. Figure 2(b) shows C–V curves for Si/ HfO_2 (no insertion layer), Si/ $\text{HfO}_2/\text{Al}_2\text{O}_3$, and Si/ $\text{HfO}_2/\text{TiO}_2$ samples after HTA at 800 °C. The MOS capacitors with Al_2O_3 and TiO_2 insertion layers have shown smaller V_{FB} shift (-0.15 and -0.12 eV, respectively) than that without any insertion layer (-0.22 eV), indicating that both Al_2O_3 and TiO_2 insertion layers effectively prevent the V_{th} shift for p–MOS capacitors after HTA process.

Figure 3 shows the CET and D_{it} values before and after HTA at 800 °C for these samples. For all these samples, the CET values increase after HTA, which is due to the formation of interface layer between HfO_2 and Si. Among the three samples, Si/ $\text{HfO}_2/\text{TiO}_2$ has the smallest CET (1.38 and 1.57 nm before and after HTA), compared to the other (1.45 and 1.62 nm before and after HTA for pure HfO_2 and 1.50 and 1.70 nm before and after HTA for Si/ $\text{HfO}_2/\text{Al}_2\text{O}_3$). This is primarily due to larger dielectric constant of TiO_2 (40–80) than that of Al_2O_3 ($k=9$) or HfO_2 ($k=25$).¹ Meanwhile, the D_{it} values were found to increase approximately twice after HTA for HfO_2 and Si/ $\text{HfO}_2/\text{Al}_2\text{O}_3$. Before HTA, the D_{it} values of pure HfO_2 dielectric and $\text{Al}_2\text{O}_3/\text{HfO}_2$ are essentially identical ($\approx 2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$), while that for Si/ $\text{HfO}_2/\text{TiO}_2$ sample was smaller ($\approx 1 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$). This better D_{it} by using TiO_2 insertion layer agrees with a previous report.¹⁶ These results clearly show that although the ability of tuning V_{FB} is almost same for Al_2O_3 and TiO_2 insertion layer, TiO_2 is a better choice due to the benefits in low CET and D_{it} .

Figure 4(a) shows C–V curves for MOS capacitors with HfO_2 gate oxide with top and bottom-inserted TiO_2 layer after HTA at 800 °C. There is only a mere difference in the capacitance depending on the position of inserted TiO_2 layer. However, we observe clear difference in V_{FB} depending on the position of inserted TiO_2 layer. Figure 4(b) shows δV_{FB} ($\delta V_{FB} = V_{FB}$ of $\text{HfO}_2/\text{insertion layer} - V_{FB}$ of HfO_2) for four different samples after HTA at 800 °C. Here, the top-inserted layers of Al_2O_3 and TiO_2 show similar values in terms of δV_{FB} (≈ 150 mV). However, larger δV_{FB} (≈ 250 mV) was achieved when TiO_2 is inserted at the bottom of HfO_2 layer. Thus, we infer that the high- k/Si interfacial layer plays a dominant role in tuning of V_{FB} . In other

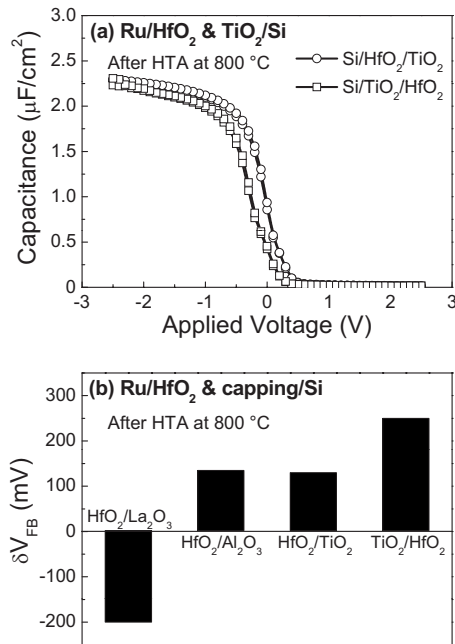


FIG. 4. (a) C-V curves of the MOS capacitors with HfO₂/TiO₂ and TiO₂/HfO₂ as a gate insulator (b) δV_{FB} of the MOS capacitors with HfO₂/La₂O₃, HfO₂/Al₂O₃, HfO₂/TiO₂, and TiO₂/HfO₂ as a gate insulator after HTA at 800 °C.

words, δV_{FB} is highly affected by the formation of an additional dipole layer at the HfO₂/Si interface. When Ti is located at the top of HfO₂, Ti atoms need to diffuse to high k/Si interface forming a dipole layer near the interface of the Si/HfO₂. Thus, the δV_{FB} is larger for bottom inserted TiO₂ layer compared to top-inserted TiO₂ layer. Finally, Fig. 4(b) also shows the result for La₂O₃ insertion layer to verify the polarity of V_{FB} shift, showing a negative shift V_{FB} ($\delta V_{FB} \approx -200$ mV) applicable in the n-FET device as reported previously.^{7,8}

Based upon our current results with the findings in previous reports, we confirm that the primary cause for the V_{FB} tuning by inserted TiO₂ layer is an additional dipole layer formation at high-k/Si interfacial layer. The Ti atoms make Hf–O–Ti and Ti–O–Si configurations at the high-k/Si interface, generating dipole layers.^{10,11} The strength and the direction of dipole vector depend on the electronegativity of the atoms, where the dipole strength has an inversely proportional relationship with electronegativity.¹¹ The electronegativity of Ti is approximately same as that of Al (1.5) which is larger than that of Hf (1.3), and smaller than that of Si (1.8).¹⁷ Thus, the direction of dipole vector is determined toward to the Si substrate because the +Q pole is formed on both Hf and Ti in Hf–O–Ti and Ti–O–Si configurations, respectively. After the dipole formation, the EWF of metal gate increases due to effect of (+) electric field from the interface dipoles, minimizing the FLP effect.

In this study, systematical studies were conducted on the properties of TiO₂ insertion layer to increase the EWF, and

thereby reduce the FLP effect in p-FETs. The results show that the HfO₂-based gate dielectric with inserted TiO₂ layer can move the V_{FB} into (+) direction after HTA process compared to the device that used only HfO₂ as gate oxide without any insertion layers. Considering the amount of V_{FB} shift and CET from the sample with TiO₂ layer inserted at the bottom of HfO₂ gate dielectric, TiO₂ insertion layer can be regarded as a highly promising candidate for suppression of FLP effect in p-FETs with HfO₂ gate dielectrics.

This work was supported by the Technology Innovation Program funded by the Ministry of Knowledge Economy (MKE, Korea, Grant No. 10030519). Also, this work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) and by Nano R&D program and Priority Research Centers Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (Grant Nos. 2009-0083749, 2009-0082853, and 2009-0093823).

¹J. Robertson, *Rep. Prog. Phys.* **69**, 327 (2006).

²C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, and D. Gilmer, *Dig. Tech. Pap. - Symp. VLSI Technol.* **2003**, p. 9–10.

³J. Robertson, O. Sharia, and A. A. Demkov, *Appl. Phys. Lett.* **91**, 132912 (2007).

⁴H. N. Alshareef, H. F. Luan, K. Choi, H. R. Harris, H. C. Wen, M. A. Quevedo-Lopez, P. Majhi, and B. H. Lee, *Appl. Phys. Lett.* **88**, 112114 (2006).

⁵M. Kadoshima, A. Ogawa, H. Ota, K. Iwamoto, M. Takahashi, N. Mise, S. Migita, M. Ikeda, H. Satake, T. Nabatame, and A. Toriumi, *J. Appl. Phys.* **99**, 054506 (2006).

⁶Y. Tsuchiya, M. Yoshiki, J. Koga, A. Nishiyama, M. Koyama, M. Ogawa, and S. Zaima, *IEEE Trans. Electron Devices* **55**, 2648 (2008).

⁷S. Kamiyama, T. Miura, E. Kurosawa, M. Kitajima, M. Ootuka, T. Aoyama, and Y. Nara, *Tech. Dig. - Int. Electron Devices Meet.* **2007**, pp. 539–542.

⁸K. Kakushima, K. Okamoto, M. Adachi, K. Tachi, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, *Solid-State Electron.* **52**, 1280 (2008).

⁹K. Iwamoto, Y. Kamimuta, A. Ogawa, Y. Watanabe, S. Migita, W. Mizubayashi, Y. Morita, M. Takahashi, H. Ota, T. Nabatame, and A. Toriumi, *Appl. Phys. Lett.* **92**, 132907 (2008).

¹⁰Y. Kamimuta, K. Iwamoto, Y. Nunoshige, A. Hirano, W. Mizubayashi, Y. Watanabe, S. Migita, A. Ogawa, H. Ota, T. Nabatame, and A. Toriumi, *Tech. Dig. - Int. Electron Devices Meet.* **2007**, pp. 341–344.

¹¹P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, M. A. Quevedo-Lopez, H. C. Wen, H. Alshareef, K. Choi, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker, H. R. Harris, P. Majhi, R. Choi, P. Lysaght, B. H. Lee, H. H. Tseng, R. Jammy, T. S. Boscke, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, *Appl. Phys. Lett.* **92**, 092901 (2008).

¹²W. J. Maeng and H. Kim, *J. Appl. Phys.* **104**, 064111 (2008).

¹³W. J. Maeng, J. Y. Son, and H. Kim, *J. Electrochem. Soc.* **156**, G33 (2009).

¹⁴F. J. Himpsel, F. R. McFeely, A. Taleb-Ibrahimi, J. A. Yarmoff, and G. Hollinger, *Phys. Rev. B* **38**, 6084 (1988).

¹⁵H. Kim, P. C. McIntyre, and K. C. Saraswat, *Appl. Phys. Lett.* **82**, 106 (2003).

¹⁶S. J. Rhee, C. S. Kang, C. H. Choi, C. Y. Kang, S. Krishnan, M. Zhang, M. S. Akbar, and J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet.* **2004**, pp. 837–840.

¹⁷*Handbook of Condensed Matter and Materials Data* edited by W. Martienssen and H. Warlimont (Springer, Berlin, Heidelberg, 2005).