A $0.1\,\%$ THD, $1\,\mathrm{M}\Omega$ to $1\,\mathrm{G}\Omega$ Tunable, Temperature Compensated Transimpedance Amplifier Using a Multi-Element Pseudo-Resistor

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(Invited Paper)

Abstract— **In this paper, a transimpedance amplifier (TIA) is presented that utilizes a modified pseudo-resistor with improved robustness against temperature and process variations, enhanced linearity, and reduced parasitics. Using a biasing scheme named pseudo current mirror, the conventional dependence on absolute process parameters is reduced to a dependence on matching of alike devices. The linearity and noise performance as well as the immunity against process variations of the presented TIA are improved by the series connection of multiple pseudo-resistor elements. Moreover, it is shown how implementing the design in a silicon-on-insulator (SOI) technology reduces critical parasitics, which in turn enables the use of the multi-element pseudo-resistor in high-speed, high-gain, low-distortion TIAs. A prototype realization in a 180 nm CMOS SOI technology achieves a tunability in transimpedance of three orders of magnitude from 1 GΩ down to 1 MΩ with corresponding bandwidths from 8 kHz to 2 MHz. By design, the contribution of shot noise is rendered negligible and the white noise floor of the prototype realization approaches the theoretical thermal noise limit, e. g., $5.5\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ for a transimpedance of 1 GΩ and $140\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ for 1 MΩ. Total harmonic distortion values of less than $0.1\,\%$ are achieved for an input amplitude of $300\,\mathrm{pA_{p-p}}$ for 1 GΩ, $4.0\,\mathrm{nA_{p-p}}$ for 100 MΩ, $40\,\mathrm{nA_{p-p}}$ for 10 MΩ, and less than $1\,\%$ is achieved for an input amplitude of $550\,\mathrm{nA_{p-p}}$ for 1 MΩ. The presented TIA consumes an area of $0.07\,\mathrm{mm^2}$ and dissipates a power of 9.3 mW for the opamp and a maximum power of 0.2 mW for the pseudo-resistor from a 1.8 V supply.**

Index Terms—**Pseudo-resistor, linearization, robustness, process variation, TIA, current readout**

I. Introduction

TRANSIMPEDANCE amplifiers featuring high gain and high speed are required as high-performance current readouts for state-of-the-art integrated and miniaturized sensor elements in various fields from biomedical to materials science applications [1]–[3]. To improve the timing resolution, in these experiments, the utilized readout should both provide a minimum parasitic capacitance and at the same time a maximum immunity against any existing stray capacitance from the sensor itself. Custom-designed feedback transimpedance amplifiers with small input capacitance and low input impedance meet this demand and are therefore the architecture of choice in all state-of-the-art implementations. Transimpedance tunability is strongly desirable because it maximizes the TIA dynamic range and thereby the potential fields of application.

The bandwidth of a TIA is in general limited by two factors: input capacitance and opamp speed. The input capacitance
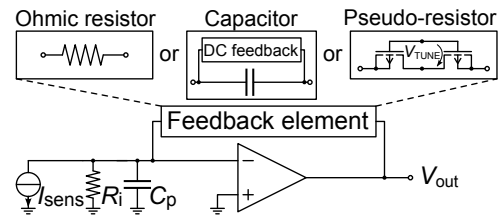

Fig. 1. Illustration of an opamp-based TIA with different possibilities to realize the feedback element.

typically consists of the capacitance of the sensor element and the opamp input capacitance, cf. Fig. 1. In the most common structure, an opamp-based resistive TIA, the large loop gain produces a virtual short across the input capacitance, providing both a low input impedance and a minimized current through the parasitic capacitance at lower frequencies. However, the design of a high-gain, high-speed resistive feedback TIA is complicated by the fact that input capacitance and feedback resistance introduce a second pole in addition to the pole of the opamp, which requires compensation to ensure stability. Moreover, realizing very large resistor values in the feedback path for high-gain TIAs is difficult because large resistor values are associated with large parasitics and the required chip area becomes excessive.

II. State of the Art

A. Transimpedance Amplifiers

Due to the difficulties of realizing resistive high-gain, high-bandwidth TIAs, most state-of-the-art transimpedance amplifiers utilize capacitors as feedback element [4]–[10], which is beneficial in many respects: Most importantly, the capacitive divider formed by the feedback capacitor and the input capacitance renders the feedback ratio β constant vs. frequency and thereby avoids the formation of a second pole. Therefore, stability is much easier achieved and, in general, the trade-off between noise, closed-loop TIA gain, and bandwidth is relaxed. Using this approach, Ferrari *et al.* presented a two-stage TIA with a capacitive feedback first stage, i. e., an integrator, followed by a differentiator second stage to provide an overall flat frequency response [6]–[9]. In [9], they report a transimpedance of 60 MΩ and a bandwidth of 4 MHz. In the Ferrari TIA, in order to achieve high gain and low noise, the feedback capacitance of the first stage is designed

with a very small value of $100\,\mathrm{fF}$. Since the integrator is not capable of processing DC currents due to output saturation, an additional DC feedback loop has been applied, which further increases the complexity of the circuit. The DC feedback has been implemented using pseudo-resistors operated in weak inversion which introduces an undesirable dependence of the noise performance on the DC bias current via the pseudo resistors' shot noise [9]. Moreover, the separate outputs for DC and AC signals require additional complexity in the subsequent signal processing. Finally, the TIA dynamic range is reduced towards low frequencies due to the small feedback capacitance and large low-frequency gain of the integrator. TIAs with resistive feedback can therefore be an advantageous choice for applications in which low complexity and scalability are desirable, e. g., arrays of sensors, and in which the recorded current spans a wide spectral range including DC.

Reflecting the need for high-gain, yet simple TIAs, Chuah and Holburn presented a resistive feedback TIA utilizing a single pseudo-resistor as feedback element [11]. They report a transimpedance of approximately $230\,\mathrm{k\Omega}$ and a bandwidth of $12.5\,\mathrm{MHz}$. The performance of the TIA is, however, very sensitive to process and temperature variations as the single-element pseudo-resistor is operated in weak inversion.

To mitigate these problems, in [12], our group proposed the use of a modified pseudo-resistor with enhanced linearity and robustness as resistive feedback element. The circuit realization presented in [13] displays a tunable measured transimpedance between $1\,\mathrm{M\Omega}$ and $1\,\mathrm{G\Omega}$ with inversely scaling bandwidths between (opamp limited) $2\,\mathrm{MHz}$ and $7\,\mathrm{kHz}$.

B. Pseudo-Resistors

Diode-connected MOS transistors, which are operated at very small drain-source voltages, i. e., in weak inversion, provide very large resistance values and are commonly named pseudo-resistors (PRs). However, MOS transistors in weak inversion feature exponential I/V characteristics [14] and therefore display poor linearity and strong dependence on process and temperature variations. That is why they are most of the time not used in the signal path and/or passband of an amplifier but rather perform auxiliary tasks such as biasing and discharge of DC bias currents, where the nonidealities do not influence the signal in the band of interest [15].

As an extension to conventional, single-device pseudo-resistors, in [16], Tajalli *et al.* presented a very compact pseudo-resistor that is composed of two symmetrically connected PMOS transistors and an NMOS source follower, which provides a tuning voltage to adjust the resistance value. At very small voltages across them, the two PMOS transistors operate in the linear mode. With increasing voltage, one transistor operates in reverse mode and the parasitic source-bulk diode starts to conduct. Therefore, this structure can only accommodate small operating voltages when supposed to operate as a resistor. Furthermore, since an NMOS transistor is used to bias the PMOS devices, there is an inherent strong susceptibility to process variations.

In [17], Shiue *et al.* introduced two additional PMOS transistors to enhance the linearity of the Tajalli structure.

In their design, when the voltage across the PR increases and the parasitic p-n junctions start to conduct, one transistor migrates from the linear to the saturation mode to produce an increased source-drain resistance. With proper sizing of the transistors, the overall voltage-resistance characteristic is mostly linear. However, the presented voltage-resistance characteristics in [17] is not sufficiently linear for many state-of-the-art applications, which often require small harmonic distortion levels in the range of 0.1 to $1\,\%$. In their paper, Shiue *et al.* also present a biasing scheme, which exploits the use of matched PMOS transistors instead of an NMOS device for biasing the pseudo-resistor elements in order to decrease the influence of process variations.

As a different measure to improve linearity, Karasz *et al.* proposed to connect multiple symmetric PR elements in series to reduce the voltage swing across each PR element [18]. Their proposed device has been optimized for a very high resistance value of $20\,\mathrm{G\Omega}$. For the resistance of the total device, a simulated variation over process corners from $10\,\mathrm{G\Omega}$ to $40\,\mathrm{G\Omega}$ has been reported. Tunability is obtained by short-circuiting a programmable number of elements.

The TIA presented by Chuah and Holburn incorporates a single pseudo-resistor in the feedback path [11]. It is operated in the linear mode and tunable by an adjustable gate potential. Simulations over process corners exhibit resistance values from $104\,\mathrm{k\Omega}$ to $40.8\,\mathrm{M\Omega}$. The resistance is reported to drop by $-37\,\%$ with increasing temperature from $10\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$.

In [12], our group proposed to connect multiple Tajalli PR elements in series to form a linearized resistive element for application in an opamp-based TIA. The simulated total harmonic distortion of the 16-element $40\,\mathrm{M\Omega}$ resistor was $0.26\,\%$ for a $0.8\,\mathrm{V_{p-p}}$ output voltage swing. In the same paper, our group introduced a circuit to compensate the influence of process variations, which provides a complete (first order) cancellation of process variations and reduces residual resistance variations to mismatch between alike devices. For the presented $40\,\mathrm{M\Omega}$ device, Monte Carlo simulations predict a residual standard deviation of $\sigma = 1.5\,\mathrm{M\Omega}$ and a mean value of $\mu = 40.4\,\mathrm{M\Omega}$. The corresponding normalized standard deviation is $3.6\,\%$. However, the performance of the manufactured device suffered from parasitic well capacitances of the PR elements.

To minimize these harmful parasitic capacitances, in [13], our group presented a realization of the pseudo-resistor of [12] in a CMOS SOI technology. Additionally, the design of [13] featured a temperature compensation scheme, which achieved a measured variation below $10\,\%$ in transimpedance over a temperature range of $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$. In the paper at hand, we report on an extended modeling and additional measurements of the design presented in [13].

III. Multi-Element Pseudo-Resistor

The proposed pseudo-resistor structure developed in our group has been highly modified compared to a conventional diode-connected MOSFET to meet the stringent requirements regarding linearity and robustness against process and temperature variations imposed by many biomedical and materials science sensing applications. It is based on the PR element
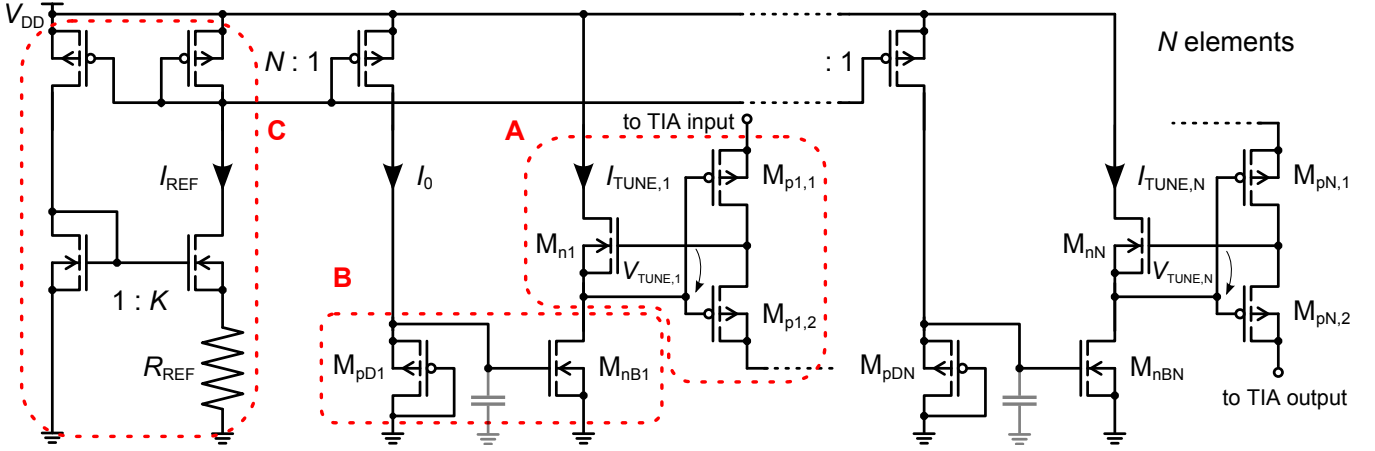
Fig. 2. Schematic of the implemented multi-element pseudo-resistor. A: pseudo-resistor element [16]. B: pseudo current mirror for compensation of process variations [12]. C: PTAT current reference for temperature compensation [13].

introduced by Tajalli, cf. Fig. 2A, and has been advanced by a biasing scheme, which we termed a pseudo current mirror (P-CM), cf. Fig. 2B, to compensate the influence of process variations [12]. The P-CM consists of an NMOS current source that is biased by a PMOS diode in order to eliminate the dependence on absolute process parameters and temperature of the PR. The combination of PR and P-CM makes the resistance of the element purely dependent on matching of alike transistors. Compensation of the residual PTAT temperature behavior has been achieved by biasing using a PTAT current source formed by a weak-inversion-operated beta multiplier, cf. Fig. 2C and [13]. Finally, the linearity can be enhanced by connecting multiple elements in series to form a multi-element pseudo-resistor (MEPR), cf. [12], [13]. In the circuit of Fig. 2, which incorporates all the above mentioned modifications, assuming perfect device matching, the total small signal resistance r_{tot} is independent of temperature and process variations and given by:

$$r_{\mathrm{tot}}\Big|_{V_{\mathrm{RES}}=0} \approx \frac{2N^2}{n\ln(K)}R_{\mathrm{REF}}, \tag{1}$$

where n is the slope factor, N the number of series-connected elements, K the current mirror ratio of the beta-multiplier, and R_{REF} the reference resistor [13].

A. Linearity

Linearization of the feedback resistor I/V characteristic can be achieved by connecting multiple elements in series while keeping the total resistance constant in order to minimize the voltage drop across every element. However, increasing the number of pseudo-resistors in series is eventually limited by the decreasing lowest tolerable TIA output voltage, as can be seen from the following discussion.

The theoretical upper voltage limit of the TIA output is determined by the opamp output stage and therefore eventually by the supply voltage. In contrast, the minimum required TIA output voltage $V_{\mathrm{out,min}}$ is determined by the biasing structure of the MEPR and especially of its Nth element, which is connected to the TIA output. More specifically, the saturation voltage of the current source transistor $V_{\mathrm{DSsat,M_{nBN}}}$ together

with the tuning voltage $V_{\mathrm{TUNE,N}}$ and the (typically very small) voltage drop $V_{\mathrm{DS,M_{pN,2}}}$ over $\mathrm{M_{pN,2}}$ define $V_{\mathrm{out,min}}$ according to:

$$V_{\mathrm{out,min}} = V_{\mathrm{DSsat,M_{nBN}}} + V_{\mathrm{TUNE,N}} - V_{\mathrm{DS,M_{pN,2}}} \tag{2}$$

In normal operation, $V_{\mathrm{TUNE,N}}$ is the dominant term in Eq. (2). However, if the output voltage falls below $V_{\mathrm{out,min}}$, the current source transistor $\mathrm{M_{nBN}}$ enters the linear mode, which leads to a decrease in tuning current and therefore a decrease in tuning voltage. If the output voltage further decreases, $V_{\mathrm{TUNE,N}}$ is eventually cut off. Thereby, output voltages below $V_{\mathrm{out,min}}$ lead to strong (signal-dependent, i. e., nonlinear) increase in the resistance of the PMOS transistor pair $\mathrm{M_{pN,1,2}}$. Since the MEPR is used in the feedback around the opamp, for a given input current, the TIA output voltage follows the value of the overall feedback resistance. Therefore, if the input signal causes the TIA's output voltage V_{out} to fall below $V_{\mathrm{out,min}}$, the feedback resistance increases strongly, which results in an abrupt breakdown of V_{out}.

Consequently, the lower limit of the TIA output voltage depends on the tuning current $I_{\mathrm{TUNE,N}}$ used in the bias network, via the voltages $V_{\mathrm{TUNE,N}}$ and $V_{\mathrm{DSsat,M_{nBN}}}$. Here, a large tuning current $I_{\mathrm{TUNE,N}}$, which results in large values of $V_{\mathrm{TUNE,N}}$ and $V_{\mathrm{DSsat,M_{nBN}}}$, results in an increased minimum required output voltage. Since in order to decrease the overall transimpedance value, the tuning current needs to be increased by decreasing R_{REF}, cf. Eq. (1), the minimum achievable resistance value is determined by the maximum bias current I_{TUNE}, which can be applied before the transition from weak to moderate inversion of the pseudo-resistor devices takes place. This is because in moderate or even strong inversion, the relatively large values of $V_{\mathrm{TUNE,N}}$ and $V_{\mathrm{DSsat,M_{nBN}}}$ lead to prohibitively large values of $V_{\mathrm{out,min}}$.

While the above consideration already applies to a single PR element, the same mechanism eventually also limits the number of PR elements which can be connected in series, introducing a trade-off between achievable linearity and maximum TIA output swing for MEPRs. This is because, on the one hand, an increase of series-connected elements linearizes the I/V characteristic but, on the other hand, it also results in an increased tuning current per unit element (to produce
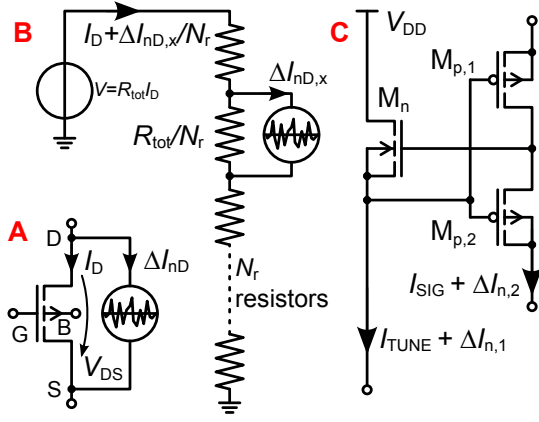
Fig. 3. Noise models. A: MOS transistor with additive noise source. B.: Resistor chain with N_r elements and one exemplary noise source. C: PR element for modeling the noise contribution of the bias network

a smaller unit element resistance) if the overall resistance has to stay constant. Therefore, the lower limit of the usable TIA output voltage range increases with the number of series-connected elements in the MEPR. This increase is typically logarithmical as long as all transistors are operated in weak inversion. Furthermore, an increased tuning current results in an increased influence of channel length modulation of the respective NMOS transistors. Channel length modulation results in a small signal-dependent variation of the tuning voltage, which results in a small curvature of the I/V characteristic of the MEPR and therefore in an eventually increased harmonic distortion.

In a systematic design of an MEPR-based TIA, the trade-off between achievable transimpedance value (signal swing) and linearity (number of elements) explained above has to be taken into account to guide the selection of the optimum number of series-connected PR elements. As an example, simulation results presented in [12] show a good compromise between linearity and signal swing for 16 elements.

B. Noise

1) Thermal Noise of the PR: The noise of a transistor with a drain current I_D can be modeled with an additive noise current ΔI_nD, as shown in Fig. 3A. According to the EKV model [14], for a long channel device, the corresponding (white) noise power spectral density (PSD) is given by:

$$S_{\Delta \mathrm{I}_\mathrm{nD}^2} = 4kT G_\mathrm{nD}, \tag{3}$$

where k is Boltzmann's constant, T is absolute temperature, and G_nD the channel noise conductance. At $V_\mathrm{DS} = 0$, the noise conductance G_nD equals the drain-source channel conductance G_ds0, cf. [14], which equals the inverse channel resistance R_ds0:

$$G_\mathrm{nD}\Big|_{V_\mathrm{DS}=0} = G_\mathrm{ds0} = \frac{1}{R_\mathrm{ds0}}. \tag{4}$$

In the linear mode of operation (i.e., for small values of V_DS), the small signal resistance value of the PR, R_px, equals its (noisy) large signal channel resistance and, therefore, the

thermal noise of a long channel PR operated in the linear mode is given by:

$$S_{\Delta \mathrm{I}_\mathrm{nD}^2}\Big|_{V_\mathrm{DS}=0} = \frac{4kT}{R_\mathrm{ds0}} = \frac{4kT}{R_\mathrm{px}}. \tag{5}$$

Consequently, the equivalent input referred noise floor of a TIA with a transimpedance of R_TIA produced by a PR in the linear mode can be written as:

$$S_{\Delta \mathrm{I}_\mathrm{n,eq,min}^2}\Big|_{I_\mathrm{in}=0} = \frac{4kT}{R_\mathrm{TIA}} \tag{6}$$

2) Contribution of Shot Noise: For a very small drain-source voltage and hence operation in the linear mode, the noise of the PR is dominated by the above-described thermal noise of the drain-source resistance. However, when the drain current increases and the pseudo-resistors approach saturation, the noise starts to be shot noise dominated as the conduction mechanism of long channel transistors in weak inversion is dominated by diffusion. According to [14], the noise of a transistor operated in weak inversion and saturation, carrying a drain current I_D, can be described as:

$$S_{\Delta \mathrm{I}_\mathrm{nD}^2} = 2q I_\mathrm{D}, \tag{7}$$

with the elementary charge q. Therefore, for a given pseudo-resistor geometry, the PR increasingly suffers from shot noise as the drain current is enlarged. In the following, it is shown that due to its working principle and in contrast to single-element PRs, the MEPR displays some immunity against the increased shot noise floor.

Fig. 3B shows a model of a resistor chain of N_r elements with a total resistance R_tot (i.e., a resistance of $R_\mathrm{tot}/N_\mathrm{r}$ for each element) biased with a current I_D, and one exemplary additive noise source $\Delta I_\mathrm{nD,x}$ at one of the PRs. For the following discussion, it should be noted that there are $N_\mathrm{r} = 2N$ PMOS transistors in an N-element MEPR. The equivalent input noise current contributed by that single noise source is given by:

$$\Delta I_\mathrm{n,eq,x} = \frac{\Delta I_\mathrm{nD,x} R_\mathrm{tot}/N_\mathrm{r}}{R_\mathrm{tot}} = \frac{\Delta I_\mathrm{nD,x}}{N_\mathrm{r}}, \tag{8}$$

due to the current divider structure of the PR network with a current division factor N_r. Hence, the equivalent input noise PSD contributed by that noise source is divided by N_r^2:

$$S_{\Delta \mathrm{I}_\mathrm{n,eq,x}^2} = \frac{S_{\Delta \mathrm{I}_\mathrm{nD,x}^2}}{N_\mathrm{r}^2}. \tag{9}$$

Then, assuming that all N_r noise sources are independent and identically distributed (iid sources), the total input-referred current noise PSD becomes:

$$S_{\Delta \mathrm{I}_\mathrm{n,eq,tot}^2} = \sum_{x=1}^{N_\mathrm{r}} S_{\Delta \mathrm{I}_\mathrm{n,eq,x}^2} = \sum_{x=1}^{N_\mathrm{r}} \frac{S_{\Delta \mathrm{I}_\mathrm{nD,x}^2}}{N_\mathrm{r}^2} = \frac{S_{\Delta \mathrm{I}_\mathrm{nD,x}^2}}{N_\mathrm{r}}. \tag{10}$$

Taking a closer look at Eq. (10), we find the intuitive result that for the thermal noise produced by a resistor chain, where each individual element contributes a resistance of $R = R_\mathrm{tot}/N_\mathrm{r}$ to the total resistance value R_tot and therefore has an element noise PSD of $S_{\Delta \mathrm{I}_\mathrm{nD,x}^2} = \frac{4kT}{R_\mathrm{tot}/N_\mathrm{r}}$, the total noise produced by the chain equals the thermal noise produced by a resistor of value R_tot, i.e.,

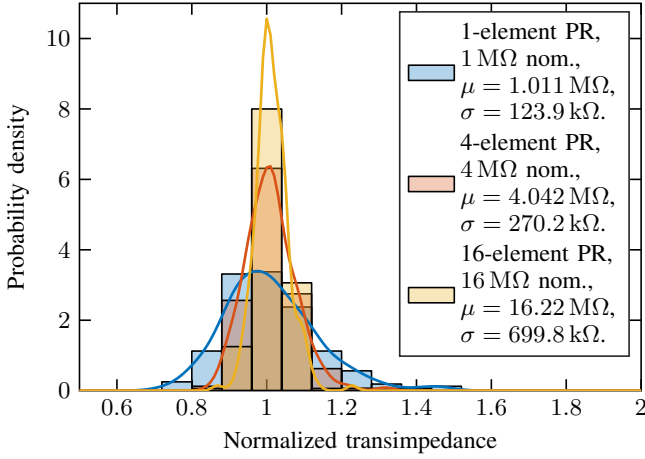$$S_{\Delta \mathrm{I}_\mathrm{n,eq,tot}^2} = \frac{4kT}{R_\mathrm{tot}}. \tag{11}$$

Fig. 4. Kernel density estimations and density-normalized histograms with 0.08 bin width of nominal-value-normalized 200-point-Monte-Carlo simulation results of a 1. 1 MΩ single pseudo-resistor (PR) element with pseudo current mirror (P-CM), 2. 4 MΩ resistor with 4 series-connected 1 MΩ PR elements with P-CM., and 3. 16 MΩ 16-element PR with P-CM.
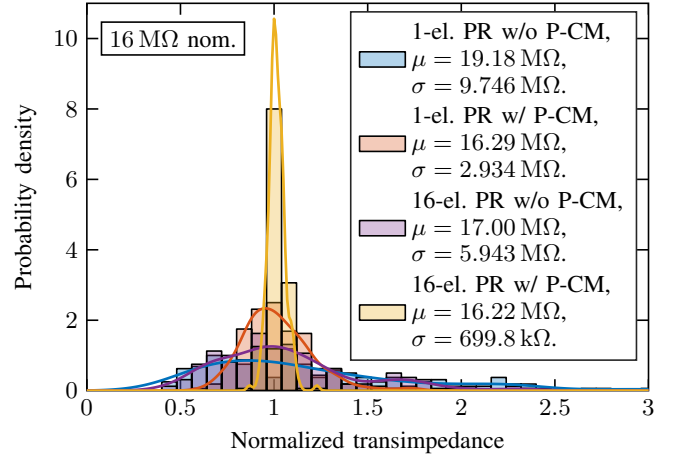

Fig. 5. Kernel density estimations and density-normalized histograms with 0.08 bin width of nominal-value-normalized 200-point-Monte-Carlo simulation results of a: 1. 16 MΩ single-element PR without P-CM, 2. 16 MΩ single-element PR with P-CM, 3. 16 MΩ 16-element PR without P-CM, and 4. 16 MΩ 16-element PR with P-CM.

However, when considering the shot noise produced by the PRs, i.e., assuming $S_{\Delta I^2_{nD,x}} = 2qI_D$, cf. Eq. (7), the total input-referred noise current PSD becomes:

$$S_{\Delta I^2_{n,eq,tot}} = \frac{2qI_D}{N_r}, \tag{12}$$

and the corresponding input noise current is therefore:

$$\Delta I_{n,eq,tot} = \frac{\sqrt{2qI_D}}{\sqrt{N_r}} \tag{13}$$

Thus, when sensing a current with a DC component of I_D and implementing the TIA feedback resistance with shot-noise limited PRs, it is beneficial to realize the total feedback resistance using a number of scaled down PRs connected in series because then, the total shot noise contribution is reduced according to Eq. (13). The proposed MEPR topology exploits this fact by increasing the number of unit elements while keeping the total feedback resistance constant up to the point where the shot noise contribution becomes negligible compared to the thermal noise produced by the PRs. In this way, the MEPR noise can always be made thermal noise limited, simply by placing a sufficient number of elements in series. This is beneficial especially for larger bias currents, where single-element PRs are frequently shot noise limited, i.e., produce noise which is larger than that of an ohmic resistor of equal resistance value.

3) Noise Contribution of Biasing Network: In addition to the pseudo-resistor elements themselves, also the biasing circuitry contributes to the total noise. To quantify this effect, we can consider the single PR element of Fig. 3B with its tuning current I_{TUNE} in the NMOS and the signal current I_{SIG} in the PMOS branch. Then, assuming all transistors to be noise-free and a noise current $\Delta I_{n,1}$ to be flowing in the NMOS branch, this noise current will be mirrored into the signal path via the ratio of the transconductances of the respective PMOS and NMOS devices according to:

$$S_{\Delta I^2_{n,2}} = \frac{G^2_{m,p}}{G^2_{m,n}} S_{\Delta I^2_{n,1}}. \tag{14}$$

As long as the transconductance of the NMOS transistor, $G_{m,n}$, is larger than the transconductance of the PMOS, $G_{m,p}$, the noise originating from the biasing circuitry is suppressed, cf. Eq. (14). This is the case if $I_{TUNE} > I_{SIG}$. Hence, an increase of the number of series-connected PR elements is beneficial for noise suppression due to increased tuning current associated with the smaller unit element resistor values.

C. Cancellation of Process Variation

The pseudo-resistor proposed by Tajalli incorporates a PMOS transistor pair biased by the gate-source voltage of an NMOS source follower. All devices are operated in weak inversion. The resistance value of this structure is very sensitive to process variations since the small signal resistance exponentially depends on absolute process parameters such as the devices' threshold voltages. Furthermore, PMOS and NMOS devices cannot be matched well because their characteristics are defined in separate process steps. The pseudo current mirror solves this problem by using an NMOS current source, which in turn is biased by a diode-connected PMOS device to provide the tuning current for the PR. The process dependence of the tuning current therefore produces a (first order) cancellation of the PR process dependence. Then, the residual resistance variations purely depend on the matching of alike transistor types, i.e., PMOS to PMOS and NMOS to NMOS, which is well under control. This residual influence of matching on the resistance value is however exponential with respect to threshold voltage mismatch [12]. Fortunately, the series connection of multiple elements decreases the influence of mismatch by averaging and the residual variation of the resistance decreases with increasing number of elements. Monte-Carlo Simulation results with 200 points, which clearly illustrate this effect, are presented in Fig. 4 and Fig. 5. Fig. 4 shows the effect of mismatch-averaging for a constant nominal element resistance, whereas Fig. 5 illustrates how, for a fixed nominal overall resistance, biasing the PR with the P-CM improves robustness.
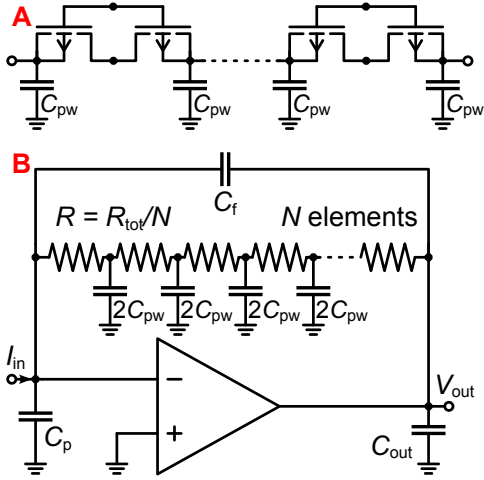
Fig. 6. A: TIA model using an RC-ladder network instead of a simple resistor as feedback element to account for the relevant parasitic capacitances of the MEPR structure. B: PR chain including the most relevant parasitic well capacitances.

IV. Well Capacitances in MEPR

To be able to properly predict the performance of a high-speed TIA using an MEPR as resistive feedback element, the parasitic capacitances of the MEPR need to be considered. Here, especially the capacitance of each PR element towards ground can have a significant influence on the performance. It is these parasitic capacitances that are typically preventing the use of resistive feedback elements in very high gain TIA applications. One of the most critical capacitances is the well capacitance C_{pw} of the PMOS pseudo-resistors from the (deep) n-well to the substrate. Other capacitances, which originate, e. g., from wiring can also contribute to the total capacitance but, fortunately, can typically be modeled in the same way as said well capacitance. The multi-element resistor chain in combination with the well capacitances C_{pw} forms an RC-ladder network, cf. Fig. 6A. Because of the symmetry of the pseudo-resistor structure, the two capacitances C_{pw} of the individual PMOS transistors sum up to a total capacitance of $2C_{pw}$ at the connection node between two elements.

An N-element RC-ladder network with equally dimensioned resistors and capacitors features an Nth-order low-pass characteristic with smooth roll-off and low quality factor. Such an RC-ladder network applied in the feedback loop of an opamp can critically reduce the available phase margin and thereby degrade the dynamic performance or even endanger stability. Fig. 6B shows a model of a TIA, in which the simple feedback resistor is replaced by an RC-ladder network. The additional maximum phase shift introduced by the $2N$ well capacitances of an N-element pseudo-resistor is $90° \times (N-1)$ because the well capacitances of the first and last transistor simply add to the existing (typically larger) input and output capacitances of the TIA.

Using the model of Fig. 6B, we have performed Spectre simulations, which clearly demonstrate the detrimental effect of excessive well capacitance on the TIA performance. For these simulations we have used an example MEPR realization consisting of 16 unit elements of size $1\,\text{M}\Omega$, summing to a
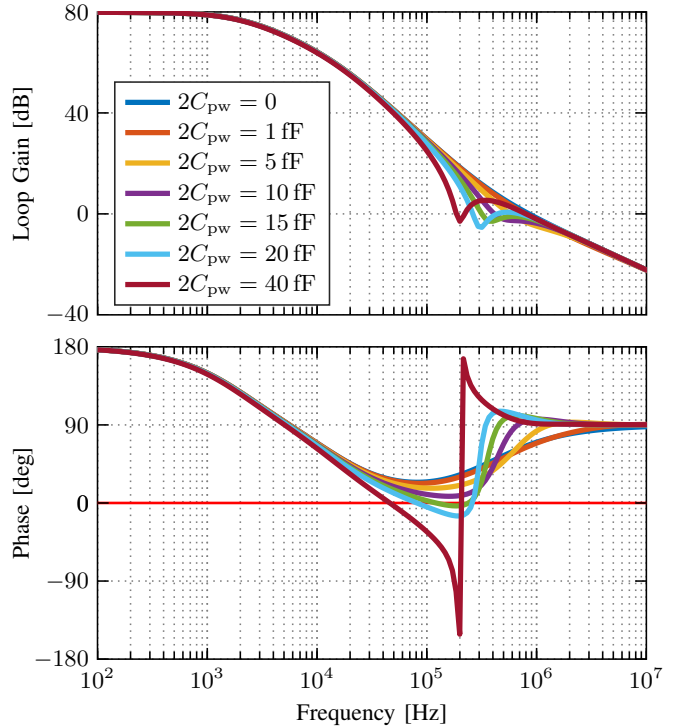

Fig. 7. Simulated loop gain of the TIA model of Fig. 6B using 16 resistive elements and 15 capacitances $2C_{pw}$ of various values

total feedback resistance of $R_{tot} = 16\,\text{M}\Omega$. The value of the well capacitance $2C_{pw}$ was swept over a realistic range from 0 to $40\,\text{fF}$. The combination of TIA input and sensor capacitance was modeled as $C_p = 5\,\text{pF}$ and the output capacitance was not considered because an opamp model with an ideal output stage ($R_{out} = 0\,\Omega$) was used for the simulations. These values were chosen to closely resemble the TIA realization of [13]. The opamp itself is modeled as a single-pole system with a DC-gain of $80\,\text{dB}$ and a gain-bandwidth product of $150\,\text{MHz}$. In order to compensate the second pole introduced by the input capacitance, a zero is introduced by the feedback capacitance C_f. With a value of $C_f = 26\,\text{fF}$, a closed-loop transfer function with second-order Butterworth low-pass characteristic and a corner frequency of $529\,\text{kHz}$ was designed. This configuration achieves the best compromise between speed and peaking of the closed-loop frequency response but, as will be shown next, is quite susceptible to performance degradations due to parasitic well capacitances.

As can be seen from the simulated loop gain and phase response in Fig. 7, the closed-loop feedback system already becomes unstable for well capacitances around $2C_{pw} = 10\,\text{fF}$. Here, it should be noted that the feedback capacitance C_f is primarily used to compensate the second pole introduced by the parasitic input capacitance C_p. However, to a certain extend, it also compensates the phase shift introduced by the well capacitances. A general estimate of how large C_{pw} can become before the onset of intolerable performance degradations is hard to obtain because it depends on a number of factors including the required TIA bandwidth, the number of PR elements and the required total TIA feedback resistance. Here, high-gain, high-bandwidth TIA realizations are most
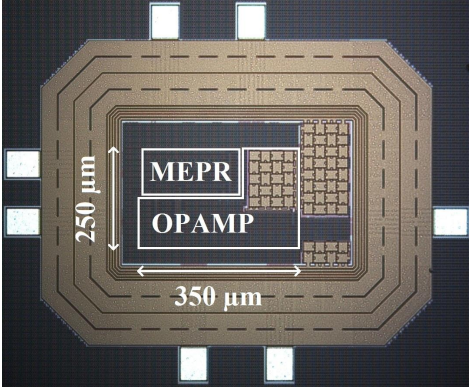
Fig. 8. Die micrograph.

susceptible to this effect and reducing the number of MEPR elements can mitigate the problem. However, as discussed above, reducing the number of MEPR elements can have detrimental effects on the TIA noise and linearity performance.

V. Realization and Measurements

A. Implementation and Realization

The presented TIA has been manufactured in a 180 nm SOI CMOS process to greatly reduce well capacitances compared to bulk CMOS and thereby enable the design of pseudo-resistor-based high-gain, high-bandwidth TIAs. The MEPR has been implemented using 16 elements. The input capacitance of the TIA is $C_p \approx 5$ pF and comprises the capacitances of the input transistors, wiring both on the chip and the PCB, and bonding pads. The opamp is a two-stage Miller design with a gain-bandwidth product of 150 MHz. Here, it should be stressed that the gain-bandwidth product needs to be chosen sufficiently large in order to suppress the influence of the input capacitance. The compensation capacitance implemented on chip is $C_f \approx 15$ fF, which is increased by stray capacitance to $C_{f,tot} \approx 20$ fF. The circuit is supplied from 1.8 V, which results in a total power consumption of 9.3 mW of the opamp and up to 0.2 mW from the MEPR at the minimum resistance of 1 MΩ. Fig. 9 shows the measured frequency responses for transimpedance values of 1 MΩ, 10 MΩ, 100 MΩ, and 1 GΩ. Corner frequencies of approximately 2 MHz, 700 kHz, 80 kHz, and 8 kHz are achieved for the respective transimpedances.

The presented design also incorporates a temperature compensation scheme, which achieves temperature coefficients of 600 ppm/K at 1 MΩ and −900 ppm/K at 10 MΩ and 100 MΩ over a temperature range from −40 °C to 125 °C, cf. [13].

The presented TIA consumes 200 μm x 350 μm of chip area of which the MEPR consumes only 80 μm x 200 μm including compensation capacitance, noise-filtering capacitances, blank switch, and dummy structures.

B. Noise Measurements

Fig. 9 shows the input referred current noise of the TIA for transimpedance values of 1 MΩ, 10 MΩ, 100 MΩ, and 1 GΩ. Each noise curve has been recorded by measuring the output
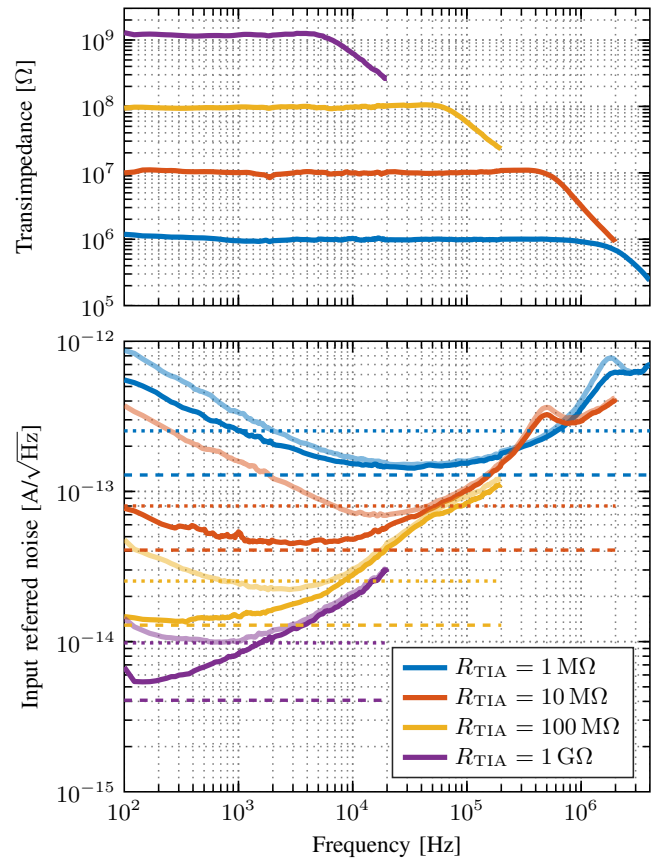

Fig. 9. Upper graph: measured frequency responses of the presented TIA for various transimpedances. An additional feedback capacitance of 100 fF was used to avoid peaking for the 1 MΩ case. Lower graph: measured input referred noise of the presented TIA. Solid lines: input referred noise for $I_{in} = 0$ A. Transparent lines: measured input referred noise at DC input currents of $I_{in} = 200$ nA (1 MΩ), 20 nA (10 MΩ), 2.0 nA (100 MΩ), and 300 pA (1 GΩ). Dashed lines: thermal noise of equivalent ohmic resistors. Dotted lines: theoretical shot noise at an equal current of $I_D = I_{in}$, cf. Eq. (7).

voltage noise and dividing by the measured TIA transimpedance. In order to verify the analysis of Sec. III-B, the measurements have been performed at zero input current (solid lines) and non-zero DC input currents of $I_{in} = 200$ nA (1 MΩ), 20 nA (10 MΩ), 2.0 nA (100 MΩ), and 300 pA (1 GΩ) (transparent lines). In Sec. III-B, it was shown theoretically that the MEPR features reduced shot noise floor compared to a single-device PR and that its minimum noise should be equivalent to the noise of an ohmic resistor. The corresponding noise levels for thermal noise (dashed lines), cf. Eq. (6), and shot noise for the corresponding currents (dotted lines), cf. Eq. (7), are therefore also indicated in Fig. 9.

For zero input current (solid lines), the minimum input referred noise of the TIA approaches the theoretical thermal noise limit. The input referred noise increases towards higher frequencies due to opamp noise, which is high pass shaped due to the input capacitance [13]. For the non-zero DC input currents, the noise increases with current especially at low frequencies due to the influence of the flicker noise of the pseudo-resistors and the biasing network. However, as it is observable in particular in the 1 MΩ measurement, the noise floor only marginally increases for the non-zero DC currents and is still far from reaching the theoretical shot noise value
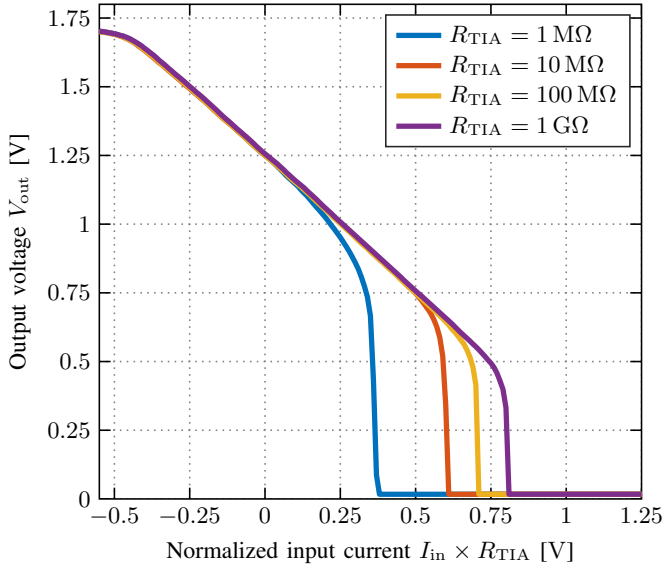
Fig. 10. I/V characteristics of the TIA for various transimpedances. The input current is normalized to obtain comparable curves. The reference voltage V_{ref} is 1.25 V. The upper limit of TIA output voltage is determined by the opamp (supply voltage), the lower limit is determined by the biasing of the MEPR.

Fig. 11. Total harmonic distortion (THD) for sinusoidal input currents up to $1.6\,u A_{p-p}$, $160\,n A_{p-p}$, $16\,n A_{p-p}$, and $1.6\,n A_{p-p}$ and a frequency of $1\,kHz$ for the corresponding transimpedance values of $1\,M\Omega$, $10\,M\Omega$, $100\,M\Omega$, and $1\,G\Omega$. The input current is normalized to the transimpedance to obtain comparable curves. The reference voltage V_{ref} has been adjusted to achieve maximum TIA output signal swing as the lower limit is dependent on the transimpedance value.

corresponding to that current. Thus, an experimental validation of the proposed shot noise reduction by the MEPR structure is given. Noise-wise, the proposed MEPR structure therefore behaves much more like an ohmic resistor, i. e., displaying a current independent minimum noise, than a single-element PR.

C. Linearity Measurements

Fig. 10 shows the measured I/V characteristics of the presented TIA for several transimpedance values. Between the two voltage limits, the curves display a linear behavior. It is clearly observable that the lower limit of usable output swing is dependent on the transimpedance value. It varies from approximately 0.50 V to 0.75 V inversely over the two decades of resistance from $10\,M\Omega$ to $1\,G\Omega$. Within this range, $V_{DSsat,M_{nBN}}$ is typically small and V_{TUNE} is logarithmically dependent on the tuning current as all transistors are operated in weak inversion. However, for $1\,M\Omega$, the lower linear output limit is further increased to more than 1.0 V. The necessary large tuning current required to set this transimpedance value causes transistors M_{nBN} and M_{nN} to enter moderate inversion. This leads to exceeding tuning and saturation voltages, which together drastically increase the lower limit of the linear output voltage range.

Fig. 11 shows the measured total harmonic distortion (THD) of the TIA's output voltage over the normalized (with respect to the transimpedance value) input current amplitude. The input ranges over which the THD stays below 1 % are $1\,n A_{p-p}$ for $1\,G\Omega$, $10\,n A_{p-p}$ for $100\,M\Omega$, approximately $100\,n A_{p-p}$ for $10\,M\Omega$, and $500\,n A_{p-p}$ for $1\,M\Omega$. Here, the THD is significantly higher for the $1\,M\Omega$ case due to the large tuning current which results in increased influences of channel length modulation and the onset of moderate inversion. Nevertheless, the low THD of the presented TIA shows that the principle
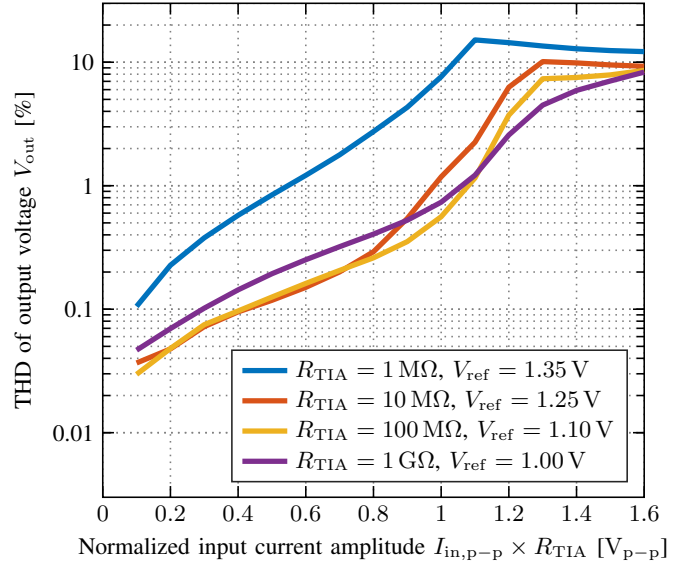
of connecting multiple elements in series makes the MEPR suitable for high-accuracy current readout applications.

VI. CONCLUSION

A transimpedance amplifier utilizing a modified multiple-element pseudo-resistor (MEPR) has been presented and analyzed in depth in this paper. Techniques to reduce the influence of temperature and process variation have been discussed and implemented in silicon. Importantly, significant improvements in the measured linearity of the transimpedance characteristic compared to a single-element pseudo-resistor have been achieved by connecting multiple pseudo-resistor elements in series. Moreover, it was theoretically predicted and demonstrated in measurements that the proposed MEPR structure successfully suppresses the bias dependent shot noise of the pseudo-resistor elements and that the proposed MEPR approaches the theoretical noise limit of an ohmic resistor. The realization of the TIA in a 180 nm SOI CMOS process clearly demonstrates that the working principle of the MEPR together with the reduced parasitics of the SOI technology render the approach of using resistive, MEPR-based feedback TIAs a viable approach for the design of low-noise, high-gain, and high-bandwidth TIAs for advanced state-of-the-art sensing applications.

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