Total-Ionizing Dose Effects on Charge Transfer Efficiency and Image Lag in Pinned Photodiode CMOS Image Sensors

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***Abstract*— The total-ionizing dose (TID) effects on image lag in pinned photodiode CMOS image sensors are investigated thanks to various device variants in order to isolate the major radiation-induced effects on the charge transfer. It is shown that the main cause of the charge transfer degradation is the radiation-induced defects generation in the premetal dielectric (PMD) and in the transfer gate (TG) spacer vicinity which modifies the potential diagram at the photodiode/TG interface by the creation of a potential pocket retaining the electrons that are not transferred. For 0.1 kGy(SiO_2) < TID < 5 kGy(SiO_2), the potential pocket degrades the pixel which exhibits very good lag performances, whereas it improves the high lag pixels by creating a speed-up implant enhancing the electron transfer or by reducing the spillback. For TID > 5 kGy(SiO_2), the defects generated in the PMD influence the whole photodiode potential inducing a pinning voltage increase and degrading the charge transfer by enlarging the potential pocket effect which becomes the main image lag source. The reported results clarify the impact of ionizing radiation on the charge transfer, suggesting radiation hardened by design solutions for future space or nuclear applications.**

***Index Terms*— Charge transfer, CMOS image sensors (CIS), image lag, pinned photodiode (PPD), radiation effects, total-ionizing dose (TID), transfer gate (TG).**

I. Introduction

PINNED photodiodes (PPD) CMOS image sensors (CIS) are today the main solid-state image sensor technology and they are widely used for the development of various scientific applications, thanks to their high performances, high integration capabilities, and low-power consumption [1]. Nowadays, the demand for these sensors is growing, notably for applications in harsh environments, such as space remote sensing and medical imaging where the total-ionizing dose (TID) can goes up to several kGy, but also such as viewing applications in nuclear environments (e.g., waste repository and ITER) for which the TID reach the MGy range.

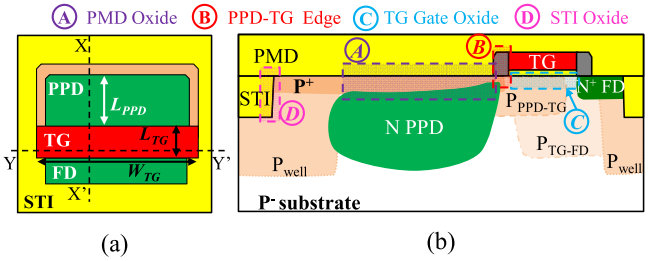

Fig. 1. (a) Top view and (b) X–X′ cross-sectional view of a 4T-PPD together with the possible TID degradation sources. PPD = photodiode; TG = transfer gate; FD = floating diffusion; STI = shallow trench isolation; PMD = premetal dielectric; P_{PPD-TG} = PPD-TG P-doped region; and P_{TG-FD} = TG-FD P-doped region.

The main ionizing radiation effect that degrades the PPD performances is the generation of different defects (i.e., positive-trapped charges and interface states) in the oxides within the pixel structure (see Fig. 1). Several TID degradation source locations, presented in Fig. 1(b), are proposed in the literature: the premetal dielectric (PMD) on top of the PPD (source A) [2], the PPD-transfer gate (TG) edge (PMD/TG spacer), source B, [3], the gate oxide (source C) [2], [4], and the shallow trench isolation (STI) around the PPD [4], [5], and the TG (source D). During ionizing irradiation, the most degraded parameter in CIS is the dark current which increases because of the generated interface states at the Si/SiO_2 interfaces [2], [3]. However, other parameters deteriorate under irradiation exposure. The charge transfer in PPD CIS can be enhanced or degraded (depending on the limiting lag causes in the nonirradiated device) by the TID-induced-trapped positive charges in the TG spacer vicinity [3], [6]. Moreover, the positive-trapped charges and interface states in the PMD lead to an increase of the pinning voltage, whereas the TID-induced-trapped charges in the TG STI sidewalls generate a TG subthreshold leakage leading to full well capacity (FWC) reduction [3]. In order to achieve good performances for the different applications in harsh environments it is then mandatory to improve our understanding of the TID-induced

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TABLE I

SUMMARY OF THE PIXEL DESIGNS INVESTIGATED

	L_{PPD} (µm)	W_{TG} (µm)	L_{TG} (µm)	P_{PPD-TG}*	P_{TG-FD}**
Pixel 1	2	2.7	0.7	Yes	Yes
Pixel 2	0.3	2.7	0.7	Yes	Yes
Pixel 3	4	2.7	0.7	Yes	Yes
Pixel 4	2	1.1	0.7	Yes	Yes
Pixel 5	2	2.7	1.4	Yes	Yes
Pixel 6	2	2.7	2.1	Yes	Yes
Pixel 7	2	2.7	2.7	Yes	Yes
Pixel 8	2	2.7	0.7	No	Yes
Pixel 9	2	2.7	0.7	Yes	No
Pixel 10	2	2.7	0.7	No	No

*P_{PPD-TG}: PPD-TG P doped implant
**P_{TG-FD}: TG-FD P doped implant

damages with the aim to develop radiation resistant CIS able to withstand the environmental constraints.

In this paper, the radiation-induced effects on the charge transfer process are investigated in 4T-PPD pixels up to 20 kGy(SiO_2) (2 Mrad). The response of different pixels which differ from their layouts (i.e., PPD and TG dimensions) as well as the influence of the TG channel doping is investigated in order to explain the contribution of the diverse radiation degradation sources in the charge transfer. The aim is to enlighten the PPD behavior under radiation and to identify possible radiation hardened by design (RHBD) solutions.

II. MATERIALS AND METHODS

The investigated CIS, constituted of 256 × 256 −7-μm-pitch 4T-PPD pixels [see cross section in Fig. 1(b)], has been designed and manufactured by using a mature 0.18-μm CIS technology. The sensor is divided in different subarrays each one being constituted of about 2500 identical pixels.

Each pixel is composed by three main components illustrated in Fig. 1: the PPD where the charges are collected, the TG transistor, which allows the electrons transfer, and the floating diffusion (FD), the N+ doped region where the electrons are transferred by the TG and, then, readout. Three other transistors are also present in each pixel to reset the FD, amplify the signal and select the pixel [7]. The studied subarrays are composed by pixel variants differing from the reference one (which design is reported in Fig. 1) by their doping profiles under the TG and by design layouts, i.e., different TG lengths, TG widths, or PPD sizes. A summary of the pixel variants is reported in Table I.

As observed in [2] to irradiate with bias applied does not lead to enhanced radiation degradations when dealing with CIS performances (dark current, pinning voltage changes, and image lag degradation) for the studied technologies. Since the CIS studied in this paper is fabricated with the same technology as one of those in [2], the circuits were exposed grounded up to TIDs from 3 Gy(SiO_2) to 20 kGy(SiO_2). The dose rate was 1 Gy(SiO_2)/s for TID from 3 Gy(SiO_2) to 1 kGy(SiO2),

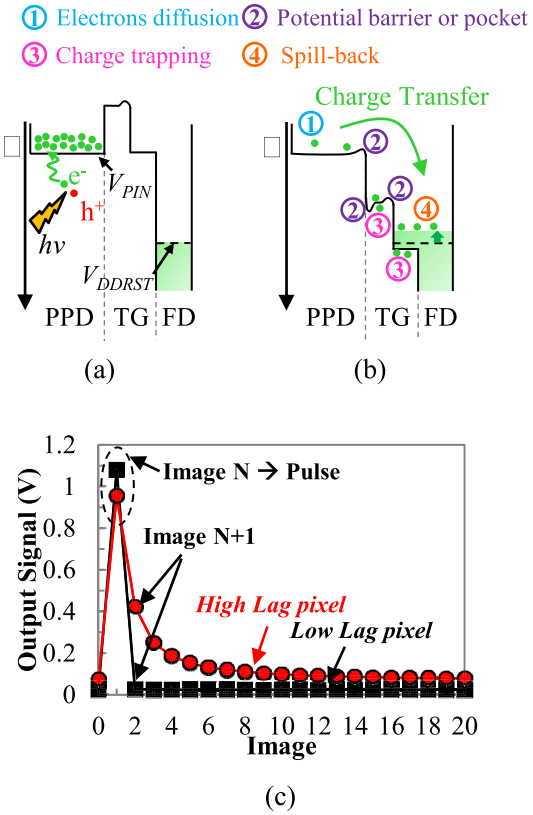

Fig. 2. (a) Schematic illustrations of the charge collection and (b) charge transfer and image lag sources. (c) Output signal as a function of the consecutive images. The pulse, used to generate the bright-to-dark transition, is synchronized in such a way that it is entirely temporal localized in a single frame (i.e., the first in the graph).

whereas the dose rate was increased up to 10 Gy(SiO_2)/s for TID above 1 kGy(SiO_2). The 10-keV X-ray irradiations were performed at CEA, DAM, DIF (Arpajon, France), with the ARACOR facility. All the measurements were performed after three weeks of annealing at room temperature.

Image lag measurements were performed at 22 °C using an LED source at 540 nm to obtain bright-to-dark transition conditions.

For our measurements, the nominal high and low TG bias conditions are $V_{HITG} = 3.3\ V$ and $V_{LOTG} = -0.5$ V, with a transfer time, i.e., the time when TG is in its ON state, of 1 μs. The reset supply voltage, V_{DDRST}, was nominally set at 3.3 V. The image lag results reported along this paper are displayed at a charge level corresponding to 25% of the FWC of each pixel in order to compare the pixels response at the same PPD filling level.

Pinning voltage characteristics were obtained by using the charge injection technique procedure implemented in [8] at the nominal bias conditions (e.g., $V_{HITG} = 3.3$ V, $V_{LOTG} = -0.5$ V, and $V_{DDRST} = 3.3$ V). These measurements give useful information about the potential diagram of the PPD-TG-FD structure allowing investigating on the TID-induced modification. Moreover, it has been possible to evaluate the charge partition phenomenon [8] in the studied devices. This phenomenon, observed by the pinning voltage characteristic measurements, is very important since it is

linked to the spillback phenomenon, responsible of a very bad charge transfer (as explained in Section III) which is observable in the normal readout CIS configuration.

III. Image Lag Sources

In a 4T-pixel (see Fig. 1), the readout of the stored charge in the PPD is done thanks to the OFF–ON switch of the TG which allows the charge transfer of the photo-generated electrons from the PPD to the FD node. During the integration phase, Fig. 2(a), the photo-generated charges are collected in the PPD which is isolated from the FD by turning the TG OFF. At the end of the integration, the TG is turned ON and the charges can be transferred to the FD [Fig. 2(b)]. In an ideal situation, all the accumulated electrons in the PPD should be transferred and converted into the voltage signal which is readout. However, this is not the real situation since different mechanisms and/or nonidealities in the transfer path can cause that a fraction of the stored charges remains in the PPD after the transfer, phenomenon known as image lag. Fig. 2(b) illustrates the different causes of the image lag than can occur in a 4T-pixel, which are linked to the different parts of the pixel, i.e., PPD, TG, and FD.

1) Thermal diffusion of the charges inside the photodiode is considered as the limiting mechanism in the charge transfer. The electrons stored in the PPD, once allowed to the transfer, diffuse along the PPD before arriving at the TG edge [9]. This can cause, if the PPD is not correctly sized or the transfer time is not long enough, that some electrons, far from the PPD-TG edge, remain in the PPD.
2) Potential nonidealities, such as barriers or pocket, occur because of the doping profile in the transfer channel and/or because of the manufacturing process. They slow down the transfer speed preventing the charges to reach the FD [10].
3) Charges trapping by fast interface states can occur when the charges pass through the transfer channel [11].
4) Spillback, i.e., the charges coming back to the PPD from the FD, happens when a too large amount of charges is transferred to the FD (e.g., if it is not correctly sized [12]) which means that the FD potential is lowered down to the TG potential and then that the charges under the TG can go back to the FD once the TG switch in its OFF state.

Because of all these image lag sources, the determination of the charge transfer efficiency in a 4T-pixel is an important and, at the same time, a tricky point, especially when dealing also with radiation degradation such as the dark current increase. The output signal as a function of consecutive images during a bright-to-dark transition [Fig. 2(c)] shows that, when a pixel has a very strong image lag (red curve), the evolution of the signal with time takes more time (about 15 images here) to go back to the dark level because of the remaining electrons in the photodiode. Conversely, in presence of good transfer performances, the dark condition is reached in the image right after the pulse (black curve).

In order to clarify on the possible lag sources in the studied design, Fig. 3 shows the reference pixel potential diagram

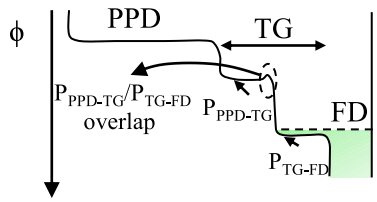

Fig. 3. Potential diagram of the reference pixel reported in Fig. 1.

along the X–X′ cross section of Fig. 1(b) before irradiation. The presence of a PPD-TG P-doped region (P_{PPD-TG}) and a TG-FD P-doped region (P_{TG-FD}) in the TG channel generates a potential step in the potential diagram, due to differences in the doping concentration of the two implants, whereas a potential barrier arises in the P_{PPD-TG}/P_{TG-FD} overlap. This potential configuration allows high transfer performances thanks to the presence of the step in the middle of the TG which prevents the spillback of transferred electrons [13]. During the charge transfer from PPD-to-FD, most of signal electrons—the small barrier induced by the overlap may retain a few carriers—do not remain in the first half of the TG channel since a higher electrostatic potential exists in the second half of the TG (near the FD).

Then, when the TG is switched in its OFF state, the potential difference between P_{PPD-TG} and P_{TG-FD} levels directs the electrons that are in the right half of the TG channel toward the FD and prevent them to return back to the PPD. The image lag is, then, mostly due to the barrier in the middle of the TG, which avoids the transfer of the few carriers retained by it. A large number of samples different from each other by the layout of the transfer channel doping profile allow investigating the radiation-induced effects on charge transfer.

The image lag is usually [14] determined in terms of charge transfer efficiency (CTE) or charge transfer inefficiency (CTI = 1 -CTE). As explained in Section II, the image lag was measured during a bright-to-dark transition. The CTI is then given by the ratio of the readout signal in the image after the pulse (e.g., dark), Q_{N+1}, to the one recorded in the frame in which the pulse is temporally confined (e.g., bright), Q_N. For our purpose, and taking in account that with the increase of the TID the degradation mechanisms can influence and/or misrepresent the information about the charge transfer only the photo generated charges (i.e., without the dark charges, Q_{dark}) are used to calculate the CTI

$$\text{CTI} = \frac{Q_{N+1} - Q_{\text{dark}}}{Q_{\text{N}} - Q_{\text{dark}}}. \tag{1}$$

IV. Radiation Effects on Image Lag

In this section, the experimental data are presented and discussed. Four sections, each one focusing on a particular radiation effect location (summarized in Fig. 1), will be developed in order to clarify the TID impact on the image lag and the influence of the generated defects with respect to the TID range considered.

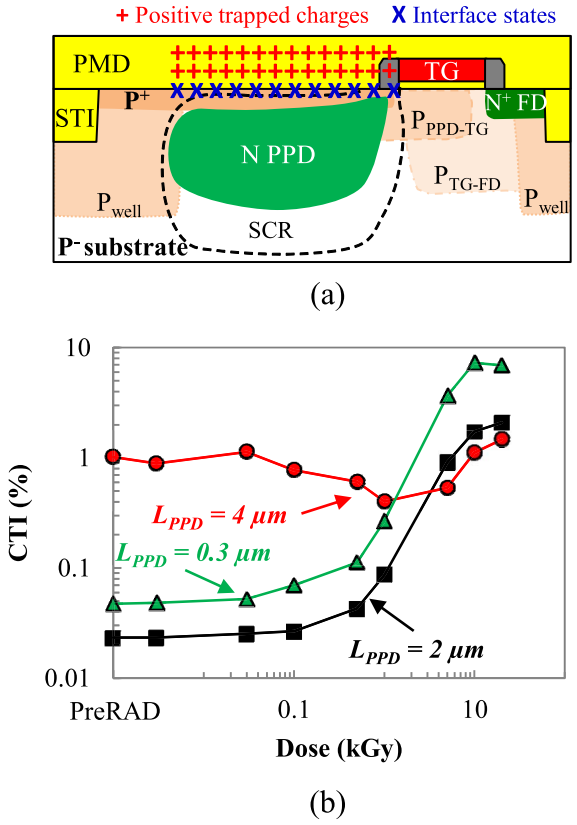

Fig. 4. (a) Schematic of PMD oxide TID effect. PPD = photodiode; TG = transfer gate; FD = floating diffusion; STI = shallow trench isolation; PMD = premetal dielectric; P_{PPD-TG} = PPD-TG P-doped region; and P_{TG-FD} = TG-FD P-doped region. (b) CTI as a function of the TID at Q_{PPD} = FWC/4 for pixels with different PPD lengths.

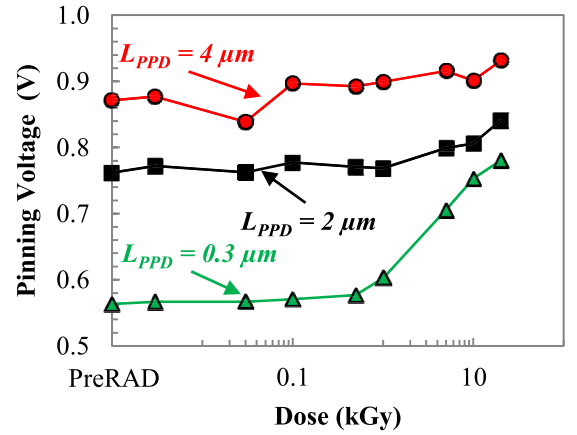

Fig. 5. V_{PIN} as a function of the TID for pixels with different PPD lengths.

A. Pre Metal Dielectric Oxide Effect

First of all the influence of PMD dielectric in the charge transfer process is studied, by testing three pixels differing by their PPD lengths (Pixel 1–Pixel 3 in Table I).

Before irradiation these pixels have a potential diagram as the one of Fig. 3. Fig. 4 shows that before irradiation, when the PPD is too long the charge transfer is strongly limited by the thermal diffusion of the electrons [9]. In the medium and small photodiodes, the limiting factor is rather the barrier in the middle of the TG since our measurements have shown that increasing the transfer time above 1 μs does not reduce the image lag. Up to 30 Gy(SiO_2), the CTI remains almost unchanged in the three pixels, whereas it suddenly changes with the increase of the TID above 0.5 kGy(SiO_2).

In Fig. 5, the evolution of the pinning voltage with the dose is reported.

It is observed that V_{PIN} monotonically increases with the dose at TID $>$ 0.5 kGy(SiO_2) when $L_{PPD} = 0.3$ μm, whereas it remains constant up to 10 kGy(SiO_2) for the other two L_{PPD}. The results reported in Figs. 4 and 5 have shown that PPD with different L_{PPD} are differently affected by the radiation above 0.1 kGy(SiO_2) as regards both lag performances and V_{PIN} characteristics. A summary of the radiation-induced changes is reported in Fig. 6.

For $L_{PPD} = 2$ μm [Fig. 6(a)], the transfer before irradiation is limited by the barrier in the middle of the TG and the pixel exhibits very good lag performances when nonirradiated (CTI $\sim$ 0.05%). After TID of 0.1 kGy(SiO_2), the CTI increase is mostly due to the modification of the potential in the PPD-TG interface where a potential pocket is created (simulation of this effect is reported in [6]) as illustrated by the blue line in Fig. 6(a). Since V_{PIN} is unchanged up to 5 kGy(SiO_2), it is possible to conclude that the potential modification for 0.1 kGy(SiO_2) $<$ TID $<$ 5 kGy(SiO_2) is only due to the positive-trapped charges and interface states in the TG vicinity and/or in the spacer. In this region the pinning layer is, indeed, thinner in order to allow the PPD-to-FD electrons transfer. V_{PIN} starts to increase at TID $>$ 5 kGy(SiO_2) thus suggesting that at these doses the whole PPD potential is influenced by radiation. A possible explanation is that, in this TID range, the interface states and positive-trapped charges generated by radiation in the PMD start impacting the pinning voltage of the PPD.

When the L_{PPD} is reduced to 0.3 μm [Fig. 6(b)], the effect of the induced defects at the PPD-TG interface becomes too important and affects the whole PPD potential. It is observed that V_{PIN} starts to increase at 0.5 kGy(SiO_2). This also explains the difference in CTI value between medium and short PPD observed in Fig. 4 since for the short PPD, the potential increase creates a bigger potential pocket that affects more the charge transfer performances in the short PPD than in the medium one.

The long PPD CTI case is displayed in Fig. 6(c). As already observed, in this pixel, the preirradiation charge transfer is strongly affected by the thermal diffusion of the electrons in the PPD that have to reach the TG. When irradiated, the potential modification induced by the generated defects in the PPD-TG edge improves the lag performance up to TID of 1 kGy(SiO_2). As shown in Fig. 6(c), at first the creation of a potential pocket near the PPD-TG edge lets the electrons to diffuse in this region during the integration phase thus reducing the thermal diffusion mechanisms. The potential pocket has rather the function of a speed-up implant in the PPD [14]. At doses higher than 5 kGy(SiO_2) the potential pocket becomes too big and the retained charges deteriorate again the electron transfer increasing the CTI. It can also be observed that in the long PPD an increase of V_{PIN} occurs at TID $>$ 5 kGy(SiO_2) due to the PMD interface states and positive transfer charges that influence the whole PPD potential.

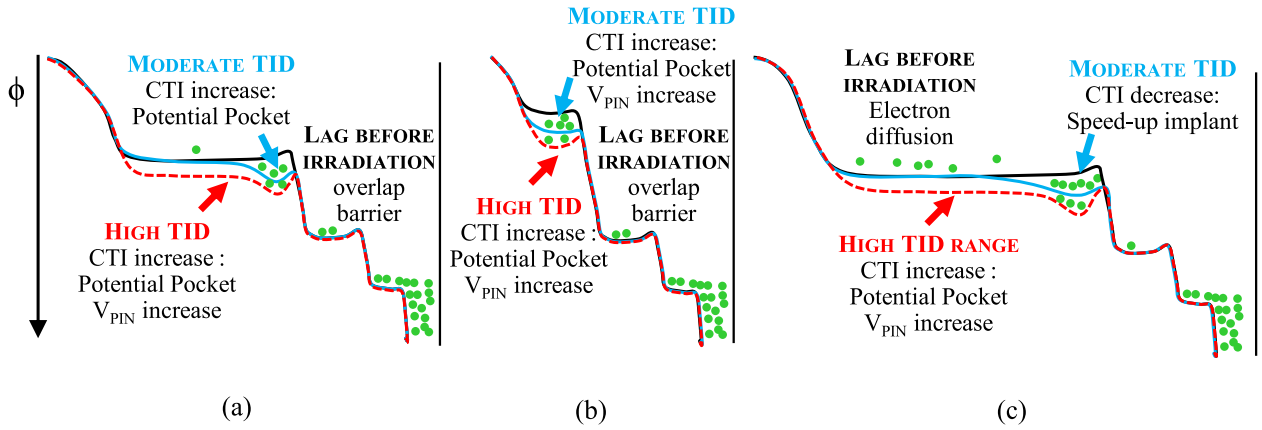

Fig. 6. Schematic potential diagrams of (a) medium, (b) short, and (c) long PPD pixels before irradiation (black line), after TID up to 1 kGy(SiO_2) (light blue line), and for TID above 5 kGy(SiO_2) (red dotted lines).

It is worth noting that the effect of interface states and positive-trapped charges present in the PMD does not affect the image lag since CTI has the same trend with radiation in both medium and short PPD. If present, PMD defects effect should affect more the medium length PPD than the smallest one thus revealing a different CTI behavior between the two pixel types.

B. PPD-TG Edge Effect

In this section, the influence of the PPD-TG edge is investigated. As already explained in Section IV-A and suggested in [3] with the increase of the dose above 0.1 kGy(SiO_2), the radiation-induced defects in the PMD/TG spacer can modify the PPD-TG edge potential.

This is mainly due to the fact that in this region the P^+ pinning layer is thinner to let the PPD reaching the TG channel for the charge transfer. Then, the generation of defects in this region more strongly influences the pixel operation. The way the PMD/TG spacer influences the charge transfer has been investigated thanks to pixels differing by their doping profiles in the TG channel which potential diagrams before irradiation are reported in Fig. 7(a)–(d) together with the main lag sources for each pixel before irradiation. From the results shown in Fig. 8, it can be noted that the image lag is strongly influenced by the TG channel doping profile.

In pixels with the antispillback step [see Fig. 7(a) and (c)], the CTI increases with the dose. The positive-trapped charges and interface states created by the ionizing radiation in the TG vicinity and in the spacer induce a modification of the potential in this region since the P^+ pinning layer is thinner to let the PPD reaching the TG channel for the charge transfer [3]. For these two pixel types, the CTI increase is then due to a creation of a potential pocket in the PPD-TG interface which retains the electrons thus degrading the image lag performances [see Fig. 6(a)].

For pixels where the image lag before radiation is caused by the spillback of the charges under the TG [Fig. 7(b) and (d)], a CTI decrease for 0.1 < TID < 5 kGy(SiO_2) is observed, as shown in Fig. 8. The radiation defects increase the potential under in the PPD-TG region thus reducing the spillback.

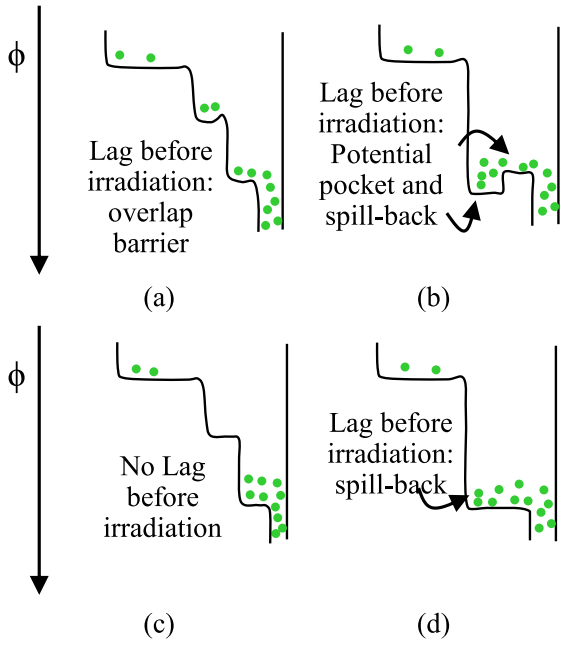

Fig. 7. Potential diagrams to illustrate the charge transfer (TG ON) limiting or improving mechanisms for pixels (a) with PPPD-TG and PTG-FD, (b) without PPPD-TG, (c) without PTG-FD, and (d) pixel D without PPPD-TG and PTG-FD.

A similar spillback reduction has been already observed in nonirradiated CIS [8] and it was shown that increasing V_{LOTG} leads to a reduction of the charge partition phenomenon and then the spillback. This hypothesis has been verified in the studied designs by the comparison of CTI before irradiation in accumulation and depletion regimes. The results reported in Fig. 9 clearly show that, in the pixels which have high lag before irradiation, more the TG OFF barrier is lowered better is the CTI at the same charge level in the PPD (see red curves), whereas for the low lag pixels there is no influence of V_{LOTG} in the charge transfer performances. This result allows then concluding that the TID-induced potential increase leads to the reduction of the spillback thus improving the image lag for the pixel exhibiting a high image lag before irradiation. On the other hand, when the TID increases above 5 kGy(SiO_2) the

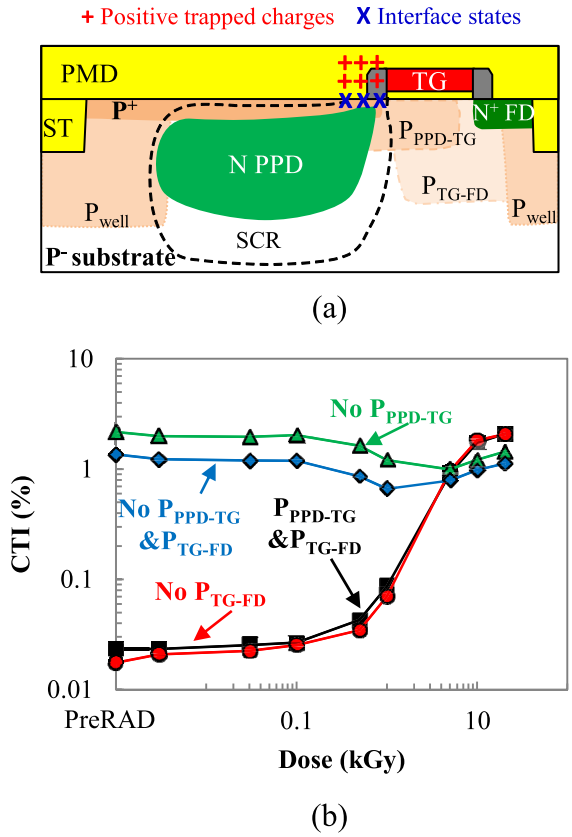

Fig. 8. (a) Schematic of TG PPD/TG TID effect is reported in the inset. PPD = photodiode; TG = transfer gate; FD = floating diffusion; STI = shallow trench isolation; PMD = premetal dielectric; P_{PPD-TG} = PPD-TG P-doped region; and P_{TG-FD} = TG-FD P-doped region. (b) CTI as a function of the TID at Q_{PPD} = FWC/4 for pixels with different TG doping profile; the inset shows the schematic degradation mechanism representation.

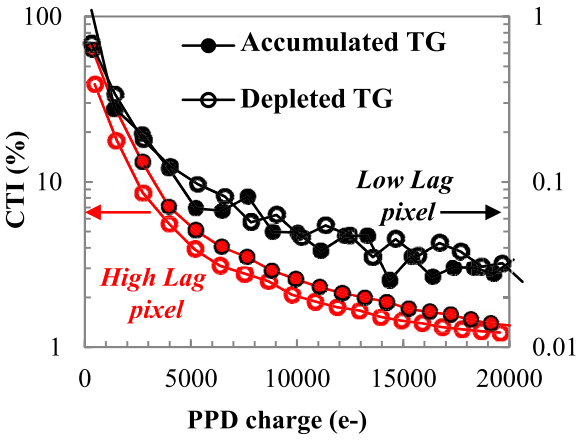

Fig. 9. CTI as a function of the photodiode charge level for a low lag pixel (black curves) and a high lag pixel (red curves) with accumulated TG (solid points) and depleted TG (open points) before irradiation.

CTI for these pixels starts to increase (Fig. 8) since the positive effects of the TG OFF barrier decrease are of less importance in comparison to the potential increase during the transfer phase (TG ON). In this case, as discussed above for the low lag pixels, positive-trapped charges create a potential pocket in the PPT-TG interface which retains part of the electrons.

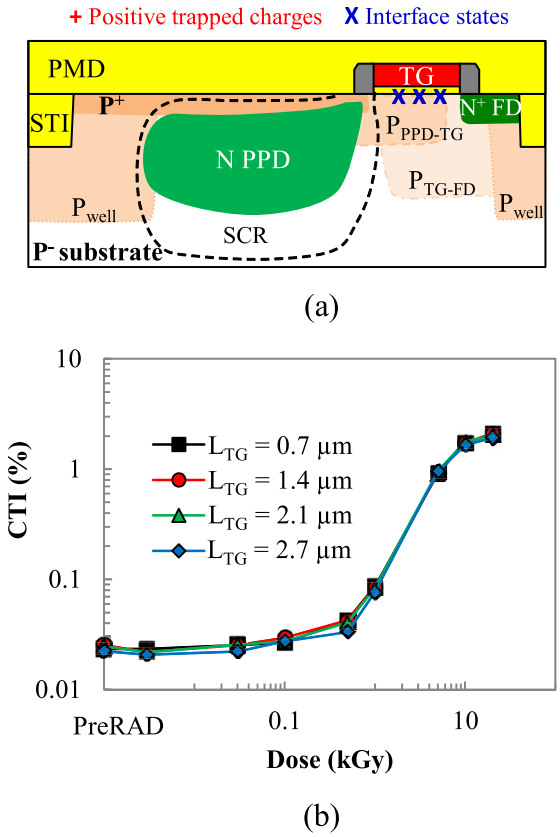

Fig. 10. (a) Schematic of TG gate oxide TID effect. PPD = photodiode; TG = transfer gate; FD = floating diffusion; STI = shallow trench isolation; PMD = premetal dielectric; P_{PPD-TG} = PPD-TG P doped region; and P_{TG-FD} = TG-FD P-doped region. (b) CTI as a function of the TID at Q_{PPD} = FWC/4 for pixels with different TG lengths.

C. TG Gate Oxide Effect

As regards the gate oxide, the effects on charge transfer by the investigation of pixels with different TG lengths (L_{TG}) have been studied; the results reported in Fig. 10 show that the CTI does not depend on the L_{TG} in the whole tested range. This suggests that the charge trapping at the $(Si/SiO_2)_{TG}$ interface does not occur in the studied pixels.

D. STI Oxide Effect

The radiation-induced STI degradation contribution, source D in Fig. 1, on the charge transfer process degradation is investigated thanks to pixels which differ by their TG width, W_{TG} (Pixel 1 and Pixel 4 in Table I).

The results, reported in Fig. 11, show that before irradiation and up to 1 kGy(SiO_2) the two pixels have almost the same CTI since the charge transfer is limited by the barrier in the middle of the TG. However, when the dose increases, the narrowest W_{TG} pixel exhibits the lowest CTI. As discussed in Section IV-B, the radiation-induced defects in the TG channel increase the P doping concentration thus influencing the image lag via a reduction of the spillback (lowering of TG OFF barrier). This effect can be seen in Fig. 12 where the pinning voltage characteristic for the two pixels is reported at different doses. The inset better highlights the charge partition plateau.

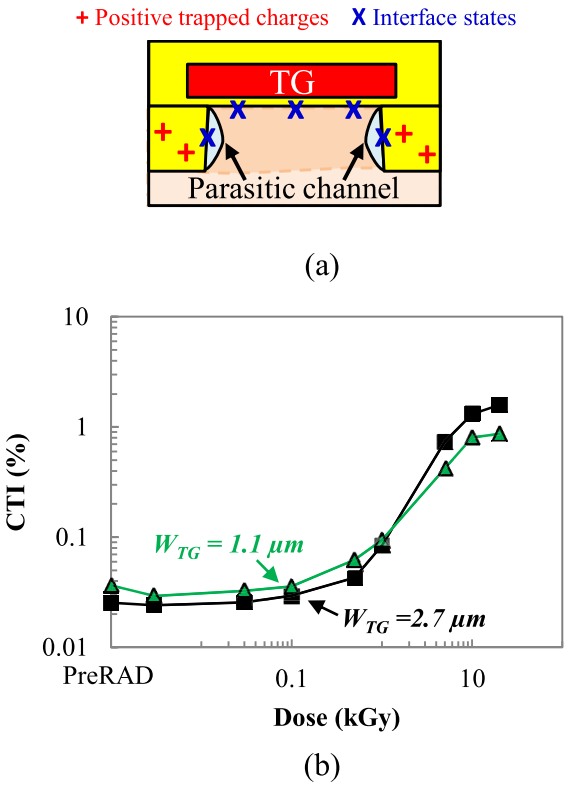

Fig. 11. (a) Schematic of STI oxide TID effect. TG = transfer gate. (b) CTI as a function of the TID at Q_{PPD} = FWC/4 for pixels with different TG widths.

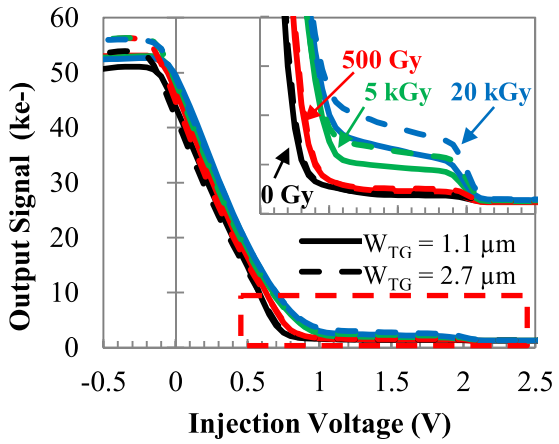

Fig. 12. V_{PIN} characteristic is reported for pixels with different TG widths. The inset shows a magnification of the characteristics to highlight the charge partition and thermionic emission regimes.

At low doses, the characteristics are equals in the two pixels, whereas the charge partition plateau is clearly lower at high doses for pixel with reduced W_{TG}. It is worth mentioning that the spillback reduction is more effective in the narrowest TG channel effect since it can be expected that the generated defects in the STI sidewalls induced higher changes with respect to the wider TG.

V. TID Degradation Recap

The results and discussion reported in Section IV have allowed identifying the role played by the different oxides in the charge transfer degradation with the irradiation.

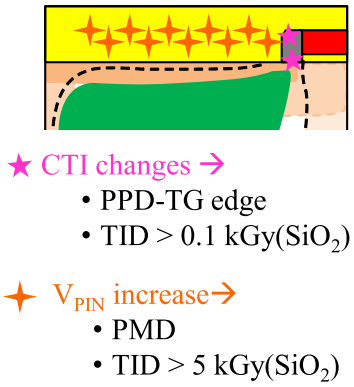

Fig. 13. Summary and localization of the TID-induced degradation sources with the TG in accumulation regime. The TID range in which each degradation source becomes important is also given.

A summary on the main-induced degradation discussed in this paper is reported in Fig. 13.

It is worth noting that the TID induces the generation of different defects which are located in the oxides within the pixel structure (i.e., PMD, TG, spacer, and STI). These defects, i.e., the positive-trapped charges and the Si/SiO_2 interface states, have, however, a similar effect on the CIS performances degradation and the single contribution is difficult to discriminate.

A. Degradation Mechanisms

It has been shown that the TID-induced effect depends on the investigated dose range [15], and that at each dose range, the defects can be generated in the oxides (PMD, TG, spacers, and STI), thus modifying one or more pixel characteristics.

1) At TID < 0.1 kGy(SiO_2) image lag performances remain unchanged for all the considered pixel designs, as well as the pinning voltage characteristics. It is possible to assume that, up to these doses, the radiation-induced defect creation in the oxides, such as interface states and positive charge traps, is not enough to modify the potential of the PPD-to-FD transfer path in the considered accumulation regime.
2) In the 0.1 kGy(SiO_2) < TID < 5 kGy(SiO_2) range, the CTI changes because of the increase of the potential near the PPD-TG edge (see Fig. 13). Image lag is degraded for the pixels where the charge transfer before irradiation is limited by the potential barrier in the middle of the TG. This degradation is mostly due to a creation of a potential pocket formed in this region since the P^+ pinning layer is thinner to let the PPD reaching the TG channel for the charge transfer and which may retain part of the electrons. If the charge transfer before irradiation is instead limited by the thermal diffusion in the PPD, the increase of the potential in the vicinity of the TG improves the lag performance acting as a speed-up implant for the electron transfer. For spillback transfer limited pixels, it has been observed that in this dose range, the CTI decreases because of radiation-induced positive-trapped charge leading to an increase of the potential in the PPD-TG region reducing the spillback.

3) For TID>5 kGy(SiO_2), the CTI increases in all the pixels because of the increase in the potential pocket amplitude which becomes the main cause of the image lag. Moreover, a pinning voltage increase has been observed in this TID range. The V_{PIN} increase has been associated with the radiation-induced defects in the PMD which influence the potential of the whole PPD.

B. Improvement Solutions

The analysis of the main degradation mechanisms induced on 4T-pixels up to TID levels of 20 kGy(SiO_2) has shown that variations in the pixel design, i.e., PPD length and TG width and TG channel doping profile, can be made in order to achieve good charge transfer performances in low to moderate TID range, i.e., up to 5 kGy(SiO_2). Conversely, when the TID level increase above 5 kGy(SiO_2) the image lag degradation affects all the studied pixels design due to the deep potential pocket in the PPD-TG edge. In this case 4T PPD pixels are not suitable and 3T-pixels with conventional photodiodes [16]–[19] have to be preferred. Indeed, they allow the use of RHBD solutions such as drawing a ring of polysilicon (or P+ doping) around the photodiode.

VI. Conclusion

In this paper, we have investigated the radiation-induced degradation on the charge transfer in PPD CIS. Thanks to different pixel designs we were able to isolate the major radiation-induced effects proposed in the literature and to study how they influence the image lag. It has been pointed out that the main cause of the charge transfer degradation is the radiation-induced defects generation in the PMD/TG spacer which modifies the potential diagram at the PPD-TG edge. It has been shown that the two TID regimes are identified. For 0.1 kGy(SiO_2) < TID < 5 kGy(SiO_2), CTI changes due to increasing of the potential at the PPD-TG edge. Moreover, the results have pointed out that the TID effect on the image lag depends on the pixel design. At TID > 5 kGy(SiO_2) CTI increase due to the creation of a deep potential pocket at the PPD-TG edge inducing too important degradations which badly affect image lag performances. Pinning voltage study has pointed out that TID degradation depends on the geometry of the PPD since an increase of V_{PIN} has been observed for the shortest PPD at 1 kGy(SiO_2), whereas for the other pixels the pinning voltage starts to increase for TID > 5 kGy(SiO_2). The pinning voltage increase has been attributed to induced defects in the PMD.

The reported results allow to conclude that PPD CIS will be able to be integrated in the future space missions (from low to moderate dose range) suggesting ways to obtain very good charge transfer performances (i.e., the optimization of the pixel characteristics such as PPD, TG and FD size, and TG channel doping profile). Conversely, when for high TID level, the PPD-TG edge degradation is too high whatever the pixel design, preventing the use of PPD CIS in such environments.

References

[1] E. R. Fossum and D. B. Hondongwa, "A review of the pinned photodiode for CCD and CMOS image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 3, pp. 33–43, May 2014.

[2] V. Goiffon *et al.*, "Radiation effects in pinned photodiode CMOS image sensors: Pixel performance degradation due to total ionizing dose," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2878–2887, Dec. 2012.

[3] V. Goiffon, M. Estribeau, P. Cervantes, R. Molina, M. Gaillardin, and P. Magnan, "Influence of transfer gate design and bias on the radiation hardness of pinned photodiode CMOS image sensors," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3290–3301, Dec. 2014.

[4] S. Place, J.-P. Carrere, S. Allegret, P. Magnan, V. Goiffon, and F. Roy, "Radiation effects on CMOS image sensors with sub-2 μm pinned photodiodes," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 909–917, Aug. 2012.

[5] P. R. Rao, X. Wang, and A. J. P. Theuwissen, "Degradation of CMOS image sensors in deep-submicron technology due to γ-irradiation," *Solid-State Electron.*, vol. 52, no. 9, pp. 1407–1413, 2008.

[6] J. Liu *et al.*, "Simulation and measurement of total ionizing dose radiation induced image lag increase in pinned photodiode CMOS image sensors," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 856, pp. 32–35, Jun. 2017.

[7] E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.

[8] V. Goiffon *et al.*, "Pixel level characterization of pinned photodiode and transfer gate physical parameters in CMOS image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 65–76, Jul. 2014.

[9] J. E. Carnes, W. F. Kosonocky, and E. G. Ramberg, "Free charge transfer in charge-coupled devices," *IEEE Trans. Electron Devices*, vol. ED-19, no. 6, pp. 798–808, Jun. 1972.

[10] C. Chen, Z. Bing, W. Junfeng, and W. Longsheng, "Measurement of charge transfer potential barrier in pinned photodiode CMOS image sensors," *J. Semicond.*, vol. 37, no. 5, pp. 054007-1–054007-5, 2016.

[11] L. Bonjour, N. Blanc, and M. Kayal, "Experimental analysis of lag sources in pinned photodiodes," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1735–1737, Dec. 2012.

[12] O. Marcelot, V. Goiffon, F. Nallet, and P. Magnan, "Pinned photodiode CMOS image sensor TCAD simulation: In-depth analysis of in-pixel pinning voltage measurement for a diagnostic tool," *IEEE Trans. Electron Devices*, vol. 64, no. 2, pp. 455–462, Feb. 2017.

[13] Z. Cao *et al.*, "Design of pixel for high speed CMOS image sensors," in *Proc. Int. Image Sensor Workshop*, 2013, pp. 229–232.

[14] J. R. Janesick *et al.*, "Fundamental performance differences of CMOS and CCD imagers: Part V," *Proc. SPIE*, vol. 8659, p. 865902, Feb. 2013.

[15] V. Goiffon, "Radiation effects on CMOS active pixel image sensors," in *Ionizing Radiation Effects in Electronics: From Memories to Imagers*. Boca Raton, FL, USA: CRC Press, 2015, ch. 11, pp. 295–332.

[16] B. R. Hancock and G. A. Soli, "Total dose testing of a CMOS charged particle spectrometer," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 1957–1964, Dec. 1997.

[17] B. Pain *et al.*, "Hardening CMOS imagers: Radhard-by-design or radhard-by-foundry," *Proc. SPIE*, vol. 5167, pp. 101–110, Jan. 2004.

[18] V. Goiffon *et al.*, "Radiation hardening of digital color CMOS camera-on-a-chip building blocks for multi-MGy total ionizing dose environments," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 45–53, Jan. 2017.

[19] V. Goiffon *et al.*, "Total ionizing dose effects on a radiation hardened CMOS image sensor demonstrator for ITER remote handling," *IEEE Trans. Nucl. Sci.*, to be published, doi: 10.1109/TNS.2017.2765481.