ijpam.eu

A Survey on Flip Flop Replacement to Latch on Various Design

S.P.Vasumathi, D.Murlidharan*

School of Computing, SASTRA Deemed University, Thanjavur

*Corresponding Author

ABSTRACT

Abstract: This paper presents survey for the replacement of flip flop to latches and the advantages of the latch based sequential design Flip flop are the major part of the design a sequential elements and this flip flop has more disadvantages as performance decreases and area increases. An alternate method to increase the performance and reduce the area size latches. Latches are used instead of flip flops in certain places to increase the performance and decrease the area.

Keywords: *Clock Skew, Clock Jitter, Time Borrowing, Flip-Flop, Latch.*

1. INTRODUCTION

A FF is a sequential element which is used to store a bit data and it has two stable state also called as bi-stable multi-vibrator. It is an edge triggered it means the output and the next change with respect to the clocks positive edge or the negative edge. Latches can be used to form the FF. There are different FF they are SR FF, JK FF, T FF and D FF. Latch are the basic block of the sequential circuit and they are built from the gates. Latches are sensitive to the level of the inputs. There are different types of latch they are SR latch, T latch, JK latch. Latches are called as transparent when the data can pass and opaque when data cannot pass through a latch. Feedback paths in latch help in retrieving the data from device. These latches can be used as a storage device to store a one bit data [18-29]. Latches are also called as asynchronous devices. The latch based performance leads a major role in the industry because it effectively reduces the performance, area. This has major

advantages like time borrowing; clock skew and clock jitter are reduced due to the latch based performance.

This paper discusses about if FF is replaced by the latch what will be the advantages in the circuit and how a FF can be replaced by the latch and where can a FF be replaced to a latch.

2. POWER and AREA EFFICIENCY of LATCH AND REGISTER

The challenges in edge triggered FF is clock skew, jitter, and Power voltage temperature variations and this reduces the performance of the system and needs additional safety margin to the system or device. In high level synthesis the FF are outplaced by latches to preserve the functionality. The critical paths of the design are outplaced by the latches. In synchronous design the latches can outplace the FFs when the design meets the following methods:

1)   Write and read do not take place at the same time.

2)   Three sequential FFs so that the middle FF can be replaced by a latch

3)   Even after the death time output of the FF should not be changed for a clock cycle

2.1)   TIME BORROWING:

Latches have time borrowing property that is if there is a pipeline stage and the first stage finishes its operation in less than the expected time then time remaining in the first stage of the pipeline can be given or borrowed to the next stage to perform its operation with carefully balanced in delays [30-42]. But FFs provides hard pipeline stages and the extra time cannot be passed to the next stage in the pipeline. [2]

2.2)   METHODS:

Motivation of latch in this paper

The FFs minimum clock period is given as

$$T_{ff} = t_{critical} + t_{sk} + t_j + t_{cq} + t_{SU}$$

The latch minimum clock period is given as

$$T_l = t_{critical} + t_{dq} + t_j$$

From both equations the latch has smaller clock period less setup time and clock skew.
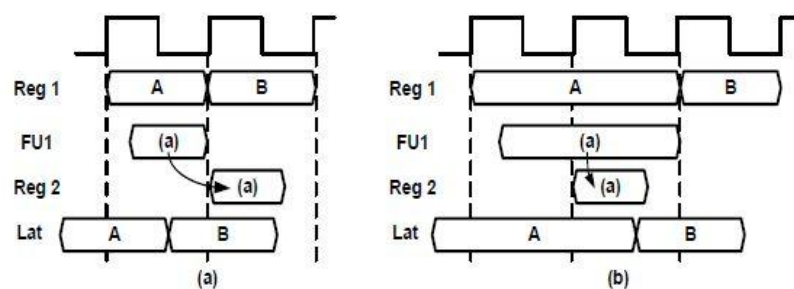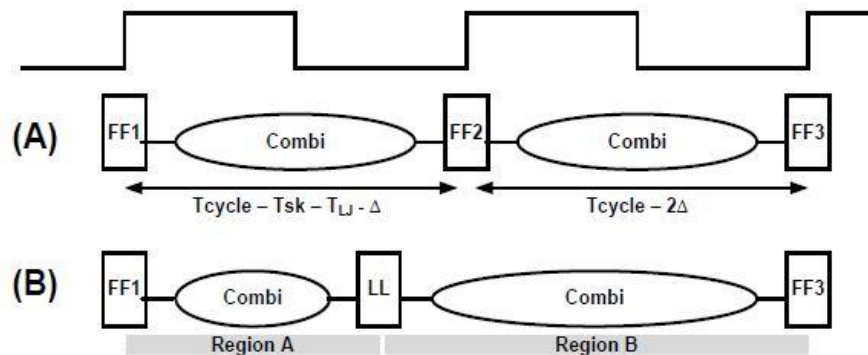

Figure1 (A) Actual path (B) Modified path.

Figure2 Condition 3 FF is replacement

The FF is replaced to latches in the netlist of device and netlist usually gives the connection information related to nets, instances and some attributes.

Each instance has the name of the instance net details and the library cell information to which they are mapped to and the instance. The netlist is generated from RTL design compiler. The netlist is modified from FFs to latches in the library cells.

```
v00ftn03nn0c0 \xprrgr1/xpr_xph_busnum_reg[0]
(.d(xpr_xpi_maddr1[24]), .clk(mb_clk_xp_g),
.rn(mb_mrst_b), .o(xpr_xph_busnum[0]) );
                    (A)


ah01cn901n0d0 \xprrgr1/xpr_xph_busnum_reg[0]
(.d(xpr_xpi_maddr1[24]), .clkb(mb_clk_xp_g),
.o(xpr_xph_busnum[0]) );
                    (B)
```

Figure3 Example for replacement of the FF to latches in the netlist library cells.

2.3)   ADVANTAGES:

1)   When latches are replaced to FF performance is increased by17%. [2, 17]

2)   Reduced power consumption when replaced to latch. [8]

3)   The area is reduced because the latches are simpler then FFs. [8]

4)   Latches have less clock skew and setup time it is also known for its time borrowing and slack passing. [2]

2.4)   DISADVANTAGES:

1)   The latch cannot perform the read and write operation at the same time.

2.5)   EXPERIMENT RESULTS:

After the functionality check the power is improve by 5.78% , area is improved by 2.75% and overall timing is improved by 25% the experiment result shows an lot of improvement when a FF is replaced by the latch.[1]

3) ANALYSING TIMING OPTIMIZATION

3.1) SKEW:

The skew is caused by the clock tree different section in the device receives different input of clock. The difference of input clock in different section causes clock skew.

3.2) JITTER:

The input clock received to the state is expected to be the input clock as such, but the received clock may deviate in different values. This causes clock jitter.[4]

 By the help of minimizing clock skew and jitter, fixed phase retiming is carried out to optimize the time. The jitter and clock skew in the clock cycle play a major role in the high-end microprocessor and speed circuit. [5,6]. Latches has the properties of less clock skew and jitter tolerance and also extra time passing and time borrowing.

3.3) TIMING CONSTRAINT:

There are two timing constrain need to be taken care of when a FF is replaced by the latches.

The races between the short paths are avoided by hold time

$$DCL., MIN=TSK+TH-TCQ$$

Worst case constrain is whether the circuit follow the original clock cycle

$$DCL, MIN=TCYCLE-TSETUP-TSK-TSJ-TCQ$$

If Latches are placed outside needed space then clock skew and jitter can be canceled.
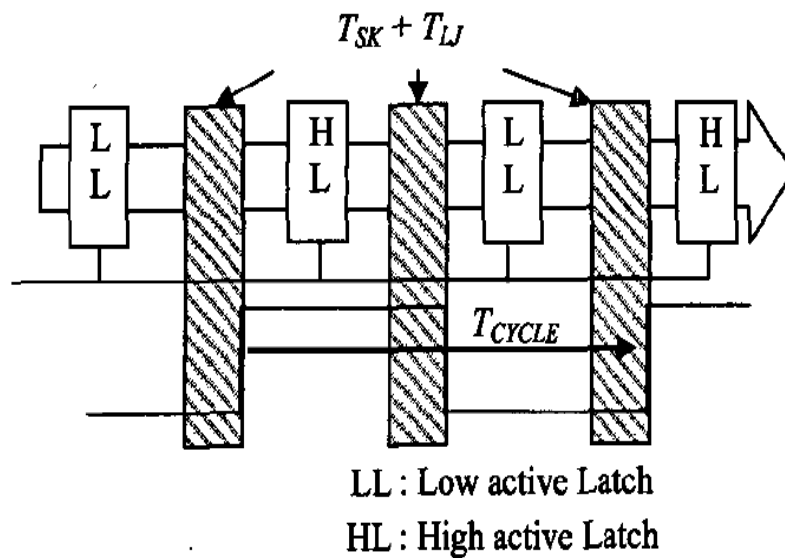
$$DCL, MAX=TCYCLE-2*DTP$$

Figure4 Balanced Latch Timing

3.4) DISADVANTAGES:

There will be lack of formal verification that is the FF is easy to verify itself in formal verification but for the latch the formal verification is difficult. [7, 8, 9]

Optimization technique is less for latches only like buffer insertion and gate resizing

The implemented method adds the SCAN test to the latch that is the SCAN test patterns for the original FFs circuits can be used after the replacement of the latches. [10, 11]

3.5) RULES:

An original FF in the circuit is chosen such that it does not have clock skew and jitter and now the FFs are replaces by latches.

Case one: States only a latch can move over a logical node.

Case two: States a pair of latch is fixed in the place of FFs.

3.6) RETIMING:

Retiming is an optimizing algorithm where the sequential elements convert into the combinational elements without changing the operation of the circuit.

The optimized circuit equation has the operation that does not change the function of the circuit.

$$Ar(e) = a(e) + R(x) - R(y) \qquad (6)$$

Where node x and y are connected to an edge e, Ar (e) is no.of FF after retiming, and R (x) is
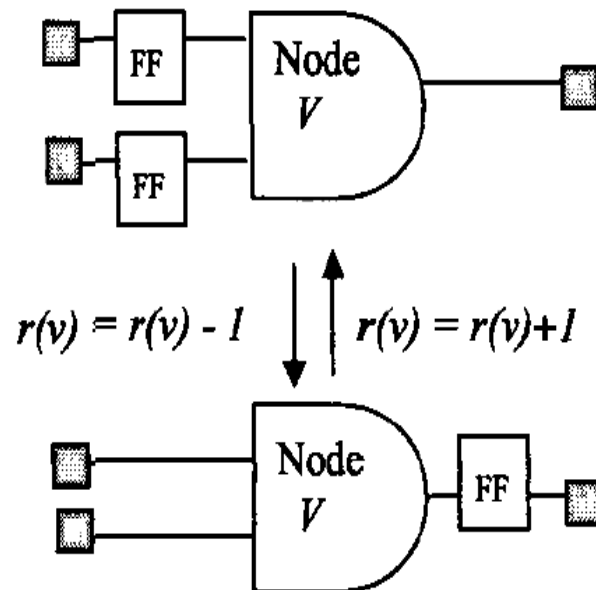
no.of FF moved from node v to outside and inside.

Figure5 Retiming from sequential to combinational

R (x)=-1,0, or1

If (a (e)! =0) then Ar (e)! =0

Fixed phase-forward retiming case   R (x) =-1, 0.

Fixed phase-backward retiming case   R (x) =1, 0.

3.7) ALGORITHM:

In optimization of timing is carried on the input and the latches are replaced only where there is no clock jitter and skew in the circuit.

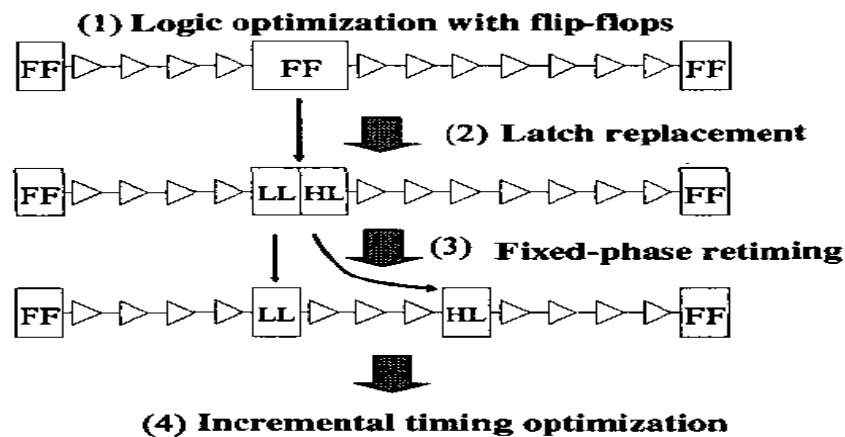Each FF is convert to a pair of active low or active high latches.

Figure6 Algorithm

3.8) EXPERIMENT RESULT:

The developed fixed phase retiming in timing optimization by outplace FFs to latches gained the improvement in maximum timing constrains of the circuit by 17.2%from the originally FF based design. [3]

4) PERFORMANCE OPTIMIZATION in FPGA

Latches which are transparent are pulsed latches and has a 50% duty cycle. Certain FFs are iteratively replaced in the circuit with latches for the improvement in the of the circuit. The multiple skewed clocks are replaced with single clock which helps improve the performance of the circuit. The impact of the minimum delays that is short delay paths which can cause hold time violation are reduced due to the use of latches in place of FFs.

Unfortunately a clock in the FPGA consumes 19-40% of dynamic power consumption. [13, 14].A clock skew is needed for improvement in the circuit speed.

4.1) MINIMUM DELAY:

The longest path between any two circuits and its speed.

4.2) METHODS:

Latches help to resolve the power barrier while using multiple clocks, and their net list modification required in retiming when replacement of FFs to latches.

Consideration: a Logic path from FF j to transparent latch i. The clock period is extened to the maximum delay. If a function starts form j to i's and does not settel on i input by next rising edge of the clock then it may settle after the clock when i is transparent which can have

long and short path delay which creates hold time violations.

4.3) HOLD TIME VIOLATION:

The short and long paths are explained with an example the dark and dot lines represents latches L2, FF2 and FF3. The launched signal from FF1 arrives at L2 at transparent mode then hold time violation. When short signal arrives at the L2 which is transparent hold time can be reduced.
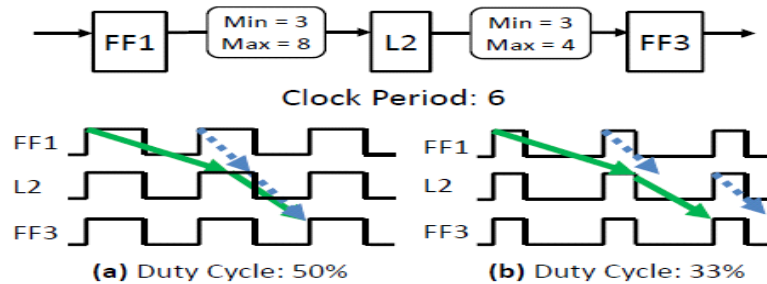

Figure7 Show pulsed clock can reduce duty cycle by 33%

4.4) TIMING CONSTRAINS:

The variation of the latch and FF timing constrain forms multiple latches which has the ability of long and short paths.

$$a_j = min_{j \to i}[max(T_{cq}, a_j + T_{dq}) + cd_{ji}] \text{ for all i (1)}$$

These equations suggest that earliest and latest arrival of clock in latch in i and they are the functions of i through combinational path. The latch i driven by a pulse width Wi

$$A_i <= P + W_i - T_{su} \qquad (2)$$

Combining the long and short path with the pulse width Wi yields

$$max_{j \to I}[max(T_{cq}, A_j + T_{dq}) + CD_{ji}] <= P + W_i - T_{su}, \text{ for all i (3)}$$

The latch hold time constrain combined with (eq 2) yields

$$min_{j \to I}[max(T_{cq}, a_j + T_{dq}) + cd_{ji}] >= W_j + T_h, \text{ for all i (4)}$$

4.5) ALGORITHM:

Maximum Cycle Ratio (MCR)

$$MCR(G) = max_{c \in C}[\sum_{e(u,v) \in c} d(u,v)/|c|] \quad (5)$$

Every FF is a latch with a varying width pulse thus requiring multiple clocks and power consumption. Here single clock are used and only specific pulse width are allowed to latches and the FF. Shortest paths are prevented from limiting the pulse width in FF.

4.6) RULES:

Step 1 clock period's best case for Pinit is calculated and its pulse widths, Winit.

Step 2 Then Using Winit in conjunction with eq 11 to choose the sequential element that has to change to latch.

Step3 Finally some FF remains FF and with the same pulse width Wfinal.

Step 4Then from larger value of Wfinal the scale is taken back to the shortest path delay violation.

Step 5 Then every single FF allocated to whichever a FF or latches and the resolved for P and W established on the allocated FF or latches.

Input: G (V; E), Emin

Output: Pfinal; Wfinal; ! Final

Pinit;!init forward (G)

E in ascending order of short path

Delay in Emin

Wfinal max (!init)

for e (u; v) sorted E do

dmin (u; v) delay of e (u; v)short path Emin

if(Tcq + dmin (u; v) <!init(v) + Th)then

Wfinal Tcq + dmin (u; v) Th

exit

for

end

if

end

for

for e (u; v) 2 E do

dmin (u; v) short path delay of e (u; v) from Emin

if Tcq + dmin (u; v) < Wfinal + Th then

force Flip Flop (v)

else

force Latch (v)

end

   if

end

   for

Pfinal;! final   forward (G)

The inputs are G (V, E) and Emin is the delay between every pair of FF.

Calculation of Pinti and Winti. Sort the edges of E according to Emin

Initialize Wfinal is pulse width max in Winti. Then calculation of hold time violation if not satisfied then it means the pulse widths are larges and it exceeds the violation. Finally Wfinal is found. Next the checking the constrain are the minimum delay less than Wfinal to a FF to assure the hold time violation does not happens again. Calculation of Pfinal and Wfinal according to the newly created structure.

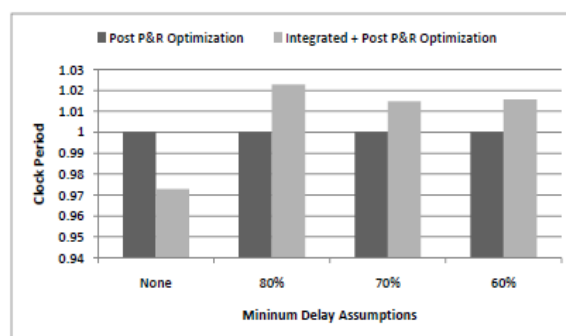**4.7) EXPERIMENT RESULTS:**

Figure8 shows the benefit of using the pulsed latches optimization while using the
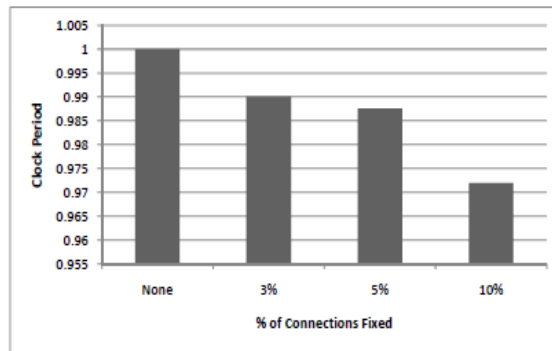clock -slacks, and optimized result is normalized to 1.

Figure9 the minimum delay that is short path is obtained by 70% and the performance is increased by 5%

Thus the performance optimization is obtained by using skewed clocks that can be replaced in place and route section which has no area or the power consumption drawback. [12]

5) TLSSD OPTIMIZED DESIGN

Muxed D are the most used sequential element because it has simplified timing analysis and less race conditions. The latches helps to replace the flip flop and it is useful in the design challenges like Power Voltage Temperatur, low-power and high performance.

5.1) OPERATION:

Figure 10 shows LSSD block diagram, where * divide the input pins and the test inputs. Figure 10 C) shows interconnect of the single latch LSSD cell.

(a)

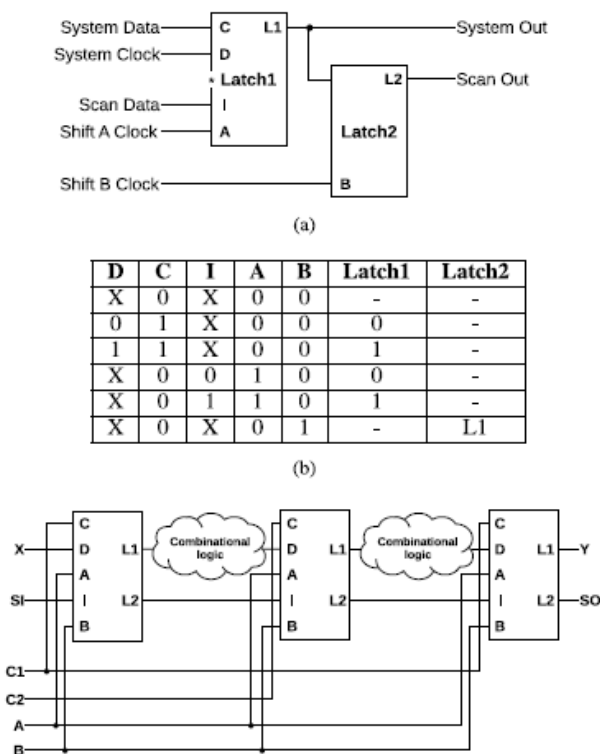| D	C	I	A	B	Latch1	Latch2
X	0	X	0	0	-	-
0	1	X	0	0	0	-
1	1	X	0	0	1	-
X	0	0	1	0	0	-
X	0	1	1	0	1	-
X	0	X	0	1	-	L1

(b)

Figure 10 A)Level Sensitive Scan Design cell, B)Truth Table, C)Interconnection of LSSD

In functional mode, when C is high the data are passed from D to latch L1. The test mode has two steps they are first the data for test are registered in latch 1 at that time A must be high. Second step is the test data are copied from latch 1 to latch 2 at that time the B must be high so that test values are copied from Latch l1 to latch l2.

This LSSD schematic has, 2 three input NANDs, 2 inverter, 8 two-input NANDs and a total of forty-eight transistors and the NANDs cross coupled which causes the transistor sizing.

TLSSD is the optimized LSSD and it contains tristate inverter and inverter so it is called as tristate LSSD. It consists of six transistors for tristate inverter and two transistors for each inverters, four transistor for tristate inverter. Hence total number of transistor is reduced by 48 to 38 and 12 transistor are reduced. This TLSSD has the electrical characterization which has simplified transistor transition and easy measure of the setup and hold time violation. The cross coupled NANDs are avoided in the design of TLSSD scan cell.

5.2) METHODS:

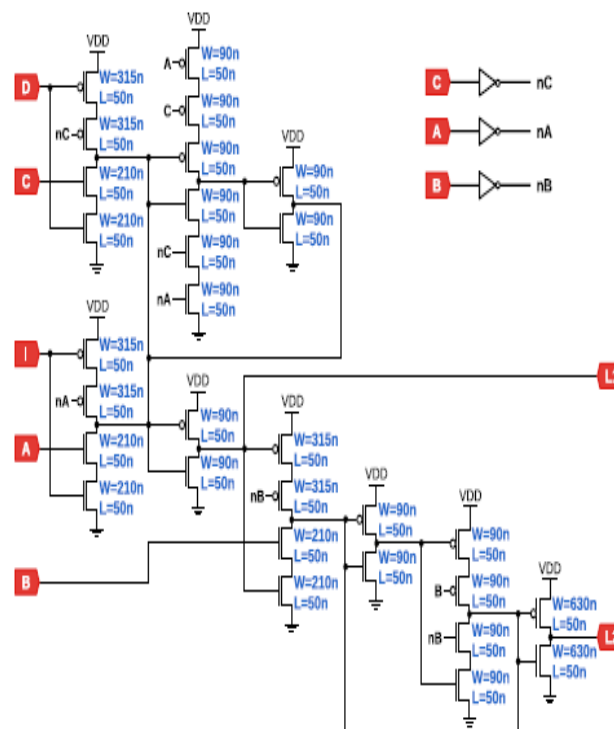The TLSSD was designed by using SPICE, using freePDK45 technology and Nan gate library.

Figure11 Tristate Level Sensitive Scan Design

The Power Delay Product (PDP) defined as the variation between the leakage power and delay of the cell.

$Rel_{PDPd} = ((t_{LSSD}*P_{LSSD})/(t_{TLSSD}*P_{TLSSD})-1)*100$

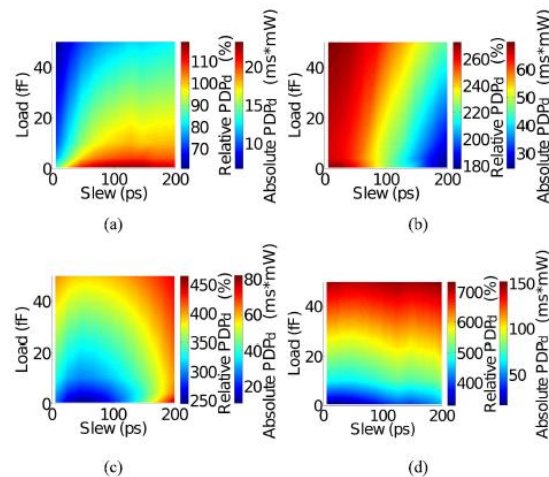$Abs_{PDPd} = ((t_{LSSD}*P_{LSSD})-(t_{TLSSD}*P_{TLSSD}))$

Figure 12 Power and Delay Product (PDP)

The Energy Per Transition (EPT) show variation between the energy and the propagation delay .Figure 13 shows the energy per transition difference (EPTd) EPT of TLSSD and EPT of the LSSD.

$$Rel_{EDTd} = ((t_{LSSD}*E_{LSSD})/(t_{TLSSD}*E_{TLSSD})-1)*100 \qquad (13)$$

$$Abs_{EDTd} = ((t_{LSSD}*E_{LSSD})-(t_{TLSSD}*E_{TLSSD})) \qquad (14)$$
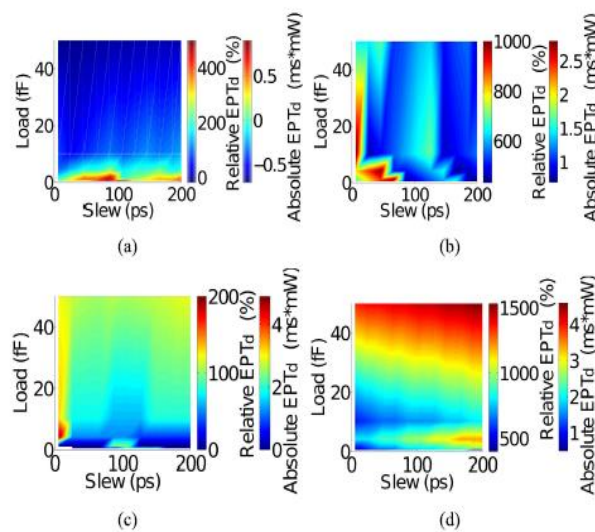

Figure 13 Energy per Transition (EPT)

6) CONCLUSION:

Various designs like time borrowing, max and min delays, Timing constrains, Retiming, Simulation and Verification phase are compared in the paper of flip flop to latch replacement and some flip flops cannot be replaced by latch in some critical paths and retiming is done for such place and more rules are explained for the replacement of flip flop to latch in paper. Hence from the comparison of the design the performance of the design in which the flip flop are replaced to latch are increased and area is reduced.

7) REFERENCES

[1] Nik Azman Nik Hassan, Asrulnizam Bin Abd Manaf, Leong Chan Ming "Optimization of Circuitry for Power and Area Efficiency by Using Combination between Latch and Register", 2011 International Conference on Computer Application and Industrial Electronics(ICCAIE)

[2] D. Chinnery, K. Keautzer, J. Sanghavi, E. Killian, and K. Sheth, "Automatic Replacement of Flip-Flops by Latches in ASICSs," Clossing the Gap Between ASIC and Custom, chapter 7 pp.185-208, Kluwer Acedemic Publisher, 2002.

[3] Young Jun Lee, Yong-Bin Kim, E Lombardi, Nohpill Park" Timing Requirement for Reliable Latch-Based Circuit Design" IMTC 200.1 - Instrumentation and Measurement, Technology Conference, Como, Italy, May,2004

[4]H. Partavi, "Clacked Storage Elements", Design of High-performance Microprocessor Circuits", IEEE Press, ZWO, pp.207-233.

[5] Y Hagihara, S. hui, A. Yoshikawa, T. Uesugi, T. Osada, S.NaLaZat0, M.ked& M. Olrada, and S. Yamada, "A Skew-Tolerant Design Scheme for Ovcr l GHz LSI's," Proceeding of ESSCIRC ZOW, pp.416-419.

[6] 1. D. Wamack, 1. M. Kcaly, 1. Pctmvick, J. G Clabes, C. J.Kimhcr, E. L. huter, P. J. Restle, B. A. Zoric, and C. J.Aaderson, "The circuit and physical design of the POWER4 microprocessor," IBM J. Res. & Dev. 46 Na.1 lanuaryZwZ,pp.27-51.

[7]C.A.J.van Eijik, "Sequential Equivalence Checking without State Traversal", Proceedings of DATE, 1998, pp618-623.

[8] GHastw, A.Mathur, and P.Banejee, "Efficient Equivalence Checking of Multi-Phase Designs Using Retiming", proceedings of ICCAD, 1998, pp557-562.

[9] D.Anastasakis, R.Damiana, H.T.ma, and T.Stanion, "A Practical and Efficient Method for Compare-Point matching",' proceeding afDAC, 2W2, pp305-310.

[10] A. Kobayashi, S. Matsuc, and H. Shiba "Flip-flop Circuit with FLT Capabilily': Proceedings oflECEO conference, 1968, p.962. (In Japanese)

[11] S. Funatsu, N. Wakatsuki, and A. Yamada, "Designing Digital Circuits with Easily Testable Consideration", Proceedings of Test Conferance, 1978, pp.98-102

[12] Bill Teng, Jason H. Anderson" Latch-Based Performance Optimization for FPGAs", 2011 21st International Conference on Field Programmable Logic and Applications.

[13] L. Shang, A. S. Kaviani, and K. Bathala, "Dynamic power consumption in Virtex-II FPGA family," in ACM FPGA, 2002.

[14] V. Degalahal and T. Tuan, "Methodology for high level estimation of FPGA power consumption," in IEEE/ACM ASP-DAC, vol. 1, 2005.

[15] KO Yoshikawa, Keisuke Kanamaru, Shigeto Inui, Yasuhiko Hagihara, Yuichi Nakamurat, Takeshi Yoshimura" Timing Optimization by Replacing Flip-Flops to Latches", 0-780-8175-0/04/$17.00(C)2004 IEEE.

[16] Leonardo Rezende Juracy, Matheus Trevisan Moreira, Felipe Augusto Kuentzer, and Alexandre de Morais Amory" Optimized Design of an LSSD Scan Cell", Optimized Design of an LSSD Scan Cell [1] M Ozaki, Y. Adachi, Y. Iwahori, and N. Ishii, Application of fuzzy theory to writer recognition of Chinese characters, International Journal of Modelling and Simulation, 18(2), 1998, 112-116.

[17] Lalgudi, K.N, Papaefthymiou, M.C. "Fixed-Phased Retiming for Low Power Design," International Symposium on Low Power Electronics and Design, August 1996, pp. 259-264.

[18] Indragandhi, V., Logesh, R., Subramaniyaswamy, V., Vijayakumar, V., Siarry, P., & Uden, L. (2018). Multi-objective optimization and energy management in renewable based AC/DC microgrid. Computers & Electrical Engineering.

[19] Subramaniyaswamy, V., Manogaran, G., Logesh, R., Vijayakumar, V., Chilamkurti, N., Malathi, D., & Senthilselvan, N. (2018). An ontology-driven personalized food recommendation in IoT-based healthcare system. The Journal of Supercomputing, 1-33.

[20] Arunkumar, S., Subramaniyaswamy, V., & Logesh, R. (2018). Hybrid Transform based Adaptive Steganography Scheme using Support Vector Machine for Cloud Storage. Cluster Computing.

[21] Indragandhi, V., Subramaniyaswamy, V., & Logesh, R. (2017). Resources, configurations, and soft computing techniques for power management and control of PV/wind hybrid system. Renewable and Sustainable Energy Reviews, 69, 129-143.

[22] Ravi, L., & Vairavasundaram, S. (2016). A collaborative location based travel recommendation system through enhanced rating prediction for the group of users. Computational intelligence and neuroscience, 2016, Article ID: 1291358.

[23] Logesh, R., Subramaniyaswamy, V., Malathi, D., Senthilselvan, N., Sasikumar, A., & Saravanan, P. (2017). Dynamic particle swarm optimization for personalized recommender system based on

electroencephalography feedback. Biomedical Research, 28(13), 5646-5650.

[24] Arunkumar, S., Subramaniyaswamy, V., Karthikeyan, B., Saravanan, P., & Logesh, R. (2018). Meta-data based secret image sharing application for different sized biomedical images. Biomedical Research,29.

[25] Vairavasundaram, S., Varadharajan, V., Vairavasundaram, I., & Ravi, L. (2015). Data mining-based tag recommendation system: an overview. Wiley Interdisciplinary Reviews: Data Mining and Knowledge Discovery, 5(3), 87-112.

[26] Logesh, R., Subramaniyaswamy, V., & Vijayakumar, V. (2018). A personalised travel recommender system utilising social network profile and accurate GPS data. Electronic Government, an International Journal, 14(1), 90-113.

[27] Vijayakumar, V., Subramaniyaswamy, V., Logesh, R., & Sivapathi, A. (2018). Effective Knowledge Based Recommeder System for Tailored Multiple Point of Interest Recommendation. International Journal of Web Portals.

[28] Subramaniyaswamy, V., Logesh, R., & Indragandhi, V. (2018). Intelligent sports commentary recommendation system for individual cricket players. International Journal of Advanced Intelligence Paradigms, 10(1-2), 103-117.

[29] Indragandhi, V., Subramaniyaswamy, V., & Logesh, R. (2017). Topological review and analysis of DC-DC boost converters. Journal of Engineering Science and Technology, 12 (6), 1541–1567.

[30] Saravanan, P., Arunkumar, S., Subramaniyaswamy, V., & Logesh, R. (2017). Enhanced web caching using bloom filter for local area networks. International Journal of Mechanical Engineering and Technology, 8(8), 211-217.

[31] Arunkumar, S., Subramaniyaswamy, V., Devika, R., & Logesh, R. (2017). Generating visually meaningful encrypted image using image splitting technique. International Journal of Mechanical Engineering and Technology, 8(8), 361–368.

[32] Subramaniyaswamy, V., Logesh, R., Chandrashekhar, M., Challa, A., & Vijayakumar, V. (2017). A personalised movie recommendation system based on collaborative filtering. International Journal of High Performance Computing and Networking, 10(1-2), 54-63.

[33] Senthilselvan, N., Udaya Sree, N., Medini, T., Subhakari Mounika, G., Subramaniyaswamy, V., Sivaramakrishnan, N., & Logesh, R. (2017). Keyword-aware recommender system based on user demographic attributes. International Journal of Mechanical Engineering and Technology, 8(8), 1466-1476.

[34] Subramaniyaswamy, V., Logesh, R., Vijayakumar, V., & Indragandhi, V. (2015). Automated Message Filtering System in Online Social Network. Procedia Computer Science, 50, 466-475.

[35] Subramaniyaswamy, V., Vijayakumar, V., Logesh, R., & Indragandhi, V. (2015). Unstructured data analysis on big data using map reduce. Procedia Computer Science, 50, 456-465.

[36] Subramaniyaswamy, V., Vijayakumar, V., Logesh, R., & Indragandhi, V. (2015). Intelligent travel recommendation system by mining attributes from community contributed photos. Procedia Computer Science, 50, 447-455.

[37] Vairavasundaram, S., & Logesh, R. (2017). Applying Semantic Relations for Automatic Topic Ontology Construction. Developments and Trends in Intelligent Technologies and Smart Systems, 48.

[38] Logesh, R., Subramaniyaswamy, V., Vijayakumar, V., Gao, X. Z., & Indragandhi, V. (2017). A hybrid quantum-induced swarm intelligence clustering for the urban trip recommendation in smart city. Future Generation Computer Systems, 83, 653-673.

[39] Subramaniyaswamy, V., & Logesh, R. (2017). Adaptive KNN based Recommender System through Mining of User Preferences. Wireless Personal Communications, 97(2), 2229-2247.

[40] Logesh, R., & Subramaniyaswamy, V. (2017). A Reliable Point of Interest Recommendation based on Trust Relevancy between Users. Wireless Personal Communications, 97(2), 2751-2780.

[41] Logesh, R., & Subramaniyaswamy, V. (2017). Learning Recency and Inferring Associations in Location Based Social Network for Emotion Induced Point-of-Interest Recommendation. Journal of Information Science & Engineering, 33(6), 1629–1647.

[42] Subramaniyaswamy, V., Logesh, R., Abejith, M., Umasankar, S., & Umamakeswari, A. (2017). Sentiment Analysis of Tweets for Estimating Criticality and Security of Events. Journal of Organizational and End User Computing (JOEUC), 29(4), 51-71.