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RESEARCH ARTICLE

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Alkali treatments of Cu(In,Ga)Se₂ thin-film absorbers and their impact on transport barriers

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Abstract

We study the impact of different alkali post-deposition treatments by thermal admittance spectroscopy and temperature-dependent current-voltage (IVT) characteristics of high-efficiency Cu(In,Ga)Se₂ thin-film solar cells fabricated from low-temperature and high-temperature co-evaporated absorbers. Capacitance steps observed by admittance spectroscopy for all samples agree with the widely observed N1 signature and show a clear correlation to a transport barrier evident from IVT characteristics measured in the dark, indicating that defects are likely not responsible for these capacitance steps. Activation energies extracted from capacitance spectra and IVT characteristics vary considerably between different samples but show no concise correlation to the alkali species used in the post-deposition treatments. Numerical device simulations show that the transport barrier in our devices might be related to conduction band offsets in the absorber/buffer/window stack.

KEYWORDS

admittance spectroscopy, alkali, CIGS, solar cells, transport barrier

1 | INTRODUCTION

The beneficial effect of sodium (Na) on the efficiency of Cu(Ga,In)Se₂ (CIGS) thin-film solar cells was discovered more than 2 decades ago.¹ Significant improvements in the grain growth and solar cell efficiency were observed when soda-lime float glass (SLG), which contains large amounts of Na, was used as growth substrate. Since then, an increasing variety of alkali species have been applied to CIGS thin-film solar cells. Post-deposition treatments (PDT) of the as-grown absorber consist of depositing thin layers of alkali fluorides and have proven to be a successful route to supply additional alkali species beyond Na diffusing from

the SLG substrate.² Current world-record devices with efficiencies of up to 22.6% all contain Na and heavier alkali species, typically potassium (K) or, more recently, rubidium (Rb).³ Despite the tremendous success of alkali PDTs, much about the impact of alkali atoms on the fundamental solar cell device properties is still unknown or under debate.

Electrical dc and ac measurements of the temperature-dependent current-voltage characteristics (IVT), capacitance-voltage relation (C-V), and frequency-dependent capacitance (thermal admittance spectroscopy, TAS) are among the most important device characterization techniques to study complete solar cell devices.⁴ Characterizing working devices is particularly important, as materials in the device stack might

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behave very differently from individual layers due to modifications occurring during further processing steps, electrical interactions, or inter-diffusion between adjacent layers.⁵ Furthermore, applied bias and illumination during realistic device operation needs to be accounted for.

Despite the importance of electrical device characterization, the standard interpretation particularly of the voltage-dependent, frequency-dependent, and temperature-dependent capacitance has frequently been challenged for thin-film solar cells. One particular capacitance step, termed "N1",⁶ is commonly observed for all CIGS thin-film solar cells, and is also dominating the frequency-response of our devices (see Section 3). The origin of the N1 signature has been discussed controversially for already 2 decades. Initially, this signature was attributed to continuously distributed defects at the CIGS/buffer interface, as the activation energy was found to be sensitive to oxidation or air annealing.^{6,7} By contrast, the N1 signature was later also identified in drive-level capacitance profiling of the CIGS bulk and was thus reevaluated as an acceptor-like bulk defect.⁸ By comparing admittance spectroscopy and deep-level transient spectroscopy (DLTS), Igalson et al⁹ concluded that a highly *p*-doped layer in the space charge region results in capacitance contributions of deep acceptor states mostly near the CIGS/buffer interface, and that N1 is a combination of interface states and interface-near deep defects in the bulk. Also using DLTS, Zabierowski et al¹⁰ found that the N1 signal consists of 4 distinct components and identified In_{Cu} -related metastable defects as potential origin of the N1 signature. Independent of the proposed nature or location of these defects, a defect response appears to be the most widely used interpretation of the N1 signal, and in fact any capacitance step above a potential freeze-out in admittance spectroscopy. There have been an increasing number of publications which provide alternative explanations for the N1 level, most linked to the transport characteristics of the solar cell. Reislöhner et al argue that the N1 signature could be explained by a mobility freeze-out due to hopping conduction,¹¹ or by percolative charge transport due to spatial inhomogeneities in the absorber.¹² Lauwaert et al¹³ showed that DLTS signals recorded for different pulse directions are not compatible with standard models of carrier capture and emission by defect states in the device. Instead, *R-C*-like non-ideal contacts or interlayers in series with the main junction were shown to result in capacitance steps and DLTS peaks which could explain the N1 signature.¹³⁻¹⁶ With the main junction located at the front CIGS/buffer interface in the device, the *R-C*-like barrier or counter-diode in series with the main junction has been attributed to the back contact in these studies. Experimentally, this is supported by the observation of a phototransistor effect in the bulk of CIGS solar cells,¹⁷⁻¹⁹ which indeed suggests the presence of a Schottky contact at the back of the device. Furthermore, Eisenbarth et al²⁰ reported that changes in the space charge region width around the N1 capacitance step do not directly correlate with the thickness of the buffer layer and might thus be more likely caused by the back contact. By contrast, Igalson et al⁹ reported on a correlation between the N1 signature and blocking of the diode current in forward bias, which they attributed to Fermi level pinning at the CIGS/buffer interface at the front of the device. Recently, we demonstrated that excessive RbF treatment leads to modifications of the CIGS/buffer interface, which affect the N1 signature observed in admittance spectroscopy.²¹

We further demonstrated that bias-dependent and illumination-dependent impedance spectra of CIGS solar cells suggest a depleted buffer layer but are difficult to reconcile with deep defects as origin of the N1 signature.²² However, both different back electrodes²³ and different buffer layer stacks²⁴ at the front of the device were reported to modify the admittance spectrum, and the main capacitance step of all devices was found to agree with the N1 signature. Differences in experimental observations and interpretation were also proposed to be a consequence of a multitude of signals potentially coexisting in CIGS devices.²⁵ Note, that signatures comparable to N1 were also observed in photo-induced current transient spectroscopy (PICTS) measurements^{26,27} on CIGS absorbers, which probe the bulk of the absorber and where no *n*-type front layers are deposited on the CIGS.

The preceding discussion illustrates that different potential explanations for the N1 signature in CIGS solar cells exist, notably bulk or interface defects, or transport barriers at the front or rear of the absorber layer. While these previous studies show that transport barriers can indeed be a potential explanation for the N1 signature, this is challenging to verify experimentally using only capacitance-based techniques, because defects and transport barriers lead to comparable frequency-responses in ac techniques. On the other hand, the dc current transport characteristics of a solar cell device in strong forward bias will be sensitive to transport barriers at different locations of the device.²⁸ Nevertheless, the complicated device structure of the CIGS hetero-junction solar cells suggests that simple analytical transport models might be insufficient to adequately explain experimental data, and that numerical device simulations could provide more detailed insight concerning the location of dominant transport barriers within the device. In this paper, we link experimental ac and dc transport characteristics of many solar cells to explore the importance of transport barriers in the device. We compare our data to numerical device simulations of the temperature-dependent current-voltage characteristics in order to identify the dominant interface barrier in the device. We use photoluminescence (PL) to verify that deep defects indeed do not play a significant role in our devices.

Due to the wide spread of results in literature even for untreated solar cells, studies of the impact of alkali PDTs on CIGS solar cells will always suffer from ambiguities in the characterization methods if only individual or few measurements are taken into account. We present a systematic study of the impact of different alkali PDTs on the electrical device properties of solar cells fabricated from state-of-the-art high-efficiency absorbers. Because likely several possible origins of the N1 signature coexist, this choice of samples ensures that our measurements are representative of current record-efficiency devices. We also develop further insight into the interpretation of capacitance steps observed in TAS based on the large set of data on highly-efficient CIGS solar cells presented here. In Section 3, we discuss temperature-dependent capacitance spectra and show that the frequency response of our devices is dominated by 1 or 2 capacitance steps, which would be identified as N1 signatures according to common practice. Photoluminescence experiments in Section 4 demonstrate that the high-efficiency absorbers show no significant defect luminescence at defect energies compatible with the N1 signature observed in admittance spectroscopy. This indicates that defect concentrations in the relevant energy range are low and should not

contribute significantly to the capacitance spectrum. Instead, we link the main capacitance step to a transport barrier evident from temperature-dependent current-voltage characteristics in Section 5 and show in Section 6 that such transport barriers are likely related to the conduction band offsets at the front of the device.

2 | SAMPLE PREPARATION AND CHARACTERIZATION

We compare 2 different sets of Cu(Ga,In)Se₂ (CIGS) thin-film solar cells fabricated at the Center for Solar Energy and Hydrogen Research (ZSW) and the Swiss Federal Laboratories for Materials Science and Technology (Empa), respectively. Details of the processing conditions are similar to those in Chirilă et al.,² Jackson et al.,³ and Chirilă et al.²⁹ All absorbers are grown by co-evaporation of Cu, In, Ga, and Se in a multi-stage vacuum process. At ZSW, sputtered Mo on SLG is used as substrate, and the co-evaporation process is performed at standard elevated temperatures. The Empa absorbers are designed for the deposition onto flexible polyimide foils, which requires substrate temperatures below 450°C at all times during the deposition process. However, to simplify handling, the Empa absorbers are deposited onto 1-mm-thick SLG substrates in this study. A silicon oxide (SiO_x) layer is introduced between SLG and Mo back contact to suppress Na diffusion from the SLG, which would also not be present if polyimide foil was used instead.

Different alkali post-deposition treatments (PDT) are performed by in-situ co-evaporation of alkali-fluorides in Se atmosphere after the CIGS deposition. The different PDTs employ KF, RbF, and CsF for ZSW absorbers, and NaF, NaF + KF, and NaF + RbF for Empa absorbers. Additional solar cells without PDT are studied as well. Note that all ZSW samples contain Na, and in lower concentrations K, due to diffusion from the Na-containing and K-containing SLG substrate. In the case of Empa absorbers, a NaF-PDT is always applied before any KF- or RbF-PDT in all samples, because the SiO_x barrier layer and reduced substrate temperature suppress alkali diffusion from the SLG substrate into the CIGS absorber. Any further reference to KF- or RbF-PDTs on Empa samples thus implies a previous NaF-PDT.

All absorbers are processed into finished solar cells by chemical bath deposition of a CdS buffer layer, sputtering of a (Zn,Mg)O/ZnO:Al (ZSW) or i-ZnO/ZnO:Al (Empa) window stack, and evaporation of Ni/Al contact grids at the respective institutes. A MgF₂ anti-reflection coating (ARC) is used on 1 set of devices, all other devices used for this study do not have any ARC. Individual solar cells with a total area of approximately 0.5 to 0.6 cm² are defined by mechanical scribing. Designated area power conversion efficiencies of the cells in the study are in the range of 13% to 14% for the alkali-free low-temperature absorbers, and 16% to 20% for absorbers containing alkali elements (up to 21% with ARC). Table 1 shows a summary of the designated area cell efficiencies η for the different PDTs and absorbers used in this study.

For electrical measurements, solar cells are glued to an aluminum sample holder using thermally conductive adhesive. The front contacts of the solar cells are connected to the measurement circuit by ultrasonic bonding of gold wire to the contact pads, the back contact is connected by manual indium soldering to the Mo back contact of the solar cells. Two wires are used for each connection in a 4-point

TABLE 1 Range of designated area power conversion efficiencies η of the devices fabricated for this study. Devices from the upper range of efficiencies for each PDT were chosen for electrical characterization. Few devices failing quality control are excluded from this table. Notes: a) untreated high-*T* absorbers contain Na from the SLG and are thus compared with the NaF-treated low-*T* absorbers; b) with ARC

PDT	ZSW (High- <i>T</i>) η [%]	Empa (Low- <i>T</i>) η [%]
None	---	13.2-14.2
NaF/(Na) ^{a)}	17.6-18.8	16.2-17.6
KF	18.6-19.2	18.9-19.3
RbF	20.0-20.3 [20.6-21.1 ^{b)}]	18.0-18.3
CsF	19.3-19.8	---

configuration to reduce the influence of wire resistance on the measurement. A temperature sensor is glued onto an identical glass substrate besides the solar cells to ensure accurate temperature readings representative of the actual temperature at the solar cell surface. The sample holder is mounted in the dark in a closed-cycle cryostat at a base pressure below 10⁻³ mbar. An optical port in the cryostat with a shutter and a neutral density filter wheel assembly permits dark and illuminated measurements at different illumination intensities without changes to the halogen lamp used as light source. The intensity of full illumination is set once prior to the measurement to yield the correct previously measured short-circuit current density at a temperature of 300 K.

The temperature-dependent dark and light current-voltage characteristics (*IVT*) are recorded while cooling down the sample in steps of 10 K (set temperature) in a range between 320 and 20 K, allowing sufficient time for temperature stabilization before each measurement. Note that the measured sample temperature might deviate significantly from the setpoint due to the low thermal conductivity of the glass substrate and typically only reaches 40 to 50 K at the lowest temperature setting of $T_{\text{set}} = 20$ K. After *IVT* measurements, the sample is heated to 300 K and kept in the dark for at least 12 hours to ensure a sufficient relaxation of any photo-induced instabilities. This is verified by ensuring a constant capacitance reading in short-circuit conditions. The admittance spectrum is recorded in the same temperature range while cooling down in a frequency range of $f = 100$ Hz to 1 MHz at a dc bias voltage of 0 V and an ac amplitude of 30 mV rms. A parallel equivalent circuit model is used to separate the conductance *G* and capacitance *C*. Note that some measurements show an extreme capacitance dispersion at high frequencies above a few 100 kHz, which does not appear to follow any consistent temperature dependence. As this feature also may differ between measurements on the same sample, the most likely origin is related to the external contacts to the sample. Thus, features at the highest frequencies are discarded during analysis.

For PL measurements, the CIGS absorbers are covered with a CdS layer and excited by the 514.5-nm line of an Ar⁺ laser at a sample temperature of 10 K. The laser spot is focused to a diameter of 80 μm (area $\approx 5 \times 10^{-5}$ cm²) and carries photon fluxes in the range of 5×10^{18} to 2×10^{21} photons cm⁻² s⁻¹. The emitted PL is collected by off-axis parabolic UV-enhanced aluminum mirrors and redirected into a double monochromator with a combined focal length of 600 mm. The collection area is estimated to be approximately equal to the excitation area, ie, approximately 5×10^{-5} cm². The PL signal is recorded by a low-noise mid-infrared InAs-based detector cooled to an operating

temperature of 77 K. To improve the signal-to-noise ratio of the measured signal, a chopper and lock-in technique are used in addition.

3 | CAPACITANCE STEPS IN ADMITTANCE SPECTROSCOPY

All samples with both Empa and ZSW absorbers qualitatively show the same features in their admittance spectra. A representative example of such a spectrum is shown in Figure 1 for a RbF-treated ZSW absorber. Some of the typical features of the capacitance spectra are more pronounced for certain samples, and we present the capacitance spectrum of a KF-treated Empa absorber in Figure 2 for comparison (note the different scale on the y-axis). From high to low measurement temperatures in the admittance spectra, we observe the following features, which are marked by arrows in Figures 1 and 2:

1. A slight capacitance dispersion at the highest temperatures, which could be caused by the presence of deep defects, interface defects, or tail states at the band edges.³⁰ This feature appears to be enhanced for some of the samples only containing Na, but at this point in time provides no further insight and hence will not be covered in the present paper.
2. A well-defined capacitance step at intermediate temperatures, typically in the range of 100 to 250 K (corresponding to a

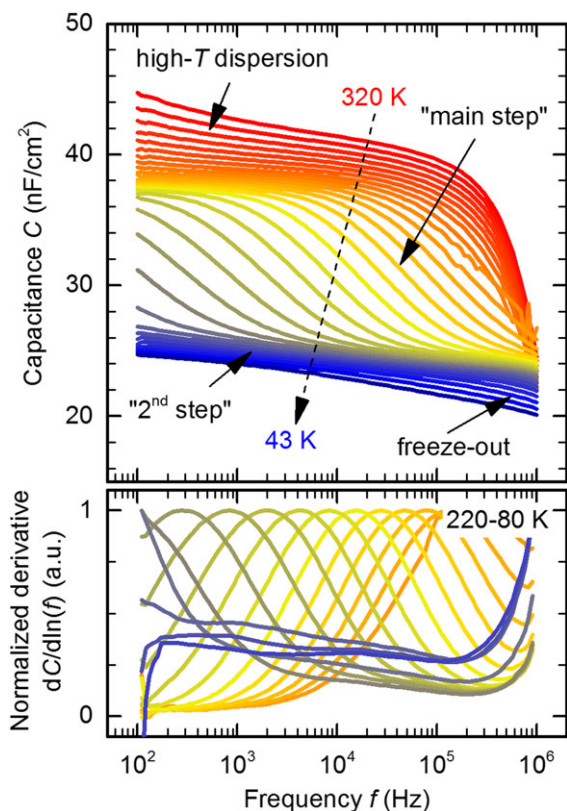


FIGURE 1 Temperature-dependent capacitance spectrum (top) for a measured temperature range of 320 to 43 K and (bottom) corresponding normalized logarithmic derivative $dC/d\ln(f)$ (bottom, 220–80 K) for a RbF-treated high-temperature absorber. The denominations used to describe the main features of the spectrum are given in the graph [Colour figure can be viewed at wileyonlinelibrary.com]

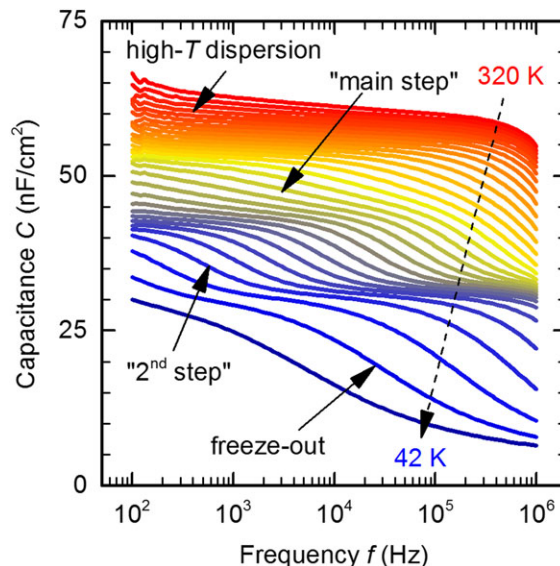


FIGURE 2 Temperature-dependent capacitance spectrum for a measured temperature range of 320 to 42 K for a KF-treated low-temperature absorber, which shows a pronounced second capacitance step and capacitance freeze-out at low temperatures [Colour figure can be viewed at wileyonlinelibrary.com]

capacitance drop from 38 to 26 nF/cm² for the example shown in Figure 1). We denominate this signature the “main” capacitance step, and it will be discussed in more detail below.

3. There appears to be a second capacitance step just below the main step, which is visible as a shoulder at a frequency range of 10 to 100 kHz in the logarithmic derivative of the capacitance curve, $dC/d\ln(f)$, as shown in the bottom of Figure 1. This feature is difficult to identify in the raw capacitance spectrum of most samples, although it is well resolved for some devices as shown in Figure 2.
4. At the lowest temperatures, the high-frequency capacitance starts to decrease, as exemplified by the last 5 curves in Figures 1 and 2. For several of the low-temperature absorbers, as shown in Figure 2, this step is unambiguously related to a conductivity freeze-out of the absorber, as the capacitance drops to the geometrical capacitance $C_{\text{geo}} = \epsilon_r \epsilon_0 / d \approx 5 \text{ nF/cm}^2$, which indicates that the absorbers become insulating at these temperatures and frequencies. Although the attribution of this capacitance step to a freeze-out is only possible for some samples, we assume that the nature of this step is most likely the same in all samples due to the similar temperature range.

The activation energy of a process responsible for a capacitance step can be obtained from the temperature dependence of the inflection frequency f_t or, more commonly, the angular inflection frequency $\omega_t = 2\pi f_t$ of the respective capacitance step. We determine the inflection frequency experimentally by finding the maxima in the derivative of the capacitance as a function of the logarithm of frequency, $dC/d\ln(f)$. The simplest form of a thermally activated inflection frequency is given by the equation

$$\omega_t = 2\pi f_t = X_0 e^{-E_a/kT}, \quad (1)$$

where X_0 is a constant. Accordingly, the activation energy is then obtained from a linear fit of $\ln(\omega_t)$ vs inverse temperature $1/T$. One

complication in the analysis arises if the prefactor X_0 is in fact temperature dependent. For a capacitance step due to a defect response, it has been shown that X_0 has a weak ($\propto T^2$) temperature dependence due to the temperature-dependent thermal velocity and effective density of states. The inflection frequency is thus given by the equation⁴

$$\omega_t = 2\pi f_t = v_{th} N_{C,V} \sigma_{n,p} e^{-E_a/kT} = 2\xi_0 T^2 e^{-E_a/kT}, \quad (2)$$

where v_{th} is the thermal velocity, $N_{C,V}$ is the effective density of states in the conduction or valence band, $\sigma_{n,p}$ is the electron or hole capture cross section of the defect, and the prefactor ξ_0 is now assumed to be independent of temperature. The activation energy E_a is then obtained from an Arrhenius plot of $\ln(\omega_t/T^2)$ vs inverse temperature $1/T$.

Although Equation 2 is typically used in the literature, the quadratic temperature dependence of the prefactor is only valid if the capacitance step is indeed caused by a defect response, and if the defect can be described adequately by an ideal defect model. Without a-priori knowledge, we therefore omit any explicit temperature dependence and determine the activation energy based on Equation 1. We find that this approach yields the same trends as Equation 2, but activation energies are typically 10% to 20% higher. Note that the Arrhenius plots appear as straight lines for both Equations 1 and 2, and thus we cannot validate 1 choice of model over the other based on the quality of the fit. Nevertheless, we always use Equation 2 when comparing our results to published data, eg, in Figure 3, to be consistent with conventions in literature.

Figure 3 shows the thermal prefactor ξ_0 as a function of activation energy E_a according to Equation 2, both obtained from a linear fit to the Arrhenius graph of $\ln(\omega_t/T^2)$ vs inverse temperature $1/T$, for all

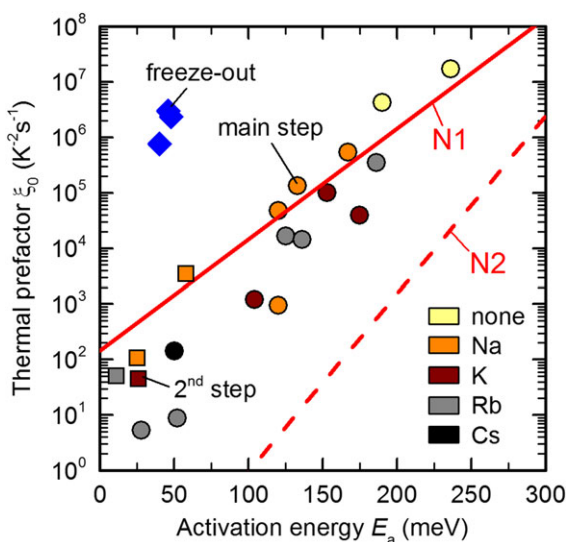


FIGURE 3 Thermal prefactor ξ_0 as a function of activation energy E_a obtained using Equation (2) for all capacitance steps resolved in the admittance spectra of all samples. Shown are the main step (circles), second step (squares), and freeze-out (blue diamonds). The symbol color indicates the alkali species as denoted in Table 1. Lines indicate literature trends for the N1 (solid line) and N2 (dashed line) signatures commonly observed in CIGS, according to values taken from Eisenbarth et al (Ref. 20) and Krysztopa et al (Ref. 34) [Colour figure can be viewed at wileyonlinelibrary.com]

capacitance peaks resolved in this study. The pairs of thermal prefactor ξ_0 and activation energy E_a for a capacitance step originating from the same fundamental thermally activated process are expected to obey the Meyer-Neldel rule and thus follow the relation

$$\xi_0 = \xi_{00} e^{E_a/E_{char}}, \quad (3)$$

with the characteristic energy E_{char} and a prefactor ξ_{00} .^{31–33} Literature trends for Meyer-Neldel lines of the commonly observed N1 and N2 signatures in CIGS are shown in Figure 3 by red lines according to Eisenbarth et al²⁰ and Krysztopa et al.³⁴

It is apparent from Figure 3 that the freeze-out step, as expected, is separate from the other steps and has no relation to the N1 and N2 signatures. Furthermore, the freeze-out, if resolvable from the admittance spectra, always appears at an energy of 55 ± 10 meV. Such an activation energy would be consistent both with a shallow acceptor level typically observed at 40 to 60 meV,³⁵ and with a mobility freeze-out due to transport barriers of approximately 60 mV at the grain boundaries.^{5,35} It is worth noting that we can identify the inflection frequencies of the freeze-out steps only for some of the low-temperature absorbers, not for any of the high-temperature absorbers. The details of the freeze-out mechanism depend on the bulk doping and transport properties across grain boundaries and are thus likely to vary between different absorber processing conditions.

The inflection frequencies of the main capacitance step observed in this study appear to follow the trend of the N1 signature reasonably well, although the scatter in our data is substantial. Such pronounced scatter around the reference line plotted in Figure 3 is fairly common for experimental data attributed to the N1 signature in literature (see, for example, the review in Ref. 34). Attributing a given capacitance step to the N1 signature based on its Meyer-Neldel line is thus inherently ambiguous, due to the large scatter in both the current experimental data and in the reported literature values. Nevertheless, this approach is common practice, and any capacitance signals at least somewhat close to the average N1 Meyer-Neldel line, or even just close to an activation energy around 100 meV, are typically attributed to the same signature. An opposite sign of the N1 peak has been observed in DLTS, compared with typical defect peaks.⁹ Transport barriers discussed in Sections 5 and 6 are indeed consistent with an inverted DLTS signal.^{15,36} Accordingly, our devices certainly show a similar behavior to those reported in literature, but the origin of the “N1-like” behavior must not necessarily be the same for devices reported by other authors. Because we link the main capacitance step to interfaces present in all CIGS devices, see Sections 5 and 6, we propose that our results are likely fundamental to CIGS thin-film solar cells.

Data for the second capacitance step is more challenging to classify. Taking into account the uncertainty in the N1 line from literature, the second capacitance step would still be consistent with the N1 signature. Alternatively, all our data could be fitted by a single Meyer-Neldel line with a characteristic energy of 16 meV, in between the N1 and N2 signatures. Both of these hypotheses appear implausible, as both main step and second step are observed in the same spectrum, and thus most likely have different origins. Although the

identification of the second step remains unsolved, the close proximity of both independent signals to the N1 line highlights the danger of using a Meyer-Neldel-like behavior to attribute different admittance steps to the same defect.

The earlier findings discussed in the Introduction, in conjunction with our observation that both independent capacitance steps are consistent with the same N1 line, warrant a more detailed investigation of the defects in the absorbers and of the transport properties of the solar cells.

4 | DEFECTS IN PHOTOLUMINESCENCE

The difficulties in unambiguously attributing capacitance steps in admittance spectroscopy to defects or transport phenomena calls for an alternative technique to investigate defect states. In PL measurements at low temperatures, defect states within the bandgap can be detected by recording the radiative recombination of photo-generated excess carriers via these defect states. Although defect-related recombination is often assumed to be dominantly non-radiative, PL measurements are highly sensitive to defect states within the bandgap. Indeed, there are several reports of deep defects detected by PL in CuGaSe₂³⁷⁻³⁹ and Cu(In,Ga)Se₂⁴⁰ thin films. Figure 4 shows the PL spectrum at a temperature of $T = 10$ K for an untreated low-temperature absorber. We observe a single emission peak in the energy range of 0.92 to 1.24 eV. This peak is fairly broad, as expected for a Cu-poor absorber,⁴¹ and the “true” peak shape is obscured by interference effects (“dips” in the PL peak).⁴² The PL spectrum clearly demonstrates that no significant PL emission beyond background noise is recorded for energies below the main PL peak, which

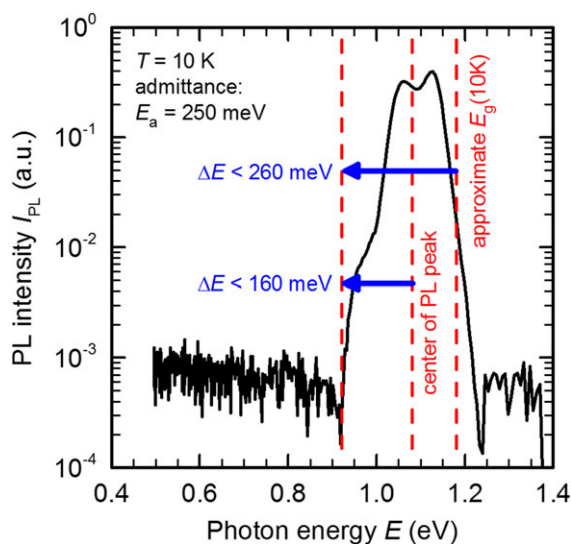


FIGURE 4 Photoluminescence intensity I_{PL} as a function of photon energy E recorded at $T = 10$ K for an untreated low-temperature absorber. The corresponding solar cell showed a main capacitance step with an activation energy of $E_a = 250$ meV. The red dashed lines represent (from left to right) the onset of noticeable PL emission above background noise, the energetic center of the PL emission peak, and the approximate energetic bandgap at $T = 10$ K extrapolated from room-temperature measurements [Colour figure can be viewed at wileyonlinelibrary.com]

corresponds to photon energies $E < 0.92$ eV (left dashed line in Figure 4). From the absence of PL emission, we can conclude that the defect densities in this energy range must be fairly small.

In order to compare electrical and optical measurements, the energetic depth of a hypothetical defect level with respect to the band edges needs to be converted into the photon energy of the corresponding PL transition. This transition energy is shifted from the band-to-band transition energy by the energetic depth of the defect. The bandgap of the chosen absorber was determined to be $E_g = 1.14 \pm 0.01$ eV at room temperature, which suggests a bandgap of approximately 1.16 eV at $T = 10$ K⁴³ (right dashed line in Figure 4). At low temperatures, excess carriers are easily localized in potential troughs caused by spatial potential fluctuations, or in tail states extending from the band edges into the band gap. Furthermore, transitions between shallow dopant levels become dominant compared with direct band-to-band transitions. Accordingly, the dominant PL peak is shifted to energies below the bandgap energy E_g . In first approximation, the energetic position of the PL maximum can be used to estimate the energy difference in the PL transition. Due to the interference effects in our case we estimate the energetic position of the PL maximum by taking the center energy between lower and upper flank of the PL peak, indicated by the center dashed line in Figure 4 at $E = 1.08$ eV.

The absence of PL emission at photon energies below 0.92 eV sets a limit for the energetic depth of defect levels present in significant amounts. Depending on the choice of reference energy of the band-to-band transition (1.08-1.16 eV), the depth of such a defect must be below 160 to 260 meV, as indicated by the blue arrows in Figure 4. Admittance spectroscopy of a solar cell fabricated from an absorber grown in the same deposition run revealed a main capacitance step with an activation energy of $E_a = 250 \pm 25$ meV. On one hand, this value is not directly ruled out by the preceding discussion if the full low-temperature bandgap without potential fluctuations is chosen as reference energy (which results in $E_a < 260$ meV). On the other hand, potential fluctuations are expected in Cu-poor CIGS,⁴¹ which could lower the upper limit to the activation energy. Furthermore, the defect luminescence would need to be sharply peaked to be consistent with the measured spectrum and not extend into the low-energy range.

We obtain similar PL spectra to the one shown in Figure 4 for all absorbers and PDTs, but the high activation energy observed in TAS for this particular sample yields the clearest interpretation. Comparison to the onset of PL emission is more ambiguous for other samples with lower activation energies of the capacitance step. Note, however, that defect signatures lying on the same Meyer-Neldel line are commonly assumed to originate from the same defect. We thus assume that a comparison on 1 particular sample, here with the highest activation energy in TAS, is representative for all samples, because all activation energies and thermal pre-factors lie on the same Meyer-Neldel line shown in Figure 3.

Based on these observations, the PL experiments do not directly refute the possibility that the main capacitance step observed in TAS might be related to defects. Nevertheless, they can be seen as a further hint that alternative interpretations, eg, a transport barrier, might be more appropriate.

5 | TRANSPORT BARRIERS IN THE DEVICE

While deep defects and transport barriers influence the ac response of a solar cell in very similar ways, as discussed in the Introduction (Section 1), transport barriers should be evident from the dc current transport characteristics. Figure 5 shows 2 representative examples of temperature-dependent current-voltage characteristics (*IVT*) measured in the dark for a RbF-treated high-temperature absorber and a NaF-treated low-temperature absorber, respectively.

Despite qualitatively similar ac admittance spectra for all samples, see Section 3, we observe 2 different types of *IVT* behavior: in some samples, the forward current contribution of the main junction, ie, an exponential current increase in forward bias, is largely suppressed at low temperatures [termed “type A”, compare Figure 5A], while other samples show a diode-like forward current over the full temperature range [“type B”, compare Figure 5B]. Accordingly, the low-temperature *IV* curves for “type A” samples are dominated by the shunt current.

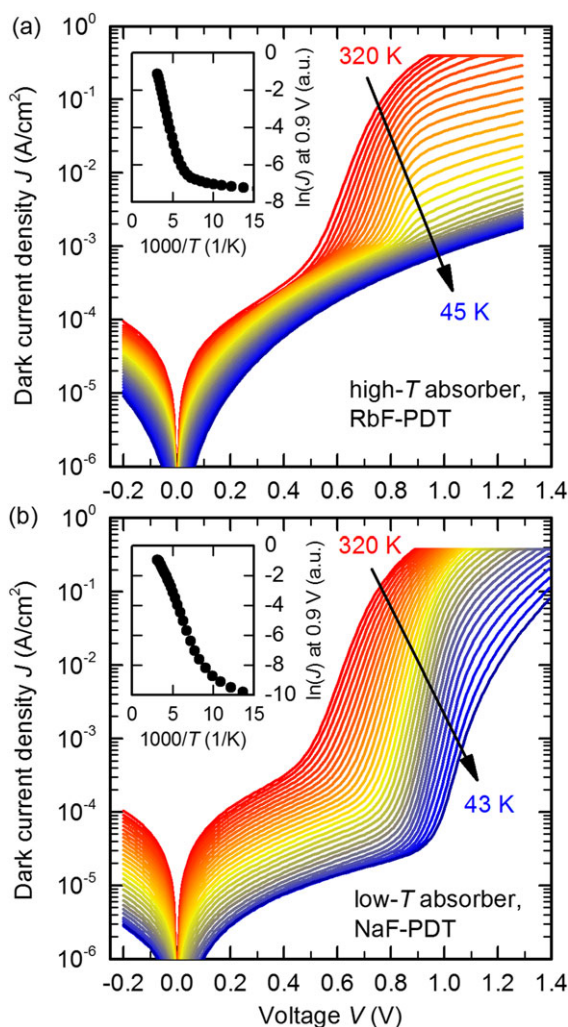


FIGURE 5 Temperature-dependent dark current density vs voltage characteristics for a temperature range of approximately 320 to 45 K for (A) a RbF-treated high-temperature absorber and (B) a NaF-treated low-temperature absorber. The insets show the natural logarithm of the respective dark current density, $\ln(J)$, at a reference voltage of 0.9 V as a function of inverse temperature $1000/T$ [Colour figure can be viewed at wileyonlinelibrary.com]

Below a certain temperature, the dark *IV* curves of these devices no longer exhibit a realistic diode-like behavior: the diode current either disappears completely compared with the shunt current, as exemplified in Figure 5A, or the diode ideality factor increases to unrealistic values well above 10. This transition occurs in a temperature range of 100 to 150 K for our samples, which agrees remarkably well with the lowest temperature where the main capacitance step in the admittance spectra is observed.

We do not find any obvious correlation between *IVT* behavior (A or B) and absorber growth temperature, buffer layer type, or alkali species. Instead, as discussed in more detail at the end of this section, we find that samples with large activation energies in the capacitance spectrum, independent of other sample properties, predominantly show type A behavior with strongly suppressed diode current. Note that the RbF-treated high-temperature absorber representing type A behavior in Figure 5A is the same sample shown in Figure 1 for the admittance spectra.

Both graphs in Figure 5 reveal a significant contribution of shunt currents to the *IV* characteristics. The shunt current decreases, according to increasing shunt resistance, with reduced measurement temperature. The temperature dependence of the shunt resistance at zero bias voltage does not follow a simple thermally activated behavior, resulting in curved Arrhenius graphs. Effective activation energies, estimated from the slope of an Arrhenius graph in a temperature range of 200 to 300 K, thus differ notably between samples. Most values however are in a range of 70 ± 30 meV, which is reasonable for CIGS where up to 3 different acceptor levels between 40 and 150 meV are expected to be responsible for the bulk doping.³⁵ Shunt currents in thin-film solar cells are commonly reported in the literature to be non-ohmic, see Dongaonkar et al⁴⁴ and references therein. Our results are in agreement with these earlier reports, and we obtain shunt current densities J_{sh} roughly obeying a power-law relation $J_{sh} \propto V^m$ with exponent m in the range 1 to 2. Although the 2 samples shown in Figure 5, as well as most samples measured in this study, differ slightly in magnitude as well as voltage and temperature dependence of the shunt resistance, the main difference in forward current stems from a different behavior of the diode current. In Figure 5, this is evidenced by the severe drop of current density measured at voltages above +0.8 V.

For a more quantitative analysis, we look at the dark *IV* curves in high forward bias, where shunt currents are negligible at room temperature. We find that the forward current cannot be adequately described over the full voltage range by a simple analytical model, assuming just a junction diode and ohmic series and shunt resistances. More elaborate device models accounting for transport barriers can certainly be devised and applied to these measurements, but they would necessarily be more complex and contain many free parameters and would thus lead to unreliable fitting results. Accordingly, we do not attempt to extract the fundamental device parameters by fitting the data for all temperatures. We rather discuss the temperature evolution of the shape of the *IVT* curves and compare our observations with numerical device simulations in Section 6. We estimate the blocking of the diode current from the temperature-dependent dark current density at a fixed reference voltage of $V_{ref} = 0.9$ V. This voltage was chosen high enough to ensure a dominant diode current

at high temperatures, but low enough to limit the impact of current saturation at high bias. Our choice of reference voltage is ultimately arbitrary, but the impact on the extracted activation energies appears to be fairly small. For example, even a choice of 1.2 V as reference voltage yields comparable activation energies within a range of $\pm 15\%$. The insets in Figure 5 show the natural logarithm of the corresponding dark current density, $\ln(J_{0.9V})$, as a function of inverse temperature $1000/T$. The current is evidently thermally activated, and the activation energy (circles in Figure 6) is obtained from a linear fit to the data shown in the insets. Data at low temperatures where the forward current starts to level off with temperature, presumably due to the impact of shunt resistance, is excluded from the fit.

An alternative approach to describe the current blocking is by means of the effective series resistance, defined as the inverse slope of the IV curve, $R_s = dV/dJ$, at high forward bias (squares in Figure 6). Here, we again chose a fixed reference voltage, at 1.2 V, in a voltage range where resistive effects clearly limit the diode current. This approach provides a figurative model for the drop in diode current and would be straightforward to implement in a numerical diode model. It is worth pointing out, however, that this effective series resistance is just a model parameter to describe the behavior of the diode current and is different from the "true" ohmic series resistance of the device. This differentiation is obvious from the admittance spectra, where the ohmic series resistance is given by the high-frequency limit of the real impedance. The high-frequency impedance only shows a weak temperature dependence and is below $5 \Omega\text{cm}^2$ for all measurements, much lower than effective series resistance values up to $5 \text{ k}\Omega\text{cm}^2$ for some devices at low temperatures. This clearly indicates that the effective series resistance, as defined above, must have a capacitive component and thus might be related

to a barrier or space charge region connected in series with the main hetero-junction.

Figure 6 shows the correlation between the activation energies of the main capacitance step (x-axis) obtained by ac admittance spectroscopy, of the effective dc series resistance at a forward voltage of 1.2 V (y-axis, squares), and of the dark dc current density at a reference voltage of 0.9 V (y-axis, circles) for samples with different PDTs on both low-temperature and high-temperature absorbers. Colors in Figure 6 represent the alkali species. Most samples exhibit a reasonably good correlation between all 3 activation energies, indicated by the blue line in Figure 6 for a 1:1 correlation. This relation supports our hypothesis that the main admittance step in these samples is indeed related to the transport properties of the solar cell, rather than deep defects in the absorber. Such a suppression of the diode current and a drastic increase in effective series resistance at low temperatures might, for example, be caused by unfavorable band offsets or non-ohmic contacts, which could impede current flow in parts of the device. The impact of the exact nature and location of a transport barrier on the magnitude and voltage dependence of the forward current will be addressed by numerical device simulations in Section 6.

We find that the magnitude of the activation energy determined from admittance or IVT fully determines the type of IVT behavior, as indicated by the red dotted line in Figure 6: devices with activation energies above this line, ie, with high activation energy due to a considerable transport barrier, all show type A behavior with drastic suppression of the forward diode current. By contrast, lower activation energies result in type B behavior exhibiting clear diode-like characteristics even at low temperatures. The critical activation energy for a change from type B to type A IVT behavior in our experiments appears to be around 150 meV.

Despite the good agreement between all 3 activation energies for many samples, we observe deviations for 2 types of samples:

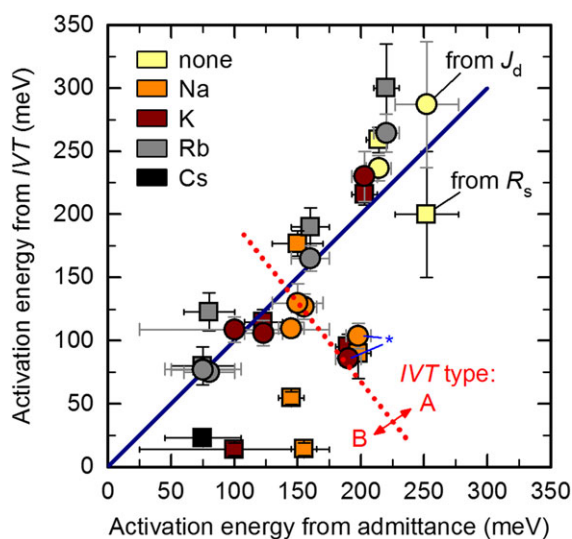


FIGURE 6 Correlation between the activation energies determined from IVT measurements (squares: effective series resistance R_s , circles: dark current density J_d) and from the admittance spectrum. The color code specifies the alkali species, the solid blue line represents a 1:1 correlation. The red dotted line separates devices showing type A and B IVT behavior. Only the activation energies of the main capacitance step are shown for each sample. Data marked with the blue asterisk could be outliers (see main text) [Colour figure can be viewed at wileyonlinelibrary.com]

- For 2 samples marked with a blue asterisk in Figure 6, the activation energies of series resistance R_s and diode current J_d agree remarkably well but are significantly lower than the activation energy of the main capacitance step. One of these samples is likely damaged (zero-bias shunt resistance below $130 \Omega\text{cm}^2$) and thus will be disregarded. For the other sample, the correlation is nearly perfect if the *second* capacitance step is taken as reference instead of the main capacitance step (activation energies approximately: main and second capacitance steps—200 and 80 meV, series resistance—90 meV, diode current—100 meV, respectively).
- For most samples with type B IVT behavior, ie, for capacitance steps with activation energies below 150 meV, the diode current follows the activation energy of the capacitance step, while the activation energy of the series resistance (squares in Figure 6) is significantly lower. Note that this behavior is not universal, and the activation energy of the effective series resistance is only reduced for low-temperature absorbers and a CsF-treated high-temperature absorber, not for any of the other high-temperature absorbers. These deviations suggest that transport properties differ between devices. For example, in low-temperature devices with moderate transport barriers in the buffer/window stack, ie, with low activation energy of the capacitance step, the series

resistance might be dominated by the bulk or back contact, and thus show a different activation energy.

The deviations discussed earlier suggest that different types of barriers might be present in the devices based on processing conditions and alkali species. We also find that the absolute value of the activation energy differs significantly between samples from different fabrication runs, even with nominally the same alkali PDT. For example, using admittance spectroscopy, we obtain activation energies of 80 and 160 meV, respectively, for 2 RbF-treated high-temperature absorbers. These values again indicate that the transport barrier in these devices is fairly sensitive to the processing conditions during device fabrication. Accordingly, our study does not reveal any reliable, systematic dependence on alkali PDT, because variations between samples overshadow any differences due to different alkali PDTs. Although we cannot discern trends between different alkali species, the activation energies found in this study suggest that the transport barrier is largest without any alkali species present and appears to be reduced to varying extent by any alkali PDT.

6 | DEVICE SIMULATIONS

In an attempt to localize the observed transport barrier within the device, we perform numerical device simulations of the current-voltage characteristics of a typical CIGS thin-film solar cell using Synopsys Sentaurus-Tcad. In a first step, we vary the conduction band offsets at the absorber/buffer ($\Delta E_{A/B}$, "A/B") and buffer/window ($\Delta E_{B/W}$, "B/W") hetero-interfaces in order to discriminate between the effects of the respective interface on the *IV* characteristics. In these simulations, current transport is modeled with drift/diffusion equations, and the back contact is assumed to be ohmic. A constant distributed series resistance of $0.5 \Omega \text{cm}^2$ is used at the back contact. In a second step, we employ different transport models at the front and rear of the cell: thermionic emission for electrons across the barrier at the window/buffer interface, and a Schottky contact for holes at the rear contact, respectively. Further details of these simulations are presented elsewhere.⁴⁵ The conduction band edge in the window layer is initially assumed to be continuous, which is representative of a standard ZnO window stack (ZnO:Al + i-ZnO). We then introduce a conduction band discontinuity also within the window stack in order to describe devices with a (Zn,Mg)O layer instead of the standard i-ZnO. Note that our simulation are only exemplary and aim to qualitatively assess trends in the effect of different interfaces on the current transport through the device. Due to the large spread of experimental activation energies, indicating that exact interface properties are likely sensitive to processing conditions, and due to the importance of choosing a suitable transport model, see discussion below, we do not attempt to pinpoint the "correct" quantitative conduction band offsets within a specific real device.

Figure 7A shows the simulated dark *IV* characteristics for a "spike" at the absorber/buffer interface with a conduction band offset of $\Delta E_{A/B} = +0.3 \text{ eV}$ (red dash-dotted line), and a "cliff" at the buffer/window interface with $\Delta E_{B/W} = -0.2 \text{ eV}$ (blue dash-dotted line) and -0.4 eV (blue dashed line). The offset at the other interface and

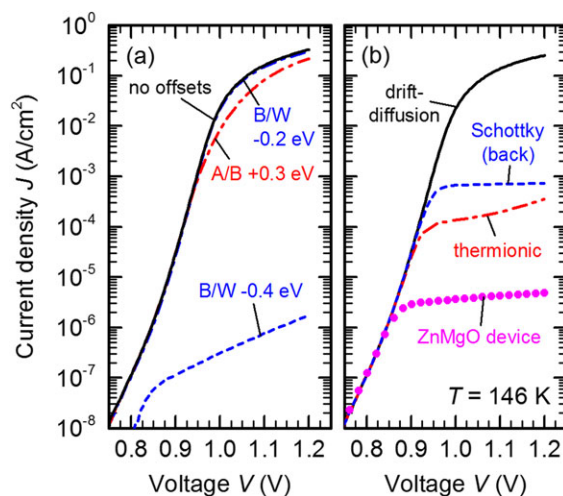


FIGURE 7 Simulated dark *IV* characteristics at a temperature of $T = 146 \text{ K}$ for different barrier parameters. A, Variation of the conduction band offsets at the absorber/buffer interface ($\Delta E_{A/B} = +0.3 \text{ eV}$, red dash-dotted line, "spike"), buffer/window interface ($\Delta E_{B/W} = -0.2 \text{ eV}$, blue dash-dotted line, "cliff"), and without offsets (black solid line). The offset at the other interface is assumed to be zero. B, Drift-diffusion (black solid line) and thermionic emission (red dash-dotted line) model with ohmic back contact and drift-diffusion model with a Schottky contact at the back (blue dashed line). The conduction band offsets are $+0.1 \text{ eV}$ at the absorber/buffer interface and -0.2 eV at the buffer/window interface. Magenta circles represent a device with (Zn,Mg)O intrinsic layer instead of i-ZnO, see Figure 8 for band offsets [Colour figure can be viewed at wileyonlinelibrary.com]

within the window (ZnO:Al/i-ZnO) is assumed to be zero. The solid black line represents the device without any conduction band offsets. The sample temperature is set to $T = 146 \text{ K}$, where experimental *IV* characteristics of all type A devices already show a pronounced suppression of the forward current. The simulations presented in Figure 7A indeed show that both an absorber/buffer spike and a buffer/window cliff can have a limiting effect on the forward current, as observed experimentally.

Simulations of the illuminated *IV* characteristics (not shown here⁴⁵) demonstrate that a conduction band spike at the absorber/buffer interface mainly acts as an extraction barrier, which results in a blocked photo-generated current for voltages below the open-circuit voltage V_{oc} , and thus mainly reduces the fill factor. The absorber/buffer offset $\Delta E_{A/B}$ is thus constrained by the experimental illuminated *IV* curves, which do not show such a loss in fill factor,⁴⁵ and $\Delta E_{A/B}$ cannot be arbitrarily increased to describe the current blocking in high forward bias beyond V_{oc} . The cliff at the buffer/window interface, on the other hand, has virtually no influence on the photo-generated current, and high values of $\Delta E_{B/W}$ cause a dramatic suppression of the forward diode current. Based on these considerations, the transport barrier observed experimentally in *IVT* and admittance measurements is most likely related to conduction band offsets between the different buffer and window layers in the front stack.

The above interpretation has 2 shortcomings: the absolute values of $\Delta E_{B/W}$ required to considerably reduce the forward current are fairly large, significantly exceeding 200 meV, and the curvature of

the IV characteristics in log-scale are not well reproduced by the simulation. We find that both issues can be resolved by the correct choice of transport model. Solid lines in Figure 7B show simulated IV curves at $T = 146$ K in the dark for a moderate choice of conduction band offsets of +100 meV at the absorber/buffer interface and -200 meV at the buffer/window interface. The standard transport model (black solid line: drift-diffusion equations, ohmic back contact) predicts a negligible impact of the conduction band offsets on the IV characteristics, consistent with the simulations in Figure 7A. Alternatively, we model electron transport across the potential barrier at the buffer/window interface based on a thermionic emission process over the potential barrier formed by the CdS buffer layer. This potential barrier is most readily apparent from the conduction band edge profile of an exemplary ZnO:Al/i-ZnO/CdS/CIGS device plotted in Figure 8 at a forward bias voltage of 1.2 V (black dashed line, "ZnO"). The resulting IV characteristics are shown as red dash-dotted line in Figure 7B. Based on the thermionic emission model, small conduction band offsets of the order of 100 to 200 meV already result in a drastically reduced forward current. Furthermore, the forward current increases again after an initial saturation, represented by the upward curvature of the logarithmic IV characteristics in Figure 7B for voltages above +1 V, in agreement with the experimental results shown in Figure 5. The dominant transport barrier observed in our experiments can thus be adequately described by thermionic emission of electrons across a potential barrier of approximately 100 to 200 meV, located in the conduction band within the window/buffer stack.

So far, we have only considered barriers at the front junction. Alternatively, the CIGS/Mo back contact might induce a certain band bending in the CIGS absorber, thus acting as a Schottky barrier at the back contact. We include a Schottky barrier with the Fermi level fixed at 145 meV above the valence band edge at the back contact [blue dashed line in Figure 7B]. This feature causes the diode current to saturate in forward bias, which results in a significant suppression of the forward current even for small conduction band offsets at the front-side of the device. Note that experimentally we do not observe a constant saturation current density in forward bias, and a Schottky contact at the back thus cannot be the sole explanation for the observed transport barrier.

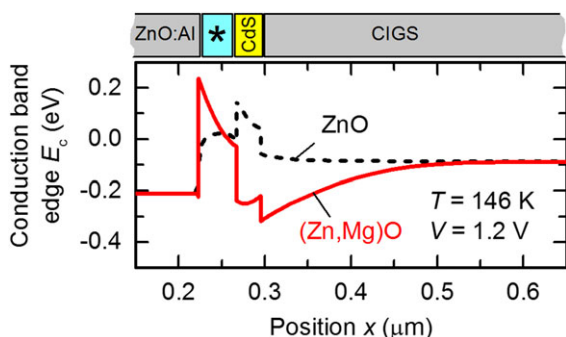


FIGURE 8 Depth profile of the conduction band edge E_c at $T = 146$ K and $V = 1.2$ V for 2 ZnO:Al/i-layer/CdS/CIGS devices with different i-layers: i-ZnO (dashed black line) and (Zn,Mg)O (solid red line). The different layers are indicated above the graph; the asterisk marks the i-layer [Colour figure can be viewed at wileyonlinelibrary.com]

In the preceding simulations, we have assumed a window layer with continuous conduction band, although devices with high-temperature absorber in our study feature a ZnO:Al/(Zn,Mg)O window stack instead of the conventional ZnO:Al/i-ZnO. For this configuration, we expect a cliff of -460 meV⁴⁶ between (Zn,Mg)O and ZnO:Al for a magnesium fraction of $[Mg]/([Mg] + [Zn]) = 0.17$ (closest datapoint to a Mg content of 0.15 for our sputter target). Figure 8 shows the resulting band alignments at a forward voltage of $V = +1.2$ V at $T = 146$ K representative for a (Zn,Mg)O device (red solid line) and an i-ZnO device (black dashed line), where we have assumed an absorber/buffer conduction band offset of +100 meV. Comparing both band alignment profiles, we find that the buffer/window interface in the (Zn,Mg)O device no longer impedes electron injection from the *n*-type contact into the absorber, and thus cannot be responsible for the roll-over of the dark IV curves. However, the blocking interface is now rather located within the window stack, between ZnO:Al and (Zn, Mg)O, resulting in a potential barrier for electron injection similar to the case of ZnO:Al/i-ZnO. The simulated dark IV characteristics of this (Zn,Mg)O device at $T = 146$ K—assuming again a thermionic emission model—are shown in Figure 7B by the magenta circles, and indeed also show a pronounced suppression of forward current. Note that the forward current does not saturate at high voltages, in contrast to a Schottky back contact. In fact, we find an exponential increase at voltages above 1.5 V (not shown in Figure 7) for these parameters, similar to the trend for the i-ZnO device [red dash-dotted line in Figure 7B]. The forward current is significantly reduced compared with a i-ZnO device, because the electron injection barrier is higher due to the high energy of the (Zn,Mg)O conduction band edge for the chosen magnesium fraction of 0.17. For lower magnesium content, the (Zn,Mg)O conduction band edge shifts to lower energies⁴⁶ and the current blocking effect is less severe.

The preceding discussion clearly demonstrates that various types of transport barriers can limit the forward current, and their impact on the current-voltage characteristics depends critically on the exact conduction band offsets and transport model employed in the simulation. Accordingly, small variations in the exact band alignment or material properties, for example caused by differences in composition or intermixing at the interfaces,⁵ will likely result in distinctly different transport properties. Indeed, we find that the experimental type A/B IVT behavior and experimental activation energies differ between samples, even for nominally identical processing conditions, as shown in Section 5. Thus, we have to be aware that the exact band diagram will most likely not be identical for different samples, and that the exact value of activation energies deduced from admittance or IVT measurements will be difficult to interpret correctly. Nevertheless, our simulations qualitatively show that current blocking in forward bias is controlled by an injection barrier for electrons, which impedes flow of electrons from the *n*-doped ZnO:Al across i-layer and CdS into the CIGS absorber. Such an injection barrier takes the form of a conduction band cliff, which could in principle be located at any interface between ZnO:Al and CIGS absorber. For reasonable conduction band energies, we find that the limiting interface is located between i-ZnO and CdS (window/buffer) for i-ZnO devices, and between ZnO:Al and (Zn,Mg)O (window/window) for (Zn,Mg)O devices, respectively.

In both cases, the transport barrier is located within the buffer/window stack and thus formed *after* CIGS growth and alkali PDT. On one hand, any variation or treatment affecting the absorber bulk or surface might still somewhat influence the subsequent growth of the buffer/window stack, and thus modify its actual transport properties. The specific *IVT* characteristics of the device might thus also depend on absorber properties, even if the limiting interface is entirely located within the buffer/window stack. On the other hand, modifications of the absorber surface due to alkali PDT will only indirectly affect the dominant transport barrier, and small variations in the buffer/window stack itself, unrelated to the alkali PDT, could obscure any influence of the alkali elements. This prediction is in agreement with our experimental results in Section 5, where we did not observe any obvious relation between alkali treatments and experimental activation energies obtained from admittance and *IVT* measurements, corroborating that the transport characteristics of the device are mainly sensitive to processing parameters unrelated to the choice of alkali PDT.

7 | CONCLUSIONS

The activation energies of capacitance steps observed in admittance spectroscopy were compared for a wide range of high-efficiency absorbers subjected to different alkali PDTs. The activation energy of a freeze-out at temperatures below 100 K was found to be 55 ± 10 meV, which is consistent with typical values of acceptor levels (carrier freeze-out) or grain-boundary barrier heights (mobility freeze-out). The activation energies and thermal prefactors of capacitance steps occurring at higher temperatures were found to agree reasonably well with the N1 signature established in literature. Remarkably, this agreement was observed even for 2 separate capacitance steps resolved in the same admittance spectra, and thus cannot be attributed to a common defect signature. Photoluminescence spectra recorded at 10 K do not show any significant PL signal at transition energies corresponding to deep defects, and thus confirm that deep defects play a minor role in these devices. Because deep defects are negligible also in untreated absorbers, alkali PDTs do not appear to alter the deep defect concentration significantly.

Temperature-dependent current-voltage characteristics were recorded to study transport barriers in the devices, which revealed a suppression of the forward current at low temperatures in all devices. In many cases, this suppression is drastic, and the *IV* characteristics no longer show an exponential diode-like behavior at low temperatures. The activation energy of the temperature-dependent dark current density at fixed forward bias was shown to correlate with the activation energy of the main capacitance step in admittance spectroscopy. For devices showing a pronounced suppression of the forward current, the same correlation also holds true for the activation energy of the effective series resistance, given by the slope of the *IV* curve in strong forward bias. The shape of the experimental *IV* curves could be reproduced in numerical device simulations by assuming a transport barrier caused by unfavorable conduction band offsets in the buffer/window stack. Our simulations suggest that the *IVT* characteristics in forward bias are most sensitive to a cliff-like conduction band offset of a few hundred meV at the buffer/window interface (eg, for a ZnO:Al/*i*-ZnO window) or within the window stack (eg, for a ZnO:Al/

(Zn,Mg)O window). Thermionic emission over this barrier needs to be taken into account to reproduce the correct shape of the experimental *IVT* characteristics.

Combining all evidence, we find that the main capacitance step observed in admittance spectroscopy for all samples cannot be attributed to a defect but appears to be caused by an electron injection barrier at the front of the device. Due to the reasonable agreement of this capacitance step with reported values for the N1 signature commonly observed in CIGS solar cells, our study provides further evidence to identify the N1 signal with a transport barrier. Such a barrier might originate from a cliff-like conduction band alignment between CdS and ZnO, or between ZnO:Al and (Zn,Mg)O window layers, although we cannot exclude additional transport barriers in the device at different locations. Our experimental results support the prediction of a dominant injection barrier located entirely within the buffer/window stack, because we do not see a consistent trend of activation energies with alkali PDT despite experimental activation energies varying over a range of 70 to 250 meV. Furthermore, nominally identical samples from different processing runs resulted in different activation energies. We conclude that the detailed barrier properties only indirectly depend on the absorber properties and are mainly sensitive to the processing conditions during buffer/window deposition. The effects of alkali treatments in our study are thus difficult to disentangle from small process variations.

Our results highlight that the electronic effects of alkali treatments of CIGS thin-film absorbers—at the moment—are not readily discernable by standard electrical measurements. We find that such measurements are heavily influenced by the buffer/window stack, which modifies or obscures any contribution from the absorber bulk or surface. Accordingly, prevailing models of un-treated and alkali-treated CIGS absorbers need to be carefully reconsidered, taking into account conduction band offsets at the front of the device.

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