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Analog/Digital Hybrid Delay-Locked-Loop for K/Ka Band Satellite Retrodirective Arrays

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***Abstract*—An analog/digital hybrid delay-locked-loop (DLL) phase conjugator (PC) for use in retrodirective array (RDA) applications is proposed, implemented and measured. Compared with previous phase-locked-loop (PLL) PC solutions, the proposed DLL PC has a number of unique features which make it superior to previous solutions in many applications. These features include 1) the ability to hold the phases of conjugated outputs even when input pilots disappear; 2) the ability to track the changing rate of phases of input pilots even when the pilot signals with dynamic phases disappear for a short period of time, i.e., the implemented RDAs can constantly track a moving target for re-transmission even when the incoming pilots are not available due to deep channel fading or time division duplex (TDD) operation; 3) the DLL PC can be flexibly configured as voltage controlled phase shifters for use in traditional phased beam-steering arrays; 4) the DLL PC can indicate direction of arrival (DOA) of incoming signals without recourse to any baseband algorithms; 5) the DLL PC is unconditionally stable. The operation of the DLL PC is articulated in this paper, prototypes are built and their performance and functions are tested. In addition, a K/Ka band RDA demonstrator for satellite communications (SATCOM), based on the proposed DLL PC architecture, is implemented and measured, validating the 'retro-direct' functionality over a wide view angle. To our best knowledge, this is the first time that a DLL has been used for PC, and it is the first time that a K/Ka band RDA based on this technology has been experimentally demonstrated.**

***Index Terms*—Delay-locked-loop (DLL), K/Ka band, phase conjugator, retrodirective array (RDA), satellite communications (SATCOM).**

I. Introduction

A RETRODIRECTIVE array (RDA) has the capability to re-transmit a signal back along the spatial direction(s) along which the array was illuminated by the incoming signals without the need for a-priori knowledge of their points of origin [1], [2]. This automatic tracking characteristic makes RDA technology useful in many applications, including long-range radio frequency identification (RFID) [3], microwave power transmission [4], physical-layer wireless spatial encryption [5]–[7], and mobile satellite communications (SATCOM) [8], [9], etc.

There are a variety of RDA architectures. These largely fall into two categories, i.e., passive and active. Passive solutions normally refer to 'Van Atta' type structures [10], which retrodirect wavefronts using symmetrical delay lines positioned between array radiating elements. While active solutions usually involve phase conjugating circuits [11]. In this category 'Pon'-type phase conjugator (PC) structures [12] have been extensively investigated. These mixer-based arrangements [12]–[15] make the RDA more flexible, in terms of its physical layout [16], receive and re-transmit frequency offsets [17], and re-transmitted signal capability [18]. However, inherent weaknesses associated with this 'Pon'-type approach include low and non-flat mixer conversion gain, undesired mixing frequency leakage components, and lack of receiver array factor gain. These negative attributes have hindered RDA deployment in the field.

These problems have recently been largely solved by introducing phase-locked-loop (PLL) based PCs [19]–[24], which have the capability of providing low spurious phase conjugated signals at constant magnitude. In addition, they have the ability to provide array factor gains on both transmit and receive using simple intermediate frequency (IF) summing circuits.

However, the PLL PC approach is not suitable in some important applications, including the scenarios 1) where the receive signals or pilot tones are not constantly available, which for example may be the result of deep channel fading or time division duplex (TDD) operation, such as are associated with SATCOM systems of the type in [25]; 2) where the information about directions of arrival (DOAs) of incoming pilots are required; 3) where the flexibility of reconfiguring PC units into phase shifters for classical phased arrays is an additional requirement.

Respectively the above weaknesses associated with the PLL PCs are rooted in the fact that the output phase adjustments are achieved by altering the frequency of local oscillators (LOs) during the loop locking process. This leads to 1) frequency

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asynchronization when the incoming pilots, which act as the PLL frequency references, are unavailable; 2) the identical locking status, i.e., frequency synchronization, for different DOAs; 3) no chance of configuring frequency asynchronized PLLs into phase shifters. Naturally if only the phases, rather than the frequencies, of LOs in PLL PC are used to adjust the loop states, the above mentioned inherent PLL PC issues can be sufficiently addressed, and the resulting 'PLLs' are essentially turned into delay-locked-loops (DLLs) [26]. In addition, the proposed DLL based PC architecture can provide significant extra useful features and functionalities when a light touch digital module is utilized.

This paper is organized as follows; In Section II the architecture of the proposed DLL PC is presented, and its unique features are summarized. Detailed DLL PC design considerations are elaborated in Section III. The measured DLL PC performance and the demonstration of its functionalities are provided in Section IV at around 2.2 GHz due to the availability of the off-the-shelf components, while also facilitating performance comparison with previously reported PLL PC solutions. In Section V, an RDA using the constructed DLL PCs deployed for K/Ka band SATCOM applications is constructed. The experiment, for the first time, validates the 'retro-direct' functionality in K/Ka band in a full-duplex fashion. Conclusions on the work presented are finally drawn in Section VI.

II. Delay-Locked-Loop Phase Conjugator

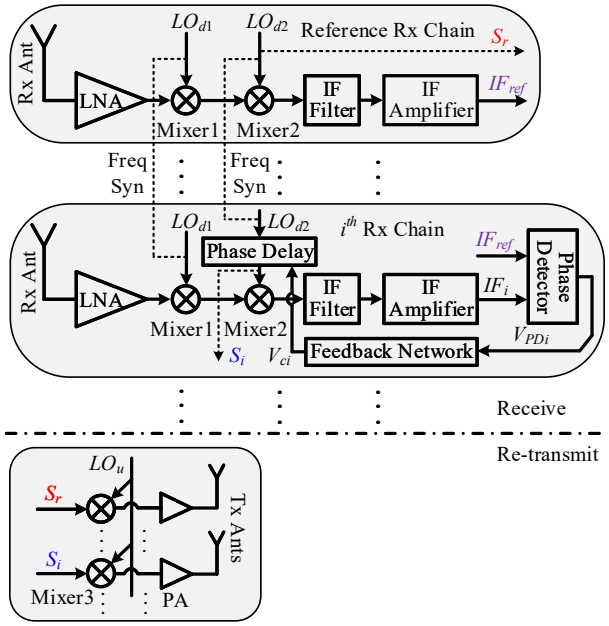

Fig. 1. Proposed DLL PC enabled RDA architecture.

The architecture of the proposed DLL PC enabled RDA is given in Fig. 1. It should be noted that although full digital RDA solutions using FPGA technology can be versatile, they lack real-time response due to their required digital signal processing power and computational speed restrictions [27]. In addition, the full digital version is also power hungry, especially when transmission data rates are high, e.g., at a data rate of 20 Mbit/s, digital and analog versions require 600 mW and 89 mW per element, respectively [27]. In the analog/digital hybrid DLL solution presented here only low-power low-frequency micro-controllers with simple computational capabilities are necessary. They are used in the feedback network shown in Fig. 1. The associated design details are presented in Section III.

In Fig. 1 only the reference and the i^{th} ($i = 2, \ldots, N$) chains are depicted for an N-element RDA. Unlike the PLL PC solutions where LOs in each receive chain used for driving down-conversion mixers, i.e., Mixer1 and Mixer2, are derived from their own frequency references, thereby resulting in phase-unlocked LOs in open loop states, the corresponding LO pairs in DLL PCs share a common frequency reference, i.e., LO_{d1} (and LO_{d2}), and consequently every receive chain in the array is automatically frequency synchronized. Since LO frequencies are fixed, in order to lock the loop in the i^{th} receive chain a controllable phase delay, which can be placed along either the first or the second down-conversion LO paths, is required. In Fig. 1 and the following discussions and in the experimental work presented in this paper this variable phase delay is inserted to alter the phase of the LO_{d2} at the second stage frequency down-conversion.

To facilitate formulation and further discussion, notations of frequencies and phases of various signals involved in the DLL PCs are listed in Table I, from which it is obvious that $f_{in\_ref} = f_{in\_i} = f_{in}$, $f_{d1\_ref} = f_{d1\_i} = f_{d1}$, $f_{d2\_ref} = f_{d2\_i} = f_{d2}$, $f_{u\_ref} = f_{u\_i} = f_u$, and $f_{IF\_ref} = f_{IF\_i} = f_{IF}$.

TABLE I. Notations of Signals in DLL PCs

		Frequency	Phase
Received incoming pilots	The reference chain	f_{in_ref}	ϕ_{in_ref}
	The i^{th} chain	f_{in_i}	ϕ_{in_i}
LO_{d1}	The reference chain	f_{d1_ref}	ϕ_{d1_ref}
	The i^{th} chain	f_{d1_i}	ϕ_{d1_i}
LO_{d2} at input ports of Mixer2	The reference chain	f_{d2_ref}	ϕ_{d2_ref}
	The i^{th} chain	f_{d2_i}	ϕ_{d2_i}
The IF signals	The reference chain IF_{ref}	f_{IF_ref}	ϕ_{IF_ref}
	The i^{th} chain IF_i	f_{IF_i}	ϕ_{IF_i}
LO_u	The reference chain	f_{u_ref}	ϕ_{u_ref}
	The i^{th} chain	f_{u_i}	ϕ_{u_i}

The system should be configured as in (1),

$$f_{IF} = f_{d2} - (f_{d1} - f_{in}), \tag{1}$$

so that

$$\phi_{IF\_\{ref,i\}} = \phi_{d2\_\{ref,i\}} - (\phi_{d1\_\{ref,i\}} - \phi_{in\_\{ref,i\}}). \tag{2}$$

From (2) we can obtain

$$(\phi_{d2\_i} - \phi_{d2\_ref}) = -(\phi_{in\_i} - \phi_{in\_ref}) + (\phi_{d1\_i} - \phi_{d1\_ref}) + (\phi_{IF\_i} - \phi_{IF\_ref}). \tag{3}$$

For the system in Fig. 1 the phase differences between LO_{d1} in the i^{th} and the reference receive chains, i.e., the second term on the right-hand side in (3), are fixed. When the DLL in the i^{th} receive chain is locked, as will be discussed in Section III, the phase difference of two inputs of the phase detector, i.e., the third term on the right-hand side in (3), is constant. As a result, we can rewrite (3) as

$$(\phi_{d2\_i} - \phi_{d2\_ref}) = -(\phi_{in\_i} - \phi_{in\_ref}) + \Delta_i, \quad (4)$$

where Δ_i is a constant for each i.

From (4) it is noticed that the phase ϕ_{d2_i} of the i^{th} DLL output S_i equals the conjugated phase of the incoming pilot, i.e., $-\phi_{in\_i}$, when using their counterparts in the reference chain as references, and when the constant phase $\Delta_i = 0$. The method used to calibrate Δ_i out is discussed in Section III. After the phase conjugated S_i is obtained this can be frequency up-converted to re-transmit, in retro-directive fashion, signals back towards the distant source where the pilot is originated.

The introduction of the DLL PC solution endows the constructed RDAs with a number of desirable capabilities that are not possible with previous PLL PC architectures. These are summarized as follows;

1) The conjugated outputs of DLLs can be held even when the incoming pilots, assuming static phases, disappear. This enables the constructed RDA to continue pointing towards the pilot source direction even when the pilot signals are not available, e.g., due to deep channel fading and/or TDD operation. This is not possible with PLL solutions since when the receive pilots are lost, there is no chance to synchronize the frequencies of LOs in each receive branch as feedback-control DC voltages are lost. Therefore, the re-transmitted directions become arbitrary in terms of both modulation frequencies and spatial beam pointing directions.
2) The conjugated outputs of DLLs can keep tracking the phases of incoming pilots by assuming constant phase rate of change, over a short period when the pilot signals disappear. This endows the constructed RDA the ability of predictively tracking a moving target even when the acquisition pilot radiated from the target disappears, thereby avoiding the repeated phase acquisition processes associated with fading channels and/or TDD systems.
3) The DLL PCs can be configured as variable phase shifters by simply opening the feedback loop in Fig. 1. In this way, the RDA operates as a traditional phased beam-steering array.
4) Unlike PLL solutions, when the DLL PC is locked, the feedback DC voltages, V_{ci} in Fig. 1, used to set required phase delays can be exploited as an indicator of the incoming signal DOA.
5) In order to compensate a fixed phase error, only a first order DLL is required, which is unconditionally stable, compared to a second order conditionally stable PLL required to achieve the same purpose [26].

III. Design Considerations

Before presenting the DLL PC implementation and the RDA experiment in Sections IV and V, some important design considerations need to be elaborated in regard to RDA design for SATCOM application.

A. Receive and Re-transmit Antenna Arrays

In order to broaden the field of view of an RDA, the chosen antennas in both the receive and re-transmit arrays need to have active element patterns with wide beams. Usually microstrip patch antennas are adopted. For some particular applications, such as SATCOM [9], [28], circular polarization is preferred. Receive and re-transmit arrays can share a same antenna aperture, e.g., when receiving and re-transmitting at the same frequency a duplexer is added for system to work in TDD mode, or when frequency-division duplex (FDD) is adopted multi-band or wideband antenna elements are required in the arrays. In FDD mode the conjugated phases need to be scaled according to the receive and re-transmit frequency ratios, as studied in [29]–[31]. Alternatively, receive and re-transmit can use separate antenna apertures with conjugated phases adjusted according to the electric distance between array elements.

B. IF Filter and IF Amplifier

As seen in Fig. 1, an IF filter is added, whose bandwidth is normally around hundreds of Hz, in order to improve receive sensitivity levels associated with SATCOM applications, typically below –120 dBm. Following the IF filter an IF amplifier with high gain is used, in order to drive the phase detector above its threshold voltage at very low received power levels.

C. Phase Detector

There are various types of phase detectors that can be used for the proposed DLL PCs in Fig. 1. Among these the exclusive OR type, which operates effectively with both sinusoid and square wave inputs, corresponding to low and high (saturation occurs after IF amplifier) receive power respectively, is preferred. This amplitude independent characteristic greatly enhances the dynamic range of the receiver. This property is validated in the experiment in the next section.

D. Variable Phase Delay

A controllable phase delay covering 360º is required to alter the phase ϕ_{d2_i} of the LO_{d2} used for the Mixer2, seen in Fig. 1. This phase delay can be directly implemented at the LO frequency f_{d2}, or be implemented at a lower frequency, then multiplied up to the required f_{d2}. In our experiment in Sections IV and V, we choose the latter approach, because 1) a small fraction of phase shifts could span 360º after frequency

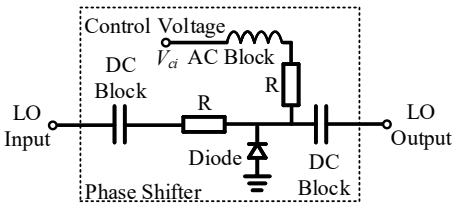

Fig. 2. Voltage-controlled phase shifter at low frequency.

multiplication, so that the most linear region of the variable phase shifter could be selected, 2) the magnitude of the LO_{d2} can be kept constant irrespective of the phase delay. The variable phase shifter at a low frequency, 10 MHz chosen in our experiment, is constructed using the simple circuitry shown in Fig. 2.

E. Feedback Network

The feedback network is the key module that endows the DLL PCs new and useful functionalities, i.e., those described in 1) to 4) in Section II.

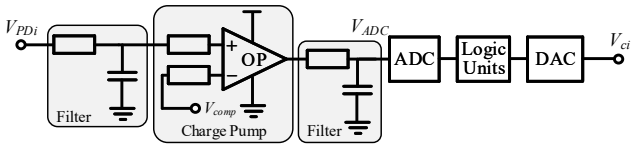

Fig. 3. Schematic of feedback network implementation.

This feedback network used in our design is an analog/digital hybrid circuitry, depicted in Fig. 3. A simple first order loop filter, sufficient to correct phase errors in the DLL, is placed after each phase detector. This is followed by an operational amplifier (OP-Amp) voltage comparator that functions as a charge pump. The reference voltage, V_{comp}, seen in Fig. 3, determines the constant phase differences between IF_i and IF_{ref}, i.e., $\phi_{IF\_i}-\phi_{IF\_ref}$, when the loop is locked. It can be adjusted to make $\Delta_i = 0$, enabling phase conjugation as discussed in Section II. The provision of the V_{comp} provides a simple and effective approach for calibrating each receive chain. The filtered charge pump output is then sampled by a low frequency analog to digital converter (ADC) to allow basic logical operations in the digital domain. Finally, a digital to analog converter (DAC) transforms digital bits back into an analog DC voltage V_{ci}, which is fed back to set the phase delay of the LO_{d2} in the i^{th} receive chain.

The functionalities of the logic units are now described. Here only very basic logic operations are involved, and they can be readily fulfilled with a low-cost low-power digital micro-controller.

1) The array can be easily configured as a traditional phased beam-steering array by selecting from a pre-stored lookup table the digital bits sent to the DAC inputs to generate the DC voltages V_{ci} for required progressive phase delay distributions across the array. In this mode, the feedback loop is opened.
2) For RDA mode, the initial pilot signal phase acquisition is achieved as follows; Scan the input bits of the DAC from **a** to **b** while monitoring the input voltages V_{ADC} of the ADC. Digital bits **a** and **b** correspond to two values of V_{ci} that set two phase delays separated by 360º. Two possible locking points, where middle ranged ADC inputs V_{ADC} are detected, can then be identified. Either locking point can be used. However, this cannot change after selection. Different choices of the locking points result in the different V_{comp} that is tuned to eliminate Δ_i in (4). A phase delay scanning range of greater than 360º may lead to more than two possible locking points and should be avoided.
3) For RDA mode, after successful initial phase acquisition, the digital modules perform the following two tasks;
   - The two digital bits around the locking bit (corresponding to the locking point obtained in the acquisition stage) are repeatedly applied at the input of the DAC. If they lead to high (or low) and low (or high) V_{ADC}, respectively, at the input of the ADC, we know that the locking point is remaining constant. If both lead to either high or low V_{ADC}, we know the input bits of the DAC should be increased or decreased to re-gain the locking point. The new locking bit could be obtained with little effort because it lies not far from the previous locking bit. The changing patterns of the locking bits against time are recorded. It should be pointed out that the phase wrapping issue associated with DLLs can be readily solved with the help of the digital module, because with the availability of the look-up table mapping V_{ci} and phase delays the feedback network knows when and how the phases should be wrapped. As an additional benefit, the knowledge of V_{ci} can provide DOA information.
   - The output V_{PDi} of the phase detector is repeatedly checked. This can be done using another ADC. When the V_{PDi} falls into a pre-determined small region, it indicates the pilot signal disappears. The choice of V_{comp} should be kept far away from this pre-determined region, which is measured and stored in advance, in order to avoid the confusion between the loop locking state and the state when the pilot disappears. Once the system notices the

Algorithm 1

Phase Acquisition:
Sweep input digital bits of DAC from **a** to **b**, until
- For the input bit **c**−1, V_{ADC} is low (or high)
- For the input bit **c**, V_{ADC} is middle ranged
- For the input bit **c**+1, V_{ADC} is high (or low)

c is the locking bit, and go to **Phase Tracking**.

Phase Tracking:
Check locking bit:
1) *If*
- For the input bit **c**−1, V_{ADC} is low (or high)
- For the input bit **c**+1, V_{ADC} is high (or low)

Go to **1)**
2) *Elseif* (For the input bit **c**−1, V_{ADC} is high (or low))
Assign **c**+1 to **c**; Go to **1)**;
3) *Elseif* (For the input bit **c**+1, V_{ADC} is low (or high))
Assign **c**−1 to **c**; Go to **1)**;
Store the previous locking bits versus time.

Pilot Signal Detection:
Repeatedly check the existence of the pilot signal:
If (Pilot signal is unavailable)
Assign **c** according to the patterns of previously stored locking bits;
Elseif
Go to **1)**.

absence of the pilot signal, the DLL will open the loop and assign the input bits of the DAC according to the previously stored patterns of locking bits. So that the constructed RDA can automatically hold the re-transmission direction along the pilot source, or continuously steer the re-transmission beam to track the moving pilot source (when the pilot source is in motion before the pilot disappears) in the period when the pilot signal is not available.

The algorithm used for RDA mode operation, implemented using the digital modules, is now described in Algorithm 1.

In our prototype, we chose the micro-controller PSoC4 [32] from Cypress, because of its low power consumption, easy programming, and its integration of 12-bit multi-channel ADC, two current-type 7-bit DACs, two OP-Amps, and ample logic resources. In other words, it contains all the components that are needed for the feedback network shown in Fig. 3.

IV. DLL PC Prototypes

Prototypes of the proposed DLL PCs were fabricated to evaluate their performance and validate their functionalities.

In order to assess performance, the entire receive chain, shown in Fig. 1, from low noise amplifier (LNA) to output S_i is required. For this purpose, a modular prototype with two entire receive chains was constructed. The inputs of the two chains were directly connected to two 10 MHz phase synchronized signal generators both generating 2.194 GHz signals. One chain was selected as reference, while the S_2 (phase delayed LO_{d2} seen in Fig. 1) in the second DLL PC enabled receive chain was measured. The phases ($\phi_{d2\_2}-\phi_{d2\_ref}$) (after Δ_2 being calibrated out) against the phase differences between two input signals ($\phi_{in\_2}-\phi_{in\_ref}$) were measured and are depicted in Fig. 4 for various input signal power levels. It can be concluded from Fig. 4 that over a large dynamic range of 125 dB (from 0 dBm to −125 dBm) the phases of the input signals can be conjugated using the proposed DLL PC structure with worst case phase errors of less than 14º.

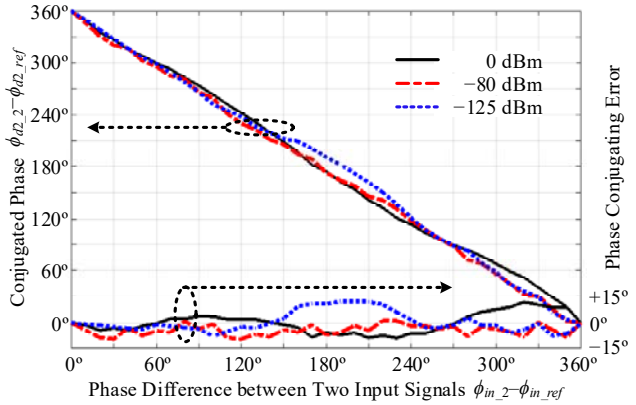

Fig. 4. Phase conjugation experimental results for various receive signal power levels.

During the experiment, the authors identified some sources causing phase errors, which include

1) the spurious and phase noise of the frequency synthesizer, i.e., ADF4360-1 used in the prototype, for LO_{d2} could generate low-magnitude IF signals at the frequency f_{IF} at the input ports of the phase detector, as the results of coupling and circuit non-linearity. The phases of these IF signals do not linearly dependent on the phases of S_r and S_i, affecting the correctness of the calibrated Δ_i in (4), especially when the power of input pilot signals is low, and, hence, the conjugated phases. These resultant IF signals, with unpredictable magnitudes and phases, have different impacts on phase errors when the phase differences of input pilot signals vary. This phenomenon can be more severe when multiple DLL PCs operate closely in space, and this is an important factor that limits the sensitivity of the designed DLL PCs;
2) the resolution and speed of the DAC in the feedback network can affect the phase noise of LO_{d2}. Thus, through the same mechanism described above in 1), phase errors occur.

In order to reduce the phase errors and further enhance the DLL PCs' sensitivity down to −130 dBm, the authors plan to test a series of options, e.g., choosing frequency synthesizers with better spectrum purity and phase noise, redesigning circuit layout to reduce coupling, constructing phase shifters directly at f_{d2} without frequency synthesizers, and selecting high-speed high-resolution DACs with reasonable power consumption. Future results on performance improvement and system integration will be reported timely.

The feedback control voltage V_{c2} was also measured and is plotted in Fig. 5. Once the control voltage V_{c2}, and hence the associated phase difference, is obtained, the DOA θ (measured from the array boresight) can be calculated through

$$\sin\theta = (\phi_{in\_2}-\phi_{in\_ref})\cdot d/k, \tag{5}$$

where k is the wave number in free space, and d is the antenna spacing. In Fig. 5 it can also be seen that the voltage can be automatically wrapped when the pre-defined boundaries, e.g., 0.7 V and 1.2 V (corresponding to the DAC input bits **a** and **b**) used in the above experiment, are reached, indicating

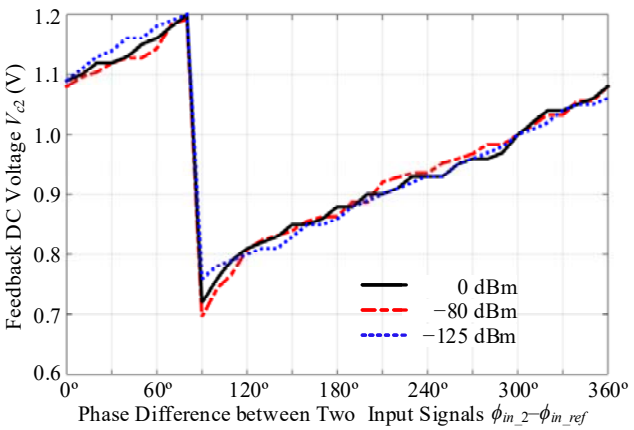

Fig. 5. Measured feedback DC voltage V_{c2} against phase differences ($\phi_{in\_2}-\phi_{in\_ref}$) between two input signals for various input signal power levels.

TABLE II. INFORMATION ABOUT IMPLEMENTED DLL PC ENABLED K/KA BAND RDA AND ITS FREQUENCY SETUP

	Components	**Notes**
Rx antenna array	IMST-designed 1-by-4 microstrip patch array	See photograph in Fig. 6; LTCC technology; Element spacing: 10.5 *mm*; Polarization: RHCP.
Tx antenna array	IMST-designed 1-by-4 microstrip patch array	See photograph in Fig. 6; LTCC technology; Element spacing: 7 *mm*; Polarization: LHCP.
LNA	CHA2092B	
Mixer1	HMC292	Measured conversion gains at 20 GHz were around 12 to 14.5 dB @ −15 dBm input.
Mixer2	MAX2680	Measured conversion gains at 2.2 GHz were around 7 dB @ −60 dBm input.
Mixer3	HMC329	Measured conversion gains at 29.75 GHz were around 8.5 to 13.5 dB @ −10 dBm input.
PA after Mixer3	CHA2092B	
IF amplifier	Two LMH6646	
Phase detector	SL74HC4046	
Frequency synthesizer for LO_{d2}	ADF4360-1	
Frequency setup	f_{in} = 20 GHz; f_{d1} = 22195.81 MHz; f_{d2} = 2.2 GHz; f_u = 31.7 GHz[a]; f_{Tx} = 29.5 GHz[b].	

a. f_u denotes the frequency of LO_u used for up-conversion before transmission.
b. f_{Tx} denotes the frequency of signals fed into transmit antennas, here $f_{Tx} = f_u - f_{d2}$.

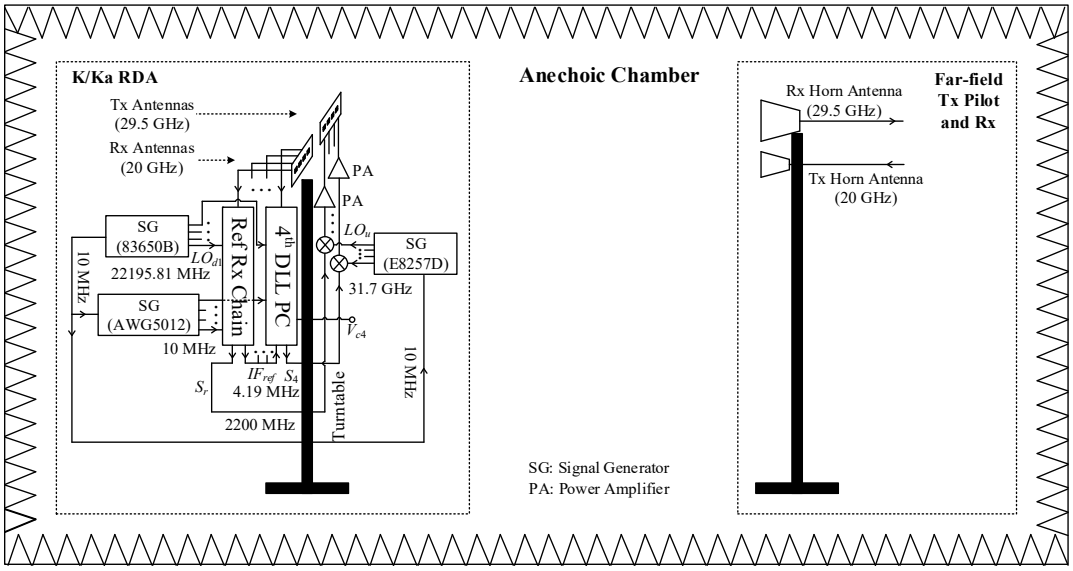

Fig. 6. Block diagram of DLL PC enabled K/Ka band RDA experiment setup.

continuous phase tracking ability unconstrained by the limited phase range of the phase delay circuitry.

Next, four integrated DLL boards targeting for K/Ka band SATCOM applications were designed and fabricated. For function demonstration purpose, one reference board and one DLL board were measured. Here the frequency of the input signal, which is the signal before the Mixer2 in Fig. 1, and the f_{d2} were set to be 2195.81 MHz and 2.2 GHz respectively, resulting in f_{IF} = 4.19 MHz.

The video of the experiment can be accessed in [33]. In the video, it can be seen that

- The DLL works for both continuous wave (CW) and QPSK modulated (PN sequence) input signals;
- The DLL can hold the phases of the output signals when the input signals with static phases disappear. This confirms the claim 1) in Section II;
- The DLL can continuously track the phases of the input signals even when the input signals with changing phases disappear for a short period of time. This confirms the claim 2) in Section II.

V. DLL PC ENABLED K/KA BAND RDA

A fully functional K/Ka band RDA based on the proposed DLL PC was designed and assembled. We chose K/Ka band because RDA equipped ground terminals can provide great benefits for the fast-growing K/Ka band satellite broadband

connections [28], e.g., RDA user transceivers on moving vehicles can automatically beamform towards the target satellites.

The detailed design information about the DLL PC enabled K/Ka band RDA is provided in Table II.

The block diagram and the photograph of the DLL PC enabled K/Ka band RDA experiment setup in an anechoic chamber are shown in Fig. 6 and Fig. 7, respectively. In Fig. 6, the DLL PC module has the same structure as that shown in Fig. 1, except for the LO_{d2} which is generated using the frequency synthesizer ADF4360-1 (sharing a common 10 MHz reference). The reference receive chain is similar to the DLL PC module, but without the feedback network and the phase shifter. Measured monostatic pattern of the RDA re-transmissions is given in Fig. 8. With repeated measurements and individual antenna test, we noticed that the ripples on the measured and calculated monostatic patterns were mainly caused by the unwanted radiation from coaxial cables connecting antenna elements and RF circuits. Thus, smoothed fitting curves are also provided in Fig. 8. This issue will be fixed in the future by integrating antennas and RF circuits on a single board.

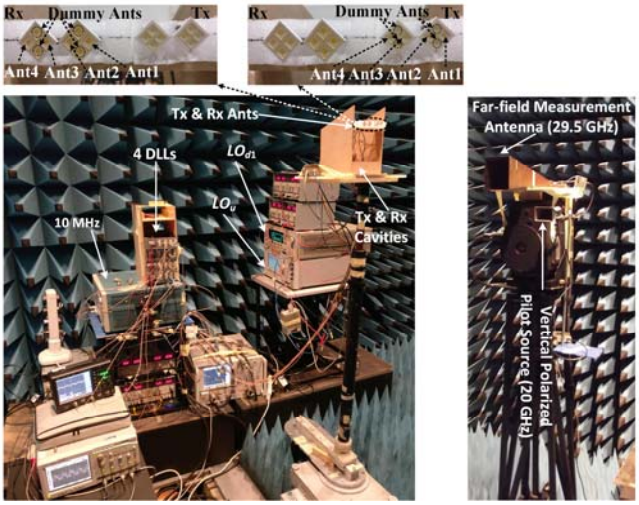

Fig. 7. Photograph of DLL PC enabled K/Ka band RDA experiment setup.

In Fig. 8 it can be clearly seen that the implemented K/Ka band RDA was capable of retrodirecting the pilot source over a wide spatial range, i.e., from −50° (or −55°) to 40° (or 50°) for gain flatness of about 3 dB (or 5 dB). The calculated monostatic pattern, obtained using measured antenna active element patterns, also plotted in Fig. 8, has slightly higher gains when compared with its measured counterpart. This is mainly caused by the non-ideally calibrated Δ_i in the monostatic pattern measurements, leading to beam pointing errors and reduced beamforming gains [34]. It is noted that when wider steering angles are required, other types of antenna elements with broader active element patterns and/or other array arrangements, e.g., curved arrays, can be considered.

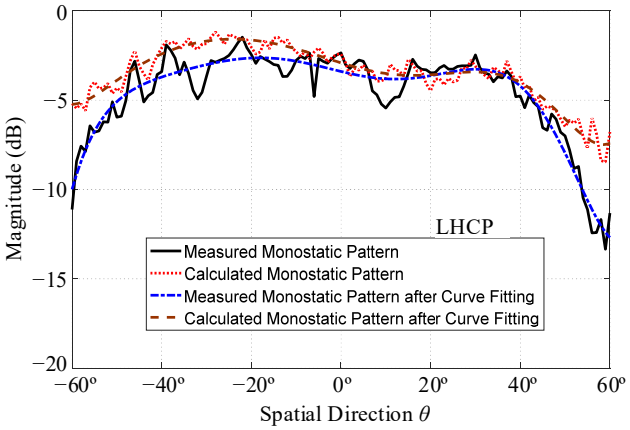

Fig. 8. Comparison between the measured RDA monostatic pattern and calculated monostatic pattern. Receive at 20 GHz and re-transmit at 29.5 GHz.

VI. Conclusion

In this paper, we have proposed a new type of phase conjugating architecture based on an analogue/digital hybrid DLL. The proposed DLL PC solution has a number of useful features that are not available with the previously reported PC solutions. The prototypes of the DLL PCs, and its first ever K/Ka band RDA demonstrator, were successfully implemented and measured to assess their superior phase conjugation performance, e.g., the large input dynamic range of 125 dB and the input signal sensitivity down to as low as −125 dBm, and to validate their unique functionalities, such as holding or tracking the conjugated phases even when the incoming pilots are lost. The proposed analog/digital hybrid DLL PCs should find many applications where robust and flexibly reconfigurable RDA/phased array deployment are required.

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