PROCESS AWARE ANALOG-CENTRIC SINGLE LEAD ECG ACQUISITION AND CLASSIFICATION CMOS FRONTEND

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भारतीय प्रौद्योगिकी संस्थान हैदराबाद

Indian Institute of Technology Hyderabad

Department of Electrical Engineering

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Declaration

I declare that this written submission represents my ideas in my own words, and where ideas or words of others have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources that have thus not been properly cited, or from whom proper permission has not been taken when needed.

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Approval Sheet

This thesis entitled "**Low Power Process Aware Analog-Centric Single Lead ECG Acquisition & Classification CMOS Frontend**" by Pankaj Kumar Jha (EE10P007) is approved for the degree of Doctor of Philosophy from IIT Hyderabad.

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Dedication

To my parents

Prof. Dr. Chiranjiv Jha & Mrs. Nirmala Jha

(प्रोफ. डॉ. चिरंजीव झा और श्रीमती निर्मला झा)

Abstract

The primary objective of this research work is the development of a low power single-lead ECG analog front-end (AFE) architecture which includes acquisition, digitization, process aware efficient gain and frequency control mechanism and a low complexity classifier for the detecting asystole, extreme bardycardia and tachycardia. Recent research on ECG recording systems focuses on the design of a compact single-lead wearable/portable devices with ultra-low-power consumption and in-built hardware for diagnosis and prognosis. Since, the amplitude of the ECG signal varies from hundreds of μV to a few mV, and has a bandwidth of DC to 250 Hz, conventional front-ends use an instrument amplifier followed by a programmable gain amplifier (PGA) to amplify the input ECG signal appropriately. This work presents an mixed signal ECG fronted with an ultra-low power two-stage capacitive-coupled signal conditioning circuit (or an AFE), providing programmable amplification along with tunable 2^{nd} order high pass and lowpass filter characteristics. In the contemporary state-of-the-art ECG recording systems, the gain of the amplifier is controlled by external digital control pins which are in turn dynamically controlled through a DSP. Therefore, an efficient automatic gain control mechanism with minimal area overhead and consuming power in the order of nano watts only. The AGC turns the subsequent ADC *on* only after output of the PGA (or input of the ADC) reaches a level for which the ADC achieves maximum signal-to-noise-ratio (SNR), hence saving considerable startup power and avoiding the use of DSP. Further, in any practical filter design, the low pass cut-off frequency is prone to deviate from its nominal value across process and temperature variations. Therefore, post-fabrication calibration is essential, before the signal is fed to an ADC, to minimize this deviation, prevent signal degradation due to aliasing of higher frequencies into the bandwidth of interest and hence capture the ECG signal accurately. However, none of the ECG front-ends reported so far include an on-chip automatic frequency tuning technique to calibrate the low pass 3-dB frequency. To alleviate this short coming, a fully on-chip ultra-low power automatic frequency tuning (AFT) mechanism is proposed. Moreover, the proposed AFC reuses the hardware in the signal chain to reduce the area overhead of the overall system. Next, a low power discrete-time (DT) $\Sigma\Delta$ ADC is incorporated for digitization. The $\Sigma\Delta$ modulator topology is preferred over the conventionally used low power successive approximation register (SAR) ADC because of the easy resolution reconfigurability offered by it, apart from the other regular benefits. An opamp-shared DT $\Sigma\Delta$ ADC is implemented using a single integrator, and can be reconfigured to provide first or second order noise-shaping with an effective number of bits (ENOB) of 6 or 10 bits, respectively. The high/low resolution reconfigurability allows the subsequent DSP, used

for classification of ECG signals, to switch to low resolution processing, hence saving power and enhances battery lifetime. Another short-coming noticed in the literature published so far is that the classification algorithm is implemented in digital domain, which turns out to be a power hungry approach. Moreover, Although analog domain implementations of QRS complexes detection schemes have been reported, they employ an external micro-controller to determine the threshold voltage. In this regard, finally a power-efficient low complexity CMOS fully analog classifier architecture and a heart rate estimator is added to the above scheme. It reduces the overall system power consumption by reducing the computational burden on the DSP. The complete proposed scheme consists of (i) an ultra-low power QRS complex detection circuit using an autonomous dynamic threshold voltage, hence discarding the need of any external microcontroller/DSP and calibration (ii) a power efficient analog classifier for the detection of three critical alarm types viz. asystole, extreme bradycardia and tachycardia. Additionally, a heart rate estimator that provides the number of QRS complexes within a period of one minute for cardiac rhythm (CR) and heart rate variability (HRV) analysis. The complete proposed architecture is implemented in UMC 0.18 μm CMOS technology with 1.8 V supply. The functionality of each of the individual blocks are successfully validated using post-extraction process corner simulations and through real ECG test signals taken from the PhysioNet database. The capacitive feedback amplifier, $\Sigma\Delta$ ADC, AGC and the AFT are fabricated, and the measurement results are discussed here. The analog classification scheme is successfully validated using embed NXP LPC1768 board, discrete peak detector prototype and FPGA software interface.

Chapter 1

Introduction

1.1 Introduction

Advances in CMOS technologies, communications, and low power circuit design techniques have given impetus considerable research in devices intended for the acquisition of biopotential signals e.g. electrooculography (EOG), electroencephalography (EEG), electrocardiogram (ECG), electromyography (EMG) and axon action potential (AAP). Biopotential signals exhibit amplitude and bandwidth ranges of a tens of μV to tens of mV , and from DC to few kHz, respectively as shown in Fig. 1.1 [1]. The abbreviation ECG (or EKG) stands for electrocardiogram, which in turn has its root

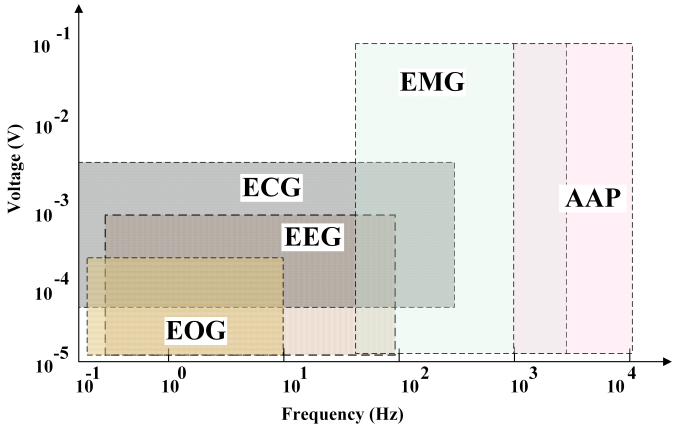


Figure 1.1: Approximate range of amplitudes and bandwidth of different biopotential signals.

in the Greek language - 'electro' indicates electrical activity, 'cardio' indicates heart and 'gram' indicates to write (here record). The amplitude and timing of this electrical activity is recorded by

an EKG. Moreover, ECG is hailed as the gold standard for detecting cardiac arrhythmias since it is a non-invasive technique and at times can be the sole marker for the presence/occurrence of heart diseases. Resulting from the depolarization and polarization of the heart, it exhibits four major deflections viz. P, Q, R, S and T. The sequence and duration of these deflections are depicted in Fig. 1.2 [2, 3]. The P wave represents the depolarization of the atria. Proliferating from the sinoa-

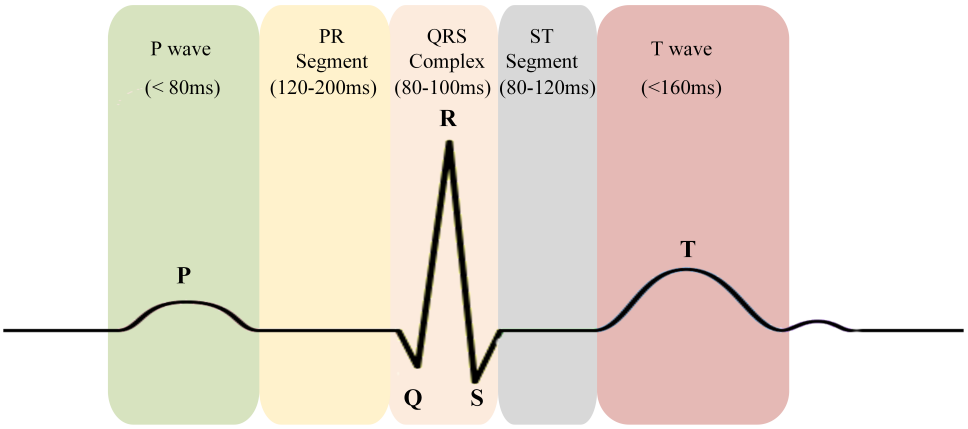


Figure 1.2: Sequence of deflections and their time duration in a normal ECG rhythm.

trial (SA) node, the atrial depolarization spreads towards the atrioventricular (AV) node, and from the right atrium to the left atrium. The PR segment represents the time it takes for the electrical impulse to propagate from the SA node through the AV node. The QRS complex reflects the swift depolarization of the right and left ventricles. Since the ventricles have larger muscle mass vis-à-vis the atria, the QRS complexes normally have a much larger amplitude than the P-wave. The ST segment represents the interval when the ventricles are depolarized. Each of the deflections and the intervals between them have a typical time duration, a range of magnitudes and dissection. Deviations from these standard shape is considered potentially pathological and hence clinically significant. Due to the advancement in technology, both the equipment recording the ECG signal and the human understanding of the ECG's morphology and pathology have evolved significantly over time.

1.1.1 Evolution of ECG Recording Systems

The major clinically pertinent landmarks in the journey of the ECG equipment's from 'bench to bedside' is compiled chronologically in Fig. 1.3 [4–10]. The physiological background is outlined

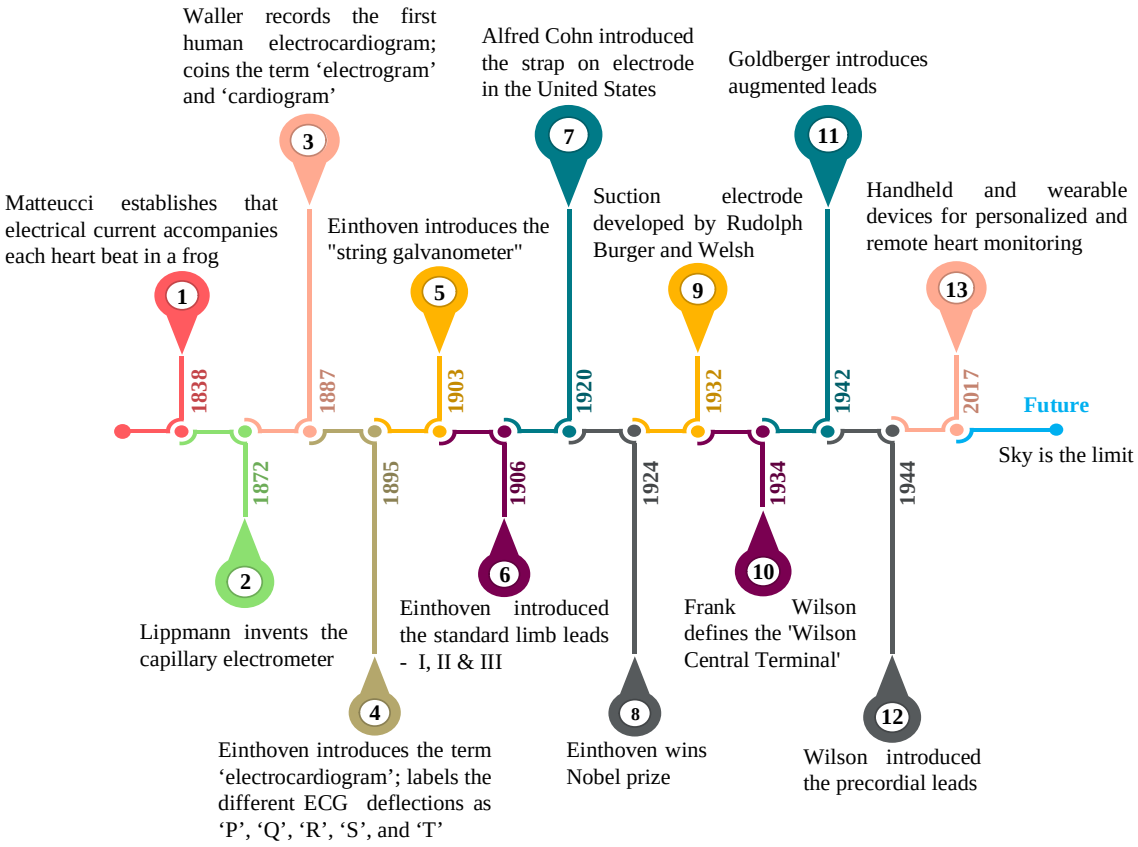


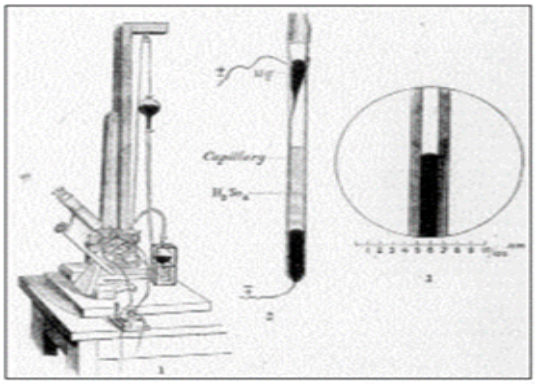
Figure 1.3: Timeline of major events in the evolution of ECG analysis recording.

below.

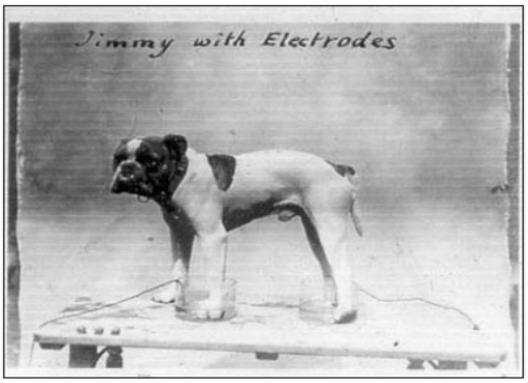
- **1838**: Carlo Matteucci (Professor of Physics, University of Pisa), demonstrated that each beat from a frog's heart is accompanied by an electric current. Working with Nobili's astatic galvanometer and an arrangement called a 'rheoscopic frog', he used the cut nerve of a frog's leg as the electrical sensor to study the electrical activity in muscles.

- **1872**: Gabriel Lippmann (Franco-Luxembourgish physicist and a Nobel laureate) invented the capillary electrometer, a glass tube containing a mercury with sulphuric acid on top (shown in Fig. 1.4a). Observed through a microscope, the movement of the meniscus of the mercury reflects the variation in the cardiac electrical potential.

- **1887**: Augustus Desirè Waller (British physiologist at St Mary's Medical School, London) recorded and publishes the first human electrocardiogram. Fig. 1.4b shows his famous bulldog Jimmy, used by Waller to demonstrate his techniques. With Jimmy standing with its paws (working as electrodes) in saline water, Waller showed that the variations in the potential



(a)



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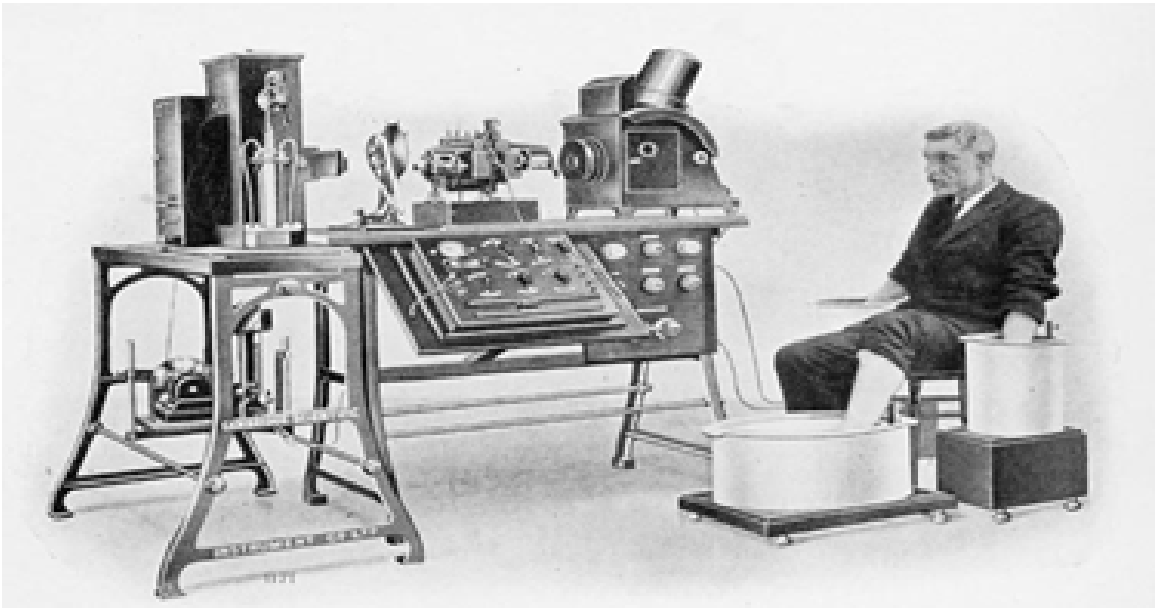
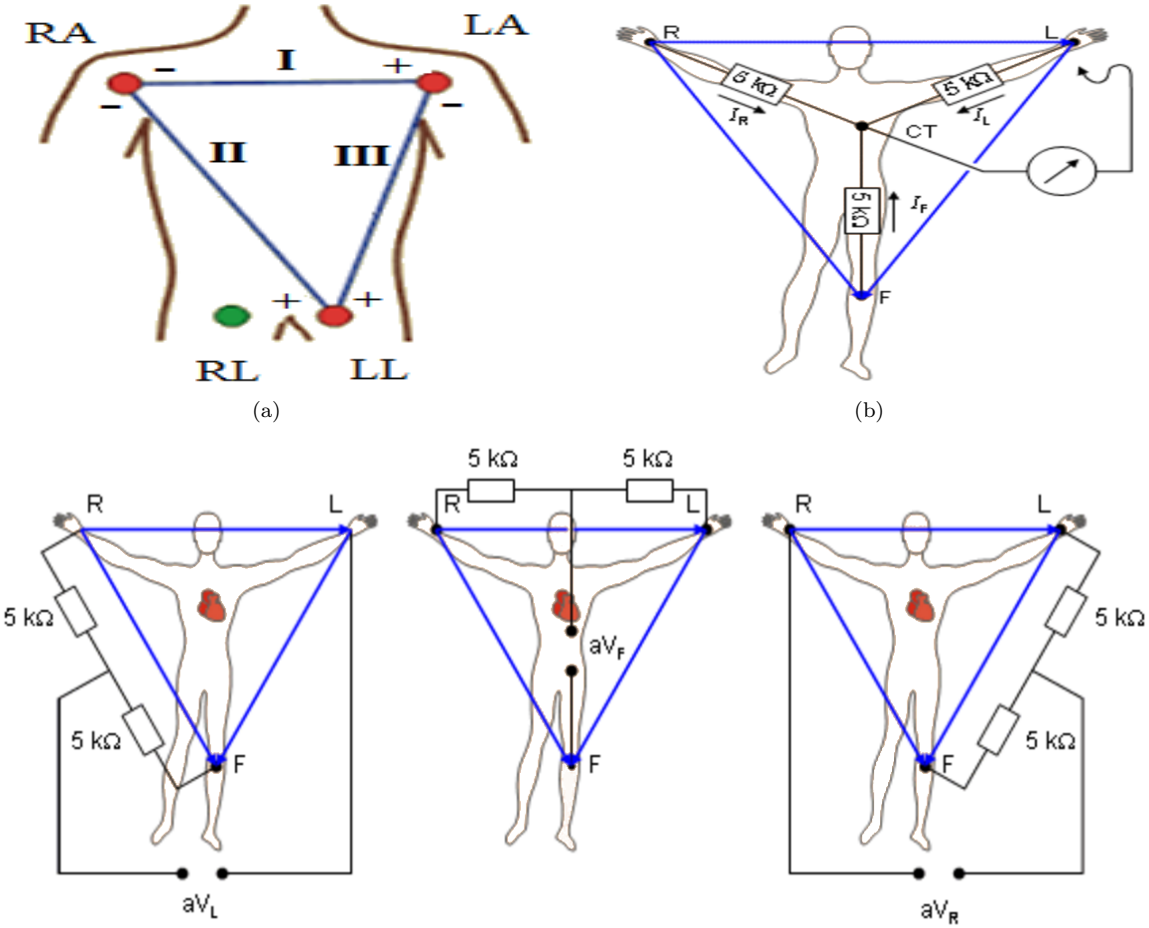


(c)

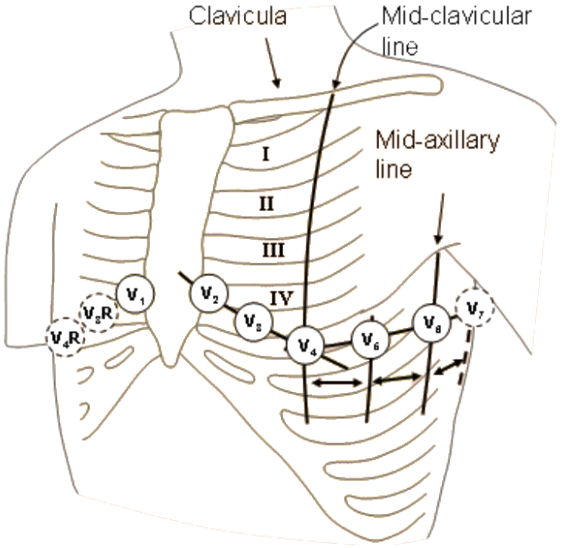
Figure 1.4: Early ECG recording techniques (a) Lippmann's capillary electrometer, (b) Waller's demonstration of his technique by recording the electrogram of his bulldog Jimmy, (c) Einthoven's string galvanometer.

difference pulsated with Jimmy's heart beat. He also coined the terms 'electrogram' and 'cardiogram'.

- **1895**: Marking the birth of clinical electrocardiogram, Willem Einthoven (Dutch physiologist) labeled the five distinct deflections as 'P', 'Q', 'R', 'S' and 'T'. It is interesting to note the labeling does not have much scientific significance. It simply follows the conventional mathematical tradition of labeling successive point on a curve, but using letters from the second half of the alphabet starting from the letter 'P'. The letters, 'N'and 'O', have been avoided because the former has other meanings in mathematics and the latter is generally

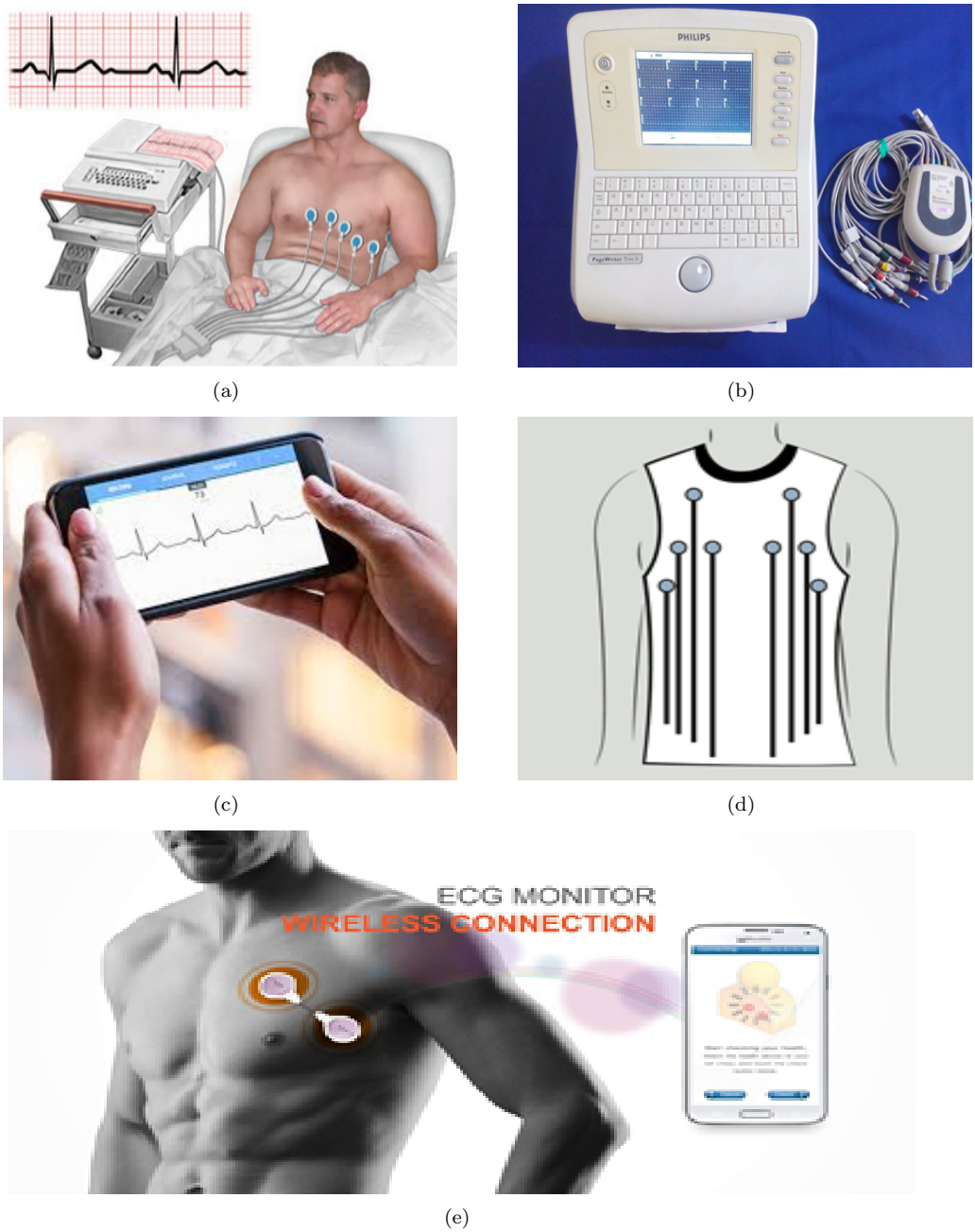


(a) (b) (c)



(d)

Figure 1.5: Definition of ECG electrode leads (a) Standard limb leads - I, II, and III , (b) Wilson central terminal, (c) Goldberger's augmented leads, (d) Wilson's precordial leads (chest leads).



(a) (b) (c) (d) (e)

Figure 1.6: Transformation of ECG sensing, recoding and analysis equipment (a) Traditional 12-lead ECG machine in a hospital, (b) Philips pagewriter trim-II ECG machine with ECG paper and chest electrodes clips, (c) Smart phone based device (d) Wearable vest (e) ECG patch

used to denote the origin of the Cartesian coordinates.

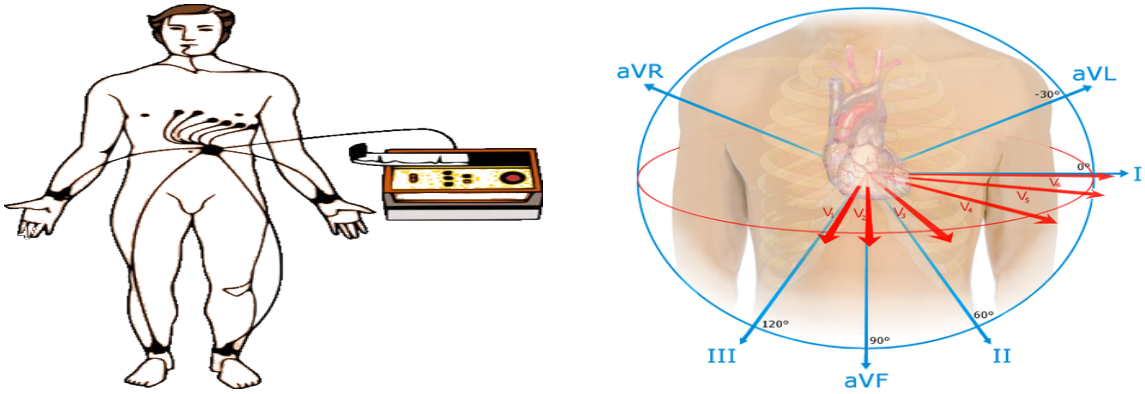
- **1903**: Einthoven introduced the 'string galvanometer'(shown in Fig. 1.4c), a three lead EKG machine, commercial built by Cambridge Scientific Instrument Company.

- **1906**: Einthoven introduced the standard limb leads - I, II and III as shown in Fig. 1.5a.

- **1920**: Alfred Cohn introduced the strap on electrode in the United States.
- **1924**: Willem Einthoven won the prestigious Nobel prize for inventing the first practical electrocardiogram in 1903.
- **1932**: Suction electrode, presently a part of the standard 12 lead ECG machine, was developed by Rudolph Burger and later modified by Welsh.
- **1934**: Dr. Frank N. Wilson (University of Michigan) defined the 'Wilson Central Terminal', an additional terminal at the center of the Einthoven triangle (shown in Fig. 1.5b) [10].
- **1942**: Dr. Emanuel Goldberger (Lincoln Hospital, New York) introduced the augmented leads (shown in Fig. 1.5c) [10].
- **1942**: Wilson proposed the precordial/chest leads . As shown in Fig. 1.5d, these leads, V1-V6, are located over the left chest [10].
- **Present**: Traditional bulky 12-lead ECG recording machines (shown in Fig. 1.6a) [11] are swiftly being replaced by compact portable commercially available machines now (shown in Fig. 1.6b). Smart phone based devices with ECG recording and processing capabilities are easily available at affordable prices. Apart from the information on the heart rate of the subject, they also involve FDA-cleared automatic algorithms with medical grade figure of merit for the detection of atrial fibrillation, e.g. Alivcor with 98% sensitivity and 97% specificity, AfibAlert with accuracy 94.6% (shown in Fig. 1.6c) [12–17]. Further, smart digital ECG-sensing wearable vests have also marked their presence in the market, e.g. Smartex and HealthWatch (shown in Fig. 1.6d) [18,19]. Moreover, convenient, comfortable, medical grade, cloud-based, and wireless continuous ECG recorders are also gaining popularity (shown in Fig. 1.6e) [20, 21].
- **Future**: e-prescribing (e-Rx) [22] , Telemedicine [23] , eHealth [24], mHealth [25], u-Health [26], etc. Sky is the limit.

1.1.2 Emergence of 2-Electrode Handheld ECG Monitoring Gadgets

Traditionally the ECG is recorded using the standard 12-lead system as shown in Fig. 1.7a. It involves ten electrodes to facilitate twelve different perspectives integrated together to create a cohesive ECG interpretation depicted in Fig. 1.7b . While nine out of the ten electrodes are responsible for sensing electrical signals, the tenth electrode (on the right leg) is driven by the ECG circuit to eliminate



(a) (b)

Figure 1.7: Standard 12-lead ECG recording (a) Clinical measurement, (b) Different views of the cardiac activity

common-mode interference noise. The nine sensing electrodes comprises left arm (LA), right arm (RA), left leg (LL), and six precordial electrodes (V1 through V6). The definition of electrodes for 12-lead ECG measurement is given in Table 1.1. With more number of electrodes, this method of recording provides more information for more accurate subsequent analysis of the condition of the heart, specially for cases where detection of heart attacks (myocardial infarctions) is critical. At the same time, the system is bulky, expensive, usually stationed at a hospital or healthcare center, and hence unsuitable for long term and unsupervised monitoring [27, 28].

Table 1.1: Definition of electrodes for 12-lead ECG sensing

Electrode #	**Lead**	**(-) Electrode**	**(+) Electrode**	**View of the heart**
1	Lead I	RA	LA	Lateral
2	Lead II	RA	LL	Inferior
3	Lead III	LA	LL	Inferior
	aVR	LA+LL	RA	None
	aVL	RA+LL	LA	Lateral
	aVF	RA+LA	LL	Inferior
4	V1			Septal
5	V2			Septal
6	V3			Anterior
7	V4			Anterior
8	V5			Lateral
9	V6			Lateral

The advancement in the integrated circuit (IC) and communication technology, evolution of smart phones, and proliferation of the applications based on Internet-of-Things (IoT) and cloud computing have paved way for a paradigm shift in the diagnosis and treatment of cardiac diseases

Table 1.2: Traditional 12-lead ECG vis-à-vis personalized 2-electrode monitoring

	12-lead	**Single lead 2-electrode**
No. of electrodes	10	2 (no ref. elect., comfort)
Portability	No (bulky)	Yes (handheld, gadgets)
Location & utility	Hospitals and health centers (unsuitable for long term, (unsupervised monitoring)	- Routine monitoring, - Personal, home, and sports recording (not used for serious diagnosis)
Cost	Expensive	Affordable
Information	More (Accuracy α no.of electrodes) Can detect heart attacks attacks (myocardial infarctions)	Limited (extract hear rate , HRV analysis) - Cannot detect heart attacks (myocardial infarctions) - Mainly used for detection of atrial fibrillation and heart rate estimation

lately. Breaking from the long-established hospital centric ECG diagnosis which aims solely at intervention and curing the illness, contemporary and futuristic methods intend to facilitate patient centric monitoring, aiming early detection and prevention of the disease. Latest affordable handheld, wearable and patch ECG sensors need of lesser number of electrodes i.e. five, three, or two. Although these devices are not intended for critical abnormalities, e.g. myocardial infarctions, they have proven to be an efficient option where the prime intent is to extract the heart rate, heart rate variability (HRV) analysis and detection of atrial fibrillation. Table 1.2 summarizes the prospects, advantages and disadvantages of using a twelve lead vis-à-vis a two electrode ECG monitoring system [29]. Fig. 1.8 illustrates the concept of a cloud based wireless and continuous ECG recording and analysis system [30–33]. Even a remote patient can record his ECG conveniently using two electrodes paired with a smart phone. The smart phone is capable of displaying the recorded ECG signal and then transmit the ECG data from anywhere in the world to a cloud server. All the processing is done in the cloud server and is relayed to a physician. The physician then delivers the diagnosis and prescription back to the subject over the smart phone. An alarm signal can also be sent to the nearest ambulance and the subject's family in case an emergency. Predominantly, the handheld device for ECG sensing is a three or two electrode system.

A standard single lead three electrode ECG front-end is shown in Fig. 1.9, e.g. the ADS129x (a low power, 8-Channel, 24-bit analog front-end for bio-potential measurements from Texas Instru-

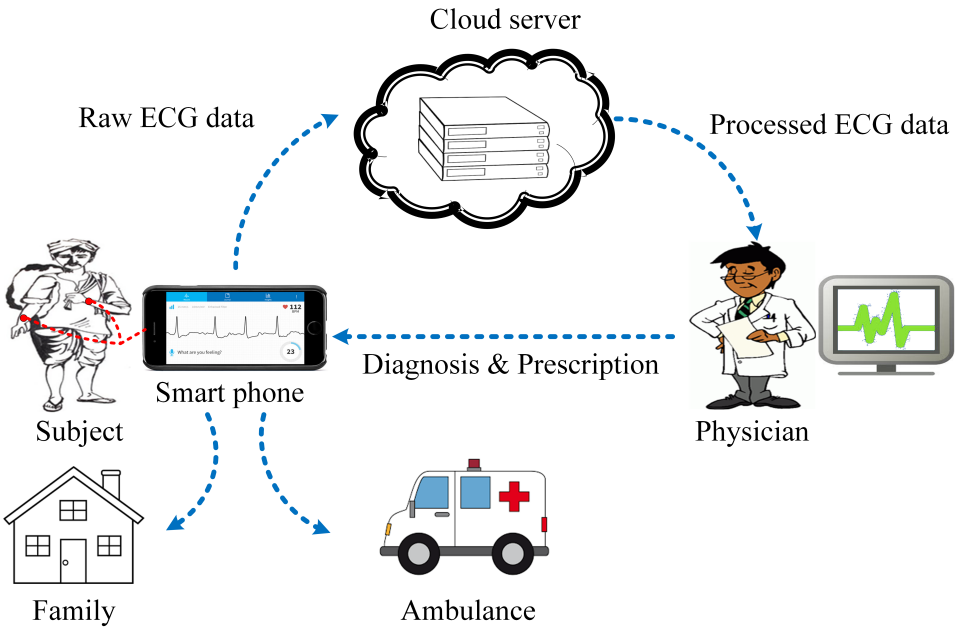


Figure 1.8: Cloud based remote ECG monitoring and alarm system.

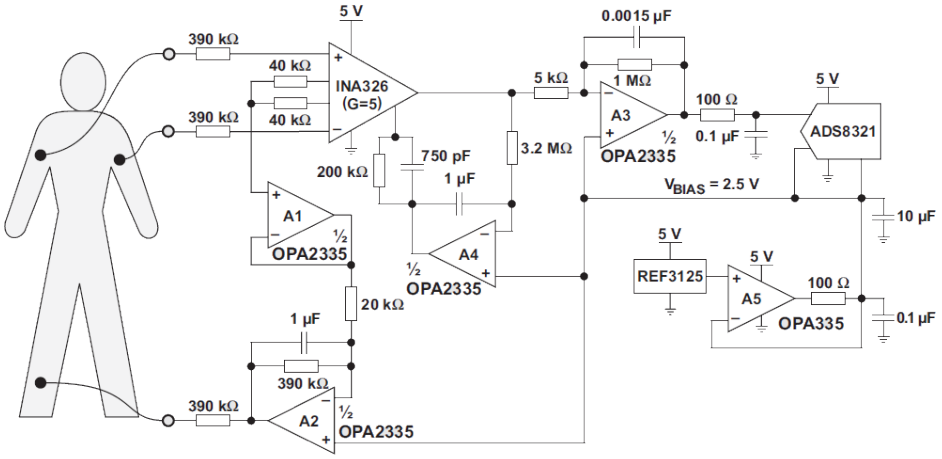


Figure 1.9: Three electrode front-end for portable ECG monitoring from Texas Instruments.

ments) and AD8232 (single-lead, heart rate monitor front-end from Analog Devices) [34–36]. Out of the three electrodes, two electrodes (left and right arm, LA and RA) sense the differential ECG signal and the third (right leg drive, RLD) is used as a reference to bias the patient at the same potential as the monitoring system. The right leg drive improves the common-mode rejection ratio (CMRR) of the circuit to reduce the effect of the electromagnetic interferences which the human body can pick up, especially the 50/60 Hz noise from electrical power lines [37]. This configuration allows three views Lead I, Lead II and Lead III as shown in Fig. 1.10. This set-up can be made

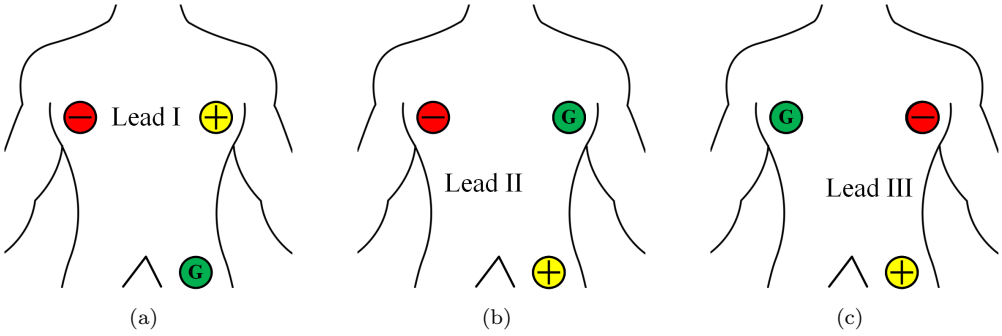


Figure 1.10: Three electrode configuration (a) Lead I, (b) Lead II, (c) Lead III.

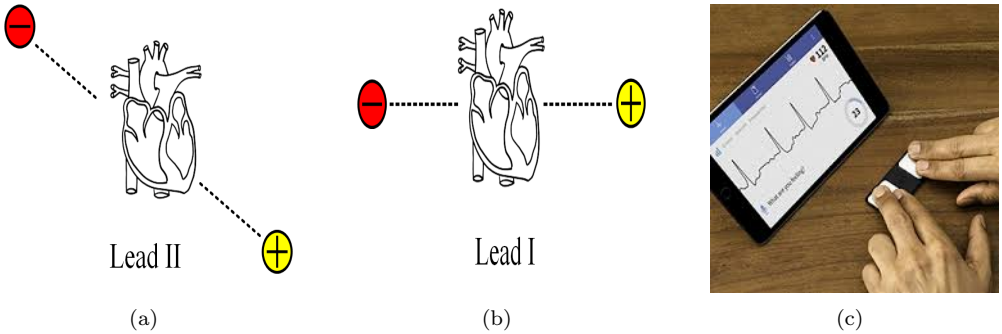


Figure 1.11: Two electrode configuration (a) Lead II, (b) Lead I, (c) Commercially available ECG sensing and recording.

more convenient for the patient by discarding the RLD electrode, although at the cost of making the measurement more vulnerable to noise [38, 39] . The resultant set-up is a two electrode configuration, generally employed by latest handheld gadgets available in the market. Despite the fact that the Lead II set-up (Fig. 1.11a) provides the maximum amplitude of the ECG signal, Lead I set-up (Fig. 1.11b) is more popular for portable gadgets (Fig. 1.11c) owing to the greater comfort of the patients while placing the electrodes [40]. Moreover, an essential aspect of two electrode ECG sensing is the possibility to replicate the electrocardiogram produced by a 10-electrode from a two-electrode electrogram. Correlation coefficient averaged over all of the leads of 0.988 has been reported [41–43]. Furthermore, the same front-end circuit used to find Lead I, e.g. ADS1298, could be used to extract Lead II and Lead III information. There is no difference in terms of acquisition circuit. The scope of application for such a device is not limited to the detection of cardiac arrhythmia only, but have been lately extended in the field of biometrics and forensic sciences [44–47].

1.2 Aim and Motivation

The World Health Organization has recognized cardiovascular diseases (CVD) as the number one killer globally and calls for a mechanism for its early detection and management using counseling and medicines [48, 49]. With cancer placed second in the present list of most fatal diseases globally, the trend is estimated to continue through 2030 [50]. [51] distinguishes CVDs not only as a health issue, but also as an economic burden. It indicates that the global cost spent on CVDs will increase from $863 billion in 2010 to $1044 billion in 2030. Direct healthcare cost (money paid directly to the doctor or hospital) and productivity losses (money lost due to absence from work or mental strain) comprises 55% and 45%, respectively, of the $151 per capita cost globally.

1.2.1 CVDs : Indian Scenario

Zeroing-in to the scenario in India, CVDs top the list of most fatal diseases, as shown in Fig. 1.12. They also score the top rank amid different causes of death across any social classification of the population, e.g. economically backward states, economically forward states, rural, urban, men, women, middle age (25-69 yrs.) etc. [52]. The prime challenges in managing the problem of CVDs are summarized in Fig. 1.13. They can be broadly classified into three categories, viz. low availability, low accessibility and low affordability.

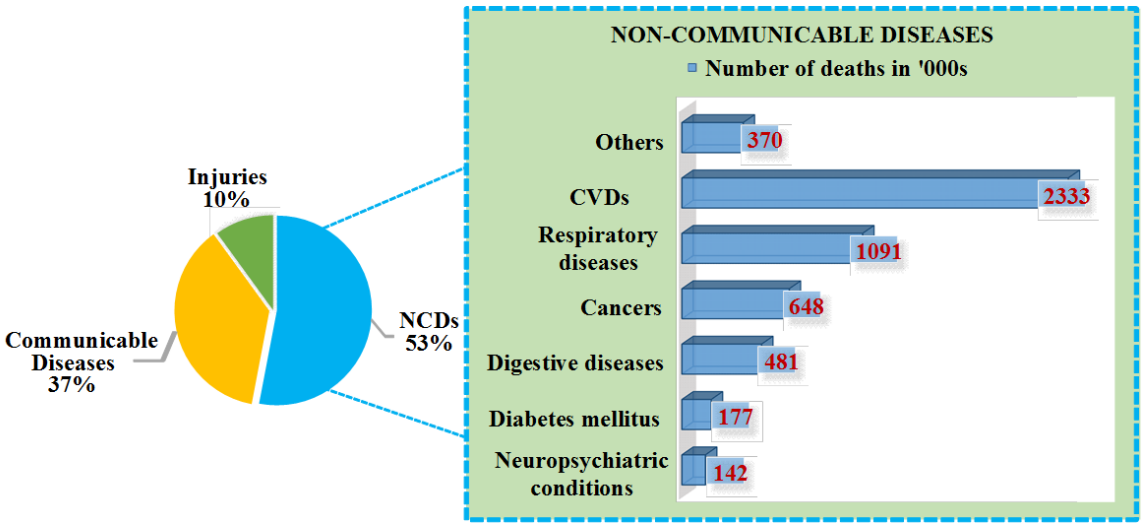


Figure 1.12: Causes of death in India, 2008.

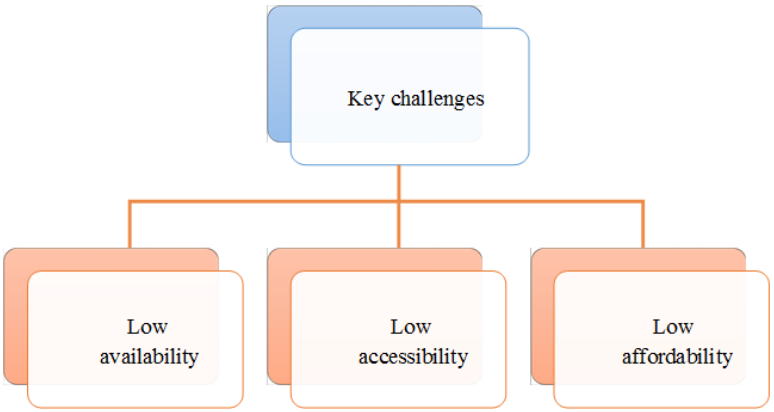


Figure 1.13: Classification of major challenges in managing the menace of CVDs in India.

Low Availability

Low availability pertains to the inadequate and inefficient infrastructure and trained personnel necessary for preventive and curative cardiac care at all levels in India. Few of the facts which have resulted in the abysmal condition of cardiac healthcare services in India are as follows [53–56]

- One doctor for every 1700 people in India
- India produces less than 30,000 doctors every year
- India trains only about 150 cardiologists every year
- Greater than 60% shortfall of specialists at the community healthcare centers level
- Only 4,000 cardiologists ,1,200 cardiac surgeons in a population of over 1.2 billion
- Shortfall of about 600,000 doctors and 1,000,000 nurses to reach the WHO recommended standard of 1 doctor for every 1000 people
- In 2010, mere 5.0% of GDP was spent on healthcare (less than any BRIC nation), out of which the government share was merely 0.9%
- Ranked 145 globally, the per capita health spending in India is sheerly $132, vis-à-vis $8632 in US
- India's annual healthcare expenditure is barely $77 billion,vis-à-vis $300 billion in China

Low Accessibility

Low accessibility refers to the inequitable access to healthcare services in India. Approximately 60% of the hospitals in India are located in the urban areas and cater to only 30% of the total population. Moreover, a mere 13% of the villagers have access to a primary healthcare facility and less than 10% to a hospital. While 92% of the doctors render their services in urban areas, leaving only 8% for the villages [57]. The primary healthcare centers can play a pivotal role in early detection and prevention of non-communicable diseases. But, the primary and secondary healthcare centers lack the necessary infrastructure and trained staff for this task, which in turn increases the burden of patient flow on tertiary centers. This huge imbalance in the population and limited accessibility needs to be addressed urgently.

Low Affordability

Finally, low affordability is concerned about the fact that majority of India's population belong to lower and middle income class with meager spending power. [58] estimates that the poor, lower, middle, upper and rich class comprises of 35%, 43%, 19%, 1% and 1%, respectively in 2015. It also predicts that the corresponding percentages would be 22%, 36%, 32%, 9% and 2% by 2025, leaving the economic condition of the majority population disheartening. The situation is further aggravated by the exorbitant cost of treatment in hospitals in Tier I cities, low penetration of health insurance especially in rural areas, no insurance coverage for preventive or diagnostic or any outpatient care, . As a result, 74% of total health spending in India was out-of-pocket (OOP), with only 14% of the population being covered by some form of health insurance. Money spent on chronic diseases consume up to 70% of the average monthly salary of people in the low income group, and nearly 45% in the highest income group. Around 28% of all diseases in the rural areas go untreated due to financial constraints. The wrath of the expensive treatment of cardiac diseases is often catastrophic for urban poor and rural people who get entangled into a vicious circle. Suffering from chronic economic backwardness, unhealthy living conditions, and mental stress, they tend to involve in unhealthy habits like smoking and drinking. This leads to the early onset of cardiac diseases among them. Social stigma and little awareness, besides poor access to healthcare and high cost of treatment, compel them to ignore the disease. It is compounded by the fear of losing wages due to absence from work. Finally, the hefty amount of OOP payments pushes 39 million Indians into poverty every year.

1.2.2 ECG Systems : A Paradigm Shift from Hospital-Centric to Patient-Centric Monitoring

In a nut shell, the majority of the Indian population cannot afford preventive cardiac care services making them vulnerable to higher risks in the future. Nearly 69% of the population residing in villages and the dismal condition of the rural healthcare due to an inadequate and inequitable infrastructure and trained medical staff calls for the development, installation and proliferation of remote wireless self-powered ECG monitoring systems [59]. The recent popularization of the pervasive, predictive, preventive, and personalized healthcare ECG monitoring systems in the global healthcare market has given impetus to the design of miniaturized, ultra low power and self-powered front-ends. The exponential reduction in cost per function enabled by ever advancing IC technology (delivers low-power and high-performance microcontrollers and radios available at cheap cost), advent innovative sensor technologies, deep perforation of broadband across all strata of the society, and market pull for wearable biomedical devices has fostered the development of devices for non-invasive physiological monitoring of various bio-potential signals in residential or other non-clinical environments. A similar drift has ushered in an era of Internet of Things (IoT), i.e. the stationing of applications comprising of distributed sensors and actuators communicating among each other. Further, connected personal healthcare (eHealth, mHealth, u-Health, e-Rx, Telemedicine, etc.), calls for the development of wireless body sensor networks (WBSN) to collect and analyze multiple bio-signals in a users daily routine. Numerous multi-chip prototype solutions for WBSN applications are already available, but they suffer excessive power dissipation and are comparatively bulky. To cater to the diverse signals in a cost-effective way, a universal platform integrating various wearable biomedical sensors, power harvesting module, signal acquisition and digitization block, local low-power processing unit and low-power radio. The battery size is limited by the size and weight constraints long-term power autonomy. While a large battery increases the form factor of the SoC (making it unwearable or unobtrusive), a small battery requires frequent replacement and reduces wearer convenience. Reduction in the power dissipation is achieved through employing of one or all of the following techniques (i) lowering supply voltage (ii) minimizing data rate through feature extraction or data compression (iii) duty-cycling transmitter with the help of on-chip memory, and (iv) employing impulse radio ultra-wideband (UWB) transmitter for better power efficiency. Hence it is desirable to extract the required power thermal, vibrational or solar energy harvesting techniques. [60] reports a wireless body area network powered by RF energy harvesting. Besides these traditional sources, the far field radio frequency identification (RFID) power can also be har-

vested. [61] has demonstrated that it is possible to create a battery with $6\mu W$ of received RF power. The largest share of power in a WBSN is consumed by the wireless transceiver. Apart form using low-power microcontrollers, it is desirable to minimize the use of the transceiver by transmitting information instead of raw data and duty-cycling of the same by triggering the transmission only when it is deemed necessary based on cardiac analysis. Therefore the ECG sensor node ought be capable of performing preliminary ECG signal analysis like QRS detection and RR interval estimation locally. The integrated solution in the form of a custom System-on-Chip (SoC) presents an viable solution w.r.t its small form factor, light weight (for portability), performance, lower power consumption (for long battery life) and node operating lifetime. Notable research effort is directed towards making it low profile, unobtrusive, user friendly, and with long battery life for continuous usage, without compromising on medical grade signal quality (even under high levels of physical activity) and multi-sensor support with sufficient on-chip signal processing performance. In a SoC various sensors are attached on clothing (wearable textile) or implanted in human body (bioinformation node, or BIN), the different biosignals acquired thereof are stored, locally processed jointly before transmission to a central base-station node (i.e., mobile phones, PCs ,or the cloud). In short, the SoC based solutions are facilitate the monitoring of patients suffering from CVDs at any time and place.

1.2.3 Literature Review : Recent ECG Monitoring Systems

Several SoC based systems for ECG monitoring have been realized in standard CMOS processes. A self-powered multi-sensor SoC comprising four integrated on-chip sensors and a smart wireless acquisition system is reported in [71]. Powered from dual-input (solar and RF) energy harvesting, it is capable of processing different types (C, R, I, and V) of sensor signals through a linear (R-square is 0.999) and reconfigurable switched-capacitor circuit sensor readout. An ECG SoC solution with a full-custom hardware media access control (MAC), digital microprocessor core and I/O peripherals, on-chip memory, micropower third order 10-bit switched opamp $\Sigma\Delta$ ADC, wireless transceiver and custom sensor interfaces is presented in [72]. It is capable of supporting a number of different types for monitoring applications including: glucose/pH using amperometric sensors, motion using a 3-axis accelerometer, heart rate/ECG (EKG) using a single lead electrode, temperature using thermistors, pressure using a Wheatstone bridge. [73] presents a true ECG-on-chip solution SoC implemented in asynchronous architecture, which does not require system clock as well as off-chip antenna. It introduces a DC-coupled analog front-end together with a baseline stabilizer to

boost the input impedance to 3.6 GΩ and mitigate the electrode offset, targeting the dry-electrode based applications. Taking advantage of the burst nature of ECG signal, a level-crossing analog-to-digital converter (LC-ADC) and a digitally implemented impulse-radio ultra-wideband transmitter are employed. Low-power microcontrollers, e.g., programmable interface controller or programmable intelligent Computer (PIC) and MSP430 (a mixed-signal microcontroller family from Texas Instruments), etc. and are not an efficient choice because of their limited functionality and speed. At the same time, more powerful DSPs [74] are too power consuming and thus unsuitable for a low power biomedical SoC. Hence, a low-power microcontroller core with a limited but few carefully-selected DSP features are desirable. The design in [75] presents a fully integrated sub-1V 3-lead wireless ECG SoC for wireless body sensor network applications. The SoC includes a two-channel ECG front-end with a driven-right-leg circuit, an 8-bit SAR ADC, a custom-designed 16-bit instruction set architecture (ISA) microcontroller, two banks of 16 kB SRAM, and a transceiver operating in medical implant communications service (MICS) band. Equivalently, [76] utilizes a customized 4-way single instruction multiple data (SIMD) processor based DSP responsible for controlling the configurability, motion artifact removal and R peak detection. Its analog front-end extracts 3-channel ECG signals and single channel electrode-tissue-impedance (ETI) measurement. The 12-bit ADC meant for digitizing the acquired signals is capable of adaptive sampling achieving a compression ratio of up to 7, reducing the power consumed in accessing the on-chip memory. The multisensor acquisition system of [77] with five dedicated channels, viz. ECG, bioimpedance (BIO-Z), galvanic skin response (GSR) and PPG, uses a power hungry ARM Cortex M0 processor and hence has to be battery-operated. Relying on the fact that heart rate can be measured by BIO-Z or PPG, apart from ECG, significantly enhancing the robustness and reliability of the measured parameters. The work in [78] demonstrates a low-power 3-lead ECG-on-chip featuring a joint QRS detector and lossless data compressor (JQDC) for wearable wireless ECG sensors. Similarly, [79] utilizes a general purpose ARM Cortex M0 processor and an HW accelerator optimized for energy-efficient execution of various biomedical signal processing algorithms for a MUlti-SEnsor biomedical IC (MUSEIC). The design in [80] describes body sensor node (BSN) SoC capable of autonomous power management and operation from harvested power, acquiring, processing, and transmitting ECG, EMG, and EEG data. The medical implant communication service (MICS) or industrial, scientific and medical (ISM) radio bands are used for transmission. [81–83] propose similar works on wearable ECG SoC. Going a step forward form these conventional designs, [84] develops an energy efficient ECG signal processor and an android application intended to detect various cardiac arrhythmia like bundle branch block, hypertrophy and myocardial infarction. An easy-to-use ECG acquisition and heart rate monitoring

system using a wireless steering wheel is demonstrated in [85]. Lead I measurement is done using a front-end augmented with dual ground electrode configuration to reduce 50/60 Hz interference. Breaking free from the conventional way of designing ECG front-ends in analog domain, a fully digital front-end architecture with no analog blocks, e.g., low-noise amplifier (LNA), and filters, and no passive elements, such as ac coupling capacitors, is proposed in [86]. The traditional LNA and anti-aliasing filter is replaced by moving average voltage-to-time converter.

Table 1.3 and 1.4 summarizes the features, scope and performance of the existing state-of-the-art ECG front-ends. It lays the roadmap for the constitution and implementation of the proposed system. As is already discussed above, minimum power dissipation is the prime concern for any wearable remote ECG acquisition system. Therefore each individual block comprising the full system, e.g. analog front-end for acquisition and amplification, ADC for digitization, circuit for gain and bandwidth calibration, other relevant circuits, etc. need to be designed with very stringent power constraints. Numerous low-power CMOS front-ends employing a plethora of topologies are already reported. Since the output of the amplifier is fed to the ADC, the amplifier's output should be band limited. Also taking clue from the recent trend, a front-end, augmented with circuits capable of R-peak detection and low complexity processing useful for preliminary diagnosis of cardiac abnormalities on the same analog platform, needs to be implemented. This forms the target of this thesis.

1.3 Highlights of Research Investigations

- Comprehensive review of the already existing low-power front-end designs for ECG acquisition (amplification and digitization) and the relevant design challenges.
- Detailed discussion on target performance parameters for a ECG front-end and the subsequent choice of design topologies and techniques to achieve the same; design of the two stage programmable gain amplifier using an operational transconductance amplifier (OTA) with a novel G_m cancellation technique; obtaining a tunable bandpass filter characteristics using pseudo-resistors is also given.
- Process-aware automatic gain control and 3-dB low pass cut-off frequency tuning circuit.
- Design of a low power discrete-time opamp-shared second order 1-bit $\Sigma\Delta$ modulator for digitization of the amplified signal.

- Ultra-low power autonomous peak detector based QRS detection circuit, employing a dynamic threshold voltage for detection.
- Low complexity fully analog domain circuit for heart rate estimation and detection of asystole, extreme bradycardia and tachycardia using the *in-situ* R-peak detector.

1.4 Overview of Thesis Contribution

This work focuses on the design of a low power ECG acquisition front-end for continuous remote batteryless/self-powered recording and monitoring. It includes a completely automatic AGC and AFT, a single opamp reconfigurable order 1-bit $\Sigma\Delta$ ADC, a peak detector based R-peak detection circuit and a simple logic for the detection of three life-threatening cardiac abnormalities i.e. asystole, extreme bradycardia and extreme tachycardia. The complete circuit is designed on an analog platform using UMC $0.18\mu m$ CMOS technology. The prime highlights of the thesis are summarized in the following sub-sections.

1.4.1 Review of Low Front-end for Continuous ECG Monitoring

Contemporary smart ECG monitoring systems intended for remote healthcare applications consists of an efficient acquisition, 'analysis', and a wireless transmission platform. An efficient acquisition involves signal conditioning, i.e. amplification and filtering, and digitization. Since the bio-potential signals are of very weak magnitudes (0.1-1 mV), they need to be amplified appropriately. The amplification is done using an instrumentation amplifier or a programmable gain amplifier (PGA). Recent research endeavors to introduce OTA topologies with lesser power consumption, greater common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), and greater linearity along with higher output voltage swings. The same PGA is also responsible for providing the bandpass filter characteristics. On top of that, provision has be made to calibrate both the gain and higher frequency bandwidth of the PGA for process variations. Therefore, the gain control or bandwidth tuning can be either controlled externally (generally through an external DSP) or fully automatic. Moreover if the front-end is to handle multiple bio-potential signals, with a wide range of dynamic ranges and bandwidths, reconfigurability is essential in terms of gain, high-pass and low-pass 3-dB cut-off frequencies. Successive approximation register (SAR) ADC is the most popular low resolution topology to digitize these signals because it is possible to implement it with power dissipation in the order of nano-watt. At the same time the $\Sigma\Delta$ ADC has gained prominence for applications

where a high resolution is required, albeit at the cost of a comparatively higher power dissipation. Primarily 'analysis' of the ECG signal includes filtering, feature extraction and classification. Generally the task of 'analysis' is done on a DSP, recent works demonstrate the possibility of shifting of the task of QRS detection, other feature detection and classification from the digital domain to analog domain. Since most of the power is consumed in the 'analysis' and transmission part of the system, implementation of the lesser complex functionalities e.g. R-peak detection, on analog platform reduces the power consumed significantly. Different front-end architectures suitable for acquiring ExG signals are explored. Implementation methodologies for a reconfigurable front-end are explored in detail. Further, the performance specification for a reconfigurable front-end is formulated by reviewing pertinent implementations of the state-of-the-art in relevant literature. The stepwise design methodology and the design challenges to achieve the target performance are also provided.

1.4.2 Low Power ECG Amplifier with Bandpass Filter Characteristics for Acquisition and Low Power Discrete-time Opamp-shared Second Order 1-bit $\Sigma\Delta$ Modulator ADC for Digitization

A high value of CMRR, good linearity for higher output voltage swings, high input impedance, bandpass filter characteristics and low power consumption are the key requirements for a generic analog front-end (AFE) for acquisition of various biopotential signals (ExG) with different bandwidth and dynamic ranges or gain requirements. Traditionally a three opamp instrumentation amplifier topology is used for amplification, but its CMRR depends upon resistor matching. Hence, the capacitive feedback topology has gained popularity. It offers a better matching between the system requirements and actual performance compared to the former. It provides high input impedance for low frequency signals inherently. Further the fact that the foundries responsible for fabrication of the IC offer good matching between capacitors and hence improves the gain accuracy and CMRR. In this work, the signal conditioning stage is implemented as a two stage amplifier with capacitive feedback. Apart from amplification, it also provides a second order bandpass filer characteristics. The heart of each of the stages is a fully differential recyclic folded cascode (RFC) OTA with a novel G_m cancellation technique to improve the CMRR. The recycling folded cascode topology is used in IA. This topology renders a higher gain and transconductance g_m compared to the folded cascode topology for same power consumption. All the transistors are operated in moderate inversion to obtain low drain currents. The g_m/I_D technique is used for sizing the transistors. An optimized

value of g_m/I_D is utilized for obtaining higher gain, linearity, output swing, while rendering low noise and consuming less power. The amplifier provides a gain of 40-60 dB and has a bandwidth of 0.05-250 Hz. Once the signal is conditioned as desired, it is ready to be digitized using an ADC.

A resolution of 6-8 bits is considered to be adequate for ECG front-ends. SAR ADC is the most popular architecture for such low resolution digitization due the possibility of implementing it with ultra low power dissipation (nW range). But since it is a Nyquist rate ADC, it requires an anti-aliasing filter of order greater than four. Also its performance is quite sensitive to post-fabrication component mismatches and it is not easy to incorporate reconfigurability in the same design. The $\Sigma\Delta$ modulator topology turns out to be the best for applications requiring a high resolution (20-24 bits) conversion. Although the $\Sigma\Delta$ ADC is a power hungry topology comparatively, it can work with anti-aliasing filters of even first order. Moreover, the $\Sigma\Delta$ is inherently less sensitive to the problem of post-fabrication component mismatches and aids area and power cost efficient switching between the two modes vis-a-vis other ADC architectures e.g. SAR ADC, pipeline ADC, etc. In this work, a low power discrete-time opamp-shared 1-bit $\Sigma\Delta$ modulator is implemented. The modulator is reconfigurable between first order low resolution mode and second order higher resolution mode. While the first order noise-shaping is obtained using one opamp, second order noise-shaping is also obtained using a single opamp. The $\Sigma\Delta$ architecture facilitates a seamless ADC resolution reconfigurability with minimal hardware and almost zero power overhead. The salient advantages of such a reconfiguration are as follows (i) this facilitates the digital circuit responsible for classification of the ECG signal, following the $\Sigma\Delta$ ADC, to reduce its power consumption by opting to process low resolution data (ii) facilitates reconfigurability between low and high resolution for preliminary and final diagnostics, respectively (iii) since the noise power at ADCs input is inversely proportional to AFE's gain, this scheme provides a choice between low and high resolution for high and low gain, respectively. Moreover, the ADC is activated only when the AGC and AFT have finished their jobs, hence saving significant amount of power.

A series of MATLAB based GUIs which aid the circuit level implementation of the $\Sigma\Delta$ ADC, right from the scratch, is developed here. Although the design is still modeled using SIMULINK, the GUI developed takes in user-defined inputs, runs the SIMULINK model with these inputs and display the relevant output hence generated in a manner which is aesthetic as well as easily comprehensible. All these GUIs have been uploaded on MATLAB Central, MathWorks [87]. They are freely available and user friendly. It will help a circuit designer fix the order (L), resolution of the internal quantizer (B) and the oversampling ratio (OSR) required to achieve the target SNR. Additionally, it also

helps the designer to have an estimate of the required performance specifications of each individual block in order to achieve the desired overall performance. The circuit is designed and laid-out. The performance parameters are verified using post-layout simulations.

Further, the post-layout and measurement results are provided.

1.4.3 Process-aware Automatic Gain Control and 3-dB Lowpass Cut-off Frequency Tuning Circuit

The dynamic range of ECG signals is from 0.1-1mV, varying from subject to subject and also for location of electrodes on different parts of the body. Since the output of the amplifier is fed to an ADC, it is necessary to ensure that (i) irrespective of the input voltage magnitude, the input is amplified sufficiently to maximize the signal-to-noise ratio (SNR) at the ADC's input (ii) the amplifier's output is strictly band limited to avoid aliasing due to sampling. Moreover, the post-fabrication component mismatches and variation further worsens the situation. This brings out the necessity of incorporating a calibration mechanism along with the amplifier, which ascertains that the circuit provides the desired gain and bandwidth across process, voltage and temperature (PVT) variations. In most of the state-of-the-art ECG acquisition circuits, like [62], this calibration is implemented by selecting an appropriate combination of capacitors manually or with the help of an external DSP. Therefore an efficient gain control (AGC) mechanism is designed to maintain the input of the ADC to an optimum level for which the ADC provides maximum SNR. The AGC is responsible to make the PGA provide a gain from 40-60dB. Similarly, an *in-situ* automatic frequency tuning (AFT) scheme responsible for maintaining the 3-dB lowpass cut-off frequency at 250Hz is designed. Both, the AGC and AFT, are designed to work completely autonomously, hence shunning the idea of externally controlled calibration. The complete scheme is designed, laid-out and their performance are validated through post-layout simulations.

The AGC and AFT are augmented with the AFE, and the complete scheme is designed, laid-out and taped out. Further, the post-layout and measurement results are provided.

1.4.4 Ultra-low Power Autonomous Peak Detector Based QRS Detection Circuit and Low Complexity Fully Analog Circuit for Heart Rate Estimation and Detection of Asystole, Extreme Bradycardia and Tachycardia

Detection of QRS complexes is the first step for any ECG classification scheme for cardiac rhythm (CR) and heart rate variability (HRV) analysis. Most of the state-of-the-art application-specific integrated circuits (ASIC) employ an ADC followed by a DSP to identify the location of R-peak and hence detect heartbeat. Primarily, the QRS detection is done in digital domain using a DSP or a low power micro-controller. But the algorithms involved are usually computationally intensive, hence making the DSP based beat detection power hungry. To further reduce the power consumption, the recent state-of-the-art ECG monitoring systems have shifted the R-peak detection from the digital domain to the analog platform itself. A comparator based detection scheme [69] has been introduced recently, but the required threshold voltage for comparison is controlled by an external micro-controller. Moreover, in case of irregular QRS complexes and rapid baseline wandering, the micro-controller reruns the calibration routine. If the recaliberation fails after enough number of iterations, then this topology identifies it as a case of arrhythmia. Multiple runs of the calibration routine will further worsen the power budget of the system. Therefore, a completely autonomous peak detector scheme for R-peak detection is designed in this work. The proffered circuit for QRS complex detection has the following advantages over the scheme where the threshold is set by a micro-controller (i) it does not involve a micro-controller and (ii) it does need to be calibrated, and hence completely automatic and power efficient (iii) since the threshold value for comparison is derived from the R-peaks itself, this topology works fine for ECG signals with varying amplitudes and rapid baseline (iv) the proposed circuit is compatible with the scheme of recovering the ECG R-wave timing from the QRS detection pulses mentioned in recent literature. The complete scheme is fully designed and laid-out. Post-layout simulations confirm the better performance of the proposed circuit. Due to lack of resources, the circuit is not taped out. The functionality of the proposed beat detection scheme is validated in prototype mode. It comprises of a mbed NXP LPC1768 board, a discrete board (with a peak detector, a buffer, a resistive voltage divider, and a comparator) and a FPGA board. The verification of the topology is done using the following steps (i) input to the peak detector is given though the DAC output pin of the mbed board and (ii) a peak detector and pulse generation circuit built using discrete components detects the occurrence of a R-peak by generating a high pulse. The output waveforms match those obtained through simulations in Cadence Virtuoso.

Primarily 'analysis' of the ECG signal includes filtering, feature extraction and classification. These operations are implemented through DSP on a system-on-chip (SoC) platform. However, DSP based techniques are more computationally intensive and consume power in the order of tens or hundreds of micro-watts. This makes them incompatible with devices requiring long life span and intended for continuous ECG monitoring. Therefore the recently published works, e.g. [88], implement the functionality of feature extraction in analog domain, rather than on a DSP. This enables significant reduction of system level power consumption by minimizing the computational burden on the DSP. Therefore, a power efficient analog classifier for the detection of three of the critical alarm types viz. asystole, extreme bradycardia and tachycardia is designed. The proposed classification scheme presents a useful trade-off between complexity, accuracy and power consumption. The functionality of the classifier is first validated using behavioral Verilog code and importing the same in Cadence Virtuoso platform. Again the working principle is validated in prototype mode. The experimental set is same as that for the detection of R-peaks. The pulses generated by the prototype is stored and input to a FPGA, and the algorithms to detect asystole, extreme bradycardia and tachycardia are verified using the FPGA. The output waveforms match those obtained through simulations in Cadence Virtuoso.

1.5 Organization of the Thesis

The organization of the thesis is as follows. A detailed discussion on the conceptualization of the complete low power ECG recording system and the derivation of the approximate performance specifications of the individual modules, hence laying out the roadmap for design of the same, is given in Chapter 2. Chapter 3 describes the design of the required instrumentation amplifier and programmable gain amplifier for the amplification and filtering (signal conditioning) of the ECG signal. It also provides design details of the opamp-shared 1-bit $\Sigma\Delta$ modulator ADC to digitize the ECG signals. The post-layout and measurement results are also provided. A comprehensive explanation of the design of the process-aware automatic gain control and frequency tuning circuit is provided in Chapter 4. The post-layout and measurement results are also included. Chapter 5 presents a fully analog QRS complex detector, and a low hardware complexity technique for the classification of asystole, extreme bradycardia and extreme tachycardia. Chapter 6 concludes the thesis and chalks out the scope for future work.

Table 1.3: Review of the contemporary state-of-the-art front-end designs - Part I

Parameter	**JSSC '07 [62]**	**JoS '13 [63]**	**TBCAS '10 [64]**	**ISSCC '10 [65]**	**JSSC '11 [66]**
Technology (μm)	0.5	0.18	0.35	0.35	0.6
V_{supply} (V)	3	1.8	3	1	2.8
Gain (dB)	58.06-67.95	45	54-73	59-71	39.4
f_L (Hz)	EEG - 0.3 ECG - 0.3 EMG - 14	0.6	0.5-50	0.5	0.36
f_H (Hz)	EEG - 40 ECG-125 EMG-350	160	500-1000	150	1300
Power (μW)	60	1	12.75	0.385	2.4
Noise (μV_{RMS})	0.056-0.057	2.8	6.08	1.15	3.07
CMRR (dB)	> 120	–	60	83.2	
THD @ 50 Hz	@ 5 mVp-p minimum gain 0.45-0.52%	–	–	<1% 0.9 Vp-p output swing	
NEF	9.2	3.4	5.5	2.24	3.09
PEF	253.92	20.8	90.75	5.01	26.38
Chopper	Yes	No	No	No	No
AGC	Ext. - cap. switch	No	Ext. - cap. switch	Ext. - cap. switch	No
AFC	Ext. - cap switch	No	Ext. - OTA bias current	HPF: pseudo-resistor LPF: cap switch	No
Architecture	AC coupled chopper IA	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback
Application	EEG EMG EMG	ECG	Neural	ECG	Neural

Table 1.4: Review of the contemporary state-of-the-art front-end designs - Part II

Parameter	**TBCAS '11 [67]**	**JSSC '09 [1]**	**TBCAS '12 [68]**	**TBCAS '15 [69]**	**TCAS '15 [70]**
Technology (μm)	0.18	0.35	0.13	0.18	0.35
V_{supply} (V)	1.8	1	1	0.8	2.5
Gain (dB)	49-66	45.6-60	40	47-88	40.3
f_L (Hz)	0.13-350	4.5 m-3.6	0.4	0.5	-
f_H (Hz)	293-12000	31-292	8.5 k	22	0.1-10 k
Power (μW)	5.4-20	0.033-0.337	12.5	51.2	-
Noise (μV_{RMS})	5.4-11.2	2.5 (0.05-460 Hz)	3.2	2.7	2.81
CMRR (dB)	62	> 71	> 60	66	> 82
THD @ 50 Hz	–	0.6% full swing	1.5% @ 1 mVp-p	–	0.1% 3.9-4.3 mV_{rms}
NEF	4.4-5.9	3.26	4.5	5.6	1.88, 1.93, 2.05
PEF	34.84-62.65	10.62	20.25	25.7	
Chopper	No	No	No	No	No
AGC	Ext. - cap switch	Ext. - cap switch	Ext. - cap switch	Ext. - cap switch	No
AFC	Ext. - OTA I_{bias} Ext. - OTA Ibias	HPF: I_{bias} of PR LPF: OTA I_{bias}	HPF - bias of feedback LPF : OTA I_{bias}	No No	No No
Architecture	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback
Application	Neural	ECG	ECG, EEG, EMG	ECG	ECG, EMG

Chapter 2

ECG Recording System: Design Essentials

2.1 Proposed ECG System : Conception to Specs

Despite the fact that instrumentation amplifiers realized using discrete components have been already been reported [89], a fully custom designed integrated circuit solution, augmented with other critical functions, promises solutions with lower power and area cost. [90] categorizes the ECG monitoring systems as recording and analyzing systems. The recording system is responsible for ECG signal acquisition, storage, and transmission. The analyzing system extracts important features of ECG to be transmitted to a doctor. Integrating both the functionalities on the same platform proves to be a more area and power efficient solution. A generic bio-potential signal remote and long-term monitoring system is shown in Fig. 2.1a. The complete system can be divided into three major blocks, viz. acquisition, analysis, and transmission. The foremost block is responsible for acquisition which pertains to signal conditioning (amplification and filtering) and digitization. The programmable gain amplifier, filter and the ADC is implemented in analog domain generally. The acquisition, digital signal processing (DSP) and wireless data transmission consume 2%, 25% and 73%, respectively, of the total power consumption approximately [88]. As majority of the power is burnt in wireless data transmission, wireless transmission of raw data is not power efficient. Recent related works have tried to make the transmission more power efficient by employing fully integrated lossless compression engine [73, 78, 91] or adaptive sampling [76]. But both these techniques involve

extra hardware and excess power dissipation. So, pre-processing the data on-chip is necessary to limit the amount of data being transmitted. Therefore, the acquisition block is followed by the block handling the analysis of the recorded signals. Analyzing the recorded data involves extraction of the vital features, location and timing of the R-peaks being the most important. Based on the information obtained from these features and by employing advanced algorithms, the recorded data is segregated into normal and abnormal ECG. Moreover, the abnormal ECG can be classified into specific arrhythmia, e.g. atrial fibrillation, myocardial infraction, etc.. The necessary processing is done using a low power DSP or an on-chip a low-power micro-controller core with a few customized DSP features. The memory required for processing is also integrated into the same system. Finally, the third block transmits the processed/raw data to a cloud or a medical expert for more accurate diagnosis. The transmission is to be made more power efficient by (i) duty-cycling the transmitter using on-chip memory, (ii) lowering frequency, and (iii) utilizing the impulse radio ultra-wide band (UWB) transmitter, IEEE 802.15.4 standard (i.e., ZigBee applications), medical device radio communications service (MedRadio), and medical implant communication service (MICS) [73,75,90,92]. The block-wise conception of such a biopotential monitoring system is discussed below, along with the justification and utility of each block.

Fig. 2.1b illustrates the pertinence of each of the blocks. A brief discourse on the sequential constitution (highlighted using encircled numbers) of the complete system, sans the radio block, using individual modules and the relevant design challenges, apart from the implicit low power implementation, is as follows:

2.1.1 Digital Signal Processor

The processing of the recorded ECG data before transmission is done using a DSP (labeled ① in Fig. 2.1b). Energy-efficient classification algorithms are executed on a digital platform. Various low power modules are used for this purpose, e.g. peripheral interface controllers (PIC), MSP430, custom-designed microcontroller [75], ARM Cortex M0 processor with a optimized hardware accelerator [77,79], customized 4-way single instruction multiple data processor [76], etc.

2.1.2 Analog-to-Digital Converter

Since the input to DSP or the micro-controller is digital, an ADC is required to convert the analog ECG signal, after appropriate amplification, into a digital signal (labeled ② in Fig. 2.1b).

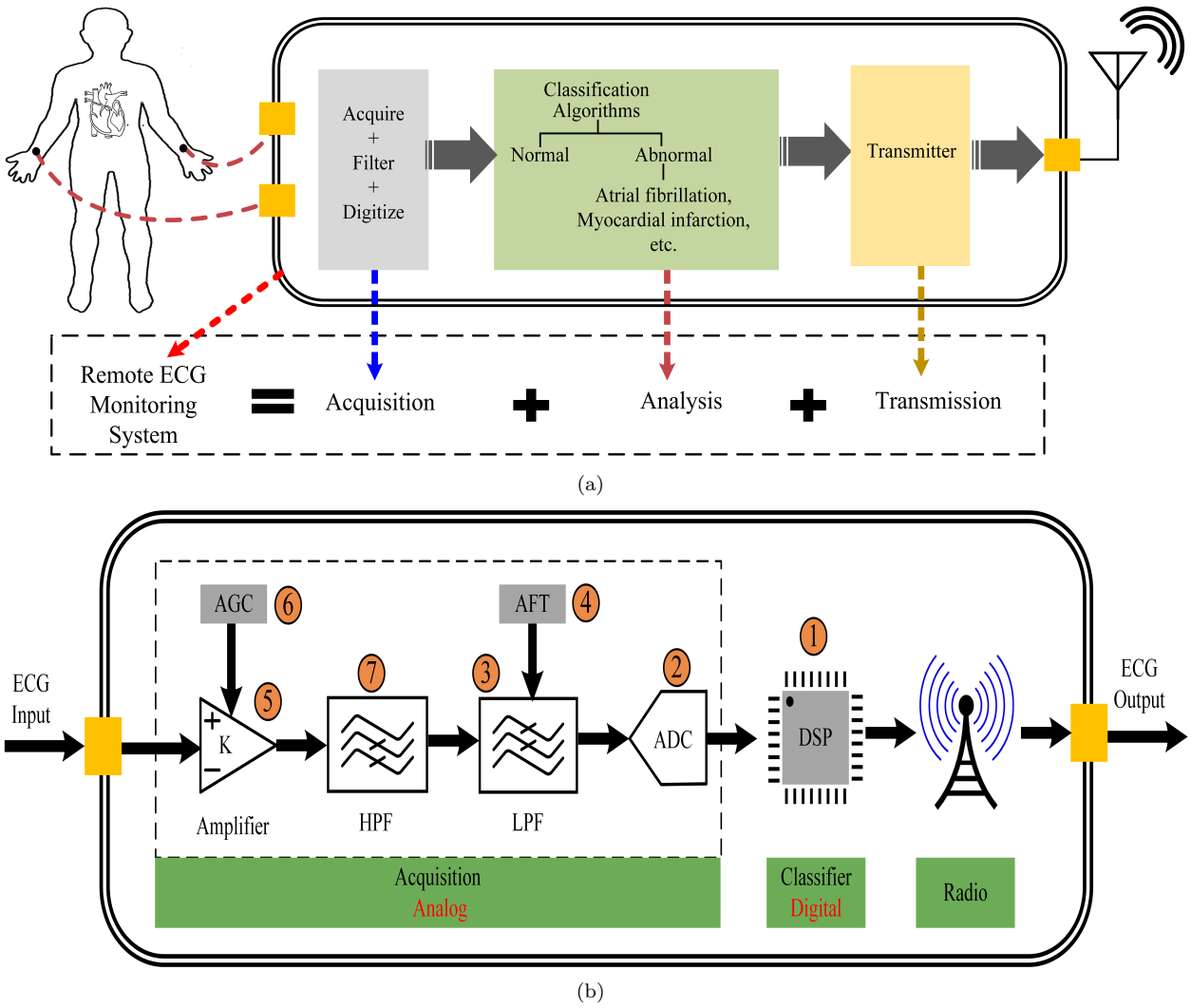


Figure 2.1: Block diagram of ECG recording system (a) Top level conceptualization, (b) Sequential block-wise conceptualization of the system.

Conventionally, SAR ADC is the most preferred choice for low resolution (6-8 bits [1,60,75,93,94]) digitization of ECG signals mainly because it allows ultra-low power implementations e.g. [1] reports a SAR ADC with 10.2 effective number of bits (ENOB) while consuming only 230 nW power. But for applications where a high ($>$ 10 bits) resolution is required, the $\Sigma\Delta$ modulator architecture is utilized at the cost of dissipating more power 24.8 μW while achieving a high signal-to-noise-and-distortion ratio (SNDR) of 80.4 dB for a bandwidth of 10 kHz. Commercially available ADS1298 [35] employs a 24 bit $\Sigma\Delta$ ADC. Other works like [72,79,81,95–97] also implement 10-12 bit $\Sigma\Delta$ ADC for biomedical front-ends. Apart from the high resolution, the $\Sigma\Delta$ ADC is a better choice because of the relaxed order of the anti-aliasing filter required before the ADC. [98] employs an 8^{th} order LPF before a 13 bit SAR ADC, whereas the order of the anti-aliasing filter can go as low as one for a

ΣΔ ADC depending on the oversampling ratio (OSR) [99]. Moreover, the ΣΔ architecture exhibits greater immunity to issues like component mismatches and offers easy reconfigurability. Another aspect to be considered while defining the target resolution of the ADC is the gain of the PGA. Fig. 2.2 (adopted from [99]) illustrates this concept. It shows that a comparatively lower resolution ADC needs to be used when a high gain is expected from the PGA, and vice versa, to make sure that the noise of the amplifier that gets amplified does not dominate the net system noise. Moreover since a low power implementation is one the prime concerns for the design of each block of the complete system, ways to achieve the target performance with reduced power consumption must be explored. Hardware sharing or reuse is one such technique. For the design of discrete-time ΣΔ modulator ADC, implementations have been reported where the target order of noise-shaping is obtained using lesser number of integrators (or OTAs) [100–110]. Such implementations are called opamp-shared ΣΔ modulator ADC.

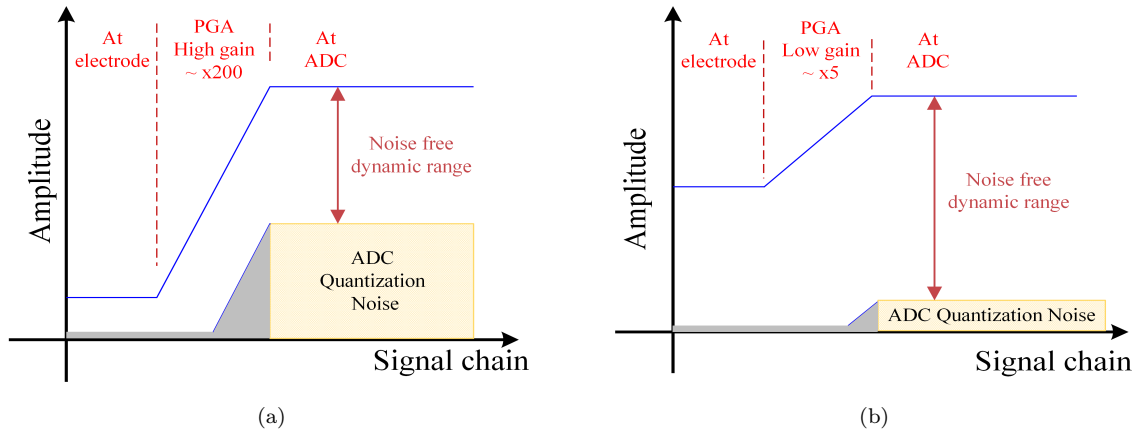


Figure 2.2: Defining the target resolution of the ADC w.r.t the gain of the PGA (a) High PGA gain with low resolution, (b) Low gain with high resolution ADC

Taking the above points into consideration, the ΣΔ modulator topology is chosen for this work. Also taking clue from Fig. 2.2 and relevant literature, a moderate 10 bit resolution is targeted here. A 10 bit resolution is sufficient to handle the target dynamic range of 0.1-1 mV, and is compatible with the popular classification algorithms and matches commercially available ECG monitoring systems like [111]. A second order noise-shaping is chosen considering its low hardware complexity, minimum power dissipation and unconditional stability. Further, using the opamp-shared technique the desired second order noise-shaping is achieved using a single integrator (or OTA).

Table 2.1: Comparative analysis of SAR and ΣΔ ADC as a choice for digitization of biomedical signals

	SAR	ΣΔ
Type	Nyquist rate	Oversampled
Resolution	8-10 bits [75, 112]	up to 24 bits [35]
Power	Very low, (hundreds of nW) [1]	High (tens of μW) [113]
Anti- aliasing Filter	sharp (typ. Order $>$ 4) [99]	relaxed (typ. Order $\sim$ 1) [99]
Performance sensitivity to post fabrication component mismatch	High [81]	Low [81]
Ease of reconfigurability	Difficult	Simple

2.1.3 Lowpass Filter

A low pass filter is required before the ADC to strictly band limit the input ECG signal so as to avoid unwanted frequencies to enter the signal bandwidth (labeled ③ in Fig. 2.1b).

2.1.4 Automatic Frequency Tuning

It is well known 3-dB filter frequency is sensitive to process-dependent component mismatches. This fact, along with the effect of parasitics force, the cut-off frequency to be highly sensitive to fabrication tolerances, and deviate from its desired nominal value. Since the output of the amplifier is fed to an analog-to-digital converter (ADC), a precise low pass cut-off frequency is required. This in turn necessitates the use of an on-chip automatic frequency tuning circuit to curtail the drift of the cut-off frequency to tolerable limits. In order to obtain the desired low pass 3-dB cut-off frequency accurately despite the post-fabrication component mismatches, an automatic frequency tuning (AFT) scheme is needed (labeled ④ in Fig. 2.1b).

2.1.5 Instrumentation Amplifier and Programmable Gain Amplifier

Since physiological signals are of weak magnitude, they need to be amplified sufficiently by an instrumentation amplifier (IA) while maintaining the signal quality so that they can be input to the ADC. The designer should make sure that the signal-to-noise ratio (SNR) of the amplifiers is greater than the resolution of the ADC. Fig. 2.3 shows that apart from the desired ECG signal, the AFE encounters a DC offset (arising due to half cell potential, baseline wander, etc.) and common mode signals like the 50/60 Hz power line interference and background noise. As shown in Fig. 2.3, the AFE is responsible for signal conditioning [114]. Signal conditioning comprises of amplification

and bandpass filtering. High pass filtering is necessary to attenuate the DC components . Low pass filtering is needed to band-limit the output of the AFE to prevent aliasing of higher frequencies due to sampling by the subsequent ADC.

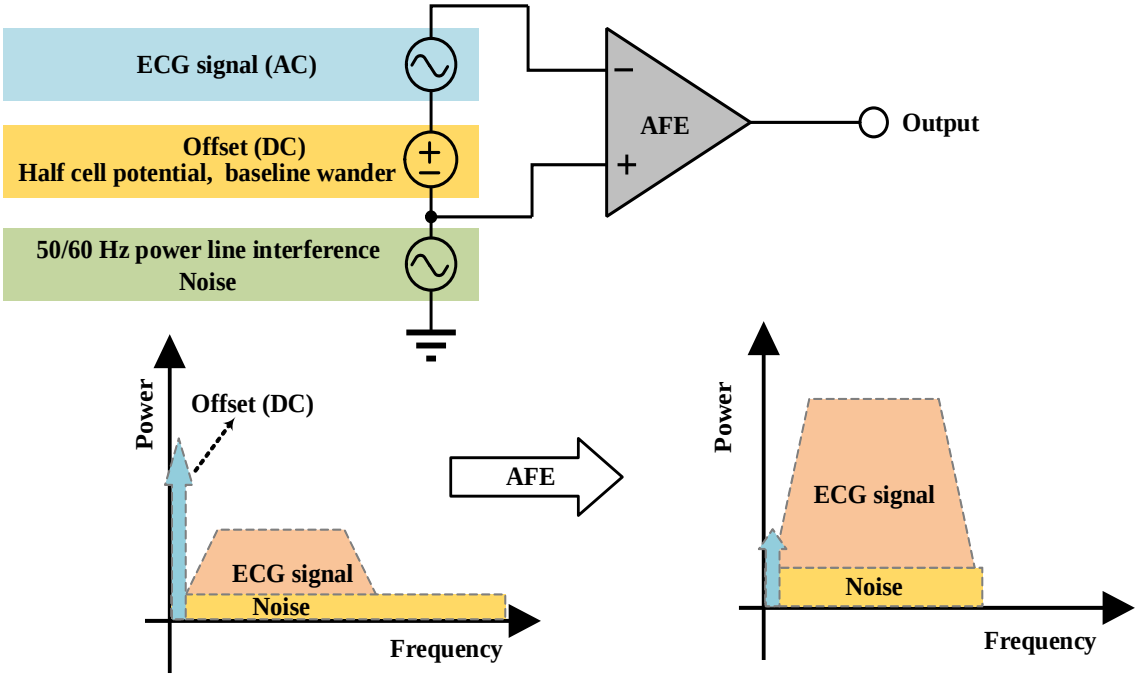


Figure 2.3: Signal conditioning done by the AFE.

Further, the magnitude of the ECG signal varies with the location of the electrodes and from patient to patient. Therefore it is imperative to amplify it with enough gain so that irrespective of the input signal magnitude the output signal has a magnitude for which the ADC exhibits optimum SNR. A programmable gain amplifier (PGA) is doled this job (labeled ⑤ in Fig. 2.1b).

A dynamic range of the ECG signal considered for this work is 0.1-1 mV (20 dB or 3.3 bits approximately), the range is attributed to the variation in the amplitude with different patient and the location of the sensing electrode [40, 115]. Also a bandwidth of 0.05-250 Hz is considered sufficient to retain all the essential features of the acquired ECG signal and include fetal ECG signal [116, 117]. The IA to be designed should cater to both these requirements. Traditionally a three opamp instrumentation amplifier topology is used for amplification, but its CMRR depends upon resistor matching [62]. Switched capacitor (SC) based IAs are proposed in [118, 119], but is ailed by the the fold-over of noise above Nyquist frequency [120]. Yet another IA topology is the current feedback (current balancing) IA [62, 121]. The gain of this IA is determined by the ratio of two resistors, and hence matching of the resistors is not mandatory to obtain high CMRR. However

the need of an opamp increases the power consumption of the IAs.

Hence, the capacitive feedback topology has gained popularity [62, 70, 122, 123]. It offers a better matching between the system requirements and actual performance compared to the former. It provides high input impedance for low frequency signals inherently. Further the fact that the foundries responsible for fabrication of the IC offer good matching between capacitors and hence, the gain accuracy and CMRR can be improved. In this work, the signal conditioning stage is implemented as a two stage amplifier with capacitive feedback. A fully differential topology is employed to obtain a high CMRR, power supply rejection ratio (PSRR) and large dynamic range.

The analysis of the working principle of the differential OTA-based capacitor-coupled ECG signal amplifier with capacitive feedback can be explained using a simplistic single-ended version of the same circuit. The schematic of the single-ended version is shown in Fig. 2.4a. The functionality, salient features and essential design aspects of this circuit are discussed below (pertinent diagrams are adopted from [122, 124]).

Amplification and bandpass filter characteristics

- The transfer function of the amplifier shown in Fig. 2.4a can be presented in to a more compact and informative form as [122]. The derivation of the transfer characteristics of the amplifier using small signal equivalent circuit is given in Appendix A.

- The transfer function of the amplifier shown in Fig. 2.4a can be presented in to a more compact and informative form as [122].

$$\frac{v_{out}}{v_{in}} = K_{mid} \quad \frac{1-\frac{s}{2\pi f_z}}{\left(\frac{2\pi f_L}{s}+1\right)\left(\frac{s}{2\pi f_H}+1\right)}, \qquad where$$
$$K_{mid} = \frac{C_1}{C_2}; \quad f_L = \frac{1}{2\pi R_2 C_2}; \quad f_H = \frac{G_m}{2\pi C_L K_{mid}}; \quad f_Z = f_H \frac{C_1 C_L}{C_2^2}. \tag{2.1}$$

  The bode plot of this transfer function is illustrated in Fig. 2.4c. The figure shows that a bandpass filter characteristics is obtained from the circuit in Fig. 2.4a.

- The midband gain, K_{mid}, is determined by the capacitor ratio $\frac{C_1}{C_2}$.

- The lower cutoff frequency (location of first pole), f_L, is set by the product of R_2 and C_2.

- The higher cutoff frequency (location of second pole), f_H, is defined by the OTA transconductance G_m, the load capacitor C_L and the midband gain K_{mid}.

- The second zero frequency, f_Z, should be pushed to very high frequencies avoiding any practical effect it may have on the amplifier's operation. This can be achieved by ensuring that the values of the corresponding capacitors satisfy the following relationship [122]

$$C_2 \ll \sqrt{C_1 C_L} \tag{2.2}$$

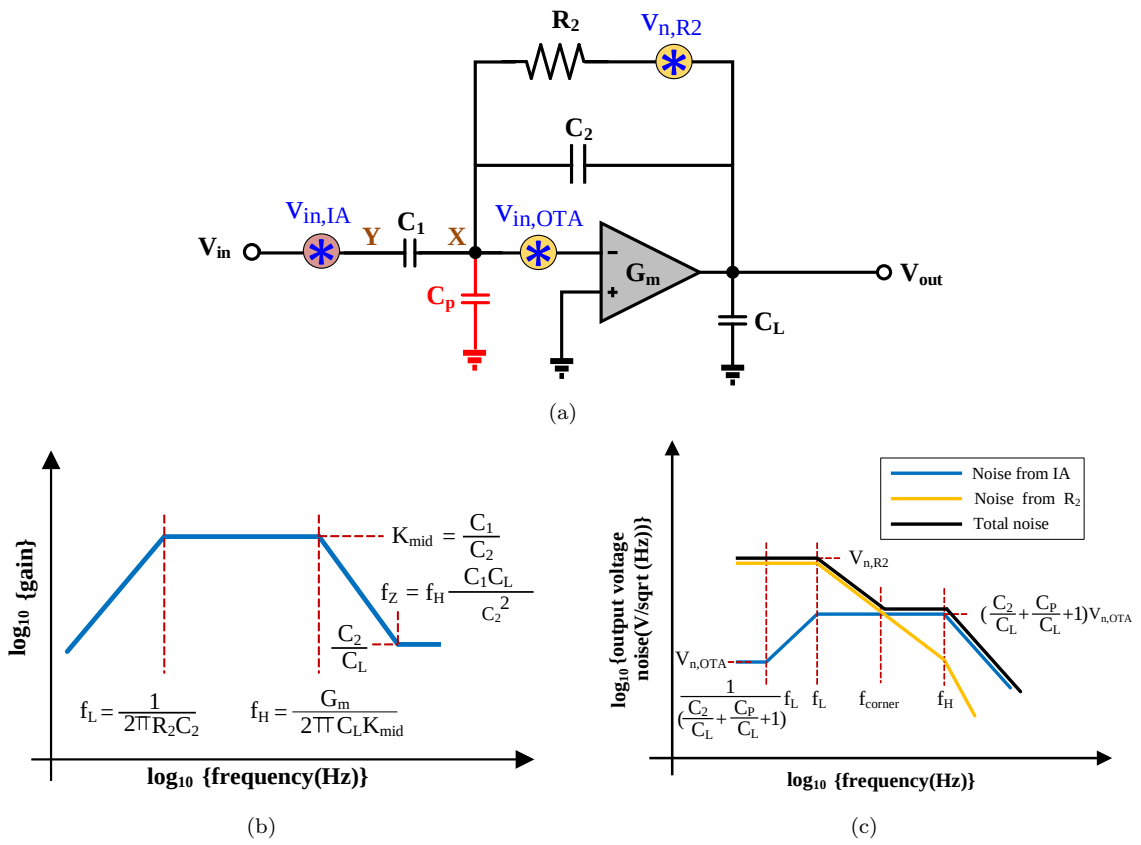


Figure 2.4: (a) Schematic of OTA-based capacitor-coupled ECG signal amplifier with capacitive feedback, (b) log-log plot of the gain *vs.* frequency for the amplifier, (c) log-log plot of the output noise *vs.* frequency for the amplifier.

Noise Considerations

- The thermal noise sources in the capacitive feedback amplifier, i.e. input-referred noise of the OTA and noise contributed by the feedback element R_2 are modeled by $V_{in,OTA}$ and $V_{n,R2}$. Both the noise sources are shown in Fig. 2.4a. The contribution to the total amplifier output noise, ignoring the $\frac{1}{f}$ noise, is shown Fig. 2.4b [122].

- The OTA contributes noise between f_L and f_H.

- Contribution from $V_{n,R2}$ dominates below f_{corner} where

$$f_{corner} \approx \sqrt{f_L f_H \frac{3C_L}{2C_1}}; \quad assuming C_1 \gg C_2, C_P \tag{2.3}$$

- As can be inferred from Fig. 2.4b, to minimize the contribution from the feedback element R_2, the designer should ensure that $f_{corner} \ll f_H$. This can be achieved by designing the amplifier such that

$$\frac{C_L}{C_1} \ll \frac{2}{3}\frac{f_H}{f_L} \tag{2.4}$$

- The noise voltage at the output of the IA, $v_{n,OTA,out}$,(shown in Fig. 2.4a) generated only by the input-referred noise of the OTA, $v_{in,OTA}$ exclusively, can be obtained by writing the KCL equation at the node 'X'

$$(v_{in,OTA})sC_1 + (v_{in,OTA})sC_P + (v_{in,OTA} - v_{n,OTA,out})sC_2 = 0 \tag{2.5}$$

which implies

$$\frac{v_{n,OTA,out}}{v_{in,OTA}} = \Big(1 + \frac{C_1}{C_2} + \frac{C_P}{C_2}\Big) = \Big(\frac{C_1 + C_P + C_2}{C_2}\Big) \tag{2.6}$$

- Considering $v_{in,IA,OTA}$ as the OTA's contribution to the overall input-referred IA noise voltage. Further $v_{n,OTA,out}$ can be referred to the IA's input (node 'Y') using the expression

$$\frac{v_{in,IA,OTA}}{v_{n,OTA,out}} = \frac{1}{K_{mid}} = \frac{C_2}{C_1} \tag{2.7}$$

- Let $\overline{v^2_{in,OTA}}$ and $\overline{v^2_{in,IA,OTA}}$ represent the input-referred noise power of the OTA and the OTA's contribution to overall input-referred IA noise voltage, respectively. Within the frequency band of interest, f_L to f_H, $\overline{v^2_{in,OTA}}$ at node 'X' can be referred to the input node 'Y', and the resultant input-referred noise contributed by OTA can be obtained using equation 2.6 and 2.7 [68]

$$\frac{\overline{v^2_{in,IA,OTA}}}{\overline{v^2_{in,OTA}}} = \Big(\frac{v_{n,OTA,out}}{v_{in,OTA}}\Big)^2 \Big(\frac{v_{in,IA,OTA}}{v_{n,OTA,out}}\Big)^2 = \Big(\frac{C_1 + C_P + C_2}{C_2}\Big)^2 \Big(\frac{C_2}{C_1}\Big)^2 \tag{2.8}$$

or,

$$\overline{v^2_{in,IA,OTA}} = \Big(1 + \frac{C_2}{C_1} + \frac{C_P}{C_1}\Big)^2 \quad \overline{v^2_{in,OTA}} \tag{2.9}$$

- Similarly, the the contribution of $v_{n,R2}$ can be referred to the input at node 'Y' and be

represented as $v_{in,IA,R2}$ [68].

$$\overline{v_{in,IA,R2}^2} = \Big(\frac{1}{1+sR_2C_2}\Big)^2\Big(\frac{1}{K_{mid}^2}\Big)\ \overline{v_{n,R2}^2} \tag{2.10}$$

- Hence, the input-referred noise contribution from the pseudo-resistor R_2 is scaled by the mid-band gain of the amplifier K_{mid} and gets attenuated at 20 dB/dec. after the sub-Hz corner frequency $\frac{1}{2\pi R_2C_2}$ (also apparent from Fig. 2.4d). This noise is negligible compared to the flicker or thermal noise [68].

- The total input-referred noise power of the overall IA at node 'Y' is

$$\overline{v_{in,IA}^2} = \overline{v_{in,IA,OTA}^2} + \overline{v_{in,IA,R2}^2} \tag{2.11}$$

- The capacitor C_1 AC-couples the ECG signal into the amplifier to reject large DC offsets from the electrode-tissue interface. The value of C_1 must be small enough to increase the input impedance ($Z_{in} = \frac{1}{sC_1}$) and hence avoid attenuation of the input signal from the electrode. At the same time it should be large enough to attenuation from the capacitive divider it forms with C_P [68, 125]. Moreover to minimize the 1/f noise of the OTA, its inputs transistors need to be of large size, increasing the value of the parasitic capacitance C_P. This in turn increases the input-referred OTA noise $v_{in,IA,OTA}$ (from equation 2.9). To counter this increase in noise, the value of C_1 can be increased, but at the cost of area. [126, 127] mention that input impedance needs to be greater than 10 MΩ while keeping C_1 lesser than 100 pF.

- Since the ECG signal has a near DC bandwidth, $1/f$ noise dominates the input-referred noise of the amplifier. According to [68] the input-referred noise of the IA should be kept below 10 μV.

Other Important Design Considerations

- As can be seen in Fig. 2.3, the IA should also be able to remove any common mode signal appearing at its input like the 50/60 Hz power line interference and the background noise. Hence, the IA designed should have a CMRR greater than 100 dB [99, 128].

- The recyclic folded cascode (RFC) architecture should be chosen over its counterpart folded cascode (FC) for the implementation of the OTA as it renders an efficient bandwidth improve-

ment for same power budget. The bandwidth improvement is achieved by using push-pull architecture [129, 130].

- The g_m/I_D methodology should be employed for sizing of the transistors of the OTA since it offers best trade-off between power consumption and performance i.e. linearity, unity gain bandwidth, noise, etc. [131–137].

- Another important aspect in the design of the amplifier is that it is not viable to achieve a high value of gain ($\sim$ 1000 or 60 dB) from a single stage. The reasoning behind this argument can be explained using Fig. 2.5a.

$$x_i = x_s - x_f = \frac{1}{1 + A\beta} \quad x_s \tag{2.12}$$

where, A represents the feed-forward gain or the open loop gain of the amplifier, β is the feedback gain ($= \frac{C_2}{C_1}$ in Fig. 2.4a), x_s is the input signal, x_o is the output signal, and x_f is the portion of x_o being fedback to the input of the feedforward amplifier. Also, the closed loop gain of the feedback system is given by

$$A_{CL} = \frac{x_o}{x_s} = \frac{A}{1 + A\beta} \approx \frac{1}{\beta} \qquad for \quad A\beta \gg 1 \tag{2.13}$$

To obtain a high value of A_{CL} in the order of 60 dB, β has to be small. But, equation 2.12 implies that the magnitude of the effective input to the feed-forward amplifier in a negative feedback system, x_i, increases with a smaller values of β. This in turn may degrade the linearity of the output of the amplifier. The same argument is true for each individual stage comprising the overall amplifier. Therefore, the overall desired gain needs to be distributed over 2-3 stages.

- Another important conclusion can be derived using the one-pole approximation of the open loop amplifier. Consider modeling the open-loop amplifier as

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_p}} \tag{2.14}$$

where, A_0 is the DC open-loop gain and ω_p is the open-loop -3 dB angular frequency. For any frequency $\omega \gg \omega_p$, the unity-gain frequency of the open-loop amplifier can be obtained by taking modulus of both sides substituting unity on L.H.S and frequency equal to ω_u on R.H.S

of equation 2.14. Solving for ω_u in terms of A_0 and ω_p can be expressed as

$$1 = \frac{A_0}{\sqrt{1 + \frac{\omega_u^2}{\omega_p^2}}} \qquad \Rightarrow \quad \omega_u \approx A_0 * \omega_p \tag{2.15}$$

Thus, the open-loop unity-gain frequency is also called the gain-bandwidth product, $\omega_{GBW,OL}$. The closed-loop transfer function of the feedback loop with the above assumptions can be expressed as

$$A_{CL} = \frac{\frac{A_0}{1+\frac{s}{\omega_p}}}{1 + \left(\frac{A_0}{1+\frac{s}{\omega_p}}\right)\beta} = \left(\frac{A_0}{1 + A_0\beta}\right)\left(\frac{1}{1 + \frac{s}{\omega_p(1+A_0\beta)}}\right) \tag{2.16}$$

While the first and second term in equation 2.16 represent the DC closed-loop gain G_{F0}, and the closed-loop pole frequency ω_{pF}, respectively. Assuming that the loop gain $A_0 * \beta \gg 1$, both these parameters can be written as

$$G_{F0} = \frac{1}{\beta}\frac{A_0\beta}{1 + A_0\beta} \approx \frac{1}{\beta} \quad ; \quad \omega_{pF} = (1 + A_0\beta)\omega_p \approx A_0\beta\omega_p \tag{2.17}$$

From the above expression, the closed-loop gain-bandwidth product is given by

$$\omega_{GBW,CL} = G_{F0} * \omega_{pF} = A_0\omega_p \tag{2.18}$$

Comparing equation 2.15 and equation 2.18, it can be concluded that

$$\omega_{GBW,CL} = \omega_{GBW,OL} \tag{2.19}$$

Hence, ω_{GBW} is same for the open-loop and closed-loop amplifier [138]. This implies that while designing the OTA for the IA, it can be designed starting with the parameter ω_{GBW}, since the $\omega_{GBW,CL}$ is known from the performance specifications provided by the application (ECG acquisition here).

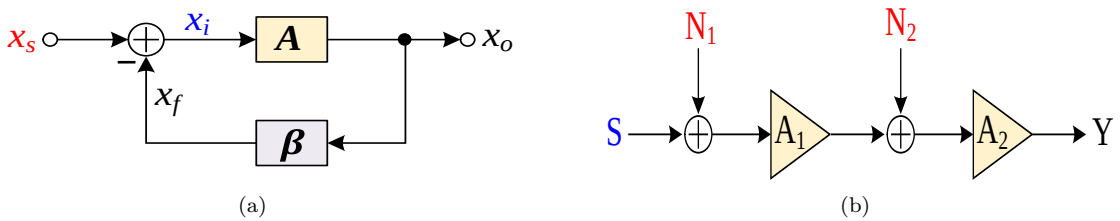


Figure 2.5: (a) Block diagram of a negative feedback system, (b) Noise in a multi-stage amplifier.

- At this juncture, it is apt to mention that the circuit noise of the first stage dominates the overall noise of the amplifier. This can be understood using an example of a two stage amplifier as shown in Fig. 2.5b. The net SNR at the output 'Y' is expressed as

$$SNR_Y = \frac{SA_1A_2}{N_1A_1A_2 + N_2A_2} = \frac{S}{N_1 + \frac{N_2}{A_1}} \tag{2.20}$$

  where, S is the input signal, N_1 and N_2 are the input-referred circuit noises of the first stage and second stage,and A_1 and A_2 are the closed loop gains of the first stage and second stage, respectively. It is evident from equation 2.20 that for a large value of A_1, the overall SNR is dependent only on N_1.

- The above discussion also hints that it is better to design the first stage with a higher gain than the second stage so that the overall SNR depends primarily on the noise of the first stage. Moreover, the second stage can be implemented to provide programmable gain. The first stage with a comparatively large but fixed gain is called the instrumentation amplifier and next stage with programmable gain is called the programmable gain amplifier (PGA).

- A figure of merit, noise efficiency factor (NEF), is introduced in [139] to deduce the power-noise trade-off and compare different state-of-the-art IA implementations.

$$NEF = V_{rms,in}\sqrt{\frac{2.I_{tot}}{\pi U_T.4kT.BW}} \tag{2.21}$$

  where, $V_{rms,in}$ is the total equivalent input noise voltage, I_{tot} is the total current drained in the system, k is the Boltzman constant equal to $1.3810^{-}23\ m^2kgs^{-2}K^{-1}$, U_T is the thermal voltage at 300 K ($= kT/q \approx 0.02586\ V$), and BW is the frequency bandwidth. NEF represents the normalization of the input-referred noise of the amplifier to the input-referred noise of a single BJT draining an equal amount of current. It helps us compare two circuits with equal supply voltages [140].

- However, as can be implied from equation 2.21, there may be cases where two amplifiers with the same total current and noise, but different supply voltages will exhibit equal NEF, but still be dissipating different powers. In such cases, NEF might turn out to be an inefficient metric to ascertain which among the two is more power efficient. To avoid such an ambiguity, [140]

introduces a more efficient metric called the power efficiency factor (PEF) and is expressed as

$$PEF = NEF^2.VDD \tag{2.22}$$

where, VDD is the supply voltage.

2.1.6 Automatic Gain Control

It is well known that the strength of the ECG signal depends on the location of the electrodes and varies from patient to patient. Moreover, the ADC achieves maximum SNR for a certain range of input amplitudes. Therefore, it is essential that the input of the PGA is amplified to a level which corresponds to level yielding maximum SNR. In addition to that, the gain of the amplifier, being determined by the capacitor ratios, may deviate from its nominal value due to component related mismatches. This brings out the need of an automatic gain control (AGC) circuit which can ensure that the output of the PGA reaches the desired level. The automatic gain control module determines the gain of the PGA (labeled ⑥ in Fig. 2.1b). It is a Mealy machine implemented on analog platform.

2.1.7 High-pass Filter

Various sources introduce a near-DC electrode offset voltage (EOV) component in the input ECG signal called baseline wandering. The major sources for this effect are (i) electrode-offset caused by skin-electrode interface due to variations in the quality of the skin-electrode contacts; (ii) motion artifacts emanating from the fluctuation in the skin potential due to stretching, deformation, and pressing on the skin and breathing or movement of the patient. The fact that the amplitude of motion artifact can go up to ten times that of the ECG signal limits the maximum gain that the PGA provides, since at higher gains this offset can saturate the signal chain. A high-pass filter with cut-off frequency below 1 Hz is employed to (i) isolate the DC voltage of the body, and hence allows the designer to do away with the right leg drive electrode (RLD) [141]; (ii) remove EOV; (iii) remove baseline wandering. Moreover, a ramp in the ST segment at the output of the PGA is observed if the high-pass cut-off frequency is lesser than 50 mHz [142]. The International Electro-technical Commission 60601 Part 2-47 sets the minimum requirement of handling +/-300 mV electrode offset [143].

Since implementing sub-Hz cut-off frequencies (or large time constants) would involve large

passive capacitors and resistors, off-chip components have been used in [62,144]. To have an idea of the huge area cost, it is worth noting that a 1 MΩ resistor 'RNHR' occupies an area of 1 $\mu m \times 1$ mm in UMC 180 nm CMOS technology. Similarly, a 1 pF 'MIMCAP' capacitor occupies an area of 30 $\mu m \times$ 30 μm in the same technology. Therefore, integrating the filter on-chip offers the following advantages (i) reduction on area cost; (ii) decrease in noise coupling (external spurious noise pickup); and (iii) increased reliability and manufacturability. Prior published works use a feasible value of on-chip capacitor and achieve a large value of resistance using MOS-bipolar pseudo-resistor [145], balanced tunable pseudo-resistor [1], floating-gate based reconfigurable pseudo-resistor [146] or gate-balanced pseudo-resistors [70]. The design challenge is to minimize the large variation of resistances under positive and negative biasing conditions, leading to a serious DC biasing offset at the output node. This nonlinearity of feedback pseudoresistors substantially degrades linearity and dynamic range in low-frequency operation, specially in low-voltage operation [1].

The solution would be to use thick-oxide PMOS devices and use a configuration which overcomes the problem of asymmetric and nonlinear resistances when the voltage across the pseudo-resistor varies e.g. [1,70,141,145,147]. Based on the above discussion, in this work, the high-pass filter 3-dB frequency is chosen to be 50 mHz (labeled ⑦ in Fig. 2.1b) and RLD is avoided. In the absence of RLD circuit, the powerline interference is supposed to be removed by digital filters after the ECG front-end.

The HPF and LPF together forms a bandpass filter (BPF).

2.1.8 Summary

The previous section is used as a preamble to the design of the targeted ECG acquisition system. The final schematic of the system is shown in Fig. 2.6. The complete system can be divided into two parts, viz. acquisition and classifier. The acquisition part can further divided into signal conditioning and digitization. The amplifier along with bandpass filter, AGC and the AFT constitute the signal conditioning portion of the system. Then the $\Sigma\Delta$ ADC is employed for digitization. Besides the blocks in Fig. 2.1, a classifier block has been introduced. It comprises a fully analog scheme comprising (i) an ultra low power on-line QRS detection circuit using an autonomous dynamic threshold voltage (ii) a power efficient analog classifier for the detection of three of the critical alarm types *viz.* asystole, extreme bradycardia and tachycardia. In the event of detection of any one of the three target cardiac disorders, the system raises an immediate alarm.

As an important value addition to the acquisition systems shown in Fig. 2.6, the proposed

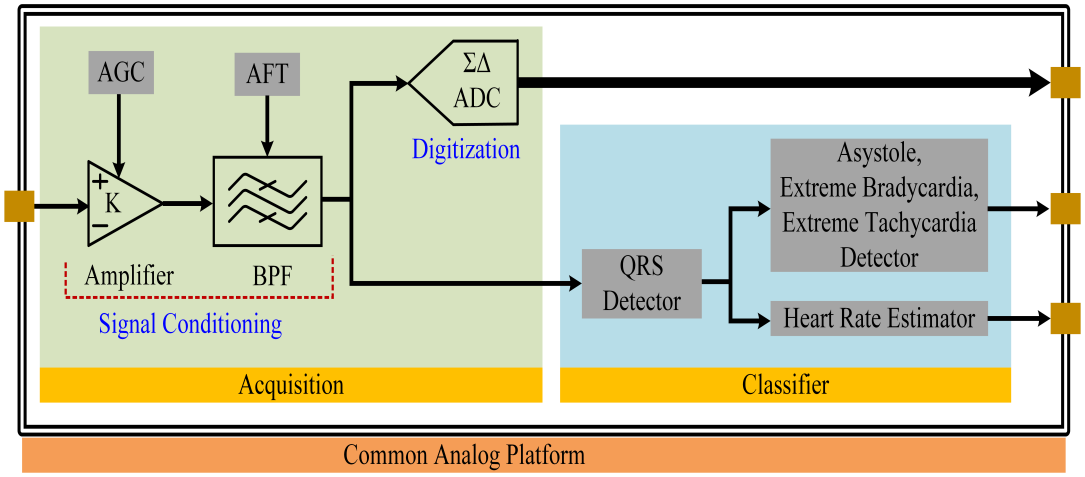


Figure 2.6: Proposed scheme and scope of work.

scheme intends to alert the proximate medical service agency in case of remote monitoring, and alert the hospital staff in case of in-hospital patients. Also it is worth mentioning from clinical application perspective that the prime purpose of this system is to classify and hence assist in the preliminary prognosis of the above mentioned abnormalities. A more accurate, detailed and unequivocal diagnosis of the patient's clinical condition is still assigned to the more computationally intensive and power hungry DSP. Therefore, the proposed classification scheme presents a useful trade-off between complexity, accuracy and power consumption. The target specifications for the AFE are summarized in Table 2.2.

A detailed procedure for design, analysis and obtained results are presented in the subsequent chapters.

Table 2.2: Target specifications for the ECG acquisition system

IA	
Parameter	**Specification value**
Dynamic range	0.1-1 mV
BW	0.05-250 Hz
Architecture	Capacitive-coupled, capacitive feedback
Z_{in}	$>$ 10 MΩ
CMRR	$>$ 100 dB
Input-referred noise	$<$ 10 μV
OTA topology	RFC
Gain	40-60 dB
Linearity	$>$ 60 dB (10 bits)
ADC	
Topology	opamp-shared ΣΔ modulator
Resolution	10 bits
Order	2^{nd}

Chapter 3

Design of Amplifier and ADC for ECG Acquisition

3.1 Introduction

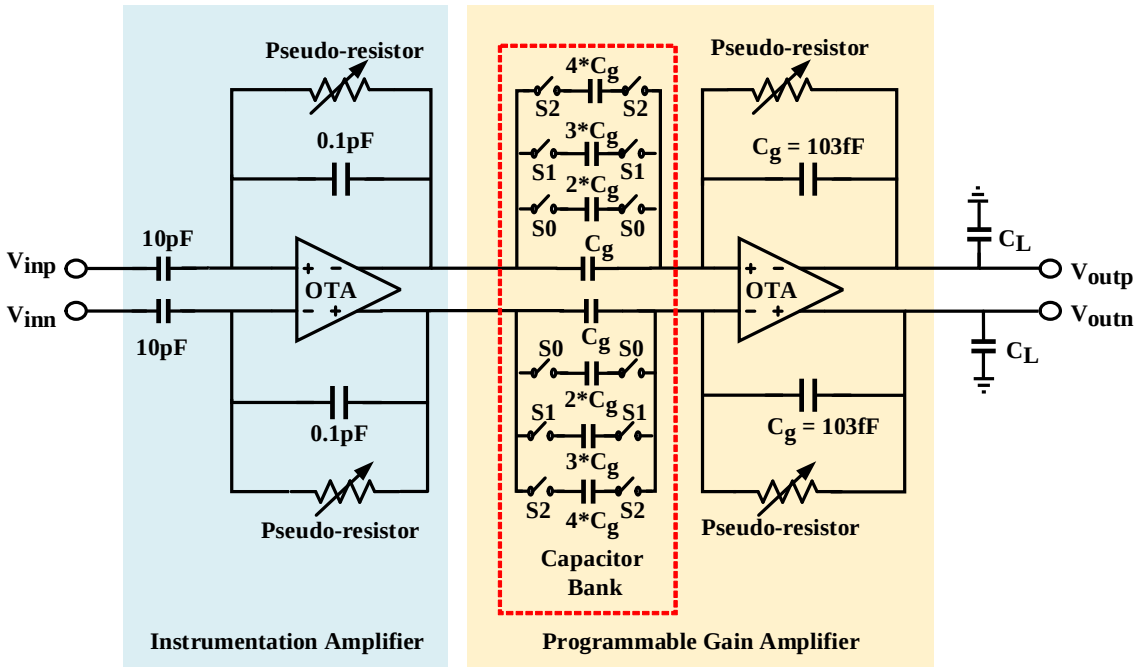
This chapter presents the design of the ultra low power amplifier and ADC required for the acquisition, amplification, bandpass filtering, finally, digitization of an ECG signal. The major design considerations and primary target performance specifications mentioned in Chapter 2 lay the roadmap for the implementation of each of the constituent blocks. The design flow employed to achieve the target performance is provided in detailed and stepwise manner. Utilizing the UMC 180 nm CMOS technology for implementation of the desired circuit, both the simulation and measurement results obtained are presented and discussed adequately.

3.2 ECG Amplifier Design

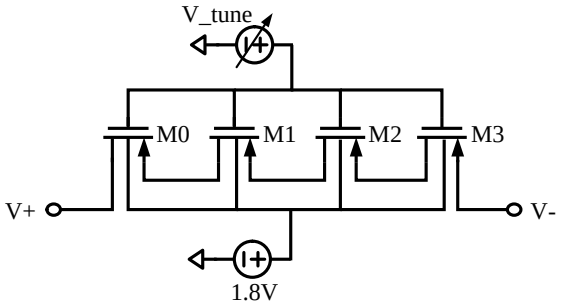
While the important features and approximate specifications of the same have already been discussed in the previous chapter, this chapter discusses the design in detail. The schematic of the two-stage ECG amplifier designed is given in Fig. 3.1a.

The design flow is as given below:

- The dynamic range of the input ECG signal amplitude is considered to be 0.1-1 mV. A gain of 100-1000 is desired here to ensure that the output signal amplitude is approximately 100 mV.



(a)



(b)

Figure 3.1: Schematic diagram of the (a) amplifier for the ECG front-end, (b) MOS based implementation of the pseudo-resistor shown in (a).

- The first stage, or the IA, provides a fixed gain of 100 ($= \frac{10\ pF}{0.1\ pF}$).
- The second stage, or the PGA, provides a variable gain from 1-10. The different combinations of the capacitors from the capacitor bank determines the gain of the PGA. The different capacitor combinations are in turn determined by the different combinations of the control switches - S0, S1 and S2. The switches can be controlled either through external pins as in [62], or through an AGC circuit. A detailed discussion on the formulation of the target AGC is presented in the next chapter.

- The schematic of the pseudo-resistor used for obtaining the sub-Hz high pass cut-off frequency

is shown in Fig. 3.1b. The highpass cut-off frequency can be tuned using the control voltage V_tune.

Low power dissipation and minimum input refereed noise of the overall amplifier are the prime concerns while designing the constituent OTA. The procedure of designing the OTA is discussed in next subsection.

3.2.1 OTA Design

A detailed and step-wise procedure to bias and size the OTA while targeting minimum power consumption and input-referred noise is provided here. The specifications of the closed-loop IA provide the starting point for the design of the OTA. The g_m/I_D methodology for sizing the transistors is adopted here to optimize the power and noise, and is summarized in Fig. 3.2 [131, 148].

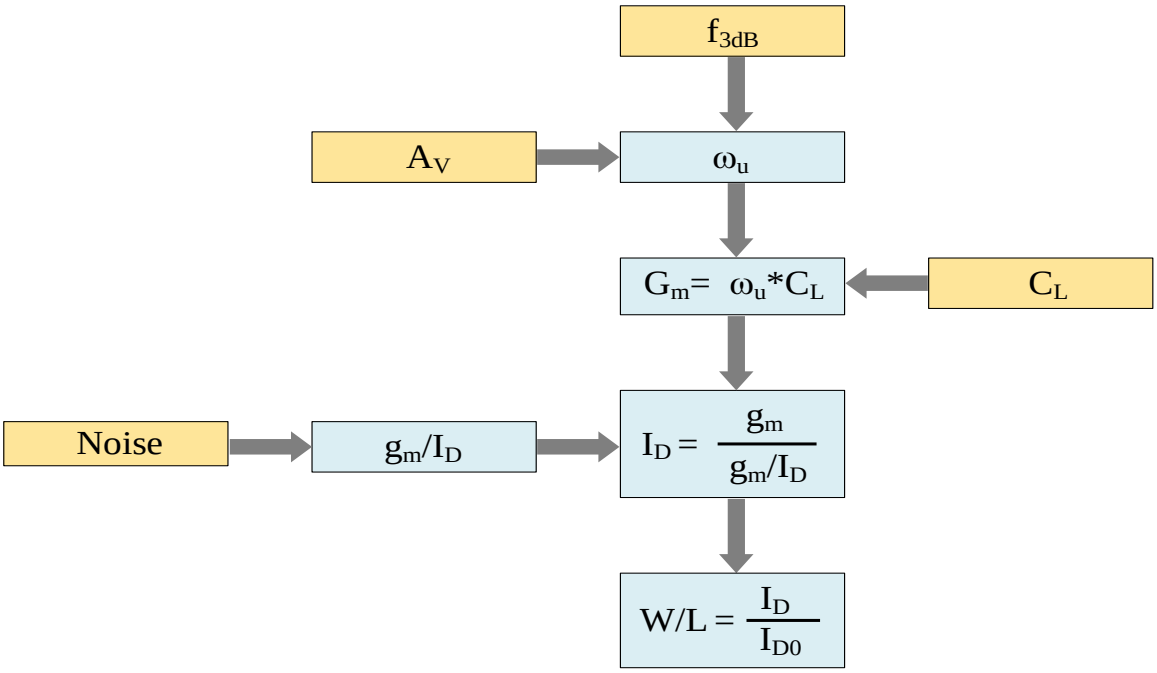


Figure 3.2: Flow chart illustrating the steps involved in the design of the desired OTA.

- f_{3dB} is the closed-loop low pass cut-off frequency of the IA. It is equal to 250 Hz for ECG signals. Similarly, A_v is the closed-loop gain of the IA. It is equal to 100 for the first stage IA. Thus the closed-loop unity-gain frequency, $\omega_{GBW,IA}$ is given by

$$\omega_{GBW,IA} = f_{3dB} * A_v = 250\ Hz \times 100 = 25\ kHz \tag{3.1}$$

- From equation 2.19, it concluded that the unity-gain frequency of the open-loop amplifier is equal to that of the closed-loop amplifier. Therefore the unity-gain frequency of the OTA, ω_u, is derived from equation 3.1.

$$\omega_u = 25\ kHz \tag{3.2}$$

- Considering a load capacitance of 12 pF, the equivalent transconductance of the OTA, G_m is given by

$$G_m = \quad \omega_u * C_L = \quad 25\ \ kHz \times 12\ pF \quad = \quad 300\ nS \tag{3.3}$$

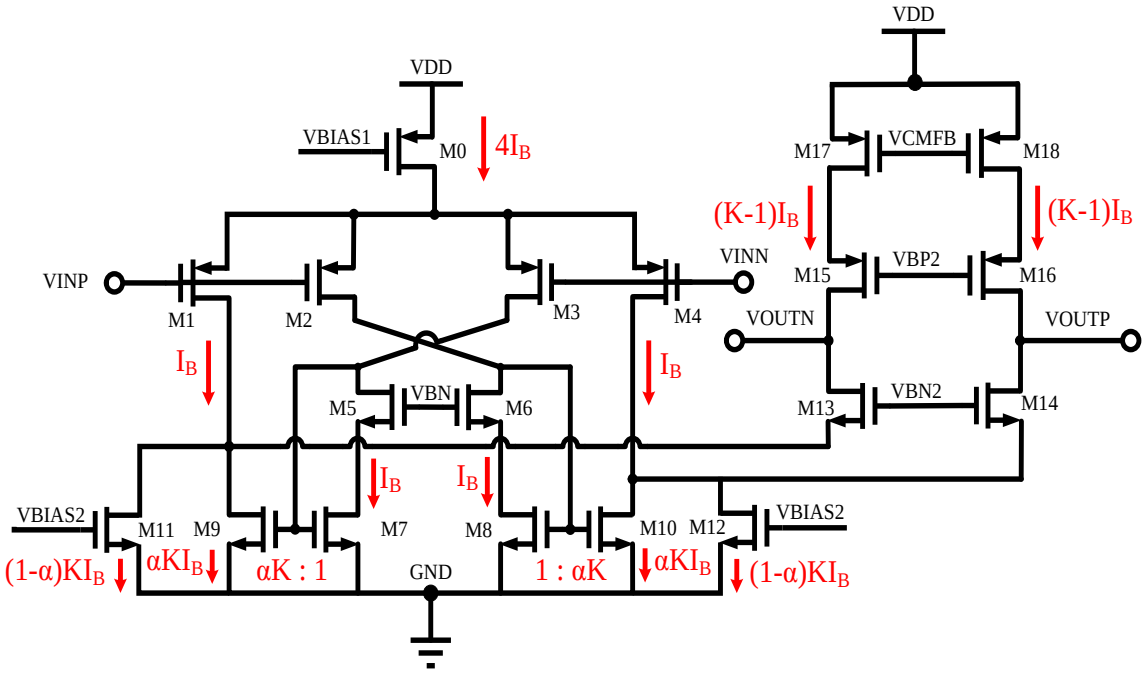


Figure 3.3: Circuit diagram of the RFC OTA.

- The modified RFC topology is proposed here and is shown in Fig. 3.3. The OTA is designed with PMOS input transistors to minimize the incurred flicker noise. Conventionally, the RFC OTA does not have transistors M11 and M12, the ratio of transconductance of M9 to M7 (and M10 to M8) is $(K:1)$. The differential and common mode gains are expressed as

$$\begin{aligned} |A_{v,DM}| &= g_{m1}(K+1) * \Big(g_{m13}r_{13}(r_{o1}||r_{o18})||g_{m15}r_{o15}r_{o17}\Big), \\ |A_{v,CM}| &= \frac{g_{m1}(K-1)}{1+g_{m1}r_{o0}} * \Big(g_{m13}r_{13}(r_{o1}||r_{o18})||g_{m15}r_{o15}r_{o17}\Big). \end{aligned} \tag{3.4}$$

In the proposed topology, a g_m cancellation technique is implemented using transistors M11

and M12, along with a factor α, so that the ratio of transconductance of M9 to M7 (or M10 to M8) becomes $(\alpha * K : 1)$. The DC current flowing through the transistors M9 and M10 in the conventional architecture is bypassed through transistors M11 and M12, which decreases g_{m9}. The differential and common mode gains of this modified RFC are expressed as

$$\begin{aligned} |A_{v,DM}| &= g_{m1}(\alpha * K + 1) * \Big(g_{m13}r_{13}(r_{o1}||r_{o18})||g_{m15}r_{o15}r_{o17}\Big), \\ |A_{v,CM}| &= \frac{g_{m1}(\alpha * K - 1)}{1 + g_{m1}r_{o0}} * \Big(g_{m13}r_{13}(r_{o1}||r_{o18})||g_{m15}r_{o15}r_{o17}\Big). \end{aligned} \tag{3.5}$$

Also, the value of α is chosen so that the product $(\alpha * K)$ tends to unity, which in turn forces $A_{v,CM}$ in equation 3.5 to tend to zero. This increases the CMRR significantly, and hence satisfies the requirement of an ECG amplifier to reject all kinds of common mode input signals.

- G_m can be expressed in terms of individual transconductance of the input transistors (i.e. M1, M2, M3 and M4), g_m as

$$G_m = (1 + \alpha K) * g_m \tag{3.6}$$

For the IA, the OTA is designed with $K = 3$ but $\alpha * K = 1$. Then, the value of g_m is obtained as

$$g_m = \frac{G_m}{1 + \alpha K} = \frac{300\ nS}{1 + 1} = 150\ nS \tag{3.7}$$

- Moderate inversion region of operation for transistors is chosen to reduce the power consumption of the design. Since the ECG is a low bandwidth signal, the flicker noise is more a cause of concern than the thermal noise. Therefore, a high value of g_m/I_D, equal to 25 V^{-1}, is chosen to minimize the incurred flicker noise.

- The desired drain current of each of the input transistors, I_D, can be obtained by using

$$I_D = \frac{g_m}{\left(\frac{g_m}{I_D}\right)} = \frac{150\ nS}{25\ V^{-1}} = 6\ nA \tag{3.8}$$

Note that I_D in the above equation is equal to the bias current I_B shown in Fig. 3.3.

- Using the expression of the drain current of a MOS transistor in saturation region, the bias voltage $(V_{GS} - V_{th})$ can be estimated from the value of chosen g_m/I_D using the expression

$$\frac{g_m}{I_D} = \frac{1}{V_{GS} - V_{th}} \tag{3.9}$$

Since the moderate region of operation is an interpolation between the weak inversion and strong inversion, the above expression is valid for biasing the proposed OTA also.

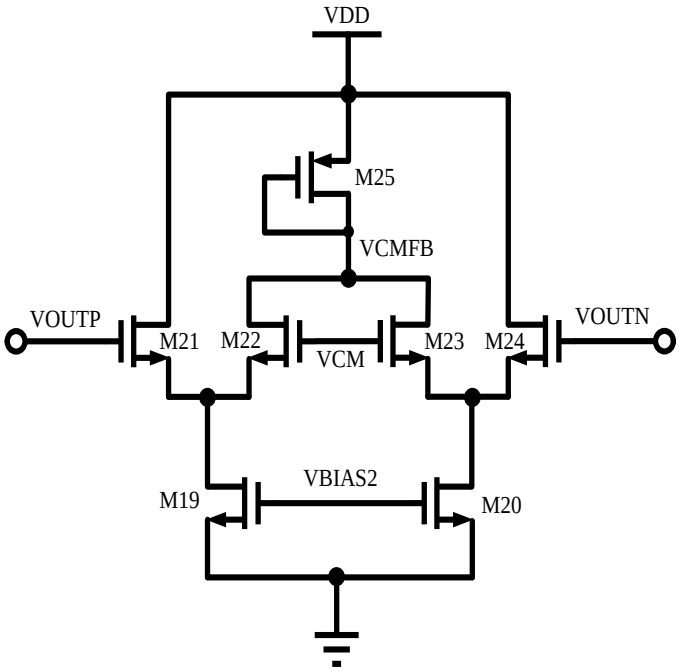


Figure 3.4: Circuit diagram of the CMFB for the OTA .

- The circuit of the common mode feedback (CMFB) circuit for the OTA is shown in Fig. 3.4. Note that the gate potentials of the input transistors of the CMFB circuit is labeled $VOUTP$ and $VOUTN$ (same as that of the output voltages of Fig. 3.3) to maintain consistency with OTA circuit. Also, the output of the CMFB circuit is labeled $VCMFB$ for the same reason. It has a gain of unity. Equation 3.5 shows that the OTA exhibits a reduced effective transconductance for common mode signals compared to differential signals. The CMRR is further improved by using a CMFB circuit. With the CMFB circuit, the effective output resistance (second term in Equation 3.5) reduces significantly, thereby further improving the CMRR. The common mode gain of the OTA with CMFB circuit is given by

$$|A_{v,CM-CMFB}| = \frac{g_{m1}(\alpha * K - 1)}{1 + g_{m1} r_{o0}} * \frac{1}{g_{m18}} \tag{3.10}$$

- The next job is to bias and size all the transistors in the OTA using the g_m/I_D methodology.
  - The OTA in Fig. 3.3 is designed such that the following condition is satisfied.

$$g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m7} = g_{m8} = g_{m9} = g_{m10} \tag{3.11}$$

- **M7** : The sizing starts with M7. Its drain current I_{D7} and overdrive voltage are fixed using equations 3.8 and 3.9. The $V_{DS,7}$ is approximated as $(V_{GS,7}-0.15)$, keeping in mind that $V_{DS,sat}$ in weak inversion region is greater than 104 mV at room temperature [148]. The value of $V_{GS,7}$ determines $V_{DS,9}$ and the drain potentials of M1 and M4.
- $V_{DS,11}$ is kept around 150 mV.
- **M1** : The equation 3.9 provides the overdrive voltage. Since $V_{G,1}$ is fixed at $V_{supply}/2$ (0.9 V here), only $V_{S,1}$ needs to be tweaked to obtain the desired $V_{GS,1}$. $V_{D,1}$ is determined by the dtain potential of M7.
- **M13** : $V_{S,13}$ is equal to the $V_{D,7}$. $V_{D,13}$ is fixed at $V_{supply}/2$ (0.9 V here). The gate potential of M13 is fixed so that M13 has a high transconductance.
- **M17** : $V_{S,17}$ is equal to V_{supply} (1.8 V here). The drain and gate potentials are chosen to keep it in saturation so as to obtain a good current source. M15 can also be sized similarly. M0 is operated in saturation region for the same reason.

- The device sizes and bias parameters are tabulated in Table 3.1 below.

Table 3.1: Device parameters of the RFC OTA of IA

Device	**W/L** (μm)	$I_D(nA)$	g_m/I_D (V^{-1})
M0	1.54/10	25.68	17.26
M1,2,3,4	4.7/10	6.419	24.17
M5,6	3.28/10	6.419	28.74
M7,8	1.29/30	6.419	23.64
M9,10	1.6/30	8.468	23.53
M11,12	1.9/30	10.77	23.35
M13,14	1.59/10	12.82	25.48
M15,16	9.3/10	12.82	24.22
M17,18	0.79/10	12.82	17.36
M19,20	3.21/30	20.04	23.11
M21,22	25.06/30	9.983	30.64
M23,24	25.65/30	10.06	30.6
M25	3.7/30	20.12	17.43
Bias Voltages			
Label	**Value (V)**	**Label**	**Value (V)**
VBIAS1	1.3	VBN	0.4
VBIAS2	0.3	VBN2	0.6
VCMFB	1.3	VBP2	0.9
VCM	0.9	–	–

- The schematic diagram of the circuit generating the bias voltages required by the OTA is given in Fig. 3.5 [149,150]. The device dimensions are tabulated in Table 3.2.

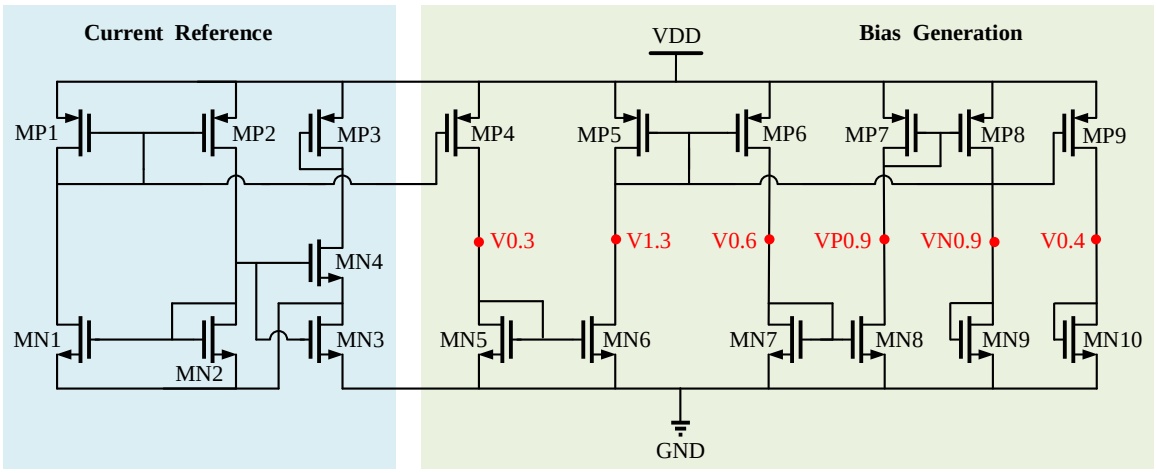


Figure 3.5: The bias generation circuit for the OTA. The node voltages are labeled in a format 'VX', where 'X' is the voltage generated in volts.

Table 3.2: Device sizes of the bias generation circuit for the IA

Device	W/L(μm)	Device	W/L(μm)	Device	W/L(μm)	Device	W/L(μm)
MP1	90/10	MN3	1/0.18	MP7	1.01/30	MN7	0.24/30
MP2	90/10	MN4	0.24/30	MP9	31.66/30	MN8	0.6/30
MP3	0.24/10	MP4	1.9/30	MP8	4.43/30	MN10	4.01/30
MN1	0.24/30	MP5	5/30	MN5	1.44/30	MN9	0.6/30
MN2	0.24/30	MP6	17.77/30	MN6	4.2/30	–	–

- The PGA is implemented with $K = 3$ and $\alpha = 1$.

Noise Considerations in OTA Design

The aim of the qualitative noise analysis is to derive an expression for the overall noise generated due to all the transistors comprising the OTA, which lays down the guidelines while sizing the individual devices so as to minimize the noise at the output nodes. Owing to the low bandwidth of the ECG signals, the flicker noise dominates the overall input referred noise of the OTA. A detailed analysis of the total input referred flicker noise of the OTA is given in Appendix B. The total input referred flicker noise of the OTA is adopted from Appendix B and is given as

$$\overline{V_{in,tot}^2} = \frac{K_p}{\mu_p C_{ox} W_1 L_1 f}\left[1 + \frac{1}{2}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_7 L_7} + \frac{1}{2}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_9 L_9} + (\frac{L_1}{L_{17}})^2 + \frac{K_n}{K_p}(\frac{L_1}{L_{11}})^2\right] \quad (3.12)$$

where, K_p and K_n are the process-dependent constants for PMOS and NMOS respectively, μ_p and μ_n are the process-dependent constants for PMOS and NMOS respectively and, W and L are the corresponding dimensions of the device.

This equation concludes that the length of the input transistor should be less compared to other transistors. Hence the transconductance efficiency, g_m/I_D, of the input transistors should be higher compared to other transistors.

3.2.2 Post-layout Simulation Results

The overall ECG amplifier including the IA (comprising of the RFC OTA described in the previous subsections) and the PGA is designed using UMC 180 nm 1P6M CMOS technology. The supply voltage is 1.8 V. The post-layout extracted simulations are done using Cadence Virtuoso. The results obtained and the important inferences about the performance parameters achieved thereof are provided below.

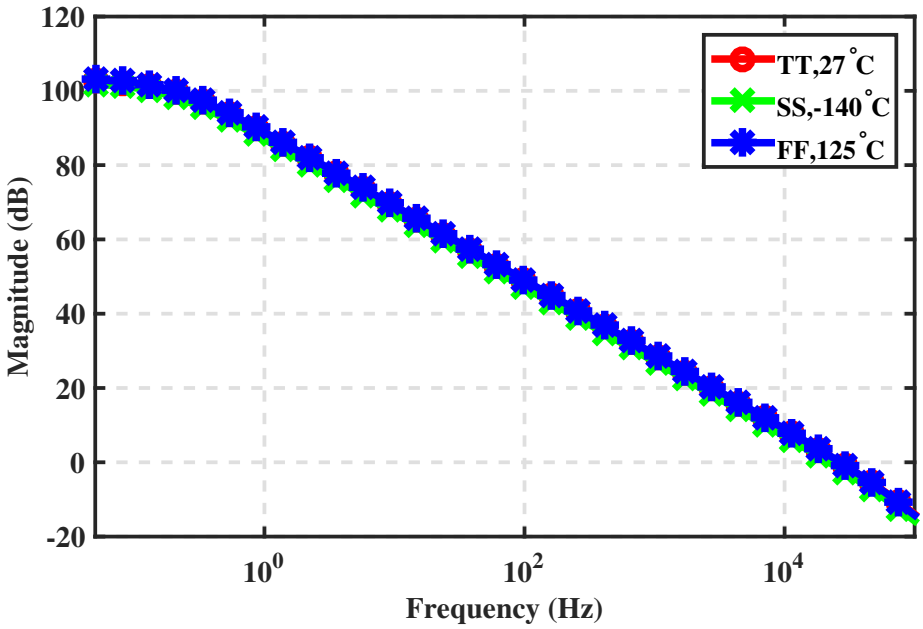


Figure 3.6: Open loop magnitude response of the RFC OTA of the IA across various process and temperature corners.

- Fig. 3.6 shows the loop gain magnitude response of the RFC OTA (see Fig. 3.3) for a differential input. As is evident that the open loop DC gain is approximately 100 dB. The post-layout extracted simulations are carried out for different temperature and process corners. In the Fig. 3.6 TT, SS and FF represent the typical-typical, slow-slow and fast-fast process corners, respectively. Simulation results show that the value of the DC gain remained same for worst case corner simulations.

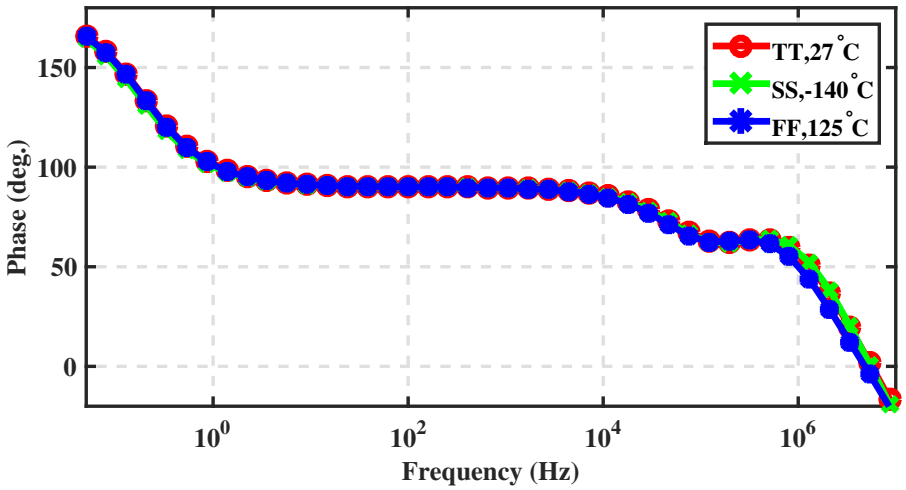


Figure 3.7: Open loop phase response of the RFC OTA of the IA across various process and temperature corners.

- The phase response of the same OTA for a differential input is shown in Fig. 3.7. It is apparent that the phase response is as desired and invariant across worst case process corners.

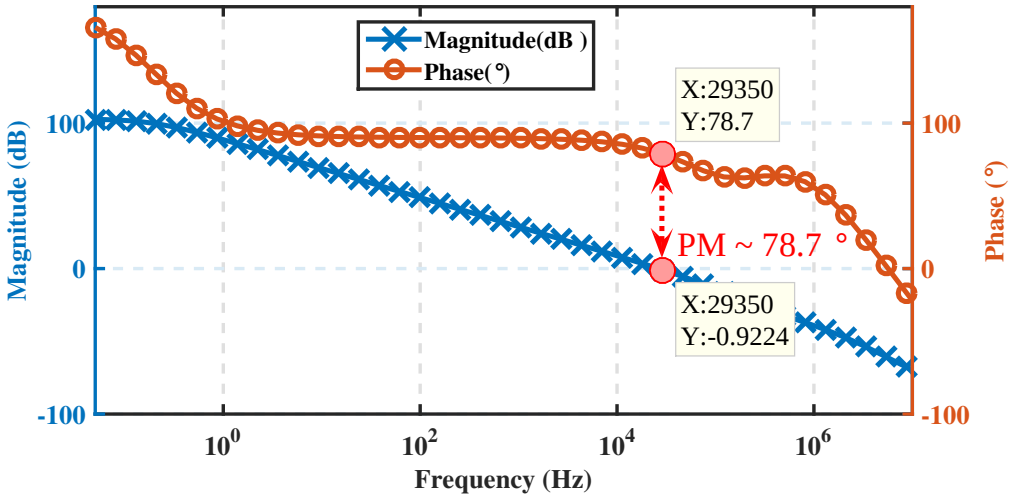


Figure 3.8: Open loop magnitude and phase response of the RFC OTA of the IA typical-typical process corner.

- Finally, both the magnitude and phase response for typical-typical process corner and a temperature of 300 K is shown in Fig. 3.8. It shows that the phase margin (PM) is approximately 78.7°, which proves the stability of the OTA.

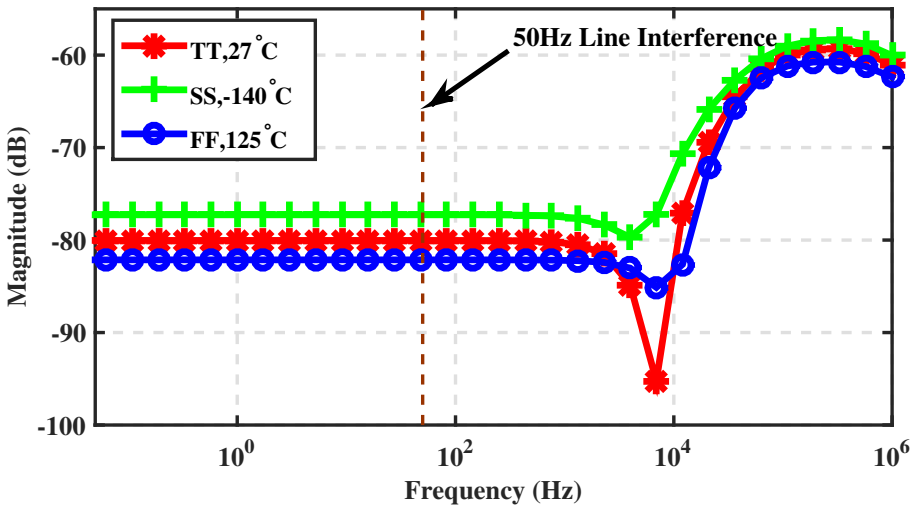


Figure 3.9: Open loop magnitude of the OTA with CMFB circuit for common mode input signals.

- The magnitude response of the OTA with the CMFB circuit for a common mode signal input is shown in Fig. 3.9. The common mode gain of the open loop OTA with the CMFB is approximately -80 dB even for worst case process corners. Therefore, the designed OTA with CMFB is particularly suitable for the high common mode rejection requirement of the ECG front-ends. It is important to observe that the designed topology efficiently rejects the 50 Hz power-line interference.

- Fig. 3.10 shows the loop gain of the loop comprising the OTA and the CMFB circuit. It can be observed that the loop has PM (= 78.7°) greater than 60° and is hence stable. Another important inference is that the UGB of this loop gain is greater than the UGB of the OTA alone (i.e. 2.5 kHz), proving that the viability of CMFB circuit throughout the UGB of the OTA.

- The spectral density of the integrated input referred noise of OTA with the CMFB circuit is shown in Fig. 3.11. The total input referred noise voltage for a bandwidth of 0.05-250 Hz is 9.56 μV.

- The contribution of each of the MOSFETs constituting the OTA with the CMFB circuit to the overall noise is tabulated in Table 3.3. As expected, the flicker noise dominates the total noise owing to the fact that ECG signal is a low bandwidth signal. Moreover, the percentage noise contribution of the individual devices is depicted in Fig. 3.12 to elaborate the same. Note

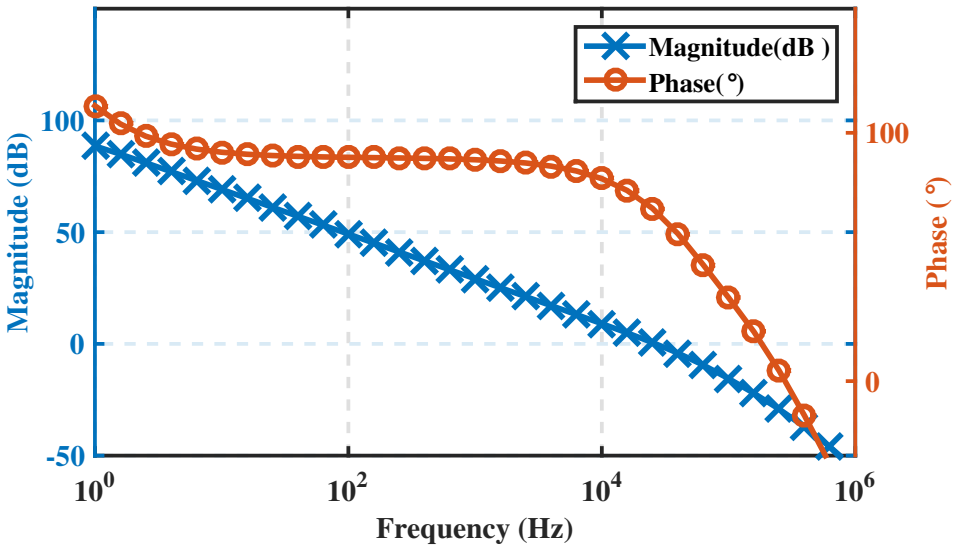


Figure 3.10: Loop gain of CMFB

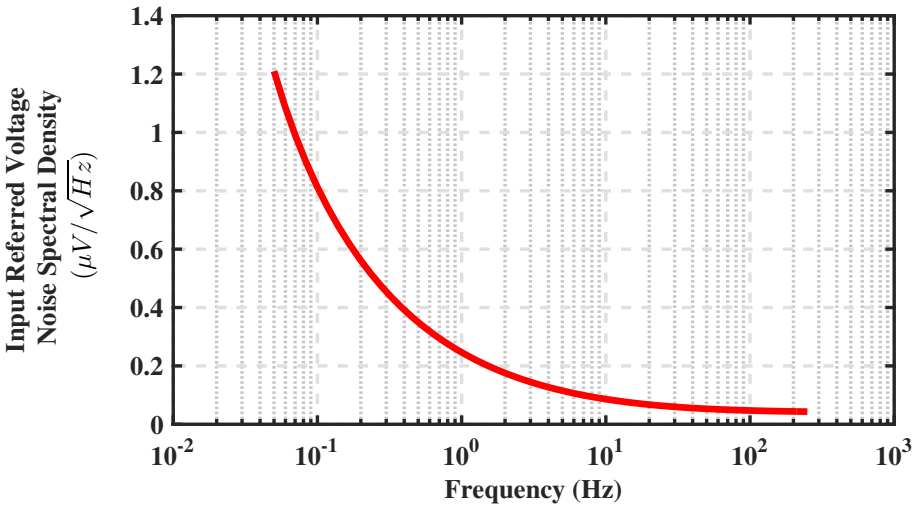


Figure 3.11: Input referred noise spectral density of the OTA with the CMFB.

that Fig. 3.12 exhibits the flicker noise contribution of the devices that are explicitly shown. Further, 'Others' include the summation of the noise contributed by rest of the devices, irrespective of the type of noise (flicker or thermal).

- The linearity of the output of the IA depends on the resistance offered by the pseudo-resistor. The resistance of the pseudo-resistor is plotted against the potential difference across it in Fig. 3.13 (V_tune = 1.8 V). It is apparent that the resitance is constant around the common

Table 3.3: Noise summary of the OTA

Device	Type of noise	% of total noise	Device	Type of noise	% of total noise
M17,18	fn	21.91	M7,8	id	0.05
M11,12	fn	7.62	M11,12	id	0.05
M7,8	fn	7.33	M17,18	id	0.04
M9,10	fn	5.79	M9,10	id	0.04
M2,3	fn	4.51	M2,3	id	0.04
M1,4	fn	2.59	M1,4	id	0.02

fn → flicker noise ; id → drain-source resistance thermal noise

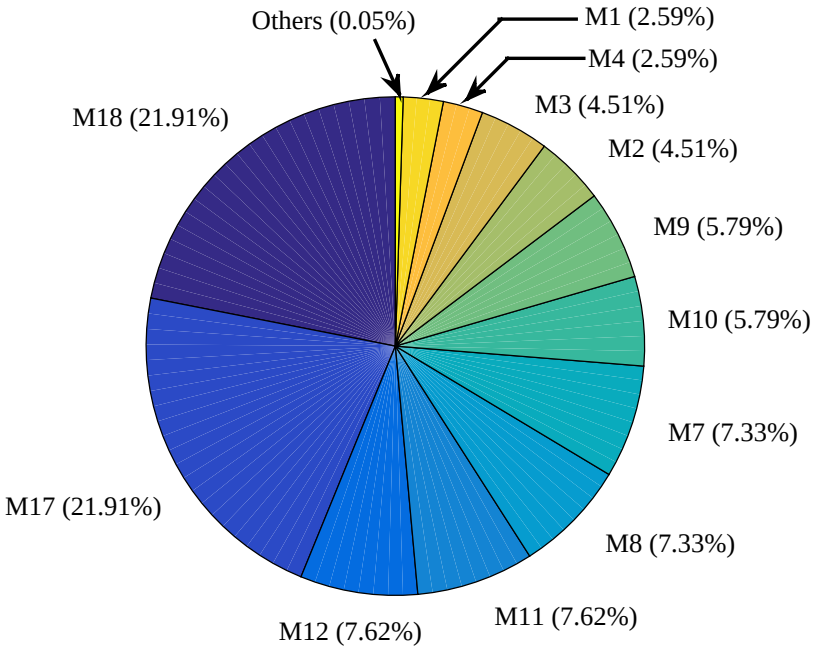


Figure 3.12: Pictorial representation of the contribution of each device to the overall noise using a pie-chart.

mode DC voltage (= 0.9 V here), and hence is expected not to be effecting the linearity of the IA.

- The power spectral density (PSD) of the differential output of the IA is depicted in Fig. 3.14. It exhibits a linearity of 75 dB approximately. Since the output of the PGA is input to the ΣΔ ADC, which targets an SNR of 10 bits (60 dB), the obtained level of linearity satisfies design requirements of the ADC.

- The highpass cut-off frequency depends on the resistance of the pseudo-resistor shown in Fig. 3.1b, which in turn depends on the gate voltage V_tune. Fig. 3.15 shows that the cut-off

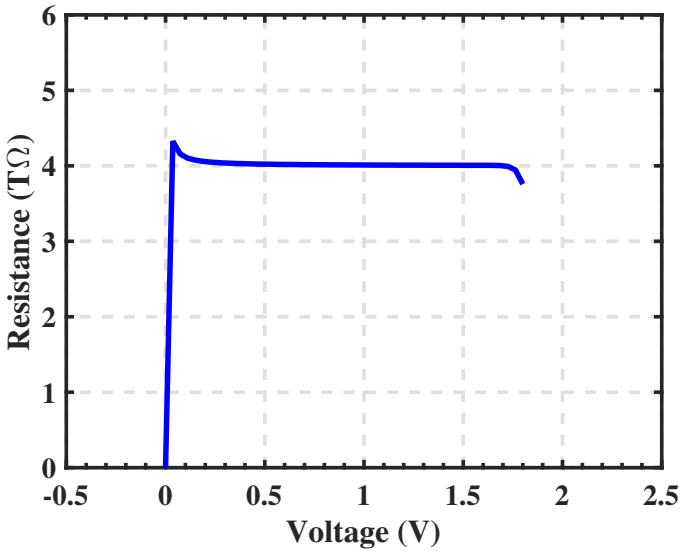


Figure 3.13: Resistance of the pseudo-resistor.

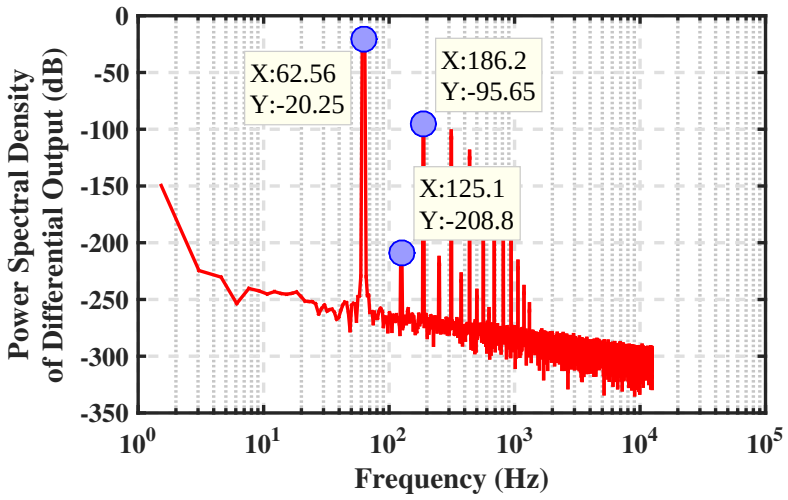


Figure 3.14: PSD of the differential output of the IA.

frequency can be controlled and varied using the V_tune, while keeping the mid-band gain and the lowpass cut-off frequency intact.

- The bias generation circuit in Fig. 3.5 consumes 3.878 μA for a supply voltage of 1.8 V.

After the required amplification and filtering, the ECG signal needs to be digitized so that it can be taken-up conventionally by a digital classifier. The $\Sigma\Delta$ modulator ADC is chosen here for the desired digitization. The following section discusses the design details of the same elaborately.

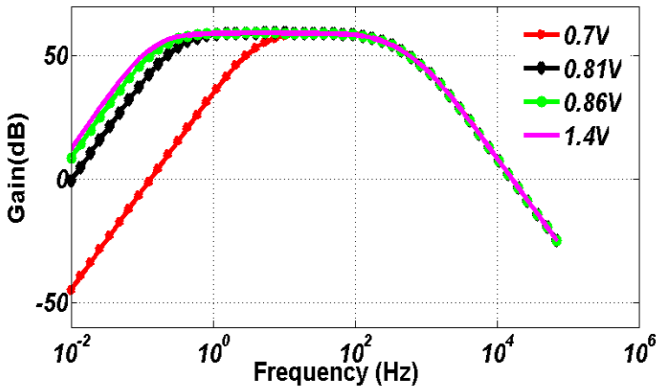


Figure 3.15: Reconfigurability of the HPF cut-off frequency.

3.3 Design of ΔΣ ADC for Digitization of ECG Signal

The ΣΔ ADC is chosen here for the digitization of the ECG signal because of the following reasons (i) relaxed requirement on the order of anti-aliasing filter, (ii) greater immunity to component mismatches, (iii) offers easier reconfigurability and (iv) requirement analog circuitry is quite simple. Other important aspects have already been discussed in the previous chapter.

An opamp-shared topology is employed here to obtain a second order noise-shaping while using a single OTA. A simplistic representation of a conventional second order 1-bit ΣΔ ADC using two

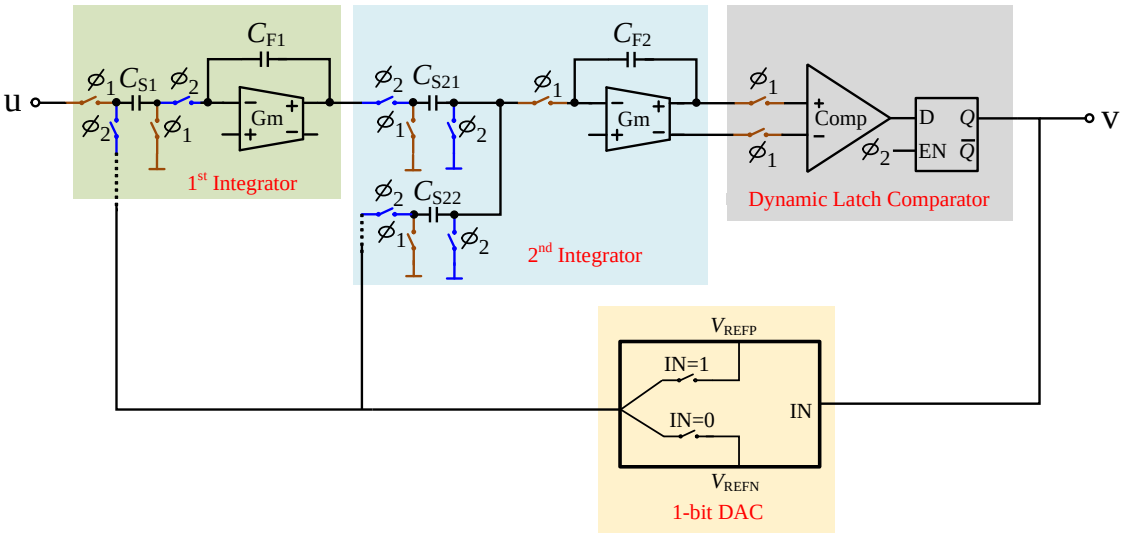


Figure 3.16: Schematic of the conventional second order ΣΔ ADC using two integrators.

integrators is given in Fig. 3.16 [151]. Two non-overlapping clock phases are represented by ϕ_1 and ϕ_2. $C_{S1,21,22}$ and $C_{F1,2}$ are the sampling and integrating/feedback capacitors respectively. The comparator and the D-latch form the dynamic latch comparator. The 1-bit DAC in feedback,

switches between V_{REFP} and V_{REFN} when output, v in the figure, of the overall modulator is *high* and *low*, respectively.

High level synthesis is a mandatory phase in the hierarchical top-down design methodology for mixed signal systems. Apart from serving as a preliminary tool aiding the understanding of the global mechanism of the system for a novice, it also acts as a testbench facilitating the validation of concepts for a designer. It provides a realistic estimation of any complex systems performance with a comparatively shorter simulation time. A precise behavioral model aids the designer to take early decisions regarding the choice of the optimal topology and the combination of design parameters, hence sparing the designer of the expensive and frustrating design re-iterations at the implementation stage.

Quantization (a non-linear process) makes the $\Sigma\Delta$ modulator technique a non-linear one. In order to achieve the desired system performance, a large set of parameters, viz. architecture, order (L), resolution of the internal quantizer (B), oversampling ratio (OSR) and scaling coefficients, need to be optimized. Apropos its non-linearity, the optimization process turns out to be difficult and time taking. Hence the optimization has to be carried out with behavioral simulations. Besides, behavioral simulations also come handy when it is required to do a qualitative as well as quantitative analysis of the effect of circuit imperfections on the performance of the modulator. So, detailed models of the modulator's building blocks, incorporating various nonidealities, can be developed using SIMULINK. Time domain simulations using this user friendly simulator can present a very realistic estimate of the degradation in the modulator's SNR due to various error sources. The degradation of the system's performance due to different circuit nonidealities is inevitable. Hence a good designer ought to indulge in scrupulous book-keeping of the predominant sources of circuit level nonidealities and the deterioration in the overall system due to each. The final achieved performance of the system including the cumulative degradation due to all the nonidealities should be higher than the minimum desired performance level.

Initially, the first and second order modulator is modeled using Verilog-A and verified using Cadence Virtuoso to understand the working principle. The codes are included in Appendix C. Next, before starting the circuit implementation of the $\Sigma\Delta$ ADC, a series of MATLAB based GUIs are developed to aid the same and extract the required design parameters to obtain the target performance. A brief note on the top level working principle of the $\Sigma\Delta$ is given in Appendix D. A concise introduction to each of the GUIs is also included in Appendix D. The circuit implementation of the $\Sigma\Delta$ ADC and its constituent blocks is discussed in the following subsection. All the necessary

circuit/component values are derived using the GUIs.

3.3.1 Circuit Implementation of the ΣΔ ADC

For conventional modulators, like that shown in Fig. 3.16, each of the opamps is idle in at least one of the clock phases. Taking clue from this fact, an opamp-shared topology is implemented here.

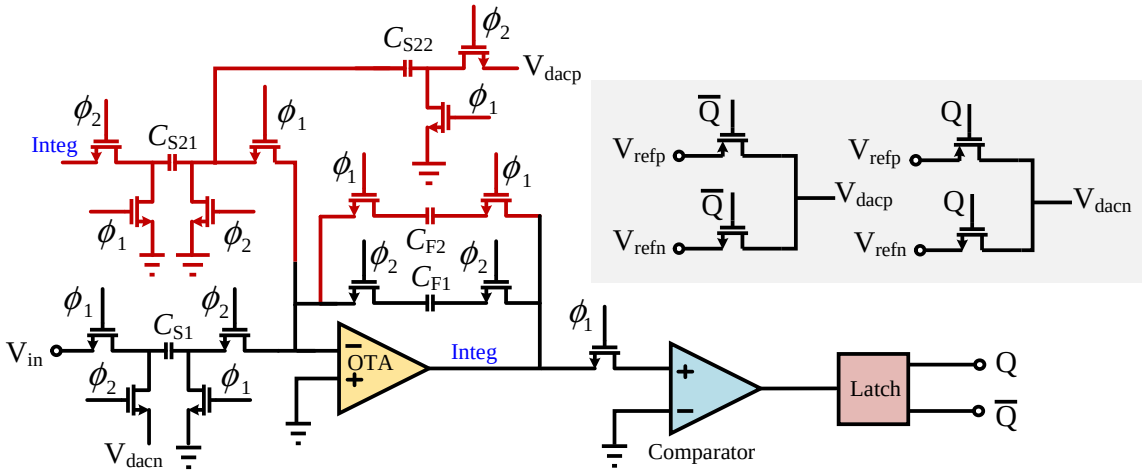


Figure 3.17: Single ended representation of the opamp-shared second order ΣΔ ADC. Here C_{S1} = 1.3428pF, C_{S21} = 2.136pF, C_{S22} = 0.79pF, C_{F1} = 8.132pF, C_{F1} = 4.066pF, $V_{refp} = V_{dacp}$ = 1.1 V and $V_{refn} = V_{dacn}$ = 1.1 V.

The single ended representation of the opamp-shared ΣΔ modulator employing a single opamp is shown in Fig. 3.17. Using a switch configuration such that the opamp is active in both the clock phases, this opamp-shared topology provides second order noise-shaping. A reference voltage of 400 mVp-p is chosen here, considering that the maximum swing of the PGA's output to be 200 mVp-p in order to achieve optimum performance. The capacitor ratios are derived from the GUI in [152], to ensure that each capacitor can be implemented as multiple instances of a fixed unit capacitors. This ascertains that the capacitor ratios (i.e. poles of the loop transfer function, or, zeros of the noise transfer function) remain unchanged despite component mismatches. The estimation of the total thermal noise in the modulator is carried out before deciding the design and component specification [153]. The choice of high resolution (10 bit) is justified as follows (i) accuracy of the classification and feature extraction algorithms processing the output of the ADC are proportional to the resolution of the ADCs. Hence the high effective number of bits (ENOB) achieved here is more medically cohesive to diagnosis, similar to the data available at [154] and (ii) it extends the utility of the scheme for the digitization of a wide range of ExG signals [155].

Moreover, the scheme shown in Fig. 3.17 also facilitates seamless resolution reconfigurability with minimal hardware and almost zero power overhead [156]. The circuit renders first order noise-shaping when only components in black color are activated, and second order noise-shaping when the components in dark red are also activated. It is advantageous in the following manners (i) this facilitates the digital circuit (following the ΣΔ ADC) to reduce its power consumption by opting to process low resolution data. The proposed ΣΔ ADC implementation aids cost-efficient (w.r.t area and power) switching between the two modes vis-à-vis other ADC architectures e.g. SAR ADC, pipeline ADC, etc. (ii) facilitates reconfigurability between low and high resolution for preliminary and final diagnostics, respectively. Since the noise power at ADC's input is inversely proportional to the AFE's gain, this scheme provides a choice between low and high resolution for high and low gain, respectively.

The design of the major constituent blocks of the modulator is discussed below.

OTA Design

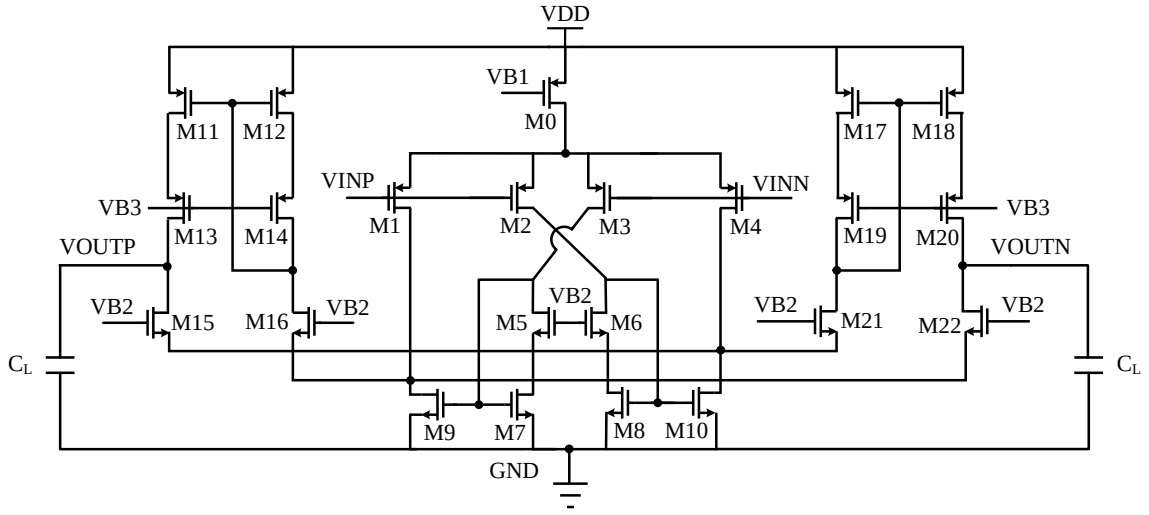


Figure 3.18: Circuit digram of the ERFC OTA used in the implementation of the ΣΔ modulator.

The enhanced recyclic folded cascode (ERFC) OTA topology is used to implement the required integrator [130, 157]. The ERFC OTA has twice the bandwidth of a conventional folded cascode OTA for the same power and area. Moreover, this topology is also benefits from the inherent common mode feedback. The circuit diagram of the OTA is given in Fig. 3.18. As earlier, the g_m/I_D methodology is utilized for biasing and sizing the OTA. Apart from a high open loop DC gain of this OTA, it is ensured that its UGB is approximately ten times of the sampling frequency

of the modulator. The device dimensions and bias voltages of the OTA are tabulated in Table 3.4.

Table 3.4: Device sizes and bias voltages of the ERFC OTA.

Device	**W/L (μm)**	**Device**	**W/L (μm)**	**Device**	**W/L (μm)**
M0	9.72/3.6	M7,8	1/9	M13,14,19,20	1.39/5.4
M1,2,3,4	1.88/3.6	M9	1.05/9	M15,16,21,22	1/9.5
M5,6	1.24/7.2	M11,12,17,18	1.27/27	–	–
Bias Voltages					
VB1	1.2 V	VB2	0.9 V	VB3	0.7 V

Switches

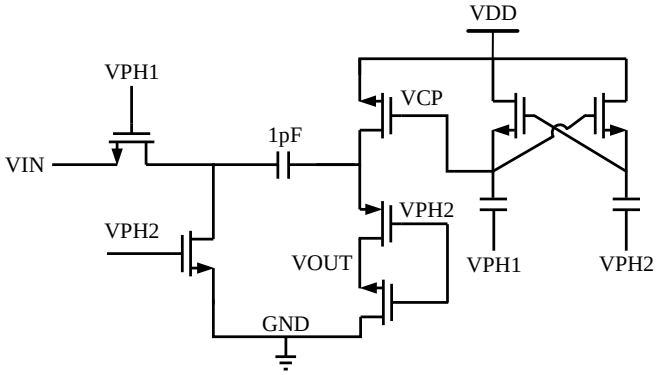


Figure 3.19: Schematic diagram of the bootstrap switch. Minimum device dimension (W/L = 0.24/0.18) is used for all the transistors. VPH1 and VPH2 are two non-overlapping clock pulses.

The switches operating directly on the input signal are implemented as bootstraped switches to minimize their nonlinear behavior emanating from the signal-dependent resistance. For input signals with large amplitudes, this would introduce large distortions and hence degrade the ADC's signal-to-noise-and-distortion ratio (SNDR) [158]. The circuit digram of the bootstraped switch used here is given in Fig 3.19. The utility of the bootstrap switch is verified through simulations using an input sinewave. For an input amplitude of 200 mV, a normal NMOS switch exhibits a total harmonic distortion (THD) of 2.064 mV whereas a bootstrap exhibits a THD of 21.52 μV only.

The other switches are implemented using normal pass transistors. The sizing of the transistors are optimized keeping in mind its load capacitance and the signal swing it has to handle.

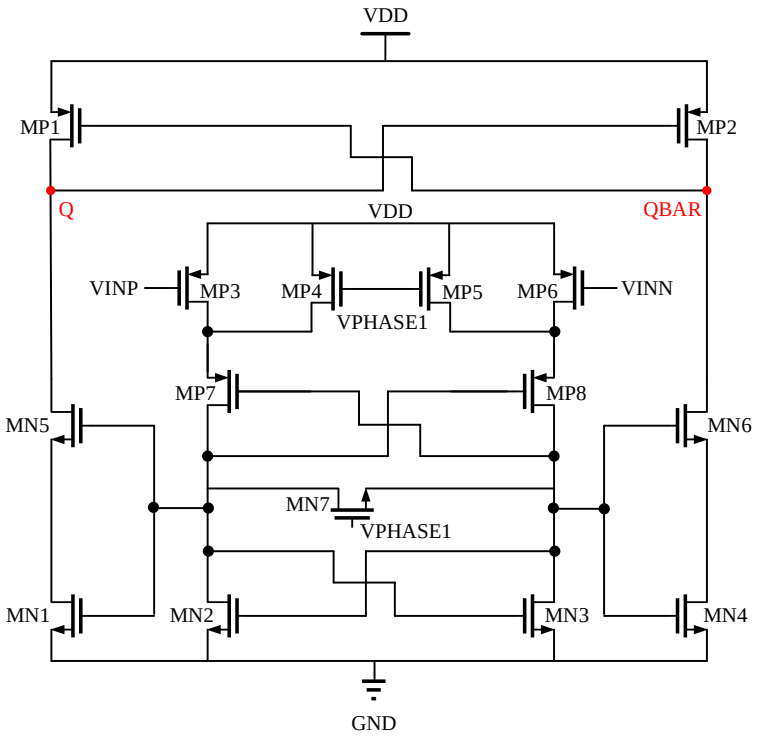


Figure 3.20: Circuit diagram of the regenerative latch comparator used for the implementation of the ΣΔ ADC.

Comparator

Fig. 3.20 shows the circuit diagram of the dynamic latch comparator implemented here. The regenerative latch is based in [159, 160]. A preamplifier is avoided here owing to the fact that its input (i.e. the output of the second integrator in Fig. 3.16) has a large amplitude. The device sizes of this comparator is given in Table 3.5.

Table 3.5: Device diamensions of the transistors of the regenerative latch comparator.

Device	**W/L (μm)**	**Device**	**W/L (μm)**
MP1,2	0.4/28	MN4,5,6	0.4/14
MP3,4,5,6,7,8	0.4/14	MN7	0.24/0.18
MN2,3	0.4/7	–	–

3.3.2 Post Layout Results

Layout of the complete circuit of the ΣΔ modulator shown in Fig. 3.17 is completed after verifying the functionality of the modulator in schematic level. The post-layout simulations are run to verify

the performance of the modulator. [161] defines two figure-of-merits, FoM_1 and FoM_2, to compare various implementations of ΣΔ modulators across different process technologies and supply voltages. The expressions for FoM_1 and FoM_2 are given below.

$$FoM_1 = \frac{Power(W)}{2^{ENOB(bit)} * 2 * BW(Hz)} \times 10^{12} \quad pJ/conv. \tag{3.13}$$

$$FoM_2 = 2kT \times \frac{3 * 2^{2*ENOB(bit)} * 2 * BW(Hz)}{Power(W)} \tag{3.14}$$

The post-layout simulations show that the modulator functions as expected. Further, important aspects of the modulator's performance are discussed below.

- The performance parameters of the of the ERFC OTA is tabulated in Table 3.6.

Table 3.6: Post-layout performance parameters of the ERFC OTA

Parameter	Value
Supply voltage	1.8 V
Current consumption	2.483 μA
Open loop DC gain	95.35 dB
UGB for C_L = 2 pF	646.25 KHz
Phase margin for C_L = 2 pF	70°
Output swing for maximum linearity	200 mVp-p

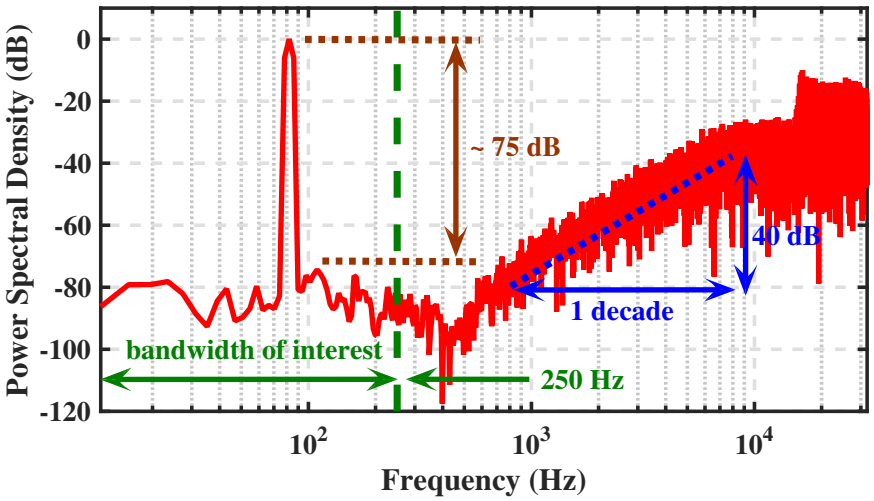


Figure 3.21: Power spectral density of the output of the ΣΔ modulator.

- The power spectral density of the topology shown in Fig. 3.17 is shown Fig. 3.21. It clearly

shows that the implemented modulator exhibits second order noise-shaping and achieves a signal-to-noise-and-distortion ratio (SNDR) of 76 dB approximately. The post-layout performance of the ΣΔ ADC is given in Table 3.7.

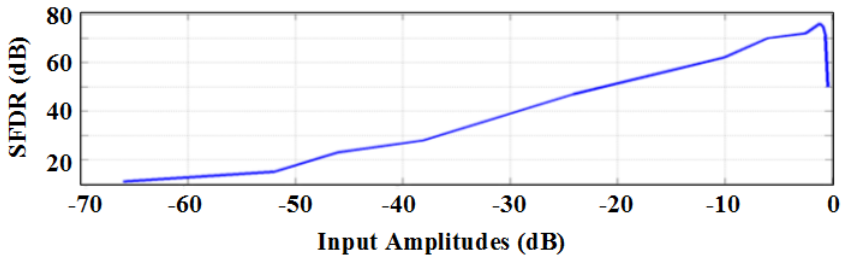


Figure 3.22: Variation of SNDR with different input amplitude for the ΣΔ ADC.

- Fig. 3.22 plots the variation of SNDR with different input amplitude for the implemented ΣΔ ADC. It is found that the modulator offers maximum SNDR for input amplitudes within the range of 0.95-1 V. This implies that the gain of the PGA is required to be adjusted so that its output lies in the same voltage range.

Table 3.7: Post-layout performance parameters of the ΣΔ ADC

Parameter	**Value**
Topology	Opamp-shared
Order	2^{nd}
Bandwidth	250 Hz
Sampling frequency	64 kHz
Power consumption	5.0652 μW
Dynamic range	76 dB
FoM_1	1.9645 pJ/conv.

- The complete system was validated for a scaled ECG signal taken from the PTB database [154]. The digital output of the ΣΔ ADC (stream of 1s and 0s) generated by the Spectre simulator is exported to Simulink (MATLAB), where it is passed through a CIC filter to reconstruct the ECG signal. The quality assessment of the reconstructed signal w.r.t. the input ECG signal is tabulated in Table 3.8 using the figures-of-merit suggested in [162, 163]. As is shown in Fig. 3.23 the reconstructed waveform captures all the essential features of the ECG signal.

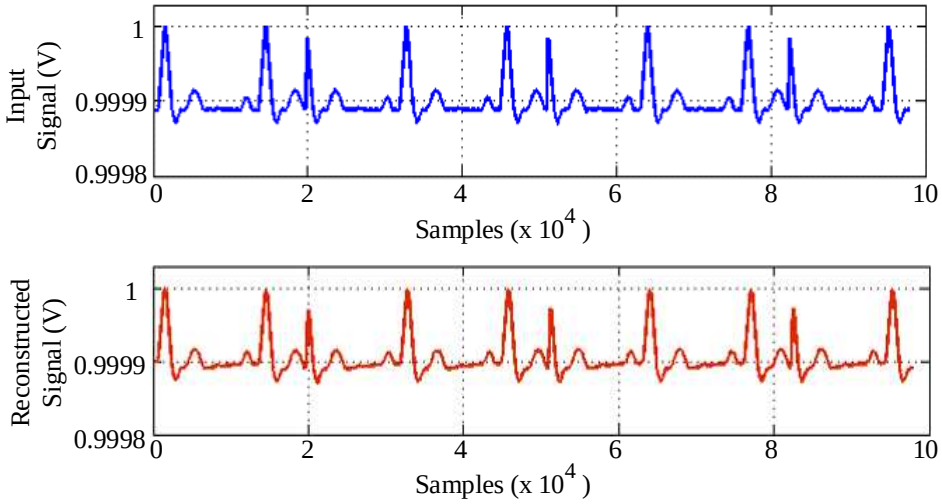


Figure 3.23: The waveforms of the scaled input ECG signal (top) and the output signal reconstructed using CIC filter (bottom).

Table 3.8: Quality assessment of the reconstructed signal

Parameter	**Value**
Percent Root Mean Square Difference (PRD)	86.11
Root Mean Square Error	2.03E-06
Signal-to-Noise-Ratio (SNR in dB)	41.29
Maximum Amplitude Error (MAE)	9.05E-06
R-squared Score	0.99

3.4 Measurement Results

After verifying the amplifier and the ΣΔ ADC through post-layout simulations, the designs are fabricated. The details of the tape-out are discussed here. The measurement results are also provided. Finally, the comparison of the design implemented here with the existing state-of-the-art is also reported.

The pin distribution was planned so as to allow the testing of all the three blocks combined as a system, as well as each of them individually. (Note that the block on the right corresponds to digital implementation of decimation filter and ECG feature extraction and classification, which is not in the scope of this thesis).

3.4.1 Results and Discussion

The measured results and analysis of the same is given here.

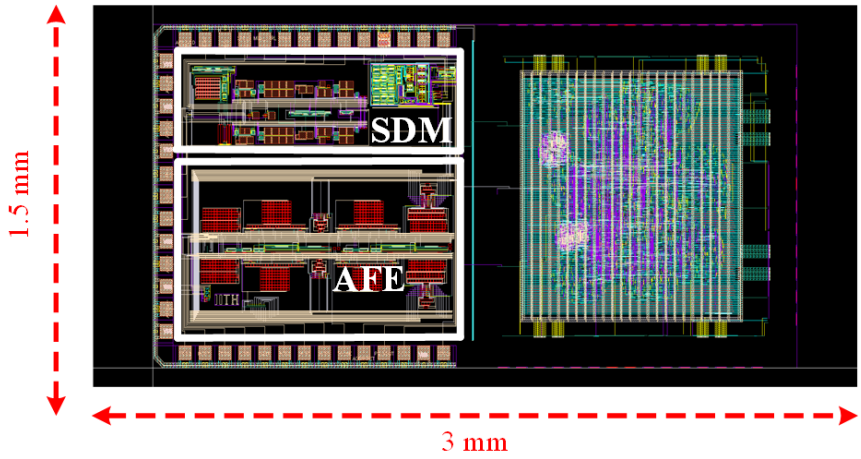


Figure 3.24: Die micrograph of the chip consisting the AFE and the ΣΔ ADC.

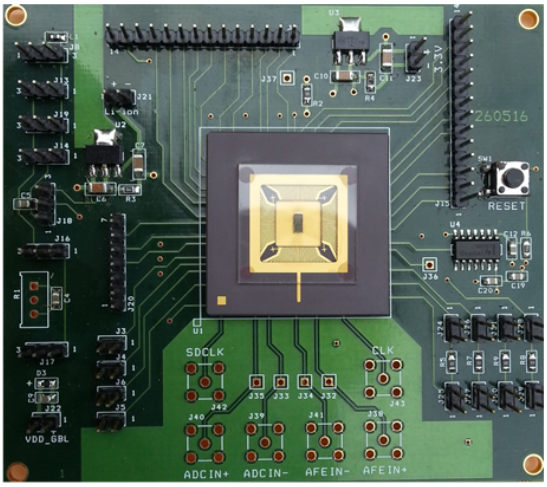


Figure 3.25: The PCB prepared for testing the chip.

Measurement Setup: The following instruments were used for the testing the chip.

(i) Signal Generator (Tektronix AFG 3022) - used to give low frequency sinusoidal (< 100 Hz) and clock (64 kHz) input to the AFE and ΣΔ ADC. Note that this instrument has two shortcomings w.r.t to the testing requirements because

- the minimum amplitude of the sinusoidal input is 25 mVpp, whereas the requirement is 0.1-1 mV.
- the purity of the sinusoidal input is only 35 dB, whereas the requirement is 70 dB approximately.

(ii) DC Voltage Source (Keysight Technologies E3631A) - used to apply the required DC supply voltage.

(iii) Oscilloscope (Keysight Technologies DSO 90404A 4 GHz) - used to view the time-domain waveform of the relevant outputs.
(iv) Spectrum Analyzer (Keysight Technologies E4446A 3 Hz - 44 GHz) - used to obtain the power spectral density of the output of the ΣΔ ADC.
(v) Digital Multimeter (Keysight Technologies 34401A) - used to measure the relevant DC voltages.

- **AFE** : The amplifier failed to perform as desired. Both the differential output nodes couldn't maintain the common mode voltage of 0.9 V. The output nodes showed no swing even when a sine wave was fed to the amplifier. The following can be concluded from the above mentioned results:
  (i) The failure of AFE can be attributed to the offset generated due to layout mismatch. The input offset is suspected to saturate the output of the amplifier.
  (ii) Another fly-in-the-ointment is the sensitivity of the amplifier because it has been designed with very low current consumption. The issue of leakage currents in low power designs is also critical.
  (iii) The bias generation circuit should be included in the design. All the bias voltages were external for this tape-out. Replica bias circuit should be designed to mitigate the variation of bias voltages across process corners.

  The performance of implemented amplifier comprising the IA and the PGA is compared to similar designs in Table 3.9. Since the amplifier in the chip shown in Fig. 6.1 failed to function as desired, the comparison is provided using the post-layout results of the same. Its is evident that implemented design falls behind other designs w.r.t to the NEF performance parameter. At the same time, it gains superiority w.r.t to obtained CMRR (a key parameter in the design of ECG front-ends) and power dissipation. Most importantly, the other implementations either do not include any kind of gain and 3-dB frequency control/tuning, or involve manual control externally using control pins. The different design parameters which are tweaked to achieve the desired gain and frequency control is also mentioned in Table 3.9. In apropos, the proposed scheme in Fig. 2.6 includes an automatic gain and frequency control mechanism.

- **ΣΔ ADC** : The measurement results show that the modulator works fine. The power spectral density plot of the output shown in Fig. 6.4 that the modulator achieves second order noise-shaping and a spurious-free dynamic range (SFDR) of 7 bits approximately. It still satisfies

Table 3.9: Performance comparison of the implemented IA with the similar existing designs

Parameter	**JSSC '07 [62]**	**TBCAS '12 [68]**	**TCAS '15 [70]**	**This work**
Technology (μm)	0.5	0.13	0.35	0.18
V_{supply} (V)	3	1	2.5	1.8
Gain (dB)	58.06-67.95	40	40.3	40-60
f_L (Hz)	EEG - 0.3 ECG - 0.3 EMG - 14	0.4	-	0.05
f_H (Hz)	EEG - 40 ECG-125 EMG-350	8.5 k	250	0.1-10 k
Power (μW)	60	12.5	-	0.47
Noise (μV_{RMS})	0.056-0.057	3.2	2.81	9.6
CMRR (dB)	> 120	> 60	> 82	120
THD @ 50 Hz	@ 5 mVp-p minimum gain 0.45-0.52%	1.5% @ 1 mVp-p	0.1%	1% @ 2 mVp-p
NEF	9.2	4.5	1.88, 1.93, 2.05	16.0443
PEF	253.92	20.25	-	463.3533
Chopper	Yes	No	No	No
AGC	Ext. - cap. switch	Ext. - cap switch	No	Yes
AFC	Ext. - cap switch	No	No	Yes
Architecture	AC coupled chopper IA	Capacitive feedback	Capacitive feedback	Capacitive feedback
Application	EEG EMG ECG	ECG EMG ECG	ECG, EMG	ECG

the required dynamic range of 3.33 bits ($= 20 * log_{10}(\frac{1mV}{0.1mV})$) considered while designing the amplifier. As discussed in previous section, the post-layout extracted simulations of the same exhibit a SFDR of 10 bits. This reduction in the obtained SFDR can be attributed to the following

- The affect of the mismatches on the design while using fixed external bias voltages.
- Unavailability of the necessary test equipment, e.g. in the absence of low-amplitude low-frequency generator with at least 70 dB linearity (a little more than the SFDR of the implemented ADC) the input to the ADC was given by generating the required differential voltages using MATLAB and applying to the input pads using 3.5 mm earphone jack. The noise introduced by the long wires and the breadboard involved are the most likely sources for degradation of the performance.

Similarly,the comparison of the $\Sigma\Delta$ ADC implemented here with other existing similar designs is presented in Table 6.1. The post-layout performance of the implemented modulator fares at par

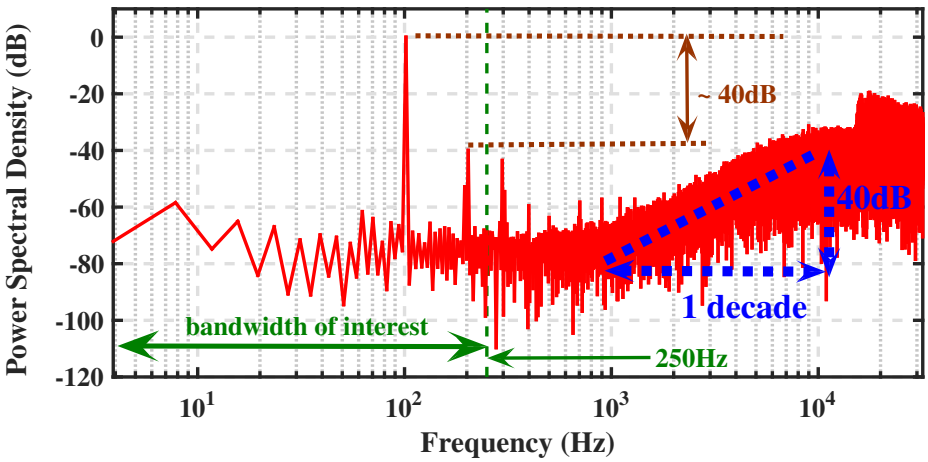


Figure 3.26: Power spectral density of the fabricated ΣΔ ADC.

or better than the other implementations mentioned in Table 6.1 w.r.t the performance parameter FoM_1 defined in equation 3.13. The performance of the fabricated modulator fall behind the other designs drastically.

Table 3.10: Performance comparison of the implemented ΣΔ ADC with similar designs

Parameter	**Value**				
	JETCAS '12 [81]	TIM '16 [113]	SPCAC '09 [96]	ICECS '05 [97]	**This work**
Technology (μm)	0.18	0.065	0.035	0.18	0.18
Voltage Supply (V)	1	1	1	3.3	1.8
Order	3^{rd}	3^{rd}	2^{nd}	2^{nd}	2^{nd}
Bandwidth (Hz)	500	10 k	781.25	10 k	250
Sampling Frequency (kHz)	32 k	1.28 M	100 k	5120	64
Power Consumption (μW)	17.6	24.8	80	1630	5.0652
Dynamic Range (dB)	55.8	80.4	62	99	76 (post-ext) 40(measured)
FOM1 (pJ/Conv.)	34.9	0.1449	1.11	49.7702	1.9645 (post-ext) 124 (measured)

3.5 Summary

The design of a variable gain amplifier and ΣΔ modulator ADC are discussed in this chapter. The step-wise design procedure and essential intricacies is also provided. Both, post-layout and measured results obtained are given. The post-layout simulation results exhibit desired performance of both

the circuits. But, a circuit which can sense the strength of the input ECG signal and decide the combination of the switches - S0, S1 and S2 (shown in Fig. 3.1) - resulting in appropriate amplification of the input signal is required. Further, the low pass 3-dB cut-off frequency is prone to deviations due to fabrication process related mismatches. Hence a calibration circuit is required which ensures minimum deviation of the cut-off frequency despite component mismatches.

These requirements lead us to two important contributions of this thesis. For addressing these issues, an efficient gain control mechanism and an automatic frequency tuning technique are introduced in the next chapter.

Chapter 4

Automatic Gain Control and Automatic Frequency Tuning

4.1 Introduction

The need to introduce AGC and AFT to ECG recording system, shown in Fig. 4.1, is already brought out in Chapter 2. It is well known that the strength of the ECG signal depends on the location of the electrodes and varies from patient to patient. Moreover, as is shown in Fig. 3.22, the $\Sigma\Delta$ ADC achieves maximum SNR for a certain range of input amplitudes. Therefore, it is essential that the input of the PGA is amplified to a level which corresponds to level yielding maximum SNR. In addition to that, the gain of the amplifier, being determined by the capacitor ratios, may deviate from its nominal value due to component related mismatches. This brings out the need of an automatic gain control (AGC) circuit which can ensure that the output of the PGA in Fig. 3.1 reaches the desired level. A simple AGC circuit is proposed in this chapter.

Similarly, equation A.6 the lowpass 3-dB cut-off frequency of the amplifier Fig. 3.1 being determined by the process dependent parameters, *viz.* transconductance of the OTA and load capacitance. Both these parameters are vulnerable to component mismatches, resulting in deviation of the cut-off frequency from its desired value of 250 Hz. Since the PGA is followed by an ADC, its output need to be strictly band limited to 250 Hz to prevent aliasing. Moreover, a cut-off lesser than 250 Hz would lead to missing essential features of the ECG signal. This necessitates the use of an automatic frequency tuning (AFT) scheme to minimize the deviation of the cut-off frequency from its nominal

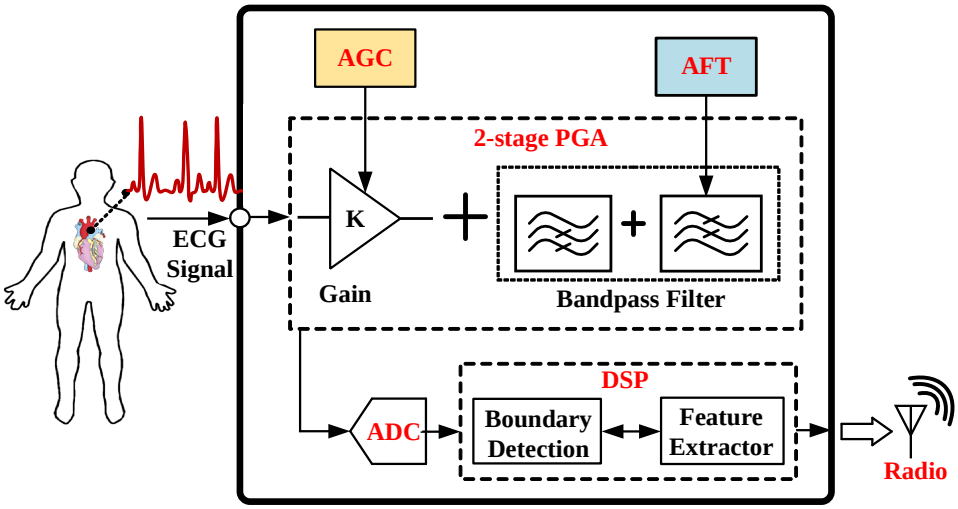


Figure 4.1: A conventional ECG front-end with the proposed AGC and AFT pointed out with colored boxes.

value of 250 Hz. A novel AFT scheme which implements the same functionality is proposed in this chapter .

4.2 Automatic Gain Control

The basic tasks of the AGC circuit are the following (i) sense the output of the PGA, (ii) compare the output with a threshold voltage, (iii) depending on the comparison results, select a combination of switches - S0, S1 and S2 - in Fig. 3.1 which makes the final output of the PGA greater than the threshold voltage. Similar gain control mechanisms are reported in [164, 165]. Scheme introduced in [164] controls the gain of the variable gain amplifier by changing its bias current and uses a peak detector with sample-hold technique. [165] controls the gain of the amplifier by changing the resistance which determines its gain.

An automatic gain control mechanism which is capable of handling all these responsibilities is proposed here and is shown in Fig. 4.2. It consists of a peak detector, voltage sense circuit and a digital circuit generating three control signals - S0, S1 and S2. The digital circuit is implemented as a finite state machine (FSM). The working of the mechanism can be understood as follows :

- **Peak Detector** : The peak detector is a negative feedback system which is responsible for capturing the voltage corresponding to the positive peak value, V_{peak}, of the swing of the input signal V_{in}. The peak detector circuit consists of an amplifier with high open loop DC gain, a current source (M1), current steering transistors (comprising of M2 and M3) and a load

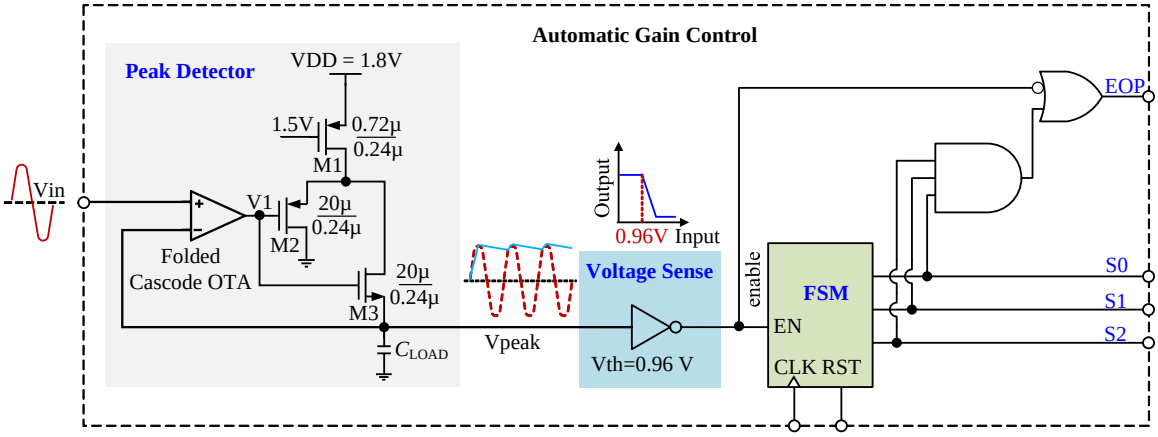


Figure 4.2: Schematic diagram of the proposed gain control mechanism. (C_{LOAD} = 30 pF).

capacitance (C_{LOAD}). When voltage across C_{LOAD} is lesser than the input V_{in}, the amplifier generates a large output V1, such that the current from M1 is steered to the C_{LOAD} via M3. The capacitor continues to get charged till the voltage across it becomes just greater than V_{in}. Then the amplifier outputs a low voltage so that the current from M1 is steered to ground via M2, while the capacitor C_{LOAD} holds the voltage across it. The amplifier (implemented as folded cascode OTA) is responsible for producing a voltage V1, such that the voltage across the load capacitor always tracks the input V_{in}. Also, the peak detector is designed such that its total discharge time is higher than the time duration between two R-peaks. Hence, here the discharge time is kept greater than 1 second to prevent the digital control logic from varying the gain during low amplitude peaks (P,Q,T) of the ECG signal.

- **Voltage Sense** : The voltage sense circuit is responsible for comparing V_{peak} with a threshold voltage (0.96 V here). The signal labeled *enable* transits from a logical *high* (1.8 V here) to a logical *low* (0 V here) when V_{peak} is greater than 0.96 V.

- **FSM** : The FSM operates only when the *enable* signal is *high*. Note that while S0, S1 and S2 are the gain control signals, *EOP* (or end of process) signal marks the end of operation of FSM. The working principle of the FSM is summarized in the form of an algorithm given below.

The gain offered by the PGA for each combination of the control signals S0, S1, and S2 is tabulated in Table 4.1.

Algorithm 1 Search for a suitable combination of the triad (S0, S1, S2) until *enable* goes *low*

Input: CLK, RST, EN
Output: EOP, $Y < 2 : 0 >$
  for each positive edge of CLK **do**
    if RST is $high$ **then**
      $Y \leftarrow 000$
      $EOP \leftarrow low$
    else
      if (EN is $high$) and ($Y \neq 111$) **then**
        $Y \leftarrow Y + 1$
      else
        $Y \leftarrow Y$
        $EOP \leftarrow \{(EN = 0)\ or\ (Y = 111)\}$
      end if
    end if
  end for
Output: $S0 \leftarrow Y < 0 >$; $S1 \leftarrow Y < 1 >$; $S2 \leftarrow Y < 2 >$

Table 4.1: Combination of the control signals S0, S1, and S2 and the corresponding gain provided by the PGA

SW	**S2**	**S1**	**S0**	**PGA Gain**
Weight	4	3	2	
RST	0	0	0	1
	0	0	1	3
	0	1	0	4
	0	1	1	6
	1	0	0	5
	1	0	1	7
	1	1	0	8
	1	1	1	10

4.2.1 Circuit Implementation

The circuit implementation of each of the major blocks comprising the AGC is discussed here. Circuit diagrams and important design considerations are also given here.

Peak Detector

The folded cascode OTA is the heart of the peak detector shown in Fig. 4.2. Evaluating the noise contribution of each of the constituent transistors, the g_m/I_D [131] technique is utilized for sizing the transistors to optimize power consumption and noise. Moreover, the input transistors are operated in moderate inversion to reduce flicker noise. The circuit diagram of the OTA is shown in Fig. 4.3 and the device dimensions are given in Table 4.2.

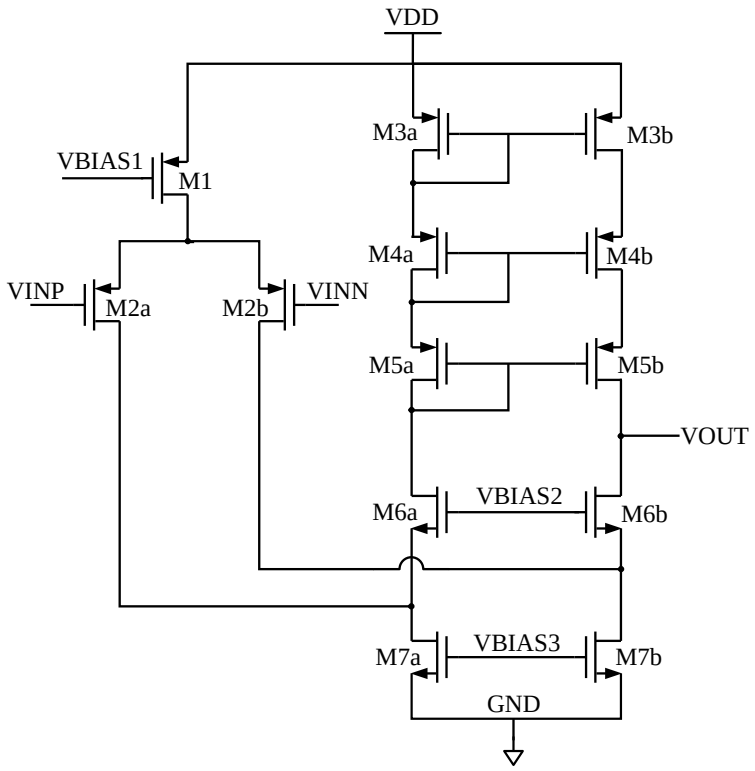


Figure 4.3: Circuit diagram of the folded cascode OTA used in the peak detector.

Table 4.2: Device dimensions and bias voltages of the folded cascode OTA

Device	**W/L (μm)**	**Device**	**W/L (μm)**	**Device**	**W/L (μm)**
M1	12.54/1	M2a,M2b	48.44/0.180	M3a,M3b	12.80/1
M4a,M4b	71.94/0.5	M5a,M5b	69.3/0.18	M6a,M5b	3u/10
M7a,M7b	1.280/10.17	–	–	–	–
Bias Voltages					
VBIAS1	1.5 V	VBIAS2	0.6 V	VBIAS3	0.3 V

Voltage Sense

The voltage sense is implemented using three inverters in cascade. Sizing of individual transistors are done such that their output transits from high to low at 0.96 V. Three inverters are cascaded to reduce the rise-time and fall-time of the final output. The schematic diagram of this sense circuit is given in Fig. 4.4. Its output $VOUT$ transits from high to low if the input VIN is greater than 0.96 V.

Digital State Machine

The FSM is designed using basic gates. It is implemented using bottom-up approach. The complete state machine is divided into smaller modules. First the universal gates are implemented, followed

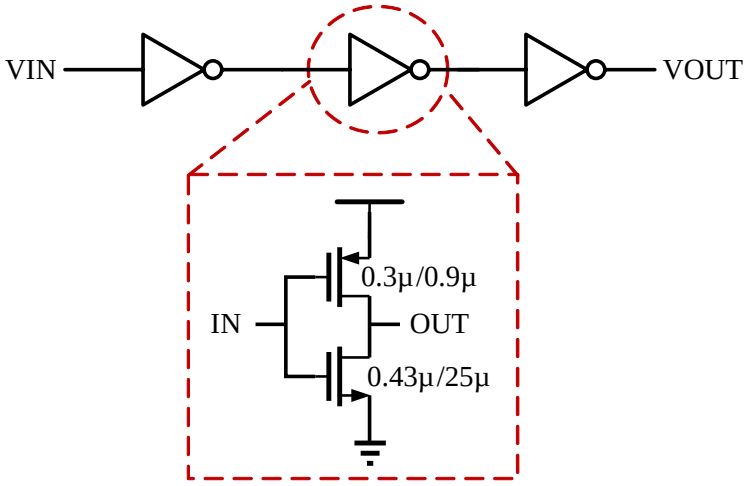


Figure 4.4: Schematic diagram of the proposed voltage sense circuit.

by bigger circuits like multiplexers, adders, etc. They are used to build each individual module, and then put together to complete the state machine design.

4.2.2 Results

Post-layout simulations of each of the modules discussed above are carried out to verify their functionality. Then the modules are connected together with the amplifer shown in Fig. 3.1 and verified. The results hence obtained turn out to be as desired.

- The performance parameters of the OTA of the peak detector is tabulated in Table 4.3.

Table 4.3: Post-layout performance parameters of the folded cascode OTA

Parameter	**Value**
Supply voltage	1.8 V
Current consumption	14.42 nA
Open loop DC gain	88 dB
UGB for $C_L = 1$ pF	25.5 KHz
Phase margin for $C_L = 1$ pF	73°

- Fig. 4.5 shows the output of the amplifier (shown in Fig. 3.1) working in tandem with the AGC circuit. The figure shows the input (top and bottom left) and output (top and bottom right) wavefroms of the AFE for an input signal strength of 0.1 mV and 1 mV, respectively. Note that the output of the peak detector is shown in brown color. It is apparent that the AGC fulfills its responsibility of fixing the gain of the amplifier such that the amplifier's output

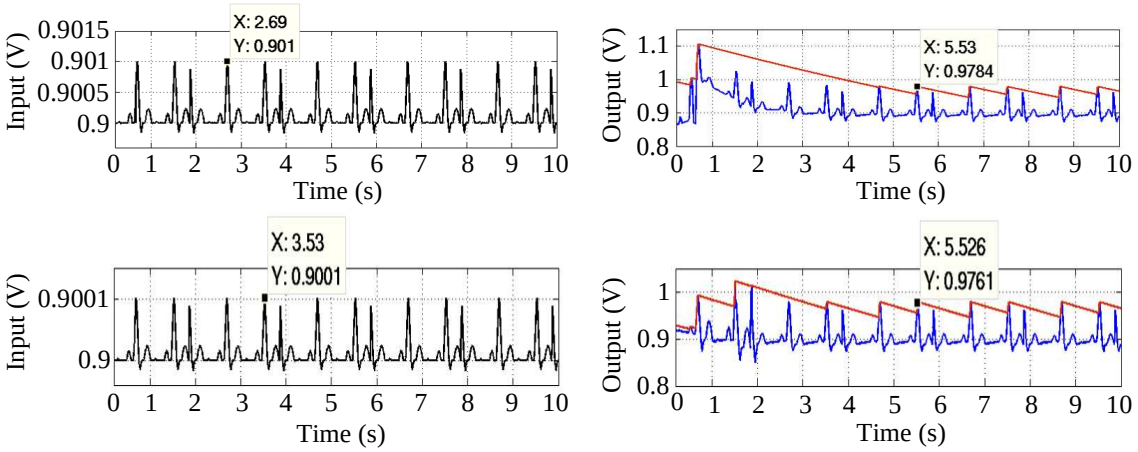


Figure 4.5: Output waveforms of the AFE whose gain is controlled by the AGC for different input amplitudes.

amplitude is greater than 0.96 V, and hence in the optimum input range of the ΣΔ ADC as discussed in the previous chapter.

4.3 Automatic Frequency Tuning

Amplification and filtering are the two prime functions of a standard analog front-end for continuous remote ECG monitoring systems, such as the one shown in Fig. 4.1 [156]. The amplifier employed in such a system and its transfer characteristics are shown in Fig. 2.4. The highpass and lowpass cut-off frequency is defined in equation A.6. It is evident that the 3-dB filter frequency depends on the ratio of the tranconductance of the OTA to the load capacitance (g_m/C_L). The operating parameters of a MOS, e.g. g_m, drift significantly across process corners, resulting in a corresponding cumulative variation in the transconductance of the OTA [166]. Moreover the integrated capacitor exhibits a variation up to 20% considering process variations [167]. These facts along with the effect of parasitics force the cut-off frequency to be highly sensitive to fabrication tolerances, and deviate from its desired nominal value. Since the output of a front-end like the one shown in Fig. 4.1 is fed to an analog-to-digital converter (ADC), a precise lowpass cut-off frequency is required. This in turn necessitates the use of an on-chip automatic frequency tuning circuit to curtail the drift of the cut-off frequency to tolerable limits.

Most of the existing AFT techniques use the Master-Slave topology wherein a replica (master) of the circuit whose corner frequency is to be calibrated is engaged to generate the necessary error correction signal. Then the correction is applied to the main circuit (slave). This methodology

relies on the assumption that the replica circuit placed on the same chip would exhibit the same deviations across process variations as the main circuit. The need of extra circuit is the major drawback of such techniques. A frequency tuning technique involving a reference current generation using an error amplifier, a current mirror, a programmable switched capacitor array and a digital implementation of AFT algorithm is used in [168, 169]. The AFT algorithm selects appropriate number of capacitors from the capacitor array so as to match the time constant corresponding to the reference current charging the net capacitance to a reference time constant. But this topology needs two external absolute references, viz. a bandgap voltage and crystal frequency. Another tuning circuit in [170] involves feeding a reference signal to transconductance stage connected in a lossless integrator mode. Then, both the original signal and the integrator's output is applied to two squarer circuits individually. Finally a comparator compares the DC value of the outputs from the two squarer circuits and generates an error signal which tunes the g_m until they become equal.

Apart from those mentioned above, there are several peak detector based techniques. [171–173] utilize a scheme wherein a unit transconductance block is configured as an integrator whose unity-gain frequency is designed to be equal to the cut-off frequency of the desired filter. A reference sinusoidal signal of frequency equal to the target cut-off frequency is applied to this integrator. Then the output of the integrator and the original signal is fed to a comparator, which generates a g_m correction signal, so as to obtain the desired filter cut-off frequency. Another technique using envelope detector, peak detector, comparator, digital control logic and reference sinusoidal and ramp signal is discussed in [174]. It tunes the pole frequency of a unit biquad by detecting the peak of its amplitude response. Implementations of automatic tuning mechanism involving phase-frequency detector (PFD), charge pump, on-chip lowpass filter and voltage controlled oscillator (VCO) also exist [175].

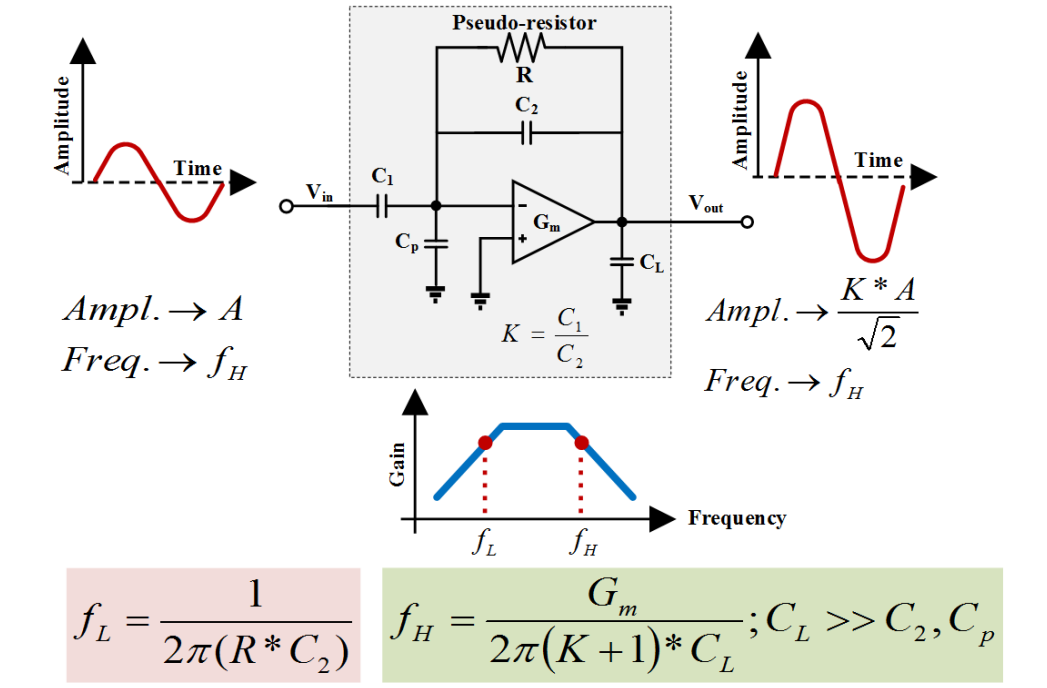
But all the techniques mentioned above suffer from at least one of the following (i) complex mechanism and its associated hefty hardware (VCO, PFD, charge pump, etc.) and power dissipation overhead (ii) auxiliary hardware involved (for Master-Slave topology) (iii) complex switching mechanism or multi-phase operation (iv) extra or multiple off-chip references (e.g. clock, bandgap voltage, ramp voltage, etc.). Therefore, a simplistic lowpass cut-off frequency tuning mechanism based on the magnitude response of the PGA is proposed in this work. It consists of a current-starved ring oscillator based reference signal generator, a digital frequency calibration mechanism, a digitally controlled switched capacitor array and a capacitor selection logic. The proposed technique is an improvement over the aforementioned ones in following terms (i) it employs a simple ultra

low power peak detector circuit and does not involve any hardware which is difficult to design or is power hungry, hence more apt for portable battery-operated remote ECG monitoring devices (ii) it does not need a copy of the main PGA circuit since it is not a Master-Slave topology (iii) involves simple switching (iv) requires a single reference i.e. clock signal, and (v) all components are on-chip and technique is fully automatic.

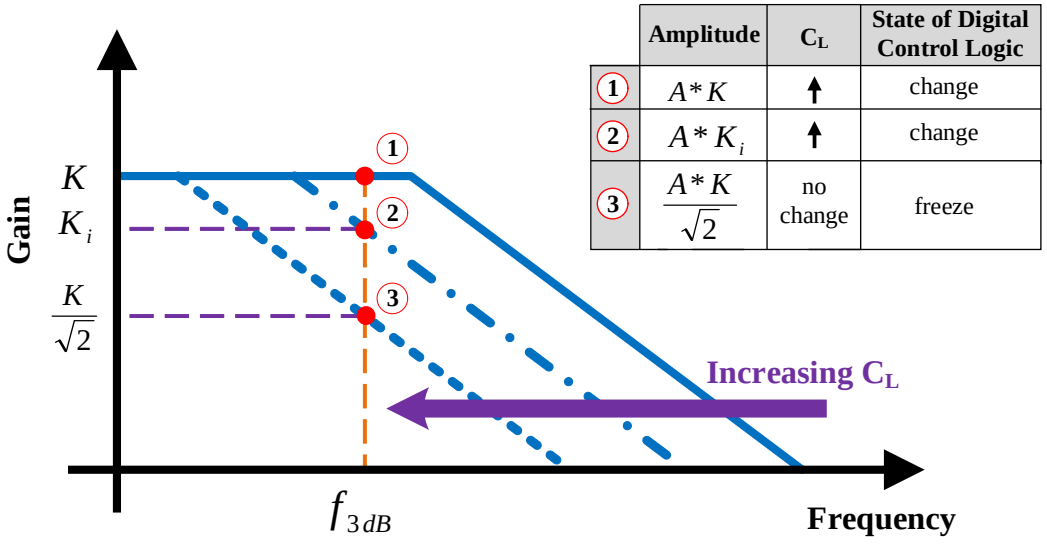
4.3.1 Operating Principle & Architecture

The operating principle of the proposed AFT technique is illustrated in Fig. 4.6. Fig. 4.6(a) shows the conventional capacitive feedback amplifier (CFA) employed for the amplification of the ECG signal. It is assumed that the AGC has finished its job of fixing the required gain of the programmable gain CFA before the procedure for AFT starts. The bandpass characteristics along with the definition of the associated highpass and lowpass cut-off frequencies, i.e. f_L and f_H respectively, is also shown. Approximate expressions for f_L and f_H are also included in the same figure. For this work, the desired f_H is equal to 250 Hz (bandwidth for ECG signals). Tuning the f_H across all process corners boils down to the choice of an appropriate value of C_L. The operation of the proposed scheme is based on the prior knowledge that if a sine-like signal (not necessarily a pure sinusoidal wave) with amplitude equal to A, is applied to the CFA, the output has an amplitude of $\frac{K*A}{\sqrt{2}}$, provided it is ensured that the frequency of the input signal is equal to f_H. The lowpass magnitude response of the CFA is shown in Fig. 4.6(b). It can be observed that the break frequency of the magnitude response shifts towards DC as the C_L is increased. In other words, our aim is to input a signal of frequency f_H faithfully and increase C_L in quantized steps. The value of net C_L for which the amplitude of the output of the CFA is reduced to $\frac{K}{\sqrt{2}}$ times the input amplitude is the desired one for any given process corner.

Implementing the above scheme would pose the following challenges (i) generating a test signal of f_H accurately across all process corners (ii) capturing the output amplitude of CFA corresponding to a gain of K, and (iii) while increasing C_L in steps, detecting the instance for which the CFA's output amplitude would go just below $\frac{K}{\sqrt{2}}$ times the input. The methodology to meet these challenges is illustrated in Fig. 4.7. The first challenge is tackled by employing an ultra low power ring oscillator based frequency generator assisted by a digital frequency calibration circuit. The output of the frequency generator is passed a three-inverter buffer and a low pass filter. The buffer's output is fed to the frequency calibration circuit, which extracts the information about the frequency of the input and generates the necessary control signal to ensure that the frequency of the generator is



(a)



	Amplitude	C_L	State of Digital Control Logic
1	$A*K$	↑	change
2	$A*K_i$	↑	change
3	$\frac{A*K}{\sqrt{2}}$	no change	freeze

(b)

Figure 4.6: Operating principle of the proposed technique to fix the appropriate C_L to ensure a lowpass cut-off frequency of f_H. (a) Block diagram of the CFA used for bio-potential signals along with the associated bandpass frequency charcteristics, (b) Variation of the amplitude of a signal of frequency f_{3dB} (f_H here) with increasing C_L (diagram not to scale).

nearly close to f_H across all process corners. The low pass filter converts the pulse output to a sine-like wave and is fed to the programmable gain CFA. The solution to the second challenge can be derived from Fig. 4.6(b) and is explained in the following steps. Let $C_{L,nom}$ be the nominal load

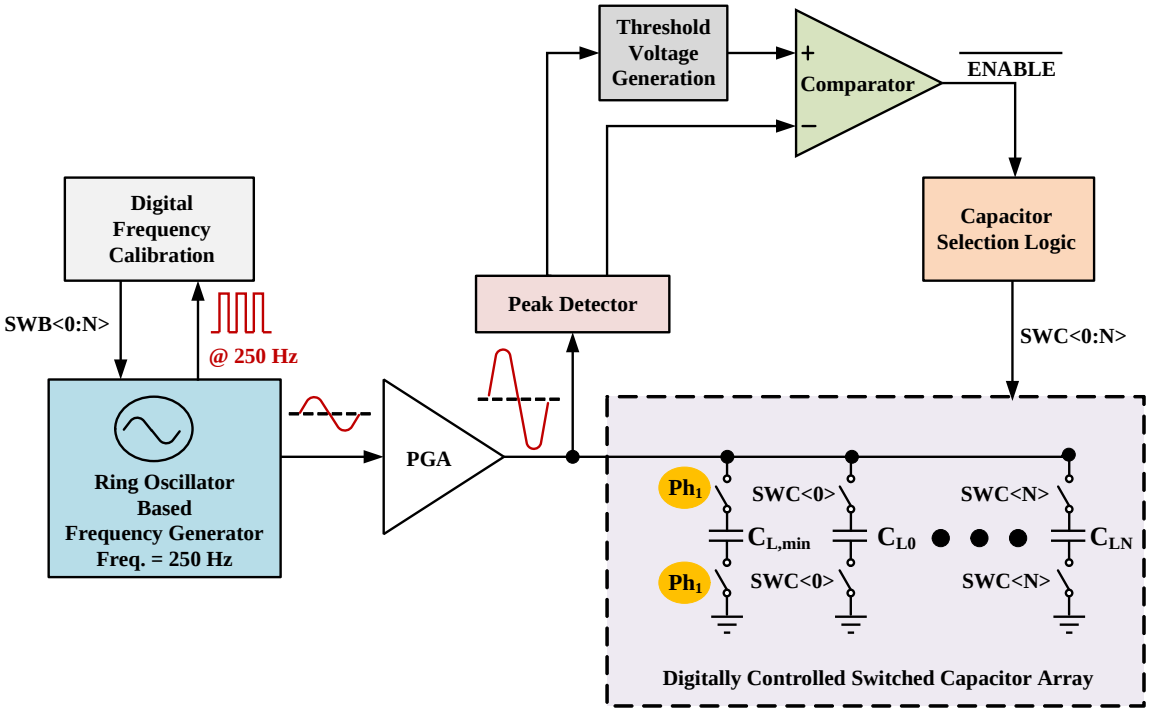


Figure 4.7: Top level block diagram of the AFT. Colored blocks pertain to AFT.

capacitance required to set f_H to 250 Hz. To start with, the load capacitance is set to $C_{L,min}$ ($\ll C_{L,nom}$), so that the break point frequency is very large compared to f_H. This is labeled as '①' in Fig. 4.6(b). With $C_{L,min}$, the output signal of the CFA at f_H has an amplitude is $(K * A)$ times the input amplitude A. This information extracted using a peak detector and is fed to threshold voltage generation. The threshold voltage generator first generates a voltage $\frac{1}{\sqrt{2}}$ times the peak voltage captured with $C_{L,min}$ as the load capacitor, and then holds the same for rest of the operation. This voltage is used as a reference or threshold by the subsequent comparator. As can be seen in Fig. 4.6(b), the amplitude of the CFA's output goes on decreasing for each step, e.g. for the case labeled '②' in Fig. 4.6(b) the CFA's output has an amplitude equal to $(K_i * A)$ where K_i $(< K)$ is the intermediate gain for a signal at f_H. Finally, the load capacitor to the CFA is increased in steps until the CFA's output amplitude becomes just greater than the reference voltage from the threshold voltage generator. This case is labeled as '③' in Fig. 4.6(b). This comparison is done by a comparator, hence solving the third challenge mentioned above.

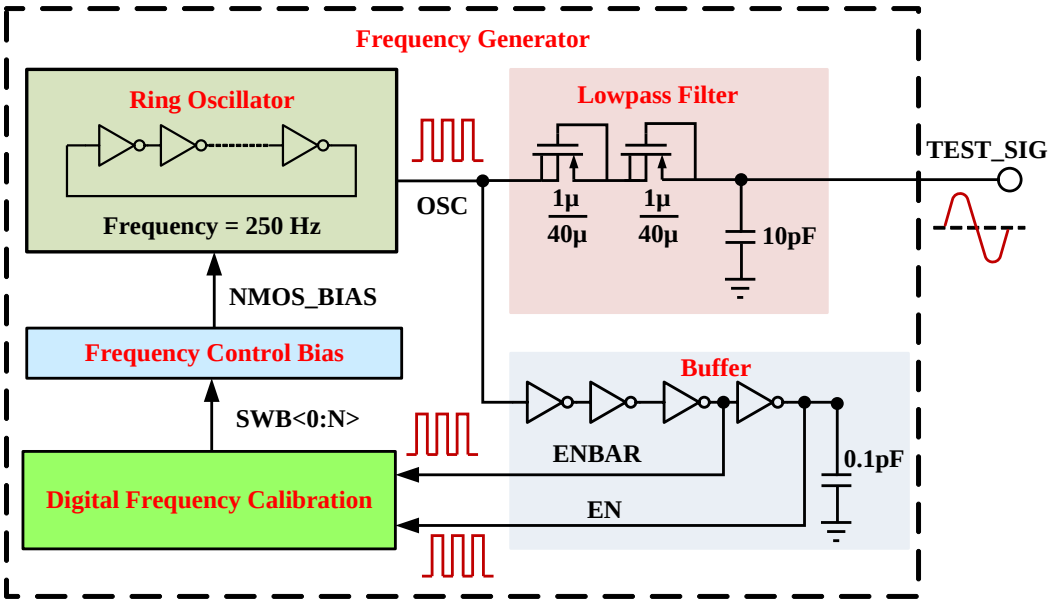


Figure 4.8: Major blocks of the frequency generator.

4.3.2 Circuit Design

Ultra Low Power Frequency Generator

The frequency generator comprises of an ultra low power ring oscillator, a lowpass filter, buffer, digital frequency calibration and bias voltage generator circuit as shown in Fig. 4.8. The ring oscillator is based on current-starved inverter topology to minimize power consumption and employs seven such inverters in loop to generate pulses, OSC, of 250 Hz. The frequency of the ring oscillator is proportional to bias potential $NMOS\_BIAS$. The lowpass filter converts the square wave into a sine-like wave, $TEST\_SIG$. It utilizes a pseudo-resistor (to emulate a large resistance) and a capacitor. The sizing of the transistors of the pseudo-resistor and the value of the capacitor is chosen so as to obtain a cut-off frequency of nearly 250 Hz. The buffer is used to sharpen the transitions of the ring oscillator's output and utilizes inverters with a threshold voltage of half the supply voltage. The buffer's output, EN and $ENBAR$, is input to the digital frequency calibration circuit. The calibration circuit extracts the information regarding the frequency of EN signal and generates necessary correction bits, $SWB < 0 : N >$, to change $NMOS\_BIAS$ voltage such that the frequency of the ring oscillator is very near to 250 Hz. A Hz-range oscillator, operating from a 0.5 V supply and consuming average power of 44.4 pW, is reported in [176]. But it involves a complex switching mechanism, which is avoided by using a simple ring oscillator.

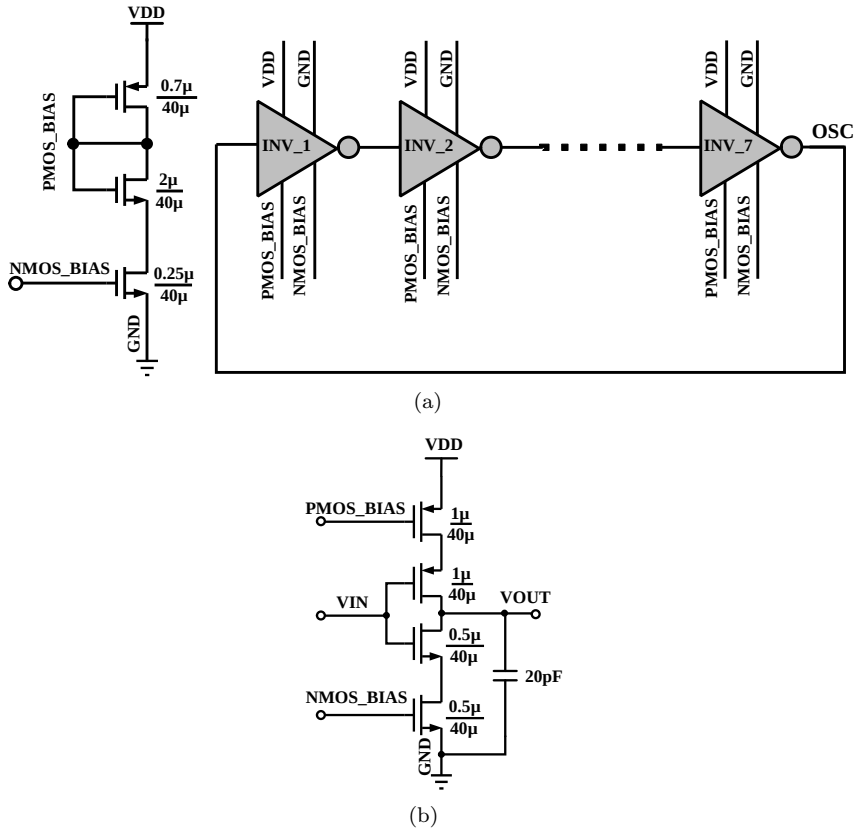


Figure 4.9: (a) Shematic diagram of the ring oscillator (b) Circuit diagram of the current-starved inverter used in the ring oscillator.

A. Ring Oscillator

The schematic diagram of the ring oscillator comprising of seven current-starved inverters in loop is shown in Fig. 4.9(a). The frequency of the ring oscillator is proportional to the potential $NMOS\_BIAS$, and is exploited as the electrical parameter to control the frequency of oscillation. The circuit diagram of the inverter is shown in Fig. 4.9(b).

B. Frequency Controlling Bias Selection Circuit

For a fixed value of the $NMOS\_BIAS$ voltage, the frequency of the ring oscillator's output changes for different process corners. This can be attributed to the variation in the performance of a MOSFET across process corners, e.g. typical-typical (TT), fast-fast (FF), and slow-slow (SS), etc., and the variation in the value of the load capacitors (Metal-Insulator-Metal capacitors) in each individual inverters (e.g. typical, minimum and maximum). Further the variation may correspond to any of the possible combinations of these different cases. The voltage values of $NMOS\_BIAS$ for which the frequency of the ring oscillator is roughly 250 Hz for each of such combination of corners is obtained from simulation. Thus a range of bias potentials, $VHIGH$ to $VLOW$, which needs to be

generated is obtained. A digital frequency calibration circuit is proposed which senses the frequency of the ring oscillator's output and then generates the necessary control signals to search and select the appropriate value of the $NMOS\_BIAS$ voltage which ensures that the frequency to be very nearly 250 Hz for any given process corner.

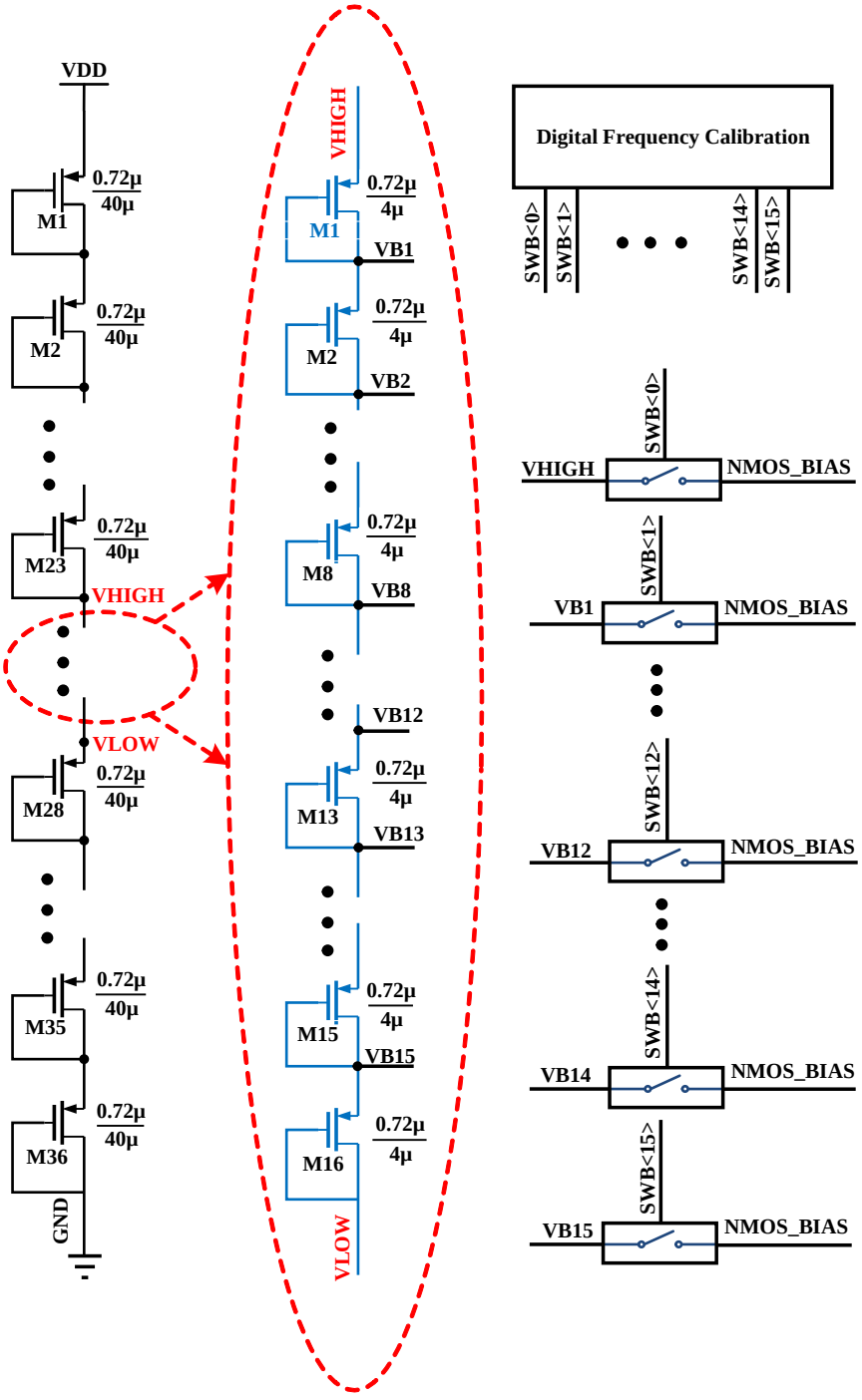


Figure 4.10: Schematic of the multiple bias generator circuit along with the bias selection logic.

A multiple bias generating circuit provides the digital frequency calibration circuit the different bias potentials as shown in Fig. 4.10. It can be divided into primary and secondary bias generation circuits and a switch array. The primary circuit works between the supply rails, and produces $VHIGH$ (= 0.65 V) to $VLOW$ (= 0.45 V) voltages. It comprises of thirty-six diode-connected PMOSs connected in series, and is shown in Fig. 4.10 with all its PMOSs in black color. Also, each PMOS's bulk is shorted to its source. Each diode-connected PMOSs behaves like a resistance and forms a simple resistive voltage divider circuit. The secondary circuit (enclosed in dashed red color ellipse) is similar to the primary, but consists of only sixteen PMOSs, operates between $VHIGH$ to $VLOW$ voltages and is shown in Fig. 4.10 with all its PMOSs in blue color. It produces sixteen bias potentials within $VHIGH$ to $VLOW$ for the calibration circuit to choose from. The switch array routes one of the bias voltages produced by the secondary bias generation circuit to the ring oscillator via $NMOS\_BIAS$ depending on the control signal ($SWB < 0 : N >$) from the digital calibration circuit. All the switches are realized as pass transistors.

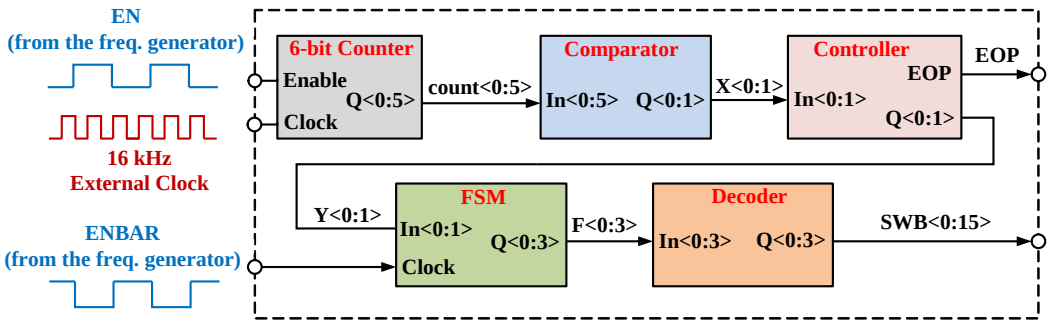


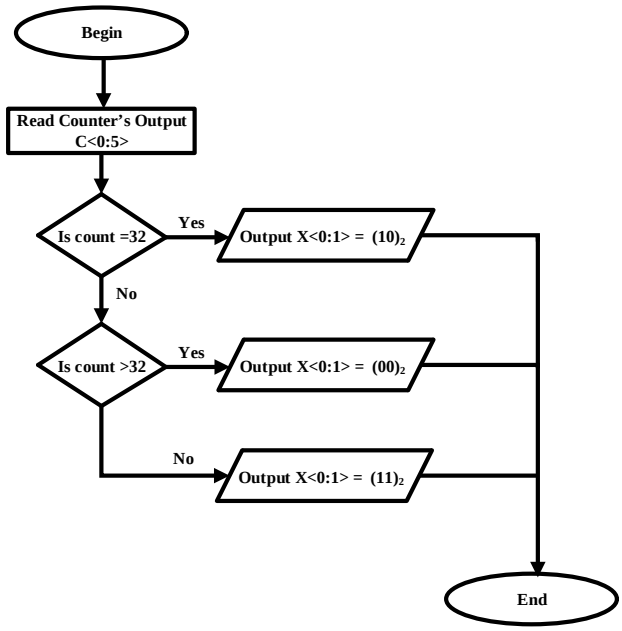
Figure 4.11: Digital frequency calibration.

C. Digital Frequency Calibration

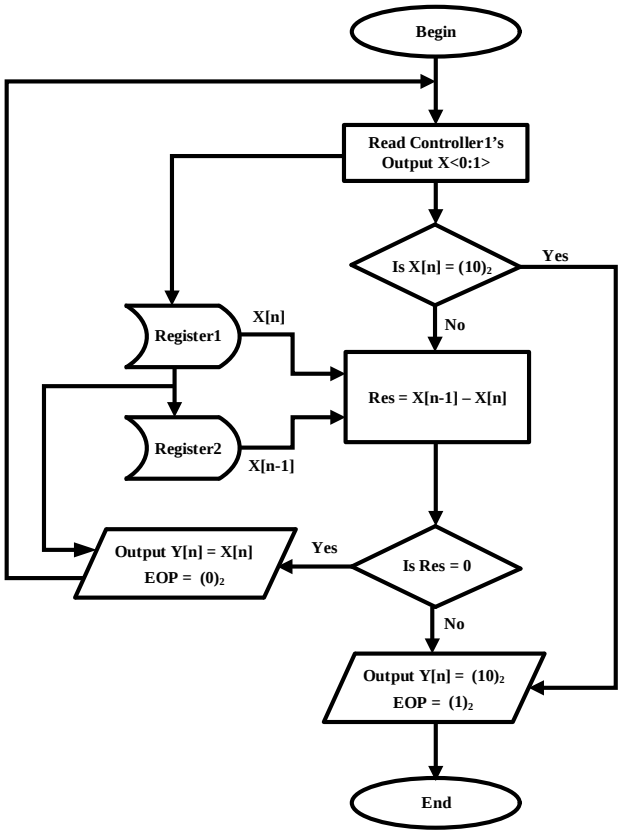
The block diagram of the digital frequency calibration is shown in Fig. 4.11. It consists of a 6-bit counter, a digital comparator, a controller, a finite state machine and a decoder. It has the two complimentary outputs of the frequency generator, EN and $ENBAR$, and an external reference 16 kHz clock as inputs.

The operating principle can be summarized as follows:

(i) The $6-bit\ Counter$ block estimates the frequency of the input EN by quantizing the 'on-time' using a higher external frequency clock (16 kHz). To understand the working, let's consider the case where the frequency EN is equal to 250 Hz. This implies that the 'on-time' of EN equals 2 ms, and a 16 kHz clock signal can complete exactly 32 cycles within this period. Similarly, if the frequency of the EN signal is greater(lesser) than 250 Hz, the 16 kHz clock can complete lesser



(a)



(b)

Figure 4.12: Flow chart (a) digital comparator (b) digital controller.

(greater) number of cycles. A 6-bit up-counter is employed as the aforementioned quantizer.

(ii) The digital comparator generates '10' or '00' ('11') if the number of cycles turns out to be equal or greater (lesser) than 32, respectively. The same is illustrated using a flow chart in Fig. 4.12(a).

(iii) Since the voltage resolution of the $NMOS\_BIAS$ calibration is finite, there might be a case where counter's output is greater than 32 for one value of $NMOS\_BIAS$ and lesser than 32 for the voltage in the next step. Then the proposed calibration scheme would be caught in a never ending loop. Therefore, the proposed technique avoids the occurrence of such an event using a controller. The controller checks the direction of each output form the comparator. To elucidate its functionality (flow chart in Fig. 4.12b) the counter detects more than 32 cycles for the default bias voltage $NMOS\_BIAS$. The calibration circuit should reconfigure itself so as to increase $NMOS\_BIAS$ in steps. This continues until the counter detects a count equal or less than 32 cycles for the first time. This is the instant when the calibration circuit ought to freeze its configuration.

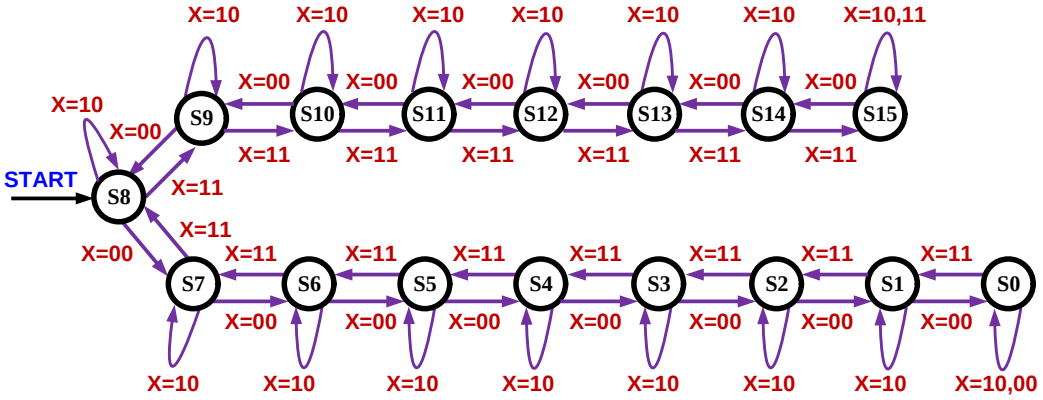


Figure 4.13: Transition digram of the FSM.

The comparator which continues to output a '11' till this instant, and would output a '10' or '00' after this. Hence, the aforementioned event can be detected by comparing the current and previous comparator's output. If both the values are equal the calibration procedure needs to continue by bypassing the comparator's output to the next stage. Otherwise the controller freezes the configuration by inputting '10' to the next stage and signals the end of calibration process by setting EOP high.

(iv) The output of the controller is fed to a 4-bit finite state machine (FSM). It transits between sixteen states (S0-S15) depending on the input from the controller. The transitions of the FSM corresponding each input is depicted in Fig. 4.13.

(v) The 4-bit output corresponding to a state of the FSM is input to a 16-bit digital decoder. The decoder's output is a one-hot key, i.e. only one among the sixteen bits is high at any time. Table 4.4

lists out the only bit among $SWB < 0:15 >$ which is set 'high' by the decoder, for each of the sixteen states of the FSM. Its switches only one of the sixteen bias selection switches ($SWB < 0:15 >$) 'on'.

Table 4.4: Output of the FSM and decoder

$F < 0:3 >$	'High' bit among $SWB < 0:15 >$
0000	$SWB < 0 >$
0001	$SWB < 1 >$
0010	$SWB < 2 >$
0011	$SWB < 3 >$
0100	$SWB < 4 >$
0101	$SWB < 5 >$
0110	$SWB < 6 >$
0111	$SWB < 7 >$
1000	$SWB < 8 >$
1001	$SWB < 9 >$
1010	$SWB < 10 >$
1011	$SWB < 11 >$
1100	$SWB < 12 >$
1101	$SWB < 13 >$
1110	$SWB < 14 >$
1111	$SWB < 15 >$

D. **Load Capacitor Selection Mechanism**

The load capacitor selection scheme is illustrated in Fig. 4.14. It consists of a two-phase generator, two peak detectors, capacitive charge redistribution circuit, a switched capacitor array, comparator and a load capacitor switch control logic. The proposed technique assumes that the AGC has fixed the gain of the PGA (with $C_{L,min}$ as the load capacitor) before the AFT procedure starts and AFT does not disturb the configuration of the PGA thereafter. Further the procedure for load capacitor selection starts only after the frequency calibration circuit of the frequency generator has finished its job of ensuring that the output of the frequency generator is very nearly equal to 250 Hz.

The sine-like output of the frequency generator, $TEST\_SIG$, is applied to the PGA with the gain fixed by the AGC. The operation of this scheme is as follows:

(i) The reference clock of 250 Hz generated by the ring oscillator shown in Fig. 4.9 is used by the phase generator to generate two complimentary phases, $Ph1$ and $Ph2$. Through simulations of the circuit of the peak detector it found out that it takes approximately 50 ms to charge its load capacitor (typically 30 pF) to the peak value of the input signal. Therefore a 9-bit counter is employed to make sure that the period corresponding to $Ph1$ is long enough to faithfully allow the load capacitor of the peak detector to charge to the peak value of the input signal. Similarly the clock frequency

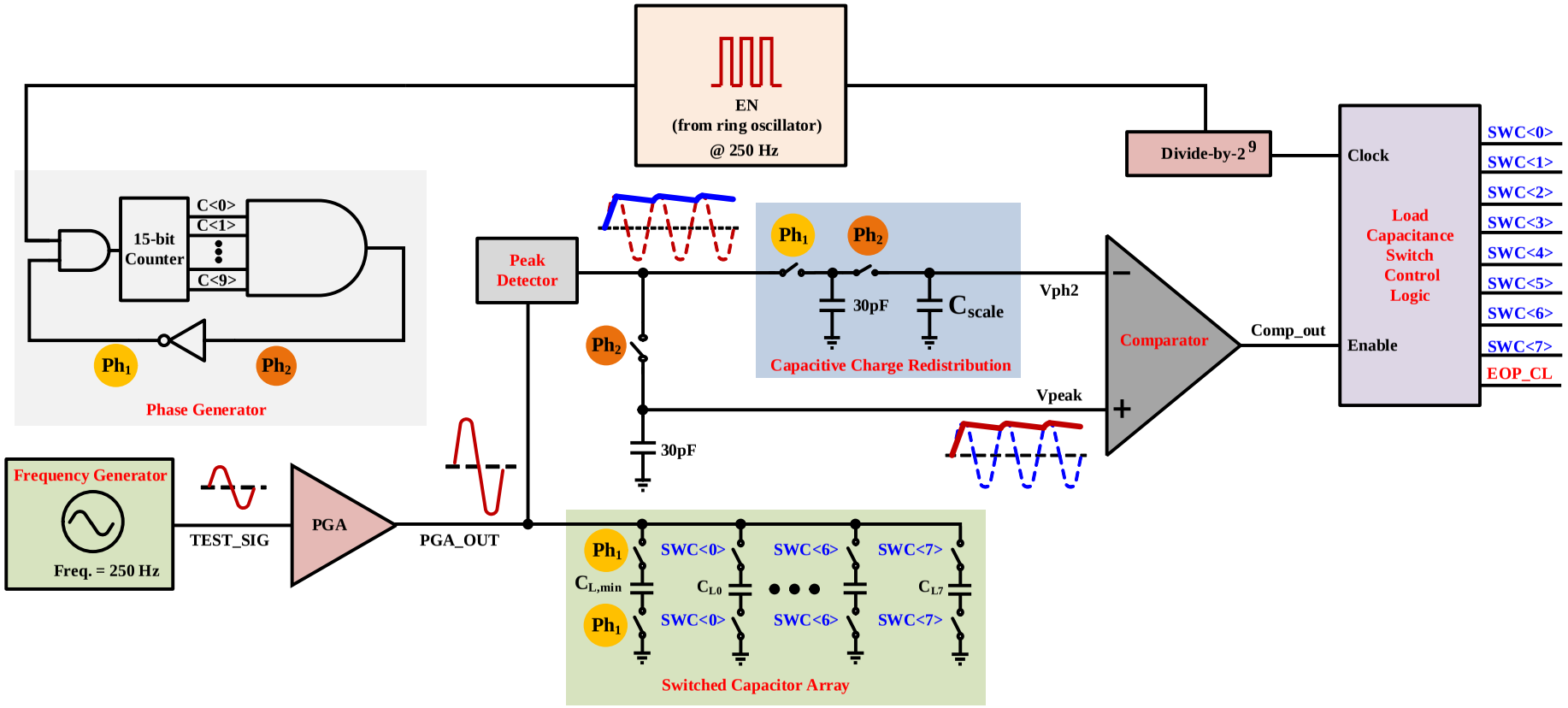


Figure 4.14: Schematic diagram of the load capacitor selection scheme.

for the load capacitance switch control logic is chosen such that for any switch configuration (or any value of net load capacitance) the peak detector has enough time to capture the peak of the PGA's output faithfully. Once $Ph1$ is high, $Ph2$ goes high and is continuously 'high' for rest of the period. In the proposed scheme, $Ph1$ marks the period in which the peak detector captures the peak of the PGA's output for a load capacitance $C_{L,min}$ (explained in Section 4.3.1). Similarly $Ph2$ represents the rest of the time where the peak detector captures the peak of the PGA's output for rest of the capacitors in the capacitor array, i.e. C_{L0} -C_{L7}.

(ii) The peak detector (Fig 4.2) is responsible for retaining the peak voltage level of the input signal [177].

(iii) The capacitive charge redistribution circuit consists of two capacitors (30 pF and C_{scale} capacitors) and two switches as shown in Fig. 4.14. After the 30 pF capacitor is fully charged during $Ph1$, this charge is redistributed between the 30 pF capacitor and C_{scale}. The value of the capacitor C_{scale} is (obtained from simulations) is chosen such that the voltage across C_{scale} is equal to $\frac{1}{\sqrt{2}}$ times the voltage stored in the 30 pF capacitor during $Ph1$.

(iv) The switched capacitor array is a set of nine capacitors ($C_{L,min}$, C_{L0}-C_{L7}) which appear as the load to the PGA sequentially in the order controlled by the load capacitance switch control logic. The value of $C_{L,min}$ is 4.06 fF and each capacitor C_{L0}-C_{L7} has a value ranging from 4.06 fF to 15 pF. This range of load capacitance required to ensure a lowpass cut-off frequency of 250 Hz is obtained from simulation across process corners.

(v) The comparator compares the voltage equal to $\frac{1}{\sqrt{2}}$ times the voltage stored in the 30 pF capacitor during $Ph1$ to the peak value of the PGA's output with net load capacitance at each instance. It outputs a 'low' when the peak voltage of the PGA's output just goes below the voltage across the C_{scale}.

(vi) The load capacitance switch control logic determines the sequence in which each capacitor C_{L0}-C_{L7} is added to form the net load capacitor for the PGA. The sequence in which each of the switches $SWC<0:7>$ are set to 'high' is given in Table 4.5. This logic sets each bit among $SWC<0:7>$ sequentially until the comparator's output goes 'low' and the EOP_CL is set 'high' marking the end of procedure of the load capacitor selection.

4.3.3 Post-layout Results

The complete proposed architecture is designed in UMC 0.18 μm CMOS technology. The post-layout extracted results obtained for the frequency generator (including calibration) and the subsequent

Table 4.5: Logic values of each bit among $SWC < 0:7 >$ for each clock cycle

	Bit # among $SWC < 0:7 >$							
Cycle #	0	1	2	3	4	5	6	7
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	0
8	1	1	1	1	1	1	1	1

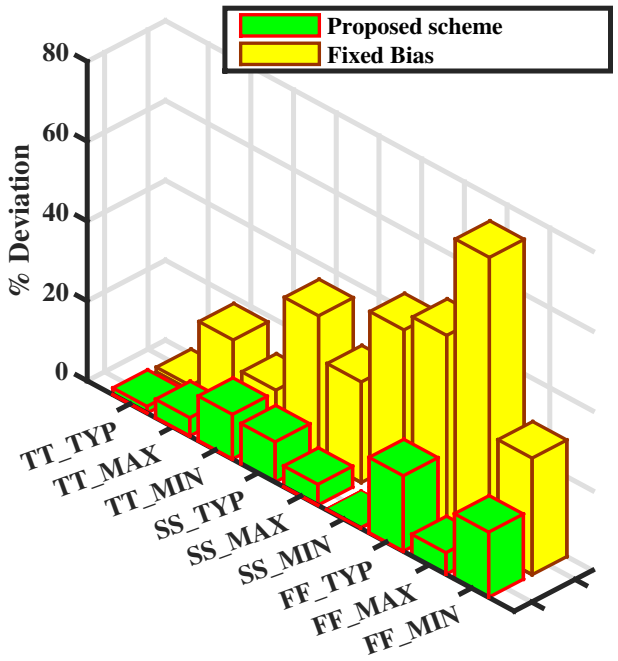


Figure 4.15: Bar plot showing % deviations of actual generated frequency w.r.t the nominal frequency of 250 Hz across different process corners.

load capacitor selection logic are presented in this section.

Table 4.6 lists out the actual frequency generated and the corresponding value of the bias voltage $NMOS\_BIAS$ from the proposed frequency generator. It can be observed that the frequency generated closely matches the desired value of 250 Hz. The proposed topology of frequency calibration by changing $NMOS\_BIAS$ is then compared to the case where $NMOS\_BIAS$ is fixed to 547.3 ms (see Fig. 4.9). The comparison is depicted in Fig. 4.15 as a plot of bar graphs of percentage deviation in the frequency generated, across different process corners, w.r.t. a nominal value of 250 Hz. For example, the label 'SS_MAX' represents a slow-slow corner w.r.t transistors and a maximum capacitor value for a given nominal value of a capacitor. Note that the label for process corners

should be comprehended in two parts, first part corresponding to transistor level variation and the second part corresponds to the capacitance variation. Both the cases exhibit maximum deviation for fast-fast process corner. Maximum deviation for frequency generation with fixed bias and with the proposed bias calibration is 73.6% and 16.32%, respectively. The figure clearly shows significantly lesser deviation for the proposed scheme for any process corner.

Table 4.6: Performance summary of the frequency generation and calibration

Process Corner	**MIMCAP**	**Frequency (Hz)**	**NMOS_BIAS (mV)**
TT	TYP.	245.8	534
	MAX.	261.5	525.84
	MIN.	222	536.32
SS	TYP.	224.8	591.79
	MAX.	236.96	578.79
	MIN.	250	623.66
FF	TYP.	202.75	496.42
	MAX.	236.51	464.91
	MIN.	209.2	479.79

The operation of the load capacitor selection logic is verified using the outputs obtained at relevant nodes (see Fig. 4.14) for a fixed value of gain of the PGA. The waveforms are shown in Fig. 4.16. The second sub-plot from top shows the stepwise reduction of PGA_OUT with addition of each subsequent load capacitor from the capacitor array. First during $Ph1$ the node $Vph1$ is charged to the peak value of the output of the PGA PGA_OUT (third from top). Then during $Ph2$, $Vph2$ attains a value equal to $\frac{1}{\sqrt{2}}$ times $Vph1$ during $Ph1$ (fourth from top). $Vpeak$ represents peak voltage of PGA_OUT during each temporal stage. The instant when $Vpeak$ goes just lower than the held value of $Vph2$, the comparator's output $Comp\_out$ goes high (fifth from top). The bottom most sub-plot displays the decimal value of the bus comprising $SWC < 7 : 0 >$. It shows that the switches go high sequentially until $Comp\_out$ is high and remains fixed after that. Fig. 4.17 plots the magnitude response of the PGA with and without calibration using the proposed AFT for a fast-fast process corner. It clearly shows that the PGA exhibits a more accurate lowpass cut-off frequency using the proposed AFT technique.

Finally, the average power dissipated in each individual block is listed out in Table 4.7. The total average power consumption is approximately 1.02 μW. Moreover the complete mechanism needs to run only for less half a minute, and hence proves its utility for portable battery batteryless self-powered ECG front-end systems. Table 4.8 presents a comparison of the proposed AFT technique w.r.t the existing state-of-the-art topologies. Although the percentage deviation form the normal

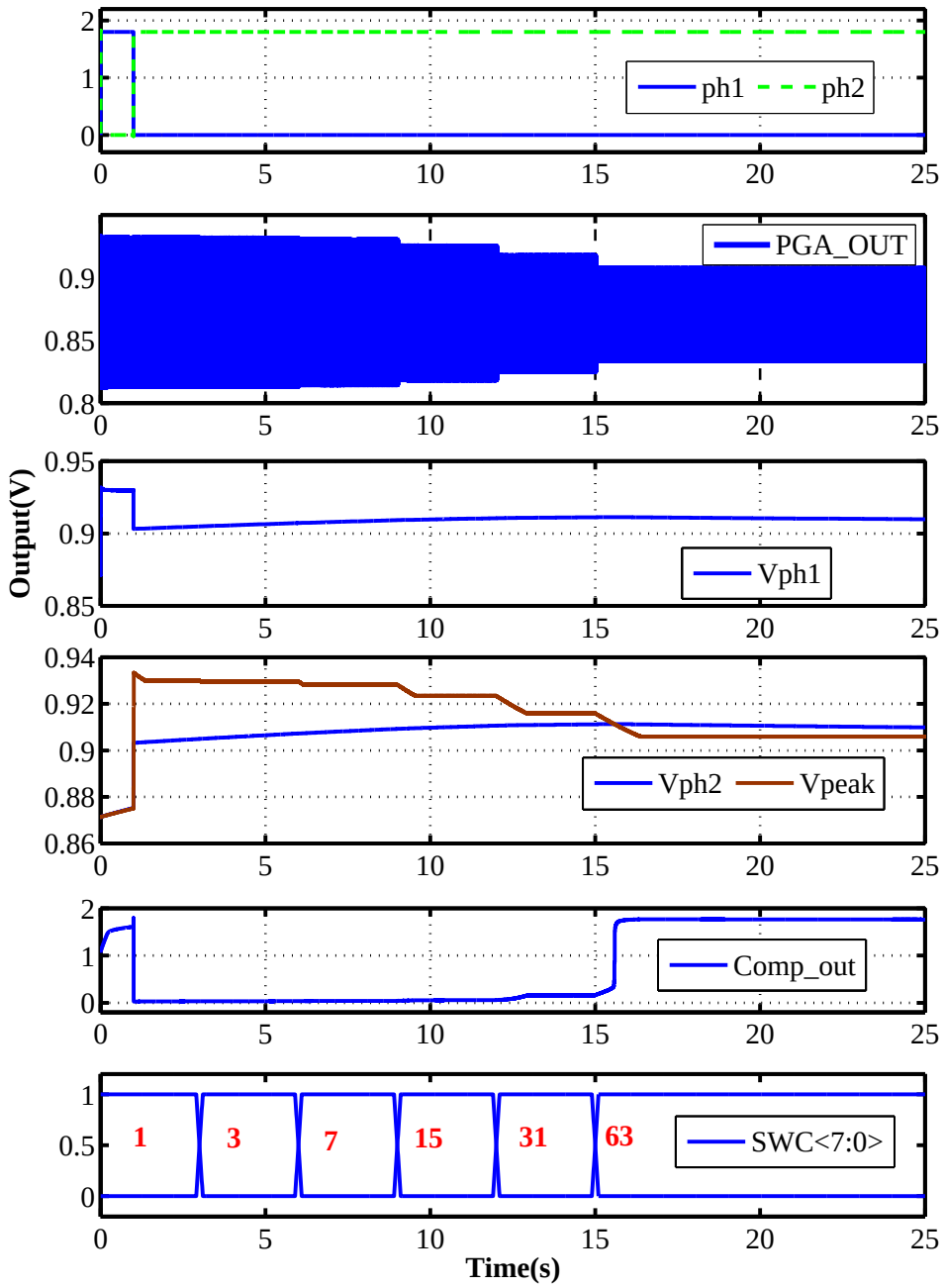


Figure 4.16: Relevant output waveforms of the load capacitor selection logic.

cut-off frequency is more than the state-of-art topologies, the absolute value of the deviation in frequency is much less. It can inferred from the above two tables that the proposed technique is better than the others in the following aspects (i) very low power consumption (ii) simple working principle and less complex hardware involved and (iii) no requirement of any extra replica of the main circuit.

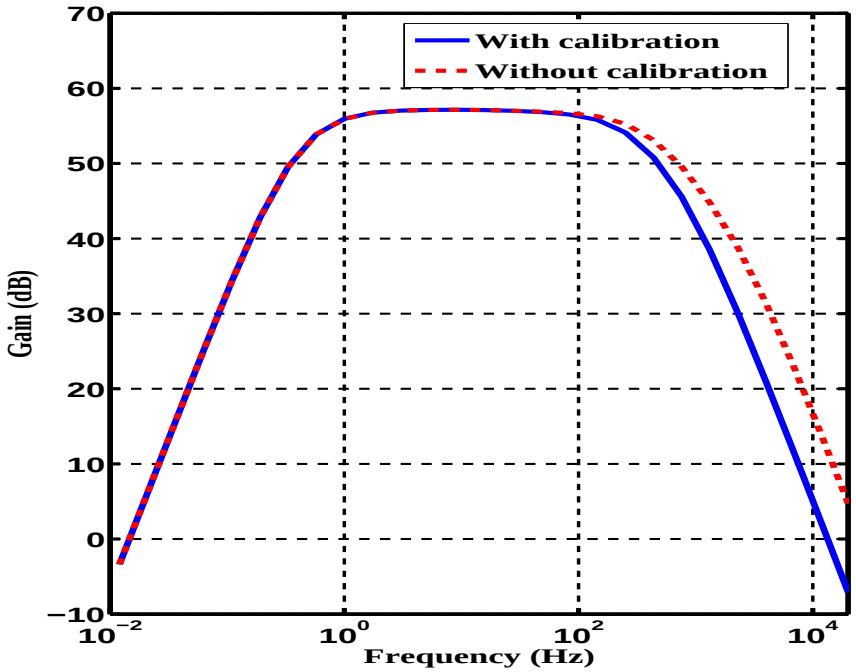


Figure 4.17: Magnitude response of the PGA with and without calibration.

Table 4.7: Average power dissipation in individual block of the proposed mechanism

Block	**Sub-block**	**Power dissipation**
Frequency Control Bias Generation		372.6 pW
Frequency Generation	7-stage ring oscillator	0.5 μW
Digital Frequency Calibration	6-bit counter	557.28 pW
	Comparator	786.78 pW
	Controller	14.6 nW
	FSM	16.2 nW
	Decoder	3.474 nW
Load Capacitor Selection	Phase generator	1.2 nW
	Peak detector	21 nW
	Comparator	24.03 nW
	Load Capacitance Switch Control Logic	443 nW

Table 4.8: Performance Comparison with state of art

Ref. No.	**Technology**	**Supply (V)**	**Filter Type**	**Cutoff Freq./ Center Freq.**	**Maximum Deviation (%)**	**Replica of Main Circuit Required**
[168]	0.18 μm SMIC	1.8	LPF	11 MHz	2.3	yes
[169]	0.18 μm CMOS	1.8	LPF	1.58 MHz	1.5	yes
[170]	0.35 μm MOSIS	2.3	LPF	80-200 MHz	5	yes
[172]	2 μm MOSIS	$\pm$ 2.5	BPF	3.58 MHz	2	yes
[174]	1.2 μm CMOS	3	BPF	105-120 MHz	0.3	yes
This work	0.18 μm CMOS	1.8	LPF	250 Hz	18	**no**

4.4 Measurement Results

After verifying the AGC and the AFC through post-layout simulations, the designs are fabricated. The pin distribution was planned so as to allow the testing of all the three blocks combined as a system, as well as each of them individually. The details of the tape-out are discussed here. The measurement results are also provided. Finally, the comparison of the design implemented here with the existing state-of-the-art is also reported.

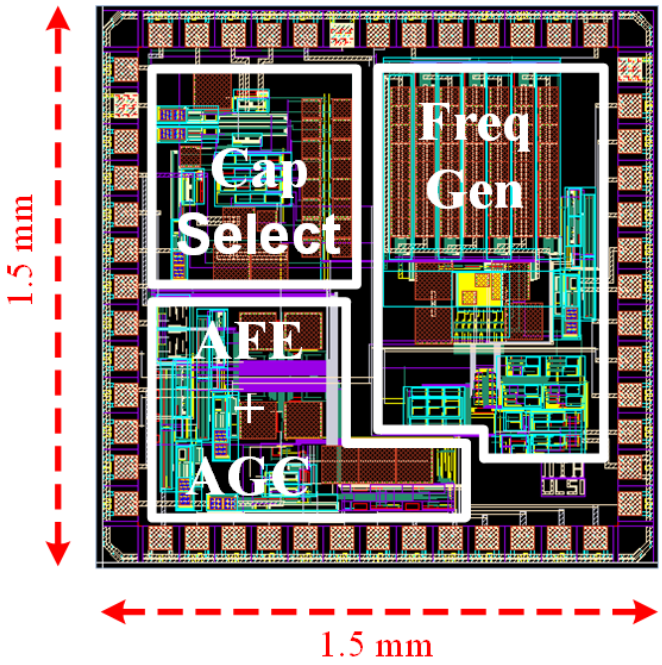


Figure 4.18: Die micrograph of the chip consisting the AGC and AFC.

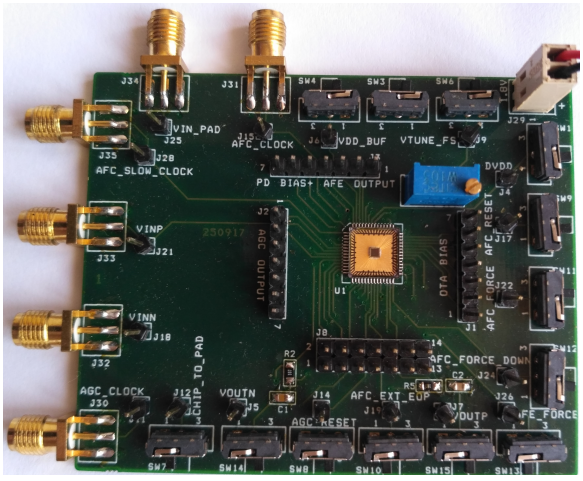


Figure 4.19: The PCB prepared to test the chip.

4.4.1 Results and Discussion

The measured results and analysis of the same is given here.

Measurement Setup: The following instruments were used for the testing the chip.

(i) Signal Generator (Tektronix AFG 3022) - used to give low frequency sinusoidal (< 100 Hz) and clock input to the AGC.

(ii) DC Voltage Source (Keysight Technologies E3631A) - used to apply the required DC supply voltage.

(iii) Oscilloscope (Keysight Technologies DSO 90404A 4 GHz) - used to view the time-domain waveform of the relevant outputs.

(iv) Digital Multimeter (Keysight Technologies 34401A) - used to measure the relevant DC voltages.

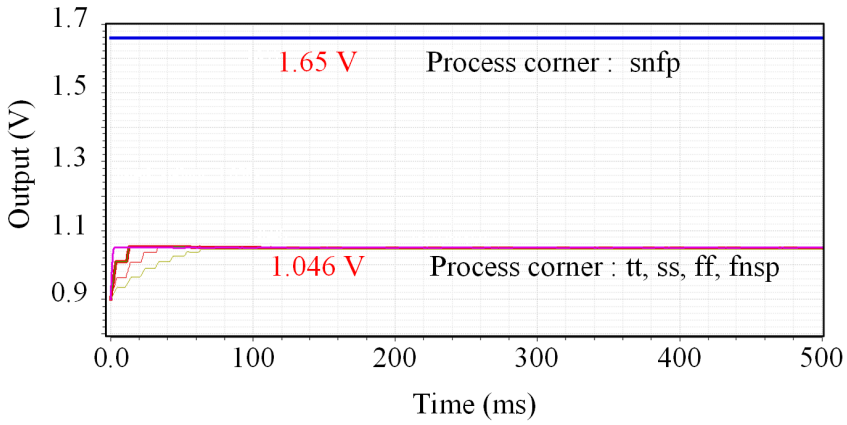


Figure 4.20: Response of the peak detector without on-chip bias generation circuit across different process corners.

- **AGC** : It consists of a peak detector and a digital implementation of a gain capacitor select logic.

  The measurement result with all bias voltages externally applied show that the output of the peak detector with is fixed to a voltage of 1.65 V, irrespective of the amplitude of the input signal. While debugging the reason for its failure, it was found that the peak detector does fails in the snfp process corner. The peak detector works as desired in rest of the corners. The peak detectors output for different corners are shown in Fig. 6.3.

  It is essential that all the bias voltages required for the peak detector are on-chip to make it work as desired across various process corners. Once the circuit generating the required

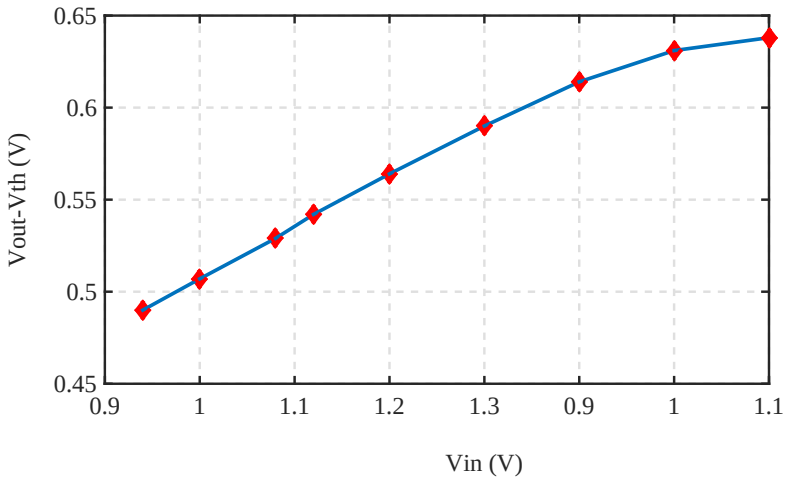
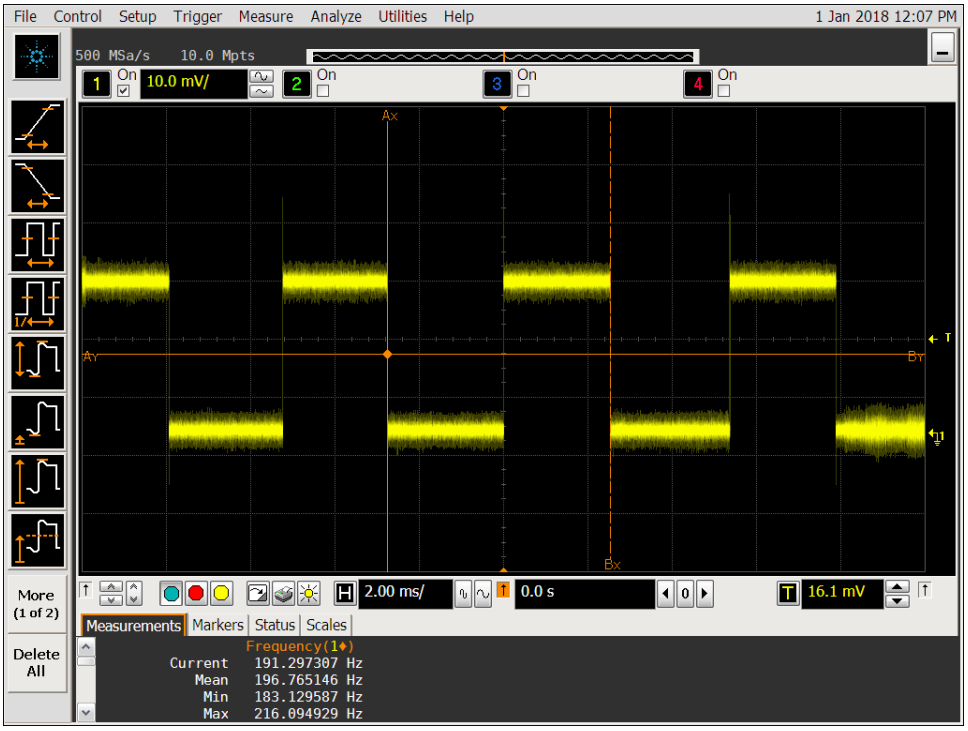


Figure 4.21: Variation of the peak detector's output with input amplitude.

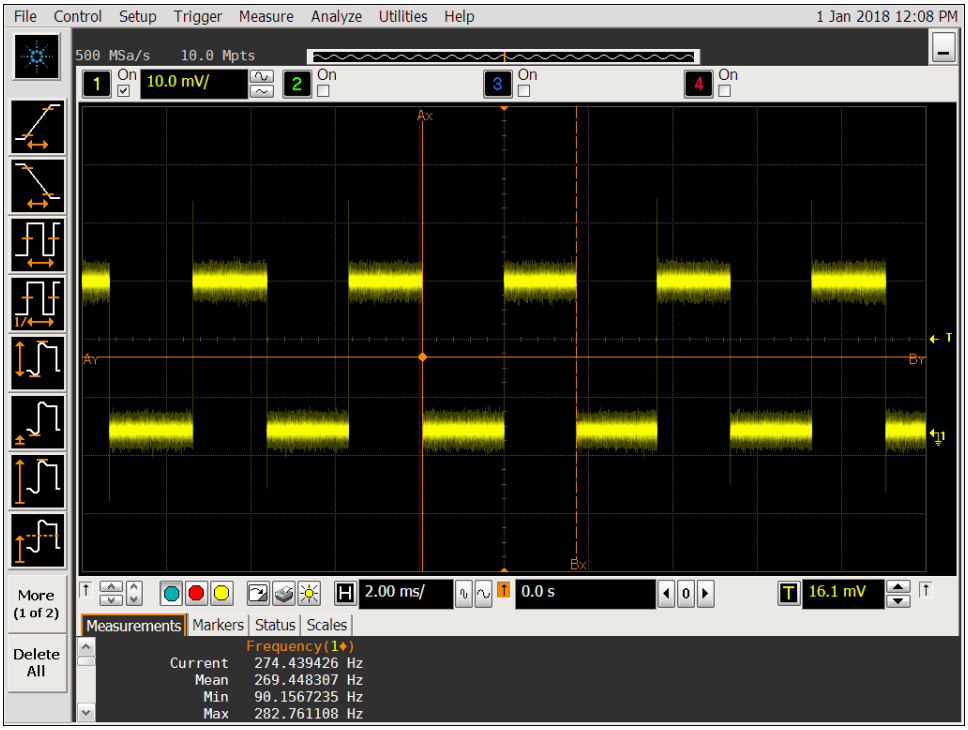
voltages is included in the design, the peak detector functions properly. The result form the fabricated chip shown in Fig. 6.5 shows that the peak detector functions as expected. The plot of the peak detector's output with input amplitude is given in Fig. 6.6. Note that the y-axis is labeled as (Vout-Vth) since the output of the peak detector is brought to the pads via a common drain buffer.

The rest of the circuit could not be tested because amplifier used in the scheme failed to perform as expected.

- **AFC** :
  - Ring Oscillator : The output pulses generated by the ring oscillator is shown in Fig. 4.22. Without enabling the digital frequency calibration circuit, the ring oscillator generates pulses of $\approx$ 180 Hz (Fig. 4.22a). After the digital frequency calibration circuit enabled the oscillator generates pulses of $\approx$ 270 Hz (Fig. 4.22b), which is closer to the desired nominal frequency of 250 Hz.
  - The rest of the circuit could not be tested because amplifier used in the scheme failed to perform as expected.



(a)



(b)

Figure 4.22: The output of the ring oscillator (a) without calibration (b) with digital calibration.

4.5 Summary

A simple low power implementation of AGC and AFC technique is discussed in detail here. Both, the working principle and circuit design are described. The complete scheme is implemented in UMC 0.18 μm CMOS technology with 1.8 volt supply. The working principle is verified using post-layout extracted simulation results. All the results obtained are as desired. The low hardware complexity and power consumption involved makes both these techniques suitable for remote self-powered long term continuous ECG monitoring systems. The power dissipation can further be reduced by designing all logical gates in current-starved mode.

Once the complete analog front-end shown in Fig. 2.6 is implemented, augmenting it with modules, capable of preliminary classification of critical cardiac arrhythmia, on the same analog platform is targeted in this work. This technique intends to reduce the power consumption of the overall system by reducing the computational burden on the conventionally employed DSP. Therefore, a fully analog QRS complex detector and a classification module for the detection of asystole, extreme bradycardia and extreme tachycardia is included to the front-end. The design details are provided in the next chapter.

Chapter 5

Analog QRS Complex Detector and Low Complexity Classifier for Asystole, Extreme Bradycardia and Extreme Tachycardia

5.1 Introduction

Electrocardiography has evolved as a wellspring of information for detection of numerous cardiac arrhythmia. Continuous and long-term ECG monitoring is indispensable specially in the case of elderly, handicapped and people with recurring cardiac disorders. Further, remote and rural healthcare services demand continuous ECG monitoring of the patient to support preventive and personalized services in real time for stationary patients, both in and out of the hospital. When augmented with an efficient alarm, such systems could alert the nearest emergency medical services and boost the safety of critically ill patients in real time, both in and out of hospitals. The detection of critical alarm types (*viz.* asystole, extreme bradycardia and tachycardia, and ventricular tachycardia and fibrillation) is paramount in such a scenario [31, 32, 178].

Contemporary smart ECG monitoring systems, shown in Fig. 5.1, intended for remote healthcare applications consists of an efficient sensing, 'analysis', and a wireless transmission platform [92, 179,

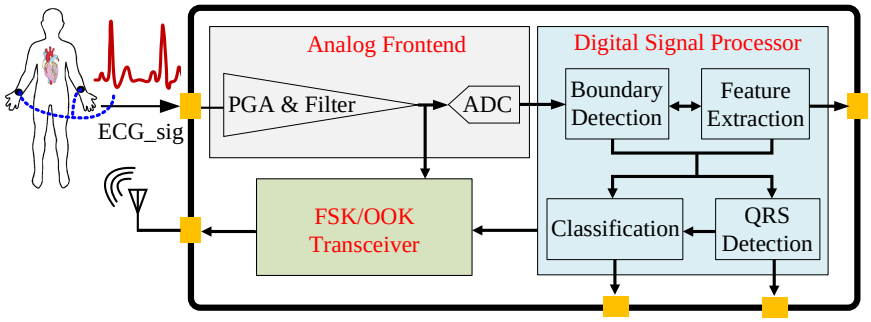


Figure 5.1: Block diagram of the conventional ECG recording system.

180]. The sensing/acquisition consists of a programmable gain amplifier (PGA), a bandpass filter and an analog-to-digital converter (ADC), and is conventionally implemented on an analog platform. Primarily 'analysis' of the ECG signal includes filtering, feature extraction and classification, and is conventionally implemented in digital domain. The required operations are implemented through a DSP [79, 181–184] on a system-on-chip (SoC) platform. Finally a FSK/OOK transceiver is used for transmission of the processed data [185]. The key point in all the traditional implementations is that the 'analysis', and transmission parts dominate the distribution of power consumption in the overall system [88].

However, DSP based techniques are more computationally intensive and consume power in the order of tens or hundreds of micro-watts, e.g. the systems in [79] and [181] report a power consumption of 345 μW and 31.1 μW respectively. This makes them incompatible with devices requiring long life span and intended for continuous ECG monitoring. Therefore the recently published works implement the functionality of feature extraction in analog domain [88, 186–188], rather than on a DSP. This enables significant reduction of system level power consumption by minimizing the computational burden on the DSP.

Detection of QRS complexes is the first step for any ECG classification scheme for cardiac rhythm (CR) and heart rate variability (HRV) analysis. Essentially the analog signal processors (ASP) in [88], [186–188] include an analog QRS feature extractor (FE) which is a power-efficient substitute for the predominantly employed computation-intensive continuous wavelet transform (CWT). This ASP assists the subsequent DSP for low-power signal analysis. [88] uses two bandpass filters for extracting the quadrature components of the ECG signal fluctuations within a specified range of frequencies. The DSP calculates the band-power by taking the sum-of-squares of the quadrature channels. The peaks in the band-power correspond to QRS complexes in the ECG signal. The width of the bandpass filter is determined by the switched capacitor (SC) low-pass filter (LPF),

because it offers a good trade-off between area and noise performance. The center frequency (16 Hz) and bandwidth (4.6-7.8 Hz) of the bandpass filter is optimized over MIT-BIH Arrhythmia database to achieve the sensitivity (SE) of 98.8% and positive predictivity (PP) of 99.8%. [186–188] also implement a similar FE for R-peak detection, which utilizes an analog first order bandpass filter with precise bandwidth control. The bandpass filter (10-15 Hz) comprises of a SC high-pass filter followed by a SC low-pass filter. The FE inputs to the DSP for band-power ($PWR = FE^2$) calculation. The DSP runs a beat detection algorithm utilizing an adaptive threshold by taking a low-pass filtered value of the PWR signal to detect the R-peak. It achieves the SE of 96.67% and PP of 100%.

All the above ASICs employ an ADC followed by a DSP to detect the location of R-peak and hence detect heartbeat. As discussed earlier, this is a power hungry approach. Hence, to remove the requirement of an ADC and signal processor, the topology in [69] proposes a comparator based topology for heartbeat detection, thereby reducing the overall system complexity, power and area. The ECG signal after preliminary amplification is fed to two subsequent amplifiers with equal gains, *viz.* a QRS complex and baseline amplifier. While the QRS amplifier preserves the features of the QRS complex, the baseline amplifier captures the low frequency baseline drift emanating from motion artifacts. Low pass corner frequency of QRS complex and baseline amplifier is kept to 25 Hz and 1 Hz, respectively. Then a positive inline DC offset is added to the output of the baseline amplifier to obtain an adaptive threshold voltage. A comparator generates a pulse whenever the output of the QRS amplifier exceeds the threshold voltage and marks the occurrence of a QRS complex in the ECG signal. The DC offset is controlled by an external microcontroller such that the period between the QRS pulses is regular and matches with that of human beings. The R-wave timing is estimated form the mid-point timing of the QRS pulses. Tested on normal chest ECG records from MIT-BIH Arrhythmia database totaling 2,304 heartbeats, this technique estimates the location of R-peaks with a standard deviation of R-wave timing error of only 1.25 ms. In case of irregular QRS complexes and rapid baseline wandering, the microcontroller reruns the calibration routine. If the recaliberation fails after enough number of iterations, then this topology identifies it as a case of arrhythmia. However, this topology involves an external microcontroller which consumes power in the order of micro-watts, even while using latest low power modules. Moreover, multiple runs of the calibration routine will further worsen the power budget of the system.

The three abnormalities targeted in this work, *viz.* asystole, extreme bradycardia and tachycardia, are critically significant w.r.t patients in the ICU or patients with chronic cardiac disease

residing in remote/rural areas. Both, extreme bradycardia (heart rate lower than 30 beats per minute approximately) and extreme tachycardia (heart rate higher than 180 beats per minute approximately) [189], occur as a consequence of reduced cardiac output. In the first case, the systolic output may not compensate for reduced beats per minute, and for the latter case it is reduced by the reduced filling time that is proportionately larger than expulsion time. Moreover, ventricular dysrhythmia (fast rhythms from bottom chambers) is associated with high morbidity and mortality. Symptomatic bradycardia that is likely to progress to asystole are Class 1 indications for pacemakers, and certainly need treatment and should receive pacemakers. Asystole means 'no systole ' or no pulse. It is annihilation of cardiac output and represents the extreme of bradycardia. When cardiac output is reduced drastically, say less than 3 liters per minute, then the brain and organ hypoperfusion occurs which is not a survivable situation without treatment. If cardiac output stops organs are damaged by ischemia, which becomes life-threatening in 2 to 4 minutes. When the heart beats very slowly (extreme bradycardia) or stops beating (asystole), it leaves no more than 2 to 4 minutes before irreversible brain damage occurs as the result of low cardiac output. Therefore, having an efficient alarming system is essential to prevent death [190, 191].

Motivated by the above discussion, this work presents a fully analog scheme comprising (i) an ultra low power on-line QRS detection circuit using an autonomous dynamic threshold voltage, hence discarding the need of any external microcontroller/DSP and calibration (ii) a power efficient analog classifier for the detection of three of the critical alarm types *viz.* asystole, extreme bradycardia and tachycardia [189]. In the event of detection of any one of the three target cardiac disorders, the system raises an immediate alarm. An important value addition to the acquisition systems like [156], the proposed scheme intends to alert the proximate medical service agency in case of remote monitoring, and alert the hospital staff in case of in-hospital patients. The proposed modules are successfully validated through the test signals taken from MIT-BIH arrhythmia database (MITDB) and [189]. The proposed architecture targets only three alarm types (*viz.* asystole, extreme bradycardia and tachycardia), leaving the other two (ventricular tachycardia and flutter/fibrillation) mentioned in [189]. This can be attributed to the hardware complexity associated with the algorithms meant for the detection of the later two. Since a full custom analog implementation of such a complex system would turn out to be an arduous task, their implementation is preferred in the automated digital domain. Also it is worth mentioning from clinical application perspective that the prime purpose of this system is to classify and hence assist in the preliminary prognosis of the above mentioned abnormalities. A more accurate, detailed and unequivocal diagnosis of the patient's clinical condi-

tion is still assigned to the more computationally intensive and power hungry DSP. Therefore, the proposed classification scheme presents a useful trade-off between complexity, accuracy and power consumption.

5.2 Proposed Classifier Topology

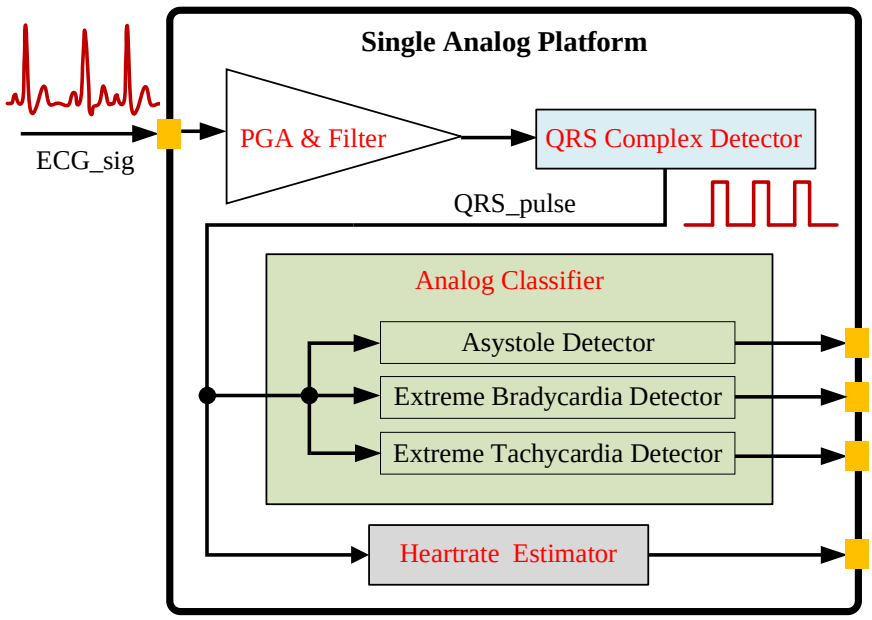


Figure 5.2: Block diagram of the proposed scheme.

The complete scheme is shown in Fig. 5.2. The blocks within the shaded region are the suggested additions to a standard continuous ECG monitoring system. This scheme includes a circuit that generates a pulse at every occurrence of QRS complex in the ECG signal, and three low complexity counter based modules for the detection of each of the target cardiac disorders. The essence of the proposed architecture is implemented on a single analog platform along with the signal conditioning block. The criteria for detection of each of the target cardiac arrhythmia is adopted from [189]. The working principle of the overall system and each individual modules is summarized in the form of an algorithm given below.

Algorithm 2 Detect occurrence of each QRS complex and thereby detect asystole, extreme bradycardia and extreme tachycardia

Let *A_detect*, *B_detect* and *T_detect* be the alarms for asystole, extreme bradycardia and extreme tachycardia respectively

Input: Appropriately amplified and filtered ECG signal *ECG_sig*

  ****
  ****** **QRS Complex Detector** **************
  ****

  Detect event of each R-peak
  if R-peak is detected **then**
    Generate a logic high pulse *ECG_pulse*
  end if
  ****
  ****** **Analog Classifier** ********************
  ****

Input: *ECG_pulse*

  ****** Asystole Detector *******
  if No *ECG_pulse* for at least 4 seconds **then**
    $A\_detect \leftarrow logic\ high$
  end if
  ****** Extreme Bradycardia Detector *************
  if Heart rate $<$ 40 bpm for 5 consecutive beats **then**
    $B\_detect \leftarrow logic\ high$
  end if
  ****** Extreme Tachycardia Detector *************
  if Heart rate $>$ 140 bpm for 17 consecutive beats **then**
    $T\_detect \leftarrow logic\ high$
  end if
  ****
  ****** **Heartrate Estimator** *****************
  ****

  Count the number of *ECG_pulse* occurring in 1 minute i.e. *bpm*
  ****

Output: *A_detect*, *B_detect*, *T_detect* and *bpm*

A detailed explanation of the formulation and working principle of each of the constituent blocks is given in the following subsections.

5.2.1 QRS Complex Detector

The QRS detection module implemented in this work consists of a peak detector, a capacitive voltage divider, a DC voltage clamping circuit and a comparator, as shown in Fig. 5.3. The proposed circuit works on the premise that the QRS complex (or heartbeat) has a higher amplitude compared to other ECG features, and hence can be detected whenever the voltage of the ECG signal is greater than a suitable threshold value. A threshold value of half the R-peak amplitude is chosen here keeping a safe enough margin over the $P-$ and T-peak excursions. First, the ECG signal, ECG_sig, after being appropriately amplified and filtered by the front-end, is fed to a peak detection circuit whose output tracks the R-peak amplitude V_{R-peak}. Second, the peak detector's output is fed to a capacitive voltage divider circuit to produce a dynamically adjustable threshold voltage, V_{TH}. Finally, the ECG signal and V_{TH} are fed to a comparator to generate pulses, ECG_pulse, to indicate the presence of QRS complexes. The pseudo-resistor clamps the DC voltage of V_{TH} to half the supply voltage. This bias potential ($= 0.9V$ here) is derived from a bias circuit consisting of diode-connected PMOSs in series.

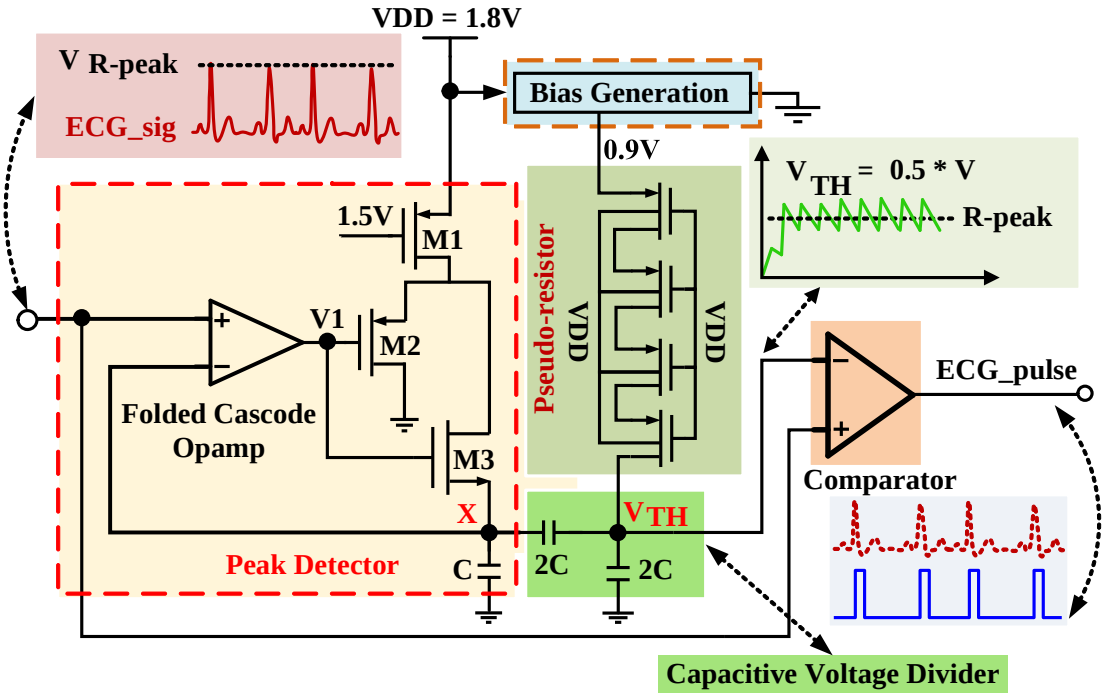
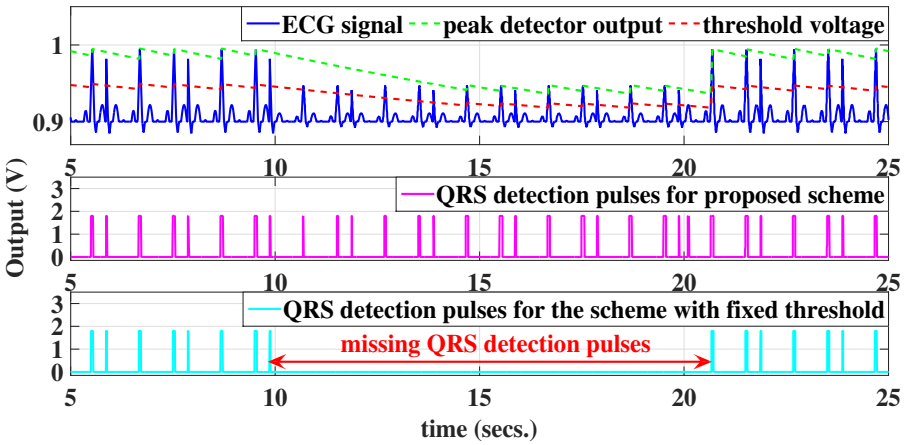


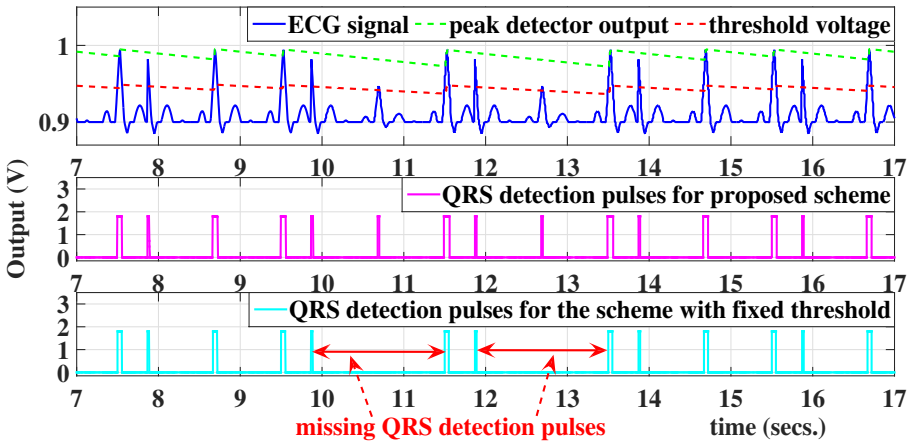
Figure 5.3: Circuit for QRS complex detection.

The peak detector circuit consists of an amplifier with high open loop DC gain, a current source (M1), current steering transistors (comprising of M2 and M3), an effective load capacitance (comprising of C and 2C) and a conventional continuous-time comparator. When voltage at node 'X' is lesser than the input ECG_sig, the amplifier generates a logical *high* (=1.8 V here) output V1, such that the current from M1 is steered to the capacitors via M3. The capacitors continue to get charged till the voltage at node 'X' is just greater than the ECG_sig. Then the amplifier outputs a logical *low* (=0 V here) voltage so that the current from M1 is steered to ground via M2, while the capacitors hold the voltage across them. The amplifier is responsible for producing a voltage V1, such that the voltage at node 'X' always tracks the input ECG_sig. The amplifier on the peak detection circuit is a folded cascode operational transconductance amplifier. Evaluating the noise contribution of each of the constituent transistors, the g_m/I_D [131] technique is utilized for sizing the transistors to optimize power consumption and noise. Moreover, the input transistors are operated in moderate inversion to reduce flicker noise. The value of capacitor labeled 'C' in Fig. 5.3 (C=10 μF here) is optimized after evaluation of the performance metrics *viz.* sensitivity and accuracy of the heartbeat detection scheme and classifier. Also the net load capacitor is expected to introduce a time delay between ECG_sig and the input at the negative terminal of the comparator. But this delay is not a critical issue here because (i) the input ECG is a low bandwidth (or slow) signal (ii) the unity gain bandwidth (UGB) of the loop gain of the feedback configuration within the peak detector is kept very high compared to the input signal's bandwidth. Moreover, this argument is vindicated by the results obtained after the proposed method is tested for multiple ECG records from [189] and MITDB. The total power consumption of this block is 21 nW.

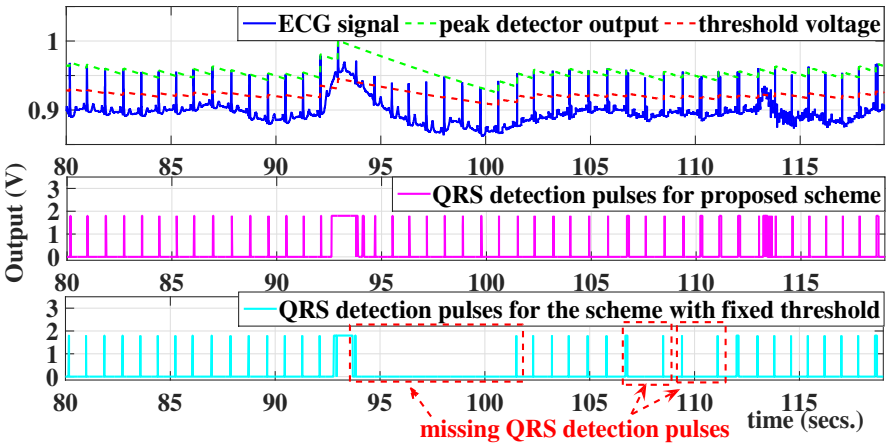
The QRS complex detection module performs more accurately compared to the scheme with a fixed threshold voltage when the input ECG signal has varying QRS complex amplitudes and rapid baseline wandering. Fig. 5.4 illustrates the comparison between the output QRS detecting pulses produced by the proffered QRS complex detection circuit (in magenta color) and the scheme with fixed threshold voltage (in cyan color). The figures also display the output of the peak detector (in green color) and the dynamic threshold voltage(in red color) fed to the comparator to detect the QRS complexes. As shown in Fig. 5.4*a-c*, the scheme with a constant threshold voltage fails to detect some of the QRS complexes, while the circuit presented here successfully detects all of them. Moreover, the input ECG signal may suffer baseline wandering even if a baseline wander filter with a fixed cut-off frequency is used in the frontend. This is because the spectral content of the baseline wander (typically 0.05-1 Hz) varies significantly, specially considering motion artifacts.



(a) Input with lower amplitude QRS complexes for some duration of time.



(b) Input with intermittent variation in the amplitude QRS complexes for short duration of time.



(c) Input with baseline wandering.

Figure 5.4: Comparison between the proposed QRS complex detection circuit and the scheme with fixed threshold voltage (= 0.95 V here) using the output pulses for different types of ECG signals.

Hence, this module was tested for ECG signals with baseline wandering from MITDB. Fig. 5.4c shows results for record #101 from MITDB. It also shows that the suggested circuit detects QRS complexes with more accuracy compared to the one with fixed threshold voltage, since the latter exhibits some missing QRS complex pulses. Further, when the technique in [69] fails to detect QRS complexes with one threshold voltage, it needs to rerun the calibration routine. In the case where the amplitudes of QRS complexes frequently vary significantly, e.g. exercise induced variations, it might wrongly identify the input ECG signal as arrhythmia. On the contrary, the QRS detection circuit presented here operates autonomously and uses a dynamically adjustable threshold voltage thereby avoiding such a situation. Finally, the technique is tested on ECG records from ten subjects totaling 1400 heartbeats from MIT-BIH Arrhythmia Database (MITDB). The proposed method achieves a better sensitivity of 99.28% and an accuracy of 93.24%, compared to the one with a fixed threshold exhibiting a sensitivity of 92.14% and an accuracy 91.48%. Therefore, the QRS detection technique in this work proves to be a more accurate and an efficient improvisation over [69].

The proffered circuit for QRS complex detection has the following advantages over that in [192] (i) it does not involve a micro-controller and (ii) it does not need to be calibrated, and hence completely automatic and power efficient (iii) since the threshold value for comparison is derived from the R-peaks itself, this topology works fine for ECG signals with varying amplitudes and rapid baseline (iv) the proposed circuit is compatible with the scheme of recovering the ECG R-wave timing from the QRS detection pulses mentioned in [69].

5.2.2 Proposed Classification Modules

The proposed classification scheme comprises of three individual modules for the detection of asystole, bradycardia and tachycardia. The working principles of each of these modules are discussed below.

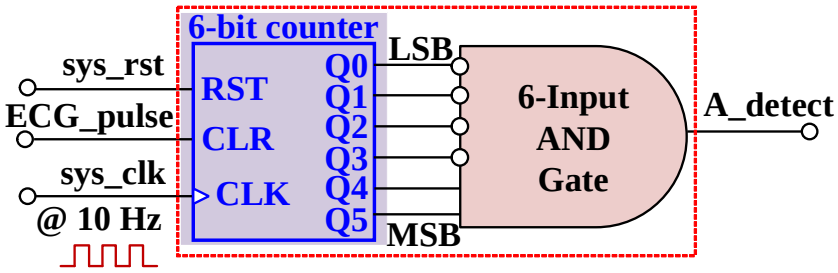


Figure 5.5: Scheme for the detection of asystole.

Asystole Detector

Absence of any QRS complex for at least 4 seconds is considered as the criterion for detection of asystole [189]. A counter based technique is applied to identify any event of asystole and raise an alarm (Fig. 5.5). Operating at a clock frequency of 10 Hz, a 6-bit counter increments its count by one whenever it encounters a positive edge of the clock. Whilst up-counting, the counter is reset at the instant of arrival of an ECG pulse. If the counter reaches a count of 40 (10 cycles per secs. $\times$ 4 secs.), or $(101000)_2$, without getting reset, A_detect goes *high* indicating the occurrence of asystole.

Extreme Bradycardia Detector

Heart rate lower than 40 beats per minute for five consecutive beats is considered as the criterion for identification of extreme bradycardia [189]. The proposed technique estimates the time duration for every five consecutive ECG pulses. A time duration greater than 7.5 seconds $(\{60 \ \ secs./40 \ \ beats\} \times 5 \ \ beats)$ for any quintuple indicates the above abnormality.

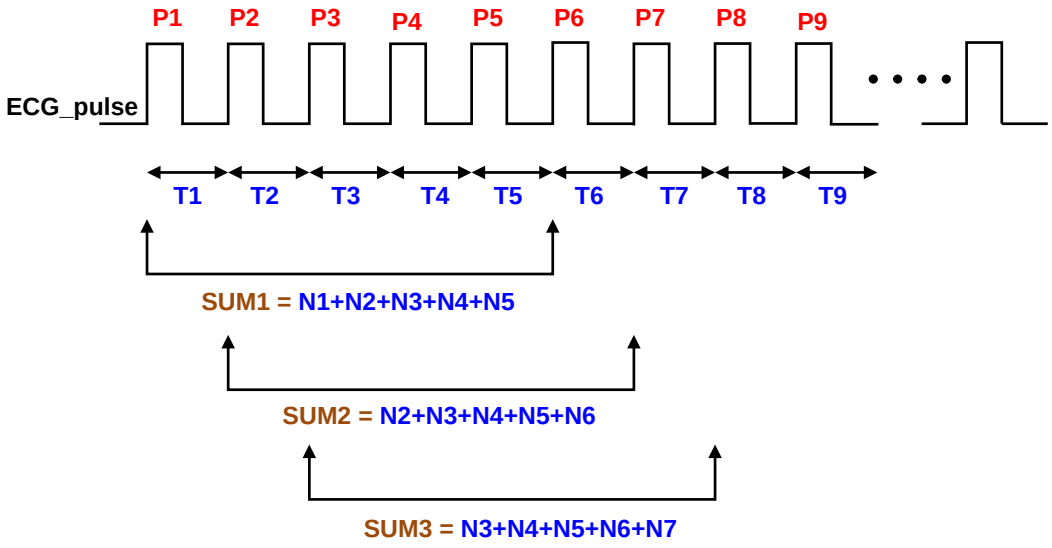


Figure 5.6: Working principle for the detection of extreme bradycardia.

A simplified illustration to explain the working principle of the proposed technique to detect bradycardia is shown in Fig. 5.6. To understand the scheme, let us assume P1, P2, P3, etc. be the first, second, third, etc., ECG pulses generated by the QRS generation circuit. Also, consider T_1 to be the time interval between any two consecutive positive edges of ECG_pulse signal, T_2 be the time interval between the next two consecutive positive edges, and so on. Then, a clock of higher frequency (30 Hz here), is used to estimate the duration between any two consecutive ECG

pulses. Again, consider N_1 to be the count of the number of higher frequency pulses within T_1, N_2 to be the count of the number of higher frequency pulses within T_2, and so on. The aim is to have a count of number of clock pulses for a period of $(T_1+T_2+T_3+T_4+T_5)$, $(T_2+T_3+T_4+T_5+T_6)$, and so on. The count of higher frequency pulses for each interval is then added to find SUM_1 $(= N_1+N_2+N_3+N_4+N_5)$, SUM_2 $(= N_2+N_3+N_4+N_5+N_6)$, and so on as shown in the diagram. Finally, each of the sums are fed to a comparator which produces *high* output when any of these sums is greater than a fixed value. Here, this fixed value is 225 (30 cycles per sec. $\times$ 7.5 sec), or $(11100001)_2$. The transition of the comparator's output from *low* to *high* signals the detection of bradycardia.

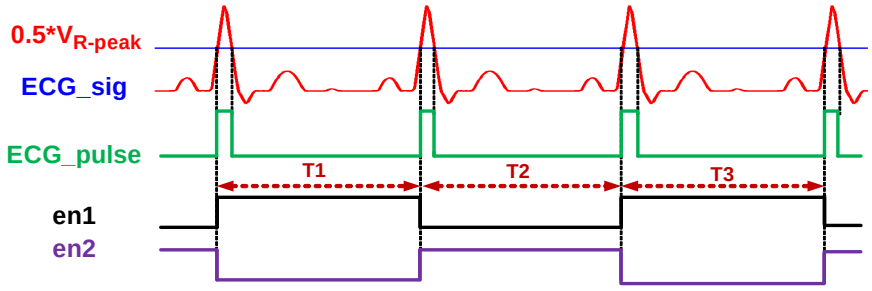


Figure 5.7: Generation of $en1$ and $en2$ from ECG_pulse.

Next, to have a count of clock pulses within a duration of T_1, an enable signal $en1$ is derived which is *high* for a duration T_1. After T_1, this enable signal should go low so that the count at the end of T_1 can be registered. Then, since the count corresponding to period T_2 is also required, another enable signal $en2$ should go *high* for T_2. Thus to obtain a count corresponding to each interval between heartbeats, $en1$ and $en2$ need to work in tandem. This is shown in Fig. 5.7. Two counters are employed to do the required counting. The first and second counter works when $en1$ and $en2$ is *high* respectively. Also, the first and second counter gets reset when $en1$ and $en2$ goes low respectively. Moreover, since the second counter should start counting when the first counter stops counting, two counters are imperative here.

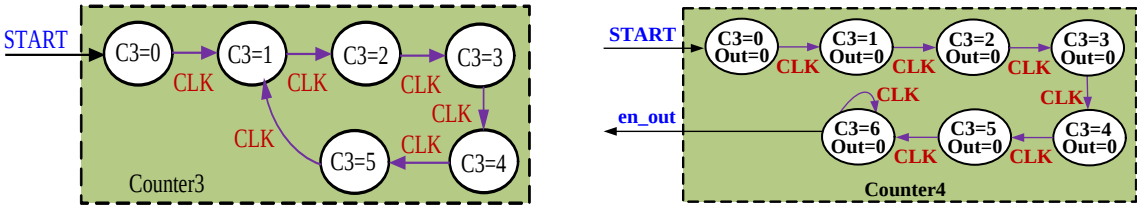
Further, it is required to store each of the counts N_1, N_2, etc. using five registers and sum each quintuple of counts. The sequence of values stored in each register with respect to each ECG pulse is shown in Table 5.1. To find the sum of each quintuple of values as shown in Fig. 5.6, the counts should be stored in the given sequence. Each new value that is stored and the corresponding register is shown in same color. A state machine (State Machine 1 in Table 5.1) is required to store each values to the corresponding register in the given sequence. The sequence of transitions of this state machine is shown in Fig. 5.8a. Moreover, the color of the output of this state machine and

the register into which the new count is to be stored is kept in same color in Table 5.1 to make the understanding of the operating principle easier. The duration for initial few ECG pulses is also worth noticing. It is essential to wait for enough number of ECG pulses before each register has a valid data and their sum is sent to the comparator. As is seen in Table 5.1, a valid sum has to be sent to the comparator only after first five ECG pulses. A second state machine (State Machine 2 in Table 5.1) is used to implement the same and puts a flag (Data_Ready_for_Comparison) *high* after five ECG pulses. The sequence of transitions of this state machine is shown in Fig. 5.8b.

Table 5.1: Sequence for data storage in the registers transition of state machines employed with respect to ECG pulses

ECG_pulse #	RST	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11
Register 1	0	N1	N1	N1	N1	N1	N6	N6	N6	N6	N6	N11
Register 2	0	0	N2	N2	N2	N2	N2	N7	N7	N7	N7	N7
Register 3	0	0	0	N3	N3	N3	N3	N3	N8	N8	N8	N8
Register 4	0	0	0	0	N4	N4	N4	N4	N4	N9	N9	N9
Register 5	0	0	0	0	0	N5	N5	N5	N5	N5	N10	N10
SM1[a]	0	1	2	3	4	5	1	2	3	4	5	1
SM2[b]	0	1	2	3	4	5	6	6	6	6	6	6
DRCF[c]	0	0	0	0	0	0	1	1	1	1	1	1

a - State Machine 1 (Counter3); b - State Machine 2 (Counter4); c - Data_Ready_for_Comparison Flag



(a) Sequence of transitions for *Counter*3.

(b) Sequence of transitions for *Counter*4.

Figure 5.8: Block diagram of the proposed analog classification module.

The circuit implementation of the scheme discussed above is illustrated through a block diagram in Fig. 5.9. The block labeled *en_gen* generates two mutually complimentary signals, *en*1 and *en*2. Operating on a clock @ 30 Hz, *Counter*1 and *Counter*2, working in relay, count the number of clock cycles within the duration for which *en*1 and *en*2 is *high* respectively. The two state machines of Fig. 5.8a and Fig. 5.8b are implemented using two counters *Counter*3 and *Counter*4, respectively. The *Controller* is responsible for storing the counts generated by *Counter*1 and *Counter*2, *C*1 and *C*2, in corresponding registers in the sequence explained in Table 5.1 and generating the sum of every quintet of registers' content. The block labeled *Count_out* acts a gate and allows the sum of counts to be fed to the comparator only after the output of *Counter*4, *en_out*, becomes *high*. The

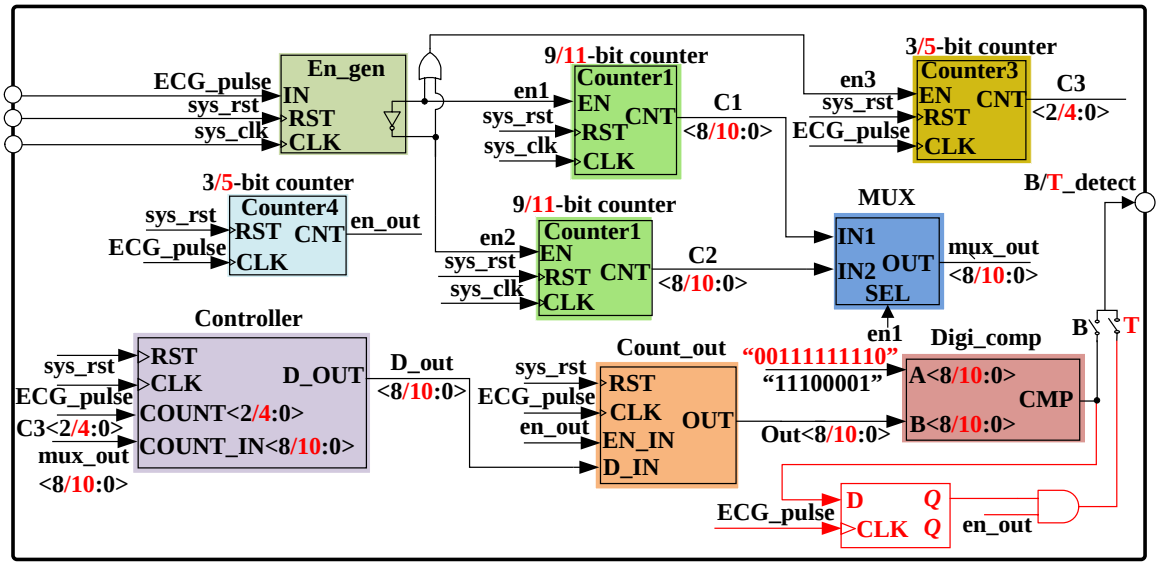


Figure 5.9: Combined block diagram of the modules for the detection of extreme bradycardia and tachycardia. The annotations and blocks in red color are applicable only for the module pertaining to tachycardia.

Digi_comp is a comparator which makes *B_detect* go *high* if the output of the *Count_out* is greater than $(225)_{10}$.

The proposed architectures for the detection of extreme bradycardia and tachycardia are very similar to each other, and hence their diagrams have been clubbed together in Fig. 5.9.

Extreme Tachycardia Detector

Heartrate higher than 140 bpm for 17 consecutive beats is considered as the criteria for identification of extreme tachycardia [189]. This technique differs from that for bradycardia only in terms of the word-length of the counters and decisive count values. Note that unlike bradycardia, the output of *Count_out* needs to be lower than a fixed value. Hence, some extra circuitry is required to wait till *en_out* is *high* and a valid comparison can be done by the *Digi_comp*.

5.2.3 Heartrate Estimator

This module provides an estimate of beats per minute or heartarte. Its operating principle is illustrated in Fig. 5.10. Operating with a clock @ 10 Hz, a 10-bit counter
(10 cycles per second $\times$ 60 secs = 600 cycles, or $(1001011000)_2$) gets reset after a duration of every one minute. Another 8-bit counter counts the number of ECG pulses as long as count from the

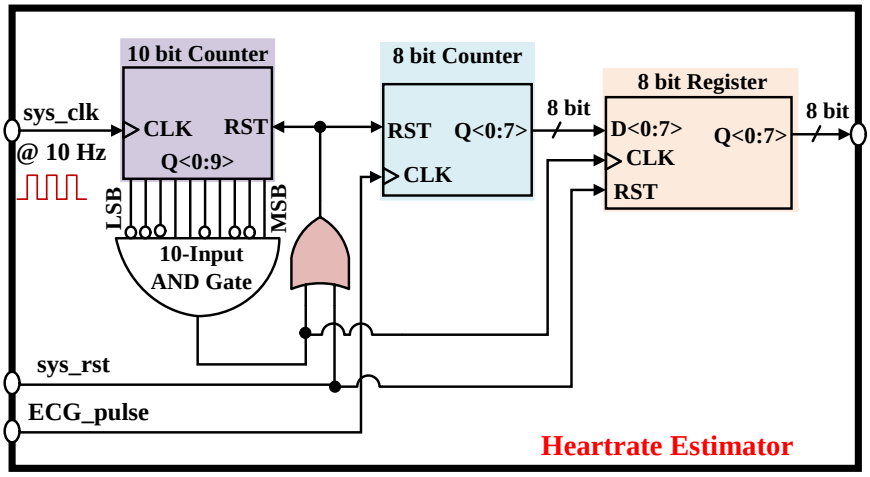
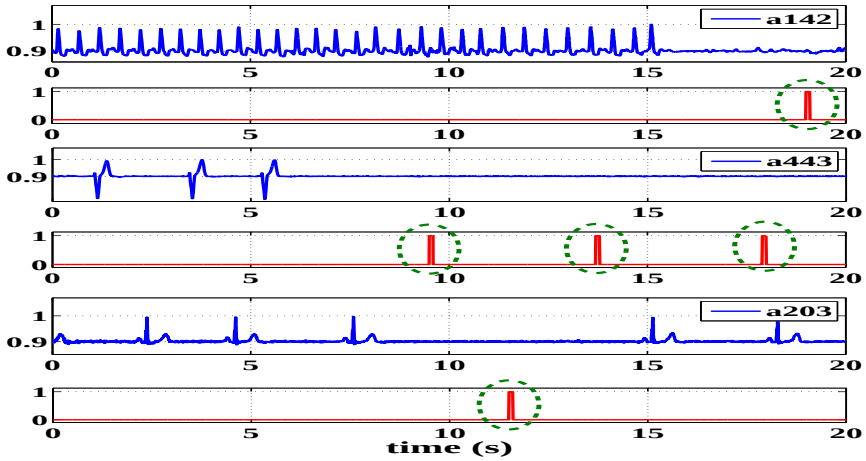


Figure 5.10: Heartrate estimator.

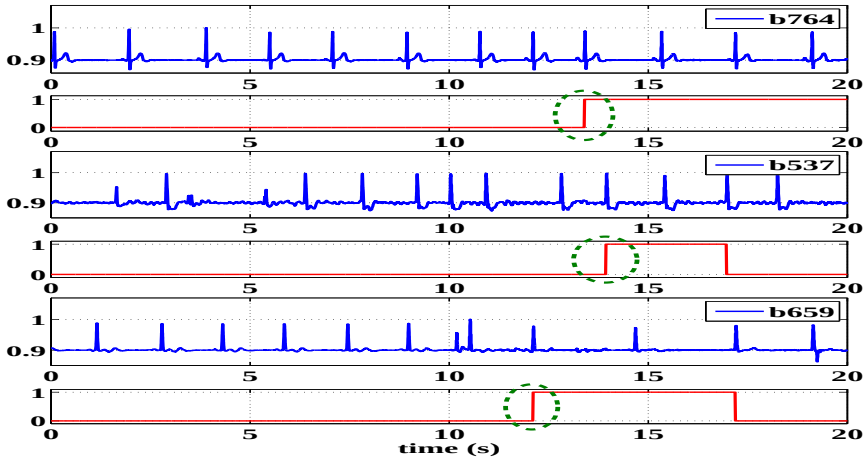
10-bit counter is non zero. This system outputs a valid count whenever the output of the 10 bit counter completes a count of $(600)_{10}$. This module consumes 40 nW of power.

5.3 Results and Discussion

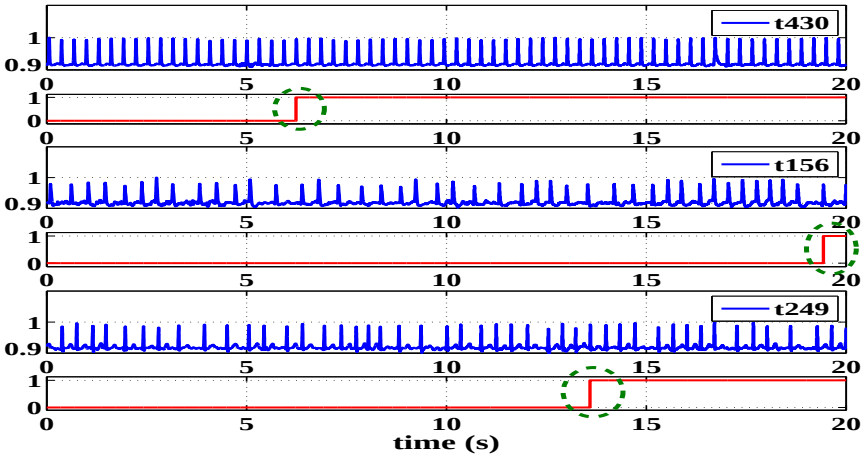
As already shown through Fig. 5.4, the proposed QRS detection circuit performs more accurately compared to the technique using a fixed threshold voltage. The QRS complex detection scheme, tested for ECG records from MITDB, exhibits a sensitivity and accuracy of 99.28% and 93.24% respectively. The proposed analog classification modules are verified and validated through the real ECG test signals taken from the '*PhysioNet/CinC Challenge 2015*' database [189]. Experimental results with test signals chosen for each of the target cardiac disorders show 95% accuracy of the proposed classifier, a performance which is almost at par with those reported in [188] and [192]. It is important to note that as in [69], the QRS detecting circuit here assumes that P/T -wave excursion are significantly lower than the R-peaks. Any P/T -wave with an amplitude greater than the threshold voltage would be identified as a R-peak. Also, a comparatively low accuracy of the classifier can be attributed to a large number of test cases resulting as 'False Negative' because the relevant 'count' obtained for the test data provided in [189] turns out to be very near but lesser than the chosen threshold. Nonetheless, it is essential to reiterate here that the this work focuses on including useful functionalities in the front-end with minimal hardware overhead and is intended for preliminary prognosis. The output waveforms for few test signals for true cases of asystole (*viz.* 'a142l', 'a443l' and 'a203l'), bradycardia (*viz.* 'b764l', 'b537l' and 'b659l') and tachycardia (*viz.*



(a) Asystole



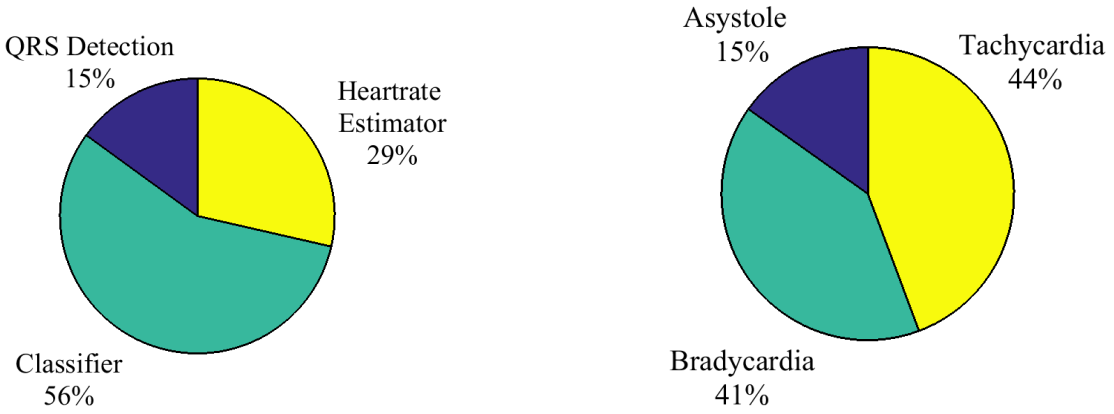
(b) Extreme bradycardia



(c) Extreme tachycardia

Figure 5.11: Output waveforms of the classifier for each of the target fatal cardiac disorders for different signals taken from [154].

't430l', 't156l' and 't249l') are shown in Fig. 5.11*a-c*. Note that the motive of these waveforms is solely to verify the functionality of the logic employed to detect the abnormalities, the absolute value of the amplitude of the input ECG and logical output of the classifier is inconsequential. Hence putting any label on the y-axis is skipped here, although all the amplitudes are voltages. The test signals and output of the corresponding abnormality detection circuits are represented in blue and red color, respectively. The waveforms show that the proposed scheme successfully detects the three target abnormalities.



(a) Full architecture (b) Classifier

Figure 5.12: Distribution of power consumption.

The complete architecture consumes 140 nW power with an area of 450 $\mu m \times 800$ μm in 0.18 μm CMOS. The results reported here are obtained through post-extracted simulations in Cadence Virtuoso. Further, this technique detects the QRS complexes while consuming only 21 nW power which is significantly lesser than the state-of-the-art DSP schemes with power consumption of tens of micro-watts or more. Within the classifier, the asystole, bradycardia and tachycardia modules consume 12 nW, 32 nW and 35 nW, respectively. The distribution of total power consumption is illustrated through pie charts in Fig. 5.12. Furthermore, this work can be considered as a proof-of-concept and the power consumption can be further reduced by designing the required gates using current starving technique, lower supply voltage,etc.

To prove the proposed concept, the architecture was verified in prototype mode (Fig. 5.13). It comprises of a mbed NXP LPC1768 board, a discrete board (with a peak detector built using IC 741 and resistors and capacitors, a buffer, a resistive voltage divider, and a comparator) and a FPGA board. The verification of the topology is done using the following steps (i) input to the peak detector is given though the DAC output pin of the mbed board (ii) a peak detector and pulse

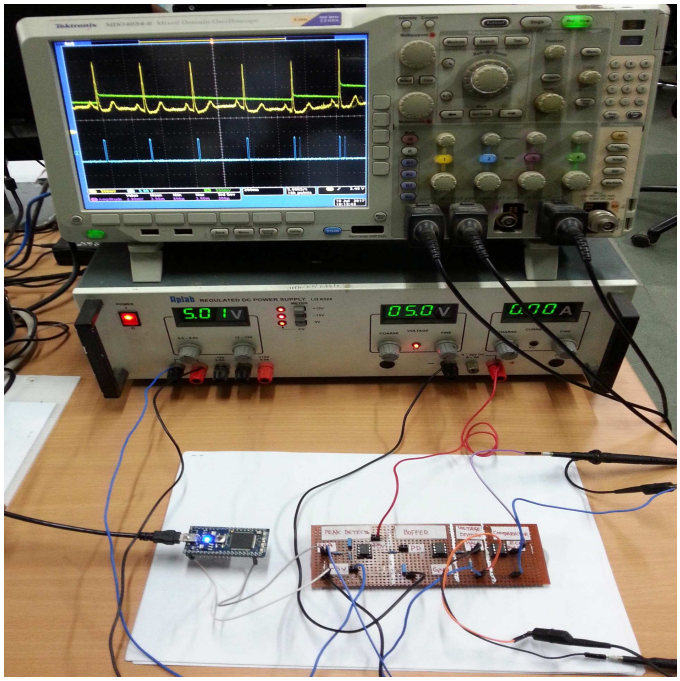


Figure 5.13: Verification set-up for testing the prototype QRS detector.

generation circuit built using discrete components detects the occurrence of a R-peak by generating a high pulse (iii) the pulses generated by the prototype is stored and fed to a FPGA, and (iv) the algorithms to detect asystole, extreme bradycardia and tachycardia are verified using the FPGA. As shown in Fig. 5.14, the output waveforms match those obtained through simulations in Cadence Virtuoso.

Table 5.2 compares the performances of few relevant state-of-the-art hardware implementations of the ECG classification schemes. Although the proposed topology lags behind in terms of accuracy *vis-à-vis* others, a stringent comparison would be unfair owing to their implementation using different technology node, supply voltages, power dissipation, usage of DSP, and most importantly the complexity of the algorithm involved. In a nutshell, the proposed classification scheme for the detection of fatal ECG abnormalities scores overs others as a viable solution with the following traits integrated together (i) fully analog implementation (ii) reasonably accurate QRS complex detection (iii) ultra low power dissipation, and (iv) clinically acceptable accuracy of the classification algorithm. All the above features make the proposed classification scheme suitable for portable long-term monitoring systems intended for preliminary diagnosis of fatal ECG disorders.

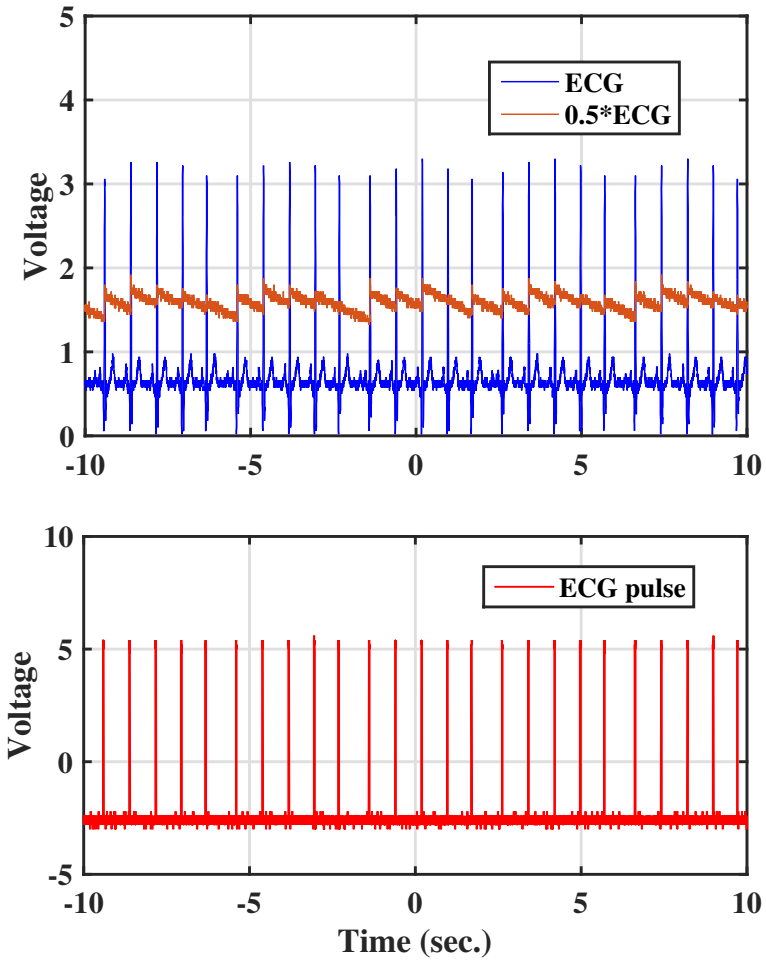


Figure 5.14: Verification of the QRS detection scheme through a prototype built using discrete components with regular ECG signal as input.

5.4 Summary

A low complexity ultra low power classifier for the detection of fatal ECG abnormalities is implemented on analog platform. Experimental results based on the test cases taken from the MITDB and [189], show that the both the autonomous QRS detection circuit and the classifier modules exhibit acceptable accuracies. The output waveforms show that the proposed scheme detects any event of the three target abnormalities successfully. This work aims to make important value additions to the standard ECG front-ends like [198], while incurring minimal additional power dissipation and hardware complexity. Hence this classifier presents a good trade-off between complexity, accuracy and power consumption, and will be more effective for long span continuous ECG monitoring rather than DSP based techniques. This classifier integrated with standard analog ECG acquisition systems, would aid preliminary prognosis of cardiac abnormalities, specially in remote monitoring

scenario.

Moreover, since the proposed methodology is first of its kind it can be considered a proof-of-concept, and the reader is free to extend the same to include the two alarm types (*viz.* ventricular tachycardia and flutter/fibrillation) left out here. Further, the system proposed here can be extended to include a module which can provide a count of number of heartbeats within a period of one minute (heart rate) and some critical statistical measures intended for R-R interval analysis (heart rate variability), *viz.* NN50 and pNN50, and at the same time are feasible to implement in fully in analog domain [199].

Table 5.2: Performance comparision with other hardware implemented ECG classification schemes

Ref.	**Technology**	V_{supply}	**Power**	**Classification Algorithm**	**Performance**	**Type**
[179]	0.065 μm CMOS	0.4 V (DSP)	45 nW (FDM) 92 nW (R-R) @ 10 kHz	Frequency Domain Metric (FDM) R-R algorithm	NA	SoC
[193]	0.13 μm CMOS	1.2 V	0.447 μW	Level-crossing sampling	BD: sensitivity→ 98.89%	ASIC
[194]	0.13 μm CMOS	1.2 V	43.7 nJ	Discrete wavelet transform (DWT)	CL : [a]TPR→0.93; [b]TNR→0.89	ASIC
[195]	0.18 μm CMOS	1.2 V	6 μW	4^{th}-order Haar wavelet-based DWT	BD : accuracy→99.44% CL : accuracy→97.25%	SoC
[196]	0.065 μm CMOS	0.7 V	0.11 mJ @ 7 kHz	Wavelet transform	BD: sensitivity →99.72% BD: positive prediction→99.49%	ASIC
[197]	0.065 μm CMOS	1 V	2.78 μW @ 10 kHz	QRS complex → [c]PAT Ventricular arrhythmia → naive Bayes	CL : accuracy→86%	ASIC
This work	0.18 μm CMOS	1.8 V	140 nW	QRS complex detection circuit Arithmetic counter based classification module	BD: TPR →99.28% , accuracy →93.24% CL: accuracy→95%	ASIC

[a]True positive rate, [b]True negative rate, [c]Pan and Tompkins algorithm, Beat detection → BD, Classification → CL

Chapter 6

Measurement Results and Comparison with State-of-the-art Implementations

6.1 Introduction

After verifying the modules in Chapter 3 and Chapter 4 through post-layout simulations, the designs are sent for fabrication. The details of the tape-out are discussed here. The measurement results are also provided. Finally, the comparison of the design implemented here with the existing state-of-the-art is also reported.

6.2 Tape-out - I

The first tape-out consisted of the following consists of three major blocks
(i) The ECG amplifier comprising the IA and the PGA (discussed in Chapter 3)
(ii) The AGC (discussed in Chapter 4)
(iii) The $\Sigma\Delta$ modulator ADC (discussed in Chapter 3)
The pin distribution was planned so as to allow the testing of all the three blocks combined as a system, as well as each of them individually. (Note that the block on the right corresponds to digital

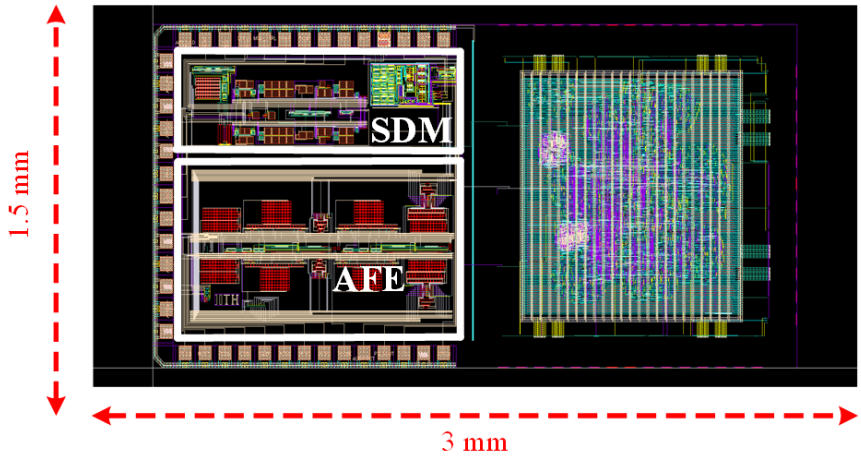


Figure 6.1: Signal conditioning done by the AFE.

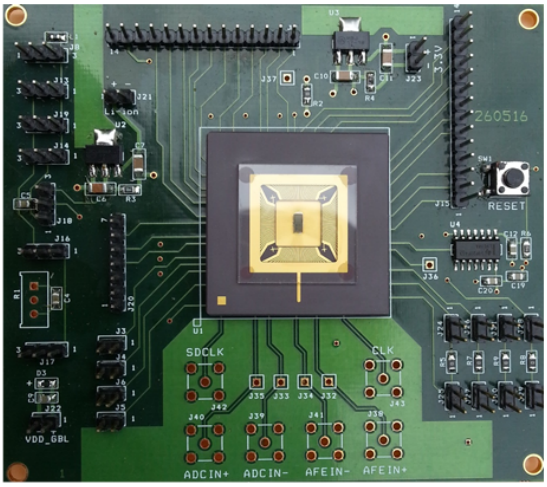


Figure 6.2: Signal conditioning done by the AFE.

implementation of decimation filter and ECG feature extraction and classification, which is not in the scope of this thesis).

6.2.1 Measured Results and Discussion

The measured results and analysis of the same is given here.

- **AFE** : The amplifier failed to perform as desired. Both the differential output nodes couldn't maintain the common mode voltage of 0.9 V. The output nodes showed no swing even when a sine wave was fed to the amplifier.
- **AGC** : It consists of a peak detector and a digital implementation of a gain capacitor select logic. The measurement result show that the output of the peak detector is fixed to a voltage

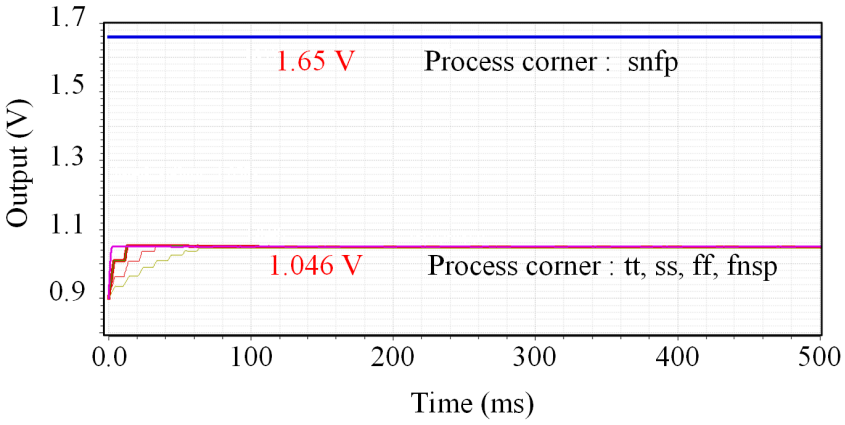


Figure 6.3: Signal conditioning done by the AFE.

of 1.65V, irrespective of the amplitude of the input signal. Since the peak detector is the first block of the AGC and it did not perform as desired, the subsequent blocks could not be tested. While debugging the reason for its failure, it was found that the opamp in the peak detector does fails in the SNFP process corner. The peak detector works as desired in rest of the corners. The peak detectors output for different corners are shown in Fig. 6.3.

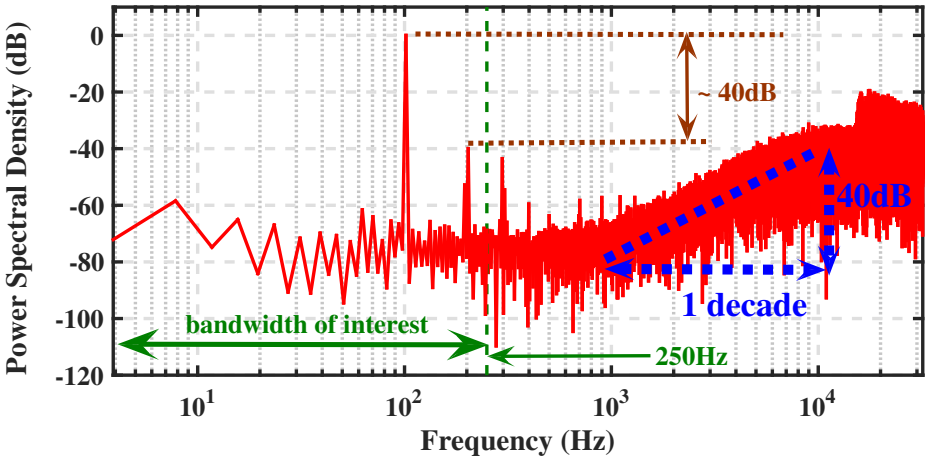


Figure 6.4: Signal conditioning done by the AFE.

- **ΣΔ ADC** : The measurement results show that the modulator works fine. The power spectral density plot of the output shows that the modulator achieves second order noise-shaping and a spurious-free dynamic range (SFDR) of 7 bits approximately. As discussed in Chapter 3, the post-layout extracted simulations of the same exhibit a SFDR of 10 bits. This reduction

in the obtained SFDR can be attributed to the following

- The affect of the mismatches on the design while using fixed external bias voltages.
- Unavailability of the necessary test equipment, e.g. in the absence of low-amplitude low-frequency generator with at least 70 dB linearity (a little more than the SFDR of the implemented ADC) the input to the ADC was given by generating the required differential voltages using MATLAB and applying to the input pads using 3.5 mm earphone jack. The noise introduced by the long wires and the breadboard involved are the most likely sources for degradation of the performance.

The following can be concluded from the above mentioned results:
(i) The failure of AFE and AGC can be attributed to the failure of the extracted design across all process corners.
(ii) The bias generation circuit should be included in the design. All the bias voltages were external for this tape-out.
(iii) Replica bias circuit should be designed to mitigate the variation of bias voltages across process corners.

6.3 Tape-out II

After locating the problems and their sources in the first tape-out, the necessary changes are made in the AFE and AGC and sent for fabrication again. Bias generation circuits for all the bias voltages required in the design are included on-chip. All the blocks are exhaustively verified across all process corners.

The second tape-out consisted of the following consists of three major blocks
(i) The ECG amplifier comprising the IA and the PGA (discussed in Chapter 3)
(ii) The AGC (discussed in Chapter 4)
(iii) The AFC (discussed in Chapter 4)
The pin distribution was planned so as to allow the testing of all the three blocks combined as a system, as well as each of them individually.

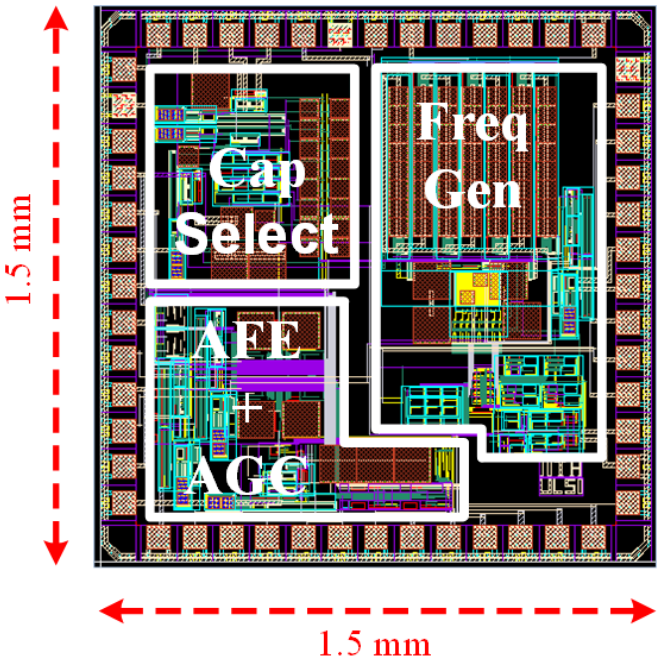


Figure 6.5: Signal conditioning done by the AFE.

6.3.1 Measured Results and Discussion

The measured results and analysis of the same is given here.

6.4 Summ Resultsary

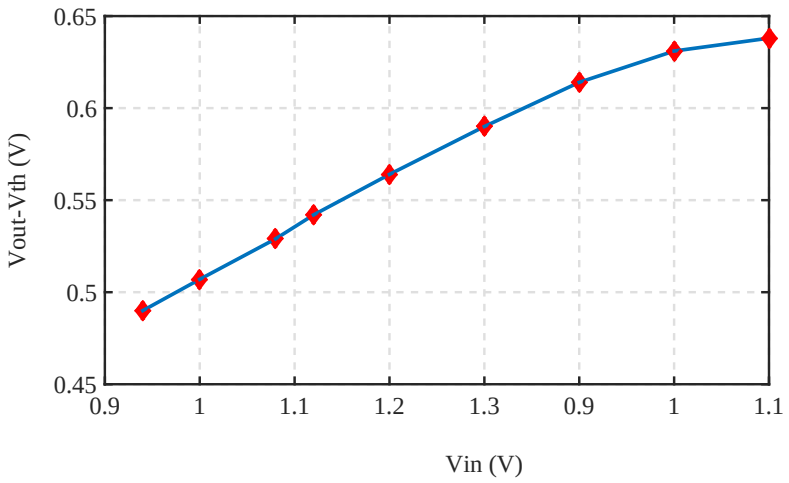


Figure 6.6: Signal conditioning done by the AFE.

Table 6.1: Comparison of the implemented ΣΔ ADC with the state-of-the-art

Parameter	**Value**				
	JETCAS '12 [81]	TIM '16 [113]	SPCAC '09 [96]	ICECS '05 [97]	**This work**
Technology (μm)	0.18	0.065	0.035	0.18	0.18
Voltage Supply (V)	1	1	1	3.3	1.8
Order	3rd	3rd	2nd	2nd	2nd
Bandwidth (Hz)	500	10k	781.25	10 k	250
Sampling Frequency (kHz)	32k	1.28M	100k	5120	64
Power Consumption (μW)	17.6	24.8	80	1630	5.0652
Dynamic Range (dB)	55.8	80.4	62	99	76 (post-ext) 40(measured)
FOM1 (pJ/Conv.)	34.9	0.1449	1.11	49.7702	1.9645 (post-ext) 124 (measured)

Table 6.2: Comparison of the implemented IA with the similar existing state-of-the-art designs - Part I

Parameter	**JSSC '07 [62]**	**JoS '13 [63]**	**TBCAS '10 [64]**	**ISSCC '10 [65]**	**JSSC '11 [66]**	**This work**
Technology (μm)	0.5	0.18	0.35	0.35	0.6	0.18
V_{supply} (V)	3	1.8	3	1	2.8	1.8
Gain (dB)	58.06-67.95	45	54-73	59-71	39.4	40-60
f_L (Hz)	EEG - 0.3 ECG - 0.3 EMG - 14	0.6	0.5-50	0.5	0.36	0.05
f_H (Hz)	EEG - 40 ECG-125 EMG-350	160	500-1000	150	1300	250
Power (μW)	60	1	12.75	0.385	2.4	0.47
Noise (μV_{RMS})	0.056-0.057	2.8	6.08	1.15	3.07	9.6
CMRR (dB)	> 120	–	60	83.2		120
THD @ 50 Hz	@ 5 mVp-p minimum gain 0.45-0.52%	–	–	<1% 0.9 Vp-p output swing		1% @ 2 mVp-p
NEF	9.2	3.4	5.5	2.24	3.09	16.0443
PEF	253.92	20.8	90.75	5.01	26.38	463.3533
Chopper	Yes	No	No	No	No	No
AGC	Ext. - cap. switch	No	Ext. - cap. switch	Ext. - cap. switch	No	Yes
AFC	Ext. - cap switch	No	Ext. - OTA bias current	HPF: pseudo-resistor LPF: cap switch	No	Yes
Architecture	AC coupled chopper IA	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback
Application	EEG EMG EMG	ECG	Neural	ECG	Neural	EMG

Table 6.3: Comparison of the implemented IA with the similar existing state-of-the-art designs - Part II

Parameter	**TBCAS '11 [67]**	**JSSC '09 [1]**	**TBCAS '12 [68]**	**TBCAS '15 [69]**	**TCAS '15 [70]**	**This work**
Technology (μm)	0.18	0.35	0.13	0.18	0.35	0.18
V_{supply} (V)	1.8	1	1	0.8	2.5	1.8
Gain (dB)	49-66	45.6-60	40	47-88	40.3	40-60
f_L (Hz)	0.13-350	4.5m-3.6	0.4	0.5	-	0.05
f_H (Hz)	293-12000	31-292	8.5k	22	0.1-10k	250
Power (μW)	5.4-20	0.033-0.337	12.5	51.2	-	0.47
Noise (μV_{RMS})	5.4-11.2	2.5 (0.05-460hz)	3.2	2.7	2.81	9.6
CMRR (dB)	62	¿71	¿60	66	¿82	120
THD @ 50 Hz	–	0.6% full swing	1.5% @ 1 mVp-p	–	0.1% 3.9-4.3 mV_{rms}	1% @ 2 mVp-p
NEF	4.4-5.9	3.26	4.5	5.6	1.88,1.93,2.05	16.0443
PEF	34.84-62.65	10.62	20.25	25.7		463.3533
Chopper	No	No	No	No	No	No
AGC	Ext. - cap switch	Ext. - cap switch	Ext. - cap switch	Ext. - cap switch	No	Yes
AFC AFC	Ext. - OTA I_{bias} Ext. - OTA Ibias	HPF: I_{bias} of PR LPF: OTA I_{bias}	HPF - bias of feedback LPF : OTA I_{bias}	No No	No No	Yes Yes
Architecture	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback	Capacitive feedback
Application	Neural	ECG	ECG, EEG, EMG	ECG	ECG, EMG	ECG

Chapter 7

Conclusion and Future Scope

7.1 Conclusion

This thesis presents the design a low power ECG front-end for the accurate acquisition and digitization of ECG signals. It also includes a low hardware complexity module for the preliminary prognosis of three life-threatening cardiac arrhythmia, viz. asystole, extreme bradycardia and tachycardia. The acquisition circuit consists of an IA with fixed gain, and a PGA whose gain is controlled using an efficient AGC mechanism. The topology of the overall amplifier also provides a $2^n d$ order bandpass filter characteristics. An AFT technique is introduced to minimize the process-dependent deviation of the low pass 3-dB frequency to prevent the occurrence of the aliasing of frequencies outside the bandwidth-of-interest into the bandwidth-of-interest. An opamp-shared $\Sigma\Delta$ modulator ADC is employed for digitizing the ECG signal. Finally a fully analog scheme is proposed for detecting the R-peaks of the ECG signal. Then a simple module for the classification of the arrhythmia mentioned above is included on the same analog platform. The major contributions here, i.e. AGC, AFT, QRS complex detector and arrhythmia classifier, are implemented while ensuring minimal power and hardware overhead to the overall ECG front-end. The relevant post-layout and measurement results are also given.

The measurement results show that peak detector of the AGC and the ring oscillator with digital correction in the AFT circuit functions as expected. The complete scheme involving the AGC and AFT working in tandem with the amplifier could not the tested because of the amplifier failed to function as desired. The functionality of the proposed QRS complex detector and classification module is verified in prototype mode. Output waveforms hence obtained match with those obtained

through simulations in Cadence Virtuoso.

The complete validation of the amplifier part using real-time ECG simulator is in process due to the unavailability of required testing facilities at present. Further, the debugging of the problems in the same through exhaustive testing is under way.

7.2 Future Scope

The proposed work in this thesis can be further carried out as follows:

- Exploration of the a novel IA topology and chopping technique to reduce the input referred noise.
- Design of a robust system, although at the cost of comparatively higher power consumption.
- Exploration of the scope of using the SAR ADC as an ultra low power substitution for the $\Sigma\Delta$ ADC used here. Investigation of simplistic techniques for resolution reconfigurability of the SAR ADC.
- Implementation of the controller module which controls the sequence in which each of the constituent blocks, i.e. amplifier, AGC, AFT, analog classifier, are activated and deactivated to save considerable start-up power consumption of the system.
- Integration of the proposed ECG front-end with additional energy harvesting modules to make the system suitable for batteryless IoT healthcare systems.
- Debugging the problem in the amplifier part through an ECG simulator.

Appendix A

Transfer Characteristics of an Capacitively-Coupled Capacitive-Feedback IA

A.1 Simplified Analysis

A simplified analysis of the capacitively-coupled capacitive-feedback IA shown in Fig. 2.4a is given below [122, 124]. The equivalent small signal model of the same is shown in Fig. A.1. The analysis

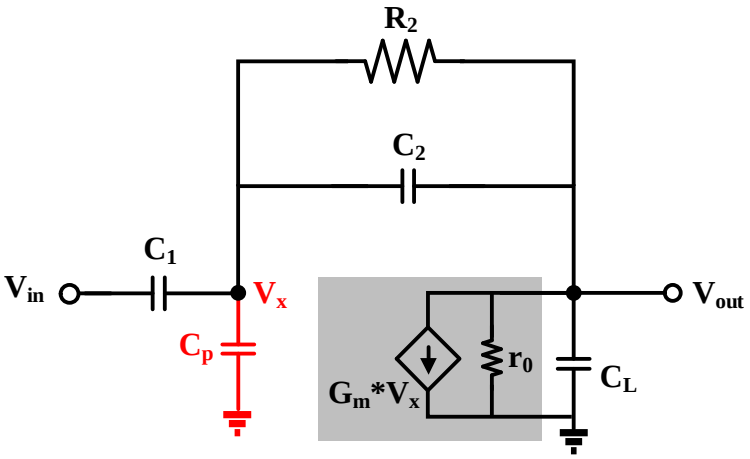


Figure A.1: Small signal model of the amplifier.

is summarized below.

- The small signal equivalent of the circuit is given in Fig. A.1. G_m represents the transconductance of the OTA; C_P represents the input capacitance of the OTA, any parasitic capacitance between node 'X' and ground and any bottom-plate capacitance from C_1 and C_2; r_0 output resistance of the OTA; C_1 is the input coupling capacitance; C_2 and R_2 are the feedback elements; C_L is the load capacitance.

- The transfer function of the configuration in Fig. A.1 can be obtained by formulating the following equation according to the KCL

$$\begin{aligned} v_X sC_P + (v_X - v_{in})sC_1 &= (v_{out} - v_X)\Big(\frac{1}{R_2} + sC_2\Big), \\ G_m v_X + v_{out}\Big(\frac{1}{r_0} + sC_L\Big) &= (v_X - v_{out})\Big(\frac{1}{R_2} + sC_2\Big). \end{aligned} \tag{A.1}$$

Solving the two equation A.1, the transfer function can be expressed as

$$\frac{v_{out}}{v_{in}} = \frac{sC_1\Big(sC_2 + \frac{1}{R_2} - G_m\Big)}{\Big[sc_1\Big(sC_2 + sC_L + \frac{1}{R_2} + \frac{1}{r_0}\Big) + sC_2\Big(sC_L + sC_P + G_m\Big) + sC_L\Big(sC_P + \frac{1}{R_2}\Big) + sC_P\Big(\frac{1}{R_2} + \frac{1}{r_0}\Big) + \frac{G_m}{R_2}\Big]} \tag{A.2}$$

Equation A.2 indicates that the system has two poles and zeros. The numerator reveals the following zeros

$$z_1 = 0; \quad z_2 = \frac{\Big(G_m - \frac{1}{R_2}\Big)}{C_2} \tag{A.3}$$

Assuming that $G_m > \frac{1}{r_0} > \frac{1}{R_2}$, and $1 \ll R_2$, the denominator of equation A.2 can be simplified as

$$\frac{s^2\Big[C_1(C_2 + C_L) + C_2(C_L + C_P) + C_L C_P\Big]}{\Big(\frac{G_m}{R_2}\Big)} + \frac{sC_2 G_m}{\Big(\frac{G_m}{R_2}\Big)} + 1 = 0 \tag{A.4}$$

The poles of the system are given by

$$p_1 = -\frac{1}{R_2 C_2}; \quad p_2 = -\frac{G_m}{\Big(\frac{C_1}{C_2}\Big)(C_2 + C_L) + C_L + C_P + \frac{C_L C_P}{C_2}} \tag{A.5}$$

The above equation can be presented in to a more compact and informative form as

$$\frac{v_{out}}{v_{in}} = K_{mid} \quad \frac{1-\frac{s}{2\pi f_z}}{\left(\frac{2\pi f_L}{s}+1\right)\left(\frac{s}{2\pi f_H}+1\right)}, \qquad where$$
$$K_{mid} = \frac{C_1}{C_2}; \quad f_L = \frac{1}{2\pi R_2 C_2}; \quad f_H = \frac{G_m}{2\pi C_L K_{mid}}; \quad f_Z = f_H \frac{C_1 C_L}{C_2^2}. \tag{A.6}$$

The bode plot of this transfer function is illustrated in Fig. A.2. The figure shows that a bandpass filter characteristics is obtained from the circuit in Fig. 2.4a [122].

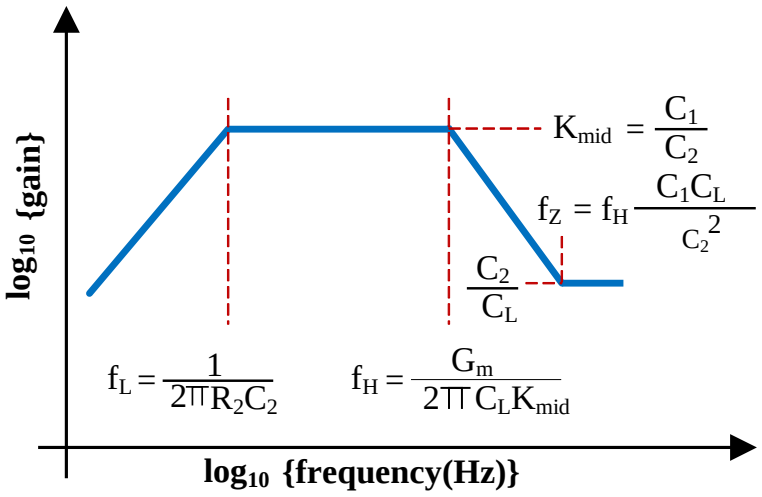


Figure A.2: The log-log plot of the gain *vs.* frequency for the amplifier.

Appendix B

Noise Analysis of the RFC OTA Used in the Design of IA

B.1 Introduction

The aim of this qualitative noise analysis is to derive an expression for the overall noise generated due to all the transistors comprising the OTA, which lays down the guidelines while sizing the individual devices so as to minimize the noise at the output nodes. Since the bandwidth considered is low, flicker noise dominates the overall noise distribution. Hence only flicker noise is considered here. The schematic diagram of the RFC OTA used to implement the IA is shown in Fig. B.1, along with the bias voltages and currents. Note that while designing the OTA, the following criteria is fulfilled.

$$g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m9} = g_{m10} = g_m \tag{B.1}$$

A qualitative analysis of the contributed by each device of the OTA to the overall input referred noise is given here. Since the bandwidth considered is low, flicker noise dominates the overall noise distribution.

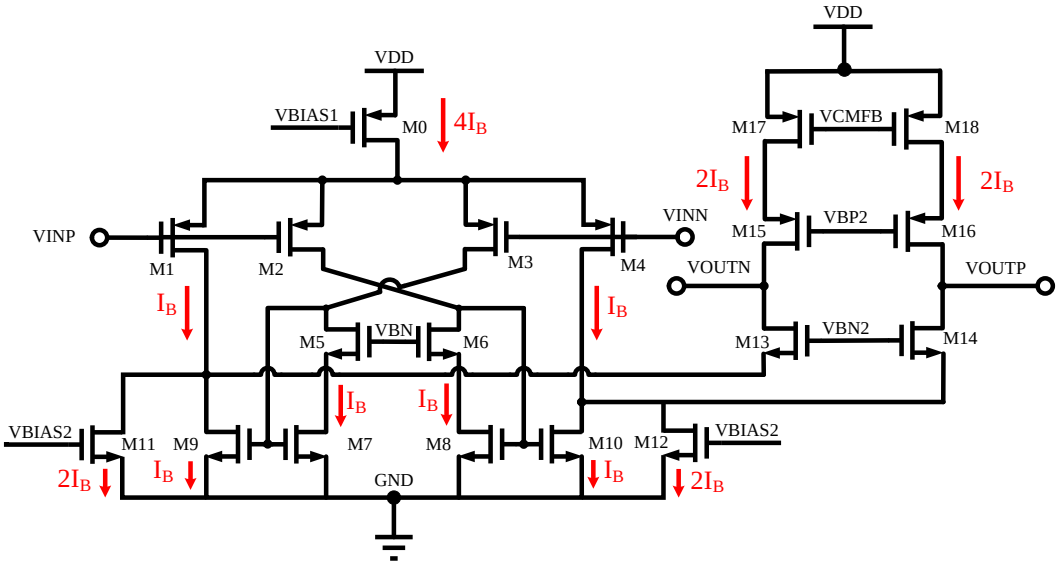


Figure B.1: Schematic diagram of the RFC OTA.

B.2 Qualitaive Noise Analysis

The noise current of M0 is distributed in M1, M2, M3 and M4. Hence the output generated due to it is equal on both the output nodes, resulting in zero differential output. Therefore, the transistor M0 has no contribution to the overall noise.

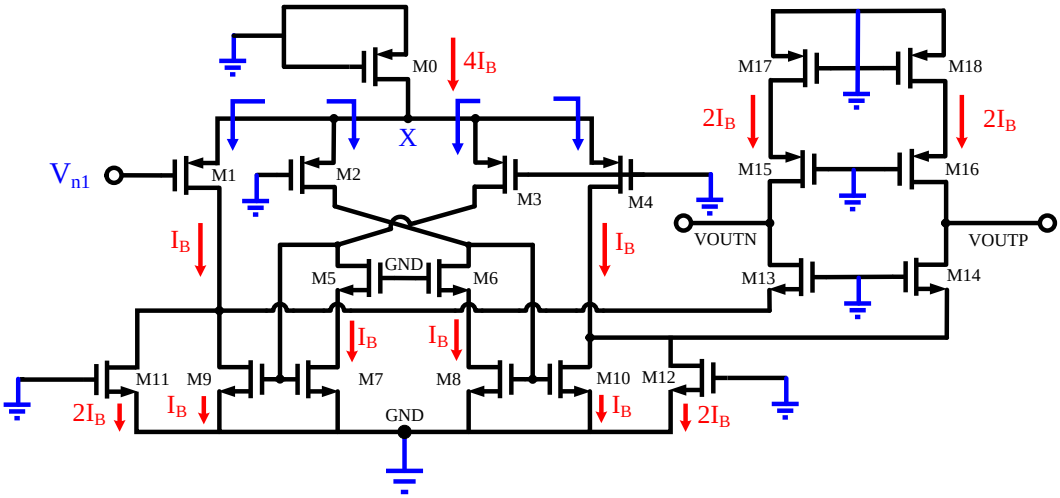


Figure B.2: Analytical schematic diagram of the RFC OTA while considering the noise of input transistor M1.

Next, the noise contributed by the input transistors are analyzed. The analysis for the other transistors are simple and are compiled at the end.

B.2.1 Noise Generated by the Input Transistors

The analysis is started by trying to estimate the noise at the node $VOUTM$ due to the input transistor M1. As shown in Fig. B.2, the flicker noise of M1 is represented by the noise source V_{n1} and the gates of all other devices are grounded.

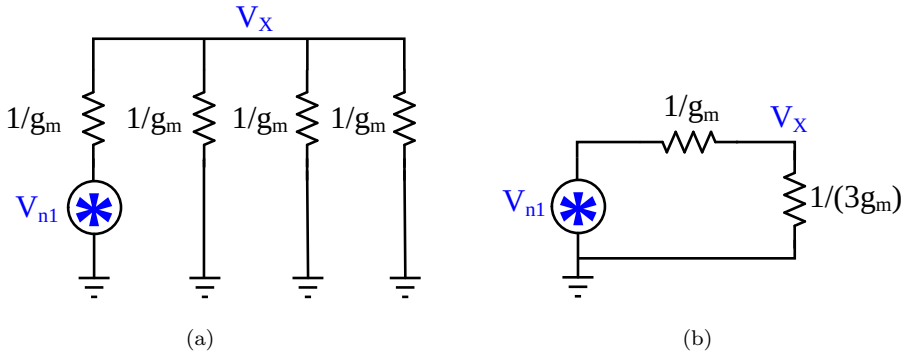


Figure B.3: (a) Thevenin equivalent resistance and voltage at node 'X', (b) Reduced equivalent circuit to determine voltage at node 'X'.

- First, let us consider the equivalent Thevenin voltage and resistance at node 'X' due to the noise source V_{n1} at the gate of M1. Fig. B.3 shows the Thevenin equivalent resistance looking into the sources of M1, M2, M3 and M4, with noise source voltage V_{n1}. It is evident from Fig. B.3b V_X turns out to be $\frac{V_{n1}}{4}$.

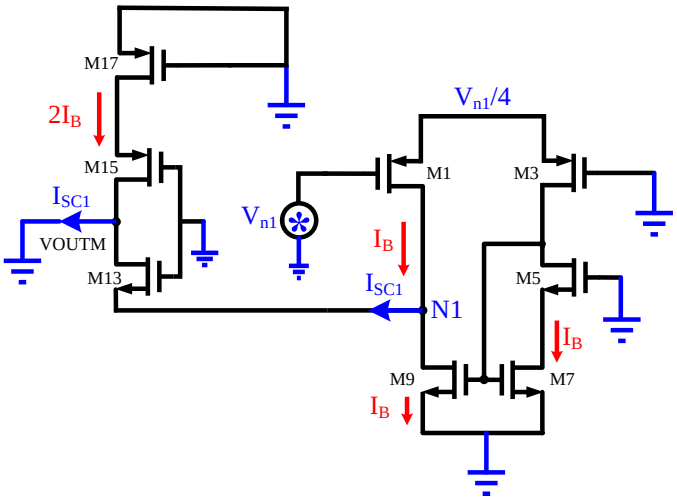
- To make the analysis simpler, the circuit in Fig. B.2 is divided in two halves. One half is shown in Fig. B.4.

- First, the short circuit current I_{SC1} at node $VOUTM$ due to V_{n1} noise source, corresponding to M1, is calculated. Note that this I_{SC1} is same as that coming out of node $N1$. An equivalent small signal model of this half is given in Fig. B.4b and is used to I_{SC1} at node $N1$. This current I_{SC1} is expressed as

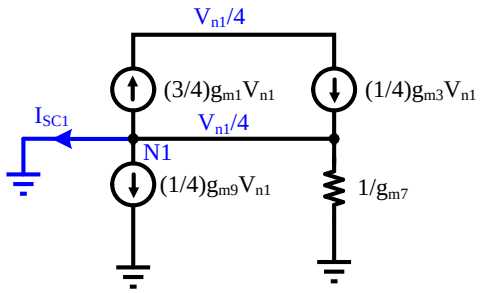
$$I_{SC1} = -\left(\frac{3}{4}g_{m1}V_{n1} + \frac{1}{4}g_{m9}V_{n1}\right) = -g_m V_{n1} \tag{B.2}$$

- Similarly, the other half is given in Fig. B.5a. Again, calculating the short circuit current I_{SC2} at node $N2$ due to V_{n1} noise source is given by

$$I_{SC2} = \left(\frac{1}{4}g_{m4}V_{n1} - \frac{1}{4}g_{m10}V_{n1}\right) = 0 \tag{B.3}$$



(a)



(b)

Figure B.4: (a) Simplified circuit of the first half, (b) small signal equivalent of the same with the noise source of M1.

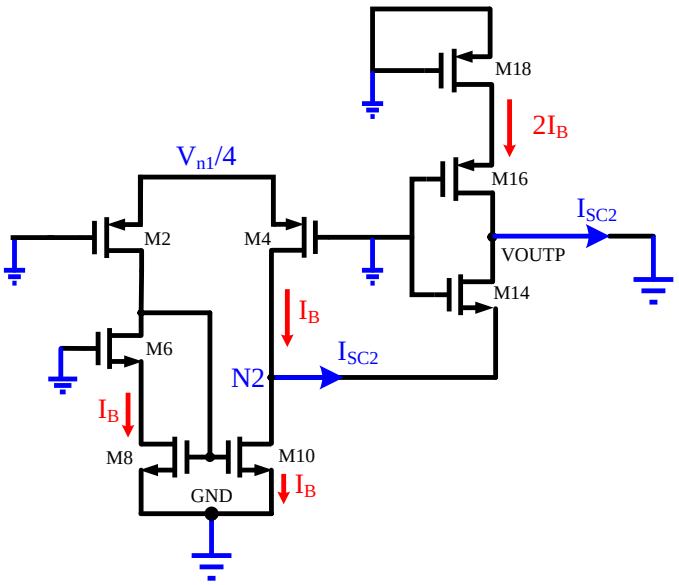
- It is evident from equation B.2 and equation B.3 that the noise due to V_{n1} (corresponding to M1) generates noise only at node $N1$, or node $VOUTM$.

- The noise generated at nodes $VOUTM$ and $VOUTP$ (or $N1$ and $N2$) by the noise of M2 is calculated following the same procedure as above. The first half of the simplified circuit is given in Fig. B.6a.

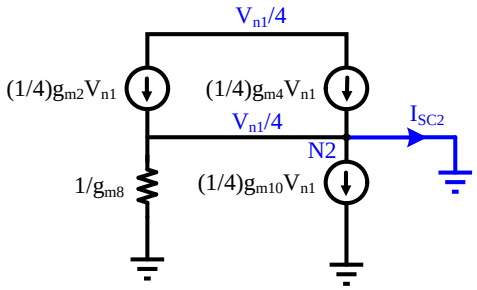
- Using the equivalent small signal model of Fig. B.6b the I_{SC2} due to M2 is given by

$$I_{SC2} = \left(\frac{1}{4}g_{m4}V_{n1} + \frac{3}{4}g_{m10}V_{n1}\right) = g_m V_{n1} \tag{B.4}$$

- The schematic of the second half and its equivalent small signal model is given in Fig. B.7.



(a)



(b)

Figure B.5: (a) Simplified circuit of the second half, (b) small signal equivalent of the same with the noise source of M1.

The noise current I_{SC1} due to V_{n2} is expressed as

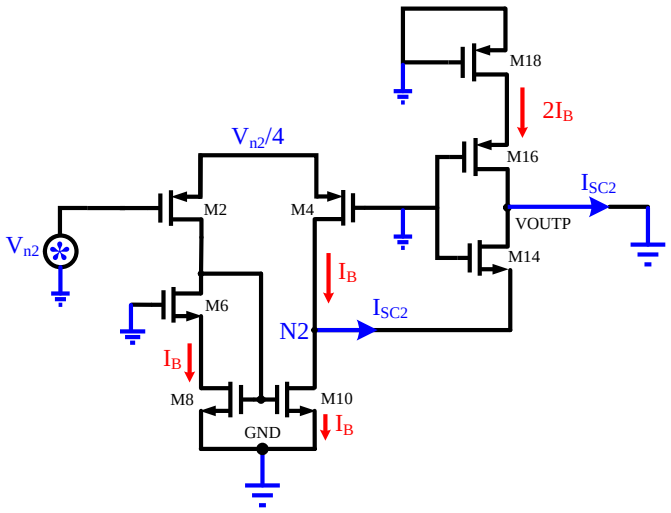
$$I_{SC1} = \left(\frac{1}{4}g_{m1}V_{n1} - \frac{1}{4}g_{m9}V_{n1}\right) = 0 \tag{B.5}$$

- It is evident from equation B.4 and equation B.5 that the noise due to V_{n2} (corresponding to M2) generates noise only at node $N2$, or node $VOUTP$.
- The noise current generated by M3 and M4 can be analyzed similar to M2 and M1, respectively.

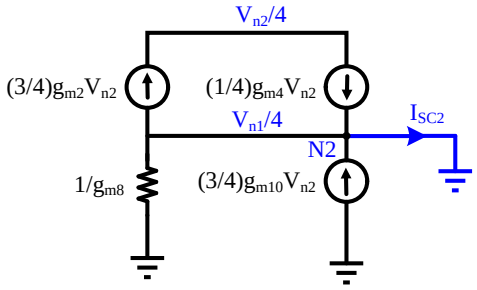
B.2.2 Overall Noise Analysis

The overall noise generated by all the transistors is considered here.

- First, the noise generated at node $VOUTM$ (or node $N1$) due to all the contributing transistors



(a)



(b)

Figure B.6: (a) Simplified circuit of the first half, (b) small signal equivalent of the same with the noise source of M2.

are given by the following equations. Note that the noise power generated by M1 at node $N1$ is $\overline{V_{n1,N1}^2}$, and so on. Also equation B.1 is used to simplify expression wherever required and R_{out} represents the output impedance of the OTA.

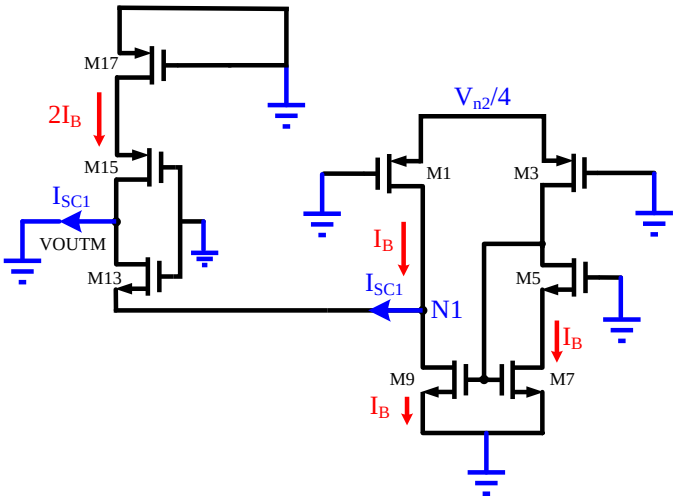
$$\overline{V_{n1,N1}^2} = \frac{K_p}{\mu_p C_{ox} W_1 L_1 f} * (\frac{3g_{m1}}{4} + \frac{g_{m9}}{4})^2 * R_{out}^2 = \frac{K_p}{\mu_p C_{ox} W_1 L_1 f} * g_m^2 * R_{out}^2 \tag{B.6}$$

$$\overline{V_{n3,N1}^2} = \frac{K_p}{\mu_p C_{ox} W_3 L_3 f} * (\frac{3g_{m9}}{4} + \frac{g_{m1}}{4})^2 * R_{out}^2 = \frac{K_p}{\mu_p C_{ox} W_3 L_3 f} * g_m^2 * R_{out}^2 \tag{B.7}$$

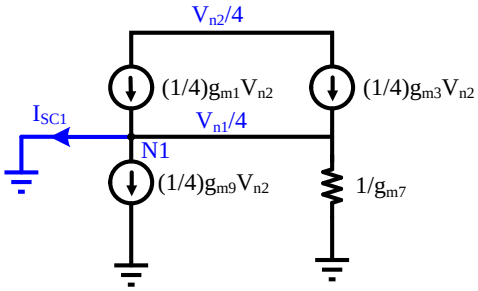
$$\overline{V_{n17,N1}^2} = \frac{K_p}{\mu_p C_{ox} W_{17} L_{17} f} * (g_{m17})^2 * R_{out}^2 \tag{B.8}$$

$$\overline{V_{n9,N1}^2} = \frac{K_n}{\mu_n C_{ox} W_9 L_9 f} * (g_{m9})^2 * R_{out}^2 = \frac{K_n}{\mu_n C_{ox} W_9 L_9 f} * (g_m)^2 * R_{out}^2 \tag{B.9}$$

$$\overline{V_{n7,N1}^2} = \frac{K_n}{\mu_n C_{ox} W_7 L_7 f} * (g_{m9})^2 * R_{out}^2 = \frac{K_n}{\mu_n C_{ox} W_7 L_7 f} * (g_m)^2 * R_{out}^2 \tag{B.10}$$



(a)



(b)

Figure B.7: (a) Simplified circuit of the second half, (b) small signal equivalent of the same with the noise source of M2.

$$\overline{V_{n11,N1}^2} = \frac{K_n}{\mu_n C_{ox} W_{11} L_{11} f} * (g_{m11})^2 * R_{out}^2 \tag{B.11}$$

- The gain of the OTA is equal to $(2 * g_m * R_{out})$.
- Each of the output noise powers is input referred by dividing the corresponding equations by the gain of the OTA. The input referred noise powers are expressed by the following equations.

$$\overline{V_{in1,N1}^2} = \frac{1}{4} \frac{K_p}{\mu_p C_{ox} W_1 L_1 f} \tag{B.12}$$

$$\overline{V_{in3,N1}^2} = \frac{1}{4} \frac{K_p}{\mu_p C_{ox} W_3 L_3 f} \tag{B.13}$$

$$\overline{V_{in17,N1}^2} = \frac{K_p}{\mu_p C_{ox} W_{17} L_{17} f} * \left(\frac{g_{m17}}{2 g_{m1}}\right)^2 \tag{B.14}$$

$$\overline{V_{in9,N1}^2} = \frac{1}{4} \frac{K_n}{\mu_n C_{ox} W_9 L_9 f} \tag{B.15}$$

$$\overline{V_{in7,N1}^2} = \frac{1}{4}\frac{K_n}{\mu_n C_{ox} W_7 L_7 f} \tag{B.16}$$

$$\overline{V_{in11,N1}^2} = \frac{K_n}{\mu_n C_{ox} W_{11} L_{11} f} * \left(\frac{g_{m11}}{2g_{m1}}\right)^2 \tag{B.17}$$

- The transconductance of a given transistor for a bias current of I_D is given by

$$g_m = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_D} \tag{B.18}$$

Using this expression the second terms in equation B.14 and equation B.17 is simplified as follows

$$\left(\frac{g_{m17}}{2g_{m1}}\right)^2 = \frac{\mu_p C_{ox}\left(\frac{W_{17}}{L_{17}}\right) 2I_B}{4 * \mu_p C_{ox}\left(\frac{W_1}{L_1}\right) I_B} = \frac{1}{2}\frac{W_{17} L_1}{W_1 L_{17}} \tag{B.19}$$

$$\left(\frac{g_{m11}}{2g_{m1}}\right)^2 = \frac{\mu_n C_{ox}\left(\frac{W_{11}}{L_{11}}\right) 2I_B}{4 * \mu_p C_{ox}\left(\frac{W_1}{L_1}\right) I_B} = \frac{1}{2}\frac{\mu_n W_{11} L_1}{\mu_p W_1 L_{11}} \tag{B.20}$$

- The expressions obtained in equation B.19 and equation B.20 are substituted into equation B.14 and equation B.17.

- The total input referred flicker noise at node $VOUTM$ is expressed as follows

$$\begin{aligned}\overline{V_{in,tot,N1}^2} = &\frac{1}{4}\frac{K_p}{\mu_p C_{ox} W_1 L_1 f} + \frac{1}{4}\frac{K_p}{\mu_p C_{ox} W_3 L_3 f} + \frac{1}{4}\frac{K_n}{\mu_n C_{ox} W_7 L_7 f} + \frac{1}{4}\frac{K_n}{\mu_n C_{ox} W_9 L_9 f} \\ &+ \frac{K_p}{\mu_p C_{ox} W_{17} L_{17} f}\frac{1}{2}\frac{W_{17} L_1}{W_1 L_{17}} + \frac{K_n}{\mu_n C_{ox} W_{11} L_{11} f}\frac{1}{2}\frac{\mu_n W_{11} L_1}{\mu_p W_1 L_{11}}\end{aligned} \tag{B.21}$$

This expression is further simplified as

$$\overline{V_{in,tot,N1}^2} = \frac{K_p}{\mu_p C_{ox} W_1 L_1 f}\left[\frac{1}{4} + \frac{1}{4} + \frac{1}{4}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_7 L_7} + \frac{1}{4}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_9 L_9} + \frac{1}{2}(\frac{L_1}{L_{17}})^2 + \frac{1}{2}\frac{K_n}{K_p}(\frac{L_1}{L_{11}})^2\right] \tag{B.22}$$

- Similar noise is generated by the corresponding counterparts at node $VOUTP$ due to symmetricity.

- The total input referred flicker noise is obtained by adding the noise powers generated at nodes

$VOUTM$ and $VOUTP$. The total power is given by

$$\overline{V_{in,tot}^2} = \frac{K_p}{\mu_p C_{ox} W_1 L_1 f}\left[\frac{1}{2}+\frac{1}{2}+\frac{1}{2}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_7 L_7}+\frac{1}{2}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_9 L_9}+(\frac{L_1}{L_{17}})^2+\frac{K_n}{K_p}(\frac{L_1}{L_{11}})^2\right] \tag{B.23}$$

This expression is further simplified as

$$\overline{V_{in,tot}^2} = \frac{K_p}{\mu_p C_{ox} W_1 L_1 f}\left[1+\frac{1}{2}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_7 L_7}+\frac{1}{2}\frac{\mu_p K_n W_1 L_1}{\mu_n K_p W_9 L_9}+(\frac{L_1}{L_{17}})^2+\frac{K_n}{K_p}(\frac{L_1}{L_{11}})^2\right] \tag{B.24}$$

Appendix C

Modeling an Ideal ΣΔ ADC Using Verilog-A

C.1 Introduction

The ideal first order and second order 1-bit ΣΔ ADC is modeled to understand the functionality of the same. The procedure to model and test the ΣΔ ADC is given below:

- Capture the behavior of the ΣΔ ADC using Verilog-A and save using the extension $< myfile.va >$
- Import the same in Cadence Virtuoso and create a symbol of the same
- Prepare a testbench in 'config' view
- Simulate using the 'ams' simulator
- Ensure that the frequency of the sine wave voltage source is provided in a format that satisfies the criteria of coherent sampling [200] and the amplitude is less than the reference voltage fedback from the DAC.

The verilog-a code used to model and the appropriate testbench is given below. (The code is adopted from [201] and Internet).

Verilog-A Model of the First Order 1-bit ΣΔ ADC

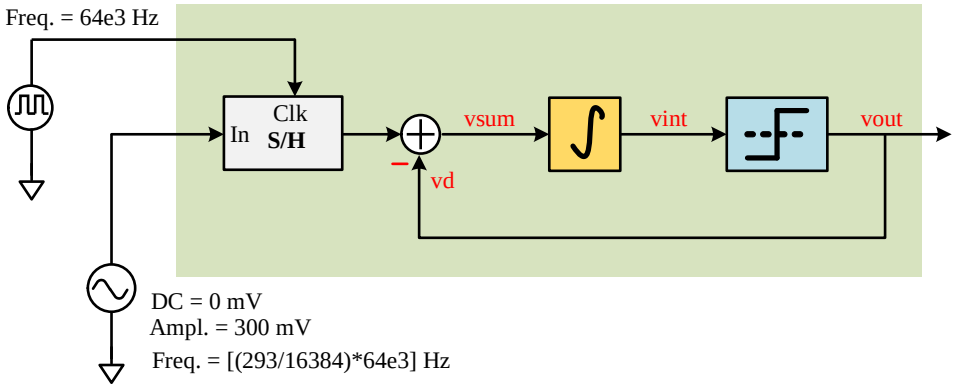


Figure C.1: Symbol for the first order 1-bit ΣΔ ADC.

```
‘include ”constants.vams”
‘include ”disciplines.vams”
module sdm_first_order(in,clk,out);
  input in,clk;
  output out;
  voltage in,clk,out;
  parameter real quantizer_vth=0.0;
  parameter real clk_vth=0.9;
  parameter real d2a_gain=1.8;
  real vsum;
  real vd;
  real vint;
  real vout;
  real hi,lo;
  analog
  begin
   @(initial_step)
   begin
    vd=0;vint=0;vout=0;
     hi = 1; lo = -1;
    end
    @(cross(V(clk) - clk_vth,1))
    begin
  // summing junction
     vsum = V(in) - vd ;
  // integrator
     vint = vint + vsum;
  // quantizer
     if (vint > quantizer_vth) vout = hi ;
     else vout = lo ;
  // D to A
     vd = d2a_gain*vout ;
    end
    V(out) <+ vout ;
  end
endmodule
```

Figure C.2: Verilog-A code to model a first order 1-bit ΣΔ ADC.

Verilog-A Model of the Second Order 1-bit ΣΔ ADC

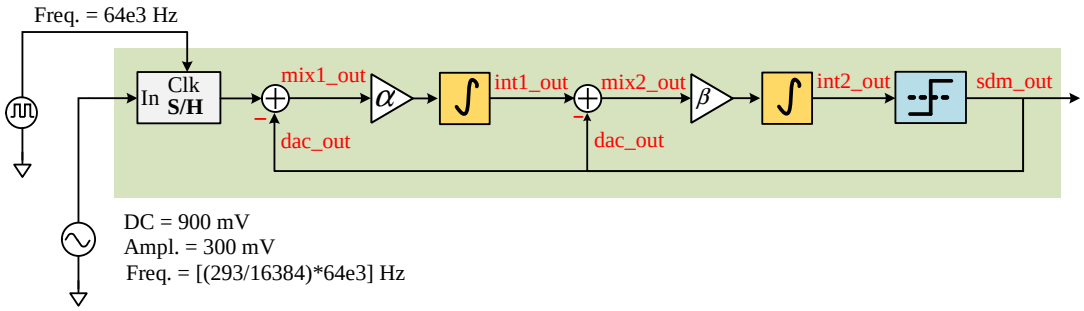


Figure C.3: Symbol for the second order 1-bit ΣΔ ADC.

```
‘include ”constants.vams”
‘include ”disciplines.vams”
module sdm(in,clk,out);
  input in,clk;
  output out;
  voltage in,clk,out;
  parameter real clk_vth=0.9;
  parameter alpha = 0.5;
  parameter beta = 2;
  parameter vdac = 0.5;
  parameter vdd = 1.8;
  parameter vss = 0;
  parameter vcm = 0.9;
  real int1_out;
  real int2_out;
  real dac_out;
  real mix1_out;
  real mix2_out;
  real t_int1_out;
  real t_int2_out;
  real sdm_out;
  analog
  begin
   @(initial_step)
   begin
    int1_out = 0.0 ;
    int2_out = 0.0 ;
    dac_out = 0.0 ;
    mix1_out = 0.0 ;
    mix2_out = 0.0 ;
    sdm_out = 0 ;
    t_int2_out = 0 ;
    t_int1_out = 0 ;
   end
   @(cross(V(clk) - clk_vth,1))
   begin
    mix2_out = int1_out - dac_out ;
    int2_out = t_int2_out + beta*mix2_out ;
    t_int2_out = int2_out ;
    mix1_out = V(in) - dac_out ;
    int1_out = t_int1_out + alpha*mix1_out ;
    t_int1_out = int1_out ;
     if (int2_out >= 0.0) sdm_out = vdd ;
     else sdm_out = vss ;
    if (sdm_out == 0) dac_out = vcm-vdac ;
    else dac_out = vcm+vdac ;
   end
   V(out) <+ sdm_out ;
  end
endmodule
```

Figure C.4: Verilog-A code to model a second order 1-bit ΣΔ ADC.

Appendix D

Development of MATLAB based GUIs to Facilitate the Preliminary Design of ΣΔ ADC

D.1 Introduction

SIMULINK has been the most potent and popular tool for modeling ΣΔ ADC and its circuit non-idealities. A lucid explanation of the working principle, modeling and circuit design is given in [151,202]. Moreover, Richard Schreier's toolbox 'delsig' and 'SIMSIDES' are very popular MATLAB based toolboxes for high-level design and simulation of ΣΔ modulators [203, 204]. SIMULINK based models are useful for estimating the effect of the different circuit non-idealities on the overall performance of the modulator's output. An excellent discourse on modeling these non-idealities is given in [205]. The example SIMULINK models and other related MATLAB codes used to explain the concepts in [205] are also freely available in [206]. Further, the procedure to model these non-idealities has been extensively reported in various papers too [207–211]. Many ready-to-use SIMULINK based models are also available on the Internet [212–215]. These SIMULINK models can further be refined and organized in the form of a graphical user interface (GUI). The development of such GUIs which help in the preliminary high-level design of ΣΔ modulator ADC is discussed in detail here.

D.2 Linearized Analysis of a Second Order ΣΔ ADC

The linear representation of a second order ΣΔ modulator ADC is shown in Fig. D.1a. Different error sources, or, non-idealities at each node is shown explicitly in the same figure as $N_1(z)$, $N_2(z)$, $N_3(z)$ and $N_4(z)$. $H_1(z)$ and $H_2(z)$ are defined as in equation D.1. The transfer function of the modulator output $Q(z)$ w.r.t the input signal $P(z)$ and noises $N_1(z)$, $N_2(z)$, $N_3(z)$ and $N_4(z)$ are specified in equations D.2-D.6 [209]. The magnitude plots of each of the transfer functions is plotted in Fig. D.1b. The plots clearly show that noise shaping increases from $N_1(z)$ to $N_2(z)$ to $N_3(z)$, which implies that the in-band power of a source of error in the forward path of the loop will decrease with an increase in the proximity of the source and quantizer. Moreover, since the error in the feedback path $N_4(z)$, is added directly to the input, it passes on to the output of the modulator without any shaping. The performance degradation due to component mismatch in the DAC corresponds to $N_4(z)$ here. Therefore the overall accuracy of the modulator is no better than that of the feedback DAC [216].

$$H_1(z) = 0.5 * \frac{z^{-1}}{1 - z^{-1}} \quad ; \quad H_2(z) = 2 * \frac{z^{-1}}{1 - z^{-1}} \tag{D.1}$$

$$STF(z) = \frac{Q(z)}{P(z)} = \frac{H_1(z)H_2(z)}{1 + H_1(z)H_2(z) + H_2(z)} = z^{-2} \tag{D.2}$$

$$NTF_1(z) = \frac{Q(z)}{N_1(z)} = \frac{H_1(z)H_2(z)}{1 + H_1(z)H_2(z) + H_2(z)} = z^{-2} \tag{D.3}$$

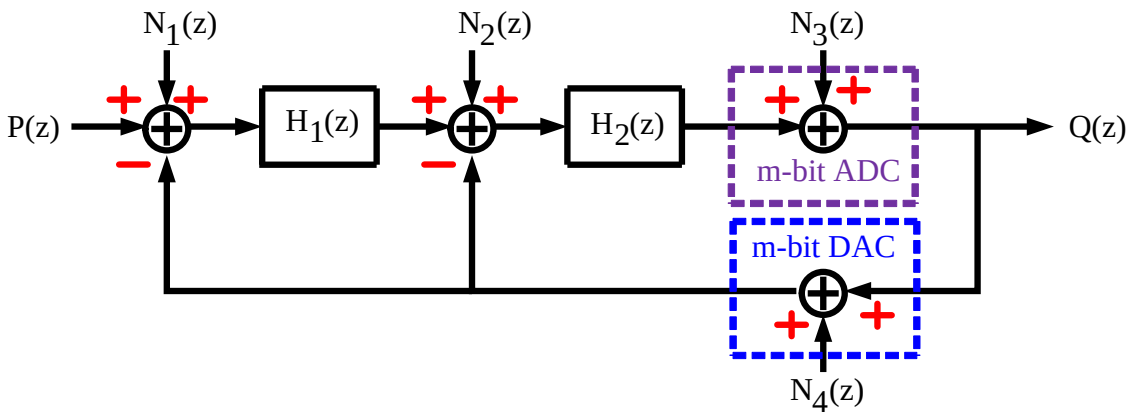
$$NTF_2(z) = \frac{Q(z)}{N_2(z)} = \frac{H_2(z)}{1 + H_1(z)H_2(z) + H_2(z)} = 2 * z^{-1} * (1 - z^{-1}) \tag{D.4}$$

$$NTF_3(z) = \frac{Q(z)}{N_3(z)} = \frac{1}{1 + H_1(z)H_2(z) + H_2(z)} = (1 - z^{-1})^2 \tag{D.5}$$

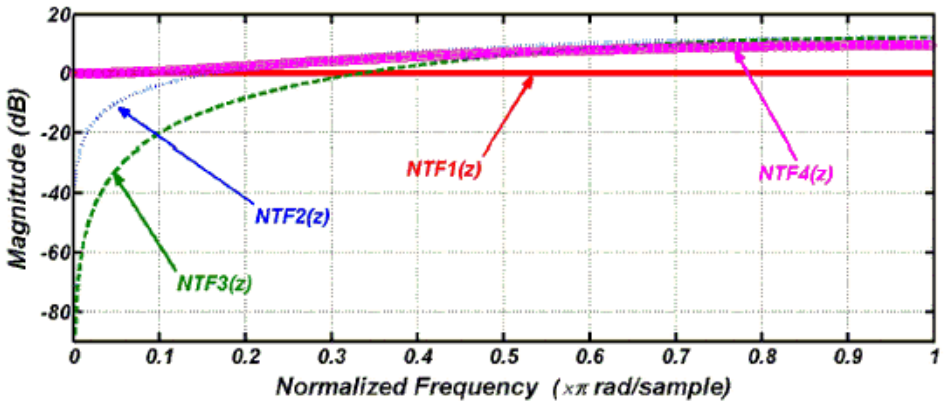
$$NTF_4(z) = \frac{Q(z)}{N_4(z)} = \frac{H_1(z)H_2(z) + H_2(z)}{1 + H_1(z)H_2(z) + H_2(z)} = -z^{-1}(2 - z^{-1}) \tag{D.6}$$

D.3 GUIs as a Toolbox to Aid the Preliminary Design of ΣΔ ADC

A series of MATLAB based GUIs which aid the circuit level implementation of the ΣΔ ADC, right from the scratch, is developed here. Although the design is still modeled using SIMULINK, the GUI



(a)



(b)

Figure D.1: (a) Linear representation of a second order ΣΔ modulator ADC, (b) Magnitude plots of all the NTFs.

developed takes in user-defined inputs, runs the SIMULINK model with these inputs and display the relevant output hence generated in a manner which is aesthetic as well as easily comprehensible. All these GUIs have been uploaded on MATLAB Central, MathWorks [87]. They are freely available and user friendly. It will help a circuit designer fix the order (L), resolution of the internal quantizer (B) and the oversampling ratio (OSR) required to achieve the target SNR. Additionally, it also helps the designer to have an estimate of the required performance specifications of each individual block in order to achieve the desired overall performance. A brief summary of each of the developed GUI is given in the following subsections.

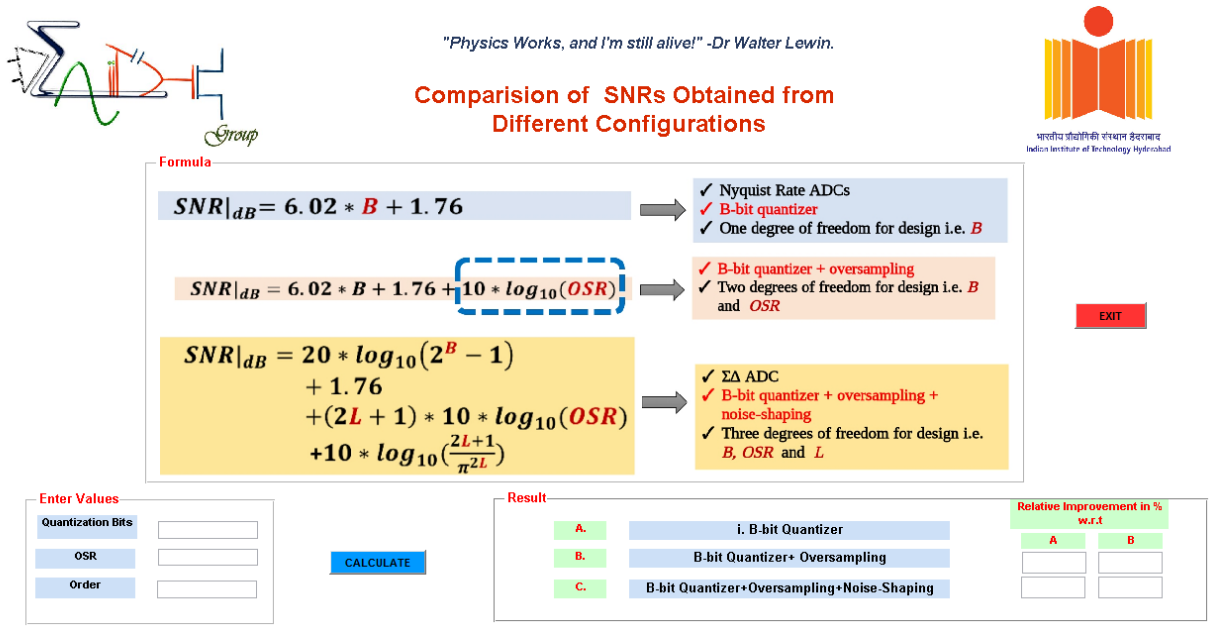


Figure D.2: Screenshot of the GUI for the comparison of resolutions obtained by an ideal ADC.

GUI to Fix the Triad(L,B,OSR) for ΣΔ ADC

The design procedure for a ΣΔ ADC begins with fix the Triad(L,B,OSR) for ΣΔ ADC. To aid the same, the following GUIs are developed :

1. **GUI for the comparison of resolutions obtained by an ideal ADC** :This GUI, shown in Fig. D.2, is intended for a comparative analysis of different resolutions obtained from an ideal ADC considering oversampling and noise shaping. It starts with calculation of the maximum signal-to-noise ratio (SNR) achievable from an ideal ADC using a B-bit quantizer. The percentage improvement in the resolution obtained when the same B-bit ADC is oversampled is also calculated. Finally, we also include noise-shaping along with oversampling. The percentage increment over the normal B-bit quantizer and oversampled ADC is calculated. This tool/GUI would take inputs from the user and provide the different values of resolution for each of the different cases mentioned above. The GUI also displays the basic formula used for calculating these values. It is available at [217].

2. **Design space exploration to find an optimum triad (L, B, OSR) to achieve a target SNR from a ΣΔ ADC** : This MATLAB GUI, shown in Fig. D.3, searches for possible combinations of L,B and OSR to achieve a target SNR/DR. This tool/GUI would take the target SNR or dynamic range as input from the user (viz. order of the modulator,

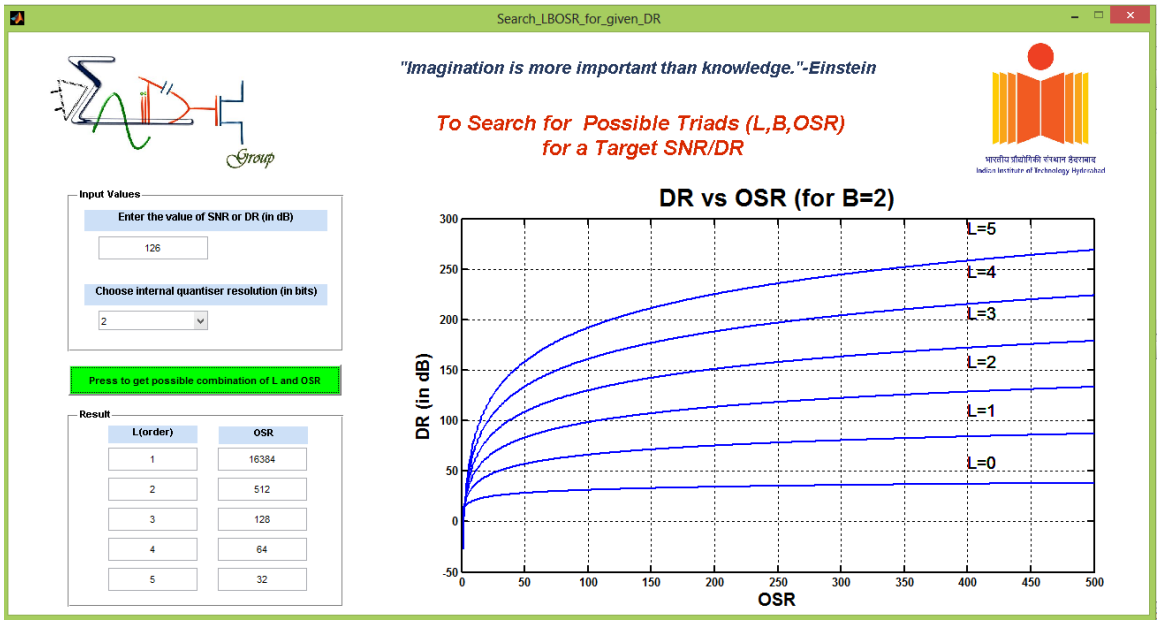


Figure D.3: Screenshot of the GUI for design space exploration to find an optimum triad (L, B, OSR) to achieve a target SNR from a ΣΔ ADC.

oversampling, resolution of the internal quantizer in bits) and provides the value of possible combinations of L,B and OSR to achieve a target SNR/DR. The limits on L,B and OSR used in the GUI can easily extended. The GUI also plots the graph of possible DR for different values of OSR for different values of L. It is available at [218].

GUI to Estimate the Effect of Circuit Non-idealities for a ΣΔ ADC

Each of the circuit comprising the ΣΔ ADC has non-idealities related with it. The various non-idealities related to individual blocks are illustrated in Fig. D.4 using a single-loop ΣΔ ADC. Each of them can be modeled using SIMULINK [207–211]. The developed GUIs allow the designer to input the estimated error introduced by any non-ideality and evaluate degradation in the overall performance.

1. **SNR estimation of a second order ΣΔ ADC while including the various circuit non-idealities using design equations** : This MATLAB GUI, shown in Fig. D.5, estimates of the SNR obtained from a ΣΔ ADC while including the various circuit non-idealities along with quantization noise using very simplified design equations [219,220]. This tool/GUI would take the various circuit design parameters and the important values associated with the non-idealities, and output the resulting SNR accounting for the non-idealities also. The user has the

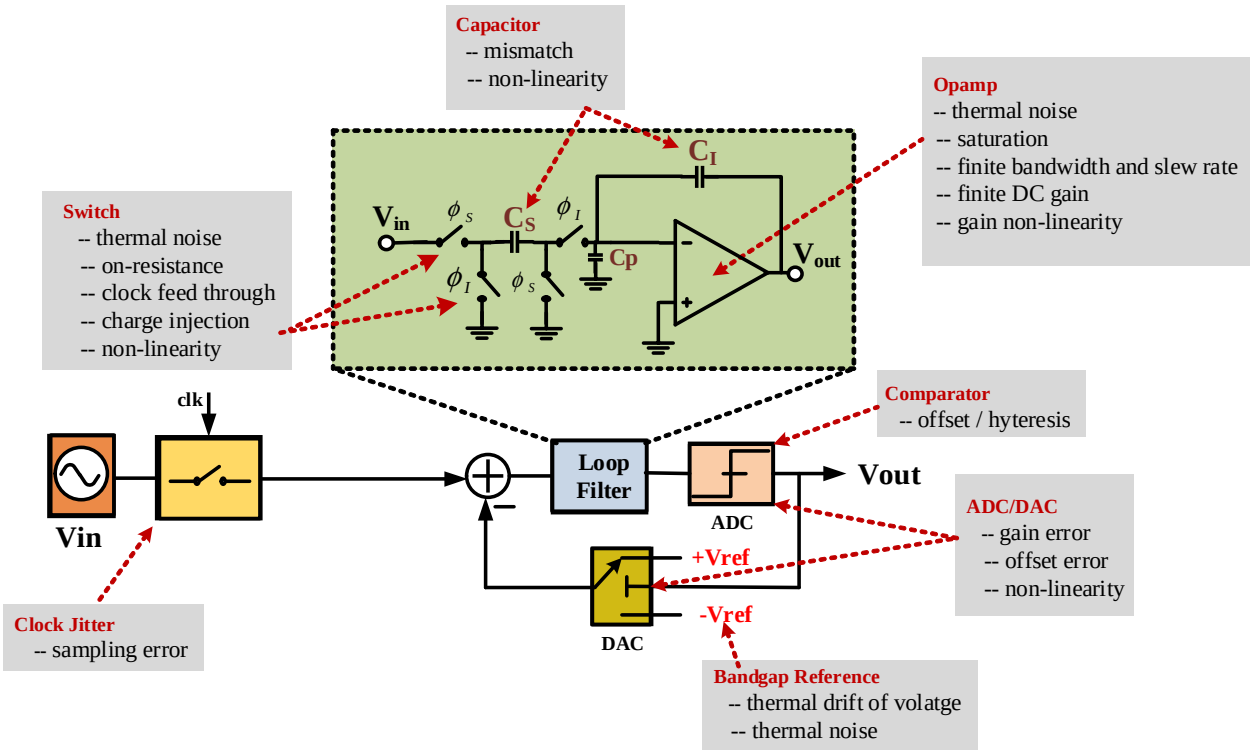


Figure D.4: Various non-idealities associated with each of the major blocks of the ΣΔ modulator ADC.

freedom to choose among the various non-idealities, the ones most relevant to him/her. Also it gives an power corresponding to the chosen noise sources as a percentage of the quantization noise. It is available at [221].

2. **SNR estimation of a second order 1-bit ΣΔ ADC with various non-idealities modeled using SIMULINK** : This MATLAB GUI, shown in Fig. D.6, estimates of the SNR obtained from a second order 1-bit ΣΔ ADC while including the various circuit non-idealities along with quantization noise using very simplified SIMULINK models. This tool/GUI would take the various circuit design parameters and the important values associated with the non-idealities, and output the resulting SNR accounting for the non-idealities also. The user has the freedom to choose (i) among the various non-idealities, the ones most relevant to him/her (ii) number of data points used for calculating the power spectral density/FFT (label as 'N') (iii) range of frequency visible on the axes. It helps the user visualize and zoom in to any sinister tones degrading the SNR value. It is available at [222].

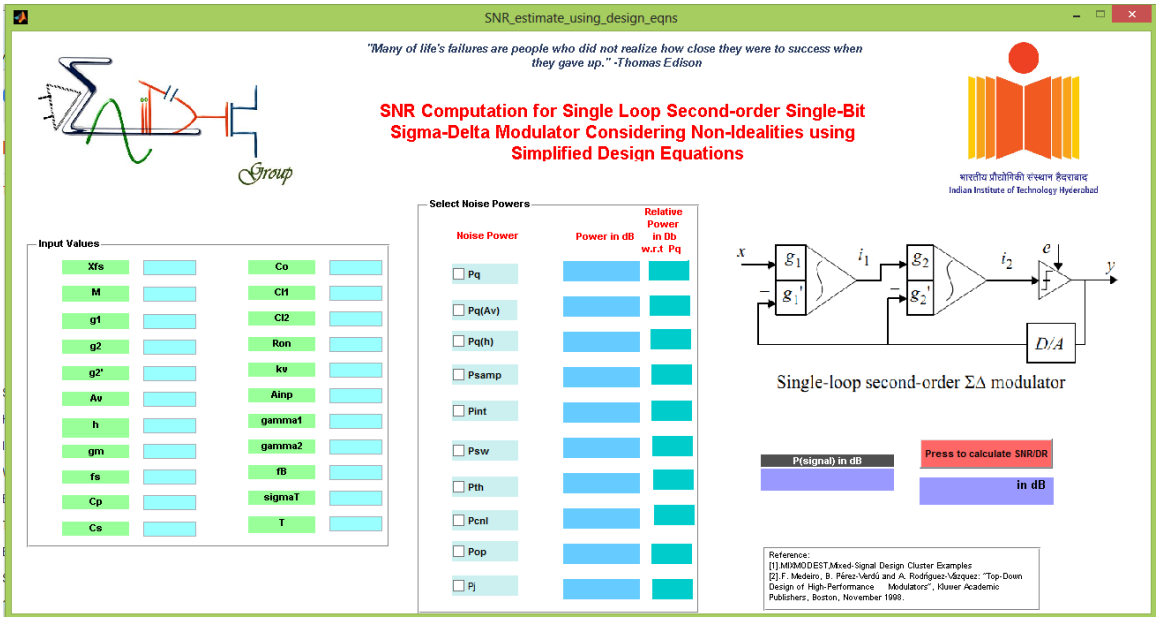


Figure D.5: Screenshot of the GUI for SNR estimation of a second order ΣΔ ADC while including the various circuit non-idealities using design equations.

Dynamic Range Scaling and Ratioanlization of Loop Coefficients of a Second Order 1-bit ΣΔ ADC

This GUI, shown in Fig. D.7, is meant to help in the understanding of the procedure of dynamic range scaling and rationalization of loop coefficients of a second order 1-bit ΣΔ ADC [151, 223–226]. This will help in the direct translation of the behavioral model of a ΣΔ ADC to its real circuit level implementation. The scaled loop coefficients represent the gain capacitor ratios required to keep the output swings of the integrators within the desired limit. The implementation of the capacitors as a combination of multiple unit capacitors helps mitigate the gain capacitors' mismatch. To facilitate the same, the scaled loop coefficients are then represented in form of fractions. These fractions are further simplified so as to keep the denominators same. The percentage error incurred in the implementation of loop coefficients using these fractions are also displayed. The user needs to follow the order given as (i) 'Without Scaling' (ii) 'With Scaling' (iii) 'Rationalize Capacitor Ratios'. It is available at [152].

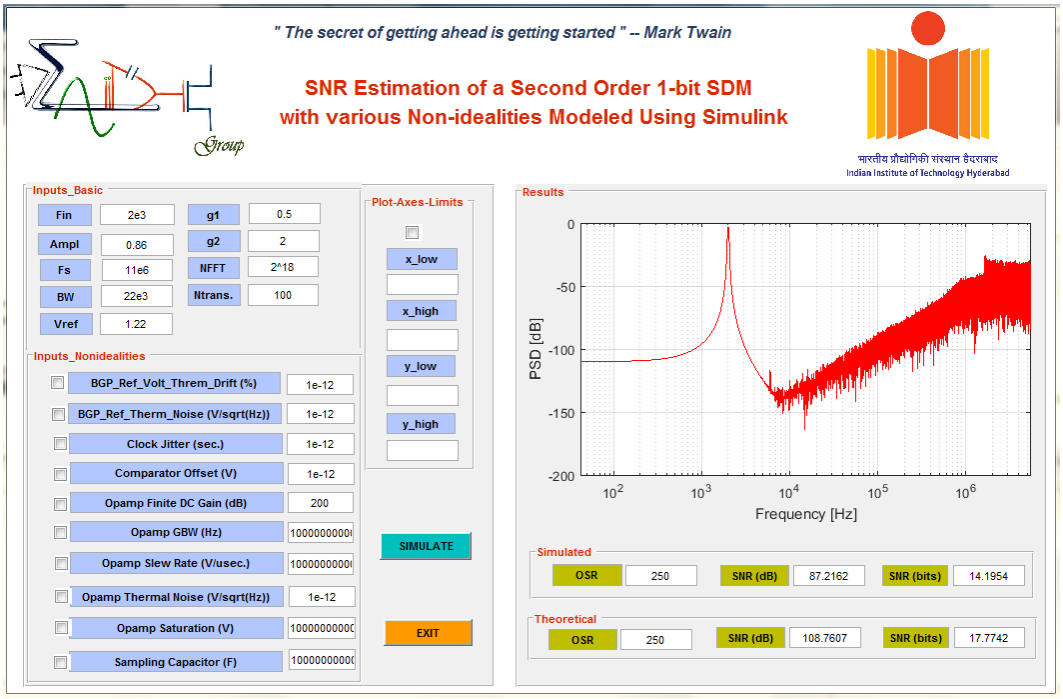


Figure D.6: Screenshot of the GUI for SNR estimation of a second order 1-bit ΣΔ ADC with various non-idealities modeled using SIMULINK.

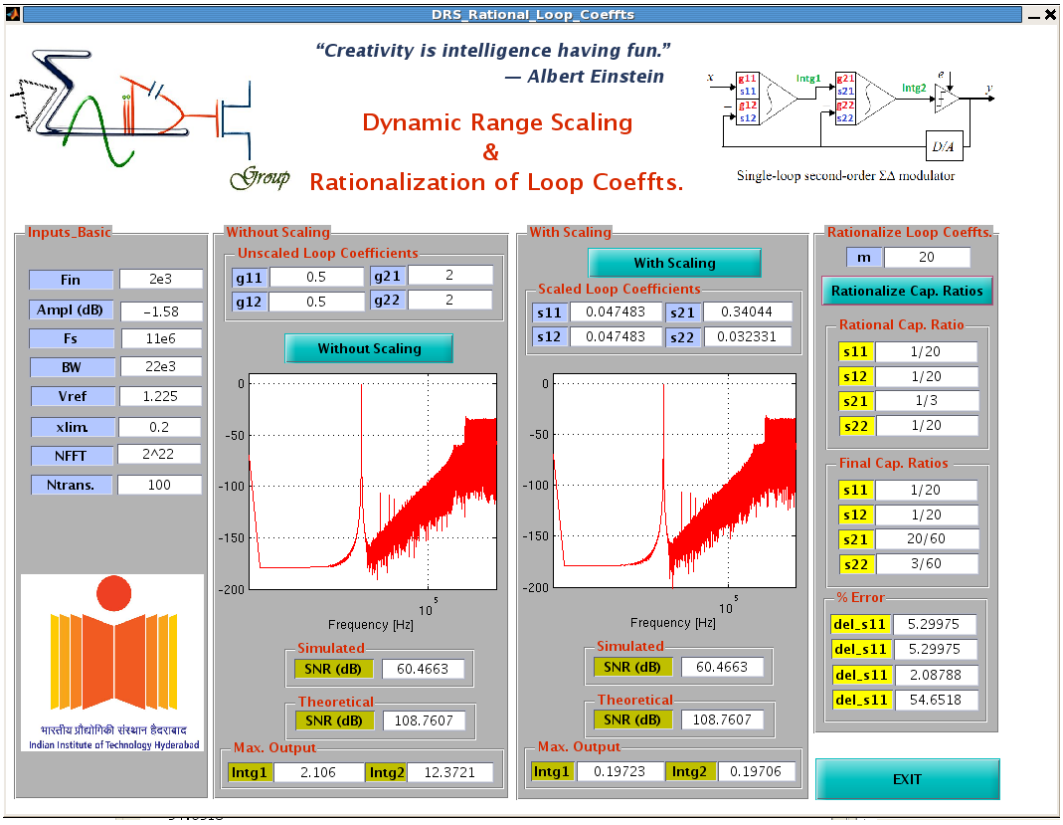


Figure D.7: Screenshot of the GUI for Dynamic Range Scaling and Ratioanlization of Loop Coefficients of a Second Order 1-bit ΣΔ ADC.

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