Designing and implementing a novel single IFFT scrambling PAPR reduction scheme in OFDM systems using FPGA with hardware co-simulation

ABSTRACT

This paper presents a novel low complexity technique for reducing the peak-to-average power ratio (PAPR) in orthogonal frequency division multiplexing systems followed by an efficient hardware co-simulation implementation of this technique by using a Xilinx system generator on field programmable gate array. In this technique, the output of inverse fast Fourier transforms (IFFT) is partitioned into M subblocks, which are subsequently interleaved. Then, a new optimization scheme is introduced in which only a single two phase sequence need to be applied. Unlike the conventional partial transmit sequence (C-PTS) which needs M-IFFT blocks and WM−1 iterations, the proposed technique requires only a single IFFT block and M iterations. These features significantly reduce processing time and less computation that leads to reduced complexity. Simulation results demonstrate that the new technique can effectively reduce the complexity up to 99.95% compared with the conventional PTS (C-PTS) technique and yields good PAPR performance. The good PAPR performance arises from the effect of both the data interleaving and the new optimization technique. Through the comparison of performance between simulation and hardware, it is distinctly illustrated that the designed hardware block diagram is as workable as the simulation, and the difference of the result is only 0.1 dB.

Keyword: OFDM; PAPR; Scramblng scheme; Hardware co-simulation; FPGA