

Characterizing the Firing Properties of an Adaptive Analog VLSI Neuron

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Abstract. We describe the response properties of a compact, low power, analog circuit that implements a model of a leaky-Integrate & Fire (I&F) neuron, with spike-frequency adaptation, refractory period and voltage threshold modulation properties. We investigate the statistics of the circuit's output response by modulating its operating parameters, like refractory period and adaptation level and by changing the statistics of the input current. The results show a clear match with theoretical prediction and neurophysiological data in a given range of the parameter space. This analysis defines the chip's parameter working range and predicts its behavior in case of integration into large massively parallel very-large-scale-integration (VLSI) networks.

1 Introduction

Models of spiking neurons have complex dynamics that require intensive computational resources and long simulation times. This is especially true for conductance-based models that describe in details the electrical dynamics of biological neurons [1]. These models include non-linear voltage-dependent membrane currents and are difficult to analyze analytically and to implement. For this reason, phenomenological spiking neuron models are more popular for studies of large network dynamics. In these models the spikes are stereotyped events generated whenever the membrane voltage reaches a threshold. The Integrate-and-Fire (I&F) model neuron, despite its simplicity, captures many of the broad features shared by biological neurons. This model can be easily implemented using analog very-large-scale-integration (VLSI) technology and can be used to build low power, massively parallel, large recurrent networks, providing a promising tool for the study of neural network dynamics [2,3].

VLSI I&F neurons integrate presynaptic input currents and generate a voltage pulse when the integrated voltage reaches a threshold. A very simple circuit implementation of this model, the "Axon-Hillock" circuit, has been proposed by Mead [4]. In this circuit an integrating capacitor is connected to two inverters and a feedback capacitor. A pulse is generated when the integrated voltage crosses the switching threshold of the first inverter. An alternative circuit, proposed in [5], exhibits more realistic behaviors, as implements spike-frequency adaptation and has an externally set threshold voltage for the spike emission. Both circuits however have a large power consumption due to the fact that

the input to the first inverter (the integrated voltage on the capacitor) changes slowly, typically with time constants of the order of milliseconds, and the inverter spends a large amount of time in the region in which both transistors conduct a short-circuit current. The power consumption is reduced, but not optimized, in the circuit described in [6], using an amplifier at the input, to compare the voltage on the capacitor with a desired spiking threshold voltage. As the input exceeds the spiking threshold, the amplifier drives the inverter, making it switch very rapidly. In [7] Boahen demonstrates how it is possible to implement spike-frequency adaptation by connecting a four transistor “current-mirror integrator” in negative-feedback mode to any I&F circuit. An I&F circuit optimized with respect to power consumption but lacking of spike-frequency adaptation mechanisms, voltage threshold modulation, refractory period and explicit leak current is described in [8]. We designed a compact leaky I&F circuit, similar to previously proposed ones, that additionally is low power *and* has spike-frequency adaptation, refractory period and voltage threshold modulation properties [9]. In this work we characterize the circuit and compare its response properties to the ones predicted by theory and observed in neocortical pyramidal cells. Specifically we measured the response function of the circuit to noisy input signals, by varying both circuit parameters and the parameters that control the statistics of the input current. The results described in this paper present a description of the integrated-circuit’s data in neurophysiological terms, in order to reach a wider scientific community. With this approach we address important questions like the feasibility of simulation of large networks of spiking neurons built using analog VLSI circuits.

2 The I&F Circuit

The I&F neuron circuit is shown in Fig. 1. The circuit comprises a source follower M1-M2, used to control the spiking threshold voltage; an inverter with positive feedback M3-M7, for reducing the circuit’s power consumption; an inverter with controllable slew-rate M8-M11, for setting arbitrary refractory periods; a digital inverter M13-M14, for generating digital pulses; a current-mirror integrator M15-M19, for spike-frequency adaptation, and a minimum size transistor M20 for setting a leak current.

2.1 Circuit Operation

The input current $I_{in,j}$ is integrated linearly by C_{mem} onto V_{mem} . The source-follower M1-M2, produces $V_{in} = \kappa(V_{mem} - V_{sf})$, where V_{sf} is a constant sub-threshold bias voltage and κ is the sub-threshold slope coefficient [10]. As V_{mem} increases and V_{in} approaches the threshold voltage of the first inverter, the feedback current I_{fb} starts to flow, increasing V_{mem} and V_{in} more rapidly. The positive feedback has the effect of making the inverter M3-M5 switch very rapidly, reducing dramatically its power dissipation.

A spike is emitted when V_{mem} is sufficiently high to make the first inverter switch, driving V_{spk} and V_{o2} to V_{dd} . During the spike emission period (for as long as V_{spk} is high), a current with amplitude set by V_{adap} is sourced into the gate-to-source parasitic capacitance of M19 on node V_{ca} . Thus, the voltage V_{ca} increases with every spike, and slowly leaks to zero through leakage currents when there is no spiking activity. As

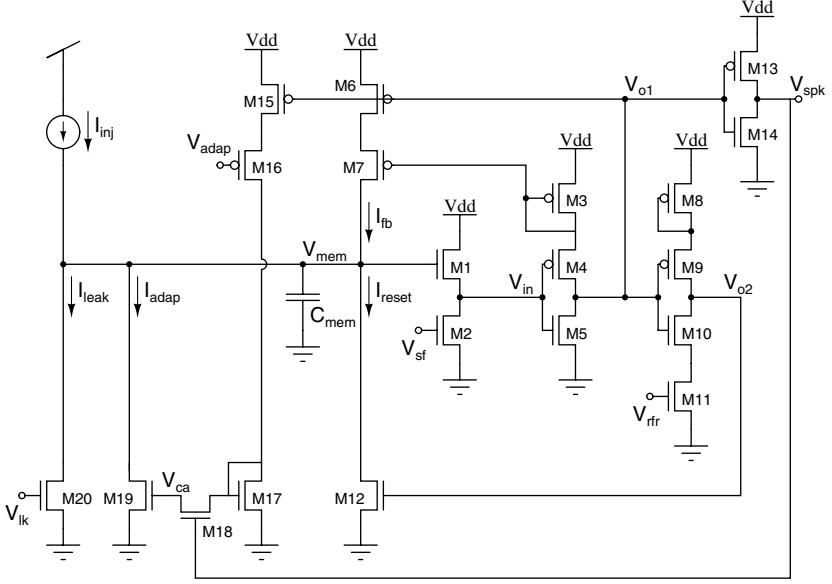


Fig. 1. Circuit diagram of the I&F neuron.

V_{ca} increases, a negative adaptation current I_{adap} exponentially proportional to V_{ca} is subtracted from the input, and the spiking frequency of the neuron is reduced over time.

Simultaneously, during the spike emission period, V_{o2} is high, the reset transistor M12 is fully open, and C_{mem} is discharged, bringing V_{mem} rapidly to Gnd . As V_{mem} (and V_{in}) go to ground, V_{o1} goes back to V_{dd} turning M10 fully on. The voltage V_{o2} is then discharged through the path M10-M11, at a rate set by V_{rfr} (and by the parasitic capacitance on node V_{o2}). As long as V_{o2} is sufficiently high, V_{mem} is clamped to ground. During this “refractory” period, the neuron cannot spike, as all the input current I_{inj} is absorbed by M12.

The adaptation mechanism implemented by the circuit is inspired by models of its neurophysiological counterpart [11,12,13]: the voltage V_{ca} , functionally equivalent to the calcium concentration $[Ca^{2+}]$ in a real neuron, is increased with every spike and decays exponentially to its resting value; if the dynamics of V_{ca} is slow compared to the inter-spike intervals then the effective adaptation current is directly proportional to the spiking rate computed in some temporal window. This results had been extensively applied to investigate the steady-state responses [14,15] and the dynamic proprieties [15] of adapted neurons.

Figure 2(a) shows an action potential generated by injecting a constant current I_{inj} into the circuit and activating both spike-frequency adaptation and refractory period mechanisms. Figure 2(b) shows how different refractory period settings (V_{rfr}) saturate the maximum firing rate of the circuit at different levels.

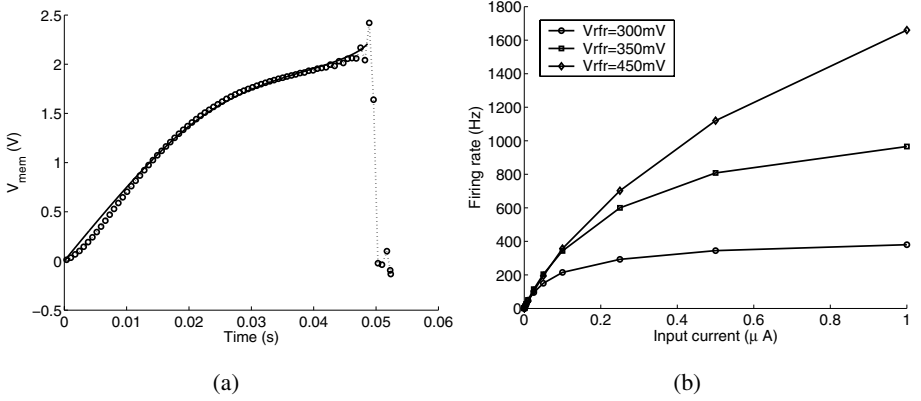


Fig. 2. (a) Measured data (circles) representing an action potential generated for a constant input current I_{inj} with spike-frequency adaptation and refractory period mechanisms activated. The data is fitted with the analytical model of eq. (5) (solid line). (b) Circuit's f - I curves (firing rate versus input current I_{inj}) for different refractory period settings.

2.2 Modeling the Neuron's Subthreshold Behavior

The circuit presented does not implement a simple linear model of an I&F. Rather its positive feedback and spike-frequency adaptation mechanisms represent additional features that increase the model's complexity (and hopefully its computational capabilities). The overall current that the circuit receives is $I_{in} + I_{fb} - I_{adapt}$, where I_{in} is the circuit's input current I_{inj} subtracted by the leak current I_{leak} (see Section 2.3), I_{fb} is the positive feedback current and I_{adapt} is the adaptation current generated by the spike-frequency adaptation mechanism. We can use the transistor's weak-inversion equations [10] to compute the adaptation current:

$$I_{adapt} = I_0 e^{\kappa \frac{V_{ca}}{U_T}} \quad (1)$$

where I_0 is the transistor's dark current [10] and U_T is the thermal voltage.

If we denote with C_a the parasitic gate-to-source capacitance on node V_{ca} of M19, and with C_p the parasitic gate-to-drain capacitance on M19, then:

$$V_{ca} = V_{ca0} + \gamma V_{mem} \quad (2)$$

where $\gamma = \frac{C_p}{C_p + C_a}$ and V_{ca0} is the steady-state voltage stored on C_a , updated with each spike.

To model the effect of the positive feedback we can assume, to first order approximation, that the current mirrored by M3,M7 is:

$$I_{fb} = I_1 e^{\kappa V_{in}} \quad (3)$$

where I_1 is a constant current flowing in the first inverter when both M4,M5 conduct, and $V_{in} = \kappa(V_{mem} - V_{sf})$ is the output of the source-follower M1,M2.

The equation modeling the subthreshold behavior of the neuron is:

$$C_0 \frac{d}{dt} V_{mem} = I_{in} + I_{fb} - I_{adap} \quad (4)$$

where $C_0 = C_m + \gamma C_a$. Substituting I_{adap} and I_{fb} with the equations derived above we obtain:

$$C_0 \frac{d}{dt} V_{mem} = I_{in} + \left[I_1 e^{-\kappa 2 \frac{V_{sf}}{U_T}} e^{\kappa 2 \frac{V_{mem}}{U_T}} \right] - \left[I_0 e^{\kappa \frac{V_{a0}}{U_T}} e^{\kappa \gamma \frac{V_{mem}}{U_T}} \left(1 - e^{-\frac{V_{mem}}{U_T}} \right) \right] \quad (5)$$

We fitted the experimental data by integrating eq. (5) numerically and using the parameters shown in Table 1 (see solid line of Fig. 2(a)). The initial part of the fit (for low values of V_{mem}) is not ideal because the equations used to model the source follower M1,M2 are correct only for values of V_{mem} sufficiently high.

Table 1. Parameters used to fit the data of Fig. 2(a)

$C_m = 0.66\text{pF}$	$I_{in} = 177\text{pA}$	$V_{sf} = 0.5\text{V}$
$C_a = 0.12\text{pF}$	$I_1 = 2.29\text{pA}$	$V_{a0} = 50\text{mV}$
$C_p = 500\text{fF}$	$I_0 = 100\text{fA}$	$\kappa = 0.6$

2.3 Stimulating the Neuron Circuit

To inject current into the neuron circuit we use an on-chip p-type transistor operating in the weak-inversion domain [10]. By changing the transistor's gate voltage we can generate the current:

$$I_{inj} = I_0 e^{\frac{\kappa}{U_T} (V_{dd} - V_p)} \quad (6)$$

where V_p is the p-type transistor's gate voltage that we can control. If we take into account the leak current I_{leak} sourced by the transistor M20 of Fig. 1 we can write the net input current to the circuit as:

$$I_{in} = I_{inj} - I_{leak} = I_0 e^{\frac{\kappa}{U_T} (V_{dd} - V_p)} - I_{0n} e^{\frac{\kappa}{U_T} V_{ik}} (1 - e^{-V_{mem}}) \quad (7)$$

On the other hand, the *desired* input current that we want inject into the neuron is:

$$I_{des} = I_{d0} \cdot \eta(\mu, \sigma) \quad (8)$$

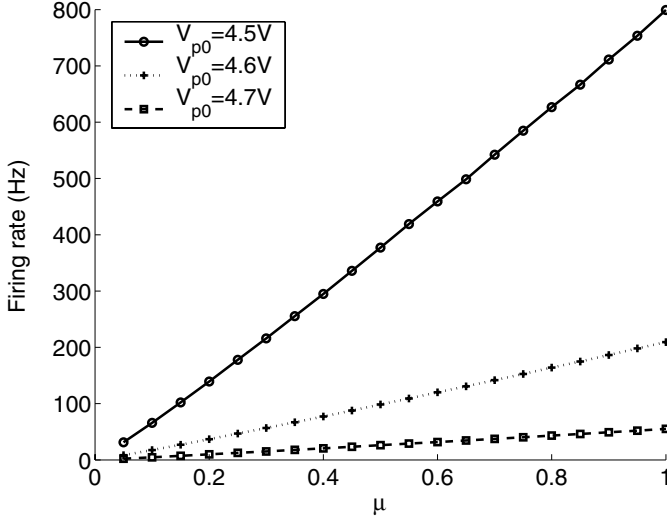


Fig. 3. f - I curves for different reference voltages V_{p0} having set the refractory period to zero. The relation between the input current and the output frequency is linear.

where I_{d0} is a normalizing factor and η represents a stochastic input signal ranging from zero to one, characterized by a mean value μ and standard deviation (STD) σ .

We can force the net input current I_{in} to be the desired input current I_{des} if we break up the current source gate voltage V_p in the following way:

$$V_p = r_1 V_{in} + r_2 V_{p0} \quad (9)$$

where V_{p0} is a constant reference voltage, V_{in} is the voltage encoding the signal η (controlled by a PC-IO card), and r_1 and r_2 are the factors of a resistive divider used to scale and sum the two voltages V_{p0} and V_{in} . In this case the net input current becomes:

$$I_{in} = I_0 e^{\frac{\kappa}{U_T}(V_{dd} - r_2 V_{p0})} e^{-\frac{\kappa}{U_T} r_1 V_{in}} - I_{leak} \quad (10)$$

which can be simplified to

$$I_{in} = I_p e^{-\frac{\kappa}{U_T} r_1 V_{in}} - I_{leak} \quad (11)$$

with constant

$$I_p = I_0 e^{\frac{\kappa}{U_T}(V_{dd} - r_2 V_{p0})} \quad (12)$$

If we map the signal η onto V_{in} in a way that

$$V_{in} = -\frac{U_T}{\kappa} \frac{1}{r_1} \ln \left(e^{-\frac{\kappa}{U_T} r_1 V_{dd}} - \eta \left(e^{-\frac{\kappa}{U_T} r_1 V_{dd}} + e^{\frac{\kappa}{U_T} r_1 V_{dd}} \right) \right) \quad (13)$$

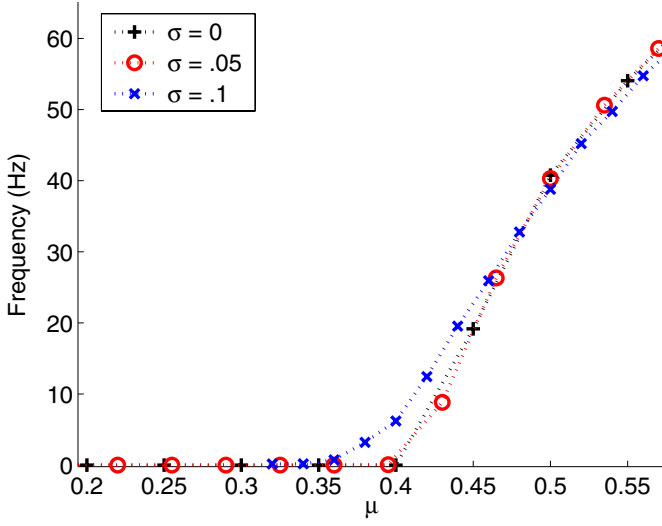


Fig. 4. f - I curves measured for three different values of σ . Note that for $\sigma = 0$ (cross marker) the presence of high non-linearity at the rheobase. For increasing σ 's the behavior at the rheobase is linearized.

we make use of the full PC-IO card dynamic range (from -5V to +5V) and obtain the desired current $I_{in} = I_{des}$, provided that the leak current is set to:

$$I_{leak} = I_p e^{-\frac{\kappa}{U_T} r_1 V_{dd}} \quad (14)$$

and that I_{d0} of eq.(8) is:

$$I_{d0} = I_p \left(e^{-\frac{\kappa}{U_T} r_1 V_{dd}} + e^{\frac{\kappa}{U_T} r_1 V_{dd}} \right) \quad (15)$$

In Fig. 3 we show the effect of V_{p0} (that affects exponentially I_{d0}) on the f - I curve measured from the circuit, for increasing values of the mean input current μ , with $\sigma = 0$.

3 Results

We first tested the neuron with the adaptation mechanism turned off, injecting an input current with a statistics parameterized by mean μ and STD σ .

3.1 General Proprieties of the I&F Circuit

We measured the I&F circuit's f - I curves as a function of its input current $I_{d0}\eta$. The signal $\eta(\mu, \sigma)$ was generated to reproduce white noise with mean μ and STD σ . Figure 4 shows the f - I curves for three different values of STD. All the curves were obtained by setting the neuron's refractory period to approximately 6.6 ms ($V_{rfr} = 280$ mV).

The circuit's firing rate f has a dependence on the the refractory period (τ_r) of the type [16]:

$$f \approx \frac{1}{\tau_r + \frac{1}{I_{in}}} \quad (16)$$

Figure 2(b) shows f - I curves obtained for three different values of V_{rfr} (τ_r). The curves tend, in the limit of $\tau_r \rightarrow 0$, to a straight line with slope inversely proportional to the circuit's spiking threshold voltage (as shown in Fig.3).

We measured the distribution of the inter-spike intervals (ISIs) generated by the circuit for two values of $\sigma = \{0.05, 0.1\}$, sweeping the mean input current $I_{d0}\eta$. To analyze the statistic of these distributions, we computed their coefficient of variation (CV), given by the ratio between the STD and the mean of the neuron's ISI [17,18]. In Fig. 5 we plot the CVs against the neuron's output frequency. The CVs are in accordance with theoretical [19] and experimental studies on neurons of layer 4 and 5 of the rat [14]. The ISI distribution for increasing input currents shifts toward lower mean-ISI, and its STD decreases. The refractory period constrains the distribution to remain above a certain ISI even if its STD decreases with the current. In the theoretical limit of a renewal process the mean and the STD of the ISI distribution should be approximately equal. By increasing the mean afferent current the CV decreases because the probability to remain above the threshold for spiking increases reducing the stochasticity of the spiking event.

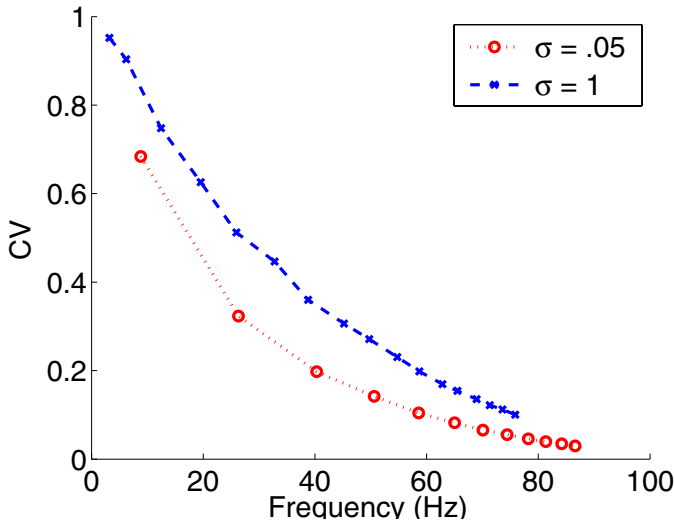


Fig. 5. Coefficients of variation of the I&F neuron's ISIs for two different values of σ plotted against output frequency. Higher σ 's produce higher spike decorrelation, similar to what is observed in Poisson processes (CV close to one).

3.2 Effects of the Adaptation on the I&F Circuit

Here we consider how the spike frequency adaptation mechanism influences the I&F neuron's behavior. We analyzed the response of the circuit to a series of depolarizing current steps with increasing values of μ (with $\sigma=0$) and with different values of the spike-frequency adaptation rate, both in the transient regime and in the steady-state regime.

Dynamic Firing Proprieties. The neuron responds to current steps with instantaneous firing rates that progressively adapt to lower (steady-state) values (see Fig. 6). The circuit's adaptation current I_{adap} is integrated by a non-linear integrator (see M15-M19 of Fig. 1) and increases progressively with every spike (see also Section 2.2). As I_{adap} is subtracted from the input current I_{in} , the neuron's net input current progressively decreases, together with its output firing rate. In the steady-state an equilibrium is reached when the adaptation current is balanced with the output firing rate (significantly lower than the initial one).

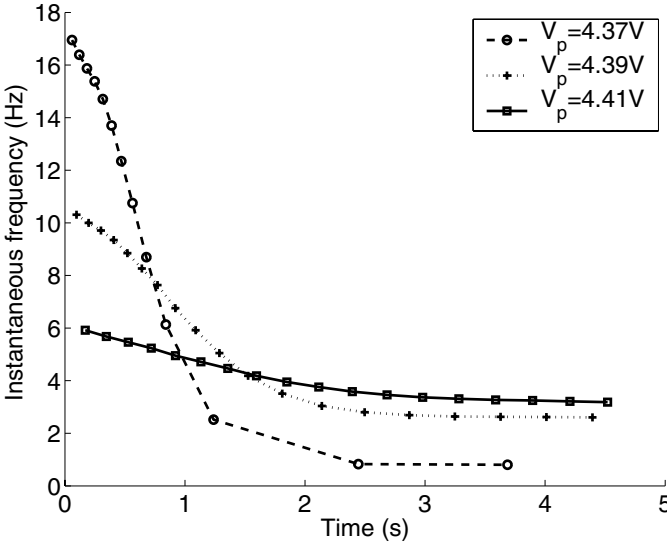


Fig. 6. Instantaneous frequency response of the circuit with $V_{adap}=4.19V$, for increasing values of input step amplitudes (decreasing values of V_p). The abscissa of each data point corresponds to the spike time from the input step onset.

In Fig. 6 we show different instantaneous frequency response curves over time ($f-t$ curves) for increasing values of the input current's step amplitude and for a fixed adaptation setting. Similar to what has been observed experimentally [20], the adaptation rate increases and the instantaneous frequency response decay time decreases, with higher input step amplitudes.

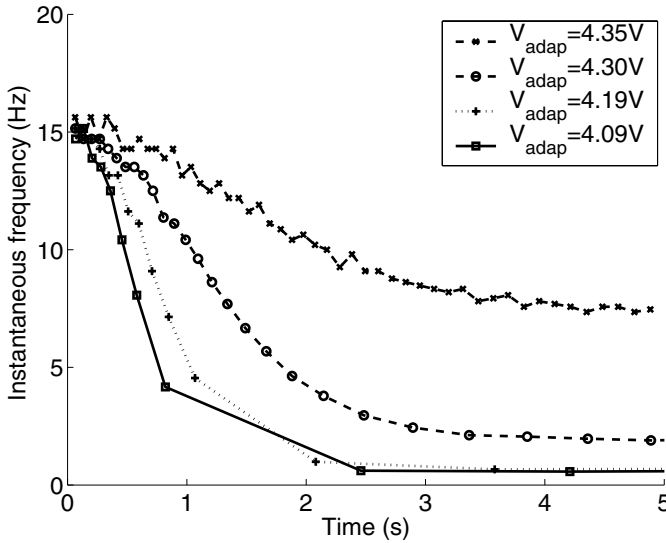


Fig. 7. Instantaneous frequency response for different adaptation rates. The neuron adapts more quickly as the adaptation rate increases (V_{adap} decreases), and the corresponding steady-state output frequency is lower.

In Fig. 7 we plotted different f - t curves for different values of the adaptation rate. The data plotted shows how increasing levels of adaptation shorten the time required by the neuron to adapt and to reach a mean steady-state value.

Steady-State Firing Proprieties. Figure 8 shows two steady-state f - I curves measured for two different spike-frequency adaptation rates. Increasing values of adaptation rate decrease the overall steady-state firing rate f , as shown also in Fig. 7. The inset of Fig. 8 evidences how spike-frequency adaptation has the effect of decreasing the slope of the steady-state curves at the rheobase, as predicted by theoretical [11] and experimental [14, 15] evidence.

4 Conclusions

We presented a novel analog VLSI circuit that implements a real-time model of a leaky I&F neuron. We characterized its response properties in a wide range of conditions, as a function of both the circuit's parameters and the statistics of the input signals. One of the most interesting properties of the circuit is its ability to model spike-frequency adaptation. We activated this feature, characterized the circuit, and showed how it exhibits different adapting behaviors when its operating conditions change. The inclusion of the adaptation mechanism addresses the question of which neurophysiological parameters in real neurons (spike induced Ca^{2+} influx, $[Ca^{2+}]$ decay time, ionic conductances) are actually captured by the VLSI circuit. Ahmed et al. [20] reported that spike frequency

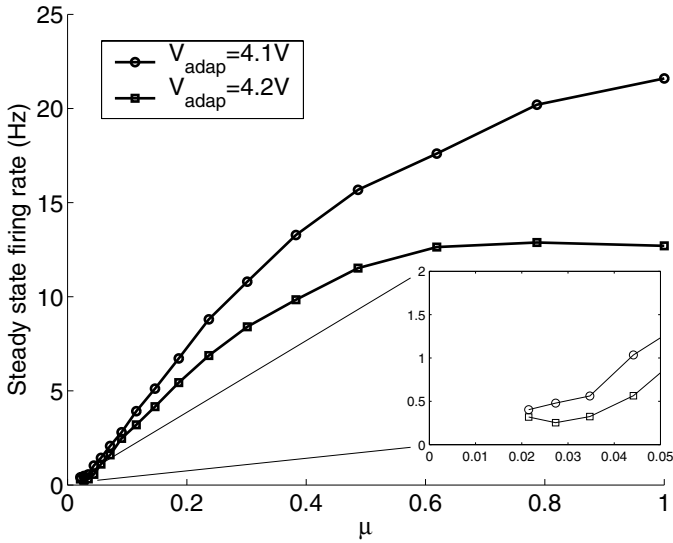


Fig. 8. f - I curves of the steady-state response of the adapted neuron for two different values of spike-frequency adaptation rate. The figure inset shows a detail of the f - I curve at low levels of current injection, confirming the adaptation induced linearization at the rheobase.

adaptation to a current step in neurons of the cat primary cortex can be well fitted by a single exponential curve depending on the degree of adaptation. This behavior is well captured by our circuit (see Fig. 6): the exponential rate decay is observed for low values of input currents, and the degree of adaptation can be set with V_{adap} . The results presented here, together with the circuit's low-power characteristics [9] make it suitable for integration in very large arrays containing also synaptic circuits [2,7,21], and for the construction of massively parallel analog VLSI networks of spiking neurons.

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