Hybrid Amorphous-Selenium/CMOS Low-Light Imager

by

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Abstract

This thesis aims to demonstrate a low-light imager capable of moonlight-level imaging by combining a custom-designed complementary-metal-oxide-semiconductor (CMOS) pixel array with amorphous selenium (a-Se) as its photosensor. Because of the low dark current of a-Se compared to standard silicon photodiodes, this hybrid structure could enable imagers fabricated in standard mixed-signal CMOS processes to achieve low-light imaging. Such hybrid imagers could have low-light performances comparable to other low-light imagers fabricated in specialized CMOS image-sensor processes.

The 320 (H) x 240 (V) imager contains four different pixel designs arranged in four quadrants, with pixel pitches of 7.76 µm x 7.76 µm in quadrants 1 to 3 and 7.76 µm x 8.66 µm in quadrant 4 (Q4). The different quadrants are built to examine various performance-enhancing circuit designs and techniques, including series-stacked devices for leakage suppression, charge-injection suppression that uses dummy transistors, and a programmable dual-capacity design for extended pixel dynamic range. The imager-performance parameters, such as noise, dynamic range, conversion gain, linearity, and full-well capacity were simulated and experimentally verified. This work will also describe the external hardware and software designs used to operate the imager. This thesis summarizes and reports the overall electrical and optical performance of pixels in quadrant 1. The observed signal-to-noise ratio (SNR) of above 20 dB at an illuminance of 0.267 lux demonstrates that the imager can produce excellent images under moonlight-imaging conditions. This was achieved mainly through utilization of the long integration time enabled by circuit techniques implemented at the pixel level, as well as the low dark current of a-Se.

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Dedication

This thesis is dedicated to the ones I love.

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Chapter 1

Introduction

Modern digital-imaging technology has come a long way since Steven Sasson introduced the first digital camera at Kodak in 1975 [1]. Digital cameras have benefited greatly from Moore's law. Charge-coupled devices (CCDs) and complementary metal-oxide semiconductors (CMOS) have been used to build smaller, more compact, and faster imagers. Still, however, few digital cameras can compete with the human visual system's performance under low-light conditions. This is chiefly because digital camera systems are affected by the noise generated in readout electronics that set practical limits on the lower detection boundary in low-light conditions. The few imagers that have exceptional low-light performance are expensive and usually require either a large form factor to house a cooling unit or a more sophisticated fabrication process to reduce the imager's electrical noise.

Improving the low-light imaging capability of cameras built with standard CMOS processes could improve many product systems, including low-cost, high-volume consumer electronics, such as smartphone cameras and computer vision systems. The low-light performance improvement can come from either the photosensor or the readout electronics.

This thesis presents a new design for building low-light image sensors that combines amorphous selenium (a-Se) as the photoconductor material with a readout circuit built using a standard mixed-signal CMOS process. With unconventional vertical stacking architecture that greatly improves the imager fill factor, coupled with the a-Se low dark current, this low-light imager's performance could be comparable to the other specialized low-light imagers already mentioned. The Silicon Thin-film Advanced Research (STAR) group at the University of Waterloo has previously shown the X-ray-imaging

potential of the a-Se/CMOS hybrid-imager structure with the AM2 imager, as Figure 1.1 shows [2]. This thesis explores the static low-light imaging capability of the same architecture with a newly designed CMOS chip by focusing on better noise performance and achieving higher SNR under low-light conditions.

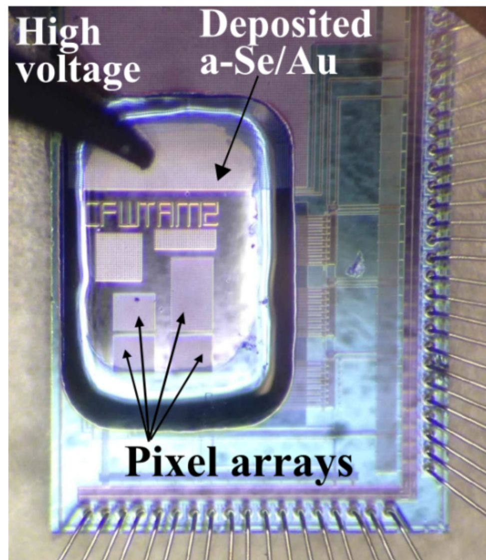


Figure 1.1: AM2 imager with an amorphous selenium photosensor on a CMOS readout integrated circuit (ROIC).

1.1 Low-Light Imaging

The human visual system contains two types of sensory cells: cones, which are responsible for detecting colors, and rods, which are sensitive to brightness. Together, they operate in 3 regions across the visible-light spectrum at different luminances (i.e., surface brightness), as Figure 1.2 shows [3]. The chart covers the luminance of common natural light sources people experience daily, from a no-moon sky to a sunny day. Luminance is the luminous flux per unit solid angle per unit projected source area in a given direction, with the units of cd (candela)/m^2. Luminous intensity, a measure of light (with the unit of cd) leaving a surface, is independent of the distance between the light source and the observer. By definition, candela is the luminous intensity, in a given direction, of a source that emits monochromatic radiation of frequency 540 x 10^{12}

Hz and that has a radiant intensity, in a given direction, of 1/683 Watts per steradian [44].

Photopic vision occurs under well-lit conditions in which both cones and rods are active but also in which cones are the dominating sensory cells and allow good color recognition and acuity. Mesopic vision occurs under dim conditions in which cones are less sensitive but rods work alongside them, enabling color detection. Scotopic vision occurs under dark conditions in which rods are the dominating sensory cells and color sensitivity drops but brightness awareness peaks.

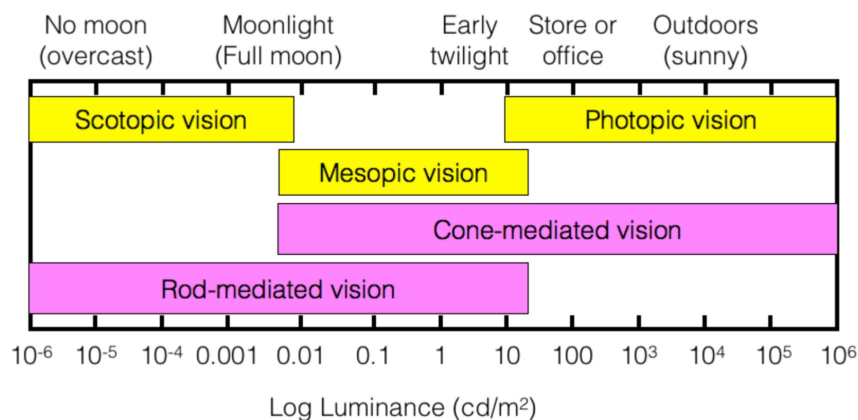


Figure 1.2: Luminance table for the human visual system.

Since luminance is used to describe the brightness of a light-emitting surface, such as the sun, the moon, LEDs, or computer monitors. It cannot be used to characterize the amount of light an imager sees. Illuminance must be used to accurately describe the amount of light an imager sees. Illuminance takes the distance between the source and the observer, as well as the size of the observer, into account. Lux is the unit of illuminance, with the unit of lumen (lm) $/\mathrm{m}^2$. Lumen is the SI unit of luminous flux, for which one lumen is defined as the luminous flux of light produced by a light source emitting one candela of luminous intensity over a solid angle of one steradian. Section 4.1.1 includes a detailed conversion between luminous intensity at a given distance and illuminance (lux). Table 1.1 [4] summarizes the common illuminance levels from natural light sources. Note that moonlight will typically provide between 0.05 and 0.267 lux of illumination [5]. This thesis will focus on imaging in the scotopic-vision region with the aim to build an imager that can produce recognizable images with illuminance of less than 0.05 lux, which is the lower boundary of moonlight illuminance, making the system moonlight-imaging capable.

Table 1.1: Common illuminance conditions.

	Lux
Sun overhead	130000
Full daylight (not direct sun)	10000-25000
Overcast day	1000
Very dark overcast day	100
Twilight	10
Deep twilight	1
1 candela at 1-meter distance	1
Full moon overhead	0.267
Total starlight + airglow	2.00E-03
Total starlight only	2.00E-04
Venus at brightest	1.40E-04
Total starlight at overcast night	1.00E-04
Venus at brightest	1.40E-4
Total starlight at overcast night	1.00E-4

1.2 Digital-Imaging Technology Overview

A digital-imaging system consists of two major blocks: the photosensor, which is responsible for converting incoming optical photons into electron-hole pairs (charge), and the readout electronics, which processes the converted charge and facilitates digitization. This section will provide a brief overview of common architectures used for both components.

1.2.1 Photosensors

The most common photosensors in consumer electronics are photodiodes formed with doped silicon-junction diodes. More specialized photosensing material can be deposited onto a CMOS-imager chip via post-processing for advanced applications, thus forming a hybrid imager. Amorphous selenium deposited on CMOS [2] is such a hybrid structure. With its low dark current, as compared to standard silicon photodiodes, a-Se can provide superior imaging performance under low-light conditions if readout electronics for both photosensors have similar noise performance. This section will discuss both types of photosensors.

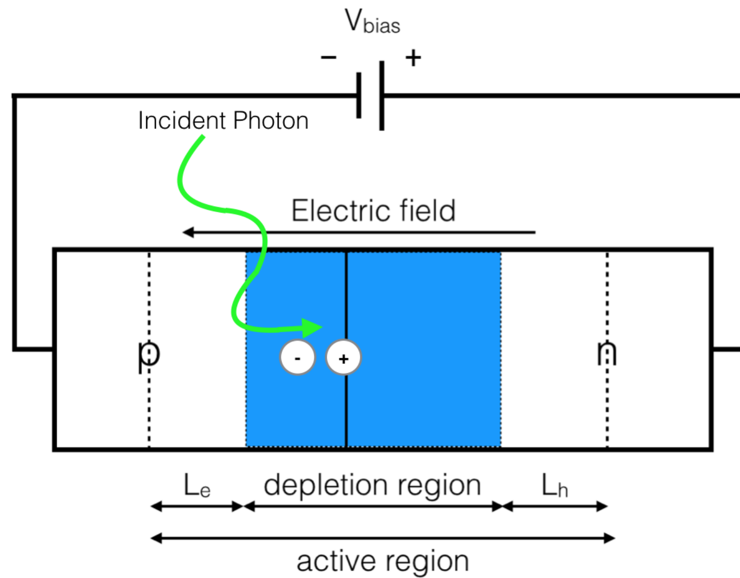


Figure 1.3: A depletion region is formed when a PN junction is reverse biased.

1.2.1.1 Silicon Photodiodes

The most commonly used photosensors in the current consumer market are the p-n, p-intrinsic-n (p-i-n), and pinned photodiodes. These photosensors share the same below-operational principles: doping adjacent regions on a silicon wafer causes a pn junction to form. When the junction is reverse biased, a depletion region forms between the doped sections, preventing the flow of electrons, as Figure 1.3 shows [6]. A photon landing in the depletion region will generate electron-hole pairs. The generated electrons and holes will drift towards the oppositely doped regions because of the reverse-biasing field and will be collected before they can recombine. However, the incoming light photons will only generate electron-hole pairs if they land in the depletion region. With current technology, typical biasing conditions will only create a depletion depth of 1 to 2 µm, which is insufficient to absorb all incoming photons. Photons landing in the doped regions will immediately recombine and, therefore, cannot be collected. Hence, to increase the area for which a photon can strike and free electron-hole pairs, an intrinsic undoped layer must be added between the 2 doped sections, which is the origin of the p-i-n (pin) photodetectors, as Figure 1.4 shows [7].

Both p-n and p-i-n photodiodes suffer from high dark current and have difficulty

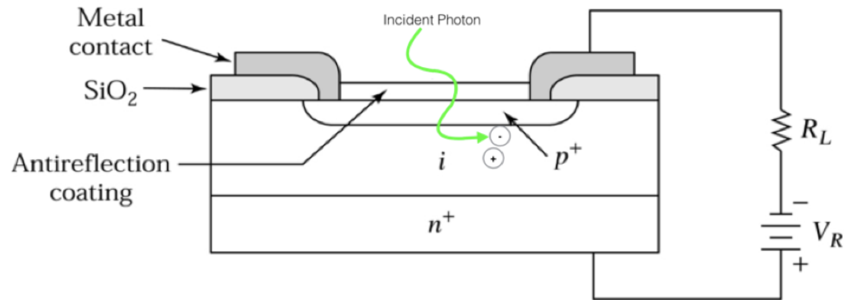


Figure 1.4: Planar diffused p-i-n photodiode.

transferring out all charges collected inside the photodiodes during each reset operation, which is the process of discharging collected charges from photodiodes and readying them to receive more charges. This incomplete charge transfer causes some charges from a previous sampling period to show in the current sample period, creating a lag-like effect. The pinned photodiode, introduced to improve these properties, [8] is a photodiode with an extra-thin p-type implant placed on the other side of the n-type substrate and pinned to a fixed voltage. With this implant in place, two back-to-back diodes are formed when a sufficiently large voltage is applied across the diode. When the depletion region of the two diodes meet, all charges in the photodiode are completely removed, assuming the biasing voltage is high enough.

The dark current in silicon photodiodes is the photodiodes' reverse-biased leakage current. It arises from the mobile charge carriers in both p-type and n-type doped regions tunnelling through the depletion junction region. Therefore, by introducing an intrinsic layer between the two doped areas, p-i-n photodiodes will have lower dark current than traditional p-n photodiodes, but the dark current is still higher than that of a-Se.

1.2.1.2 Amorphous Selenium Photoconductors

Figure 1.5 shows the operational principle of a-Se deposited on a CMOS pixel-array readout IC. When incoming photons strike, they are absorbed within a few tens of µms and will generate a cloud of electron-hole pairs. The cloud size depends on the incident photon energy. With the a-Se biased, the electrons and holes will, following the electrical field within the a-Se, travel to the biased top and bottom electrodes. The top electrode usually provides a positive biasing high voltage, and the bottom electrodes

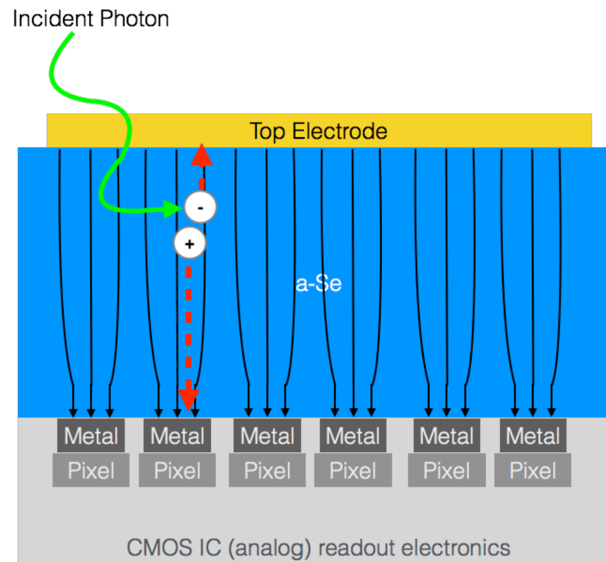


Figure 1.5: a-Se vertically stacked on a CMOS-readout IC

are the exposed metal pads from individual pixels at a lower voltage potential. The metal opening in individual pixels creates a low resistance path to the integration capacitor that allows the photon-generated electrons to be collected at the high-voltage top electrode. The holes will then travel to the closest pixel metal pad and be stored in the integration capacitor. This process is called hole collection. When an incoming photon is absorbed into a-Se, a positive voltage response will result in the corresponding pixel below. Because of the potential difference between the top electrode and the pixel reset voltage, the electrical field inside the a-Se will bend towards each pixel opening, effectively collecting all charges generated inside the photosensor. Holes have higher mobility than electrons in a-Se; therefore, using hole collection will improve the lag performance.

The photosensor's dark current is an important parameter for low-light imaging. Dark current is the photosensor's leakage current under normal operational bias without exposure to any incoming signal. Lower dark current allows a photosensor to produce a recognizable signal from a weaker incoming source. With the silicon bandgap at 1.12 eV and a-Se at 2 eV [12], electrons in silicon photodiodes require less energy than in a-Se to jump from the valence band into the conduction band. With the same thermal energy present, silicon exhibits a higher leakage current, ranging from 1 to 10 nA/cm^2 [9], while a-Se detectors exhibit leakage current less than 0.02 nA/cm^2 [13]. Low dark

current also allows the imager to collect incidental signals (i.e., integrate) for a longer period, thereby collecting a stronger signal (assuming constant incidental flux).

1.2.2 CMOS Readout Electronics

This section will describe some common pixel-electronics designs, as well as the designed imager's basic architecture.

1.2.2.1 Imaging Technology Overview

Low-light performance of standard CMOS imagers has always suffered in comparison to other imaging sensors, including CCD and vacuum-tube imagers [16]. In an ideal imager, the minimum detectible signal should be limited by the photon shot noise generated from the light source. However, the low-light performance in current CMOS imagers featuring p-n, p-i-n, and pinned photodiodes is fundamentally limited by the electronic noise collected during integration.

Alternative low-light imaging systems, such as the high-gain avalanche rushing amorphous photoconductor (HARP), commonly use a-Se as photosensing material. To minimize electronic readout noise, vacuum tubes pick up the signal converted within a-Se [16]. While these imagers perform superbly in the dark, the cost to build and operate them is extremely high.

1.2.2.2 Silicon-Photosensor CMOS Imager vs Hybrid CMOS Imagers

Figure 1.6 shows a standard CMOS-imager layout that incorporates a silicon photodiode and that includes a 3-transistor (3-T) active pixel sensor (APS). Later sections will explain the 3-T APS operation.

Although this APS design is compact, it suffers from a few imperfections. Because the photosensors are coplanar to the readout circuitry, part of the pixel must be dedicated to the readout transistors, meaning the pixel's fill factor is limited. Fill factor is the area of the photosensor divided by the total pixel area. As Figure 1.6 shows, a typical layout with silicon photodiodes can only utilize about 60% of the pixel area. Moreover, since the photodiode sits in the substrate, the routing above the photosensitive area must be minimal, making it difficult to route traces within the pixel array. Since light often needs to penetrate a few nanometers of metals in the routing layer above

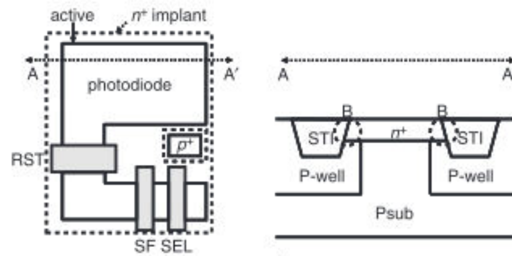


Figure 1.6: 3T pixel layout [17]

the pixel area, the optical tunnels can create a host of undesired optical effects for low-f-number optical systems, including light scattering, vignetting, crosstalk, and diffraction problems [19]. Micro-lenses can be used to guide light onto the photodiodes, but they also add uncertainty and complication during fabrication and operation, including non-uniformity and reflection.

The fill factor is especially important for low-light imaging where the signal is small. This is because the fill factor is directly proportional to the percentage of incoming signals collected. Backside illumination is commonly used to overcome the fill-factor issue. During processing, the silicon wafer is flipped and thinned, allowing light to strike the photodiodes from the backside and thereby prevent signal loss to the routing-metal layers, as Figure 1.7 shows. This process, however, is expensive, and extensive tuning is needed to reduce non-uniformity in the array. Moreover, because of the extra processing steps, the wafer yield also suffers, resulting in a high manufacturing cost of BSI devices.

On the other hand, as Figure 1.5 shows, the performance of a hybrid imager, for which the CMOS-readout electronics are coated with a photosensor (a-Se) for light detection, could be improved under certain situations. This design can improve the imager's low-light performance, as compared to that of imagers using silicon photodiodes, because of the low dark current of a-Se. Moreover, since a-Se has served as a photosensor since the introduction of Xerox photocopiers, its optical properties have been well studied and characterized [20]. Lastly, by using the hybrid-imager structure, the readout electronics and the photodiodes no longer need to be coplanar, which allows IC designers to shrink the pixel pitch or use the space to implement various performance-enhancing circuit designs.

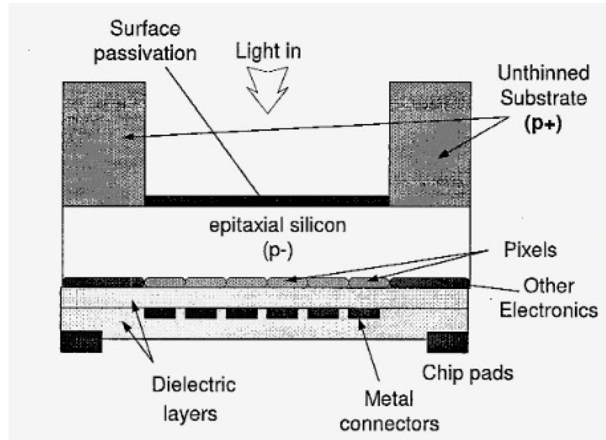


Figure 1.7: Backside illumination cross section schematic [21]

1.3 Performance Metrics

To characterize imager performance, this section will discuss a few characterization parameters commonly used for imagers. These parameters can be used to evaluate both the photosensor and the readout electronics, as well as the imaging system's performance.

1.3.1 Conversion Gain

For all APS circuitries, each positive or negative charge converted from an incoming photon will cause a positive or negative shift in voltage at the integration node once the charge is transferred and stored onto the integration capacitor. The voltage magnitude V_{charge}, induced by the collected charge, is given by

$$V_{charge} = \frac{Q}{C_{int}} \tag{1.1}$$

where Q is the number of electrons or holes (in Coulombs) collected at the integration node and C_{int} is the integration node capacitance.

The conversion gain of imagers targeting low-light conditions should be as high as possible because the readout electronics will sample voltage change caused by incoming photons.

1.3.2 Noise

The readout electronics' noise sets the practical limit on the lower detection boundary, so the noise sources must be identified. The electronics noise can be divided into two categories: temporal noise and spatial fixed-pattern noise. Temporal noise is the variation in a constant signal when taken across multiple points in time. The common types of temporal noise in a 3-T pixel design include

- thermal noise on the integrating capacitor,
- dark current shot noise from some photosensors,
- leakage current shot noise from transistors, and
- flicker noise from in-pixel amplifiers.

Moreover, because of the nature of light, the incoming signal will also have associated shot noise. The signal shot noise will be small compared to electronics noise at low-light levels, but it will become the dominant noise source when the signal is higher.

Fixed-pattern noise is mainly attributed to process-induced variation across the imaging array, such as threshold voltage and source-follower gain offset, as well as column-to-column variation resultant from impedance mismatch. The following chapter will discuss each noise source in detail.

1.3.3 Photon Transfer Curve

The photon transfer curve (PTC) can be used to extract a few key parameters from an imaging system by contrasting the signal and noise at the imager's output. The only noise introduced at the input is the shot noise associated with the incidental signal. Any further discrepancy must be added by the imaging system. The photon shot noise n_{shot} (discussed further in later sections) is given by

$$n_{shot} = \sqrt{N_{sig}} \tag{1.2}$$

where N_{sig} is the number of charges in the incident signal.

Figure 1.8 shows a typical PTC that can be broken down into 3 sections. The first plot section is when the slope is zero, indicating the imager's lower detection boundary.

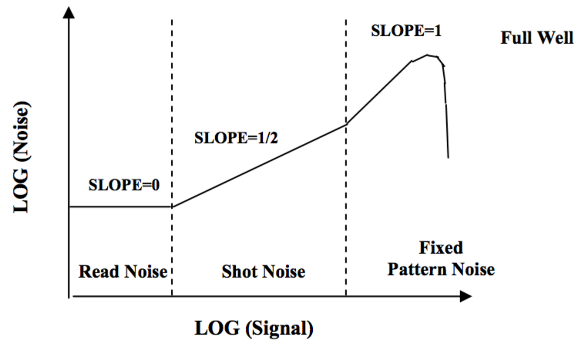


Figure 1.8: Typical photon-transfer curve.

The temporal noise from the readout electronics and the subsequent analog-to-digital conversion circuitry is larger than the incoming signal, meaning signals in this region will be buried by the system noise.

The second section is when the slope is 1/2. Here, the dominating noise is the photon shot noise from the incoming signal. Given that light's shot noise can be modelled with Equation 1.2, when it is plotted on a log-log scale, it will show as a straight line with a slope of 1/2.

The last region can be further broken down into two parts: The first is when the pixel-gain non-uniformity and fixed-pattern noise dominate, and since this non-uniformity is linearly proportional to the incidental signal, the slope during this phase equals to unity. The second is when each pixel reaches its capacity and can, therefore, no longer hold additional charges. When this occurs, the charge will overflow to adjacent pixels, creating an averaging effect that reduces the fixed-pattern noise and photon shot noise. Normally, the fixed-pattern noise can be suppressed using gain and offset correction, therefore extending the shot-noise dominant range all the way to the imager's full-well capacity [25].

1.3.4 Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is a chief metric for image-system characterization and provides the lowest detectable signal, as well as a figure of merit to define when an image is of acceptable quality. The SNR can be calculated by

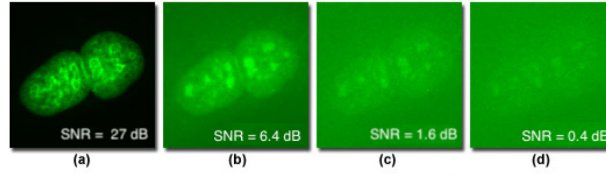


Figure 1.9: Images with ranging SNR.

$$SNR = 10 \times log_{10} \left(\frac{P_{sig}}{P_{noise}} \right) \tag{1.3}$$

where P_{sig} is the power of the incoming signal, and P_{noise} is the image system's noise power at the given signal level. The minimum detectable signal is defined where SNR = 0 dB, while a SNR of 13.97 dB will produce recognizable images based on the Rose criterion [10]. Moreover, based on the ISO 12232 standard [11], a SNR of 20 dB will generate clean and acceptable images, while an SNR of 32 dB will generate images with excellent quality. Figure 1.9 shows images with SNRs ranging from 0.4 dB to 27 dB.

In a digital imager, two major noise sources are the shot noise resultant from undesired leakage current from the photosensor and readout electronics. Since shot noise is the square root of incidental signal, the shot-noise-dominated SNR will grow in a square-root manner with an increasing integration period. Given the leakage shot noises are the dominant noise sources in a digital imager, a longer integration period could produce a higher SNR. Imagers using silicon photodiodes will suffer from the continuous leakage current through both the photosensor and the readout electronics, preventing the CMOS imagers from achieving long integration periods. The shot noise from the dark current of the photosensor and the leakage current of the readout electronics will set a practical lower bound on SNR for a 3-T APS design.

1.3.5 Full-Well Capacity and Dynamic Range

An imager's dynamic range (DR) represents the range of incidental signal that the imager can observe before the pixel capacity is saturated. It can be calculated by

$$DR = 20 log_{10} \left(\frac{N_{sat}}{n_{dark}} \right) \tag{1.4}$$

where N_{sat} is the signal-charge saturation level in number of electrons (also referred to as the pixel full-well capacity) and n_{dark} is the pixel's noise level when no signal is present, usually expressed in root-mean-square (rms) number of electrons [23]. Since most optical-imaging scenarios contain both bright and dark information in a single frame, a high DR is crucial when designing an imager.

The number of electrons N_{sat} that an imager can hold can be calculated using

$$N_{sat} = C_{int} \times \frac{V_{max} - V_{min}}{q} \tag{1.5}$$

where C_{int} is the integration node's capacitance; V_{max} and V_{min} are the maximum and minimum voltages that the readout circuit could extract, respectively, from the pixel; and q is an electron's charge in Coulombs.

1.3.6 Quantum Efficiency

Quantum efficiency characterizes a photosensor's ability to convert incidental photons into electron-hole pairs and is usually expressed as a function of wavelength. An external quantum efficiency (EQE) is the quantum efficiency of an imaging system, accounting for that system's sensory components, including reflection by the top electrode, fill factor, and lenses. Figure 1.10 measures and characterizes the EQEs of a-Se at several wavelengths across various electrical fields, obtained with a HARP camera that employs vacuum pickup tubes as the readout technique, thus greatly limiting the readout electron noise [26]. Note that the EQE increases considerably across the applied electrical fields, possibly because of a stronger electrical field that reduced the energy gap between the valance band and the conduction band in a-Se. The plot also shows that a-Se will have an EQE close to 1 at shorter wavelengths, even with a relatively low bias, which is similar to a p-n photodiode.

When a strong field is present, usually above 80 V/µm, a-Se could enter avalanche mode. In avalanche mode, the initial electron-hole pairs, separated by the energy of incidental photons, will collide with adjacent electron-hole pairs. With a high field present, all the electron-hole pairs in a-Se are already partially energized, and the initial electron-hole pair will set off a chain reaction and create many more electron-hole pairs than normal. Each incoming photon can, therefore, result in an EQE much greater than 1. This is the low-light camera HARP's operational principle [16].

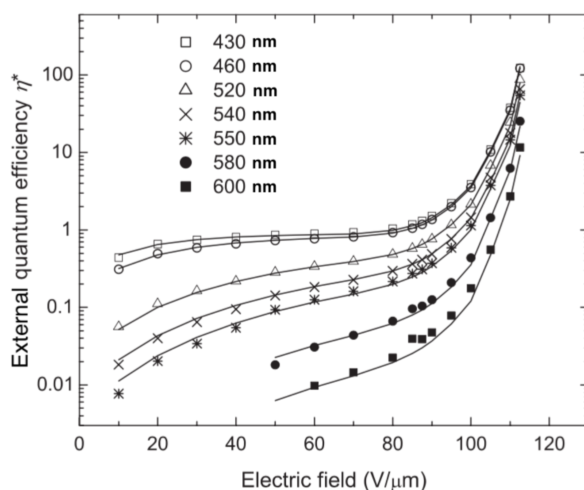


Figure 1.10: Measured a-Se EQE across various electrical fields.

1.4 Motivation and Objective

Most CMOS imagers require specially modified fabrication processes to lower the leakage currents already previously. This process modification, however, leads to high development and manufacture costs. Incorporating analog blocks onto a modified process while maintaining their performance is difficult. Designing a low-light imager that can be made using a standard mixed-signal CMOS process can potentially reduce the cost of such imagers and allow multiple blocks of analog and digital circuitries to be implemented on the same die, achieving a camera-on-chip system.

A-Se has been widely used as a photosensor in commercial products, including photocopiers [20] and high-performance cameras [16]. The STAR group at the University of Waterloo developed the a-Se-deposition process, enabling this work to build a hybrid imager by combining a-Se with a custom-designed CMOS imager. This research project aims to design a CMOS imager that is compatible with the a-Se deposition process and that can take advantage of the low dark current of a-Se photosensor to achieve low-light imaging through long integration.

1.5 Thesis Organization

Chapter 2 will cover more background information necessary to understand this project's design choices. It will focus on the CMOS-readout technologies. It will discuss different circuit structures, common noise sources, and the significance of each in the proposed system. It will then cover a study conducted to evaluate the low-light imaging capability of the proposed hybrid structure using simulated parameters, which are also used to extract the imager design's key-performance specifications.

Chapter 3 will cover the imager's circuit design and simulation results, focusing on the design and modifications made in each quadrant from the standard 3-T voltage-mode APS, as well as other on-chip components, including the analog buffer and the bond pads. This chapter also describes the external software and hardware built to control the imager.

Chapter 4 will cover the electrical and optical experiment setups and the imaging system results. The results will be compared to the design targets and simulation results, with comments and discussions on the discrepancies between them.

Chapter 5 will discuss the conclusions drawn from the experiments and compares this work with a few other recent works that target low-light imaging. It will also discuss future works that could improve the imager's performance.

Chapter 2

Background and Feasibility Study

This chapter will cover necessary background information and the feasibility of achieving low-light imaging using the hybrid image structure. Topics discussed include common pixel structures, noise sources, and a performance-simulation study based on estimated imaging conditions. The simulation will explore the feasibility of designing an a-Se-CMOS-hybrid imager that can achieve the desired performance under low-light conditions.

2.1 CMOS Pixel Architecture

All CMOS pixel architectures can be split into 2 categories: passive and active pixel sensors (PPSs and APSs). This section will cover both designs, discussing, in detail, the advantages and disadvantages of each.

2.1.1 Passive Pixel Sensors

Figure 2.1 shows the schematic of a typical PPS with its readout circuit. Each PPS contains a photosensor (like the photodiode shown in Figure 2.1). Using the single transistor as an on-off switch, it will allow the charge integrated on the pixel capacitor C_{pixel} to be transferred to a column capacitor C_L. The charge amplifier will then sample the integrated signal and pass it down the readout path for digitization.

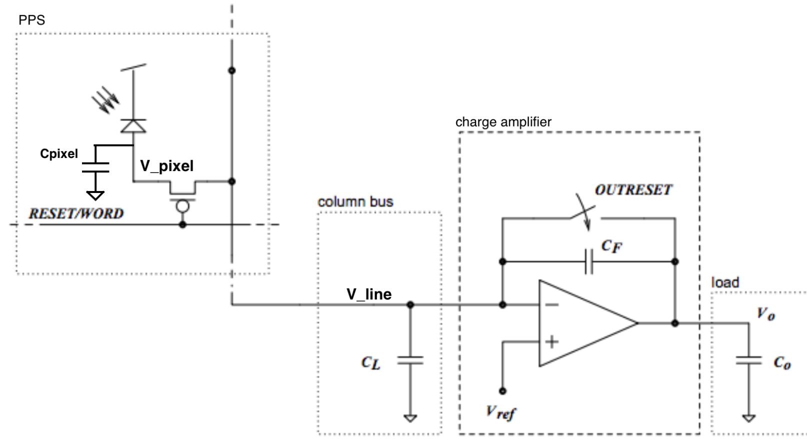


Figure 2.1: PPS with charge amplifier readout circuit [29].

The PPS's main advantage is its compactness, due to its simplicity. PPS can be used to implement an array with a high-fill factor and high resolution. However, it lacks performance in SNR because of its large-column capacitor-incurred kTC noise which cannot be kept small in a reasonably-sized imaging array. Moreover, the charge-sharing mechanism used between the pixel V_{pixel} and the column capacitor V_{line} in steady state is governed by

$$V_{line} = \frac{C_{pixel}}{C_{pixel} + C_L} \times V_{pixel} \tag{2.1}$$

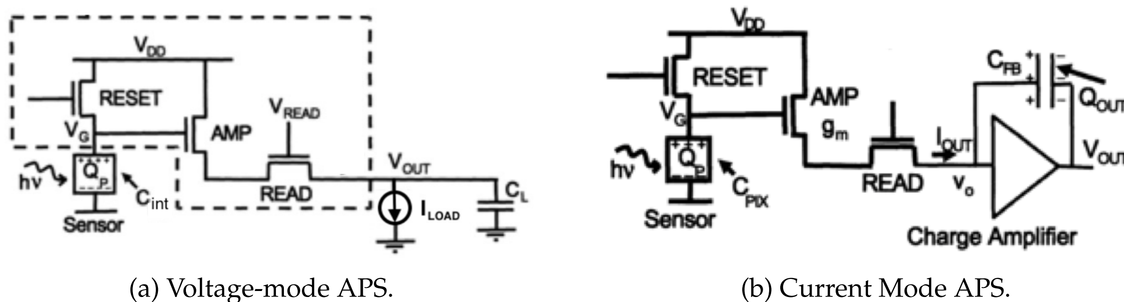
where C_{pixel} is the capacitance of the photosensor and the integration capacitor in each pixel, and C_L is the column line capacitance. The column capacitance needs to be kept small small, as compared to the pixel capacitance, for an efficient readout. Therefore, PPS also lacks scalability. At the same time, the charge-sharing process's duration follows the column capacitor's RC-time constant and the pixel's output resistance, which limits the design's readout speed.

2.1.2 Active Pixel Sensors

The key difference between the PPS and APS design is the use of an amplifier inside each pixel. This section will discuss two common APS designs.

2.1.2.1 Three Transistor (3-T) APS

APSs can be implemented with at least 3 transistors. Figure 2.2 shows the voltage-mode APS and the current-mode APS [22]. In both designs, the first transistor is a reset device that sets the integration node's voltage to a user-defined potential that will ready the pixel to integrate more incoming charges. The second device is an amplifier (AMP) MOSFET acting as either a source follower that buffers the integrated voltage in voltage mode or a transconductance amplifier that converts integrated charge into a current in current mode. The last transistor is a row-select read (READ) device that connects the pixel to a column bus. Later sections will explain the array structure and timing.



(a) Voltage-mode APS. (b) Current Mode APS.

Figure 2.2: Schematic of voltage and current mode APS.

During normal mode of operation, both 3-T APSs will operate in 3 modes (as shown in the Figure 2.3 timing diagram):

1. Reset: The reset transistor is turned on, allowing the integration node to be reset to V_{DD}, assuming the pixel is performing electron collection.

2. Integration: The reset transistor is turned off, and the charge generated within the photosensor will be collected at the integration node.

3. Readout: Once the pixel has integrated for a user-defined period, the READ transistor will turn on, connecting the AMP device's source to a current load in voltage-mode or a charge amplifier in current-mode.

Comparison of the two operational modes shows voltage mode has a clear speed advantage when implemented in a large array. Since current-mode APS requires the

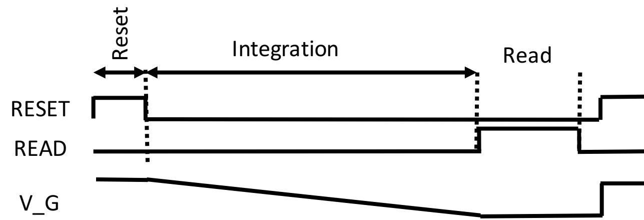


Figure 2.3: Timing diagram of 3T voltage-mode APS.

AMP device to be biased in the linear region, the current-mode AMP will carry a smaller current for the same-sized AMP in voltage mode. In a large imager array, the column-bus capacitance will be large as well, meaning the voltage-mode APS will be able to charge the column capacitance faster than the current-mode APS and, thus, operate at a higher speed.

The APS design boasts another advantage, as compared to PPS: by isolating the pixel capacitance from the column line through an active device, the charge collected during integration does not need to be shared with the column capacitance. This means that the readout speed and the scalability can be greatly increased, and the pixel read operation becomes non-destructive. This importantly allows the collected data to be read multiple times as needed, enabling more advanced and sophisticated sampling methods, such as the correlated double-sampling technique. The 3-T design, however, often suffers from image lag, an effect caused by incomplete reset of the photodiode between adjacent integration periods, and thermal noise. Hence, the introduced 4-transistor (4-T) design minimizes noise and is commonly used with the pinned photodiode to eliminate lag.

2.1.2.2 Four Transistor (4-T) APS

The 4-T APS design aims to remove most electrical noises produced in a 3-T design by introducing a transfer gate (TG) between the photodiode and the integration node, as Figure 2.4 shows. By adding the TG device, the 4-T design enables the correlated double-sampling technique (CDS), which can remove most reset thermal noise caused by each reset operation. Moreover, the extremely short time between the 2 samples, usually on the order of a few µs, significantly reduces the leakage-current shot noise's impact from other devices. An a-Se photosensor, however, operates differently from a typical silicon photodiode because the a-Se is unable to provide a large capacitance to hold the integrated charge. The imager must rely on an explicit capacitor inside

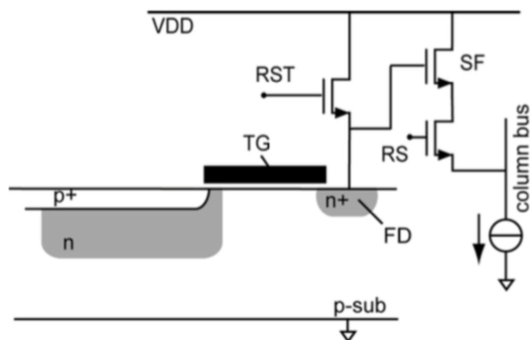


Figure 2.4: Schematic of a 4-T pinned APS [23]

the pixel, which would increase the pixel pitch's minimum size. Moreover, for CDS to occur, the time between the 2 samples must be sufficiently short so that the noise in both samples can be correlated. This timing cannot be achieved with the previous design and is difficult to achieve with the digital control circuitry considered for this design [2].

The other advantage of a 4-T design is the high conversion gain it provides. A floating diffusion (FD), as Figure 2.4 shows, can be made small. Hence, when the TG gate turns on, the charge-sharing action between the large photodiode capacitance and the FD results in a high conversion gain. A similar design can be created with a 3-T-a-Se hybrid pixel, since a-Se has a much lower capacitance than a photodiode.

2.2 Noise

As the previous chapter mentions, the low-light performance of CMOS imagers is fundamentally limited by noise in the readout system. In an ideal noise-free imager, the shot noise from the incoming light should be the dominant noise source. Improving the lower boundary of detection in an imaging system can be achieved by improving SNR at lower input levels. This can be done through a few methods, including by increasing the signal conversion gain and decreasing the readout electronic noise. In the case of static imaging, for which the frame rate is not a major concern, an extended integration period can improve SNR when the signal is low. The following section will discuss the mechanism and sources of common noise in imagers.

2.2.1 Temporal Noise

Temporal noise is the variation and uncertainty of a constant signal when sampled at different times. It is a limiting factor of CMOS-imager performance and is contributed to by both photosensors and readout electronics. This section discusses the major temporal noise sources and their mechanisms.

2.2.1.1 Photon Shot Noise

Photon shot noise is the fundamental noise generated by the light source. Assuming the light source's flux is perfectly uniform and constant, the incoming photons' arrival follows the Poisson distribution. This distribution's standard variation is simply the square root of the incoming photons, as Equation 1.2 shows.

2.2.1.2 Dark Current Shot Noise (DCSN)

The same principle of photon shot noise also applies to the pixel's dark current and leakage current. The leakage current in a 3-T design comes from both the reset device operating in the subthreshold region during integration and the protection diodes that prevent the source follower's gate from over charging. The photosensor also produces dark current, which in some cases can produce shot noise. The dark-current shot noise n_{DCSN} in electrons rms is given by

$$n_{DCSN} = \sqrt{\frac{\frac{I_{sLeak}+I_{eLeak}}{q}}{FrameRate}} \tag{2.2}$$

where q is the charge of a single electron (1.602 x 10 $^{-19}$ C), I_{sLeak} is the photonsensor's leakage, I_{eLeak} is the CMOS electronics' leakage current, and frame rate is the integration time's inverse, defined in frames per second (fps).

2.2.1.3 Thermal Noise

In conventional resistive conductors, electrons will have randomness in their motion resultant from the ambient environment's thermal energy. In an APS pixel design, the reset transistor, which can be modelled as a resistor during reset, is responsible for setting the voltage on the integration capacitor. At the end of each integration, the number

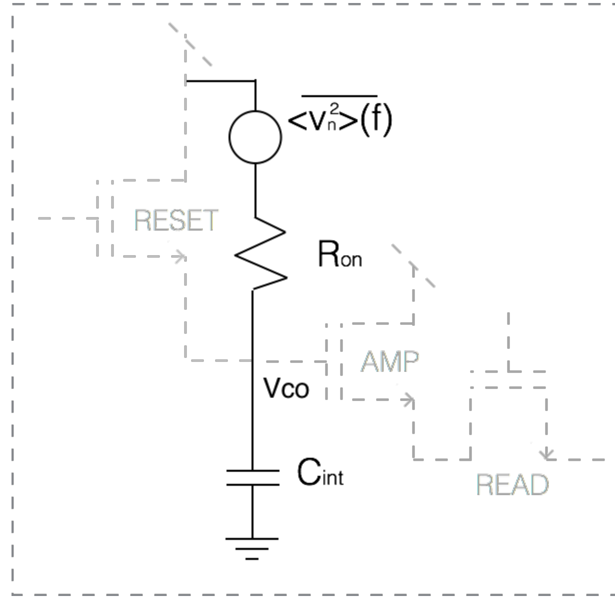


Figure 2.5: Thermal noise schematic for reset operation in 3-T pixel.

of electrons stored on the integration capacitor could vary based on the capacitor's size and the ambient temperature. Figure 2.5 shows a simple schematic that represents the reset operation. The thermal noise, here, is modelled as a voltage source with the noise-voltage-power spectral density V_n^2 in series with the reset transistor resistance R_{ON}.

The noise voltage power spectral density $V_n^2(f)$ is defined by

$$V_n^2(f) = 4kTR_{ON} \tag{2.3}$$

where k is Boltzmann's constant and R_{ON} is the on resistance of the reset transistor in the linear region. The resistor's impedance and the capacitor form a voltage-divider network; therefore, the noise voltage V_{co} across the integration capacitor represents the noise seen by the pixel at the integration node.

To apply the transfer function to the noise power, the transfer function's magnitude square $|H(f)|^2$ must be used. With the noise voltage across the capacitor given by

$$V_{c_o}^2(f) = V_n^2 \times |H(f)|^2 = \frac{1}{1 + 4\pi^2 R_{ON}^2 C_{int}^2 f^2} \times 4kTR_{ON} \tag{2.4}$$

the average noise power is given by

$$V_{c_o}^2 = \frac{kT}{C_{int}} \tag{2.5}$$

Notably, the result is not dependent on the resistance. Equation 2.6 shows the thermal noise n_e^- in terms of electrons rms

$$n_e^- = \frac{\sqrt{kTC_{int}}}{q} \tag{2.6}$$

As the equation shows, a smaller capacitor and a lower operating temperature will reduce thermal noise. Many existing low-light, high-performance imaging systems are often cooled to reduce thermal noise. However, since a-Se can delaminate at low temperatures, this method is not suitable for the proposed hybrid structure. As discussed and as Equation 1.1 states, an imager's conversion gain is inverse proportional to the integration capacitance. A smaller capacitor will, therefore, increase the amplification of incoming photons while the thermal noise increases by $\sqrt{C_{int}}$. Hence, in a thermal-noise-dominant system, the SNR will increase proportionally with $\sqrt{C_{int}}$.

2.2.1.4 Flicker Noise

Two theories used to explain flicker noise are McWhorter's theory and Hooge's hypothesis. In McWhorter's theory, flicker noise is caused by the trapping and detrapping of charges in the oxide traps near the Si-O_2 interface [31] and is inversely proportional to $C_{ox}{}^2$ (gate-oxide capacitance). In the bulk mobility fluctuation theory, based on Hooge's hypothesis, flicker noise is inversely proportional to C_{ox}. A unified model for flicker noise PSD $V_{n_o}^2(f)$ was presented previously [32], but because of the model's complexity, the following simplified version, is often used [33]:

$$V_{n_o}^2(f) = \frac{K}{C_{OX}WL} \times \frac{1}{f} \tag{2.7}$$

where W and L are the width and length of the transistor, and K is a process-dependent technology parameter usually extracted from wafer measurements.

Given that flicker noise's upper and lower frequency boundaries are set by component characteristics inside the system, Equation 2.8 can be used to calculate the total flicker noise $V_{n_o}^2$ in the system:

$$V_{n_o}^2 = \frac{K}{C_{OX}WL} \times \int_{f_{low}}^{f_{high}} \frac{1}{f} df = \frac{K}{C_{OX}WL} \times ln\left(\frac{f_{high}}{f_{low}}\right) \quad (2.8)$$

f_{low} represents the equivalent frequency of longest continuous operation and f_{high} is the device's upper cut-off frequency, usually defined by a low-pass filter on the readout path.

2.2.2 Spatial Noise

Spatial noise is the variation across the imaging array at one time and will be discussed in this section.

2.2.2.1 Under Dark Condition

When no signal is reaching the imaging array, the main variation across each pixel is caused by the device mismatch and fabrication-process imperfection. On the pixel level, the difference between device sizes could cause a mismatch in gate-source voltage, especially when all pixels are exposed to the same biasing current during readout. The difference in oxide thickness could affect the source follower's threshold voltage. The inconsistency in doping and temperature across the wafer could also affect the devices' leakage current. On the array level, since each pixel column shares a common readout-selection circuitry, the mismatch between the devices from column to column will generate a different output across the array. However, since the aforementioned variations have no temporal dependency, they are referred to as fixed-pattern noise.

2.2.2.2 Under Illumination

When the imaging array is exposed to a light source, each pixel could respond differently even if the incoming signal is perfectly uniform across the entire array. Since the charge is converted into voltage and then buffered through the AMP device for readout, as Figure 2.2 shows, the conversion gain will differ across the array. Moreover, since the buffered signal through the AMP device is a function of the transconductance g_m in both the voltage and current modes, the difference in g_m will cause each pixel's gain to vary.

Fortunately, digital processing can largely suppress fixed-pattern noise. A gain table can be created by exposing the imager to a known uniform flux, and an offset table can be obtained by taking an image in complete darkness then subtracting the dark frame from the actual image output.

2.3 Feasibility Study

Supported by previous noise discussion and key electrical measurements, including the subthreshold leakage current collected from previous works [2], we performed simulations to explore the performance limitations of an a-Se/CMOS low-light imaging system. This study will focus on the 3-T voltage-mode APS, which should provide better noise performance than a PPS design and faster readout than a current-mode APS.

The main electrical noise contributors in a 3-T voltage-mode APS are the reset operation's thermal noise, leakage-current shot noise from the reset transistor operating in subthreshold conduction during integration, and the source follower's flicker noise. An imager's SNR is calculated with different control parameters, including pixel capacitance, pixel pitch, and across low-light luminance levels.

An important advantage of using a hybrid-imager structure is that the pixel pitch is not limited by the photodiode in each pixel. Instead, various performance-enhancing circuits can be implemented to achieve better image quality while enabling the possibility of a high-resolution imager to be built.

To determine whether a standard mixed-signal CMOS process and a typical 3-T design could provide the performance needed to take advantage of a-Se, we performed calculations and simulations to quantify and to help us understand the impact of the parameters that can be controlled throughout the design process. To show a low-light-capable imaging system, we chose a target SNR of 20 dB at 0.01 lux, which is starlight-level illuminance, for this study to create design margins.

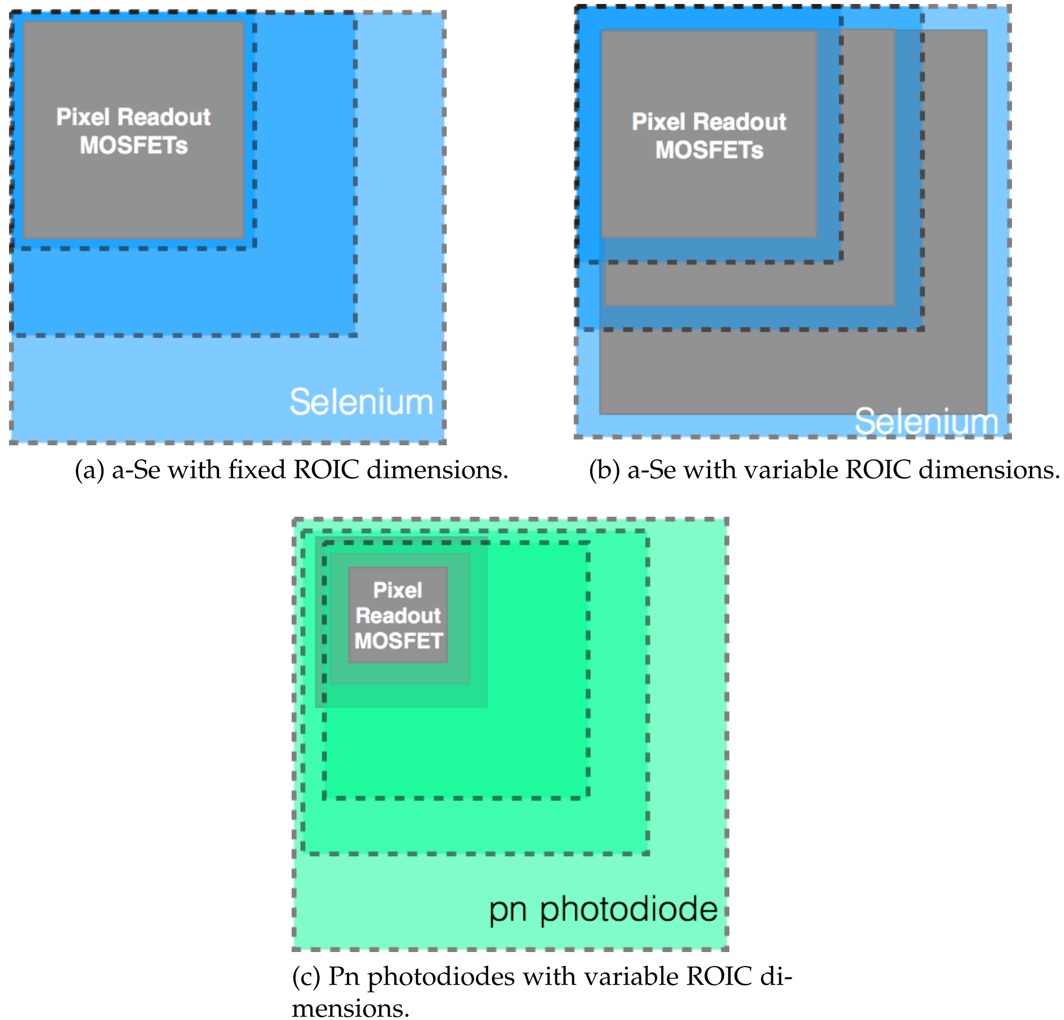
2.3.1 Pixel Architecture Setup

This section compares three configurations under different illuminances and pixel pitches. To achieve the high sensitivity desired for low-light imaging and inspired by the 4-T APS design, we assumed all configurations to use the parasitic capacitance of the devices connected to the integration node as the integration capacitor. The three configu-

rations we studied include 2 hybrid a-Se-CMOS configurations and a p-n photodiode-CMOS pixel design. The simulation setups of each model are as follows:

1. A-Se with fixed-size-of-pixel-readout MOSFETs, as Figure 2.6a shows, where the pixel pitch is varied, while the readout-integrated-circuit (ROIC) transistors are kept constant at the minimum size; any increase in integration capacitance will result from the photosensor
2. A-Se with scalable-size-of-pixel-readout MOSFETs, as Figure 2.6b shows, where the pixel pitch is varied, while the readout transistors are sized accordingly; both the photosensor and the larger transistors will increase the integration capacitance
3. A P-N photodiode with scalable-size-of-pixel-readout MOSFETs, as Figure 2.6c shows, where the photodiode size is varied and the readout transistors are sized accordingly; both the photosensor and the larger transistors will increase the integration capacitance

The significance of these three models are described below.



(a) a-Se with fixed ROIC dimensions.

(b) a-Se with variable ROIC dimensions.

(c) Pn photodiodes with variable ROIC dimensions.

Figure 2.6: Simulated pixel structures.

2.3.1.1 A-Se Photosensors

The first two models emphasize the performance of a-Se as a photosensor, while studying the impact of the readout transistor sizing on overall imager SNR. The MOSFET devices' parasitic capacitances were simulated through Spectre^{TM} using TSMC's CMOSP18 parameters. We calculated the capacitance added by a-Se C_{Se} assuming a thickness of roughly 10 µm. It can be estimated with Equation 2.9.

$$C_{Se} = \frac{\epsilon_0 \times \epsilon_r}{d} \quad [F/m^2] \tag{2.9}$$

where ε_0 is the permittivity of freespace, 8.84 x 10^{-12} F/m, ε_r is the dielectric constant of selenium (7.39) [18] and d is the thickness of the dielectric material, in this case the thickness of a-Se which is assumed to be 10 µm. We calculated a-Se's parasitic capacitance as 6.5 aF/µm^2, much smaller than the parasitic capacitance added by the MOSFETs. The first architecture minimizes the pixel's integration capacitance, therefore improving SNR in a thermal-noise-dominated system. The second architecture focuses on minimizing leakage current from the reset device and the protection diode, using longer-channel devices as the pixel pitch increases.

2.3.1.2 Silicon Photodiode

The third simulation configuration assumed a p-n photodiode as the photosensor, hence the hybrid imager's performance can be compared to traditional silicon photodiode designs. We extracted the p-n photodiode's capacitance from a series of CMOS-imager data sheets from ON Semi [27] [28], which had a unit capacitance of 0.86fF/µm^2, 2 orders of magnitude higher than the a-Se photosensor's.

2.3.2 Simulated Imager Performance

This section discusses the noise analysis setup and results from various simulations.

2.3.2.1 Simulation Setup

To study and predict the imagers' performances, the simulation model includes the following control parameters to mimic operation of the imaging operations, as Table 2.1 summarizes.

We first simulated the system in Excel and later imported the simulation into MATLAB for versatile control and easier parameter sweeps. Table 2.2 summarizes the equations and parameters used during simulation and shows their relationship with other system parameters, including pixel size, signal level, and integration period. For ease of calculation, we assumed a monochromatic source that generates photons with a wavelength of 450 nm. With the assumed quantum efficiency of 1, each incoming photon

Table 2.1: Simulation control parameters.

Parameters	Range	Comment
Illuminance	0.01 - 1 lux	Brightness observed by the imager
a-Se biasing voltage	40 V/µm	40 V/µm should provide a quantum efficiency close to 1 for shorter wavelengths (430 nm - 460 nm).
Wavelength	440 - 550 nm	To account for the non-uniform quantum efficiency of a-Se, longer wavelengths are omitted due to a-Se's low QE for red light.
Temperature	300 K	
Frame rate	10 - 0.3 frames per second	To study the effect of read-out speed and different integration periods on system noise and performance

will generate 1 electron-hole pair. Also, to show the impact of integration capacitance on SNR in each setup, all results are shown in V_{rms}.

The universal parameters used in the table are C_{int}, the integration capacitance in Farads, and A, the area of the pixel in µm^2.

Table 2.2: Equations used in performance simulation.

	Equation	Constants & parameters
Signal Shot Noise	$V_{SSN} = \frac{q}{C}\sqrt{\mathrm{N_{sig}}}\ \mathrm{A}$	N_{sig} = number of incoming photons
Reset Thermal Noise (kTC)	$V_{kTC} = \sqrt{\frac{kT}{C}}$	k is Boltzmann constant T = 300K, room temperature
Leakage Current Shot Noise	$V_{LCSN} = \frac{I_{\mathrm{CMOSLeak}}}{C \times FrameRate}$	$I_{CMOSLeak}$ CMOS reset device leakage current

Since the flicker noise was calculated to be less than 2 electrons with parameters extracted from previously built prototype [2], we ignored it in the following analysis for the sake of simplicity.

2.3.2.2 Results and Discussion

A key parameter that defines an imager's low-light capability is its noise floor. Lower noise floor will allow the detector to have a better SNR when the signal is weak. As previously stated, the three major noise sources are

- photon shot noise from the signal
- reset kTC noise
- leakage-current shot noise from the reset device

Figure 2.7 shows a breakdown of noise contribution for the 3 structures under study. For the simulation, we assumed an integration time of 2.5 frames per second and an illuminance of 0.01 lux. We extracted the leakage current from a previous 5 µm x 5 µm pixel layout and scaled for smaller designs. We assumed the leakage current is inversely proportional to the MOSFET W/L ratio. We chose the pixel-size range because the smallest pixel that can be achieved in the targeted 180-nm CMOS technology is roughly 4 µm x 4 µm. The 8 µm x 8 µm upper bound is defined through numerous simulations.

As the figure shows, all structures' dominant noise sources are the MOSFETs' leakage current shot noise and the reset operation's thermal noise. Further examination showed that photodiode structure always suffers from higher kTC noise and dark current shot noise. This is partially caused by the large capacitance added by the photodiodes. Therefore, a-Se can be said to provide superior noise performance in low-light conditions as compared to traditional p-n junction photodiodes.

2.3.2.2.1 Effect of Integration Capacitance on SNR Comparison of the two a-Se architectures demonstrates that the MOSFET leakage current is the dominating noise factor at smaller pixel pitches. However, as the pixel size increases, the reset device's channel increases too, resulting in a linear reduction in leakage current. Furthermore, with a bigger pixel pitch, more advanced circuit techniques, such as reset-device series stacking, can be used to effectively reduce the leakage current by up to an order of magnitude. As Figure 2.7 shows, as the pixel pitch increases, the overall noise decreases though the kTC noise increases because of additional capacitance added by bigger MOSFETs. Therefore, to optimize the imager for low-light performance, the leakage current from the pixel electronics and the photosensor must be minimized.

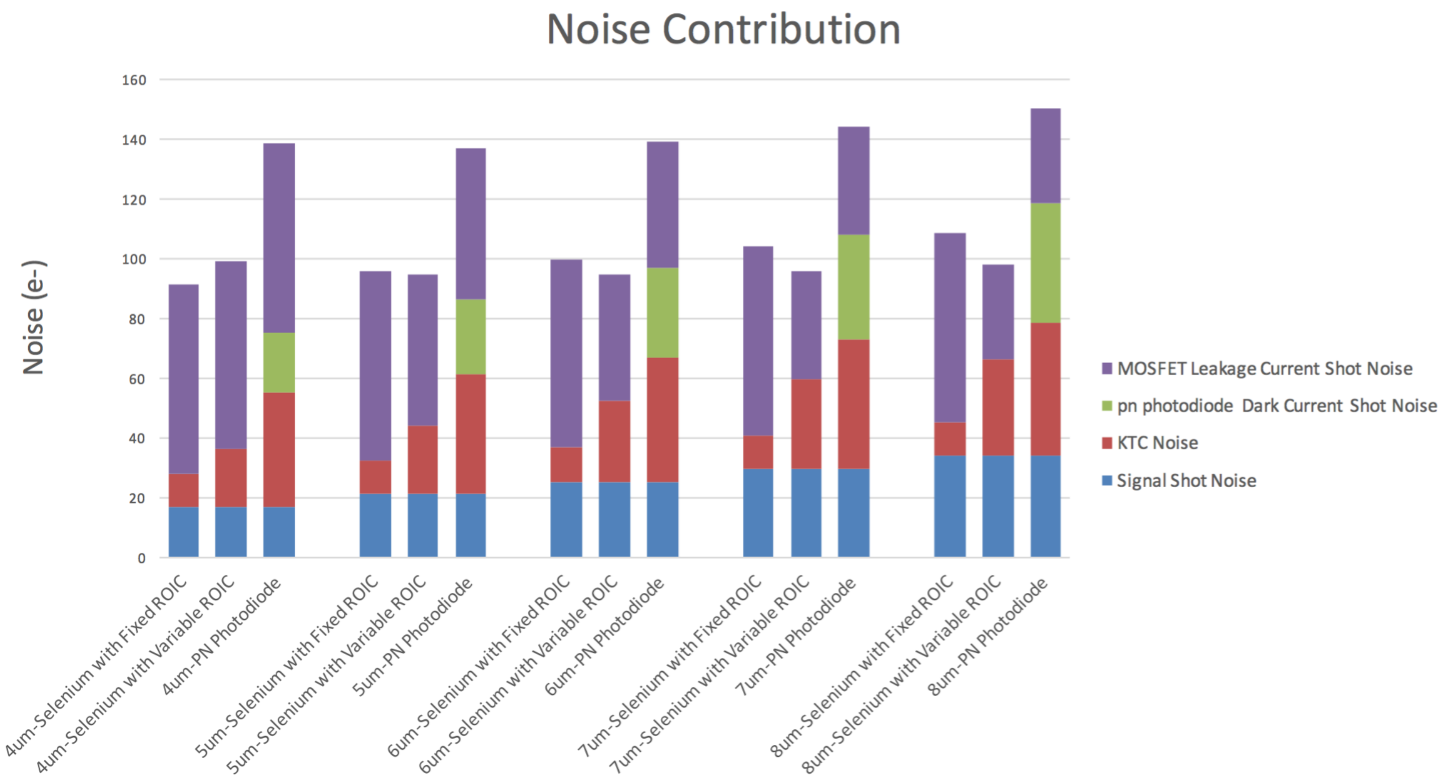


Figure 2.7: Noise contribution summary at 0.01 Lux and 400 ms integration.

Since the imager's DR is not a primary design target, small integration capacitance is tolerable for this design. Also knowing that thermal kTC noise is one of the dominant noise sources in the readout electronics [2] , the SNR due to kTC noise only is given by

$$SNR_{kTC} = \frac{\frac{q_{sig}}{C_{int}}}{\sqrt{\frac{kT}{C_{int}}}} = \frac{q_{sig}}{\sqrt{kT}\sqrt{C_{int}}} \tag{2.10}$$

which shows SNR is inversely proportional to the integration capacitance's square root. Therefore, a lower capacitance value can provide better SNR. Moreover, with the pixel's conversion gain inversely proportional to the integration capacitance, a smaller capacitance will also allow an incoming photon to be converted to a higher voltage.

2.3.2.2.2 Effect of Integration Period on SNR Increasing the integration period will also improve SNR in low-light conditions. Knowing that the thermal-noise magnitude is not time dependent and that the photosensor and readout electronics' shot noise increases as a square root of time while the signal collected increases linearly, the SNR could benefit greatly from a longer integration period. The SNR assuming dark current shot noise is the dominate noise source is given by

$$SNR_{shot} = \frac{q_{sig} \times \sqrt{T_{int}}}{\sqrt{q_{sig}}} \tag{2.11}$$

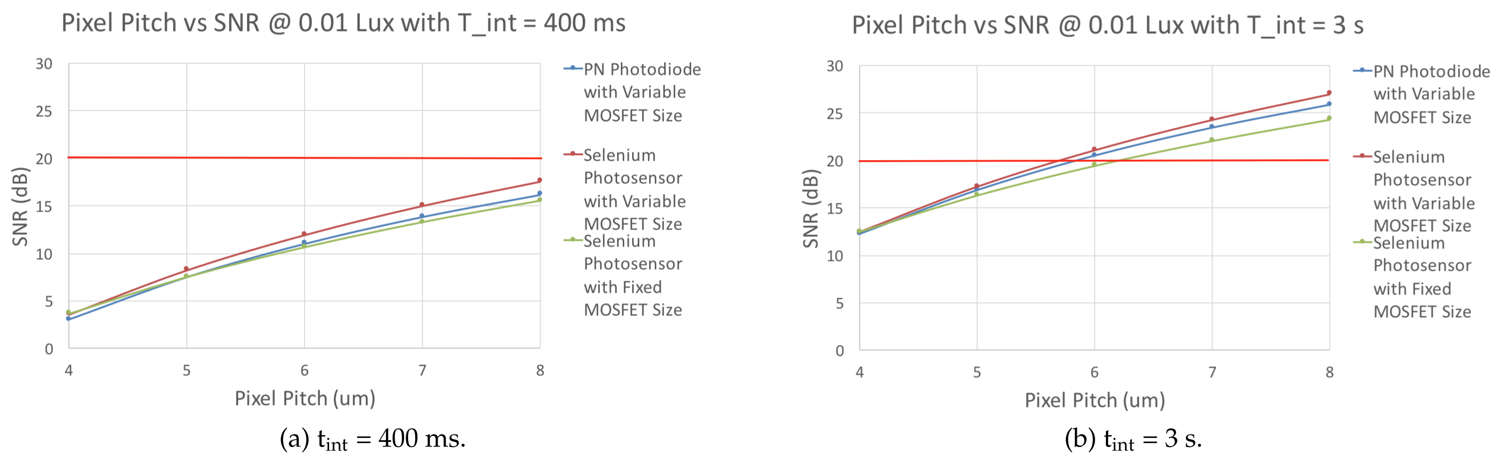
where T_{int} is the imager's integration time of the imager. Figure 2.8 shows the resulting SNR after 0.4 seconds and 3 seconds of integration.

Equation 2.11 and Figure 2.8 show that all designs' SNRs can benefit greatly from having a longer integration period. All 3 architectures had an SNR close to 1 at 400 ms of integration period, but with 3 s of integration all SNRs increased by more than an order of magnitude. However, the advantage of using a-Se is still not obvious. Because of the high leakage current assumed in the pixel design, its dominating noise level has drowned out the benefit of a-Se. Figure 2.9 shows the same simulation repeated with the reset device's leakage current dropped from 4 fA to 1 fA.

This second simulation set illustrates an advantage of using the hybrid structure: with a-Se's low dark current, given the MOSFET's leakage-current shot noise is not the dominating noise source, the same readout electronics will provide better SNR for a-Se detectors. Moreover, both a-Se hybrid structures can achieve an SNR of 20 dB at 0.4 s of

integration when the pixel pitch is above 7.5 µm, while almost all pixel sizes can result in an SNR greater than 20 dB when the integration time is increased to 3 s.

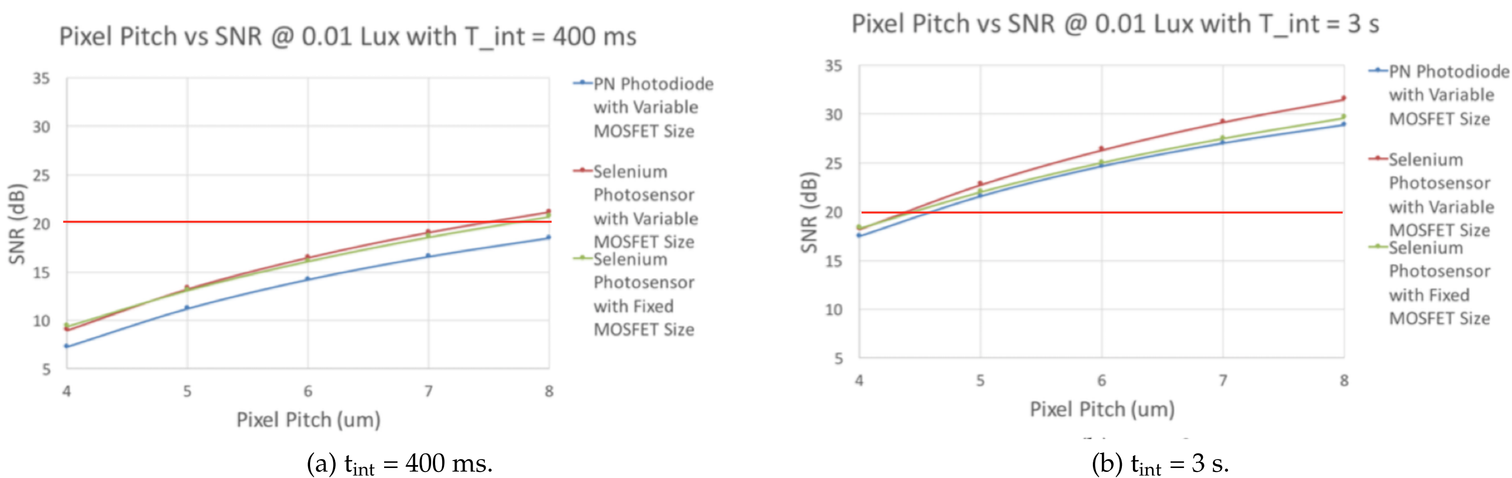
In conclusion, an imager that has a small integration capacitance and can perform long integration for low-light imaging is desirable. Suppressing the readout electronics' leakage current and the photosensor's dark current are key to demonstrating the benefit of a-Se sensors with long integration time. From the SNR simulation, to illustrate the advantages of the hybrid structure, the leakage current must be minimized.



(a) t_{int} = 400 ms.

(b) t_{int} = 3 s.

Figure 2.8: Pixel pitch vs SNR at 0.01 Lux with I_{leak} = 4fA, with red line indicating the target SNR.



(a) t_{int} = 400 ms.

(b) t_{int} = 3 s.

Figure 2.9: Pixel pitch vs SNR at 0.01 Lux with I_{leak} = 1 fA, with red line indicating the target SNR.

Chapter 3

Design

This chapter will discuss, in detail, the imaging system's design. Figure 3.1 shows the system's top-level block diagram, which consists of 3 major blocks:

- A CMOS imager, which uses a-Se as the photosensor
- A custom PCB and a custom FPGA, which are used to digitize analog data coming off the imager and also act as the bridge between the software-generated control signals and the chip
- Control software, which is responsible for generating the initialization indicator signals, monitoring the FPGA's status, reading the FPGA memory block's data, and saving the data locally for post-processing.

MATLAB scripts then parse the saved data and reconstruct the serial output into recognizable image formats.

3.1 CMOS Imager Design

This section describes the CMOS imager's design, including all 4 quadrants, the digital control circuitry, and the on-chip buffer.

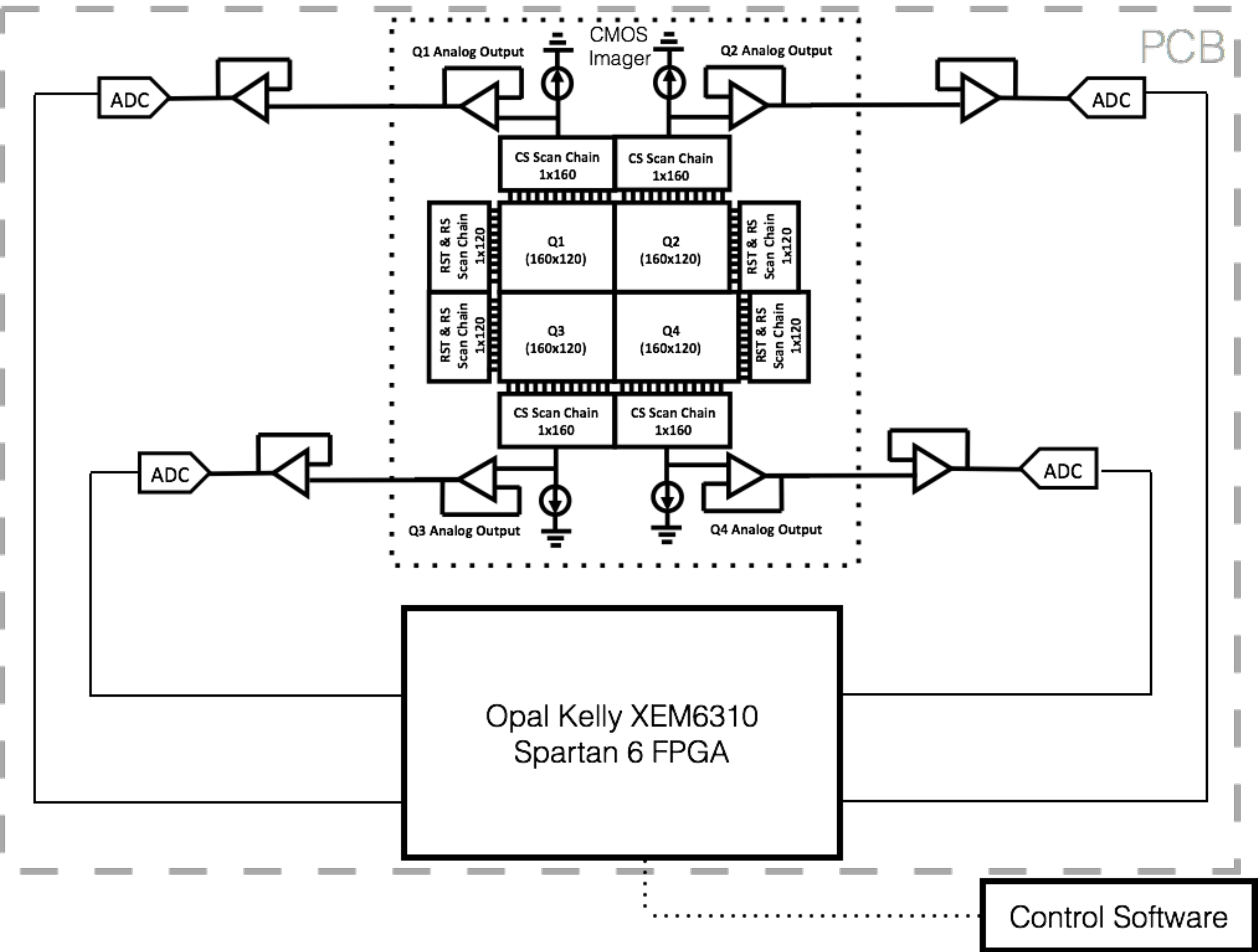


Figure 3.1: Block diagram of imaging system.

3.1.1 Pixel Array

The a-Se photosensor's low dark current enables the system to have extended integration time, providing a significant static-imaging advantage as compared to silicon photodiodes. To take advantage of this material characteristic, the CMOS-readout circuits' leakage current needs to be minimized. A minimum-sized device's leakage current, for the 180-nm CMOS mixed-signal process used to fabricate this hybrid imager, is on the order of 100 fA to 1 pA. This means that to utilize a-Se's low dark current, the reset device's leakage current and the protection diodes need to be suppressed by employing the circuit techniques discussed in this chapter. The CMOS imager contains 4 experimental designs, all of which are variations of the 3-T voltage-mode APS. Each array contains 160 x 120 pixels and each quadrant includes a different modification that explores the performance of various circuit techniques. We studied and compared, between quadrant 1 (Q1) and Q2, the effects of leakage and charge-injection suppression circuitry. This chapter will study the difference in kTC noise and leakage-current shot noise induced by NMOS and PMOS reset transistors by comparing Q2 and Q3. Q4 is an experimental design in which a secondary metal-insulator-metal (MIM) capacitor can be connected to the integration node, forming a dual dynamic-range pixel architecture. This chapter will describe, in detail, each quadrant's design.

3.1.2 Pixel Design

This section discusses the detailed design, operation, and performance of all four quadrants. To maximize the imager's DR, all MOSFETs and diodes used in the design hybrid imager are 3.3 V-rated devices, which means the transistors could operate up to a gate voltage of 3.3 V, instead of the normal 1.8 V.

3.1.2.1 Quadrant 1 (Q1)

As Figure 3.2 shows, Q1 is like a typical 3-T voltage-mode APS but with 4 major modifications: stacked reset devices, protection diodes, a low-Vt-source follower, and a passgate as row-select logic. This section will discuss the effect and reason for these modifications. Table 3.1 lists the device sizes. The pixel V_{out} output during readout is defined by

$$V_{out} = V_{in} - V_{GS_{SF}} - V_{DS_{RS}} \tag{3.1}$$

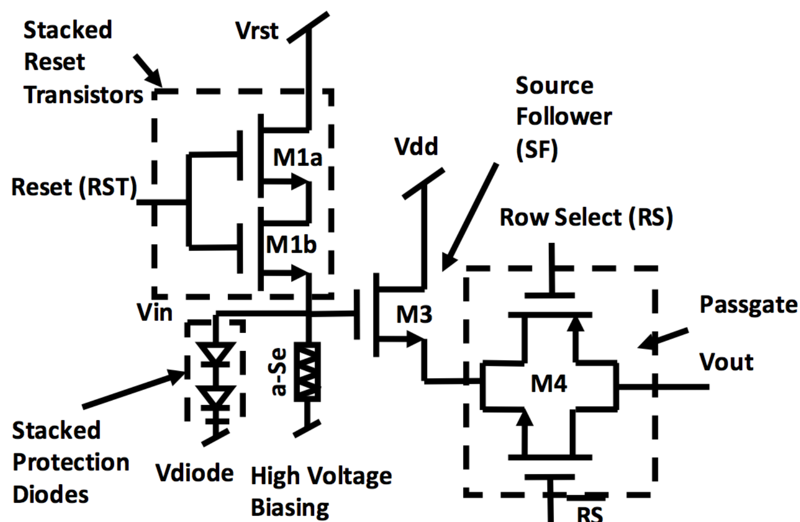


Figure 3.2: Schematic of pixel design in Q1.

where V_{in} is the integrated charge at the gate of the source follower, $V_{GS_{SF}}$ is the gate-to-source voltage of the source follower, and $V_{DS_{RS}}$ is the drain to the row-select-pass-gate logic's source voltage.

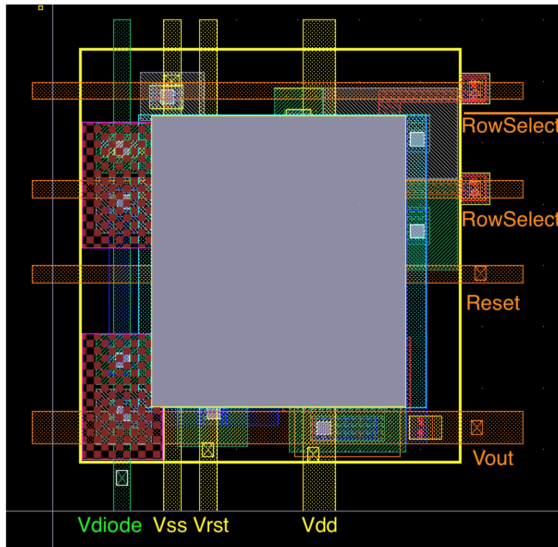
Since the used CMOS process' operating voltage is relatively low, a typical MOSFET threshold voltage of 0.7 V would take away 20% of the operating range, given a standard supply voltage of 1.8 V and high voltage option of 3.3 V. Therefore, to preserve the pixel operational range, we used a native NMOS device as the source follower. A native device has a threshold voltage close to 0 V. The trade-off is its large minimum-size requirement and low transconductance g_m when compared to regular devices with the same size and biasing. However, since it is used as a source follower to isolate the integration node from the readout path, no gain is required from this device; therefore, the low g_m would not have a significant impact on the pixel performance. A larger device size could also be acceptable because minimizing the pixel size is not a primary target for this design. Moreover, if only a single NMOS or PMOS is used as the row-select device, the row select device would not be able to buffer the entire voltage operational range. Hence, we used a pass-gate pair as the row-select logic. The V_{RST} line is normally set to 0.6 V, which provides sufficient operating voltage for the biasing-current-mirror-down readout path. Lastly, given the protection diodes' 0.6 V forward voltage, to prevent the integration node voltage from rising above 3.3 V, the V_{diode} line was usually set to 2.1 V. We used P+/N-well diodes (pDiode) as the protection diodes, which are often

Table 3.1: Q1 pixel device sizing summary.

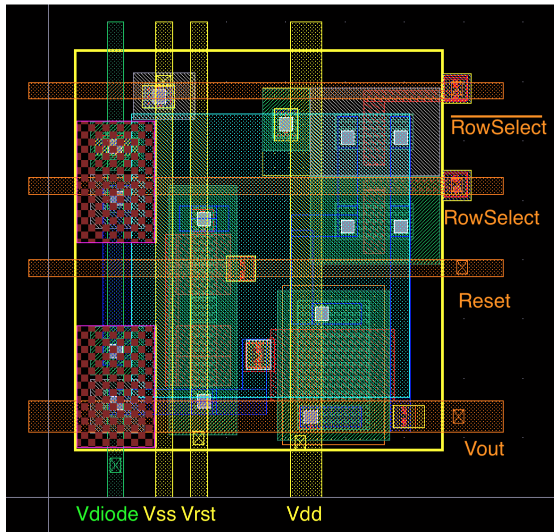
Device	Purpose	Type	Dimensions
M1a&b	Reset	3.3 V NMOS	W/L = 0.22 µm/0.35 µm
M3	Source Follower	3.3 V Native NMOS	W/L = 1.2 µm/1.2 µm
M4	Row Select	3.3 V NMOS & PMOS	W/L = 0.6 µm/0.35 µm
D1&D2	Protection Diode	3.3 V pDiode	Area = 0.2025 µm^2

used as ESD protection devices. To ensure the high-voltage plane will not contact the imager, extra care must be taken when designing the shadow masks used for depositing a-Se and the top electrode.

Figure 3.3b shows the full APS layout in Q1 without a passivation opening. To expose the pixel-integration node to the a-Se photosensor, each pixel contains a passivation opening. The passivation opening removes the top polyimide protective layer from the wafer, exposing the top-most metal layer. This process is generally used for creating bond pads. Figure 3.3a shows a passivation opening of 5.7 µm x 6.2 µm. This layout's pixel pitch is 6.8 µm x 7.76 µm; however, since a pixel should have an equal height-width aspect ratio, we increased the X-direction pitch to 7.76 µm.



(a) Layout with pad opening, as implemented in Q1.



(b) Layout with pad opening omitted to show internal structure.

Figure 3.3: Layout of pixel in Q1.

3.1.2.1.1 Series Stacked Reset and Protection Diode In digital-circuit design, stacking MOSFETs is a commonly used technique for improving leakage performance. With the high-leakage current and its associated shot noise, the reset device in a 3-T voltage-mode APS can cause a DC-level shift over time and increased noise during integration. When a MOSFET is operating in weak inversion or subthreshold mode, its current $I_{D,WI}$ has an exponential relationship with the gate-source voltage, as shown by

$$I_{D,WI} = I_t \frac{W}{L} e^{\frac{V_{GS}}{\frac{nkT}{q}}} (1 - e^{\frac{V_{DS}}{\frac{kT}{q}}}) [36] \tag{3.2}$$

where I_t is a constant based on the device's physical parameters; V_{GS} is the gate-source voltage; V_{DS} is the drain-source voltage; and n is the substrate factor, ranging between 1 to 2 for silicon ICs.

Transistors M1a and M1b in Figure 3.2 are a stacked NMOS pair of the same size. Because the leakage current has an exponential relationship to V_{DS}, stacking the 2 devices together will reduce the V_{DS} across both devices by more than 50% and up to 90%, depending on the original potential difference between the VDS across the stacked devices. With a typical CMOS technology, the nodal voltage between the stacked devices is about $\frac{1}{7}$ of V_{DD} [38], which can yield a leakage improvement of close to an order of magnitude, even if only 2 devices are stacked [35].

A typical APS design would also include a protection diode connecting to either the system power or ground, depending on whether the imager is performing electron or hole collection. In the Q1 design, the protection diode is implemented with D1 and D2. These diodes prevent the integration node from charging above the rated MOSFET-gate voltage, damaging the transistor permanently. The diode current I_D also follows an exponential behavior with respect to the potential across it, governed by

$$I_D = I_s (e^{\frac{qV_D}{nkT}} - 1) \tag{3.3}$$

where I_s is the diode's saturation current. During normal pixel operation, however, the diode is reverse biased. Since the current does not change much across the reverse-biasing range, the effect of stacking will not be as substantial as the MOSFET. Based on circuit simulation, the diode leakage current is reduced by roughly 2x over its intended operational range.

3.1.2.1.2 Separate diode trace to reduce leakage Since the imager is intended to operate under low-light conditions, the diode leakage current can be further reduced by

Table 3.2: Gate capacitive effect in different regions. [40]

Capacitance	Cut-Off	Triode	Saturation
C_{gb}	$C_{ox}WL_{eff}$ (maximum)	0	0
C_{gd}	0	$1/2C_{ox}WL_{eff} + C_{ox}WL_D$	$C_{ox}WL_D$
C_{gs}	0	$1/2C_{ox}WL_{eff} + C_{ox}WL_D$	$2/3C_{ox}WL_{eff} + C_{ox}WL_D$

connecting the biasing terminal to a supply line separated from the system power or ground, such as V_{diode}. If the imaging condition and the signal level is known, the biasing line can be set to a voltage close to the expected signal level, hence, reducing the potential difference across the diodes and, therefore, minimizing leakage current.

3.1.2.1.3 Parasitic Capacitance at the Integration Node As previously stated, the conversion gain is determined by the capacitance present at the integration node. Since this design's primary target is low-light imaging, a high conversion gain is preferable. Therefore, rather than use either a dedicated MIM or MOS capacitor, we used the MOSFETs' parasitic capacitance to achieve the lowest capacitance possible. This method's downside is that the parasitic capacitance's linearity will not be constant across the entire operation range since the parasitic capacitance will change across the MOSFETs' different region of operation. A MOSFET's parasitic capacitance can be divided into 2 major groups: the gate capacitive effect (governed by C_{OX}) and the junction-capacitance drain and source bodies [40]. Figure 3.4 shows a summary of the parasitic capacitors of interest in a typical NMOS device. Table 3.2 shows the relationship of C_{OX}-based capacitors with the different operating regions, including the gate-to-source capacitance C_{GS}, the gate-to-drain capacitance C_{GB}, and the gate-to-body capacitance CGB. In the figure and table, L_{eff} is the MOSFET's effective channel length and L_D is the gate-source/drain overlapping channel length.

The junction capacitance C_{SB} and C_{DB} from the reset transistor is more complicated and difficult to model as it is a function of doping concentration and depletion depth, the latter changing with different biasing voltage across the junction. It also depends heavily on the drain and source wells' sizes, meaning the only method to accurately extract them is through post-layout simulation. To account for the additional capacitance added by the routing metals and interconnects after all the connections were made, we simulated the parasitic capacitance at the integration node through post-layout extraction.

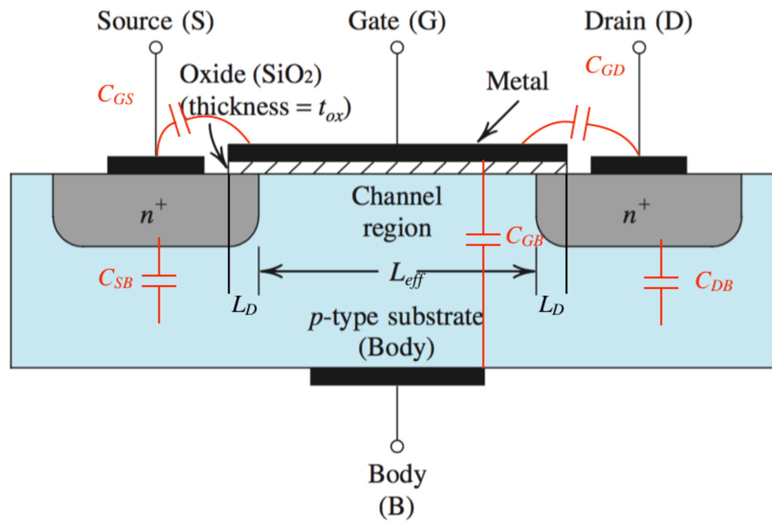


Figure 3.4: Parasitic capacitances of the MOSFET. [39]

3.1.2.1.4 Timing Operation The modified 3-T design's timing operation is like the 3-T voltage-mode APS, but with a few additional devices operating through each region. Figure 3.5 shows this design's timing diagram.

The pixel's operation during each phase of operation is described below:

1. Reset: The reset devices M1a and M1b are turned on, allowing the previously integrated charge sitting on the integration capacitor to be discharged and set to the same potential as the V_{RST} line. Given enough time for the reset devices to discharge the integration node, the only DC offset from the reset operation is the charges injected into the integration node when the reset device is turned off. This phenomenon is named charge injection, and it is addressed in Q2.

2. Integration: During the integration period, the reset devices are turned off and holes generated within a-Se, caused by incoming photons, will be collected at the integration node. The reset device and the protection diodes will also leak charge into the integration node, pulling the voltage closer to a steady-state value somewhere between V_{DIO} and V_{reset}. With the leakage-current suppression circuitry in place, the signal generated from the a-Se photosensor can overpower the net leakage current, even in low-light conditions. The results section will further discuss this in more detail.

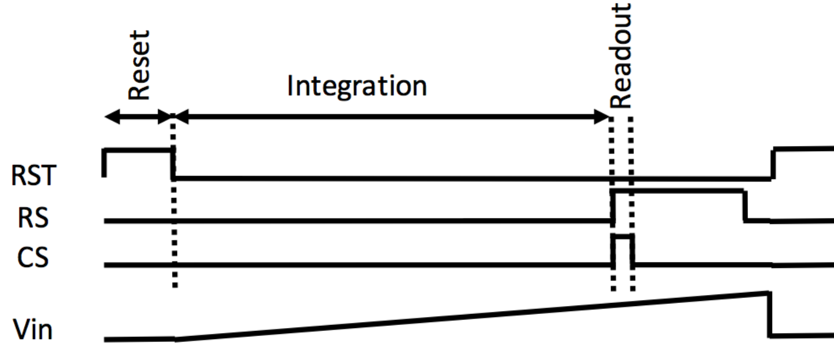


Figure 3.5: Timing diagram of Q1.

3. Readout: Once the pixel has integrated for a defined period, the row-select pass-gate will turn on. This action will connect all pixels in a single row to their respective column bus. A column-select mux will be turned on, allowing the biasing current from the current mirror down the readout path to sequentially pass through each pixel's source follower. This allows the integrated voltage to be buffered to the column line through the source follower. The on-chip op amp in the readout path will buffer the voltage off the chip, which is then digitized by an ADC on the PCB.

3.1.2.1.5 Pixel Gain The low frequency gain of the source follower M3 A_{VSF} can be calculated with

$$A_{V_{SF}} \approx \frac{g_m}{g_m + g_{mb} + g_{ds}} = \frac{1}{1+\eta} \tag{3.4}$$

where g_m is the transconductance of the native source follower, g_{mb} is the transconductance caused by the body effect of the device, and $\eta = \frac{g_{mb}}{g_m}$. [33].

For a typical transistor-source bulk voltage, η remains greater than 0.2. However, since a native device is used, η was simulated in the technology kit and found to be close to 0.05, providing a source-follower gain close to 1. Moreover, with

$$\frac{\omega C_L}{g_m} << 1 \tag{3.5}$$

where ω is the angular frequency, this amplifier's pole will be much higher than the operating frequency, therefore it is reasonable to use the low-frequency gain of the source follower across the entire operating frequency.

3.1.2.1.6 Noise Under low-light conditions, to detect low incoming signals, the system noise, especially temporal noise, must be kept low. The previous chapter discussed the main noise source in a 3-T transistor, including thermal noise and leakage shot noise from both the reset MOSFET and the protection diodes. All pixel-noise analyses are input-referred to the integration node V_{in}. The thermal noise is deposited to the integration node after each reset operation. With a simulated capacitance of 3.62 fF, the thermal noise can be calculated with Equation 2.6 to be 24.19 e^-.

The leakage shot noise is difficult to simulate and calculate because of its dependency on the fabrication process and on DC operating points, which constantly change during normal operation. Moreover, with a mixed-signal design kit, the leakage currents characterized in the simulation model are designed to reflect the worst-case scenario, as reflected in the difference between simulated results and measured results. From simulation, the combined net leakage current of the double-stacked reset device and the protection diodes is on the order of 200 fA, while the measured leakage from the fabricated device was only about 3 fA. Based on the measured result, the leakage-current-induced shot noise can be calculated with Equation 2.2. This gives a shot noise of roughly 17.67 e^- at 16.67 ms of integration or 86.6 e^- when operated at 400 ms of integration.

Lastly, we extracted the system's flicker noise from noise-simulation results. Since the simulated result yields a flicker noise of less than 10 e^-, flicker noise is not a predominant noise source.

The overall noise of a Q1 pixel at the integration node can be calculated by adding the above results together in quadrature, which gives 89.9 e^- when operating at an integration period of 400 ms.

3.1.2.1.7 Full Well Capacity, Dynamic Range & Conversion Gain Full-well capacity can be calculated with the simulated integration capacitance of 3.62 fF and with the operating voltage ranging from 0.4 V to 3.3 V. From Equation 1.5, the full-well capacity of the APS in Q1 is 65,612 e^-.

Calculating this APS design's DR with Equation 1.4 gives a result of 57.26 dB. This DR is low compared to traditional imagers. Given the device's sensitivity, we expect it

Table 3.3: Q1 pixel parameters comparison

Parameter	Target	Model Simulated	Q1 Simulated
Conversion gain (µV/e$^-$)	-	26.6	44.2
Input referred electronic noise @ 400 ms t_{int}(e$^-$)	53.7	46.63	89.9
SNR @ 0.01 Lux (dB)	20	21	16.03
Dynamic Range (dB)	-	67.35	57.26
Full Well Capacity (e$^-$)	-	108,750	65,612

to saturate under normal room illuminance. However, because we are trading DR for higher sensitivity or better performance under low-light conditions and since the goal for this imager is to provide low-light imaging, a reduction in DR is expected.

With an integration capacitance of 3.62 fF, the imager's conversion gain is 44.2 µV/e$^-$, which is comparable to a high-gain 4-T design. The pixel's overall gain is the product of the conversion gain and the source follower's gain. With the source follower providing a gain of 0.9, the effective pixel-output-referred gain will be 39.78 µV/e$^-$.

3.1.2.2 Quadrant 2 (Q2)

Prior to a transistor turning off, charge will exist in its channel. Turning the MOSFET off eliminates the channel, which means the existing electrons in the channel must be transferred to either the drain or the source. The electrons tend to travel to the side with lower resistance, but some will still travel to the higher-resistance node. During the reset operation, the integration node is set to the desired reset voltage, and, when the MOSFET is turned off, some of the electrons from the reset-device channel will be pushed into the integration node. This effect is called charge injection. Another coupling effect produced during the reset period is the AC coupling through the reset device's gate-source parasitic capacitor when the transistor is turned on and off; however, the magnitude of this is insignificant compared to the channel charge injection and is, therefore, not the focus for the design.

Charge injection from the reset transistor of a typical 3-T-voltage-mode APS design that includes a large capacitor at the integration node is less concerning because the few electrons injected onto the capacitor will not significantly change the DC voltage. This phenomenon's impact is more severe in this design because of the small integration capacitance since even a small number of electrons can noticeably shift DC level. Equation 3.6 models the amount of charge existing in the channel of the reset NMOS device Q_{ch-n}

Table 3.4: Q2 pixel device sizing summary.

Device	Purpose	Type	Dimensions
M1a&b	Reset	3.3 V NMOS	W/L = 0.22 µm/0.35 µm
M2	Charge Injection Reduction	3.3 V NMOS	W/L = 0.22 µm/0.7 µm
M3	Source Follower	3.3 V Native NMOS	W/L = 1.2 µm/1.2 µm
M4	Row Select	3.3 V NMOS & PMOS	W/L = 0.6 µm/0.35 µm
D1& D2	Protection Diode	3.3 V pDiode	Area = 0.2025 µm^2

while it is in a steady state, given by [41]

$$Q_{ch-n} = W_n L_n C_{ox}(V_{DD} - V_{RST} - V_{th}) \tag{3.6}$$

where W_n and L_n are the width and length of the MOSFET, C_{ox} is the gate-oxide capacitance per unit area, V_{DD} is the gate voltage applied to the reset device when it is turned on, V_{RST} is the reset voltage at the reset device's drain, and V_{th} is the NMOS's threshold voltage.

To counter this effect, a dummy transistor can be inserted between the reset device and the integration node. We implemented this solution in Q2 pixel designs through transistor M2, as Figure 3.6 shows. The dummy device's drain and source were shorted together so it won't affect normal operation. Its gate connects to the inverted reset signal, so when the reset device M1a & b are turned off and charges are being pushed out of its channel, the dummy device will turn on and create a channel, preventing the charges from injecting into the integration node, therefore keeping the DC-level constant.

Table 3.4 lists the size of the devices used in this pixel design, along with the layout of the pixel in Figure 3.7. Through simulation, charge injection can shift the DC by 200 mV in the design without the dummy device (Q1). With the dummy device implemented, the DC shift reduced to less than 10 mV from schematic simulation and 30 mV from layout-extracted simulation.

Q2's device sizes are the same as Q1's except that the integration node is connected to the dummy device's source instead of the reset device. However, since the dummy device source's junction dimension is the same as the reset device, the depletion capacitance will not change, hence, the same noise performance and specifications, including full-well capacitance, DR, and conversion gain, should be the same as Q1.

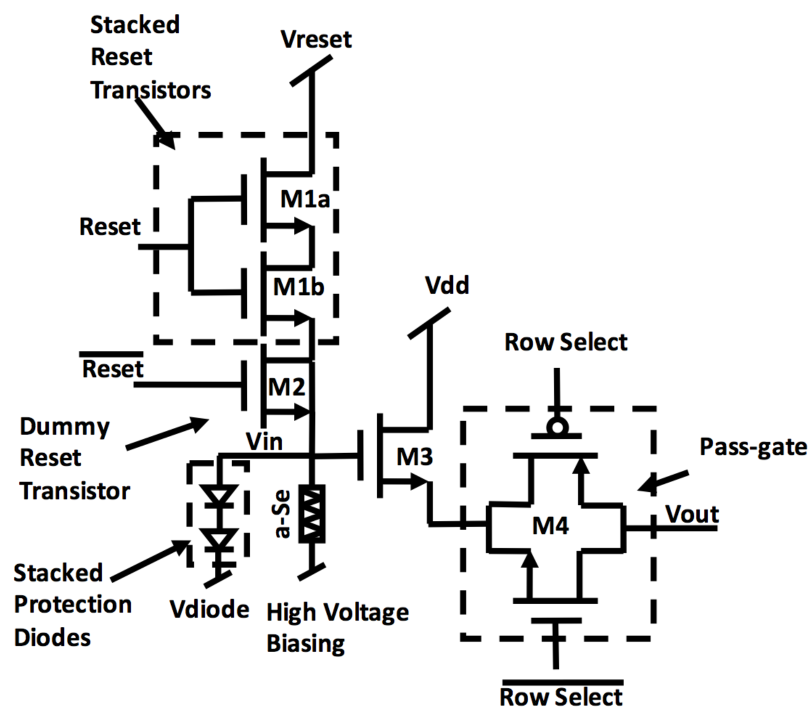
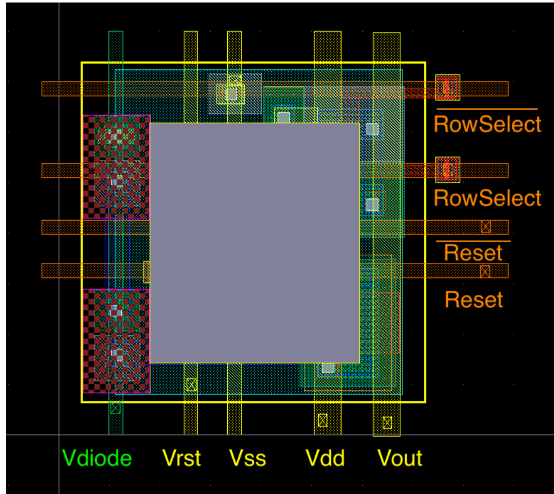
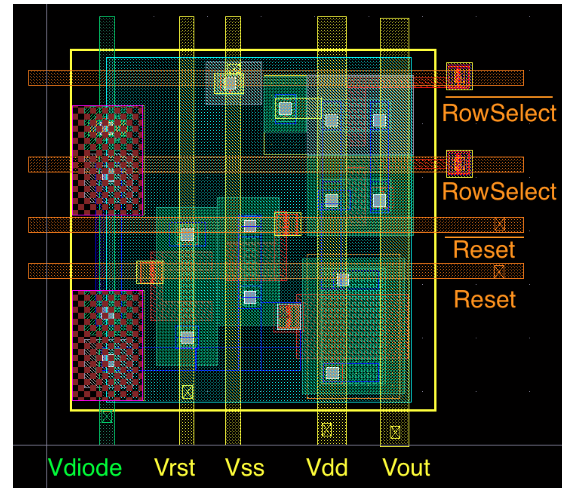


Figure 3.6: Schematic of pixel design in Q2.



(a) Layout with pad opening, as implemented in Q2.



(b) Layout with pad opening omitted to show internal structure.

Figure 3.7: Layout of pixel in Q2.

3.1.2.3 Quadrant 3 (Q3)

Because the reset transistors' leakage-current shot noise is a dominant Q1 noise source, we built Q3 to study the effect of using a PMOS device as reset transistors instead of NMOS. The reason for the other designs' use of NMOS as a reset device is that PMOS is unable to pass low-reset voltage onto the integration node. Since we are planning to operate a-Se in hole collection mode, each incoming signal will cause positive voltage shift. The pixel voltage, therefore, needs to be reset to a low DC value to leave room for holes to integrate. The use of a PMOS device will significantly reduce the device's DR. However, by using PMOS as the reset device, the parasitic diode formed from the p-type source to the n-well body will replace the explicit protection diodes thereby creating a reference design to any additional effect of the double-stacked diode may add to the pixel circuitry. Figure 3.8 shows the Q3 schematic. Table 3.5 lists the device sizing. Figure 3.9 shows the layout.

The estimated capacitance is like Q2's, but without the protection diodes we estimate the overall integration capacitance to be 3.23 fF. Through simulation, the lowest voltage that a PMOS could reset to is 1.4 V. With the reduced operational voltage range, the full-well capacity will reduce to

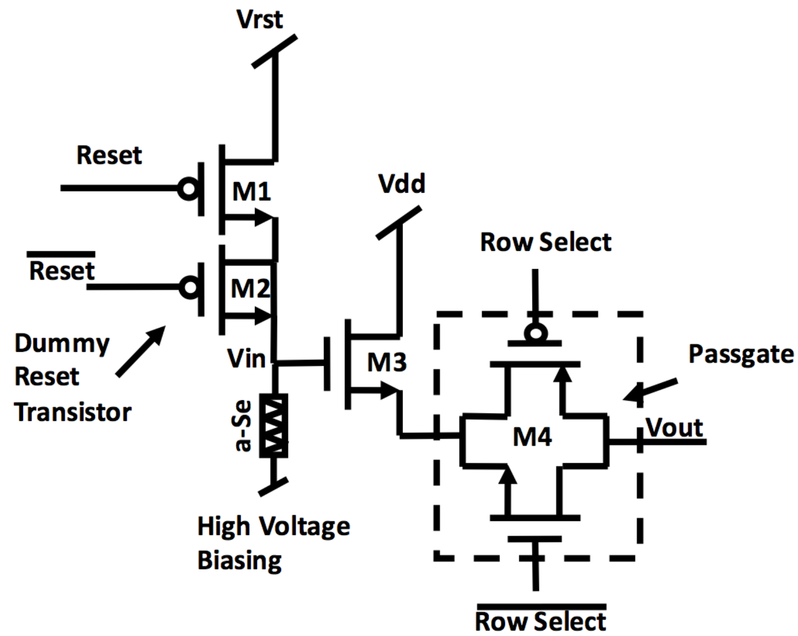
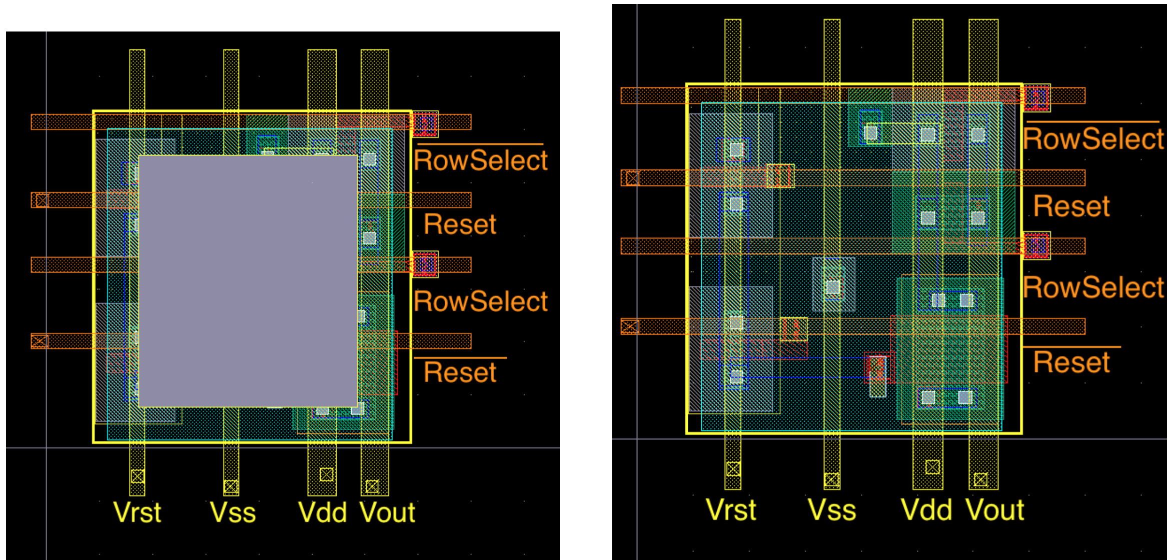


Figure 3.8: Schematic of pixel design in Q3.

Table 3.5: Q3 pixel device sizing summary.

Device	Purpose	Type	Dimensions
M1	Reset	3.3 V PMOS	W/L = 0.22 µm/0.35 µm
M2	Charge Injection Reduction	3.3 V PMOS	W/L = 0.22 µm/0.35 µm
M3	Source Follower	3.3 V Native NMOS	W/L = 1.2 µm/1.2 µm
M4	Row Select	3.3 V NMOS & PMOS	W/L = 0.6 µm/0.35 µm



(a) Layout with pad opening, as implemented in Q3.

(b) Layout with pad opening omitted to show internal structure.

Figure 3.9: Layout of pixel in Q3.

$$\frac{(V_{DD} - V_{reset}) \times C_{int}}{q} = \frac{(3.3V - 1.4V) \times 3.23fF}{1.6 \times 10^{-19}C} = 38,365e^{-} \tag{3.7}$$

which is only 58% of the FWC in Q1 and Q2. The smaller capacitance will lead to less thermal noise; however, without the series-stacked protection diodes, we expect the leakage current to rise; therefore, the overall noise should not vary much from the 2 previous quadrants.

3.1.2.4 Quadrant 4 (Q4)

One downside of using parasitic capacitance as the integration capacitor is the small full-well capacity because it will saturate easily in the presence of a strong signal. Q4 implements an alternative solution that takes advantage of the high gain the small integration capacitance provides while still allowing the same pixel to integrate large signals when needed. A detachable explicit MIM capacitor connects to the integration node by a NMOS transistor, as Figure 3.10 shows. When the capacitor-control MOSFET is turned off, the device will demonstrate similar characteristics as Q1; however, with

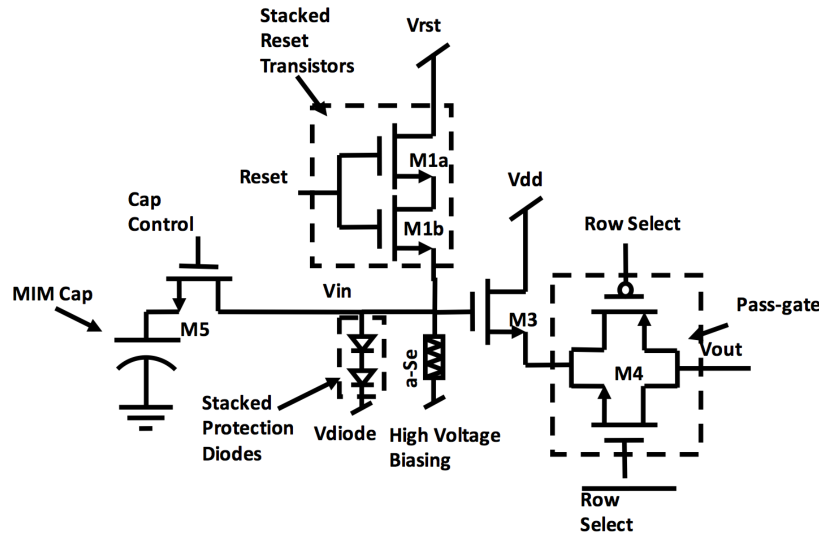


Figure 3.10: Schematic of pixel design in Q4.

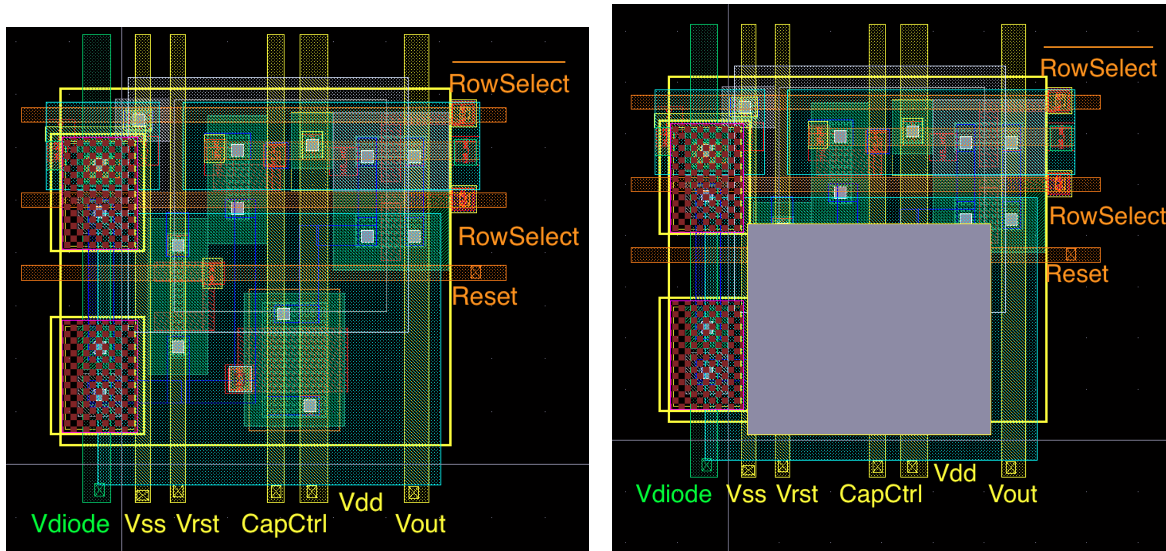
the capacitor-control device turned on, the total well capacitance will increase from 3.62 fF to 20.62 fF, producing a 560% increase in FWC. Figure 3.11 and Table 3.6 respectively show the Q4 MOSFETs' layout and sizing.

However, the increased integration capacitance also comes with higher kTC noise and a reduction in the signal gain. The kTC noise will increase from 24.19 e^- to 57.74 e^-, increasing the total noise to 103.6e^-, while the pixel gain drops from 44.2 μV/e^- to 7.75 μV/e^-.

Table 3.7 summarizes the performance of all quadrants.

Table 3.6: Q4 pixel device sizing summary.

Device	Purpose	Type	Dimensions
M1	Reset	3.3 V PMOS	W/L = 0.22 μm/0.35 μm
M2	ResetX	3.3 V PMOS	W/L = 0.22 μm/0.35 μm
M3	Source Follower	3.3 V Native NMOS	W/L = 1.2 μm/1.2 μm
M4	Row Select	3.3 V NMOS & PMOS	W/L = 0.6 μm/0.35 μm
M5	Capacitor Control	3.3 V NMOS	W/L = 0.42 μm/0.49 μm
D1 &D2	Protection Diode	3.3 V pDiode	Area = 0.2025 $μm^2$
C1	Extended Capacitor	3.3 V MIM	Capacitance = 17.74 fF



(a) Layout with pad opening, as implemented in Q4.

(b) Layout with pad opening omitted to show internal structure.

Figure 3.11: Layout of pixel in Q4.

3.1.3 Digital Control

Given that the use of scan chains by the design's 4 arrays, each of them 160 columns by 120 rows, was a simple and robust solution to generate the necessary digital control signals. If decoders are used to generate the control signals, an 8-bit and a 7-bit design must be accordingly used. This method requires up to 100 connections to come off the chip just for addressing alone. Therefore, given the limited chip dimension, the low-pin-count scan chain is the more suitable solution. Figure 3.12 shows the timing control connection for a 3x3 array. Figure 3.13 shows this small array's timing.

Table 3.7: Summary of all quadrants.

Parameter	Q1	Q2	Q3	Q4 (Cap off/on)
Conversion gain (μV/e$^-$)	44.2	44.2	44	44.2/7.76
Input referred noise @ 400 ms integration(e$^-$)	89.9	89.9	89.9	89.9/103.6
Dynamic Range (dB)	57.26	57.26	52.6	44.2/7.75
Full Well Capacity (e$^-$)	65,612	65,612	38,365	65,612/373,737

Figure 3.12: 3x3 array connection illustration.

The row-select scan chain selects the first row RS[0] at the end of the integration period while the integrated signal is ready to be transferred to its own column bus. By scanning through the column-select scan chain, the current mirror at the bottom of the array sequentially biases each pixel in the row, allowing the data to transfer to the on-chip op amp. Once the column-select scan chain finishes cycling through the row, the row-select scan chain shifts one bit and the second row is turned on. At the same time, the reset-scan chain enters the array, resetting the previously sampled row. This timing flow runs consecutively between frames with the frame rate dictated by how fast the pixels can be read out. Notably, the rising edge of the clock feeding into the scan chain triggers the shift operation; therefore, the column-select clock must run 160 times faster than the row- and reset-scan chain clocks

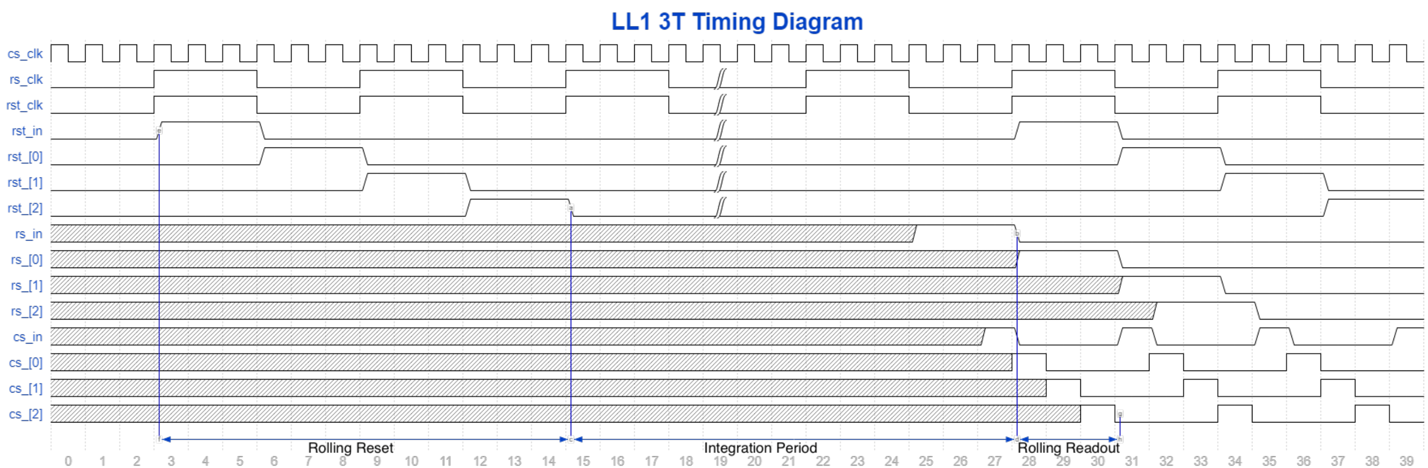


Figure 3.13: Timing diagram of 3x3 array operation.

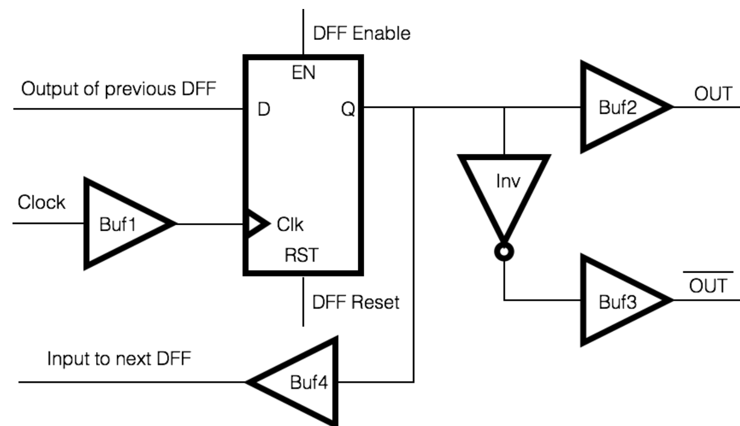


Figure 3.14: Scan chain schematic.

3.1.3.1 Scan Chain Configuration

Scan chains built using master-slave positive edge triggered D flip-flops (DFFs) with asynchronous enable and reset were selected for this design for the ease of implementation and robustness. The full scan chain is formed by connecting the output of one DFF to the input of the next DFF in the chain, as illustrated in Figure 3.14. Additional delay is introduced between DFFs with a chain of 6 inverters. The purpose of this delay circuitry is to account for potential hold violations, avoiding two adjacent DFFs to be turned on at the same time. This will occur if the pulse to the next DFF arrives too early, or the clock skew causing the edge to arrive at the next DFF too early. The effect of the delays was simulated in Cadence, where a digital delay unit is placed between the clock inputs of two adjacent DFFs, representing possible clock jitter and skew. With the 6 inverters as the delay unit, adjacent DFFs can tolerate up to 800 ps of clock skew. The output of each DFF is then connected to a chain of inverters, sizing up at 2x rate to match up a load of fanout of 4, equivalent to a row of pixels, in order to reduce propagation delay.

3.1.3.2 D Flip-Flop

The positive-edge-triggered DFF can be broken down into 3 parts: the asynchronous reset and enable controls, the inverted signal generation circuitry, and the master-slave-positive-edge-triggered DFF. Figure 3.15 shows the schematic of a single DFF.

I built the DFF by cascading a positive latch (master) with a negative latch (slave). While the clock is low, the master stage is transparent, transmission gate T1 will be on,

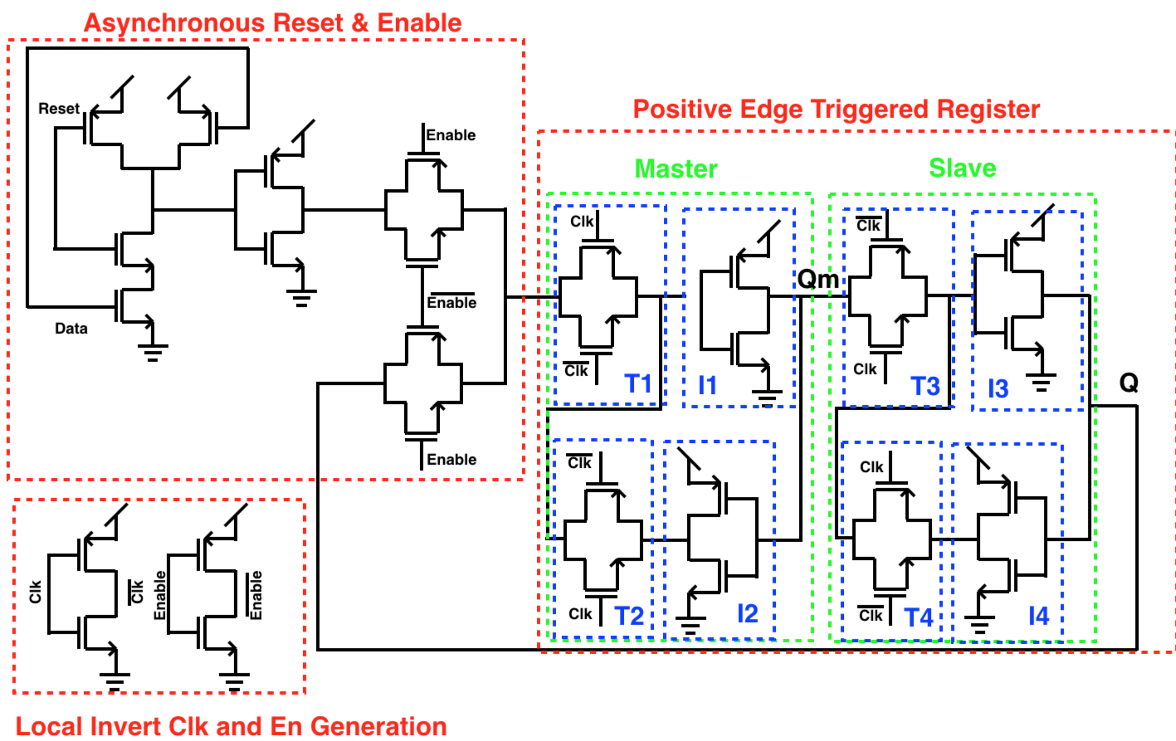


Figure 3.15: D flip-flop schematic.

and the inverted data will sit on the node QM. With T2 off, the feedback in the master latch is disabled. During the same phase, T3 will be off and T4 will be on, so the slave will not be sampling the incoming data at Qm but instead allow cross-coupled inverters I3 and I4 to hold its previous value. When the clock goes high, T1 will turn off, disabling the master's capacity to sample incoming data, and with T2 turned on, the master stage will hold its data immediately prior to the rising edge of the clock. The master stage then drives QM to the inverted data value, thereby making this DFF positive-edge triggered. At the same time, the slave latch will sample the inverted data sitting on node QM and output the data onto the node Q.

In the analysis above, we assumed no delay exists between the clock and its inverted signal, meaning there is no instant in time when both the clock and clock bar will be high or low. If that were to happens, the DFF would be transparent. To ensure optimal clock and clock-bar-delay matching, the $\overline{clock}$ signals are buffered locally for each DFF, feeding off the same incoming clock signal.

One downside of this DFF design is the number of gates the $\overline{clock}$ and clock signal need to drive. With a desired rise-and-fall time of less than 3 ns and a total capacitance of approximately 0.1 pF, which is contributed by all DFFs in a single 160-device scan chain, the clock driver needs to have a large driving strength.

A simple NAND gate, combined with an inverted in each DFF, muxes the reset signal with the incoming data. Another transmission gate before the DFF realizes the enable function. A second transmission gate with an inverted enable control signals closes the feedback loop from the DFF's output to the master latch's input, allowing the DFF to hold its value while disabled.

3.1.3.2.1 Driving Strength One of this imager's design targets is to show the real-time imaging capability of a-Se. This requires the imager to operate at 60 frames per second. With that in mind, at the fastest readout speed, the maximum time allowed for the readout circuitry to spend on each pixel is $1/60/120/160 = 868ns$, which means the column-select-scan-chain buffer's period must exceed $1/868ns = 1.152MHz$.

Therefore, the digital control signals driving the array should have a rise-and-fall time of less than 5 ns so that the transition time will take up less than 2% of the pixel readout time. Hence, we buffered each flip-flop's output through a chain of 2x-sized-up inverters to meet the rise-and-fall-time requirement while minimizing propagation delay. A schematic simulation with a 120x160 array connects as the load, and one pair of inverters is added to the buffer chain at a time. With only 2 pairs of inverters, the simulated signal's rise-and-fall time is less than 1 ns. This over-design accounts for the

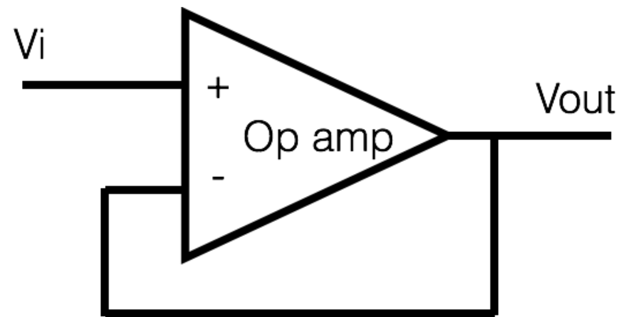


Figure 3.16: Unity gain buffer created using high gain op amp.

parasitic capacitance and propagation delay added by the routing traces, as well as the silicon process and corner variations.

3.1.3.2.2 Testability To verify the scan chain's functionality in the fabricated ICs, the output of the last DFF in each scan chain passes directly off the chip. This allows us to monitor the expected output when an input pulse is passed into the scan chain. However, since the total number of needed bond pads should be limited, we implemented 2 3:8 decoders, built using transmission-gate logics, to consolidate the scan-chain outputs, thus dropping the pin count from 12 to 8. All devices used have the minimum size of a PMOS device in the CMOSP18 3.3 V process, with W/L = 220 nm/350 nm, since speed is not a critical concern for a functionality- and connectivity-verification circuit.

3.1.4 On Chip Voltage Buffer

Since each pixel's analog output voltage must be transmitted off the chip to a discrete ADC to digitize the data, and because of the capacitance and inductance added by external PCB traces, chip bond wires, and the potential probing tips of test equipment, an on-chip buffer is required to reduce loading effects. Figure 3.16 shows a simplified diagram of the analog buffer. Here, a high-gain op amp connects in a unity-gain-feedback configuration. This section will describe the high-gain op amp's design.

3.1.4.1 DC Gain

To take advantage of the 14-bit ADC used for digitizing the analog data, the op amp's close-loop gain should deviate less than 1/2 least significant bit (LSB) away from unity

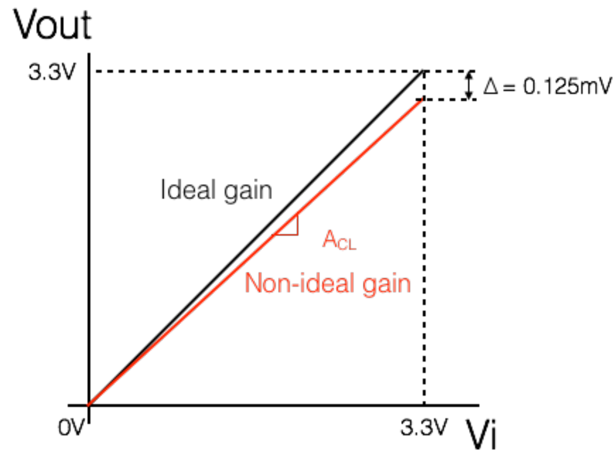


Figure 3.17: Non ideal gain of unity gain buffer.

when the input applied Vi is at its maximum value. Given that the chosen ADC has an internal reference voltage of 4.096 V, $\frac{1}{2}$ LSB equals $4.096/2^{14}/2 = 0.125mV$.

Given that the maximum signal coming off the chip is 3.3 V, for the buffered signal to be within 0.125 mV of the highest possible output of 3.3 V (as Figure 3.17 shows), the buffer's closed-loop dc gain A_{CL} can be obtained by calculating the slope of the non-deal gain shown in red in Figure reffig:gainslope, given by

$$A_{CL} = \frac{3.3 - \frac{4.096}{2^{14} \times 2}}{3.3} = 1 - \frac{\frac{4.096}{2^{14} \times 2}}{3.3} = 0.9999621 \tag{3.8}$$

The buffer's closed-loop gain A_{CL} is also given by

$$A_{CL} = A_{OL}/(1 + A_{OL}) \tag{3.9}$$

where A_{OL} is the op amp's open-loop dc gain. The open-loop dc gain must be greater than 27031.6 V/V, or 88.6 dB, to achieve the close-loop gain in Equation 3.8 at an input voltage of 3.3 V. However, this gain requirement decreases at a lower input voltage because a lower gain is needed for a smaller input value to be within 1/2 LSB of the ADC. The next section will show the calculated result.

3.1.4.2 Slew-Rate

The op amp's slew-rate (SR) is one of the buffer's important specifications. Slew rate is the maximum rate of an amplifier's output in response to an abrupt change of input level. Given the chip is designed to operate at 60 frames per second; thus, each pixel will be connected to the readout path for 868 ns. Since the last 420 ns of each readout operation is dedicated to ADC sampling, the buffer's output swing must handle the full rail transition from 0 to 3.3 V within the first 448 ns, assuming the buffer is slew-rate limited for the entire settling period. To create design margin, the buffer was chosen to be able to drive its output with a magnitude change of 3.3 V within 10% of the time allowed for analog signal to settle at the amplifier's input. Therefore the desired slew rate SR_{ideal} is calculated by

$$SR_{ideal} = \frac{3.3V}{\frac{448ns}{10}} = 73.6V/\mu s \tag{3.10}$$

When the buffer's input is a step voltage, the maximum rate of change at the buffer's output $\frac{dV_o}{dt}\Big|_{max}$ will occur at time zero, given by

$$\frac{dV_o}{dt}\Big|_{max} = \frac{V_{step}}{\tau_{buf}} \tag{3.11}$$

where V_{step} is the step input's amplitude (3.3 V) and τ_{buf} is the buffer's time constant, defined by

$$\tau_{buf} = \frac{1}{GBW} \tag{3.12}$$

where GBW is the buffer's gain-bandwidth product, expressed in rad/s. Therefore to satisfy the ideal slew rate of 73.6 V/µs, the GBW of the buffer must be greater than 3.54 MHz. With the open loop dc gain calculated to be 27031.6 V/V from the previous section, the -3 dB frequency of the buffer must be greater than 131 Hz. The dominating first pole was found in later section to be above 1300 Hz.

In order to provide additional design margin, we targeted a slew rate of 82 V/µs.

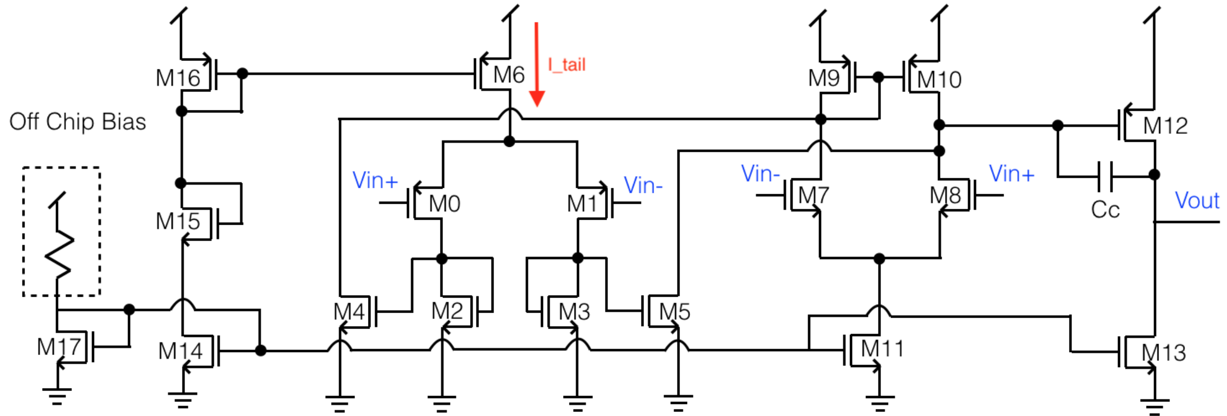


Figure 3.18: Schematic of rail-to-rail op amp.

3.1.4.3 Input Common Mode Range

Since the pixel circuit has been optimized to achieve the maximum voltage, the op amp should not be the bottleneck for the system's DR. We selected an op amp with both NMOS and PMOS input pairs to achieve rail-to-rail input common range, as Figure 3.18 shows. The NMOS input pair cascades onto the PMOS input pair by way of a simple current-summing technique achieved through transistor M2-M5. Table 3.7 lists the sizing and some relevant DC characteristics of the devices.

The sizing and some relevant DC characteristics of the devices are listed in Table 3.8.

To better understand the op amp, this section will analyze each stage separately. Since the op amp's anticipated capacitive load is roughly 20 pF and the dominant pole should be controlled by the compensation capacitor, we configured the compensation capacitor to be roughly 0.3 times the load capacitance.

Given that the previous section calculated the desired slew rate, the required input pair tail current I_{tail} to be able to source enough current through the feedback capacitance of 6 pF to achieve the calculated slew rate is found by

$$I_{tail} = SR \times C_C = 475.6uA \tag{3.13}$$

which can be used to set each input pair's tail current. For most of the input common range, both input pairs will be in saturation, the total tail current of the combined input stage needs to meet the value calculated above. Assuming that the NMOS and

Table 3.8: Op amp transistor sizing.

Device	W/L (μm)	gm (A/V)	Ids (A)
M0&M1	50/1	6.625E-4	-1.47E-4
M2&M3	20/1	9.9091E-4	1.47E-4
M4&M5	20/1	1E-3	1.4799E-4
M6	50/1	1.32E-3	-2.932E-4
M7&M8	10/1	6.38E-4	1.2799E-4
M9&M10	20/1	9.8293E-4	-2.7599E-4
M11	20/1	9.305E-4	2.5599E-4
M12	500/0.5	1.931E-2	-5.9897E-3
M13	200/0.5	2.672E-2	5.9897E-3
M14	20/1	1.351E-3	2.99E-4
M15	20/1	1.361E-3	2.99E-4
M16	50/1	1.361E-3	-2.99E-4
M17	20/1	1.361E-3	3.022E-4

PMOS pair will sink roughly an equal amount of current (to balance the 2 input pairs' gm; explained later in this section), we assumed each tail current would be 237.8 uA, or $I_{DM7\&M8,\,M4\&M5}$ = 118.9 uA, where $I_{DM4\&M5} = I_{DM0\&M1}$, which means the current that charge/discharge the capacitor will be shared equally between the two input pairs through the current summing transistor M4 and M5, hence allowing the two input stages to share the required tail current load.

By simulating individual devices, we estimated and used the NMOS and PMOS's process-transconductance parameters during the op amp's design process, with $k'_n = \mu_n C_{ox} = 215 \times 10^{-6}[A/V^2]$ and $k'_p = \mu_p C_{ox} = 39.7 \times 10^{-6}[A/V^2]$.

The PMOS input pair is suitable for amplifying signals from near ground to $Vmax_{PMOS}$. The PMOS pair's minimum common input range is the minimum voltage $V_{minPMOS}$ required for the load pair M2 and M3 to stay in saturation. Therefore,

$$V_{minPMOS} = V_{ov0,1} = \sqrt{\frac{2 \times I_{D_{M0,1}}}{k' \times \frac{W}{L}_{M0,1}}} \tag{3.14}$$

In order to keep the overdrive voltage V_{OV} small, a large W/L is desired. Therefore the 20/1 ratio was chosen, which has a V_{OV} of 0.26 V.

The maximum common-mode input voltage $V_{max_{PMOS}}$ of the PMOS input stage can be calculated as

$$V_{max_{PMOS}} = V_{DD} - V_{ov6} - V_{SG0,1}, \tag{3.15}$$

To minimize the overdrive voltage, the W:L ratio of M6 should also be sufficiently small, yet large enough to source enough current through the PMOS input pair. Therefore, we chose the 50:1 ratio, and the V_{ov} of M6 is 0.54 V. Since the NMOS stage will have a high gm when the input voltage is close to the V_{DD} rail, the large V_{ov} is acceptable.

The gain of the PMOS input stage is given by

$$A_{vPMOS} = g_{m0,1} \times \frac{1}{g_{m2,3}}||r_{o0,1} \approx g_{m0,1} \times \frac{1}{g_{m2,3}} \tag{3.16}$$

The NMOS input pair is a standard differential pair with a current-mirror active load. The V_{min} of this stage is the V_{ov} of M11 for it to stay in saturation: 0.31 V, while V_{max} = V_{DD}-$V_{ov9,10}$. The NMOS input stage's gain is given by

$$A_{vNMOS} = -g_{m7,8} \times r_{o8}||r_{o10} \tag{3.17}$$

The 2 input pairs combine together through transistors M2 to M5. The diode-connected transistors M2 and M3 force the PMOS input stage's Rout to almost $1/g_{m2,3}$. Then transistor M4 & M5, its small signal v_{gs} changing by $g_{m0,1}$ x $1/g_{m4,5}$, will change the small signal current $i_{d4,5}$ in each NMOS input pair's branch by

$$i_{d4,5} = -g_{m4,5} \times v_{gs4,5} = g_{m4,5} \times v_{in+/-} \times g_{m0,1} \times \frac{1}{g_{m2,3}} \tag{3.18}$$

with $g_{m2,3}$ approximately the same as $g_{m4,5}$, $i_{d4,5}$ can be simplified to $g_{m0,1} \times V_{in+/-}$. Given the negative gain, the current change will be in the same direction as the NMOS pair current. Therefore, further increasing the current imbalance when a differential signal is present at the inputs. This is the basis of the current-summing technique.

However, the current-summing input pairs' overall g_m is nonlinear across the entire input common range. As Figure 3.19 shows, when V_{in} is close to ground, the NMOS pair could turn off, which means the PMOS pair, which is still on, will dominate the input pairs' net gm and vice versa. However, even when one of the input pairs is fully turned

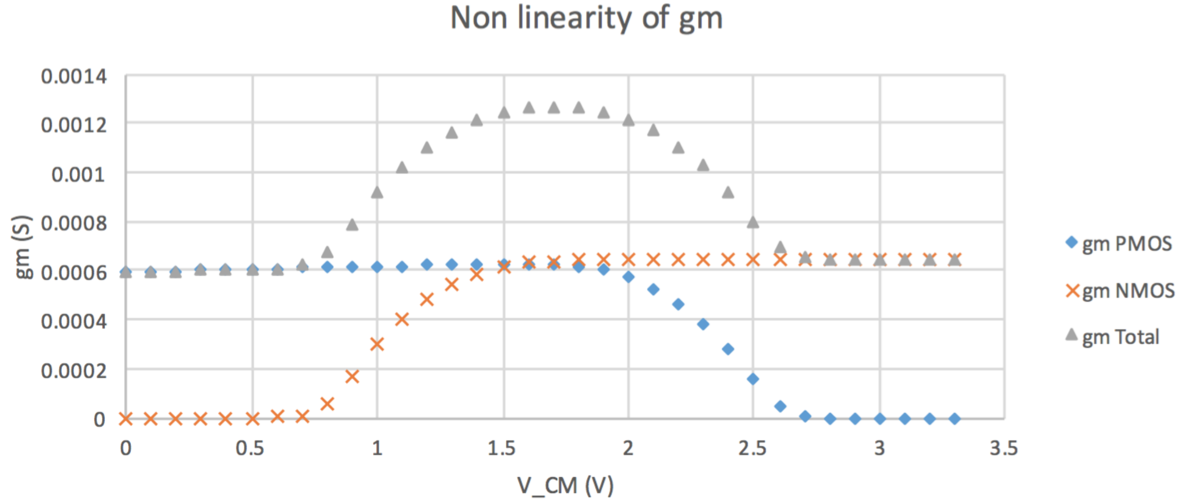


Figure 3.19: Non-linearity of transconductance g_m.

on, the gain will still be above 80 dB within the normal voltage range of operation. Therefore, the nonlinear g_m near the rails is acceptable.

The total gain of the PMOS and NMOS combined input stage A_{Vinput} is given by

$$A_{Vinput} = -(g_{m0,1} + g_{m7,8}) \times r_{o7,8}||r_{o10}||r_{o11} \tag{3.19}$$

The last stage is a common source stage, and the gain of this stage $A_{V_{CS}}$ is simply

$$A_{V_{CS}} = -g_{m12} \times r_{o12}||r_{o13} \tag{3.20}$$

The V_{min} of the output stage is the V_{ov} of M13, = 0.231 V. And the V_{outmax} = V_{DD} - V_{SD12} = 3.3 V - 0.54 V = 2.75 V. When the voltage is higher than 2.75 V, the output will enter triode and the gain will no longer be linear.

The overall gain of the op amp A_{V_o} is given by

$$A_{V_o} = A_{Vinput} \times A_{V_{CS}} \tag{3.21}$$

Figure 3.21 shows the op amp's simulated gain when both input pairs are biased at a common voltage (V_{CM}) of 1.65 V DC. The combined input pairs' simulated gain

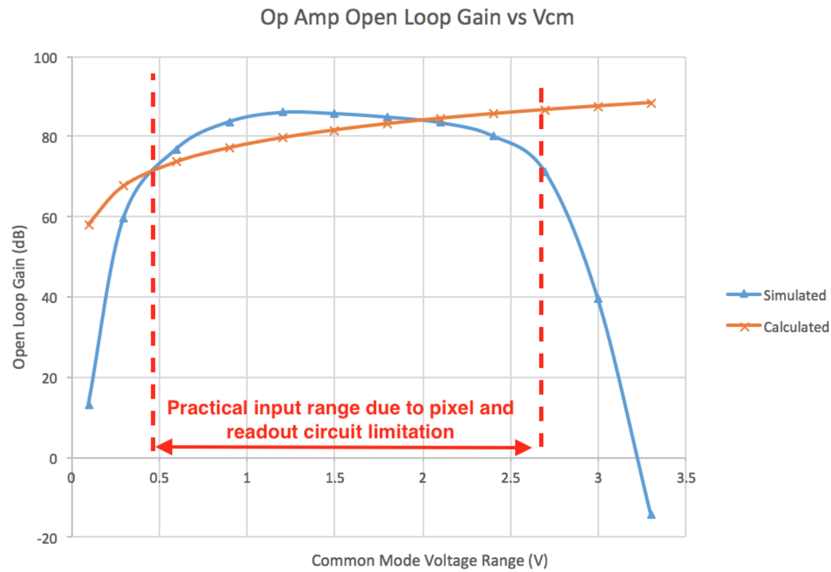


Figure 3.20: Non-linear op amp open loop gain across common mode voltage range.

equals 204.9 V/V and the output stage's gain equals 88.49 V/V, giving an overall gain of 18,131.6 V/V, or 85.17 dB.

Figure 3.20 plots the op amp's simulated open-loop dc gain across the input common range to illustrate the impact of nonlinear input g_m and the low maximum voltage from the common-source output stage. It also shows the gain required for the difference between the input and output voltages to be less than 1/2 LSB. Notably, the required gain is lower at lower voltage. Within the intended pixel-operation voltage limits (0.4 V to 2.75 V) imposed by the minimum voltage required by the current mirror and maximum buffer-output-stage voltage respectively, the DC open-loop gain of the buffer is mostly higher than that of the required gain. For the common-mode voltage closer to 2.75 V, the open-loop gain can be up to 10 dB lower than the required value. However, since this difference in gain will only cause a 0.023% constant offset in the closed-loop configuration, equivalent to 2.5 digital number (DN) when sampled by the ADC, yet the shot noise required for the imager to reach this voltage level is greater than 40 DN, this difference is acceptable.

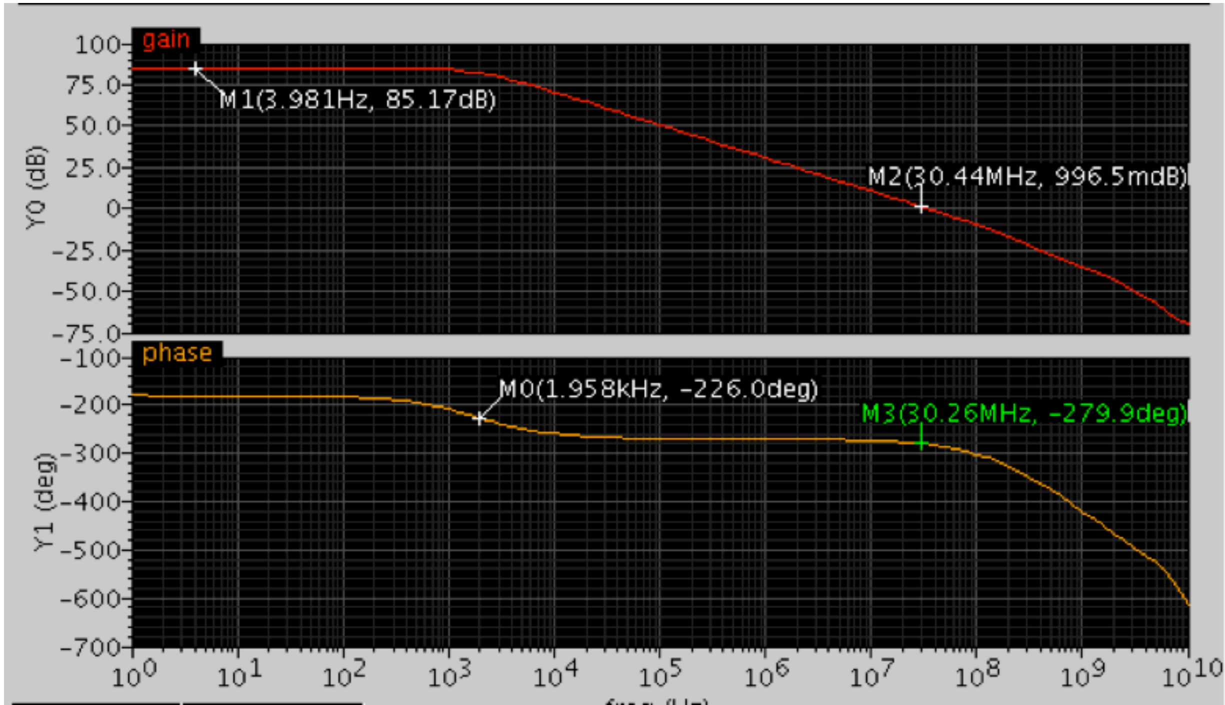


Figure 3.21: Bode plot of rail-to-rail op amp open loop gain and phase at V_{CM} = 1.65 V.

3.1.4.4 Frequency Response and Stability

Since the compensation capacitor is connected from the CS stage's output to the combined stage's output, this capacitor's effective capacitance is multiplied by CS's gain as per Miller's theorem. Since this capacitor was already 2 orders of magnitude larger than any other device's parasitic capacitance in the circuit, it will dictate the dominating pole $fp1$ with the output resistance at the summing stage, as calculated by

$$f_{p1} = \frac{1}{2\pi R_{oinput} \times (A_{V_{CS}} \times C_C)} = \frac{1}{2\pi R_{oinput} \times (g_{mM12} \times r_{oCS}) \times C_C} = 1388Hz \quad (3.22)$$

where $A_{V_{CS}} \times C_C$ is the equivalent input capacitance as based on Miller's theorem. From Figure 3.21, the first pole's location is roughly at 1958 Hz. The difference between the estimated value and the simulated value can be explained by the output resistance used during calculation.

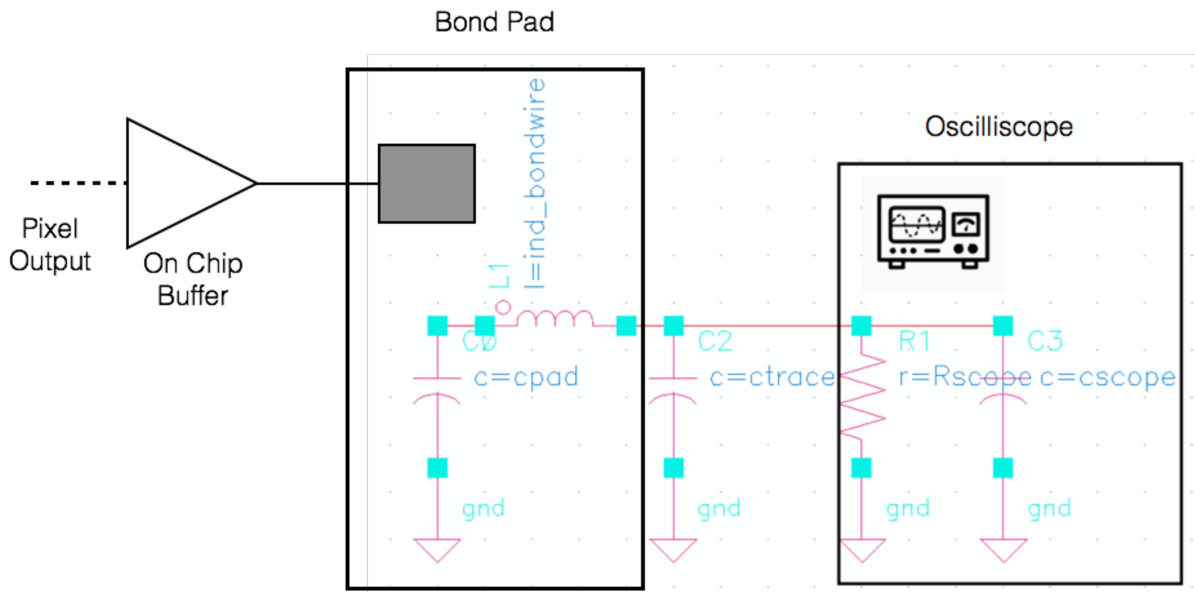


Figure 3.22: Op amp realistic load.

As for the device's stability, without any load added to the op amp, the phase margin is 80.1 degrees. To simulate the op amp's realistic load condition, we added a few passive components to the simulation setup, as Figure 3.22 shows.

The first capacitor C_{pad} at the output represents the bond pads' parasitic capacitance, typically at 250 fF for a 70 µm x 80 µm pad. The inductor $I_{ind\ bondwire}$ bondwire represents the wire bonds' inductance, assuming the bond wire will add at least 1-2 nH/mm, with a total length of 7 mm, the total inductance of the wire bond was set to 15 nH. The second capacitor C_{trace} represents the PCB's parasitic capacitance, estimated to be 500 fF. The last resistor R_{scope} and capacitor C_{scope} pair represents the worst load condition when the output is directly probed with a passive probe from an oscilloscope. C_{scope} will be roughly 12 pF, we used 20 pF to create design margins. The scope's input resistance is usually 1 MΩ, assuming a 10x probe is not being used.

With this simulation setup, the op amp's stability is shown in Figure 3.23. The system's phase margin is still sufficiently high at 63.8 degrees. We simulated the op amp across the process corners and temperatures. The lowest phase margin was 58 degrees under the worst loading condition, demonstrating this design will be stable.

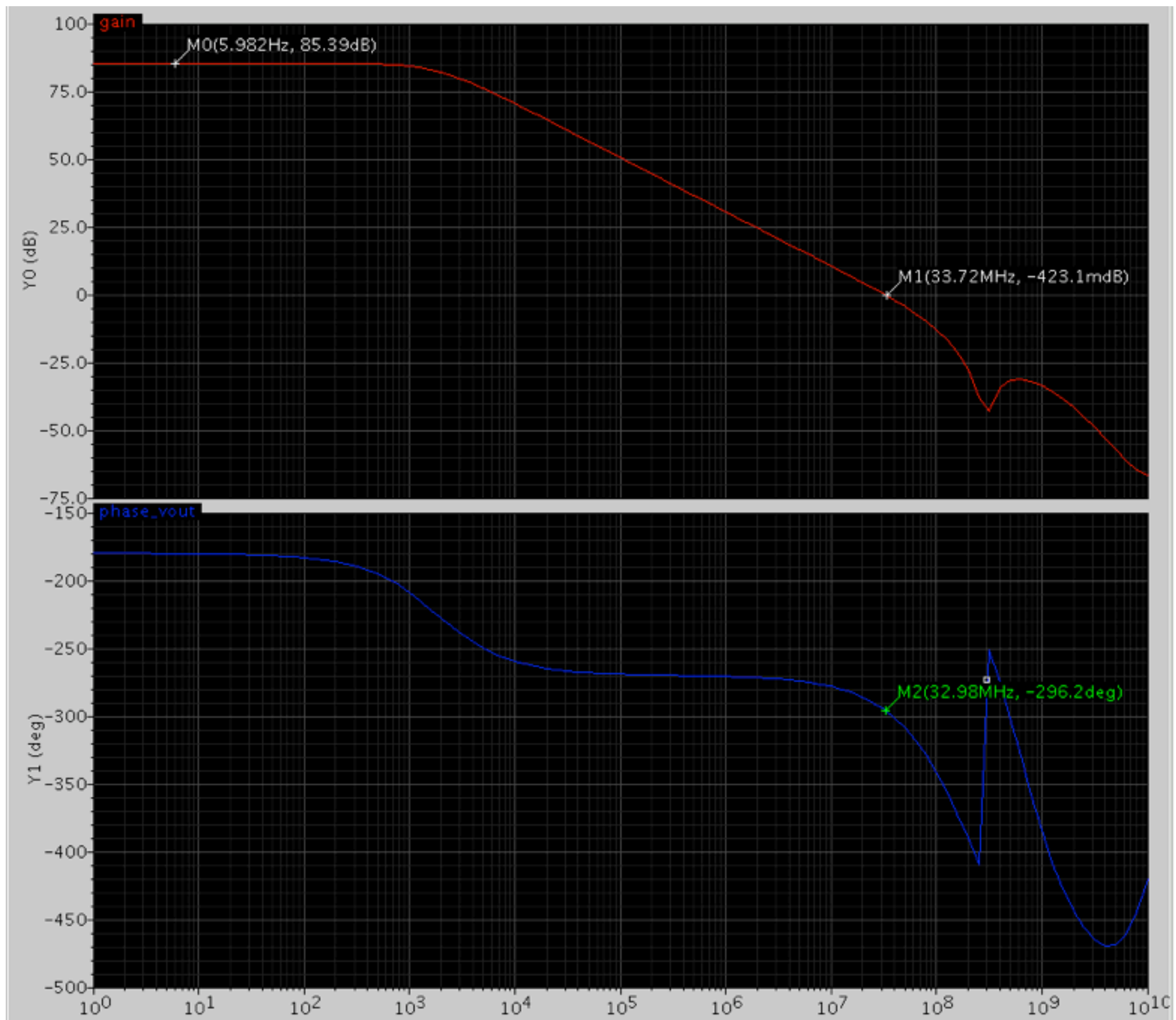


Figure 3.23: Bode plot of op amp with realistic load at V_{CM} = 1.65 V.

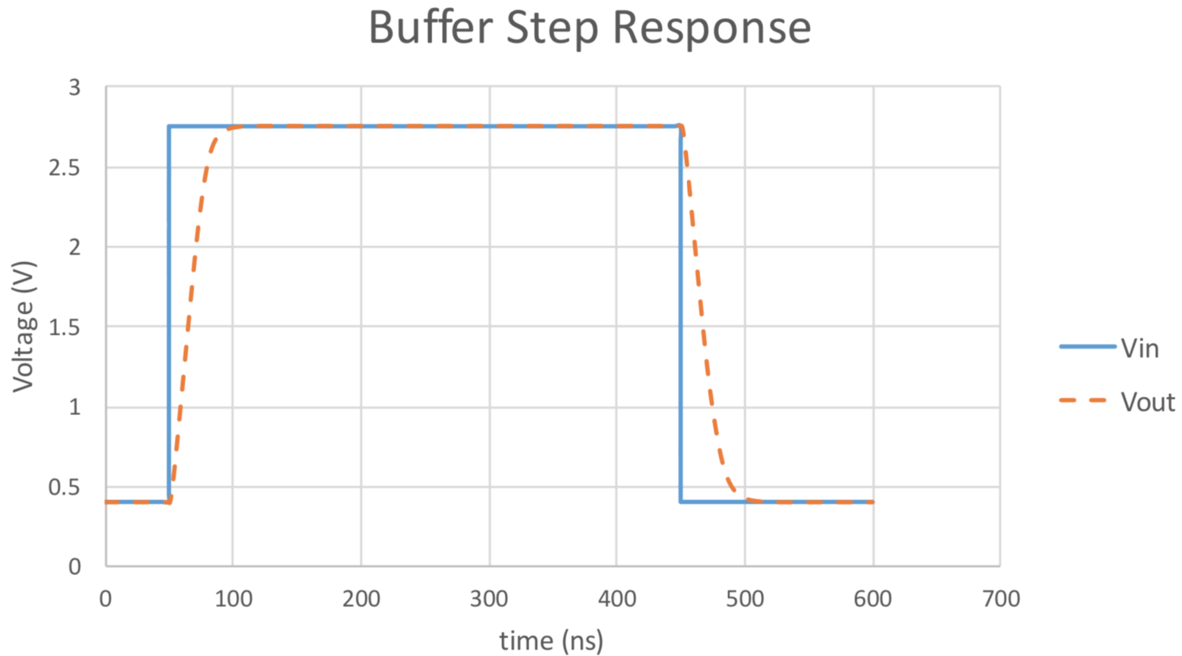


Figure 3.24: Step response of on chip buffer in closed-loop configuration.

3.1.4.5 Step Response

I simulated the op amp's step response in closed-loop configuration from 0.4V to 2.75V. We used a pulse with a rise-and-fall time of 1 ps as the input signal. Figure 3.24 shows the results. On both the rising and falling edges, the op amp's output settles to within 99.97% of the stepped voltage in the first 55 ns. The maximum positive slew rate is extracted to be 78.2 V/µs, and the maximum negative slew rate is extracted to be 63.7 V/µs. We expected the difference in positive and negative slew rates because the output stage does not provide an equal charge and discharge current to the compensation capacitor nor to the loading capacitor. However, both slew rates are sufficiently high enough to allow the output voltage to swing between 0.4 V to 2.75 V in less than 43 ns, much shorter than the designed settling time of 448 ns.

3.1.4.6 Layout Consideration

Because of the size of the devices used to build this op amp, the process variation across the wafer may cause performance issues, especially for the current-summing stage. If the load transistors have different device characteristics, the gain will not be the same for different input polarities. To account for potential offsets, such as threshold voltage variation, and that the devices are relatively large, we used the cross-coupled fingered technique during layout to minimize the effect of cross-wafer process variation.

3.1.4.7 Noise

I simulated the op amp's noise power spectral density (PSD) based on the extracted layout. Figure 3.25 shows the result from my simulation of the noise PSD from 10^{-4} Hz to 1 GHz for completeness. The input pairs' flicker noise dominates the overall system noise because of the input stage's gain. The simulated PSD follows the flicker-noise behavior, maximizing at lower frequency and decreasing as a function of $\sqrt{1/f}$, as Equation 2.8 shows. We calculated the overall input-referred noise of 554 µVrms by integrating the area under the PSD from 0.025 Hz to 29.83 MHz. We calculated the lower bound of 0.025 Hz by assuming that the longest continuous sampling would be 100 frames of data taken at 2.5 frames per second and that the upper bound of 29.83 MHz is the noise-equivalent bandwidth of a low-pass filter down the readout path. When it is input referred to the integration node at a pixel in Q1, this noise translates to 17.32 e^-, which accounts for only 4.2% of the total noise when the input refers to the integration node of a pixel in Q1.

3.1.4.8 Testability

Characterizing the op amp separately from the internal circuitry is essential to decoupling pixel performance. We used three transmission gates to insert a test path between the output of all pixels and the buffer. Figure 3.26 shows the test path mechanism. During normal operation, switch A and B will be turned on, allowing the signal coming from each pixel to be directly buffered off the chip. Switch combination B and C can be turned on while switch A is turned off, enabling a test voltage/signal to be passed directly into the buffer. Lastly, in case the op amp design does not work as expected, the switch A and C configuration can be used to sample the pixels' output directly off the chip without going through the buffer.

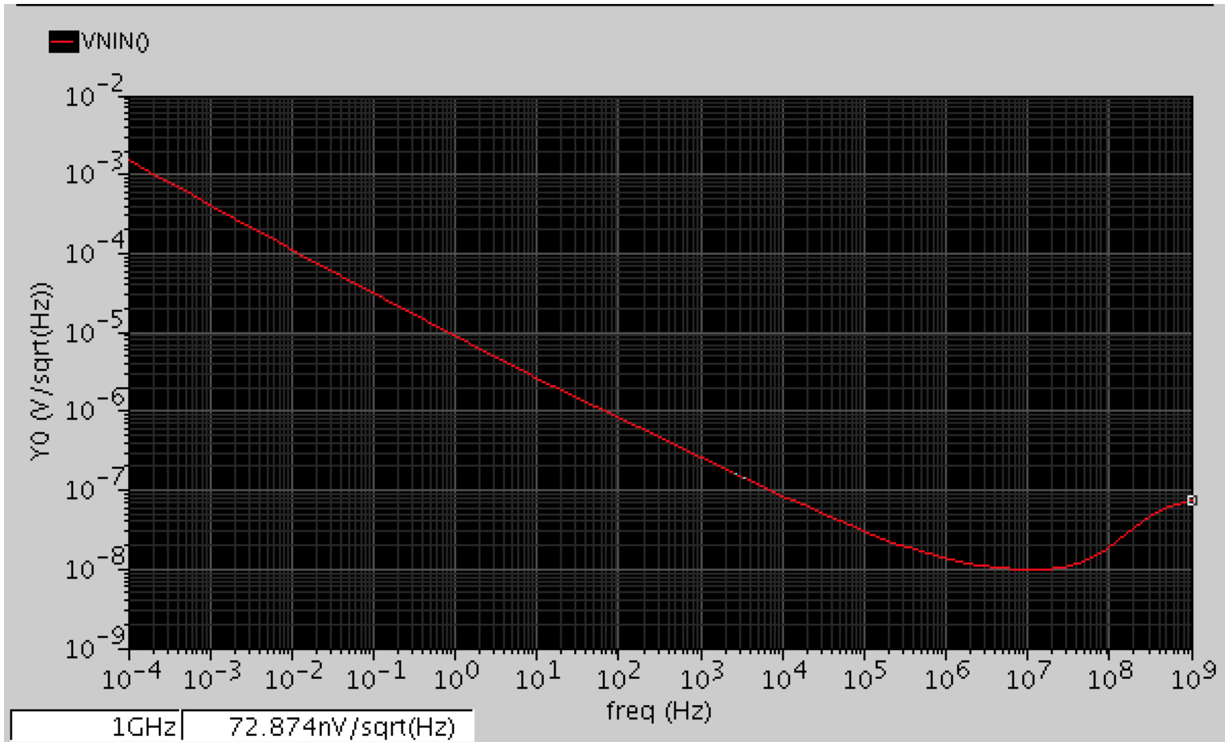


Figure 3.25: Op amp simulated input noise power spectrum.

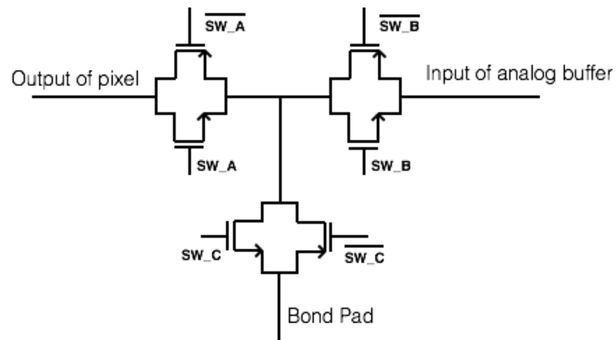


Figure 3.26: Three switches configuration for testability.

3.1.5 I/O Protection

I used 5 bond-pad designs in this work to provide ESD protection to the internal circuitry, as well as to prevent in-rush current damage.

The analog and digital signals both use the same configuration: the signal coming from the chip is decoupled from the bond pads through a 163 Ω poly resistor to limit current in case of an ESD event. The 2 diodes connect from the signal path to the power and ground respectively, preventing the signal going above VDD or below ground.

The second configuration is the power and ground connection to the core of the IC. The design is like the analog- and digital-bond pads that have protection diodes connecting to the bond pads' V_{DD} and V_{SS} ring. However, we replaced the poly resistor with a smaller 7.8mΩ metal 2 to minimize IR drop during normal operation, since the power and ground pads will carry significantly more current as compared to regular signal pads.

I designed the last bond-pads pair to provide power to the entire bond-pad ring. These cells' pads are isolated from the internal circuitry and directly connect to the bond pads' power and ground ring. Appendix A lists the chip-pin outs, along with the chip's bonding diagram when attached to a 120-pin Cerquad package.

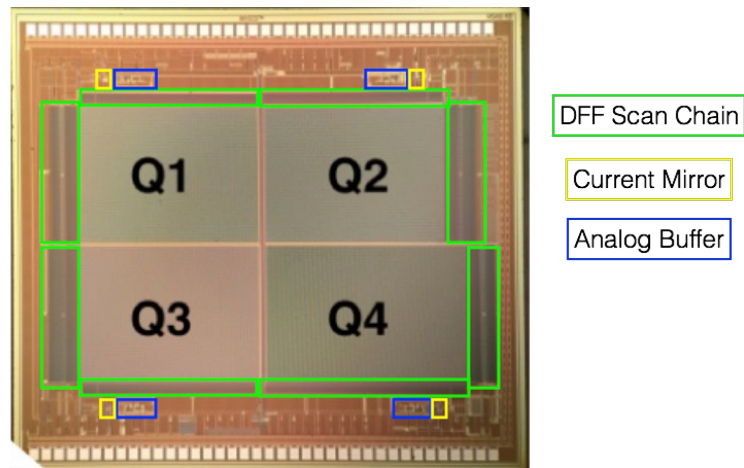
3.1.6 Fabricated CMOS Imager

The imager was fabricated in CMOSP18 Mixed Signal process by TSMC through CMC. Figure 3.27a shows the IC with major blocks labelled before any chip post processing.

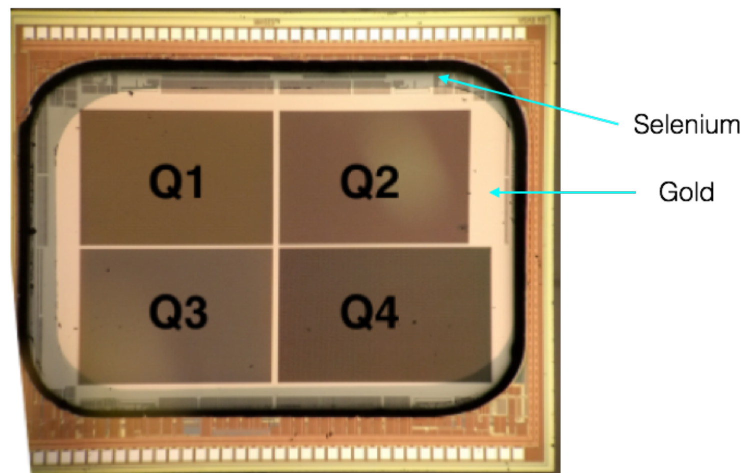
3.1.6.1 A-Se and Gold Deposition

Through post-processing, 16 µm of a-Se with 20 nm of gold acting as top electrode is deposited onto the CMOS imager. Figure 3.27b shows the die after deposition. Both a-Se and gold were deposited through thermal evaporation in the G2N cleanroom. The dice was placed inside a custom-designed shadow mask, exposing only the active array while shadowing the surrounding electronics and bond pads.

The coated die is then packaged using a 120-pin Cerquad package. The research team on campus then performed a special room-temperature wedge bonding because deposited a-Se could crystallize if exposed to high temperatures. Figure 3.28 shows the packaged die with wire bonds.



(a) Before post processing.



(b) After a-Se and gold deposition.

Figure 3.27: Unprocessed and post processed CMOS imager.

3.1.6.2 High Voltage Biasing and Epoxy Sealing

To form a stable mechanical connection between the bond wire and bond pad/surface, a high temperature or an external force can be used to form a stable contact. If high temperature is used, the a-Se will crystallize, meaning the conversion gain will drop and the device will lose its imaging capability. Moreover, since gold is a relatively soft material, especially at only 20 nm, any external force will likely push it away and make

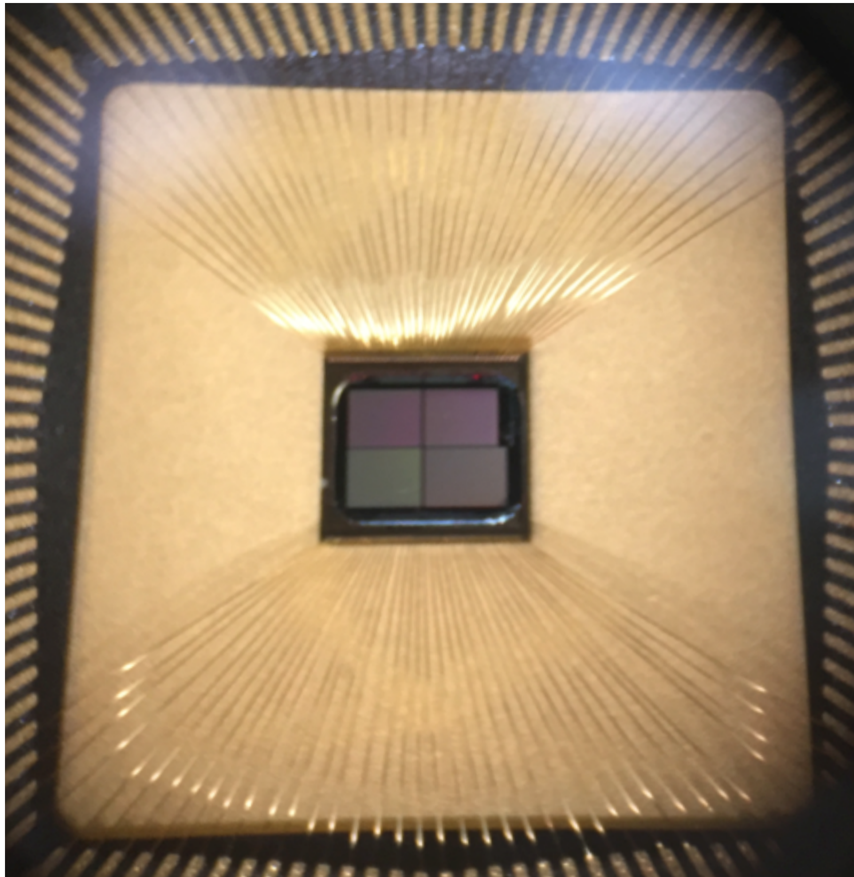


Figure 3.28: Wire bonded CMOS imager.

direct contact with the a-Se underneath. In addition, if the a-Se experiences a localized external force, it will become a seed for crystallization to start growing, which will significantly reduce the imager's operational life.

I used two methods throughout the system testing to apply high voltage to the top electrode. We first applied the high voltage through a probe tip, which requires an operator to carefully place the tip onto the gold without puncturing or scratching it. This method was quick and effective; however, it is a risky process since it can easily damage the top electrode and, since the tip often needs to be moved during early testing, damage the bond wires .

The second method applied high voltage through a thin wire glued to the top electrode with conductive adhesive, thus avoiding the mechanical factor of the probe tip

and wire bonding technique. We also used silver paste to glue the die into the package for this same purpose. This method was better in terms of reliability and stability, and we used it for most of the experiments, except during early-chip bring ups.

To protect the bond wires and avoid vibration in the system causing adjacent wires to short, we filled the package's cavity with MG Chemicals' 832C Translucent Epoxy. We chose this epoxy for its viscosity and semi-transparency, as well as its ability to cure under room temperature once mixed. We gently heated the part-A solution on a hotplate for roughly an hour until a sufficient amount could be extracted, then we mixed with the part-B hardening agent in a petri dish at a 2:1 ratio. We applied a few droplets of the final mixture onto the bond wires and the package's open area through a small syringe. We guided out most of the air bubbles formed during this process with a needle. The epoxy viscosity created sufficient surface tension from the cavity to the edge of the chip, preventing the epoxy from covering the chip's imaging area. Figure 3.29 shows the chip after making the high-voltage connection and curing the epoxy sealing.

3.2 External Hardware

I placed the bonded imager on a custom-designed 4-layer PCB, which we used to sample the analog data coming off the imager. As such, it will send the digitized data to the user terminal through an Opal Kelly XEM6310 evaluation board. This section describes this custom PCB's design.

3.2.1 PCB block diagram

The PCB consists of four major blocks, as Figure 3.30 shows. The figure shows the power connections in red, the digital communication connections in blue, and the analog data connection in green. The power portion generates supply voltages for both the imager and the ADC banks. To protect the imager from in-rush current and voltage spikes, the power supply to the ESD protection diodes inside the bond pads are powered on first. The full schematic of this 4-layer PCB can be found in Appendix B. We used this revision of the PCB to obtain the die's initial electrical characteristics and the optical test results. Figure 3.31 shows the PCB with its major blocks labelled.

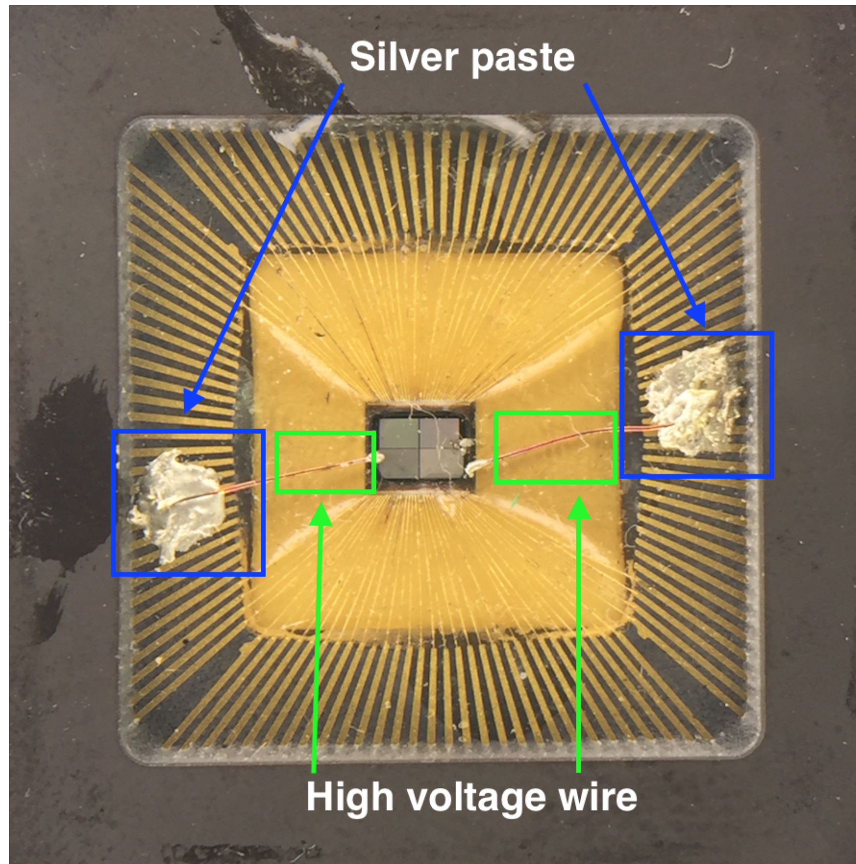


Figure 3.29: High voltage connected with epoxy sealant.

3.2.1.1 Pre-ADC Buffer

Although the signals on chip are buffered through a high-gain op amp in unity feedback, another discrete buffer on the PCB preserves signal integrity and conditions the imager output signals for the ADC to sample. We chose AD8021 was for its low noise, high-speed, and rail-to-rail-input and -output buffering range. With its 2.1 nV/$\sqrt{Hz}$ input-voltage-noise PSD, the total noise for the imager's maximum operational frequency (19 MHz) would be 9.15 µV, equivalent to 0.23 e^- when input referred to Q1 pixel-integration node.

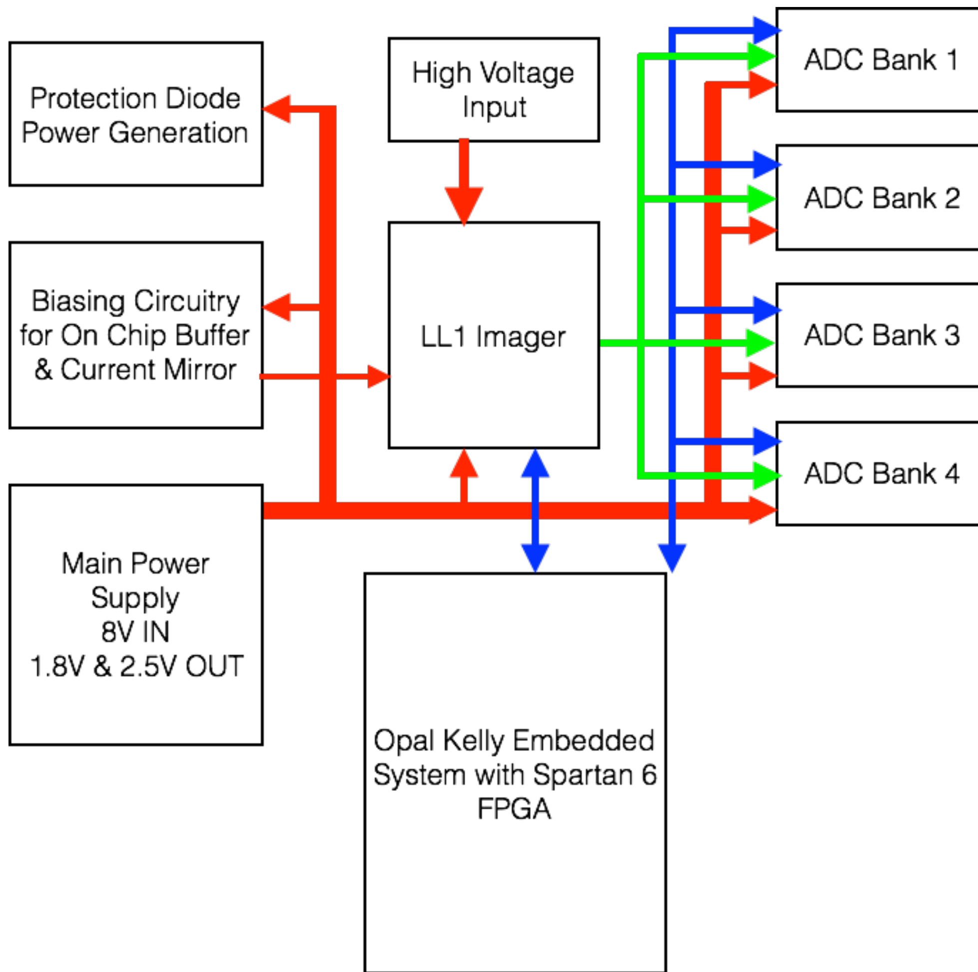


Figure 3.30: External hardware block diagram.

3.2.1.2 ADC

I used the 2MSPS AD7944 14-bit ADC to digitize the data because of its ease of implementation, high speed, and simple SPI interfacing. Also, since it can generate an internal reference voltage of 4.096 V, it eliminates the need of external reference-voltage circuitry, a common source of noise. Because of the large input capacitance, the ADC's kTC noise is small compared to the noise generated inside each pixel. The ADC's rms-quantization noise $V_{Q_{nrms}}$ can be calculated by [43].

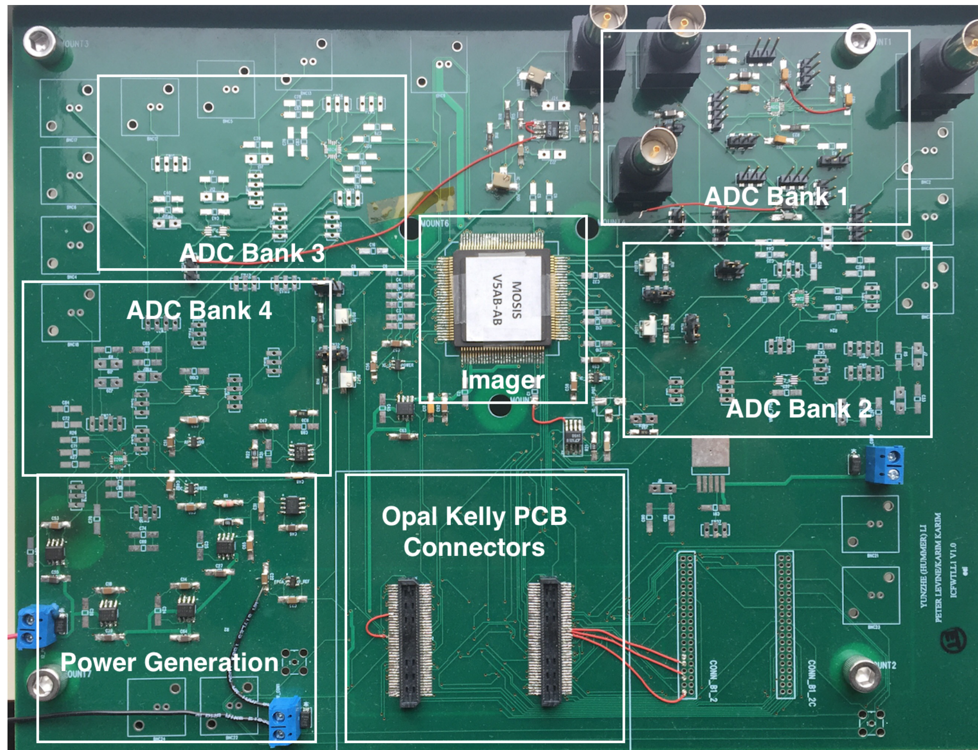


Figure 3.31: Rev0 PCB used for testing.

$$V_{Q_{nrms}} = \frac{V_{LSB}}{\sqrt{12}} \tag{3.23}$$

where V_{LSB} is the LSB voltage of the ADC. With a 4.096 V reference voltage and 14 bit precision, the quantization noise is 72 µV, or 2.25 e^- when input referred to Q1 pixel integration node . The ADC blocks were designed by following the design reference provided for this ADC.

3.2.1.3 Power and Grounding Scheme

Since the digital components switch constantly, meaning the current draw from the system's digital portion fluctuates. The sudden change in current can cause fluctuation in the DC voltage level. If the analog and digital circuits share a common power supply, the fluctuation can easily be coupled onto the analog signals and unnecessary noise. To

reduce the digital-to-analog cross talk, separate LDOs generate the AVDD and DVDD for the imager. Since the system's power efficiency and heat generation and dissipation were not primary concerns, all supplies on the PCB are generated using LDOs to lower the system noise.

Although we used a ground plane to lower the effect of common-ground impedance coupling, the instantaneous current draw change caused by the digital block could still be coupled into the analog ground. If the 2 grounds are connected anywhere on the PCB, the digital switching noise can easily couple into the analog blocks. Therefore, separating the 2 grounds on the PCB is highly desirable. However, the 2 grounds still need to be kept at the same potential, meaning that a connection between them is unavoidable. Using the star grounding scheme where the grounds are joined together off the PCB, normally at the power supplies' grounds, separates the PCB's 2 grounds yet still keeps them at the same potential.

I created a second revision of the PCB with additional capabilities, including the updated 16-bit ADCs and software-controllable DACs for various biasing voltages, which allow for a simpler and automated process to obtain a gain and offset map.

3.3 Control Software

I developed the software used to control and read the digitized data from the custom-designed PCB by referencing the STAR group's previous work [2]. The software can be broken down into three major blocks:

1. The Verilog block is responsible for interfacing and controlling and transferring data from the imager.
2. The C++ block is responsible for generating control signals and saving data from the imager to the local host.
3. MATLAB scripting is used to process and generate images from raw data, as well as calculate system noise.

3.3.1 Division of tasks between Verilog and C++

The C++ module is responsible for generating system start indicators, monitoring trigger tripped by the FPGA module, as well as saving the data taken from the Opal Kelly

into either binary, hex, or decimal formats. The FPGA is responsible for translating the start-indicator signal from the C++ GUI into a series of timing control signals for the IC and the ADCs while loading data read back from the ADC onto a buffer and for tripping a trigger when data is available for the GUI to save.

3.3.2 Verilog Hardware Description Language

The system's top module is responsible for communicating with the C++ software to provide and monitor incoming and outgoing trigger signals, as well as wires used to transfer the data between the FPGA memory module and the end user terminal. It also generates the indicator signal for the ADC to sample data at its input.

3.3.2.1 System State Machine

The HDL-state machine's top level is responsible for interfacing between the C++ control commands and the sub-modules, including the ADC and the IC-digital-control timing generation. As Figure 3.32 shows, the system maintains in the idle state until an initiate signal is received from the control software. Once the initiate signal is received, the system will synchronize the column-select clock (cs_clk) and the row-select clock (rs_clk), aligning the control signals for image capturing. This is a necessary step because the system-state machine runs off the ADCs' clock, which is much faster than either the cs_clk or the rs_clk.

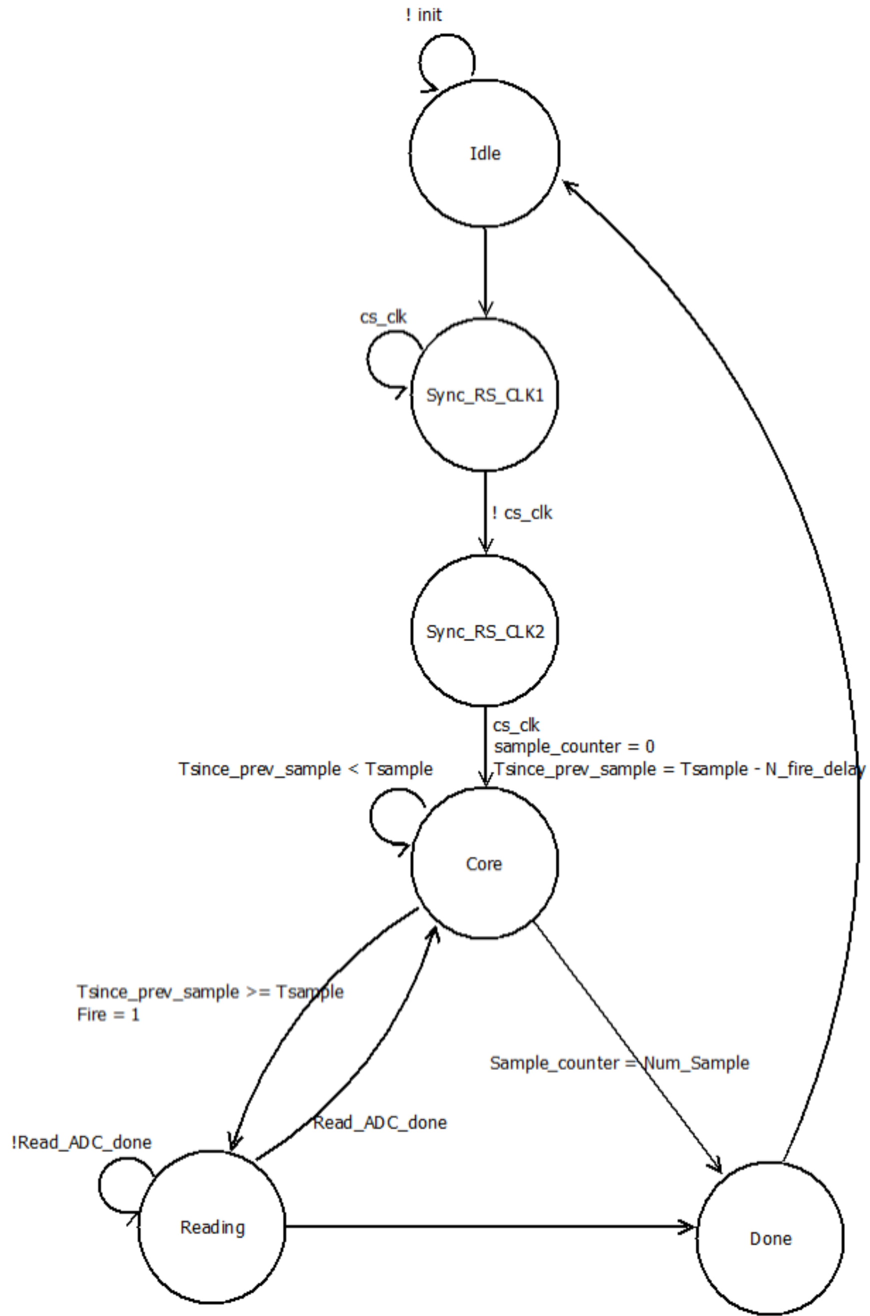


Figure 3.32: State machine of HDL.

Chapter 4

Experimental Results

This chapter presents the electrical and optical results obtained with the system. We used one chip without deposited a-Se for measuring the IC and PCB's electrical performances. Another chip deposited with a 20 µm-thick layer of a-Se and a 20 nm-thick layer of gold as the top contact is used to measure optical performance. Because of time limitations, only Q1 is fully characterized in this work.

4.1 Setup

For IC characterization, the custom PCB is powered up through four separate power sources. The FPGA board connects to the PC using a USB3.0 connection for sending and receiving control signals and data transfer. Figure 4.1 shows the optical experiment setup. We mounted the PCB inside a Faraday cage on an anti-vibration table, placing the bench-top power supply units outside the cage. We then covered the Faraday cage with 2 layers of shrouds and the imaging setup with anti-reflective black cloth to minimize light reflection and to further block ambient light during testing. We used optical rods place various LED sources directly above the imager. During the experiment, we placed a set of filters (NEK01S from Thorlabs) with different optical densities between the LED and the imager to accurately control the illuminance at the imager. We could not change the LED current by controlling the biasing voltage for this measurement since the LED's output luminance is not linear with its biasing voltage. We also imaged the R3L3S1N test target from Thorlabs during the experiment. We placed a convex-plano lens between the test target and the imager to collimate the light. We placed ta

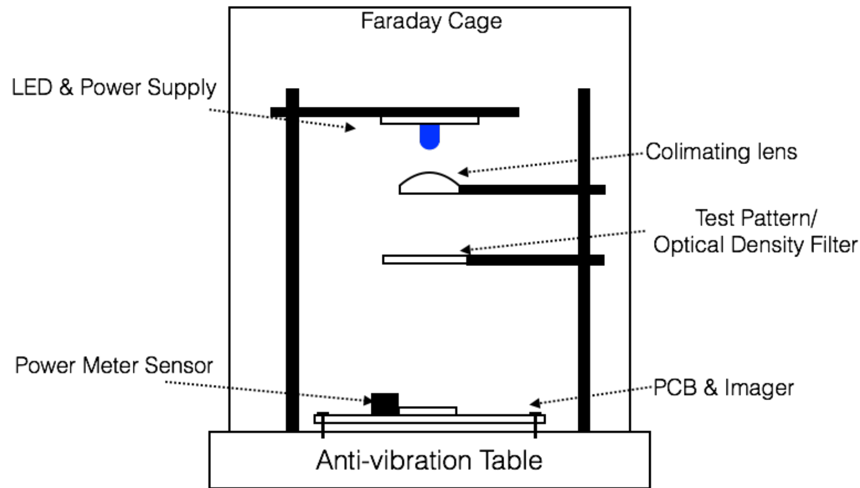


Figure 4.1: Optical experiment setup.

Newport-power-meter sensor right beside the IC to monitor and record the illuminance. It reports in radiant power.

4.1.1 LED Luminance Conversion

To characterize and extract the imager's optical performance, including conversion gain, optical-response linearity, and SNR, the signal seen at each pixel must be calculated in number of photons. Most LED and light-source manufacturers define device brightness in luminous intensity, often with the units of milli-candela (mcd). To estimate the number of photons seen by each pixel during testing, mcd (a luminous-intensity unit describing the brightness of a light-emitting source) must be converted into lux (the illuminance level seen by the imager). The lux value can then be used to calculate the radiant power at each pixel. With the known photon energy at a given wavelength, the number of photons can be estimated. With the numbers of incoming photons known, the measured results can be compared to the simulation model.

Luminous efficacy, quantified in lumens per watt, is the ability of a light source to emit visible light with a given amount of power, which is also a function of the wavelength of light (color). In other words, if the same amount of power is used to create light of different color, the resulting brightness will be different to the human eye and, therefore, would have different luminance levels. Figure 4.2 characterizes this nonlinear

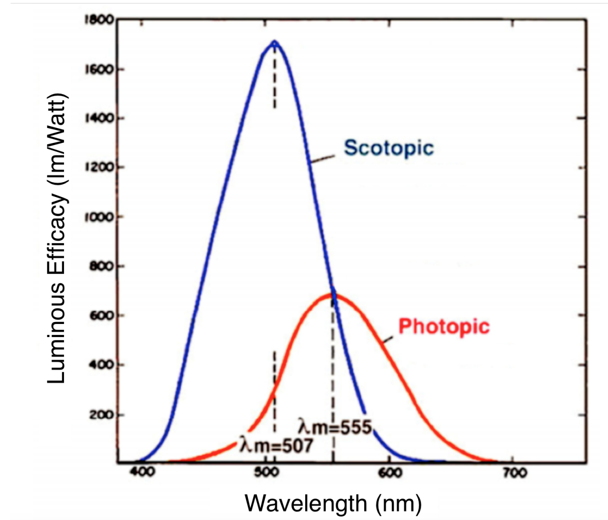


Figure 4.2: Scotopic and photopic vision. [45]

sensitivity by showing the scotopic and photopic vision's luminous efficacy K (lm/W) across the visible spectrum.

Given the wavelength of light and luminance shown by the luminous efficacy table, the number of photons can be calculated. We used a blue LED (TLHB5400, manufactured by Vishay Semiconductor) during testing. Figure 4.3 shows the experimental setup. According to the data sheet, this LED has a typical luminous intensity I_V of 15 mcd centered at 466 nm with 20 mA of forward-biasing current. We show the conversion process from the luminous intensity I_V (mcd) to illuminance-level E (lux) below. The light source's luminous efficacy can be used to calculate the radiant power P (nW/cm^2), then the exact number of incoming photons can be extracted by dividing the radiant power (normalized to single-pixel area) by the photon energy given by Equation 4.8. The number of photons is needed to match the measured results with the simulation model.

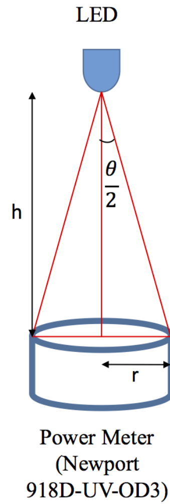


Figure 4.3: Illuminance calculation setup.

1. Assuming the light source is uniform and isotropic within the sensing area of the power meter, its luminous flux Φ_V with units of lumen (lm), which is independent of the setup's geometry, equals to the luminous intensity I_V in candela (cd) times the solid angle Ω (sr), meaning

$$I_V = \frac{\Phi_V}{\Omega} \tag{4.1}$$

2. To extract the absolute value of luminous flux Φ_V with the setup's geometries taken into account, i.e. calculating the luminous flux landing on a power meter sensor with radius r, the fraction of solid angle can be calculated through simple geometry. As Figure 4.3 shows, the apex angle θ that is used to calculate the solid angle Ω can be found by

$$\frac{\theta}{2} = arctan\left(\frac{r}{h}\right) \tag{4.2}$$

where r is the radius of the sensor in mm, and h is the distance between the sensor and the LED, also in mm.

3. We can then convert the apex angle calculated previously from degree to fraction of a solid angle Ω with units of steradian (sr) by using

$$\Omega = 2 \times \pi \left(1 - cos\left(\frac{\theta}{2}\right)\right) \tag{4.3}$$

4. Therefore with the luminous flux normalized to the setup's geometry, the illuminance E seen by the sensor in lux is given by

$$E = \frac{\Phi_V}{\pi \times r^2} = \frac{I_V \times \Omega}{\pi \times r^2} \quad \left[lux = \frac{lm}{m^2}\right] \tag{4.4}$$

   where r is the radius of the sensor in m.

5. Once the illuminance E is found, the radiant power per unit area P can be found with the luminous efficacy (shown in Figure 4.2) at the source's wavelength by

$$P = \frac{E}{K} \quad \left[\frac{W}{m^2} = \frac{J}{s \times m^2}\right] \tag{4.5}$$

   where K is the luminous efficacy in lm/W, and the total energy E_{total} of the incidental photon landing in a sensing area can be found by

$$E_{total} = P \times A \times t \quad [Joules] \tag{4.6}$$

   where A is the sensing area in m^2, and t is the integration time in seconds.

6. In order to determine the total number of incidental photons with a given sensing area, we must find the photon energy E_{ph} of each photon at the given wavelength by using

$$E_{ph} = \frac{h \times c}{\lambda} \quad [Joules] \tag{4.7}$$

   where h is Planck's constant, c is the speed of light and λ is the wavelength of the incident photon.

7. Finally, the number of incidental photons n_{ph} landing on the sensing area can be found by dividing the normalized total photon energy E_{total} with the individual photon energy,

$$n_{ph} = \frac{E_{total}}{E_{ph}} \tag{4.8}$$

The luminous efficacy for the LED used is 1056 lm/Watt. We placed the LED at several different heights to validate the calculation method. We measured the radiant power with the Newport 918D-UV-OD3 power meter. Figure 4.4 shows the calculated-versus-measured results.

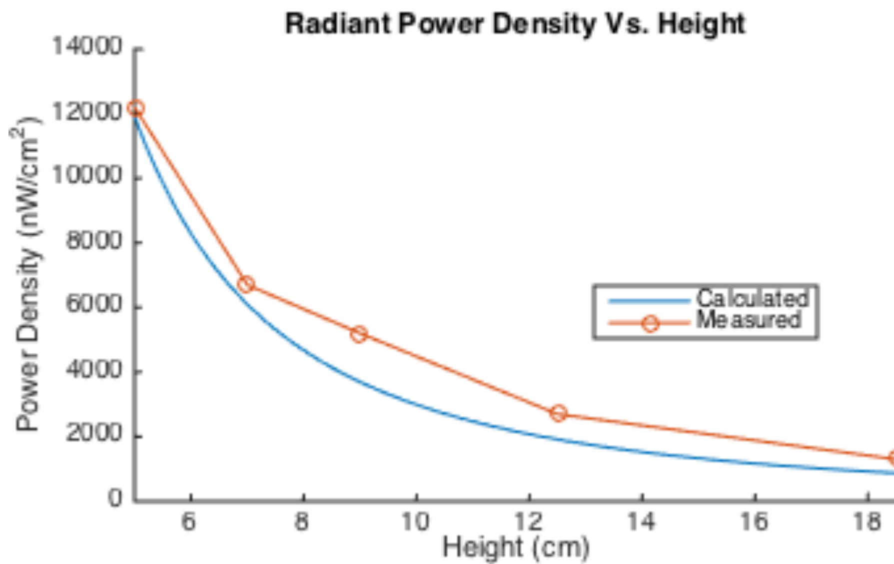


Figure 4.4: Comparison between measured and calculated radiant power density across different height.

4.2 Measured Imager Performance

This section will discuss the imager's electrical and optical performance.

4.2.1 Electronics Characterization

To characterize the imager's performance, the noise and linearity of components on the readout path, including the ADC (AD7944) and the off-chip unity-gain buffer (AD8021), must be characterized first. Knowing the imager's voltage range is 0.4 V to 2.75 V, we generated a test input with a DC power source decoupled with a 10-µF capacitor.

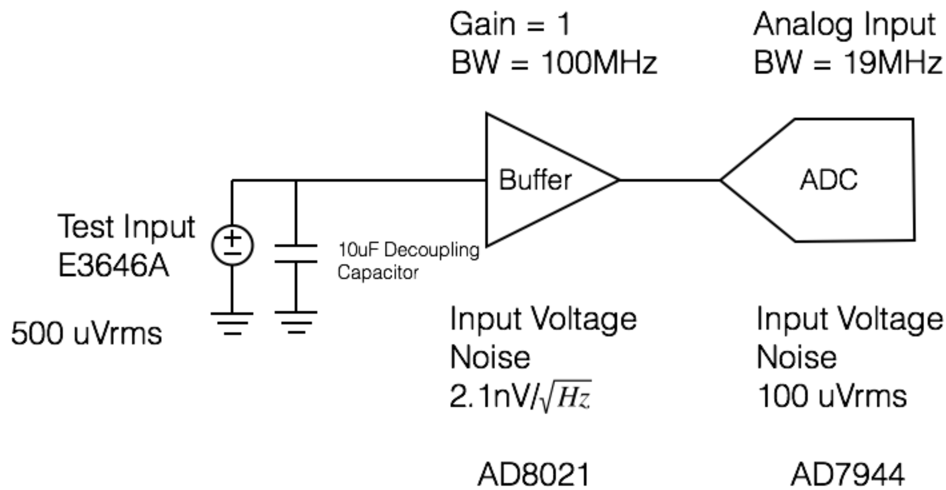


Figure 4.5: Off-chip readout path measurement setup.

4.2.1.1 Noise Performance of Off-Chip Buffer and ADC

Figure 4.5 shows the component on the readout path after the signal is passed off the chip. The data will go through unity-gain buffer first, which conditions the signal and decouples the high-input capacitance of the ADC (AD7944) from the on-chip buffer.

I applied the test input through an E3646A bench-top power supply, which has a noise of 500 µVrms [47]. A 10-µF capacitor at the supply's output decoupled the input signal before the signal entered the unity-gain buffer.

The unity-gain buffer AD8021 is a low-noise high-speed amplifier built for 16-bit ADCs. Figure 4.6 shows the noise PSD. We broke down the buffer's noise calculation into two sections. The first is the plot's 'linear' region between 10 Hz and 10 kHz, where the dominant noise source is flicker noise. We extracted the noise between these frequencies to be 2.26 µVrms. Although the buffer has a bandwidth of 200 MHz, the upper bound of white noise from 10 kHz onwards is limited by the low-pass filter imposed by the ADC's input resistance and capacitance, with -3 dB frequency of 19 MHz [49] and noise-equivalent bandwidth of 29.8 MHz. The total contribution of white noise between 10 kHz and 29.8 MHz is 11.25 µVrms. The unity-gain buffer adds a total of 13.51 µVrms of noise to the readout path.

The ADC used (AD7944) has a typical noise of 100 µmVrms [49], which includes the quantization noise as well as thermal noise from the sampling capacitors.

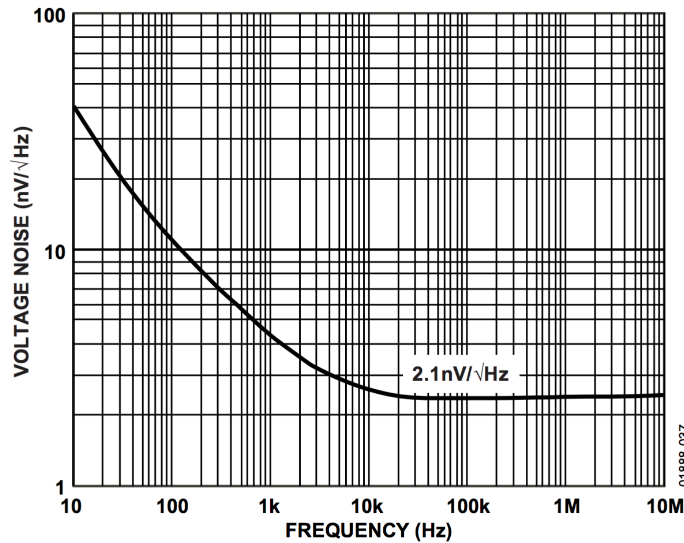


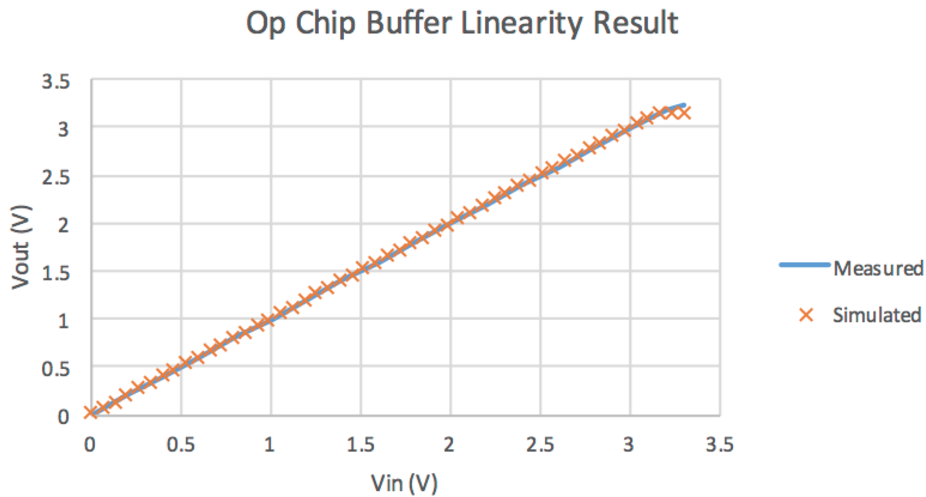
Figure 4.6: Noise power spectral density of AD8021. [48]

Therefore, with a DC supply as input, including the unity-gain buffer AD8021 and the ADC AD7944, the total calculated noise $V_{rms_{Total}}$ is 510 µVrms. This translates to 2.04 DN after digitization. We used the DN as the unit of digitized data coming out of the ADC wherein 1 DN is equivalent to 1 LSB of the ADC. The total noise measured in this experiment setup was 373 µV at a common-mode voltage of 1.65 V, which translates to 1.497 DN. Since the dominant noise source in this experiment was from the test input source, the lower measured noise is most likely because the supply has a lower noise, as the data sheet states. However, we expected the ADC noise to be higher than 100 µVrms, as the data sheet states, for 2 reasons: The first reason is that the layout and routing of the PCB trace and power/ground plane did not maximize the ADC's noise performance. The layout suggested by the data sheet was not precisely duplicated, and the lead-frame-chip-scale package (LFCSP) prevented the center ground pad from being properly soldered onto the PCB. Moreover, because of a mistake in the AD7944 datasheet connection block diagram, the analog power supply (AVDD) had to be shorted to the digital supply (DVDD) to apply the appropriate operational voltages.

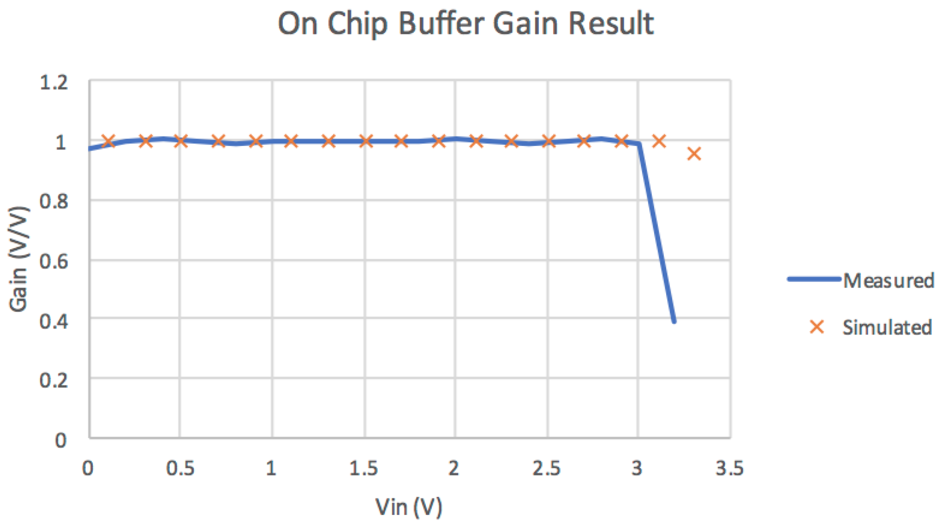
By calculation, the buffer and ADC had a total noise of 100.91 µVrms, which is only 3.7 e^- when input is referred to the integration node of a pixel in Q1, accounting for less than 0.16% of the pixel's noise.

4.2.1.2 On Chip Buffer

I tested the on-chip-rail-to-rail-unity-gain buffer through the tri-switch configuration. We applied a test voltage directly to the input of the buffer and used a high-precision multimeter to measure the buffered voltage at the buffer's output. The readout chain should be avoided to isolate the potential gain reduction from off-chip components. Figure 4.7a shows the sweep's result, along with the simulated outcome, while Figure 4.7b shows the measured and simulated buffer gain shown. The average gain from 0.6 V (reset voltage) to 2.75 V (maximum output voltage of on-chip-buffer-output stage) is 0.994 V/V. Compared to the simulated gain of 1.000 V/V, the difference is 0.602%, an acceptable gain considering the buffer has a simulated noise of 554 µVrms noise. We used 0.6 V as the lower boundary in this calculation because we used 0.6 V instead of 0.4 V during experiments to ensure that the current mirror stays in the saturation region. Moreover, the digital multimeter used to measure the output voltage is only precise down to 0.1 mV, and as a result, it will impose a limitation on the gain measurement's accuracy. As discussed in the design chapter, since the op amp's output is a common-source stage, it is unable to buffer signal close to V_{DD}; therefore, we observed a nonlinear behavior above 3 V.



(a) On chip buffer linearity.



(b) On chip buffer gain.

Figure 4.7: On chip buffer linearity and gain measurement vs simulation results.

To extract the noise, we again used the same configuration for characterizing the off-chip buffer and ADC, applying the test voltage at the on-chip buffer's input. The on-chip buffer's simulated noise was 554 µVrms at a common-mode voltage of 1.65 V.

Adding it to the previously calculated noise that used this test setup, the expected noise should be 753 μVrms = 3.01 DN. The measured noise was 3.21 DN at the common-mode voltage of 1.6 V, and the higher-measured noise could be explained with the same reasoning from the previous measurement setup.

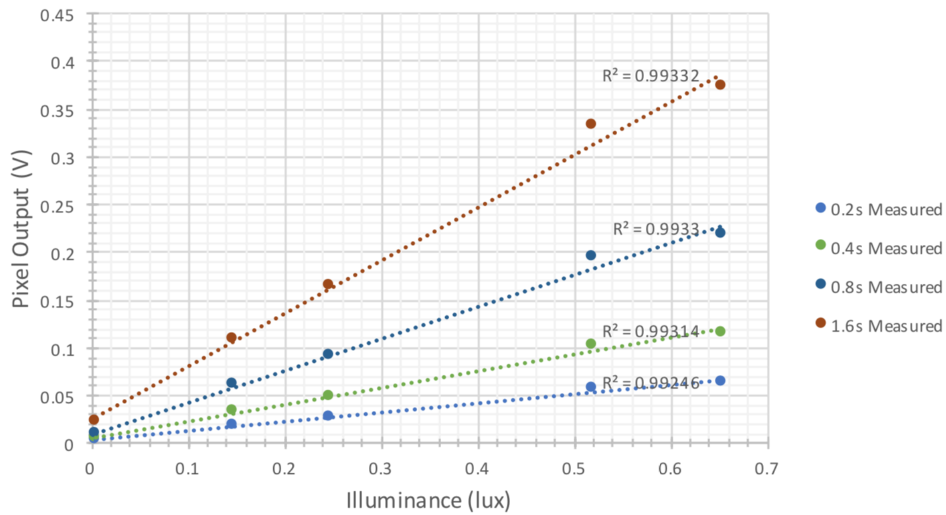
4.2.2 Optical Response Characterization

This section will present various measurements for Q1.

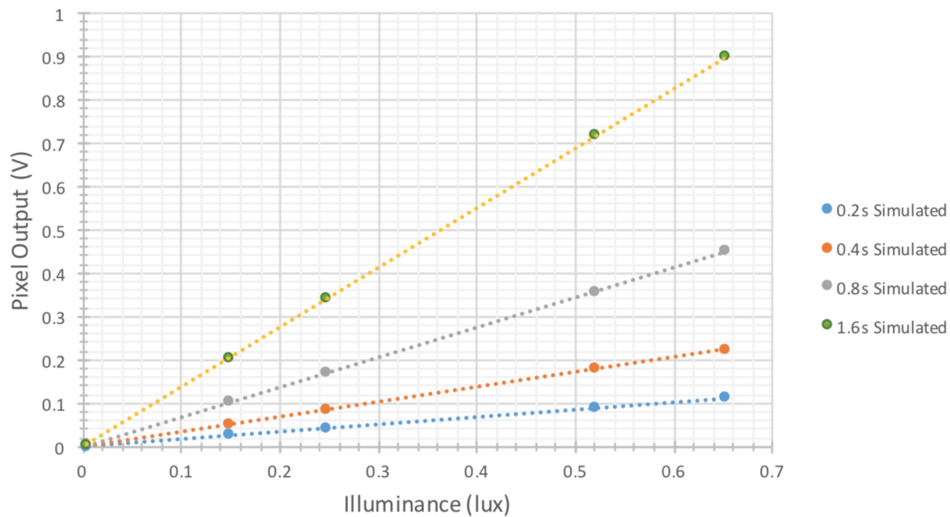
4.2.2.1 Pixel Linearity, Full Well Capacity and Effective Conversion Gain

I measured the imager's optical linearity by exposing the system to a control luminance using the method described in the previous section. Figure 4.8a shows the averaged measured optical response of all pixels in Q1 at low-illuminance level across a few integration times with a-Se biased at 3V/μm. We updated the simulation model introduced in Chapter 2 with a few measured parameters, including the CMOS circuitry's leakage current and an actual pixel size of 7.76 x 7.76 μm^2, the lower-than-anticipated quantum efficiency of a-Se at 3 V/μm and the transmittance of the top gold electrode. We kept the a-Se biasing voltage low because of the short distance between the high-voltage wire and the chip surface. The top passivation layer on the die was only 1.75 μm, which has a breakdown voltage of 37 V. Additional post-processing, such as spin coating or the thermal evaporation of a thin layer of polyimide onto the chip surface, could increase this breakdown voltage to over 500 V. However, such processes have a minimum requirement on die size or otherwise require special adaptive pieces to be built for a chip like this to be coated. For these reasons, we did not do these post-processes for this work. Note that the fourth illuminance data set in Figure 4.8a is constantly higher than the linear fitted line across all integration periods, this is likely caused by the non-linearity of the optical density filter used to create the desired illuminance.

Figure 4.8b shows the simulated results with estimated illuminance.



(a) Measured data, averaged across array Q1.



(b) Simulated data.

Figure 4.8: Pixel output vs. low illuminance at various integration times with wavelength of incident light peaking at 466 nm.

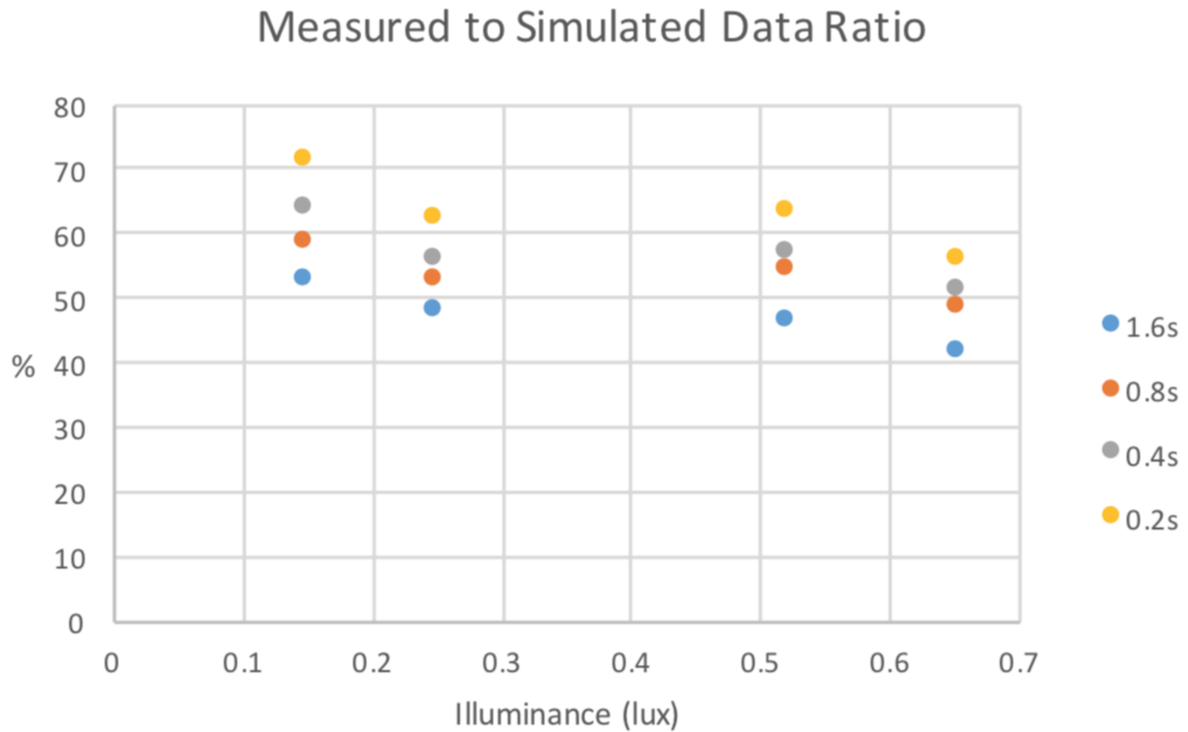


Figure 4.9: Measured to simulated ratio.

R^2 is a statistical measure of how close the data fits a linear regression. It is calculated by minimizing the distance between the fitted line and all data points. R^2 values of the measured data show that the optical-response linearity of the Q1 pixel design is fairly linear, even at low luminance level, and is almost constant across integration times. The signal also increases with longer integration period as expected. However, comparing the measured and simulated pixel outputs at each integration period (as Figure 4.9 shows) shows that the measured pixel-output voltage is roughly 50% to 70% of the simulated data. A few potential causes include

1. The integration capacitance assumed during simulation, calculated based on device size through schematic simulation, was smaller than the actual capacitance in the pixel; therefore, the simulation used a higher conversion gain than the pixels actually have. Given the calculated integration capacitance of 3.67 fF, the actual integration capacitance could easily vary up to +/- 30%. The total integration at

the integration node can be extracted if test devices with their terminals routed off chip directly; however, because of time and space limitations, it was not done on this design.

2. The quantum efficiency of a-Se for light at wavelength of 466 nm could be lower than the assumed 20% at 3V/μm, since it was extrapolated from Figure 1.10. The extrapolated number could have an error margin of up to 20% for light at 466 nm and up to 50% for light at 560 nm with the quantum efficiency extrapolated to be 4%. This could be measured and verified separately; however, since doing so would require the fabrication of selenium test cells, which are time consuming, we did not do so for this work.

3. From a literature review, we found that the thin, gold, top electrode would have an optical transmittance of 58% at 466nm and 78% at 550nm when it is only 7.2 nm-thick [50]. Given that the gold's thickness is 10 nm, we expected the transmittance decrease but no more than 10%.

Combining these variations together, the simulated data could deviate up to 67% from the measured results at wavelength of 466 nm and up to 72% for wavelength at 560 nm, making the difference between simulation and measured results more than acceptable.

Figure 4.10 illustrates the measured and simulated linearity results of up to 85 lux with 400 ms of integration, taken with a green LED (wavelength of 550 nm). Comparing the measured data to the simulated data, the maximum difference is 31.4% with the quantum efficiency of light at 550nm extrapolated to be approximately 4%. Since the error margin of green light is up to 78%, this difference is expected and acceptable. This plot demonstrates that the incoming signal of higher-than-40 lux was high enough to saturate the imager.

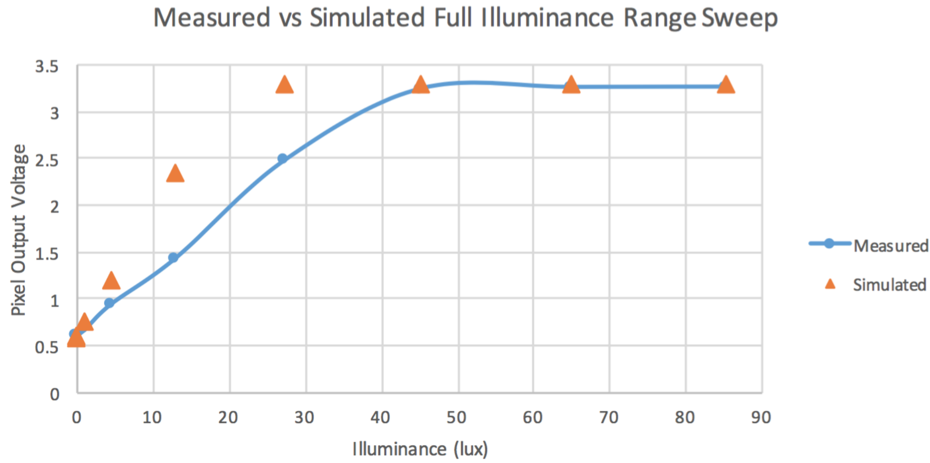


Figure 4.10: Pixel output across wide illuminance range at 0.4s integration with wavelength of incident light peaking at 550 nm.

The average full-well capacity of 57.6 ke$^-$ can also be extracted from the plot for pixels in Q1. The difference compared to the capacity of 75 ke$^-$ is caused by the discrepancy in total integration capacitance, as well as the decreased voltage-operating range since the reset voltage was set to 0.6 V instead of 0.4 V to ensure the current mirror's operation. The effective conversion gain of 0.82 µV/e$^-$ for green light at wavelength of 550 nm and 4.82 µV/e$^-$ for blue light at 466 nm can also be extracted from these measurements. The effective conversion gains are much lower than the estimated value since the quantum efficiency assumed during early simulations was close to unity while the true QEs for blue and green at the used biasing voltage are only 20% and 4%, respectively, and the simulation model used to generate the estimated conversion gain also ignored the optical transmittance of gold. Note that this experiment used a green LED with a wavelength of 550 nm because the blue LED used for low-light characterization does not have a high enough luminance to saturate the imager.

4.2.2.2 Pixel Leakage Characterization

One of my most important design goals was leakage suppression, which enables long integration. The overall leakage is measured across the array. Figure 4.12 shows the output. Notably, the array's output settles to just above 1.8 V after 12 seconds of integration, caused by the 3 sources of leakage in each pixel: the protection diode, the reset

devices while operating in weak inversion, and a-Se dark current when it is biased, as Figure 4.11 shows.

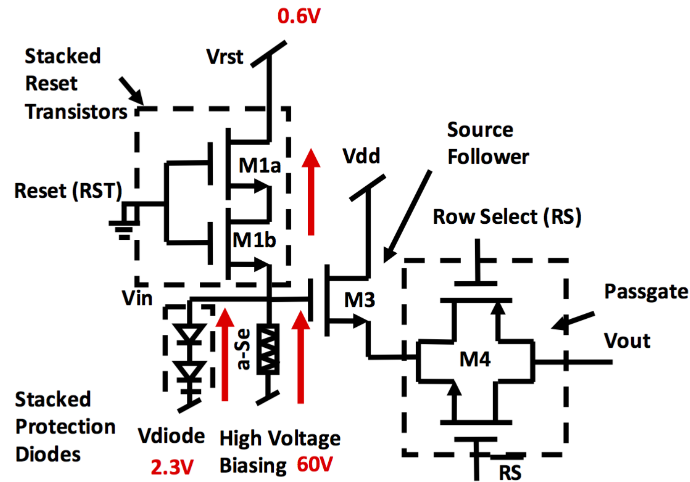


Figure 4.11: Q1 pixel schematic in the integration phase with leakage current directions shown with arrows.

The diodes will try to pull the integration node voltage towards V_{diode} (constant at 2.3 V), while the reset device will try to pull the voltage down to V_{RST} (constant at 0.6 V) during the experiments. Since the pixel voltage increased for the first 6 seconds, the diode is the dominant leakage source when the integration voltage is low. When the potential difference across the diode is reduced from the increasing voltage at the integration node, the leakage current through the reset device will become similar in magnitude to the diode leakage current. At higher voltage, the leakage current flowing into the integration will equal the leakage current flowing out, therefore, causing the net voltage change at the integration node to be close to 0 V.

Moreover, this settling behavior also affects the incoming signals as the integration period increases, especially when the signal is weak. Assuming the imager is exposed to a constant light source, as the integration time increases into the steady-state region the imager's conversion gain will be reduced. The reset transistor's leakage current will, therefore, increase and pull the integration voltage towards the steady-state value. At the same time, though, the net leakage current flowing through the integration node will remain largely unaffected; therefore, the leakage current's shot noise will not be reduced. The next section will describe the settling effect's impact on SNR.

The leakage current from both the electronics and a-Se can be extracted from Figure 4.12 as well. We calculated the dark current of a-Se as 0.2579 fA per pixel, similar to dark current extracted from the group's previous work, which yields a dark current of 2 pA/mm^2 (or 0.12 fA/pixel area) [13]. We measured the leakage current of the protection diode and reset device as 1.46 fA. The circuit simulation yielded a leakage current of 66.7 fA, which we expected since foundries commonly report the worst-case leakage current in the device model, while the lot-measured leakage current is an order of magnitude lower.

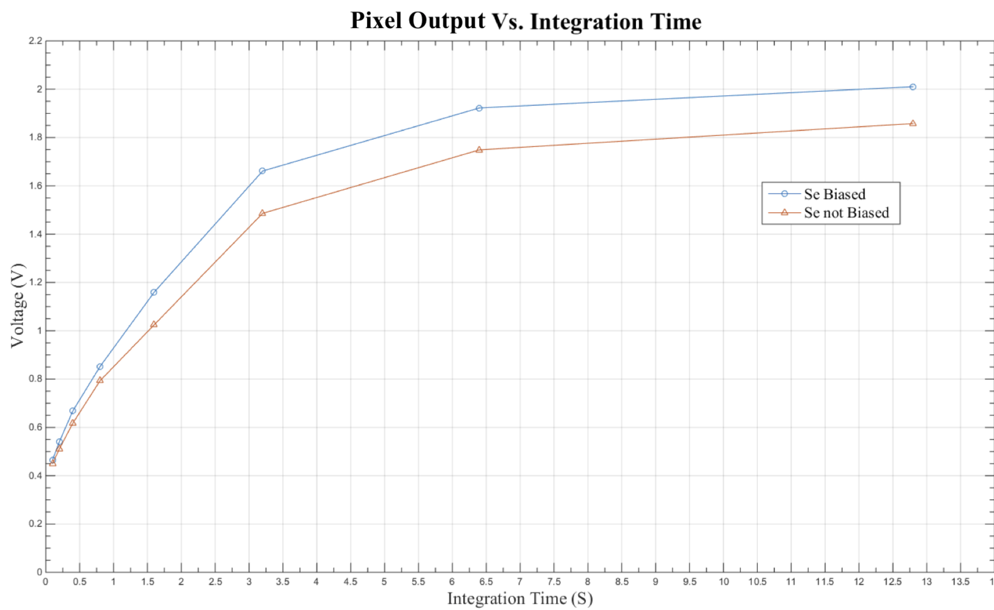


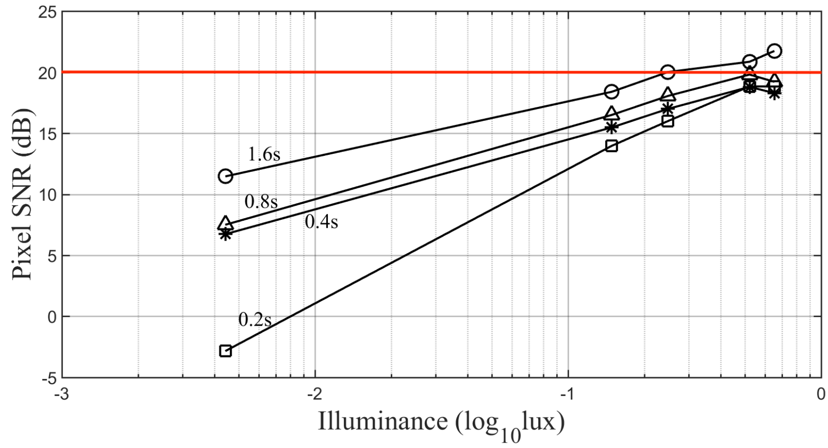
Figure 4.12: Averaged pixel output vs integration time.

4.2.2.3 SNR and Noise Characterization

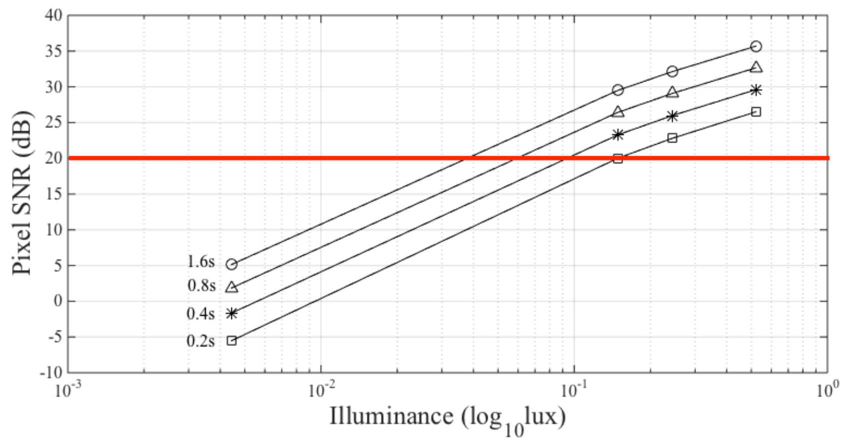
Figure 4.13 shows the imager's simulated and measured SNR at low-illuminance levels. Integration periods of longer than 0.8 s at 0.05 lux with 466 nm light source, from both measured and simulated results, demonstrate a SNR of more than 13.97 dB. This illuminance level (0.05 lux) is a significant milestone as it is the lower boundary of moonlight illuminance [51] and shows that this imager can perform moonlight imaging. Furthermore, the measured SNR of 1.6 s is still above 10 dB at 0.004 lux, which is close to the

illuminance of a moonless clear sky with airglow (0.002 lux), meaning the imager can produce recognizable images based on the Rose criterion in a moonless illuminance environment. Moreover, both simulated and measured results achieved an SNR of higher 20 dB at 0.25 lux (upper boundary of moonlight illuminance), which means the system can generate images with excellent quality based on the ISO 12232 standard.

In both the simulated and measured plots, SNR increases with increased integration time, proving that longer integration time is a valid method for increasing SNR in low-light conditions. However, the linearity of measured SNR does not track the simulation model well. Since the averaged pixel-output voltage of Q1, studied in an earlier section, was very linear, the nonlinearity in reported SNR is most likely caused by the ambient environment, including motion, light leakage, power supply noise, and main supply noise that may have occurred during measurement.



(a) Measured SNR.



(b) Simulated SNR.

Figure 4.13: Signal and SNR vs illuminance for various integration periods, with red line indicating target SNR.

Although longer integration will improve the imager SNR, the transient-leakage-current settling effect mentioned in the previous section will impose an upper limit on SNR. This can be clearly observed in Figure 4.14, which shows the weaker signals' SNR will degrade at 3.2 seconds of integration while that as the signal gets stronger the SNR will start increasing again.

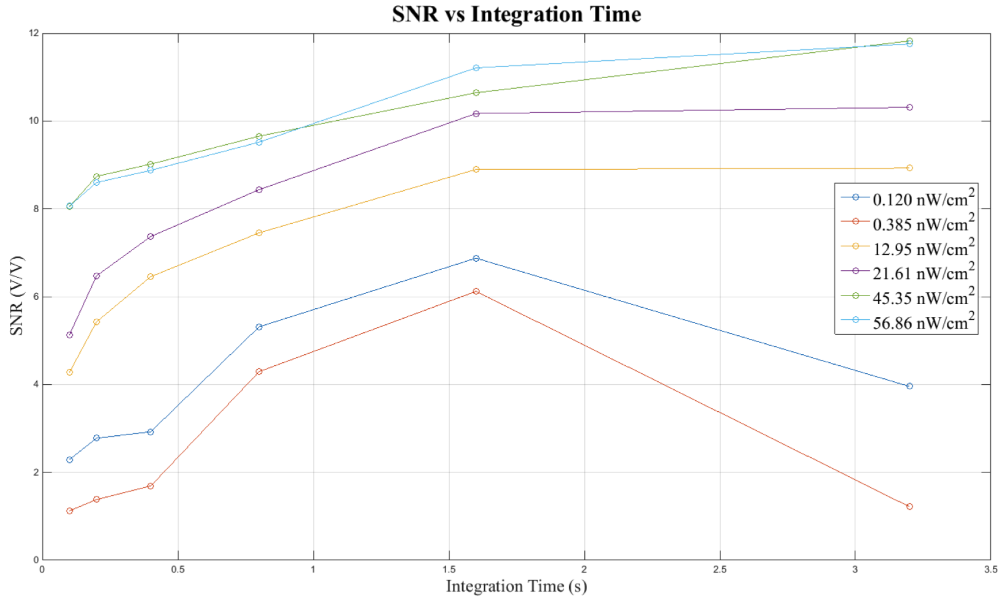


Figure 4.14: Imager SNR vs T_{int} in low-light conditions.

Table 4.1 summarizes the input-referred noise of Q1 at its integration node across different integration times. We estimated the electronic noise without the dark current of a-Se at 400 ms of integration as 89 e^- while the measured noise peaks at 90 e^-. Since the device's leakage current and conversion gain is nonlinear as integration time increases, the projected noise becomes less accurate. Notably, for the noise reported in the table, we used the maximum value of the histogram, instead of the mean value. As Figure 4.15 shows, since the dominant noise sources are leakage currents from the protection diode and reset device operating in weak inversion, their noise distribution follows the Poisson distribution. Therefore, the maximum peak value, rather than the mean, should be used for calculation.

Table 4.1: Calculated vs measured noise across integration period.

Integration Period (ms)	Calculated Noise (e^- rms)	Measured Noise(e^- rms)
200	52.76	70.8
400	91.69	89
800	175.8	144
3300	693.45	420
6400	1385.93	800

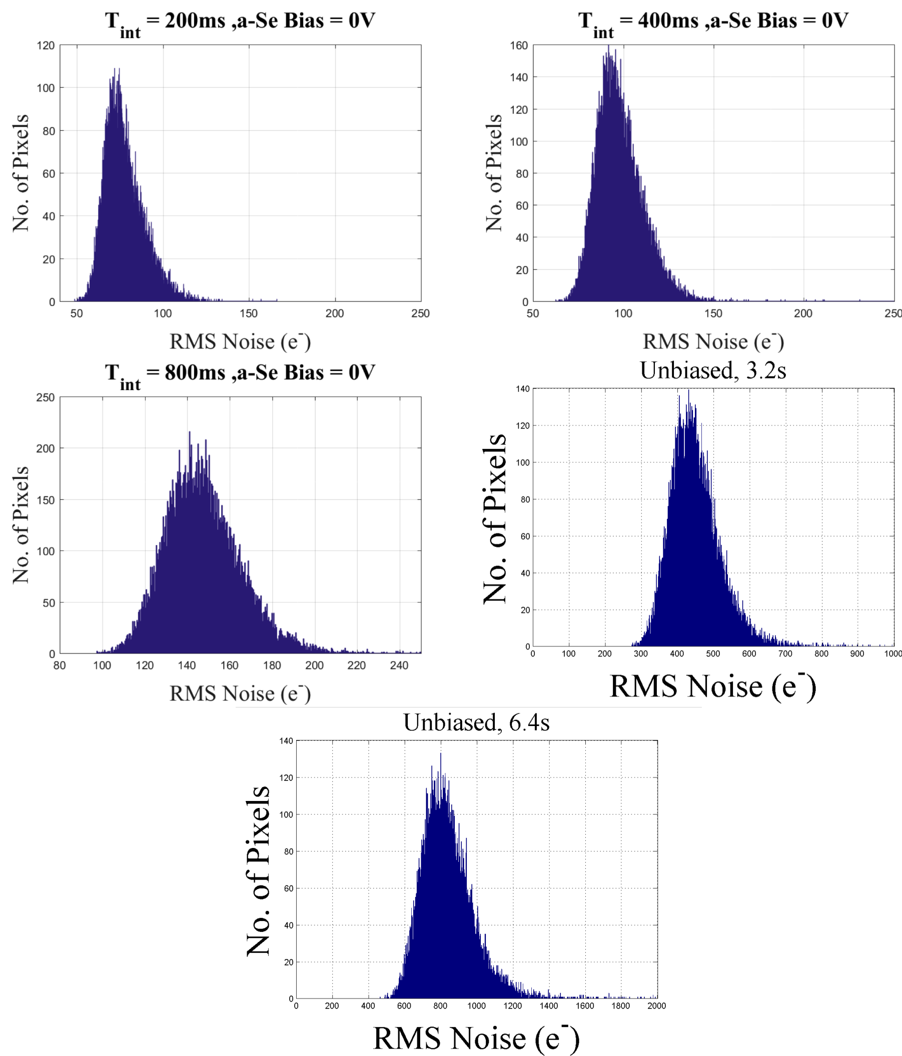


Figure 4.15: Array noise measurements across integration time.

4.2.2.4 Imaging Results

I obtained results for the optical-imaging setup, as the previous section shows, at controlled luminance levels. We inserted a line-pair test target into the setup and focused on Q1 with a convex-convex lens, as Figure 4.16 shows. With the addition of the focusing lens, the imager's illuminance will increase by the square of the magnification factor M. This is because the circular lens will focus the same number of photons landing on a larger area πr^2 down to a smaller area $\pi(\frac{r}{M})^2$, effectively increasing the luminous flux and, therefore, increasing the illuminance.

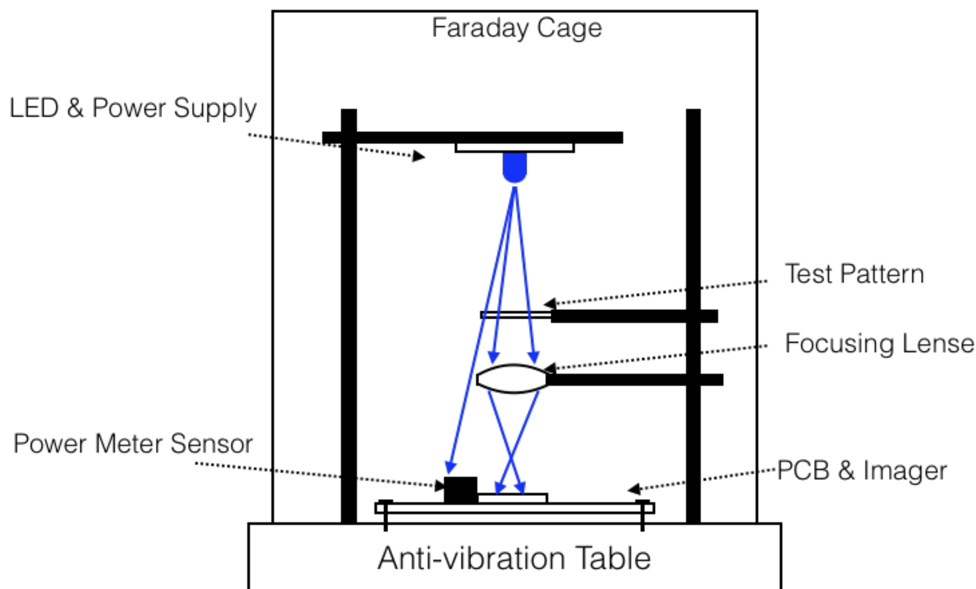
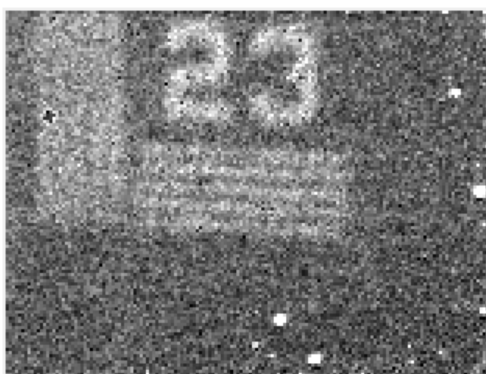


Figure 4.16: Optical imaging setup.

Based on the lens placement, it had a close-to-unity magnification for the images shown below. The 23 line pairs per mm target used included 5 bright lines and 4 dark lines with a total edge-to-edge distance of 195.6 µm. These 9 lines were projected over 27 pixels in the image, and, with a pixel pitch of 7.76 µm, these lines covered 209.52 µm on the imager. This means the target was magnified by 1.07x, which would increase the illuminance by 14%.

The imager's illuminance can be extracted by counting the delta between bright and dark parts of the image. With a 700 DN difference between bright and dark in 4.17b, the radiant power calculated to 9.33 nW/cm^2, taking into account the magnification

effect and later confirmed with a power meter that measured the radiant power as 10 nW/cm^2. This radiant power, with a given wavelength of 466 nm, translates to 0.1 lux, which is within the moonlight- illuminance level. Figure 4.17 shows the imager's output at 0.4 s of integration and 3.2 s of integration, showing that this work does visually improve image quality with longer integration. Figure 4.18 shows that the same image taken at 0.82 lux which demonstrates the target's details, approaching twilight-illuminance level. The images shown are single frames of raw captured images without correction. With an extracted SNR of 32 dB, it shows that this imager can produce excellent images under low illuminance, based on the ISO 12232 standard [11].



(a) 0.4 s of integration time.

(b) 3.2 s of integration time.

Figure 4.17: Imaging of line pair target at 0.1 lux.

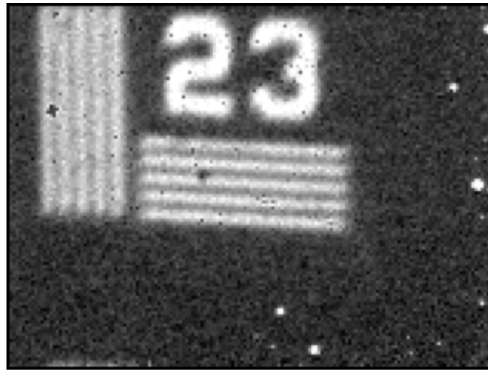


Figure 4.18: Image target taken at 0.82 lux with 0.4 s of integration time.

Note that the bright spots in the images are caused by imperfection in the a-Se deposition process, as well as a-Se crystallization due to frequent of power and temperature cycling.

Chapter 5

Conclusion

Our work demonstrates the potential for combining CMOS technology with a-Se to achieve moonlight-level imaging. The simulation model built prior to the imager's design underestimated a few aspects of the imaging condition, including the quantum efficiency of a-Se and the optical transmittance of gold. With these parameters updated, the model matched the measured results to within the same order of magnitude. The model can be further improved if the values extrapolated from other works, including the integration capacitance and quantum efficiency of selenium at low biasing voltage, can be measured in house. A better SNR can be achieved with longer integration periods because of the low dark current of a-Se and reduced leakage current of the CMOS-reset devices. However, since this CMOS process is not optimized for leakage performance, the leakage-current shot noise is the dominant noise source in this work. Table 5.1 compares our imager with a few other imagers built for low-light imaging applications.

This work suffers from higher electronic noise caused by the standard CMOS process because all other devices shown in the table were fabricated in a CMOS image-sensor (CIS) process. Some of the performance improvements enabled by the CIS technology include lower leakage-current MOSFET devices, achieved through optimizing silicon doping and device implants, as well as high-k-gate-oxide material, which are used to reduce flicker noise [53] [54] [55]. On top of the specialized CIS process to further reduce readout noise, all required additional process modifications, such as an in-pixel amplifier to boost the incoming signal and increasing conversion gain by reducing parasitic capacitance at the integration node through process modification [54], or to have replaced the reset MOSFET with an implant to further suppress thermal and leakage current shot noise.

Table 5.1: Imager performance summary and comparison with previous work.

	Q1 in this work	[52]	[53]	[54]	[55]
Process	180-nm MS	180-nm CIS	180-nm CIS	110 nm CIS	180-nm CIS
CMOS process modifications	No	No	Yes	Yes	Yes
Cooled	No	No	No	Yes	Not reported
Sensor	a-Se (3V/µm)	pinned PD	pinned PD	pinned PD	pinned PD
APS type	3-T	4-T	4-T	4-T	4-T
Active array size	160Hx120V	640Hx480V	180Hx480V	25Hx512V	128Hx198 V
Pixel size (μm^2)	7.8x7.8	6.5x6.5	5.5x5.5	11.2x5.6	10x10
Fill factor (%)	100	40	49	Not reported	33
Conversion gain ($\mu V/e^-$)	4.82	160	240	220	45
Full-well capacity (ke^-)	57.6	6.4	76	1.5	Not reported
Max. exposure time (ms)	3200	12.5	68.9	149	333
Read noise (hist. peak) (e^-_{rms})	91 @ 0.4 s	0.48	0.74	0.27	Not reported

Another of the current system's shortcomings is its inability to cool the imager. [54] was able to achieve the 0.27 e^- rms read noise partially because the imager was cooled to - 10 ^{o}. If our imager setup was cooled just above the temperature that causes a-Se to delaminate, both the shot noise generated from the leakage current and the kTC noise would decrease, although the effect would be insignificant as a-Se cannot be cooled to below 278 K.

Notably, all other works reported in the table have employed the 4-T pixel design, with either in-pixel or column-level amplification to minimize noise contribution of readout electronics down the signal path. A 4-T design enables CDS, which can significantly reduce kTC noise and leakage-current shot noise from the reset device. With an in-pixel or column amplifier, the readout path's noise contribution will be significantly reduced as the gain, when input is referred to the pixels' integration node suppresses the noise's magnitude. The downside of using the 4-T design is the limited fill factor. Given that our imager's fill factor is 2 times larger than all other works reported, the hybrid structure could collect twice as much incoming signal under the same illumination condition.

The lower conversion gain reported in this work is mainly caused by the low quantum efficiency of a-Se at low biasing voltage. To realize the full potential of using a-Se with CMOS technology, such as taking advantage of the high conversion gain provided by using parasitic capacitance as the integration capacitor, our photosensor's quantum efficiency must be improved. If the voltage applied to the a-Se can be increased up to 8 V/µm, the imager will see a 5x increase in conversion gain, while the dark current can be kept lower than a typical pn photodiode. Moreover, the main trade-off for achieving

the high conversion gain in [52] [54] [55] is the small full-well capacity, meaning the imagers will saturate at low illuminance. [53] was able to achieve both high conversion gain and high full-well capacity by utilizing a process modification named lateral overflow integration capacitor.

Lastly, since the ultimate purpose of an imager is to capture clean images, the resulting SNR at a given illuminance is the most important figure of merit. The maximum exposure time of our imager is significantly longer than any other works and will, thus, allow us to collect more signal, therefore minimizing the impact of higher read noise and achieving comparable SNR at low illuminance. Other imagers will not be able to integrate for an extended time, both because of their small full-well capacity, which will quickly saturate because of the MOSFET leakage current, and the higher photosensor dark current. At the same time, the longer integration period means that our imager's current application is limited to static imaging. However, since this work aims to show that the CMOS and a-Se hybrid structure is capable of low-light imaging, this is acceptable.

5.1 Future Work

Since this imager can only achieve acceptable SNR with a long integration period, limiting its potential applications, the read noise must be lowered. A specialized CMOS process for image sensors could be used in future work to further reduce the dominating electronic noise, which could enable the imager to compete with other sub-electron noise imagers. Other advanced techniques that have been used to bring readout noise to sub-electron rms value can be implemented in the design, such as high-column amplification and correlated multiple sampling enabled by a 4-T pixel design [46].

One major benefit of a-Se that this work did not take advantage of is the ability to operate the photosensor in avalanche mode, where the conversion gain of the photosensor can reach up to 10^4. The HARP camera already uses such technology [16]. However, this mode of operation requires a high biasing voltage, usually above 80V/µm. With the current PCB setup and the close proximity of the high-voltage biasing line to the CMOS die, as well as a lack of proper encapsulation, high-voltage biasing cannot be applied.

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APPENDICES

Appendix A

LL1 Pin Out Summary

Figure A.1: LL1 CMOS chip bonding diagram.

Table A.1: LL1 IC pin out summary.

Pin Number	Pin Name	Analog Digital	Input Output	Range (V)	Description
1	q3_en_cs	D	I	0-3.3	Q3 Column Select Enable
2	vrst_pMOS	A	I	1.4	Reset voltage for Q3
3	q3_direct_out	D	O	1.4-3.3	Q3 pixel direct output
4	vss	A		0-3.3	Ground
5	q3_vout	A	O	1.4-3.3	Q3 buffered output
6	avdd	A		3.3	Analog power
7	dvdd	D		3.3	Digital power
8	botBufBias	D	I	1.2	Q3 Q4 on chip buffer biasing
9	grst	D	I	0-3.3	Global reset
10	dvdd	D		3.3	Digital power
11	switchA	D	I	0-3.3	Master tri-switch A
12	switchB	D	I	0-3.3	Master tri-switch B
13	switchC	D	I	0-3.3	Master tri-switch C
14	vss	A		0	Ground
15	rst_clk	D	I	0-3.3	Reset scan chain clock
16	dvdd	D		3.3	Digital power
17	vdio	A	I	2.3	Diode voltage control
18	botCMBias	A	I	1.2	Q3 Q4 current mirror biasing
19	botMuxOut	D	O	0-3.3	Q3 Q4 selective digital output
20	vss	A		0	Ground
21	botmuxA	D	I	0-3.3	Bottom digital signal mux select control
22	botmuxB	D	I	0-3.3	Bottom digital signal mux select control
23	botmuxC	D	I	0-3.3	Bottom digital signal mux select control
24	dvdd	D		3.3	Digital power
25	avdd	A		3.3	Analog power
26	vss	A		0	Ground
27	q4_vout	A	O	0.7-3.3	Q4 buffered output
28	q4_direct_out	A	O	0.7-3.3	Q4 pixel direct output

Continued on next page

Table A.1 – continued from previous page

Pin Number	PinName	Analog Digital	Input Output	Range (V)	Description
29	q4_en_cs	D	I	0-3.3	Q4 column select enable
30	q4_capCtrl	D	I	0-3.3	Q4 cap control
31	q4_en_rs	D	I	0-3.3	Q4 row select enable
32	dvdd	D		3.3	Digital power
33	q4_en_rst	D	I	0-3.3	Q4 reset scan chain enable
34	vddring	A		3.3	IO pads power
35	N/C				
36	N/C				
37	N/C				
38	N/C				
39	N/C				
40	N/C				
41	N/C				
42	N/C				
43	N/C				
44	N/C				
45	N/C				
46	N/C				
47	N/C				
48	N/C				
49	N/C				
50	N/C				
51	N/C				
52	N/C				
53	N/C				
54	N/C				
55	N/C				
56	N/C				
57	dvdd	D		3.3	Digital power
58	q2_en_rst	D	I	0-3.3	Q2 reset scan chain enable
59	q2_dummy_ctrl	D	I	0-3.3	Q2 dummy device enable
60	q2_en_rs	D	I	0-3.3	Q2 row select enable

Continued on next page

Table A.1 – continued from previous page

Pin Number	PinName	Analog Digital	Input Output	Range (V)	Description
61	q2_en_cs	D	I	0-3.3	Q2 column select enable
62	avdd	A		3.3	Analog power
63	q2_direct_out	A	O	0.7-3.3	Q2 pixel direct output
64	vss	A		0	Ground
65	irst	D	I	0-3.3	Reset scan chain input
66	q2_vout	A	O	0.7-3.3	Q2 buffer output
67	avdd	A		3.3	Analog power
68	ics	D	I	0-3.3	Column select scan chain input
69	vss	A		0	Ground
70	vrst	A	I	0.7	Reset voltage for Q1, Q2 and Q4
71	q2_rst_out	D	O	0-3.3	Q2 reset scan chain output
72	q2_cs_out	D	O	0-3.3	Q2 column select scan chain output
73	q2_rs_out	D	O	0-3.3	Q2 row select scan chain output
74	vssring	A		0	Ground for pad ring
75	rs_clk	D	I	0-3.3	Row select scan chain clock
76	vddring	A		3.3	Power for pad ring
77	cs_clk	D	I	0-3.3	Column select scan chain clock
78	topMuxC	D	I	0-3.3	Top digital mux control
79	topMuxB	D	I	0-3.3	Top digital mux control
80	topMuxA	D	I	0-3.3	Top digital mux control
81	vss	A		0	Ground
82	topMuxOut	D	O	0-3.3	Top digital mux output
83	irs	D	I	0-3.3	Row select scan chain input
84	top_buf_bias	A	I	1.2	Q1 Q2 buffer biasing
85	dvdd	D		3.3	Digital power
86	q1_vout	A	O	0.7-3.3	Q1 buffered output
87	vss	A		0	Ground
88	q1_direct_out	A	O	0.7-3.3	Q1 pixel direct output
89	topCMbias	A	I	1.2	Q1 Q2 current mirror biasing
90	avdd	A		3.3	Analog power

Continued on next page

Table A.1 – continued from previous page

Pin Number	PinName	Analog Digital	Input Output	Range (V)	Description
91	q1_en_cs	D	I	0-3.3	Q1 column select scan chain enable
92	q1_en_rs	D	I	0-3.3	Q1 row select scan chain enable
93	q1_en_rst	D	I	0-3.3	Q1 reset scan chain enable
94	dvdd	D		3.3	Digital power
95	N/C				
96	N/C				
97	N/C				
98	N/C				
99	N/C				
100	N/C				
101	N/C				
102	N/C				
103	N/C				
104	N/C				
105	N/C				
106	N/C				
107	N/C				
108	N/C				
109	N/C				
110	N/C				
111	N/C				
112	N/C				
113	N/C				
114	N/C				
115	N/C				
116	N/C				
117	vssring	A		0	Ground for pad ring
118	q3_en_rst	D	I	0-3.3	Q3 reset scab chain enable
119	q3_dummyCtrl	D	I	0-3.3	Q3 dummy device control
120	q3_en_rs	D	I	0-3.3	Q3 row select scan chain enable

Appendix B

LL1 PCB Schematics

Figure B.1: PCB schematic of CMOS chip with decoupling capacitors.

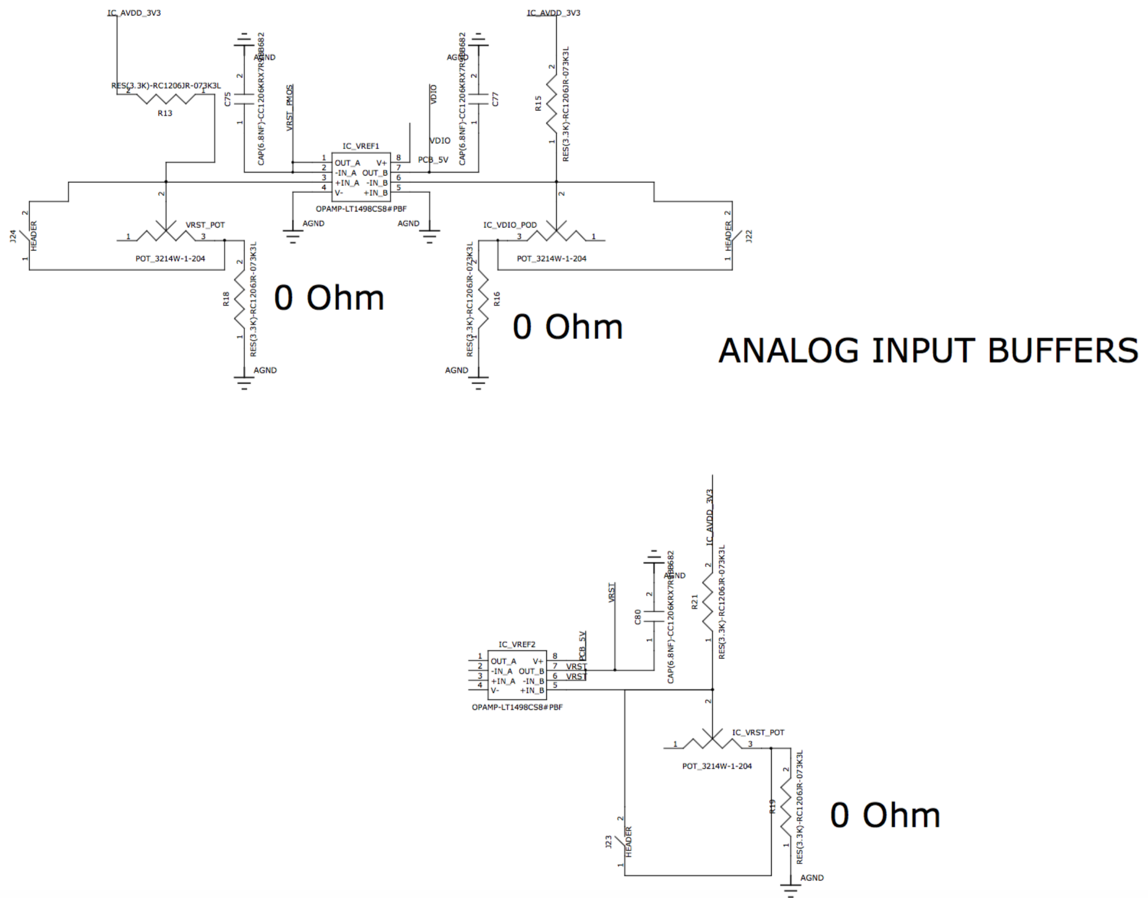


Figure B.2: PCB schematic of analog biasing and signal buffers.

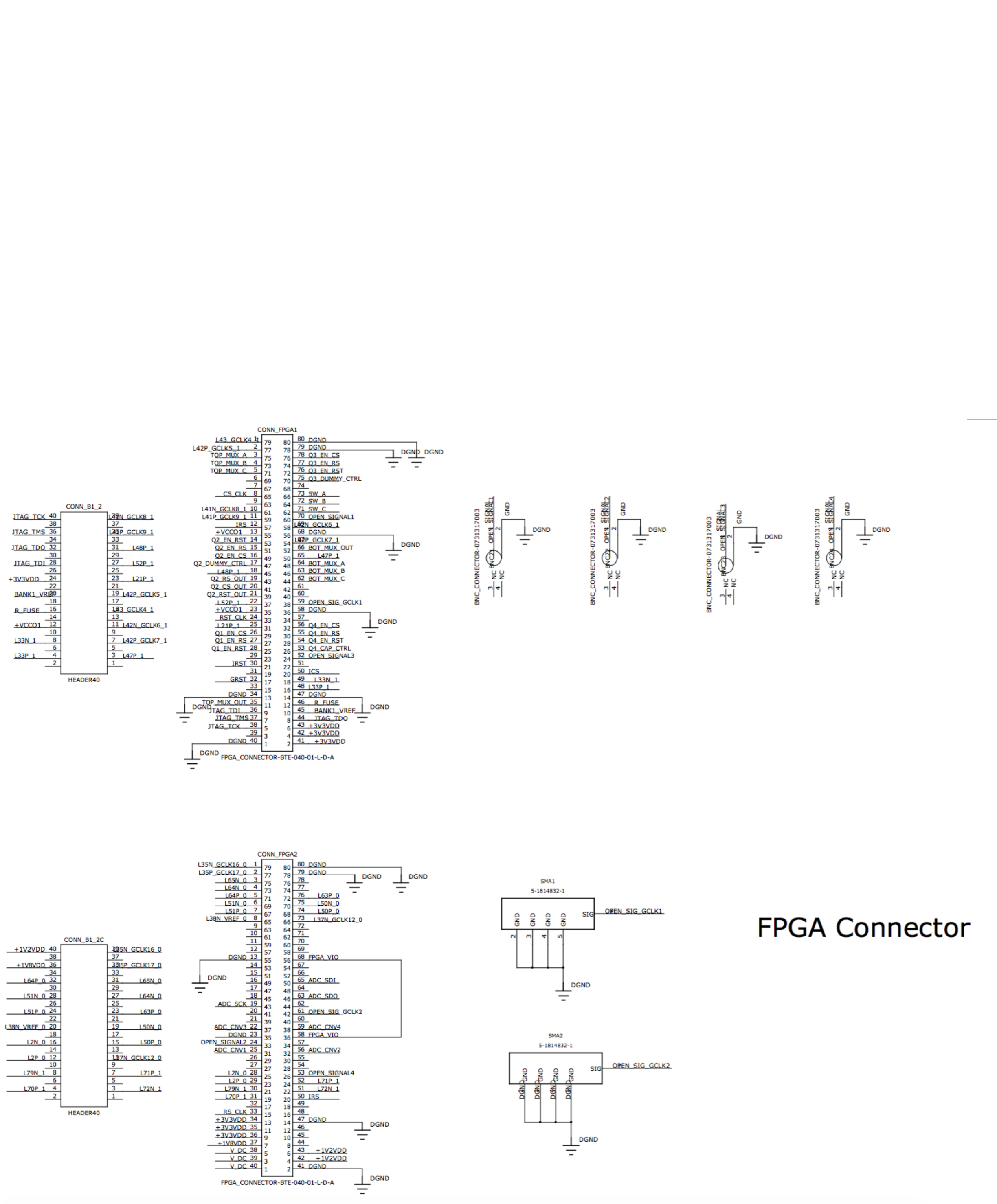


Figure B.3: PCB schematic of Opal Kelly FPGA connectors.

Current Biasing

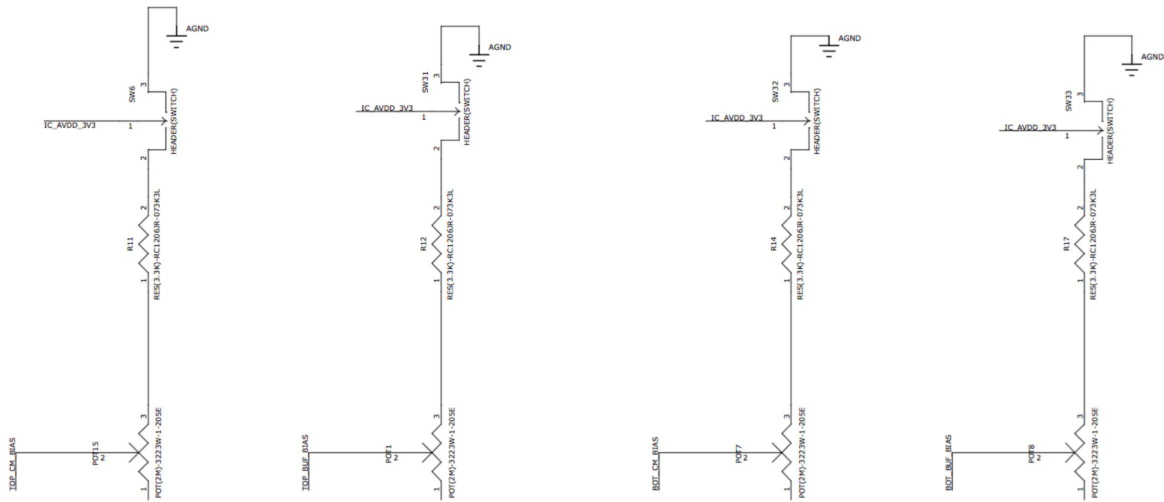


Figure B.4: PCB schematic of CMOS current biasing circuits.

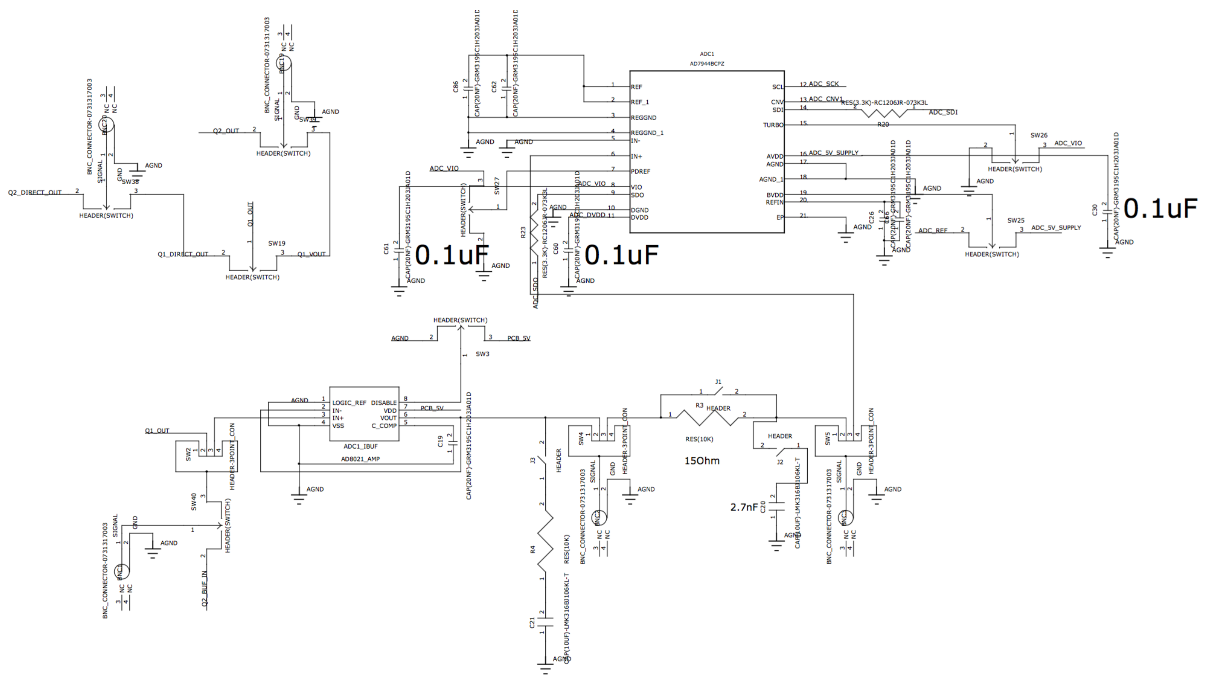


Figure B.5: PCB schematic of an ADC with pre-amp buffer.

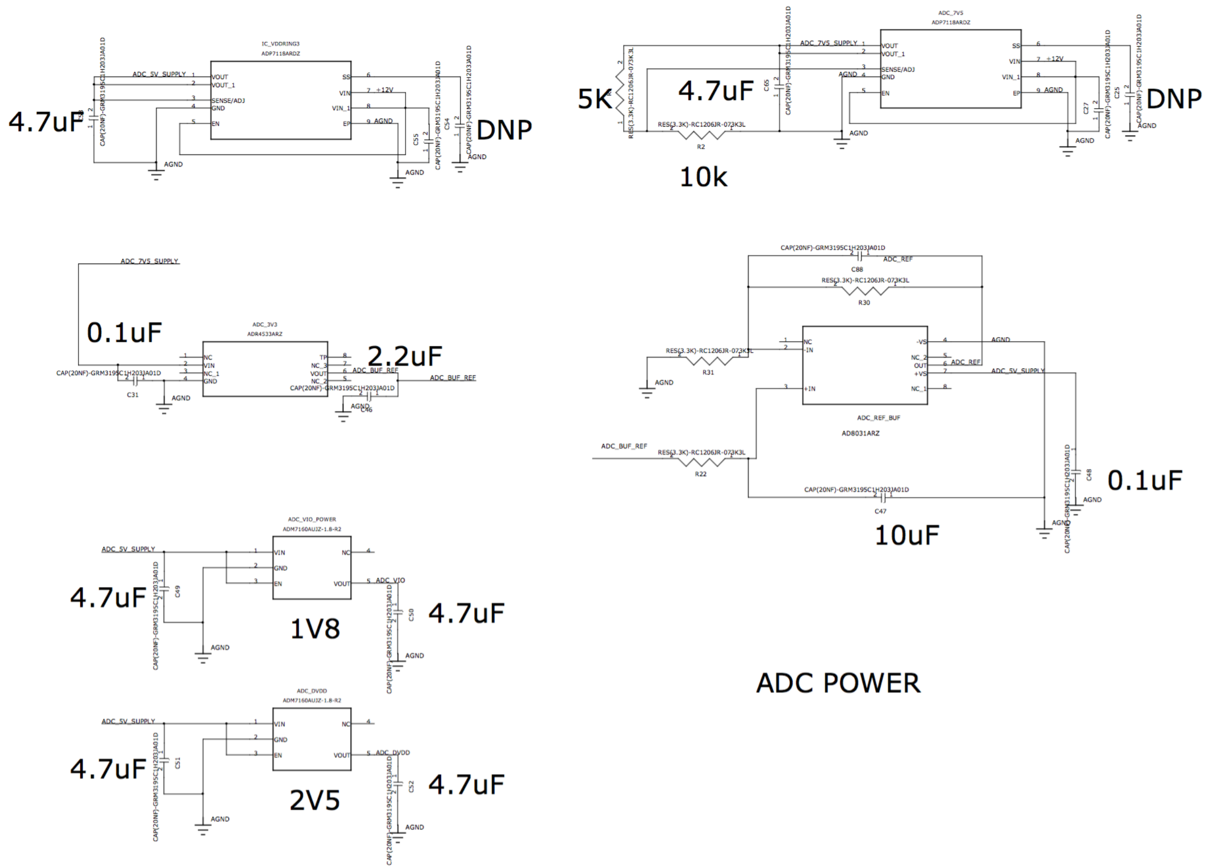


Figure B.6: PCB schematic of ADC power generation circuits.

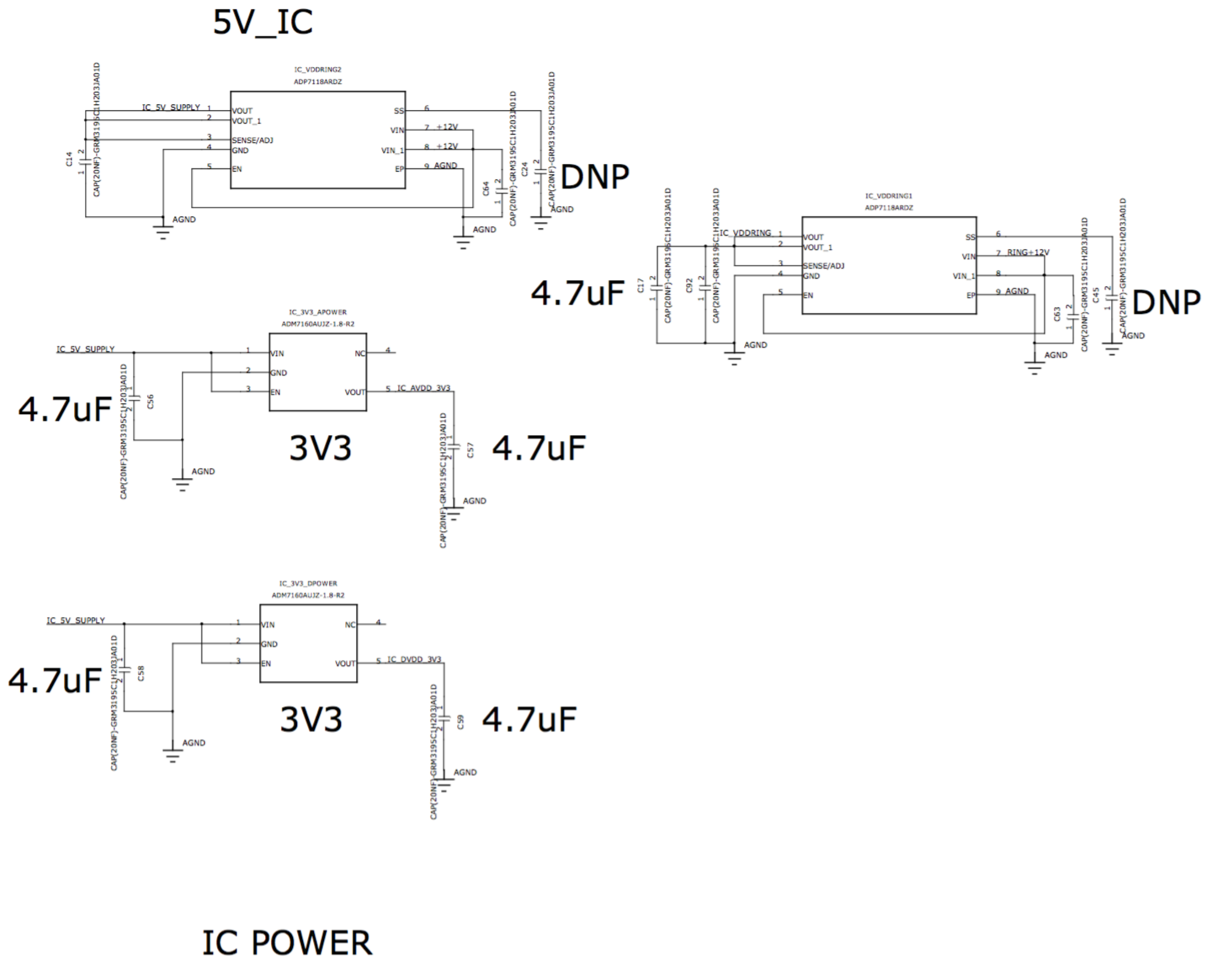
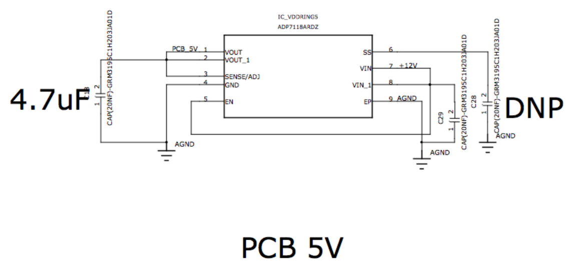


Figure B.7: PCB schematic of CMOS power generation circuits.



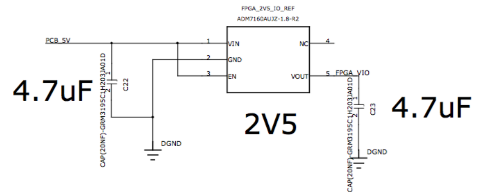


Figure B.8: PCB schematic of PCB main power generation circuits.