A 4-Channel 12-Bit High-Voltage Radiation-Hardened Digital-to-Analog Converter for Low Orbit Satellite Applications

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***Abstract*—This paper presents a circuit design and implementation of a 4-channel 12-bit digital-to-analogue converter (DAC) with high-voltage operation and radiation-tolerant attribute using a specific CSMC H8312 0.5-μm BiCMOS technology to achieve the functionality across a wide-temperature range from -55°C to 125°C. In this work, an R-2R resistor network is adopted in the DAC to provide necessary resistors matching which improves the DAC precision and linearity with both the global common centroid and local common centroid layout. Therefore, no additional, complicated digital calibration or laser-trimming are needed in this design. The experimental and measurement results show that the maximum frequency of the single-chip 4-channel 12-bit R-2R ladder high-voltage radiation-tolerant DAC is 100 kHz, and the designed DAC achieves the maximum value of differential non-linearity (DNL) of 0.18 LSB, and the maximum value of integral non-linearity (INL) of -0.53 LSB at 125°C, which is close to the optimal DAC performance. The performance of the proposed DAC keeps constant over the whole temperature range from -55°C to 125°C. Furthermore, an enhanced radiation-hardened design has been demonstrated by utilising a radiation chamber experimental setup. The fabricated radiation-tolerant DAC chipset occupies a die area of 7mm $\times$ 7mm in total including pads (core active area of 4mm $\times$ 5mm excluding pads) and consumes less than 525 mW, output voltage ranges from -10 V to $+10$ V.**

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***Index Terms*—Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC), Mismatch Calibration, R-2R ladder, Single Event Effects (SEE).**

I. Introduction

OVER the past decades, various technologies and methodologies have been proposed to improve the system on chip (SoC) resilience to the radiation effects in space and nuclear applications, hostile domain electronics, medical equipments and high-energy physics experiments, etc. This work is oriented to avionics applications, where radiation tolerance mainly refers to circuits and system's ability to resist any number of undesirable radiation-induced phenomena in the case of extreme environments, including wide temperature, intense radiation, high pressure or strenuous vibration, etc. In order to avoid the traditional bulky and costly protective "warm boxes" or "electronics vaults", newly-designed electronics systems must robustly operate over a wide temperature range in extreme environments. The single event effect (SEE) caused by atmospheric radiation has been recognised in recent years as a design issue for avionics systems. There are various types of single event effects, which are the result of a single particle depositing sufficient energy, causing a disturbance in an electronic device; on the other hand, total-dose effects arisen from the leakage currents, which are related to transistor edge effects and field-oxide trapped charges is another important issue for radiation-tolerant circuit design [1].

Due to the increased need of radiation-tolerant analog and mixed-signal circuits in recent years, the development of precision analog circuits becomes more important. For instance, as an interface between analog and digital worlds, Digital-to-Analog Converter (DAC), which converts the signal from "0" and "1" is expressed in digital expressions to a continuous amplitude value of the analog, is an indispensable module in the whole electronic system. At present, DACs and Analog-to-Digital Converters (ADCs) are very prevalent in modern electronic devices; however, their performance is often a bottleneck for practical applications [2]–[6]. The goal for engineers is to design and manufacture high performance radiation-tolerant DAC and ADC by using commercial processes that are inexpensive and widely available in the industry.

In this work, we report a design and implementation of a monolithic 4-channel 12-bit high-voltage radiation-tolerant DAC chip, which can satisfy the circuit specifications for low orbit satellite application to tolerate single event effects and

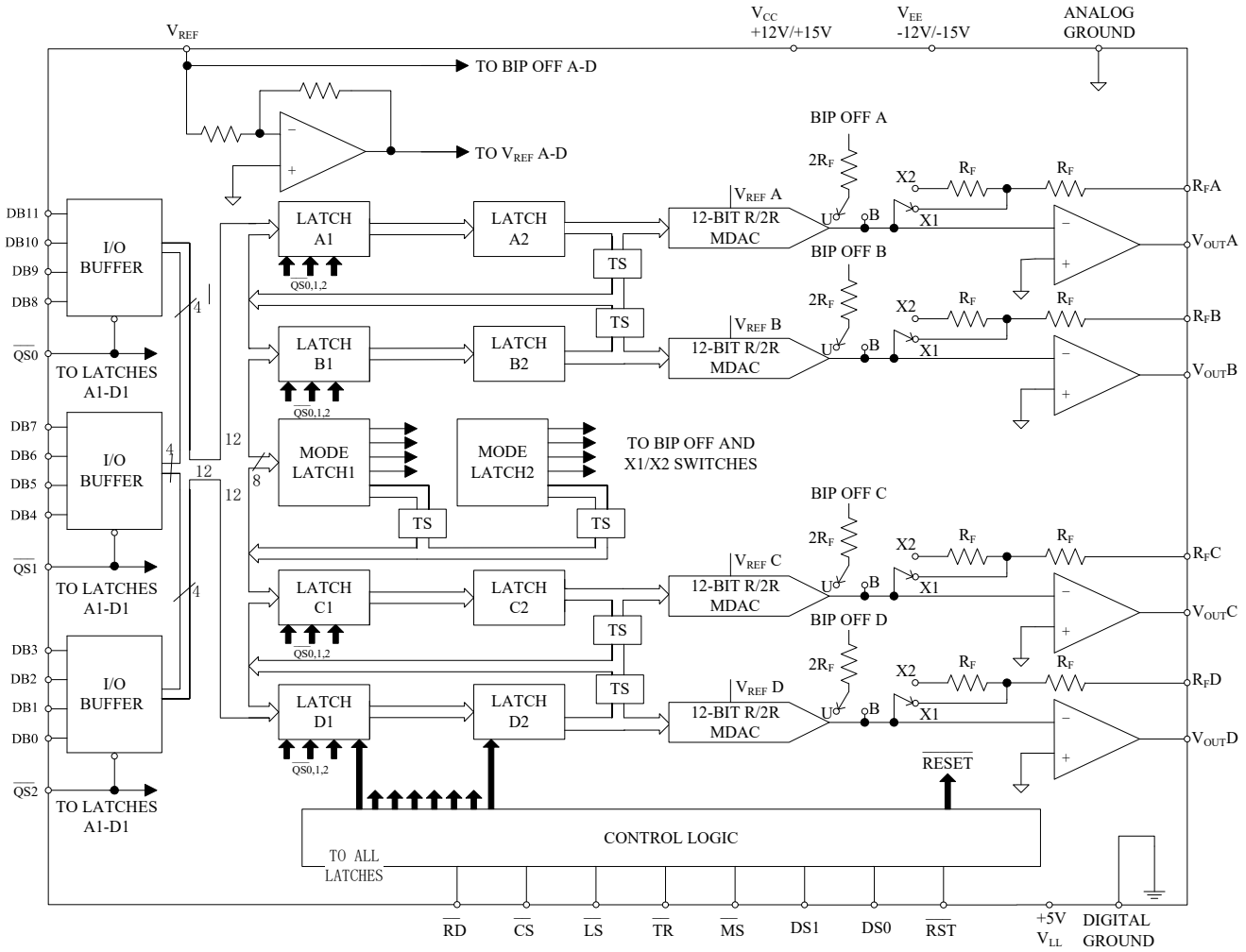

Fig. 1. The overall structure of the single-chip 4-channel 12-bit high-voltage radiation-hardened DAC [7].

to resist total ionising dose of 10 krad (Si). It is fabricated by using a custom designed CSMC H8312 0.5-μm BiCMOS technology, which integrates high-voltage (HV) bipolar, HV and low-voltage (LV) CMOS devices. It is worth mentioning that V_{GS} and V_{DS} of MOS can reach as high as 30V, also, V_{CE} of bipolar can reach 30V.

The contributions of this work can be summarized as follows:

(i) Conventional DAC with R-2R resistor network usually adopts a complex thin-film resistor process and laser-trimming to achieve necessary matching of resistors. Mechanical stress during packaging and long-term drift of laser-trimming components often pose serious problems to such R-2R converters. In this work, a novel and reasonable resistive array layout and wiring method are well-designed and characterised. In detail, both the global common centroid and local common centroid layout have been fully implemented. Therefore, no additional, complicated digital calibration or trimming are needed in this work;

(ii) Guard rings are the key techniques in the radiation-hardened design. In this work, both valid and invalid guard ring designs have been demonstrated at the radiation chamber, which is of great inspiration for both industry and academia;

(iii) It is worth mentioning that the 4-channel 12-bit DAC with high-voltage operations and radiation-tolerant attribute proposed in this work is a milestone and exhibits a great impact on the aerospace industry of China.

The paper is organised as follows: A brief overview of DAC design is presented in Section II. Section III describes the circuit design and the main features of the proposed DAC. Section IV discusses the collected experimental results, while the key outcomes are finally summarised in Section V.

II. System Overview

The overall structure of the proposed single-chip 4-channel 12-bit R-2R high-voltage radiation-hardened DAC with read-back capability is shown in Fig. 1. In general, it provides four voltage-output DACs on one chip to offer the highest density. The output range of each DAC is fully and independently programmable. Readback capability allows to verify the contents of the internal data registers, which is obtained by setting the address of the DAC (DS0, DS1) and Quads (QS0, QS1, QS2) on the address pins and bringing the RD and CS pins low.

The analog portion consists of four DAC cells, four output amplifiers, a control amplifier and switches. The positive and negative power supply voltages of analog part reach as high as $\pm$15V. High-voltage, low-threshold transistors are applied whose safe operating voltage can reach as high as 30V. In

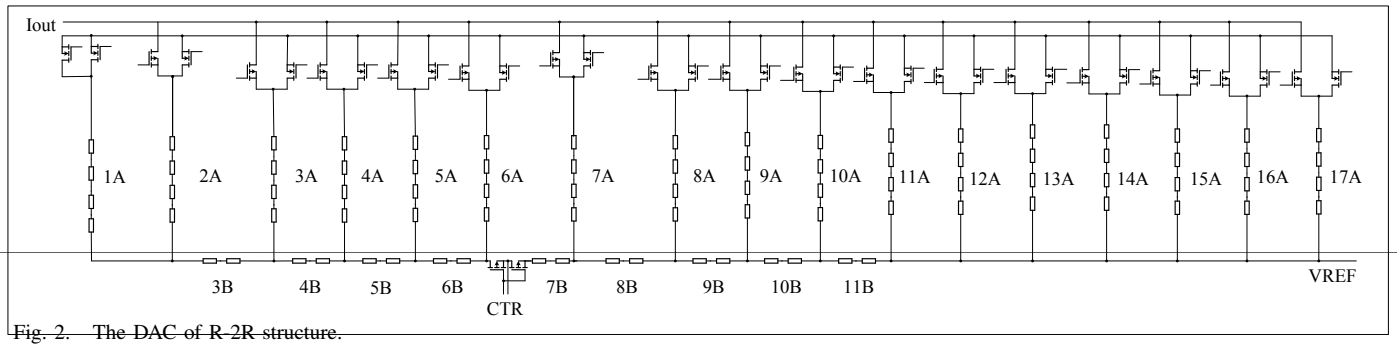

Fig. 2. The DAC of R-2R structure.

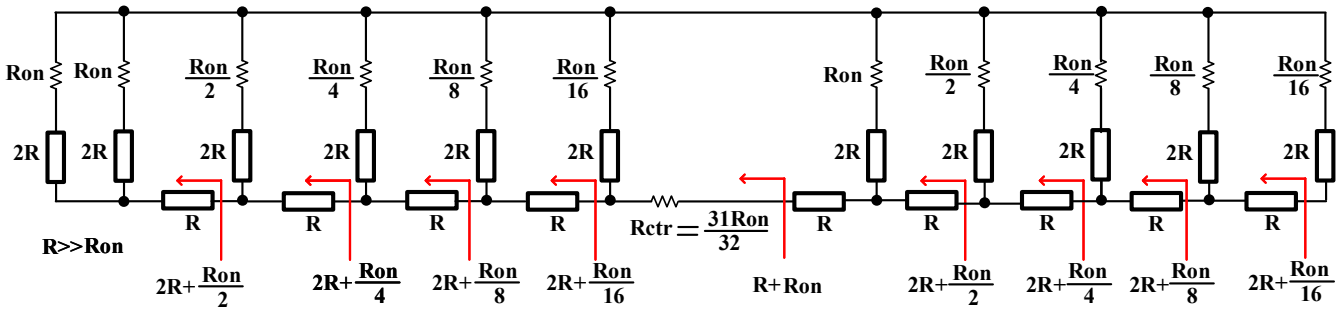

Fig. 3. The equivalent circuit of simplified R-2R structure.

other words, V_{GS}, V_{DS} of MOS and V_{CE} of bipolar can reach as high as 30V. High-precision poly resistor is chosen in this work, which can meet the requirements of high voltage operations.

Each 12-bit DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range with a gain of one or two times the reference voltage. All DACs can operate from a single external reference, and the output range of each DAC is fully and independently programmable. Each DAC offers flexibility, accuracy and good dynamic performance, in which a novel layout of R-2R resistive array can satisfy the demands of DAC linearity. It is worth mentioning that no calibration or laser-trimming are applied to the resistive array. The performance of each DAC is guaranteed to be monotonic and stable over the full operating temperature range from $-55°$C to 125°C.

The power supply voltage of digital portion is only 5V, DB0 $\sim$ DB11 are the inputs of DAC. An asynchronous RESET-TO-ZERO control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch, and the asynchronous reset signal can be asserted at any time.

III. Circuits Design

A. 12-Bit R-2R DAC design

As shown in Fig. 2, DAC is the core component of the 4-Channel 12-Bit radiation-hardened DAC. The DAC uses segmentation to reach higher resolutions, thermometer codes are applied to the MSB, as shown for the last seven resistors on the right from 11A to 17A in Fig. 2, which can overcome the undesired glitch impulse effectively [8], [9]. Split switch CTR in the centre splits the lower 6 bits and the higher 6 bits. In this work, the value of resistor of R-2R ladder is much larger than the on-resistance of the switch. Fig. 3 shows the equivalent simplified R-2R ladder.

In R-2R ladder, the linearity of the R-2R ladder is sensitive to the matching of the resistive networks [10]–[14]. Conventionally, the R-2R structure is fabricated from thin-film resistors which are laser-trimmed to achieve high linearity and guarantee monotonicity. In the traditional layout of resistive array, the resistors are always interconnected by multi-layer metal. Not only the routing is complicated, but also the gain error calibration becomes more complex. Furthermore, traditional layout of resistive array usually focuses on the matching accuracy between MSB resistors, but ignores the matching between LSB and MSB resistors and the matching between LSB resistors.

In this work, a novel layout technique considers not only the matching between MSB and LSB resistors, but also the matching between LSB resistors. Therefore, it can significantly improve the matching of resistive array, as well as the precision and linearity of DAC. The resistors of each channel are split into a different number of resistors with the same size, which is able to minimise the device mismatches and the parasitic resistance and capacitance. Likewise, the resistors in the R-2R are symmetrically aligned with only single metal interconnection wire so as to minimise the effects of the parasitic resistances of the metal interconnects. In Fig. 2, the resistors of one channel have been marked from No. 1 to 17, and then divide them into section A and section B according to the locations of the resistors. In the following, Fig. 4(a) shows the global distribution of the resistors, while Fig. 4(b-d) illustrate the detailed local distributions of X region, Z region and Y region. Both global and local common centroid can be ensured with this proposed layout.

In Fig. 4(a), the resistors of section B are only placed in

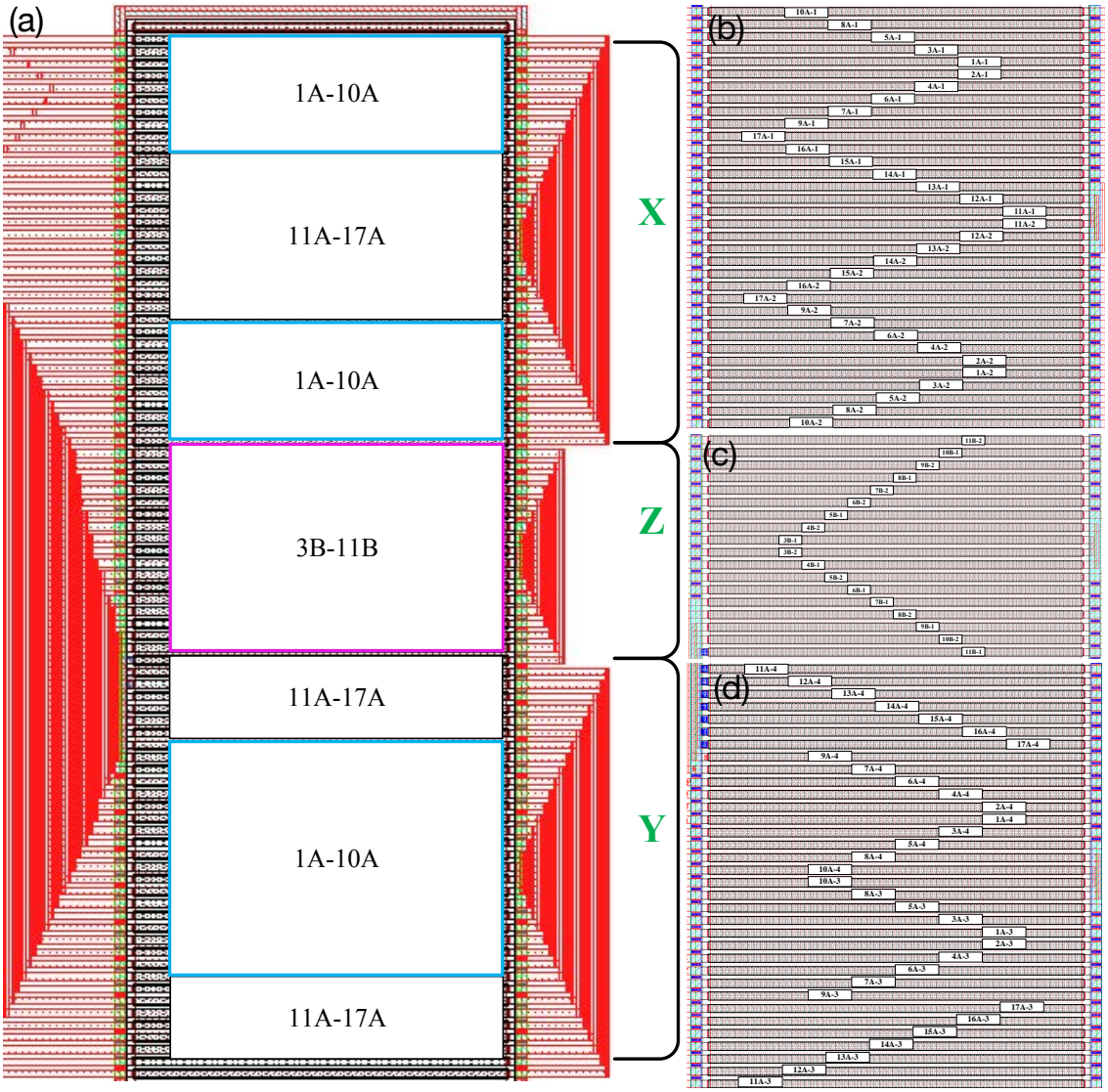

Fig. 4. (a) The overall distribution of resistive array. The distribution of resistors in (b) X region, (c) Z region, and (d) Y region.

the centre of the whole array, while the resistors of section A are divided into two parts: 11A to 17A (higher bits) and 1A to 10A (lower bits). Higher bits and lower bits are arranged in cross type to ensure centroid symmetry. Meanwhile, the resistors of section A are placed on both sides of section B. Then, obviously, the resistors of both section A and B have realised the common centroid distribution in this way. Next, the resistive array which is already arranged in a global common centroid is divided into three regions: X region, Y region and Z region. The resistors of section B belong to Z region (in the centre), and the resistors of section A belong to both X and Y regions. For example, the resistor 1A is separated into four equal parts: 1A-1, 1A-2, 1A-3 and 1A-4, where 1A-1 and 1A-2 are located in X region, while 1A-3 and 1A-4 in Y region. All the resistive array must realise local centroid distribution in X, Y and Z regions respectively.

The distribution of the resistors in X region is shown in Fig. 4(b) in details. Resistors 1A to 10A are divided into two groups and the two groups are placed symmetrically with each other. For example, the resistor 1A is divided into 1A-1 and 1A-2. In general, 1A and 2A are symmetrical, 3A and 4A are symmetrical, 5A and 6A are symmetrical until 7A, which is placed on the side of 6A rather than 5A, then 8A and 10A are placed on the side of 5A, 9A is placed after 6A and 7A. In the centre, 11A-1 to 17A-1 and 11A-2 to 17A-2 are symmetrically placed on both sides of the axle wire in X region in order.

The distribution of the resistors in Y region is shown in Fig. 4(d), which is similar with that of the resistors in X region in Fig. 4(b). Resistors from 1A to 10A are divided into two groups and the two groups are placed symmetrically with each other. For example, resistor 1A is divided into 1A-3 and 1A-4. In general, 1A and 2A are symmetrical, 3A and 4A are symmetrical, 5A and 6A are symmetrical until 7A, which is placed on the side of 6A rather than 5A, then 8A and 10A are placed on the side of 5A, 9A is placed after 6A and 7A. In the centre, 11A-1 to 17A-1 and 11A-2 to 17A-2 are symmetrically placed on both sides of the axle wire in the Y region in order. 1A-3 to 10A-3 and 1A-4 to 10A-4 are placed on both sides of the axle wire in Y region.

The resistors in Z region contain all resistors of group B.

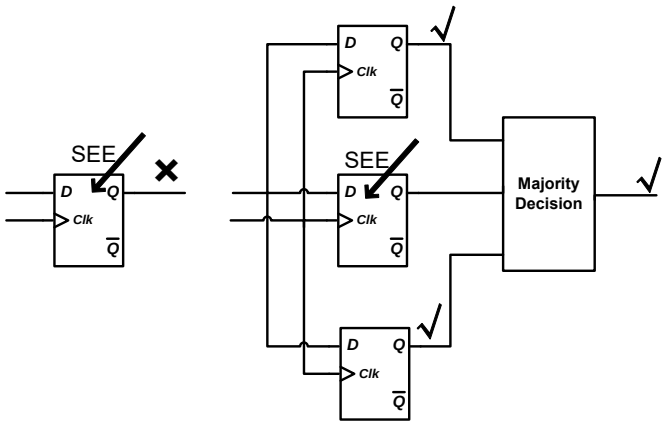

Fig. 5. D-latch with triple modular redundancy design.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
0	1	1	0
0	1	1	0
0	1	1	0
0	1	1	0

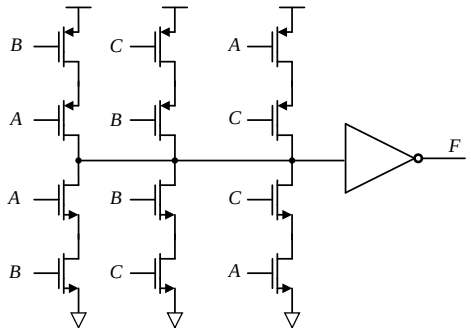

Fig. 6. Truth table and majority voter

The distribution of the resistors is shown in Fig. 4(c): the resistors from 3B to 11B are divided into two groups and these two groups are placed symmetrically with respect to the centre.

Finally, such a layout distribution is not only globally common centroid in the whole array, as shown in Fig. 4(a), but also common centroid in every local region respectively (X, Z and Y regions in Fig. 4(b-d)). Therefore, the resistor mismatch caused by stress and temperature gradients can be decreased to the most extent. Moreover, in this design, the connection between the entire resistive arrays uses only the same metal (layer-M1) without holes and multi-layer interconnects. Therefore, the system mismatch caused by holes and multi-layer interconnects is dramatically decreased. Afterward, the wire length of every resistor from 1A to 17A is balanced. For example, the resistor 1A includes 1A-1, 1A-2, 1A-3 and 1A-4, Fig. 4(b) shows that the wire from 1A-1 to 1A-2 is long, but in Fig. 4(d), wire from 1A-3 to 1A-4 becomes shorter. The same case with resistor 17A, wire from 17A-1 to 17A-2 is short (Fig. 4(b)), but 17A-3 to 17A-4 becomes longer (Fig. 4(d)). In this way, the length of the interconnection of every resistor may be roughly equal.

B. Design issues about Reliability

In this design, analog block adopts a HV design, and the digital block contains both HV and LV designs. In the analog block, the length of the HV MOS is larger than 3μm, which can ensure single-event tolerance of the device [15]. However, the total ionizing dose tolerance is poor. Hence, in order to improve the tolerance of total ionising dose, guard rings are applied to substrate to a large extent.

In this design, PMOS is located in N-well, which has a N+ N-well guard ring inside. Meanwhile, N-well is surrounded by the P+ P-sub guard ring. Finally, outside of P+ P-sub guard ring is a HV N-well, whose function is to isolate two P-sub substrates between inner and outside. NMOS is surrounded by the P+ P-sub guard ring, outside of which is also the HV N-well. Therefore, the number of the P+ P-sub guard rings is about twice of N+ N-well guard rings.

Redundancy is also a common mitigation strategy to achieve system safety and reliability. In digital circuits, triple modular redundancy design is adopted to improve the ability to resist single event upset (SEU). However, it occupies more area and sacrifices speed. In some cases, the speed becomes 80% of conventional designs with about 3.2 times of increase in the resource and power. Therefore, the triple modular redundancy is used only in the crucial sub-blocks. For example, Fig. 5 shows a D-latch with triple modular redundancy [16], where three same Latches and majority voter constitute one D-latch. Fig. 6 shows the truth table and majority voter. Special radiation resilience experiments of D-latch have been carried out at the radiation chamber facilities of the China Institute of Atomic Energy in Beijing, China, which will be introduced in details in Section IV.

C. Operational Amplifiers Design

The output operational amplifier is one of the most challenging parts of DAC. In order to reduce power consumption, the operational amplifier used in this design is a simple two-stage amplifier. Compared with the bipolar operational amplifier, CMOS operational amplifier shows higher input

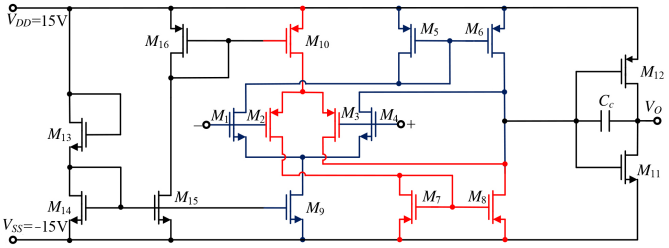

Fig. 7. The two-stage operational amplifier.

TABLE I
PERFORMANCE SUMMARY OF OPERATIONAL AMPLIFIER

Corner	Temperature (°C)	Gain (dB)	Gain bandwidth (MHz)	Supply voltage (V)
tt	−55	139.4	1.2	±15
tt	125	125.4	1.2	±15
ss	−55	139.3	1.2	±15
ss	125	130.0	1.1	±15
ff	−55	140.4	1.3	±15
ff	125	115.4	1.2	±15
fs	−55	139.2	1.1	±15
fs	125	116.1	1.2	±15
sf	−55	139.9	1.3	±15
sf	125	123.7	1.2	±15

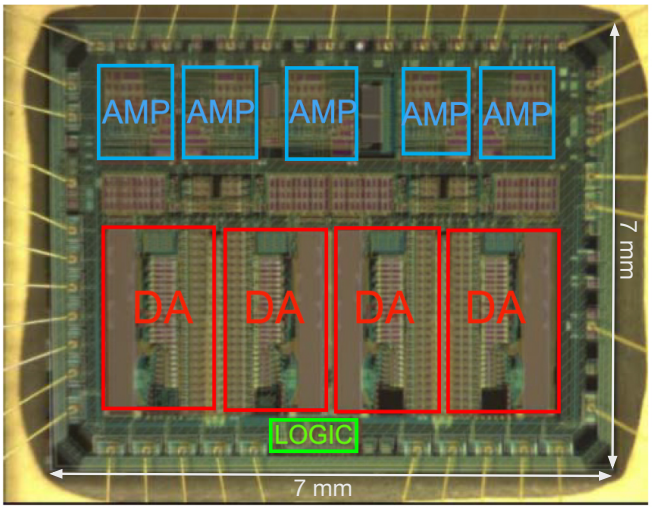

Fig. 8. The fabricated 4-channel 12-bit DAC microphotograph: whole chip including pads (with back-annotated layout).

impedance, smaller static power consumption [17]. In this design, the power supply is ±15V, operational amplifier with high open loop gain, sufficient phase margin, high common mode rejection ratio and large input/output swing is demanded.

For the radiation-hardened design, it is necessary to take measures to improve the noise immunity of the operational amplifier. It is found that most of the noise in the circuit blocks comes from the input level. Therefore, complementary input and differential structure are used to suppress the noise.

The two-stage operational amplifier used in this work is shown in Fig. 7, where M1-M4 constitute the input stage, M5-M8 act as active loads, M9 and M10 are tail current sources, M11 and M12 constitute output stage, and miller capacitor Cc provides for the frequency compensation [18]–[22]. The DC gain of the operational amplifier is greater than 110 dB, and the gain bandwidth (GBW) is greater than 1 MHZ, the high open loop gain of the operational amplifier in a negative feedback configuration is sufficient to compensate for the expected fluctuations.

Table I summarises the performance of the operational amplifier.

IV. Measurement Results

The 4-channel 12-bit DAC is manufactured on one monolithic IC chip by 0.5-μm BiCMOS technology (CSMC H8312). Fig. 8 shows the layout and chip photo. The whole area of prototype is 7mm × 7mm including pads (core area is 4mm × 5mm), and the maximum frequency of the DAC is 100 kHz. Measurement results show that: the power consumption of the 12-bit DAC is less than 525 mW. As a commercial product, 525 mW signifies the power consumption under the extreme case, which includes both analog and digital power. For the analog part, the positive and negative power supplies reach as high as ±15V, considering 10% of fluctuation , the maximum current of analog power supplies is 15 mA, leading to 495 mW of analog power consumption; On the other hand, the power supply of digital portion is only 5V, also considering 10% of fluctuation, the maximum current of digital power supply is 5.45 mA, therefore, the total power consumption is 525 mW. Differential non-linearity (DNL) at 27°C, 125°C and −55°C are [−0.23 LSB, 0.2 LSB], [−0.17 LSB, 0.18 LSB] and [−0.23 LSB, 0.14 LSB], respectively (Fig. 9(a-c)), and integral non-linearity (INL) at 27°C, 125°C and −55°C are [−0.55 LSB, 0.67 LSB], [−0.53 LSB, 0.26 LSB] and [−0.35 LSB, 0.7LSB], respectively (Fig. 9(d-f)). In conclusion, DNL and INL are well within 1 LSB in all cases, close to the performance of ideal DAC. The number of samples for DNL/INL measurements is 400, all of these samples achieve the similar performance, which demonstrate that the novel layout adopted in this work gives a good matching performance.

Fig. 12(a-c) reflect the resilience to total-dose effects. In these experiments, the chip was irradiated by a ^{60}Co source at room temperature at dose rate of 0.0064 rad (Si)/s. Fig. 12(a) shows that the chip loses validity at the total-dose of more than 20 krad (Si). Fig. 12(b-c) show that the currents of positive power supply and negative power supply fluctuate rapidly at total-dose up to 30 krad and 10 krad (Si) , respectively. Results of Fig. 12(a-c) demonstrate that the 12-Bit radiation-hardened DAC can satisfy demands for low orbit satellite applications.

A special set of single event latch-up (SEL) experiments are performed at the radiation chamber of China Institute of Atomic Energy in Beijing. 4 samples were irradiated by $^{35}Cl^{14+}$ (5 MeV/amu) and $^{74}Ge^{20+}$ (3 MeV/amu) sources within 3 cm beam width in vacuum environment. In total, every sample received 1×10^7 ions/cm^2 at 22°C, with a $^{35}Cl^{14+}$ flux of 1.1×10^4 ions/cm^2/s and a $^{74}Ge^{20+}$ flux of 1.2×10^4 ions/cm^2/s, respectively. The linear energy transfer (LET) for $^{35}Cl^{14+}$ ions is 13.3 MeV cm^2/mg, while the LET for $^{74}Ge^{20+}$ ions is 37.5 MeV cm^2/mg.

Laser pulse was applied to simulate radiation source (white point in Fig. 10) for failure analysis, in order to find the failure node. When exposed to laser pulse at the radiation chamber, as expected, D-latch with three guard rings and D-latch with five guard rings show different single-event latch-up effects. Here, three-channel oscilloscope including channel 2, 3 and 4 and multimeter are used to observe and analyze the latch-up phenomenon together. On the left of Fig. 11(a), the D-Latch layout includes three guard rings, located at the top, middle, and bottom, as identified with red boxes. At the right side of Fig. 11(a), 0.25 A current of the 5V digital power supply (corresponding to channel 2) demonstrates that the chip loses validity, because the thyristor between PMOS and NMOS (the region between the two red lines in Fig. 10) has been triggered by the laser pulse. In this case, two more guard rings have been added, as shown at left of Fig. 11(b). At right of Fig. 11(b), the current reduces to 0.02 mA by using 5 guard rings, which demonstrates that latch-up disappears and five guard rings function well under radiation of $^{35}Cl^{14+}$ and $^{74}Ge^{20+}$ sources. Therefore, for the sake of designing radiation-tolerant integrated circuits, it is vital to separate NMOS and PMOS completely.

However, guard rings sacrifice the chip area. In Fig. 11 (a), the area of the conventional layout of D-latch with three guard rings is 97 μm × 110 μm, while the area of the improved

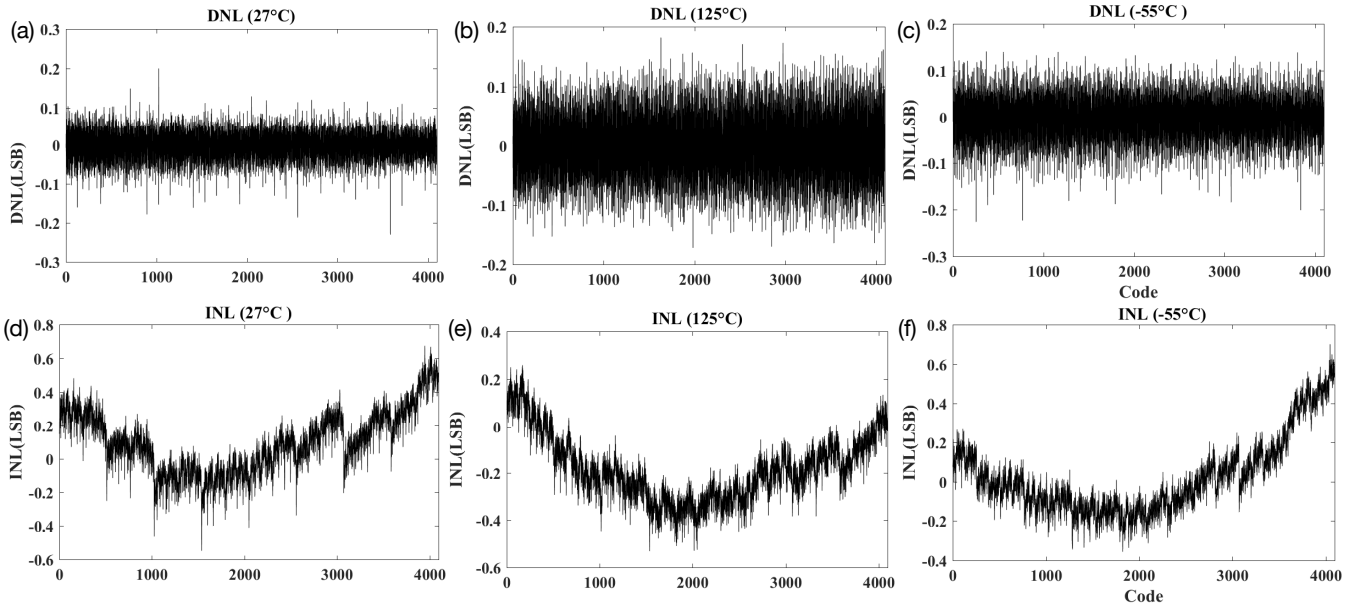

Fig. 9. Measured DNL of the fabricated 12-bit DAC at (a) 27°C, (b) 125°C and (c) −55°C. Measured INL of the fabricated 12-bit DAC at (d) 27°C, (e) 125°C and (f) −55°C.

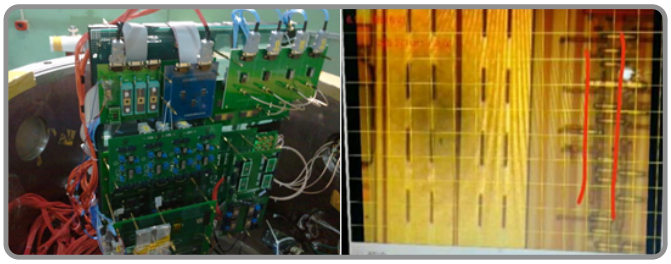

Fig. 10. Radiation test setup utilising the radiation chamber facilities of the China Institute of Atomic Energy in Beijing, China.

layout of D-latch with five guard rings is 238 μm × 150 μm (Fig. 11 (b)), then 0.025 mm^2 of area overhead for one D-latch. There are in total 64 D-latches, leading to 1.6 mm^2 of area overhead for all of the D-latches.

Some similar commercial products are compared with the proposed 4-channel 12-bit DAC, as shown in Table II. The proposed novel layout of resistive array can ensure enough static linearity and obviate the calibration of R-2R DAC, superior to all the other four products (all need laser-trimming). Among all the products, AD 7837 achieves the best DNL and INL only with 2 channels. For 4-channels products, the proposed design in this paper shows very good static linearity. Finally, only the proposed DAC considers the resilience to radiation, which makes it suitable for broader applications compared with others.

V. Conclusion

This paper uses a 0.5-μm HV BiCMOS process to design a monolithic 4-channel 12-bit high-voltage radiation-tolerant DAC chip, output voltage ranges from −10 V to +10 V. The experiment results show that the power consumption is less than 525 mW. Both the DNL and INL are well within 1 LSB, close to the ideal performance of DAC.

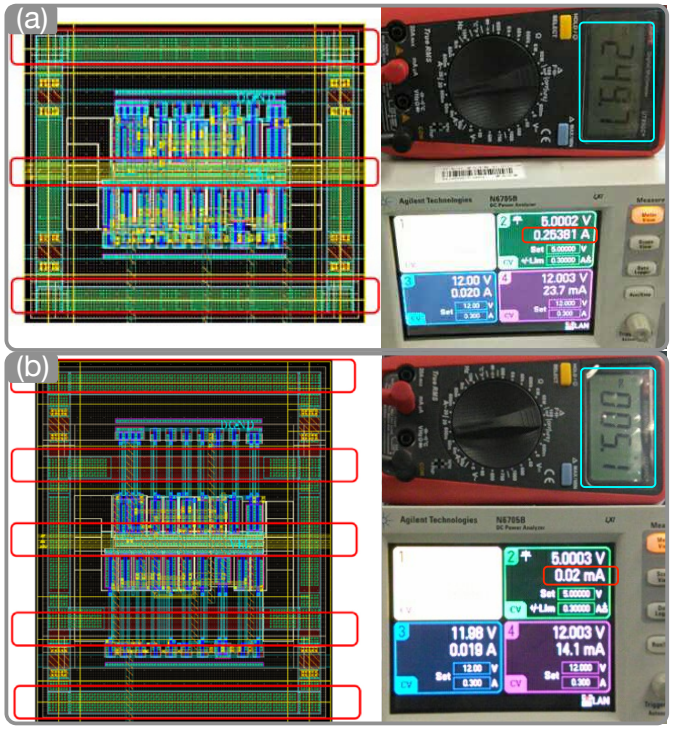

Fig. 11. (a) Conventional layout of D-latch with three guard rings and 0.25 A of 5V digital power supply demonstrates that the latch-up occurs. (b) Improved layout of D-latch with five guard rings and 0.02 mA of 5V digital power supply demonstrates that the latch-up disappears.

VI. Acknowledgments

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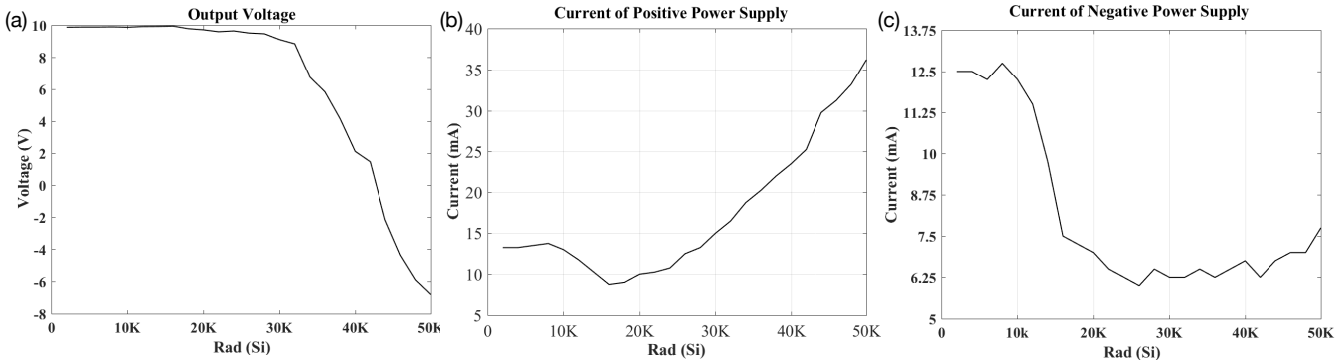

Fig. 12. Measured results of the fabricated 12-bit DAC: (a) Output Voltage, (b) Current of Positive Power Supply, and (c) Current of Negative Power Supply.

TABLE II
COMPARISON OF PERFORMANCE ON SEVERAL COMMERCIAL DACS

	This work	AD664 [7]	DAC8412 [23]	AD7837 [24]	AD8522 [25]
Resolution (bits)	12	12	12	12	12
Technology	BICMOS	BICMOS	BICMOS	CMOS	CBCMOS
Number of Channels	4	4	4	2	2
Temperature Range (°C)	[-55, 125]	[-55, 125]	[-55, 125]	[-55, 125]	[−55, 125]
DNL (LSB)	0.23	0.75	1	0.1	1
INL (LSB)	0.67	0.75	1	0.2	1.5
Calibration of R-2R DAC	no	laser-trimming	laser-trimming	laser-trimming	laser-trimming
Resilience to radiation design	yes	no	no	no	no
Package (mm×mm×mm)	CQFJ44 16.5×16.5×1.8	DIP28 36.6×13.5×9	LCC28 11.2×11.2×2.4	DIP24 31.1×6.6×3.25	SOIC14 8.65×3.9×1.55

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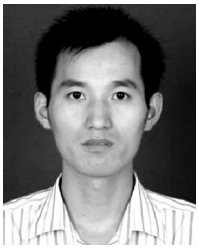

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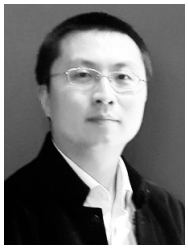

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