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III-V Device Integration on Silicon Via Metamorphic SiGe Substrates

J.A. Carlin[a], C.L. Andre[b], O. Kwon[c], M. González[a], M.R. Lueck[a], E.A. Fitzgerald[d], D.M. Wilt[e], and S.A. Ringel[a]

[a] Dept of Elec and Comp Eng, The Ohio State University, Columbus, Ohio 43210, USA
[b] Akso Nobel Chemical LLC, Chicago, Illinois 60607, USA
[c] Lumileds, Inc., San Jose, California 95136, USA
[d] Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA
[e] NASA Glenn Research Center, Cleveland, Ohio 44135, USA

A range of high performance minority carrier devices have been successfully fabricated on Si "virtual" substrates where threading dislocation densities (TDDs) as low as $1x10^6$ cm^{-2} are routinely achieved. Minority carrier lifetime data achieved on GaAs-on-Si layers exploiting this novel SiGe buffer approach to monolithic integration (τ_p = 10.5 ns and τ_n = 1.7ns) verifies the high III-V material quality. Single junction GaAs solar cells with high efficiencies for GaAs/Si of 18.1% under AM1.5-G illumination were demonstrated. Further exploiting the novel GaAs/Si material quality, even more complex minority carrier devices including dual-junction solar cells and LEDs were fabricated, yielding high performance consistent with the high III-V/Si mobilities. In both cases, certain device metrics on SiGe outperformed identical GaAs monolithic devices. Finally, a visible laser on Si was achieved, demonstrating the success and further potential of this III-V/Si integration methodology.

Introduction

The range of lattice constants accessible in the SiGe alloy system opens an opportunity for direct, all-epitaxial integration of III-V materials and devices on Si. Using SiGe interlayers grown on Si, the ability to generate a "virtual" substrate in which the surface lattice constant can be adjustable is proving to be a promising path to monolithically integrate III-V devices and performance-enhancing III-V layers with Si-based electronics. While our previous work has successfully demonstrated the ability to obtain high quality III-V compounds on Si via a relaxed SiGe graded buffer and strict control of the III-V/Ge interface, the ability to capitalize on promising material results to realize advanced minority carrier devices is a hurdles that is seldom realized although reports of low dislocation, high quality III-V materials on Si being achieved have been plentiful (1,2). Here, we summarize the integration of various III-V minority carrier devices on GaAs/Si using an integration approach where low reported TDDs have resulted in high minority carrier lifetimes, successfully demonstrating that III-V material quality can translate into device performance for this integration approach. Specifically, growth, characterization and device results for III-V high performance single and dual-junction solar cells, visible wavelength LEDs and visible wavelength laser diodes monolithically integrated on Si via ultra low dislocation density SiGe interlayers will be discussed.

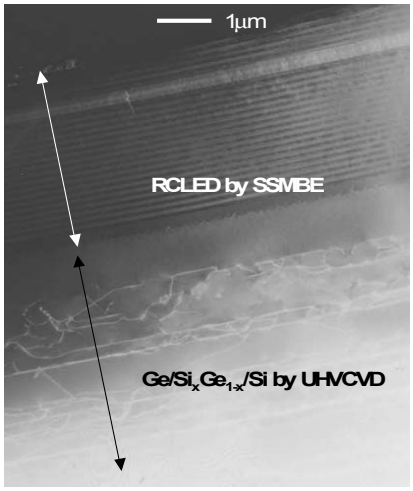


Figure 1. Cross sectional TEM image of a III-V device layer grown on a SiGe substrate.

Experimental

All the device structures discussed here were grown by molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) on "virtual" Ge-on-Si starting substrates. The virtual Ge substrates were generated on Si using an ultra high vacuum chemical vapor deposition process by which SiGe layer composition was stepped from Si to Ge at an average grading rate of 10% Ge/μm. The grade is interrupted at the 50% Ge layer to perform a critical chemical mechanical polishing (CMP) step to remove the deepest "crosshatch" features that cause dislocation pinning and pileup formation, thus promoting efficient dislocation glide without unnecessary nucleation of new dislocations. Additional details of the SiGe substrate process are described elsewhere (1). Final threading dislocation densities (TDD) of the relaxed Ge/SiGe layers used for III-V overgrowth were typically 1-4x10^6 cm^{-2} as measured by plan-view TEM, etch pit density (EPD) and electron beam induced current (EBIC) but have been measured as low as 8x10^5 cm^{-2} using the relaxed SiGe graded buffer technology. III-V growth was subsequently initiated by MBE using methods previously demonstrated to control nucleation of the III-V/Ge interface, enabling elimination of anti-phase domains and cross-diffusion of Ga, As and Ge to below SIMS detection limits for a GaAs nucleation layer of less than 100nm (2). For all GaAs/SiGe/Si epi structures discussed here, GaAs nucleation was completed by MBE using this method and capped with 100nm of GaAs grown at 500^{o}C as described elsewhere (3,4). Following this initial nucleation, either MBE or MOCVD was used to grow the devices as indicated in the following sections. As shown in the TEM image of Figure 1 for an AlGaInP LED grown on SiGe, very abrupt III-V interfaces, critical for successful device operation, are obtained using this direct growth approach on an engineered substrate that had no final surface polish. Similar results have been obtained for both MBE and MOCVD grown devices, both of which will be discussed in this work. Larger scale plan-view TEM and EPD images reveal that the TDD values within the III-V layers match those found within the virtual substrates, showing that heterogeneous nucleation of new dislocations at the III-V/IV interface is minimal and an ideal low mismatched heteroepitaxial condition is achieved. Higher resolution images also confirm the complete lack of the electrically active antiphase domain boundaries which are typical of a polar/non-polar epitaxial interface.

Device specific experimental parameters will be discussed individually in the following sections.

Material Characterization and Device Performance

Minority Carrier Lifetime

The ability to control the nucleation and propagation of threading dislocations (TDs) has been a consistent metric for characterizing the quality of highly lattice mismatched metamorphic layers and, more specifically, GaAs integration on Si substrates. However, although many reports over the years have claimed TDD's below $1x10^6$ cm^{-2}, these reports have not subsequently been able to successfully realize III-V optoelectronic integration on Si. In part, this discrepancy can be attributed to the difficulty of accurately counting the dislocation density within the metamorphic III-V materials which then leads to incorrect assumptions about the III-V material quality. To resolve this inconsistency, rather than rely solely on the determination of TDD, a more direct indication of how the GaAs/Si integration will translate to device performance has been adopted. Specifically, minority carrier lifetimes in GaAs layers grown on Si-based substrates have been studied over the last 15 years to accurately assess the quality of these metamorphic III-V layers (2, 5-11). Consistent with the wide range of TDD's that have been reported for varying GaAs/Si integration approaches, a large variation in lifetime has been measured stemming from the epitaxial hurdles present in the GaAs/Si material system; namely, a 4% lattice mismatch and a nonpolar/polar interface. The influence of lattice mismatch on lifetime has been modeled as

$$\frac{1}{\tau} = \frac{1}{\tau_{\max}} + \frac{1}{\tau_{TDD}}, \quad \text{where} \quad \tau_{TDD} = \frac{4}{\pi^3 (D)(TDD)}, \qquad [1]$$

τ_{max} represents the minority carrier lifetime in the absence of TDs and τ_{TDD} represents the lifetime contribution resulting from recombination at TDs, which depends on *D*, on the minority carrier diffusion coefficient, and on the TDD (10,12). In one instance, minority carrier lifetime measurements facilitated using GaAs double heterostructures (DHs) grown on Si substrates via direct epitaxy using III–V strained-layer superlattices as interlayers have been reported to be up to 2 ns in *n*-type GaAs. These lifetimes are believed to be defect-limited due to the high residual TDDs (>$7x10^6$ cm^{-2}) and the fact that these lifetimes are much lower than homoepitaxial lifetimes (τ_{max}) achieved at the same dopant concentrations (7-10). Other attempts to reduce the TDD and thus increase τ_p have utilized thick Ge layers or $Si_{0.04}Ge_{0.96}$ layers, resulting in reported lifetimes of 3 and 2.5 ns, respectively (5,6). However, while these lifetimes are some of the highest reported, no reports have produced lifetimes which would be consistent with achieving TDD's approaching $1x10^6$ cm^{-2}. Recently, our work using compositionally graded SiGe up to 100% Ge has resulted in reports of TDDs in GaAs on Si of ~$1x10^6$ cm^{-2}. Verifying the accuracy of these TDD measurements, here we discuss the highest minority carrier lifetimes reported to date which are consistent with theory, equation [1].

Experimental. $Al_{0.3}Ga_{0.7}As/GaAs/Al_{0.3}Ga_{0.7}As$ DHs were grown on n-type Ge substrates and SiGe graded buffers as described above to facilitate bulk minority carrier lifetime (τ_p) measurements by room temperature time resolved photoluminescence (TRPL). TRPL was performed using a time-correlated single-photon counting technique

on the DHs under low level injection conditions by monitoring the GaAs band-to-band transition wavelength. (Further details on this measurement technique can be found in Ref. 11) TDD for the SiGe graded buffers used in these experiments ranged from $8x10^5$ – $2x10^6$ cm^{-2} as measured by etch pit density, plan-view TEM and EBIC. All III-V layers were grown by solid source MBE. All DHs were nominally silicon doped $n=1x10^{17}cm^{-3}$ with multiple GaAs well thicknesses of 0.5, 1.0 and 1.5μm. Additionally, the GaAs buffer thickness grown prior to the active III-V layers was varied from 0.1 to 1.0μm to assess the dependence of the III-V layer quality on the proximity to the GaAs/Ge interface.

Results and Discussion. Figure 2(a) shows a collection of TRPL lifetime data extracted from standard luminescence decay measurements for DHs on Ge and GeSi substrates. In all cases, the data was successfully fit with well-defined, single exponential decay transients. Assuming identical interface recombination velocities (S) at the upper and lower interfaces, τ_p and S can be extracted from the TRPL lifetime (τ_{TRPL}) by

$$\frac{1}{\tau_{TRPL}} = \frac{1}{\tau_p} + \frac{2S}{d}, \qquad [2]$$

where (d) is the thickness of the GaAs in the DH structure (7). For the control samples on the Ge substrate, figure 2(a) shows consistent S and τ_p (17-19 ns) values independent of the GaAs buffer thickness used. These results are comparable to published results for homoepitaxial GaAs in the absence of photon recycling, implying, in agreement with XTEM data, that proper control of the GaAs/Ge interface enables the elimination of electrically active APD defects and the growth of high quality GaAs in close proximity to the GaAs/Ge heterointerface. Figure 2(a) also provides data for DH growth on graded SiGe "virtual" substrates with a minimal 0.1μm GaAs buffer. Values for the interface recombination velocities (S) comparable to that found for the Ge substrate indicate that the periodic crosshatch morphology inherent in the fabrication of the graded SiGe substrates does not have significant impact on the interface properties at this scale. Additionally, the n-GaAs minority carrier lifetime was found to be as high as τ_p = 10.5ns,

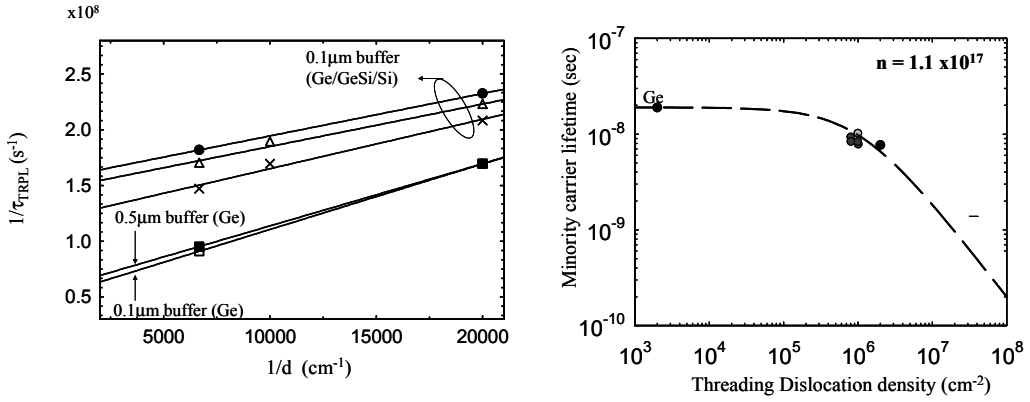


Figure 2. (a) Plot of TRPL lifetime versus DH thickness extracted from TRPL decay curves on both Ge and SiGe substrates for varying GaAs buffer thicknesses and (b) t_p values plotted with theoretical lifetime dependence on TDD, equation [1].

the highest value reported for GaAs on Si. Figure 2(b) shows a plot of equation [1] with τ_{max} = 19ns, consistent with the GaAs quality on the Ge substrate and D_p = 7.1 cm^2/s for holes in n-type GaAs. The results for the lifetimes obtained from the TRPL data on the SiGe graded buffer are plotted against this theoretical curve for measured TDD values. As shown, below a TDD of ~1x10^6 cm^{-2} the lifetime is extremely sensitive to the TDD. While previous reports have indicated the reduction of TDD's below 1x10^6 cm^{-2} and lower, no previous reports have successfully obtained lifetimes greater than 3ns, indicating either the incorporation of an additional lifetime limiting defect or a mischaracterization of the true TDD. Here, the ability to consistently obtain TDD's in GaAs/Si as low as 1x10^6 cm^{-2} through 1) the use of SiGe graded buffers and 2) precise control of the GaAs/Ge interface is consistent with the demonstration of lifetimes in excess of 10ns (Figure 2(b)) and has significant implications for realizing the promise of integrating III-V devices on Si substrates. This high τ_p and thus high material quality for metamorphic GaAs grown on SiGe has provided a realistic opportunity for epitaxially integrating various III-V compounds with Si, the remaining challenge being a demonstration that the high minority carrier lifetime (not TDD) can successfully translate into minority carrier device performance. To that end, high-performance minority carrier III-V devices, such as solar cells, light emitting diodes, and laser diodes have been designed and fabricated. Discussions and characterization of those devices successfully exploiting the high minority carrier lifetime provided by the SiGe integration pathway to GaAs/Si are reviewed in the following sections.

Solar Cells

The desire to integrate high efficiency and radiation resistant III-V solar cells for space applications on alternative substrates that are stronger, lighter and less expensive than III-V substrates has led to the development of various types of III-V cells on Ge wafers, since Ge offers advantages in strength and cost over GaAs while providing a similar lattice constant. However, the attributes of Ge are less desirable than Si, the preferred alternative substrate, which is far cheaper, lighter, stronger and possesses a higher thermal conductivity. Unfortunately, until recently GaAs/Si solar cells, where device performance is dominated by minority carrier collection in the base region, were impractical and unsuccessful due to the lifetime limitations (<1-3ns) inherent in the high TDD integration approaches. Applying the results discussed above, we have the opportunity to exploit the high minority carrier lifetimes accessible in the GaAs/Si system by the SiGe graded buffer to enable high efficiency GaAs/Si solar cells and demonstrate the successful transition from material quality metrics (τ_p) to device performance. Here, in addition to results from the fabrication of single-junction (SJ) solar cells more structurally complex dual-junction (DJ) high efficiency solar cells are also discussed.

Experimental. SJ GaAs solar cell structures were grown by MOCVD after deposition of a 0.1 μm GaAs nucleation layer by MBE on the SiGe substrates as previously discussed. Further details concerning the influence of MOCVD over growth on the MBE initiation layers can be found elsewhere (14,15). The GaAs and $In_{0.49}Ga_{0.51}P$ layers were grown at a substrate temperature of 620°C, a growth rate ~ 2 μm/hr, and a V/III ratio of 100. The $In_{0.49}Ga_{0.51}P$/GaAs p+/n DJ solar cell device layers were grown by solid source MBE. The growth rates used for the bottom cell were 1.0 μm/hr and 0.6 μm/hr, for the GaAs and $Al_{0.7}Ga_{0.3}As$ layers, respectively. N-type GaAs and $Al_{0.7}Ga_{0.3}As$ layers were grown at 610°C with an As_2:III beam equivalent pressure (BEP) ratio of 14:1 with

p^{++} GaAs contact layer (1000Å)	~1x10^{19} cm^{-3}
p^{+} $In_{0.49}Ga_{0.51}P$ window (500 Å)	~1x10^{18} cm^{-3}
p^{+} GaAs emitter (5000 Å)	~2x10^{18} cm^{-3}
n GaAs base (2.0 μm)	~1x10^{17} cm^{-3}
n^{+} $In_{0.49}Ga_{0.51}P$ back surface field (1000 Å)	~1x10^{18} cm^{-3}
n^{+} GaAs buffer (1000 Å)	~1x10^{18} cm^{-3}
low-temperature n^{+} GaAs buffer (1000 Å)	~2x10^{18} cm^{-3}
SSMBE Ge buffer layer (300 Å)	uid
Ge termination layer (~1.0 μm)	~1x10^{18} cm^{-3}
n SiGe step graded buffer layers (~ 10 μm)	~1x10^{18} cm^{-3}
n Si substrate	~0.5-2 1x10^{18} cm^{-3}

(a)

p++ GaAs contact layer (1000 Å)	~1x10^{19}
p+ $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ window (300 Å)	~2 x10^{18}
p+ $In_{0.49}Ga_{0.51}P$ emitter (500 Å)	~2 x10^{18}
n $In_{0.49}Ga_{0.51}P$ base (5500 Å)	~7 x10^{16}
n+ $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ back surface field (300 Å)	~2 x10^{18}
n++ GaAs TJ (250 Å)	~2 x10^{19}
p++ GaAs TJ (250 Å)	~2 x10^{19}
p+ $In_{0.49}Ga_{0.51}P$ window (400 Å)	~3 x10^{18}
p+ GaAs emitter (5000 Å)	~2 x10^{18}
n GaAs base (20,500 Å)	~2 x10^{17}
n+ $Al_{0.7}Ga_{0.3}As$ back surface field (1000 Å)	~2 x10^{18}
n+ GaAs buffer (2000 Å)	~2 x10^{18}
Ge (300Å)	uid
n+ SiGe substrate	~1 x10^{18}

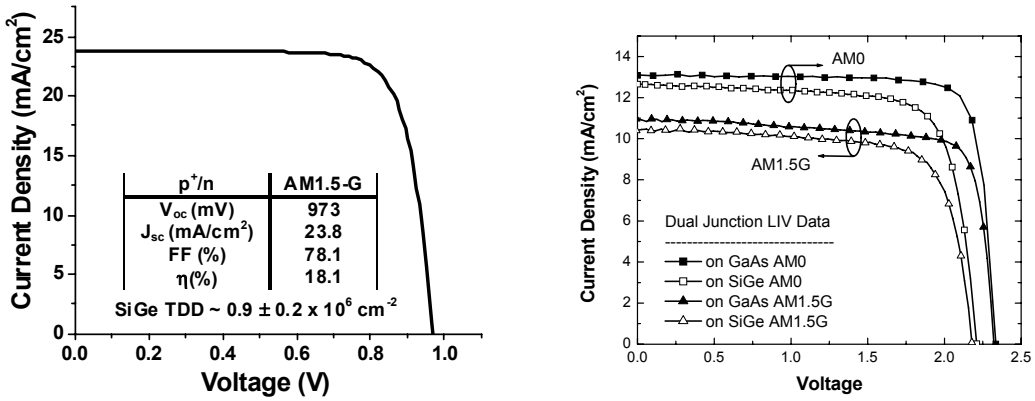
(b)

Figure 3. (a) SJ GaAs p+/ and (b) DJ InGaP/GaAs p+/n solar cell structures on SiGe.

reference to the Ga BEP, while the p-type GaAs and $Al_{0.7}Ga_{0.3}As$ layers were grown at 575°C with an As_2:III ratio of 24:1. The GaAs tunnel junction layers were then grown at 550°C with an As_2:III ratio of 24:1 and a growth rate of 0.6 μm/hr. Subsequently, the $In_{0.49}Ga_{0.51}P$ and $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ layers were grown at a rate of ~ 1.15 μm/hr, a growth temperature of 490°C, and a P_2:III BEP ratio of 9:1 with reference to the In BEP.

Figure 3(a) shows the standard SJ GaAs heteroface solar cell structure while figure 3(b) shows the standard structure used for the DJ cells. Cells were grown on both GaAs, Ge and SiGe substrates in both cases. XTEM of the SJ solar cell structure grown on SiGe shows no structural defect formation at the MBE / MOCVD regrowth interface following the growth stop and transition to the second growth environment. Moreover, higher magnification images also confirm the suppression of APD disorder at the MBE GaAs/Ge interface for both cell structures as expected. Devices were processed using conventional photolithography and wet chemical etching. During final processing an anti-reflection coating (ARC) of MgF_2 / ZnS / MgF_2 was deposited in a thermal evaporator. Illuminated current density versus voltage (J-V) measurements under AM0 and AM1.5-G spectrums were measured at the NASA Glenn Research Center and the National Renewable Energy Laboratory, respectively, in order to determine the short-circuit current density (J_{sc}), the open-circuit voltage (V_{oc}), the fill-factor (FF), and the efficiency (η) of the solar cells for space (AM0) and terrestrial (AM1.5-G) applications.

SJ Solar Cells Results. Figure 4(a) shows the illuminated current density versus voltage (J-V) response for a p+/n single junction GaAs solar cell grown on a SiGe/Si substrate. AM1.5-G energy conversion efficiencies reached 18.1%, the highest independently verified one-sun efficiency reported to date for a single p^+/n or n^+/p junction GaAs solar cell grown on a Si-based substrate (16,17). The AM0 efficiency for the same cell shown in figure 4(a) was 15.5% with a V_{oc} of 980 mV, and is also the highest independently verified efficiency and V_{oc} reported to date under this spectrum (17). The high performance obtained, in spite of the large lattice mismatch (4%) between the fully relaxed GaAs cell and the Si substrate, is attributed to the achievement of a high V_{oc}, 973 mV, which is the consequence of maintaining a low TDD value of ~ 1x10^6 cm^{-2} while simultaneously eliminating other mismatch related defects such as anti-phase domains and auto-doping, which could otherwise lower V_{oc} (2,3). These already high efficiencies are limited by a large, 10%, design induced metal grid finger shadowing. A



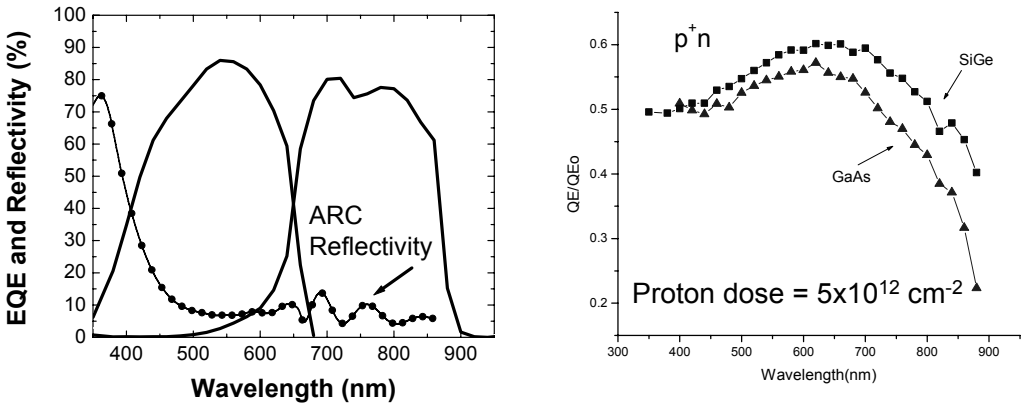
(a) (b)

Figure 4. Illuminated J-V curves under (a) AM1.5-G spectra for a SJ cell (area=0.0444 cm^2) grown on SiGe substrate and (b) AM0 and AM1.5-G spectra for DJ cells grown on GaAs and SiGe substrates.

more accurate comparison with previous results would be obtained by scaling the data in figure 4(a) for a metal coverage 4.5%, commensurate with the GaAs/Si cell from (16) and (17). This yields efficiencies for GaAs/SiGe/Si of 18.8% and 16.5% at AM1.5-G and AM0, respectively, more than 1% absolute higher than other verified reports (18-20).

The high V_{oc} values obtained in this work are responsible for the high cell efficiency. Compared with reports where a TDD of ~ $8x10^6$ cm^{-2} produced an AM1.5-G V_{oc} of 891 mV, the reduction in the TDD in SiGe/Si substrates to ~$1x10^6$ cm^{-2} reduced the dislocation-mediated depletion region recombination in the GaAs/SiGe solar cells and thus increased the V_{oc} to 973 mV (16). The inability to reduce the TDD below ~ $5x10^6$ cm^{-2} using other direct III-V/Si integration methods had been the primary impediment to achieving higher efficiency GaAs-on-Si solar cells which stalled research in this area (12). Modeling of this recombination process has predicted theoretical V_{oc} values that track the experimental results as a function of TDD for various GaAs/Si and GaAs/SiGe/Si cell structures. These results directly track the lifetime versus TDD dependence shown in figure 2(b), and predict that a TDD of ~ $5x10^5$ cm^{-2} is needed for heteroepitaxial GaAs p+/n cells to achieve V_{oc} values in excess of 1000 mV, which would closely match state of the art homoepitaxial GaAs cells.

DJ Solar Cells Results. Building on the SJ solar cells successful realization of device performance from the promising material quality metrics, more complex device structures were pursued. Specifically, DJ solar cells requiring not only GaAs and AlGaAs layers similar to that required for the SJ design but large bandgap materials (InGaP and InAlGaP) and thin (500Å) tunnel junctions were fabricated to further demonstrate the robust nature of this III-V/Si integration methodology. Figure 4(b) shows AM0 and AM1.5G lighted J-V measurements on tandem cells grown on SiGe and on GaAs substrates. Total area efficiencies of 15.3 % and 18.6 % for AM0 conditions and 16.8% and 20.0% for AM1.5G conditions were obtained for the cells grown on SiGe and GaAs, respectively. Details of current collection for the tandem design can be seen in figure 5(a), which shows a typical external quantum efficiency (EQE) spectrum for one of the DJ cells along with the measured reflectivity of the ARC. EQE is a measure of the



(a) (b)

Figure 5. (a) EQE of the GaInP and GaAs subcells of a dual junction grown on GaAs. Reflectivity of a non-optimum ARC coating is also shown. (b) Normalized EQE data for SJ-GaAs p^+/n cells on GaAs and SiGe following a proton dose of $5x10^{12}$ cm^{-2}.

carrier collection as a function of wavelength, with the higher energy particles being collected in the top cell and the lower energy particles collected in the bottom cell. Integration of AM0 J_{SC} values for the subcells shows successful current matching in the cell design and is in close agreement with the true measured J_{SC} for the tandems, indicating that the presence of residual threading dislocations for the cells on SiGe have no differential effects on subcell current generation and current matching. However, figure 5(a) also clearly reveals external limitations reducing collection efficiency below 540 nm (InAlGaP window and ARC layer) which must be improved in order to increase the overall cell efficiency. The high V_{OC} of 2.2 V, which is within 150 mV (~95%) of the control device Voc on GaAs, is attributed to the low TDD maintained throughout the entire DJ structure grown on the graded SiGe, and is indicative of low carrier recombination rates throughout the bulk and interface regions of the DJ cell. Further, filtered light I-V measurements made on the DJ/Si cell through a 1.24 eV low pass filter confirmed that no photovoltage was emanating from the GaAs/Ge interface region on the SiGe substrates, verifying that the high Voc is due to only the additive effects of the GaInP and GaAs subcells as desired and electrical control of the GaAs/Ge heterovalent interface was maintained. Separate measurements of GaAs and GaInP single junction cells grown on identical SiGe substrates display individual V_{OC} values of 0.95 and 1.28 V respectively, closely matching the Voc output of the DJ cell. This important result suggests minimal voltage loss due to the thin interconnecting tunnel junction in spite of growth on the crosshatched SiGe surface. Overall, while the ultimate efficiency of these preliminary devices is limited by external processing factors, J-V and EQE measurements show high Voc and successful tunnel junction operation consistent with previous material quality metrics and indicate that the sub-cells did not suffer from the more complex DJ growth process compared to the simpler SJ cell growths (21).

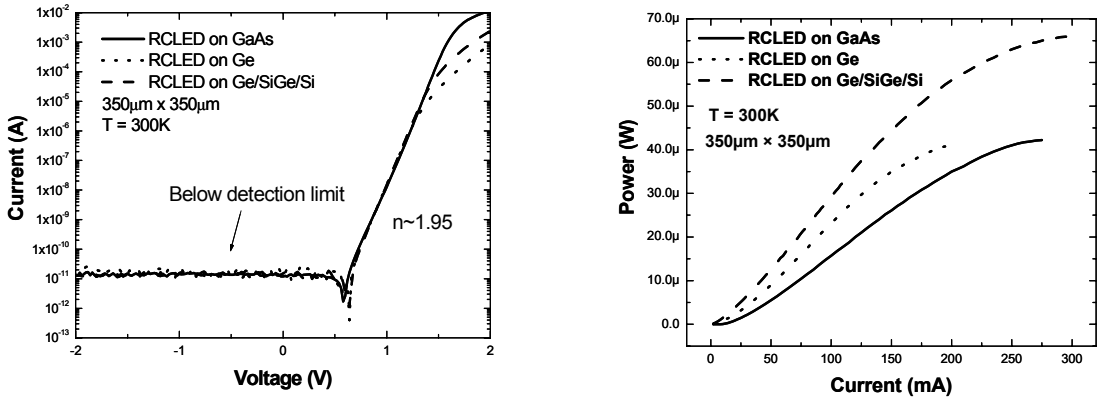
Space Flight and Radiation Testing. Further highlighting the promise of this approach for space PV applications, the above research was selected to participate in the Materials International Space Station Experiment number 5 (MISSE5) for on orbit testing of advanced photovoltaic technologies in the low Earth orbit (LEO). The payload, deployed on the International Space Station in August 2005 for a projected one year on

orbit test, consisted of five GaAs/SiGe cells (three with area = 4.0 cm^2, two with area = 1.0 cm^2) and two GaAs homoepitaxial control samples (area = 4.0 cm^2) that were fully packaged and mounted consistent with space payload requirements. Constant device performance monitoring during orbit indicates normal cell operation and no degradation in the GaAs/Si device performance (J_{sc}, V_{oc}, FF, η) during the initial 6 month period of data acquisition currently available (22,23). Combined with the promising results discussed above, the ability to withstand packaging, thermal cycling and operation in the space environment without degradation is proving the SiGe integration approach to be a promising technology. Finally, while the MISSE5 experiment was not completed in a heavy radiation environment, one important metric which must be considered for all solar cells operating in a space environment is the "hardness" of the cell performance to the radiation damage inherent in the space environment and the impact on end-of-life (EOL) performance. Toward this end, the effects of 2MeV proton irradiation on the introduction of recombination centers (defect/trap levels) in III-V solar cells on SiGe substrates were investigated by deep level transient spectroscopy (DLTS). Results showed no variation in the radiation induced trap states/levels for p+/n or n+/p devices on GaAs, Ge or SiGe substrates. However, the introduction of the SiGe substrate was found to improve the radiation tolerance of the devices, resulting in as much as a 40% reduction in the trap introduction rate for hole traps in p-type GaAs. Demonstrating the direct impact of this fact on device performance, figure 5(b) shows normalized EQE data for SJ-GaAs following a proton dose of $5x10^{12}$ cm^{-2}. The EQE results indicate far less degradation in the EQE response, particularly at longer wavelength, after radiation damage for cells grown on SiGe versus homoepitaxial GaAs. The improved radiation tolerance can be attributed to the interaction between radiation-induced point defects and residual dislocations present in the metamorphic GaAs/SiGe samples and represents a significant performance advantage to EOL device performance (24).

Visible Emitters - RCLEDs and Lasers

The desire to integrate III-V optoelectronic devices with Si for added functionality and the realization of system on a chip designs has long called for the ability to integrate emitters on Si. Unfortunately, the demanding material quality requirements and complex designs for such devices have kept the promise of such integration unrealized to date. However, with the successful application to large area solar cells discussed above and the apparent lack of additional recombination centers in the III-V/SiGe material over homoepitaxial GaAs as indicated by DLTS data, the SiGe system appears to be well suited for the realization of even more complex and material-quality demanding III-V devices (24). To further explore the applicability of the SiGe system for device integration and specifically to investigate the impact of this methodology on III-V radiative recombination pathways in optical devices, both surface emitting resonant cavity light emitting diodes (RCLEDs) and AlGaInP graded index separate confinement heterostructure (GRIN-SCH) visible lasers were fabricated. In combination with the large area solar cells devices described above, the successful realization of III-V emitters on Si would represent a complimentary set of material-quality demanding minority carrier devices and would demonstrate the real potential for this monolithic integration technique.

Experimental. Following standard MBE initiation for interface control (for the Ge and SiGe substrates only) as described above, epitaxial growth for the RCLED device layers and AlGaInP GRIN-SCH visible laser structures were subsequently performed at



(a) (b)

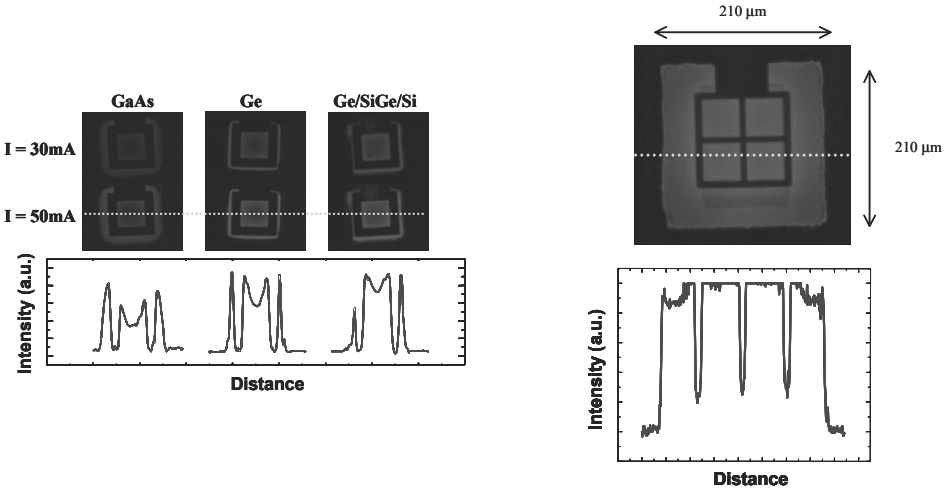
Figure 6. (a) Dark current versus voltage (I-V) and (b) output power versus current (L-I) data for RCLEDs on GaAs, Ge and SiGe substrates.

substrate temperatures of 620°C for As based and 490°C for P based active layers. For the RCLED devices, a one-λ thick AlGaInP optical cavity was grown, which consisted of a 4-period 80 Å $Ga_{.51}In_{.49}P$/60Å $(Al_{.3}Ga_{.7})_{.51}In_{.49}P$ multiple quantum well surrounded by n and p type $(Al_{.3}Ga_{.7})_{.51}In_{.49}P$ spacer layers designed for a target emission wavelength of 650 nm. The one-λ cavity was sandwiched between an n-type bottom distributed Bragg reflector (DBR) consisting of 18 periods (~ 97 % reflectivity) and a p-type top DBR consisting of 5 periods (~ 74 % reflectivity). Both λ/4 DBRs were comprised of $AlAs/Al_{.5}Ga_{.5}As$ periodic structures doped p-type (2×10^{18} cm^{-3}) and n-type (2×10^{18} cm^{-3}) for the top and bottom, respectively. Ring geometry mesa devices with dimensions ranging from 100 μm to 350 μm were fabricated as described elsewhere (25). All RCLED devices were processed in the same manner except for the additional RCLED on SiGe that incorporated a thick AlGaAs current spreading layer, for which a mesh type top metal contact layer was applied instead of a ring type contact to improve current spreading. The GRIN-SCH structure consists of a compressively strained 70 Å $Ga_{.42}In_{.58}P$ single quantum well (QW) symmetrically surrounded by 1250 Å thick $(Al_{.6}Ga_{.4})_{.51}In_{.49}P$ confinement layers and in turn by 250 Å thick graded layers for which the $(Al_xGa_{1-x})_{.51}In_{.49}P$ composition linearly varies from x = 0.6 to x = 0.7. The details of the GRIN-SCH design and processing, target emission wavelength of 680 nm, can be found elsewhere (26). Full laser structures were fabricated into ~ 1300 μm long oxide-strip gain-guided lasers having widths ranging from 10 μm to 100 μm, where a 2000 Å thick dielectric Si_3N_4 film by plasma enhanced chemical vapor deposition was used for electrical isolation.

RCLED Results and Discussion. Figure 1 above shows a cross-sectional TEM image of an entire RCLED device structure grown on SiGe, where the desired confinement of a high density of threading dislocations in the SiGe buffer is observed and sharp device interlayers and RCLED/SiGe interfaces are evident. TDD values of ~ 1×10^6 cm^{-2} were confirmed as discussed above for device layers on the SiGe substrates using EPD, EBIC and plan-view TEM. Basic electrical and optical characteristics of processed devices were examined by current versus voltage (IV) and electroluminescence (EL) measurements at 300K. Figure 6(a) shows the measured IV curves of three RCLEDs grown on the different substrates. All IV curves are nearly identical with ideality factor

of about 1.95 for 350 μm × 350 μm mesa devices before reaching the high current injection region that generates series resistance roll-off. Extremely low reverse leakage currents that are below detection limit were achieved for devices grown on either Ge or SiGe substrates. The outstanding IV characteristics and their close match with the homoepitaxial device results confirm the high electronic quality of the devices in spite of the large total lattice mismatch between the AlGaInP RCLED and the Si substrate, consistent with the structural quality shown in figure 1 and demonstrate in the solar cells discussed above. The behavior of these large bandgap AlGaInP devices on Si is also consistent with the high quality results for large area III-V solar cells discussed in the previous section (18-20).

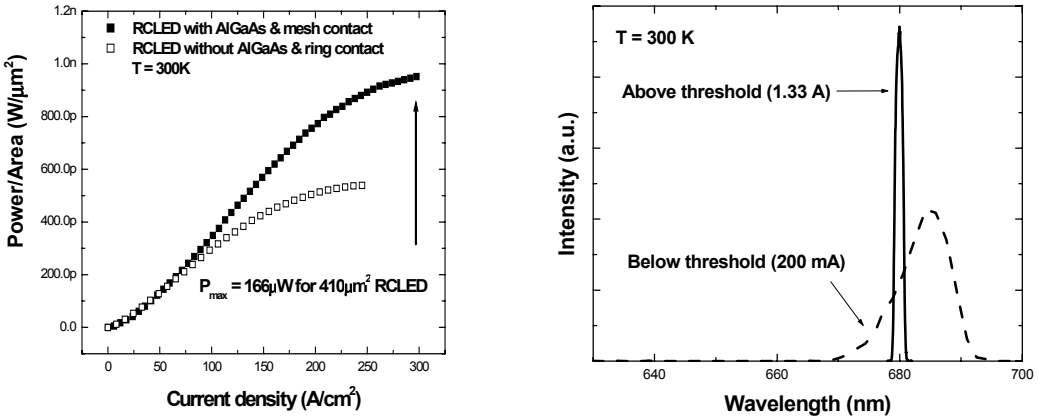
Normalized EL spectra were taken for RCLEDs grown on different substrates, where the sizes of RCLEDs are identical and EL measurements were performed under 160 mA of continuous current injection. No attempts to control sample heating were made at this time. The center emission wavelengths were 658.5 nm, 656.5 nm, and 662 nm for RCLEDs grown on GaAs, Ge, and SiGe substrates and full width half maximum (FWHM) values of 5.3 nm, 4.5 nm and 7.0 nm were obtained, respectively. Figure 6(b) shows output power obtained as a function of continuous current injection for devices grown on GaAs, Ge, and graded SiGe substrates. Again, no attempts to prevent current induced heating were made. As can be seen, the RCLED grown on SiGe outperformed the RCLEDs grown on Ge and GaAs substrates, with 66 μW maximum output power achieved at 300 mA injection current, where the output power was measured by using a calibrated Si photodetector facing on top of the RCLED surface. There are several reasons that may explain this observation. As shown, the optical output power from the devices grown on Si saturates at much higher current injection levels compared to the other substrates. This implies that the higher thermal conductivity of Si (1.3 W $cm^{-1}°C^{-1}$) as compared to 0.55 W cm^{-1} $°C^{-1}$ and 0.58 W cm^{-1} $°C^{-1}$ for GaAs and Ge, respectively, may play a role in removing heat due to high current injection. Another likely explanation has to do with differing amounts of current spreading as a function of substrate and the role of dislocations for the device grown on SiGe. In this case, there exists a high density of dislocations only within the planar SiGe buffers buried beneath the n-side of the RCLED mesa area. Hence, electrons injected through this dislocation network are randomly spread by the local resistances attributed to individual dislocations as discussed in other work (27,28). This current spreading acts to diffuse injected carriers uniformly across the smaller area RCLED mesa in more random trajectories that would otherwise occur for uniform field-induced transport for typical lattice-matched structures that do not include regions of high dislocation density only on one side of the RCLED. The expected result would then be improved uniformity in radiative recombination across the active multi-quantum well region. In fact, this is exactly what is observed by electroluminescence images taken for RCLEDs grown on each of the three different substrates GaAs, Ge and SiGe/Si, as shown in figure 7(a). Even though the RCLED device structures are identical for each case, the electroluminescence intensity profiles across each RCLED indicate that the enhancement of current spreading follows the increase in dislocation density (of the passive substrate regions) from GaAs, to Ge to SiGe substrates. Note that the ratio of luminescent intensity taken from the edge of metal contact and the middle of a device mesa is evidence that the current spreading effect for the RCLED grown on the SiGe substrates is improved compared RCLEDs on the other substrates.



(a) (b)

Figure 7. EL images obtained (a) under 30 and 50mA current injection levels for identical RCLEDs on GaAs, Ge and SiGe substrates and (b) under 10mA current injection for an RCLED on SiGe after applying an AlGaAs current spreading layer and mesh top metal contact. Intensity line scans were extracted across the center of the devices at 50mA for GaAs, Ge and SiGe and 10mA for the SiGe device as shown.

The current spreading issue is a well known, important factor for obtaining high efficiency surface emitting LEDs and can be further improved by applying highly doped wide band gap materials on top of the device layers and/or by modifying the geometry of the top ohmic metal contact layer (29,30). In the general operation of these LED devices, current supplied to the top metal contact flows through the p-type layer and down through the junction where photon generation occurs. One can imagine if the resistivity of p-type layer is too high or the layer thickness is too thin, the current can not laterally spread out appreciably from the top p metal contact to the junction, thus the current flow will remain confined beneath the metal contact resulting in the trapping of light emission under the contact and re-absorption within the device layer. To examine the impact of current spreading on RCLED performance, modifications were applied such as a mesh structured metal contact and a 3 µm thick p^+ $Al_{.67}Ga_{.33}As$ layer (~ 2.05 eV bandgap) grown on top of the p-DBR. Figure 7(b) shows an EL image and intensity line scan across one of the RCLEDs on SiGe after applying these current spreading modifications. Comparing this figure with that of the original SiGe RCLED shown in figure 7(a), the intensity line scans confirm that a uniform luminescence with an even lower current injection level was achieved with the current spreading modification for similar area devices. Furthermore, figure 8(a) shows improved LI characteristics of the modified RCLED grown on the SiGe substrate. A maximum output power of 166 µW under 500 mA of current injection is now obtained for a 410 µm × 410 µm size RCLED due to enhanced current spreading as compared to the original RCLED on SiGe, confirming that current spreading is a crucial factor for improving the luminescent efficiency of the RCLED on SiGe (It should be noted that the EL power measurements were made without benefit of the usual optical enhancements found in fully manufactured RCLEDs, such as encapsulation, etc). In addition, the EL linewidth is now extremely sharp, with an FWHM value of 3.63 nm under 50 mA of current injection. This small FWHM value is equivalent or even superior to EL linewidths reported for AlGaInP RCLED devices grown on conventional lattice-



(a) (b)

Figure 8. (a) Comparison of RCLED LI characteristics on SiGe before and after designing in an AlGaAs current spreading layer and mesh top metal contact. (b) Room temperature EL spectra for the spontaneous emission below threshold (dashed curve) and the stimulated emission (solid curve) above threshold, respectively, for an AlGaInP GRIN-SCH grown on SiGe/Si.

matched GaAs or Ge substrates, indicating that the optical quality of AlGaInP red RCLEDs on Si using metamorphic SiGe buffers are appropriate for the application of high density optical data communications while proving the capability of III-V LED monolithic integration with Si VLSI circuits (30-32).

GRIN-SCH Laser Results and Discussion. Electrical and optical characteristics of the III-P/Si laser diodes were obtained by light versus current (LI) and EL spectrum measurements at room temperature. Measurements were made on the as-grown and as-cleaved edge emitting lasers in pulsed mode operation with a pulse width of 200 ns at 10 kHz repetition rate. While the formation of the laser facets on the Si-based substrates is not straight-forward, facet orientation parallel to the [110] offcut direction produced a smooth facet and demonstrated successful device operation (26). Figure 8(b) shows EL spectra obtained from a representative AlGaInP laser diode grown on SiGe. Spontaneous and stimulated emissions were observed at peak wavelengths of 684 nm and 680 nm, respectively. The spectrum for stimulated emission was measured at the current level of 1.33 A, which is close to $1.3 \times I_{th}$. The shift of the stimulated emission peak toward a shorter wavelength compared to the spontaneous emission indicates that successful population inversion has occurred in the III-P/Si laser diode. Similar threshold current densities of $J_{th} \sim 1.65$ kA/cm^2 and $J_{th} \sim 1.60$ kA/cm^2 were obtained for AlGaInP lasers grown on SiGe/Si and on GaAs substrates, respectively, by taking the dimensions of the p-contact area with no correction for the current spreading. Output powers of 80 μW for the laser diode grown on SiGe/Si and 1.04 mW for the laser diode grown on GaAs were obtained before reaching thermal saturation. To the best of our knowledge, this is the first report of room temperature stimulated emission in the visible spectrum by AlGaInP laser diodes grown on Si. While the performance for these initial devices is below that of their homoepitaxial counterparts, similar to those devices discussed above, current performance limitations do not appear to be tied to the material quality or residual TDD.

While the impact of TDD on dark line defects related to long term reliability, for these laser designs must still be analyzed, scattering losses induced by the residual cross-hatch surface roughness and current crowding associated with the lateral conduction are currently attributed to performance limitations. However, achieving lasing in these initial devices which inherently exacerbate any material quality or design limitations further highlights the promise of SiGe metamorphic substrates as a pathway to GaAs integration.

Conclusion

Using a novel SiGe graded buffer approach to III-V integration on Si, several "firsts" in device performance have been realized. After successfully realizing the high minority carrier lifetimes (τ_p=10.5ns) which are enabled when TDD values approaching $1x10^6$ cm^{-2} are achieved using the SiGe system, GaAs SJ p^+/n solar cells with high efficiencies of 18.1% under AM1.5-G illumination were demonstrated. This performance is highlighted by the ability to finally achieve the high V_{oc} values which were theoretically predicted if TDD values of ~$1x10^6$ cm^{-2} could be realized. In fact, the high V_{oc} values successfully translated to the more complex DJ design, which successfully included a thin tunnel-junction layer in spite of the inherent surface roughness, to achieve a V_{oc} > 2V. Additional radiation results on SJ-GaAs cells indicate that the integrated devices on the SiGe substrate are more radiation hard than those on homoepitaxial GaAs, providing as much as a 40% reduction in the trap introduction rate for hole traps in p-type GaAs. Capitalizing on these performance achievements, more complex and material-quality demanding visible light emitters were designed and tested. RCLEDs with a maximum output power of 166 μW and an extremely narrow FWHM of 3.63 nm were achieved. In fact, similar to the radiation results demonstrated on the SJ cells, the RCLEDs fabricated on the SiGe substrates outperformed identical GaAs homoepitaxial devices, further validating the transition of the high quality III-V materials to device performance. Finally, a room temperature visible laser on Si (AlGaInP GRIN-SCH) successfully achieved stimulated emission and was found not to be performance limited by the III-V material quality but rather surface roughness and current crowding which can be further improved in future designs. Overall, the successful demonstration of these complex and demanding prototype devices highlights the potential of the SiGe integration methodology for future optoelectronic applications and gives the promise of even more enhanced device performance for certain applications as TD levels are further reduced in future generations of the SiGe graded buffer technology.

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