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Portable Environmental Data Logger and Sensor

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PORTABLE ENVIRONMENTAL DATA LOGGER AND SENSORS

(Part II of Completion Report for Project A-023-ARK)

by

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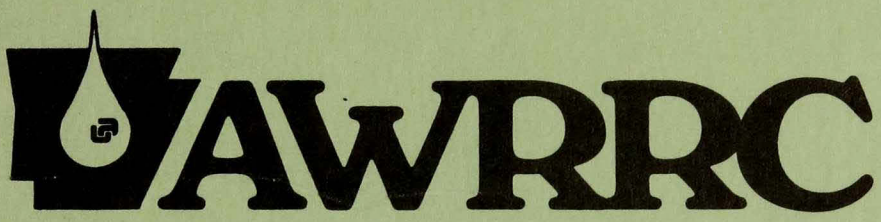
Principal Investigator



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Effects of Changes in Surface Water Regime and/or Land Use on the Vertical Distribution of Water Available for Wetland Vegetation

by

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REPORT FORMAT

Part I - Dynamic Model of the Zone of Aeration
(Included as a separate document)

Part II - Portable Environmental Data Logger and Sensors
(Included herein)

Each of Parts I and II is complete within itself, and may be distributed separately or as a single report

PROJECT COMPLETION REPORT

PROJECT NO. A-023-ARK

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PART II

PORTABLE ENVIRONMENTAL DATA LOGGER AND SENSORS

by

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ABSTRACT

An instrumentation and recording package and several transducers were constructed and used to collect data on the environmental parameters thought to affect wetland vegetation growth and reproduction. These parameters were temperature, humidity, wind velocity, depth of water table, and amount of surface water. The data were collected four times a day and recorded on a magnetic cassette tape that could record for as long as 90 days. The tapes were read and the data were converted to engineering units by a microcomputer-based instrument constructed for that purpose.

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I. INTRODUCTION

The objective of this research project was to develop a dynamic model of the zone of aeration for wetlands, describing the vertical distribution of water available for use by vegetation. This model was intended to be used to predict how the vertical distribution is affected by changes in land use or the surface water regime or both.

To acquire the data necessary for developing the model, an instrumentation system was designed to monitor the most significant environmental parameters affecting vegetative growth, reproduction, and death. This report describes the instrumentation system and its use.

The instrumentation system was constructed with state-of-the-art components to minimize power consumption and physical size. The system comprises two separate units: (1) the field unit, which is a small, battery-powered, weatherproof package that can collect and record data on audio tape cassettes for 90 days without human attention, and (2) the laboratory unit, which is the data decoder and analyzer.

The field unit was placed in a wetlands area south of the scrubgrass region of the White River National Wildlife Refuge. This area was chosen because its logging history is known and because it has been designated a "primitive area" that is to remain in its natural condition.

II. THE FIELD UNIT

The field unit consists of two separate functional groups: the timing and power assembly and the data-collecting and -recording path. Figure 1 is a block diagram of the field unit. The timing and power assembly--which comprises the clock, control logic, and power supply--provides the timing signals and operating power for the data path. The data path includes the following elements: sensors and signal conditioners, multiplexer-converter, encoder, and recorder.

Every 6 hr, data on temperature, humidity, liquid level, and wind are collected, processed, and recorded. This 6-hr cycle provides samples at representative times throughout the day. Shorter cycles, while providing more samples per day, would reduce the number of days that could be recorded on a given length of tape. Because of the likelihood that the test site would be under water for long periods of time, it was desirable to get as many representative recordings per day for as many days as possible without the need for changing tapes. A 90-day period was considered to be sufficient, and the 6-hr cycle provided this number of days on a standard audio tape cassette.

To minimize power consumption during this long period, low-power devices are used wherever possible. In addition, power is provided to the data path only during the 28 sec required to collect data every 6 hr. During this active period, power consumption is approximately 5 W. With the power to the data path turned off, the power consumption during the standby state is only 36 mW.

Clock and Control Logic

The Control Logic printed-circuit card is the master timekeeper of the system and generates all signals necessary to control the data path.

Figure 2 is a schematic diagram of the card. Because this card is the timekeeper, it must have power at all times; hence, low-power CMOS integrated circuits are used throughout the card. The Control Logic generates four major boolean terms: Flag, BTO, BT1L, and SC. Figure 3 is a timing chart. Flag is generated every 6 hr to enable the data path by turning on the power supplies. After a 21.25-sec warm-up period, BTO turns on the tape. In 3.5 sec, the signal SC starts the actual data-collecting and -recording sequence, which takes approximately 0.5 sec. At the end of data recording, a follow-up pattern is recorded until the end of BTO. Flag is then reset.

The heart of the Control Logic card is a series-divide configuration containing two CD4020 counters, one CD4013 flip-flop, and one CD4018 counter to provide a total frequency division of 3,221,225,472. A frequency of 149.131 kHz from a crystal-controlled oscillator (Figure 4) is applied to the first CD4020 counter at pin 10, which is the clock input. The last stage of the counter is connected to the clock input of the second CD4020. Because a CD4020 is a 14-stage binary counter with each stage (except the second and third) pinned out, the two connected CD4020s can be considered as a 28-bit register starting with the first stage of the first counter as least-significant bit 2^0 and ending with the last stage of the second counter as most-significant bit 2^{27}. Table I shows the relationship between frequency and the bit weight of the binary word. The table also shows the pin number of each stage.

The frequency of the 2^{27} bit corresponds to a pulse every 30 min. This bit is connected to the clock input of the CD4013, a D-type flip-flop that divides the frequency by two, giving one pulse every hour. The $\overline{Q}$ of

this flip-flop is connected to the input of the CD4018, which is a Johnson counter that divides the 1-hr pulse by six. This division causes the output of the CD4018 to go high every 6 hr.

TABLE I

Output Frequency vs. Bit Weight for Control Logic Register

Output	Bit	Frequency (Hz)	Pin
		First Counter	
Q_1	2^0	7.45655×10^4	9
Q_2	2^1	3.72828×10^4	-
Q_3	2^2	1.86414×10^4	-
Q_4	2^3	9.32069×10^3	7
Q_5	2^4	4.66034×10^3	5
Q_6	2^5	2.33017×10^3	4
Q_7	2^6	1.16509×10^3	6
Q_8	2^7	5.82543×10^2	13
Q_9	2^8	2.91271×10^2	12
Q_{10}	2^9	1.45636×10^2	14
Q_{11}	2^{10}	7.28179×10	15
Q_{12}	2^{11}	3.64089×10	1
Q_{13}	2^{12}	1.82044×10	2
Q_{14}	2^{13}	9.10223	3
		Second Counter	
Q_1	2^{14}	4.55111	9
Q_2	2^{15}	2.27556	-
Q_3	2^{16}	1.13778	-
Q_4	2^{17}	5.68890×10^{-1}	7
Q_5	2^{18}	2.84445×10^{-1}	5
Q_6	2^{19}	1.42222×10^{-1}	4

TABLE I--Continued

Output	Bit	Frequency (Hz)	Pin
Q_7	2^{20}	7.11112×10^{-2}	6
Q_8	2^{21}	3.55556×10^{-2}	13
Q_9	2^{22}	1.77778×10^{-2}	12
Q_{10}	2^{23}	8.88890×10^{-3}	14
Q_{11}	2^{24}	4.44445×10^{-3}	15
Q_{12}	2^{25}	2.22222×10^{-3}	1
Q_{13}	2^{26}	1.11111×10^{-3}	2
Q_{14}	2^{27}	5.55556×10^{-4}	3

The output of the CD4018 is connected to the clock input of a second CD4013 flip-flop. Because the D input of this flip-flop is connected high, a one is loaded into it every 6 hr by the positive-going transition of the output of the CD4018. The output of this flip-flop is the boolean term Flag, which activates the data path. The reset input of the CD4013 flip-flop is connected to the 2^{22} bit of the second CD4020, which resets Flag after 28 sec.

Eight miniature switches are incorporated into the printed-circuit card to permit manual control of the logic for testing and for setting the time of day for the first data recording. Subsequent recordings are made on the 6-hr cycle. The time is set by using the jam inputs on the CD4018 and the set and reset inputs on the first CD4013 flip-flop. Table II shows the relationship between the switch positions and the time until the first recording.

TABLE II

Switch Positions to Synchronize Recording Time with Real Time

Time	SW1	SW2	SW3	SW4
6.0	0	0	0	0
5.5	1	0	0	0
5.0	0	1	0	0
4.5	1	1	0	0
4.0	0	1	1	0
3.5	1	1	1	0
3.0	0	1	1	1
2.5	1	1	1	1
2.0	0	0	1	1
1.5	1	0	1	1
1.0	0	0	0	1
0.5	1	0	0	1

Once the switches have been positioned to set the time, SW5 is toggled once, jamming the count into the counters. Then SW7 is used to power an LED display for direct reading of the count. Switch SW6 sets the boolean term Flag to one and powers an LED to verify the state of Flag. Switch SW8 is used to reset the file counter on the Encoder card and has an LED to verify switch position.

The tape recorder is enabled by the boolean term BT0, which is defined by the equation

$$BT0 = (Flag)(2^{20})(2^{21}).$$

The boolean term BT1L, which enables the preamble, goes high simultaneously with BT0. The boolean term BT1L is generated by lengthening BT1 by one-

half of a full clock pulse (2^{19} bit). This lengthening is accomplished by loading BT1 into a one-bit-delay, the output of which is BT1S. The boolean term BT1S is then ORed with BT1, giving BT1L, which is defined by the expression

$$BT1L = BT1S + BT1,$$

where

$$BT1 = (BT0)(2^{19}).$$

The preamble, which is a series of ones and zeros recorded before the data, is generated by dividing the clock pulse by two. This division is accomplished by using a CD4013 flip-flop connected in the binary-divide mode. The flip-flop is controlled by the boolean term $\overline{BT1L}$ applied to its reset input. Thus, if $\overline{BT1L}$ is low, the flip-flop divides by two; if $\overline{BT1L}$ is high, the flip-flop is reset to a zero state.

The Multiplexer-Converter card is enabled by the boolean term SC, which is defined by the equation

$$SC = \overline{(BT1L)(\overline{BT1})}.$$

This boolean term is normally high and goes low to enable the Multiplexer-Converter card.

Power Supply

The power requirements of the data path are the typical digital and analog voltage levels of +5 V and ±15 V. These voltages are provided by a Stevens Arnold WC-series dc-to-dc converter (Figure 5). The voltage to this converter is controlled by Flag and is on, therefore, for only the 28 sec necessary to stabilize the systems and collect the data.

Power for the timing circuits and other components which must remain on at all times is provided by the MC1723 voltage regulator (Figure 6), which has an output of 5 V.

The voltage to operate both the dc-to-dc converter and the MC1723 is provided by a Eagle-Picher CF12V20 lead-acid battery. This 12-V, 20-A hr sealed battery is designed to have a very low internal leakage current. The low leakage current is necessary to prevent self-discharge at a rate faster than the 3 mA required during the standby condition.

Sensors and Signal Conditioners

The sensors and related signal conditioners record two measurements of temperature, humidity, and liquid level (one of water table and one of surface water), and one measurement of total wind.

The temperature sensors are Corning TSR5-1001J temperature-sensitive resistors with a well-defined temperature-resistance relationship,

$$R = 880.6 + 4.654T + 5.016 \times 10^{-3}T^2 + 5.783 \times 10^{-6}T^3,$$

in the temperature range of -20° C to +150° C. This is a temperature coefficient of approximately 5900 ppm/°C. The signal-conditioning

circuitry for the temperature measurements (Figure 7) provides an output of ±5 V for the temperature range of -20° C to +40° C, or a linear change of 1/6 V/°C.

Phys-Chemical Research Corp. PCRC-11 electro-humidity sensors are moisture-sensitive resistors usable in the range of 10% to 90% relative humidity with a resistance change from 4 MΩ to 1.8 kΩ. These sensors are used in a half bridge excited by a 1-V, 1-kHz signal that locates the center of the operating range at 60% RH. The bridge output is precision rectified, amplified, and filtered to provide a ±5 Vdc signal over the working range of the sensor (Figure 8).

The signal from each liquid-level sensor depends upon the variation of the bouyancy force with degree of submergance of a vertically oriented column. This change in bouyancy force is manifested by a change in the length of a spring resisting movement of the column. The change in length repositions the core of a Robinson-Halpern Model 225A-300 linear variable differential transformer (LVDT) attached to the column end of the spring. The signal-conditioning circuitry for the level sensors provides a 1-V, 1-kHz excitation voltage (Figure 9) for the LVDT, precision rectification of the output signals, and filtering of the rectified signals (Figure 10). The circuitry is designed to provide an output signal varying from -5 V to +5 V as the degree of submergance varies from 0 to 10 ft.

The total wind is determined by counting the number of revolutions of a Weather Measure Corp. W120S anemometer. A 16-bit binary counter (Figure 11) is used to keep track of these revolutions with the eight most-significant bits being used as a measure of the total wind. These eight bits allow for an average wind velocity of approximately 16 mph with a resolution of 1/16 mph.

Multiplexer-Converter

Upon receipt of the SC signal from the Control Logic card, the Multiplexer-Converter card (Figure 12) sequentially samples eight channels of analog data and converts the analog voltages into a serial, 8-bit, offset binary code, as shown in Table III. The circuitry of this card consists of a multiplexer, a sample-hold, an analog-to-digital (A-D) converter, a parallel-to-serial converter, and the necessary logic.

TABLE III

Input-Output Relationship for the A-D Converter

Analog Input Voltage	Offset Binary Output
+4.96	1111 1111
+4.37	1111 0000
+3.75	1110 0000
+2.50	1100 0000
0.00	1000 0000
-2.50	0100 0000
-3.75	0010 0000
-4.37	0001 0000
-4.96	0000 0001
-5.00	0000 0000

One of the eight input channels is selected by the AM3705 8-channel MOS analog multiplexer. Channel selection is controlled by a 3-bit binary code. The relationship between the channel selected and the binary code is shown in Table IV.

TABLE IV

Multiplexer Channel Selection

Logic Inputs				Channel
2^0	2^1	2^2	OE	
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

The output of the multiplexer is connected to the input of the LM0023C sample-hold. The sample-hold temporarily stores the voltage while the Datel AD89B converter is converting this voltage level into a binary word. After conversion is completed, the binary word is parallel loaded into the 8-bit shift register CD4021. Once loading is completed, the binary word is shifted out serially at a rate of 146 baud.

The control boolean signals are generated by the Multiplexer-Converter timer (a CD4020 counter) and various gates. The complement of the 2^2 bit from the Control Logic card is the signal that drives this timer, which can be considered as an extension of the first CD4020 counter on the Control Logic card. Table V shows the relationship between the output frequency of each stage of the timer and the binary bit weight of each stage.

TABLE V

Output Frequency vs. Bit Weight for Multiplexer-Converter Timer

Output	Bit	Frequency (Hz)	Pin
Q_1	2^3	9.32069×10^3	9
Q_2	2^4	4.66034×10^3	-
Q_3	2^5	2.33017×10^3	-
Q_4	2^6	1.16509×10^3	7
Q_5	2^7	5.82543×10^2	5
Q_6	2^8	2.91271×10^2	4
Q_7	2^9	1.45636×10^2	6
Q_8	2^{10}	7.28179×10	13
Q_9	2^{11}	3.64089×10	12
Q_{10}	2^{12}	1.82044×10	14
Q_{11}	2^{13}	9.10223	15
Q_{12}	2^{14}	4.55111	1
Q_{13}	2^{15}	2.27556	2
Q_{14}	2^{16}	1.13778	3

The 2^{16} bit of the timer is connected to its reset input. When this bit goes high, it resets all of the stages to zero. In addition, the complement of this bit is connected to the input of a latch made from two CD4011 NAND gates. The output of this latch is connected to the input of a CD4025 NOR gate. Therefore, when the 2^{16} bit goes high, the output of the latch will go high and disable the input signal to the timer. The latch is reset by the boolean term SC.

The binary selection code for the analog multiplexer AM3105 is generated by bits 2^9, 2^{10}, and 2^{11} on the timer. These bits are initially zero and count up to eight in a binary sequence.

The boolean term BCE is used to control the multiplexer, the sample-hold, and the A-D converter. This boolean term is defined by the equation

$$BCE = \overline{\overline{(2^{10} + 2^{11} + 2^{12})\ (2^{9})} + (2^{8}) + (2^{9})}.$$

The boolean term BLOD is used to parallel load the binary data from the A-D converter into a CD4021 shift register. This boolean term is defined by the equation

$$BLOD = \overline{(2^{10} + 2^{11} + 2^{12})(2^{9})}.$$

The clock pulses used to shift the binary data out of the CD4021 are from the 2^{9} bit of the timer. Hence, the data are shifted out at a rate of 146 baud in the format of NRZ binary code.

Figures 13 and 14 show the timing sequence for the system. The boolean term BCE goes high for 850 μsec. When BCE is high, the A-D converter is reset, the sample-hold is placed in the sample mode, and the multiplexer is enabled. A low state of BCE disables the output of the multiplexer, places the sample-hold in the hold mode, and starts the A-D converter. Approximately 200 μsec later, the conversion is complete and the binary data are ready for loading into the shift register.

When the boolean term BLOD is in a high state, the eight bits of data are parallel loaded into the shift register. However, because BLOD goes high simultaneously with the clock pulse, the binary data do not begin shifting out of the shift register until the next positive transition of the clock pulse. The data would be one-half of a clock pulse late if it

were not for the fact that the timer is started one-half of a clock pulse early. This is accomplished by the boolean term SC, which goes low one-half a clock pulse before the preamble ends.

Encoder

The Encoder card (Figure 15) converts the NRZ signal from the Multiplexer-Converter card and the preamble from the Control Logic card into a biphase signal. This biphase signal modulates the voltage-controlled oscillator (VCO), producing a frequency-shift-keyed (FSK) signal that is recorded on the tape. In addition, this card generates a 7-bit file number and provides an 8-bit, parallel-input digital data channel. These parallel signals are converted to NRZ format preceding the NRZ signal from the Multiplexer-Converter card. The Encoder card then provides logic to select this combined NRZ data or the preamble for processing into the biphase signal.

The sequence of operations starts on the rising edge of the boolean term BT0. When this edge occurs, the count in the file counter is increased by one. Next, the boolean term BT1L goes high, loading the count of the file counter into the first shift register. The high state of BT1L also loads any data on the parallel data channel into the second shift register. Simultaneously, the preamble is selected for recording. When the boolean term BT1L goes low, the preamble is ended, and the data contained in the shift registers are clocked out and gated to the biphase encoder. At the end of ten 8-bit data words, the shift registers contain all zeros, which are clocked out until the boolean term BT0 goes low.

The serial output from the Multiplexer-Converter card is connected to the serial input terminal of a CD4021 shift register. The output of this

register is connected to the serial input of another CD4021 shift register. Thus, the data from the Multiplexer-Converter card are serially clocked through both shift registers. The two clock inputs of the shift registers are connected together and are driven by the clock pulses generated by the Control Logic card. The output of the second CD4021 is ANDed with the boolean term BT1L. The AND gate is made from two CD4001 two-input NOR gates. When BT1L is high, the output of the second NOR gate (pin 4) is low, independent of the state of the data. The output of this gate is connected to one of the inputs of a third NOR gate, and the preamble is connected to the other input. Therefore, data or the preamble is selected as a function of the state of BT1L, because the preamble is always zero when BT1L is low. The output of this third NOR gate is inverted and connected to the data input terminal of the CD4037 biphase encoder.

The parallel-input enable terminals (pin 9) of the two CD4021 shift registers are connected together and to BT1L. A high state on the enable terminals loads the signals on the parallel-entry lines into the shift registers simultaneously. The eight parallel-entry lines from the first shift register are brought off the card, giving an 8-bit, parallel-input digital data channel. The first bit of the second shift register is connected low; the other seven bits are connected to the CD4024 counter. The zero from the first bit flags the decoding unit, enabling the unit to differentiate between the preamble and data by the occurrence of two consecutive zeros. The counter is reset by SW8 on the Control Logic card.

The biphase encoder is a CD4037. Clock is connected to the A input, and the complement of clock is connected to the B input. The NRZ data from the CD4001 NOR gate are connected to the C input. Therefore, every half of a clock period, the output signal on D is the complement of the input

signal on C. This is the format for biphase-encoded data. The D output is connected to the control terminal of an electronic switch (CD4016) to control the frequency of the VCO (8038).

The input terminal of the electronic switch is connected to a voltage-divider network consisting of two serial resistors connected across the +5-V and -15-V power supplies. The resistor values are selected so that the input voltage to the electronic switch is always positive (about 2 V). A diode is used to protect the switch in case the +5-V line is lost. The output signal of the switch is connected through a resistor to the input control terminal of the VCO. In addition, a reference voltage generated by a resistor network inside the 8038 chip is connected to the VCO input terminal.

When the D output of the CD4037 is high (binary one), the switch is closed, applying the voltage from the divider network to the input of the VCO. Because the reference voltage is higher than the voltage at the output of the switch, current flows through the coupling resistor, reducing the voltage on the VCO control input terminal. This increases the frequency of the VCO to about 3 kHz. When the D output is low (binary zero), the switch is open, and no current flows through the coupling resistor. The VCO control terminal then rises to the reference voltage level, lowering the VCO frequency to about 2.1 kHz. Thus, the signal out of the VCO is an FSK signal. The sinusoidal output is recorded by the field-unit tape recorder.

Recorder

The recorder is a Phi Deck Model 1 audio cassette recorder deck. This recorder deck is designed for electronic switching of the tape handling

functions, which facilitates remote operation of the recoder. No electronics were provided with the deck, so a record amplifier (the 741 on the Encoder card, Figure 15) and a bias oscillator (Figure 16) are used. Also, power switches and control logic (Figure 17) are required to operate the recorder with the control signal BTO.

III. THE LABORATORY UNIT

After the audio tape cassette containing the information about the measured variables has been returned from field, it is necessary to reconstruct the original data words. This manipulation involves demodulating the recorded FSK signal to obtain the biphase-coded signal, which is then translated to recover the NRZ signal and clock. A microcomputer is used to read and interpret the NRZ signal and produce a print out of the original data. Figure 18 is a block diagram of the decoding process.

Cassette Tape Reader

The cassette tape reader used for playback of the recorded tape is the complement of the tape recorder incorporated in the field unit. It also is a Phi Deck Model 1 audio cassette recorder deck. The electronic switching feature of the deck allows the microcomputer to control the tape transport.

FSK-Biphase Demodulator

The Demodulator card converts the recorded FSK signal into a binary biphase format. A binary one corresponds to a high frequency (about 3 kHz), and a binary zero corresponds to a low frequency (2.1 kHz). Thus, the Demodulator card recovers the biphase signal originally encoded by the field unit. Figure 19 is a circuit diagram of the Demodulator card.

The FSK signal is amplified and offset to ensure that the signal is always positive and approaches a level of 5 V. This signal is applied to the input of an MC3302 voltage comparator. This comparator, which has a hysteresis window of 1 V centered at 2.5 V, is used to remove any AM from

the signal. The output from the comparator is connected to the input of a CD4046 phase-locked loop (PLL), consisting of two phase comparators, a VCO, and a buffer amplifier.

Phase comparator II of the PLL is used to demodulate the FSK signal because it is an edge-controlled comparator, which makes it independent of the duty cycle of the input signal. In addition, the phase difference between the VCO and the input signal is very close to zero for this type of comparator. Two simple low-pass filters are connected in series between the output of phase comparator II and the input of the VCO of the PLL to provide maximum suppression of the fundamental input frequency. Because of the nonlinearity of the internal amplifier of the PLL, an external 741 is used as a voltage follower. The output signal of this amplifier is filtered by a passive low-pass filter and applied to the input of a second MC3302 voltage comparator. The output of this comparator is the recovered biphase signal.

Also incorporated on the Demodulator card is a circuit to detect whether the PLL is locked or unlocked. This circuit requires that the PLL be locked for a finite period of time before a lock signal is generated. Binary one or zero outputs from the lock detector correspond to locked or unlocked conditions, respectively. The state of the PLL is determined by NORing the output of phase comparator I and the phase-pulse output of phase comparator II. When the PLL is locked, the output of the NOR gate will be a binary zero. A zero output will discharge the capacitor through the resistor to ground, allowing the following gate to switch, after a given period of time, producing the lock detector signal. A one output from the NOR gate will instantaneously charge the capacitor through the

diode. Therefore, there will be a time delay in the detection of lock-up, but there will be no time delay when the PLL drops out of lock. The other NOR gates are used to buffer and shape the output signal.

Biphase-NRZ Translator

The Translator card (Figure 20) converts the biphase signal from the Demodulator card into the NRZ format. It also synthesizes the 146-Hz clock signal. Figure 21 shows the format for the encoded biphase signal with the clock pulses. The frequency of the biphase signal is always 73 or 146 Hz. The 73-Hz signal implies a series of alternate ones and zeros; the 146-Hz signal implies a constant one or zero.

The clock signal is synthesized by doubling the frequency of the biphase signal, giving 146 or 292 Hz. If the resulting frequency is 292 Hz, every other pulse is deleted; if the frequency is 146 Hz, no pulses are deleted. The frequency is doubled by the use of two 74123 monostables and a 7400 two-input NAND gate. One monostable is triggered on the rising edge of the biphase signal, while the other monostable is triggered on the falling edge of the biphase signal. The $\overline{Q}$ outputs of these monostables are NANDed together. The pulse widths of both monostables are small compared with the pulse width of the input signal. The signal at the output of the NAND gate is, therefore, double the frequency of the input signal. This frequency-doubled signal is NANDed with the $\overline{Q}$ output of a third 74123 monostable. If the $\overline{Q}$ output of the third monostable is high, a pulse from the frequency-doubled circuit will trigger the monostable, and the $\overline{Q}$ output will go low. The pulse width of the third monostable is three-fourths of the period of the 146-Hz signal. Hence, once the third monostable is triggered, the $\overline{Q}$ output will remain low long enough to delete every other

pulse when the frequency is 292 Hz but pass all pulses when the frequency is 146 Hz. Therefore, the signal at the output of the NAND gate is the synthesized clock signal.

Because NRZ is encoded into biphase by complementing the NRZ data every one-half of a clock period, the method used to decode biphase is to use the synthesized clock to load the biphase data into a 7474 flip-flop, the output of which is the recovered NRZ data. This method is shown in Figure 21. The output of this flip-flop is loaded into a second 7474 flip-flop that also is controlled by the synthesized clock; but, in this case, the clock is enabled by the lock detector, which also presets the flip-flop into a one state before the start of the data sequence.

Microcomputer

Once the NRZ and clock signals have been recovered, an MOS Technology KIM-1 microcomputer, enhanced with additional memory and peripherial equipment, is used to reconstruct the original binary data words. This computer then implements the algorithms required to convert these binary data words into meaningful engineering units, such as temperature in degrees Celsius, percentage of relative humidity, and water level in feet. Figures 22 and 23 are block diagrams for these decoding and conversion algorithms. After conversion to engineering units, the data are printed using a Hycom model DC-2106A 21-column line printer.

IV. RESULTS AND DISCUSSION

The field unit was in service in a wetlands area of the White River National Wildlife Refuge from January 31, 1976, until May 4, 1977. Figure 24 is a photograph of the installation, with the instrumentation package (Figure 25), the power supply (Figure 26), and the sensors secured to a large tree. This tree was located approximately 250 yd from the normal bank of the White River. As shown in Figure 24, the two ventilated shelters containing the humidity and temperature sensors are located approximately 8 ft and 22 ft above the forest floor. At the 10-ft level is the anemometer. The vertical pipe to the left of the tree contains the surface water sensor. Farther to the left and barely protruding from the ground is a pipe that contains the water table sensor. The tube running from the pipe and up the tree vents the pipe to atmospheric pressure above flood level and contains wires connecting the sensor with the instrumentation package.

Table VI is a typed reproduction of the microcomputer display of the data collected at this site on two different days. The headings and the time of day have been added. The Julian date of 6061 indicates that the first block of data was taken March 1, 1976. The second block of data was taken July 15, 1976.

The measurement of wind is an average of the wind speed at 10 feet above the forest floor. The anemometer used gave a pulse for each revolution. These pulses were counted for the entire 6-hr period. At the end of each period, the eight most-significant bits of the counter were read and recorded. The least-significant bit of these eight represents an average wind velocity of 1/4 mph. The "Wind" column of Table VI shows the result was zero on these two dates, which indicates that the average wind

was less than 1/4 mph. This result verifies observations made during visits to the site that the air was very still on the forest floor and that the anemometer was not turning even though leaves were moving in the treetops. It was impossible to get the anemometer to tree-top height.

TABLE VI

Typical Computer Printout

Date	Time	Wind (mph)	Relative Humidity (%)		Liquid Level (ft)		Temperature (^{o}C)	
			1	2	1	2	1	2
6061	3 AM	0	61	59	2.4	-5.5	21	24
	9 AM	0	62	59	2.8	-5.5	23	24
	3 PM	0	59	57	3.0	-5.5	25	19
	9 PM	0	59	57	2.9	-5.4	28	25
6196	3 AM	0	81	79	0.0	-8.5	18	20
	9 AM	0	70	68	0.0	-8.5	19	18
	3 PM	0	67	65	0.0	-8.5	28	26
	9 PM	0	73	56	0.0	-8.6	20	20

The relative humidity sensors located at the two levels showed no appreciable difference and generally ranged from 50 to 80 percent with a slightly higher humidity at the lower level (sensor 1 in Table VI).

Liquid level measurement 1 in the table is for water above the surface. As shown in Table VI, there were flooding conditions on March 1, with surface water approximately 3 ft deep that day. The water table was 5.5 ft below the surface. The July reading indicates that there was no flooding and that the water table had dropped by 3 ft. This indicates a possible connection between the river level and the water table; however, during the period of data collection, no correlation could be found, which

invalidates the original premise that historical records of river level could be used to obtain the water table history. Analysis of the soil samples taken while drilling the well for measurement of the water table showed that the particles constituting the soil were microscopic in nature, creating a matrix that is extremely impermeable. From this analysis it was predicted that there would be a very large time delay and extremely attenuated response of the water table to changes in the river level.

As with the humidities, the temperatures showed no significant differences at the two levels. In Table VI, measurement 1 is the upper level.

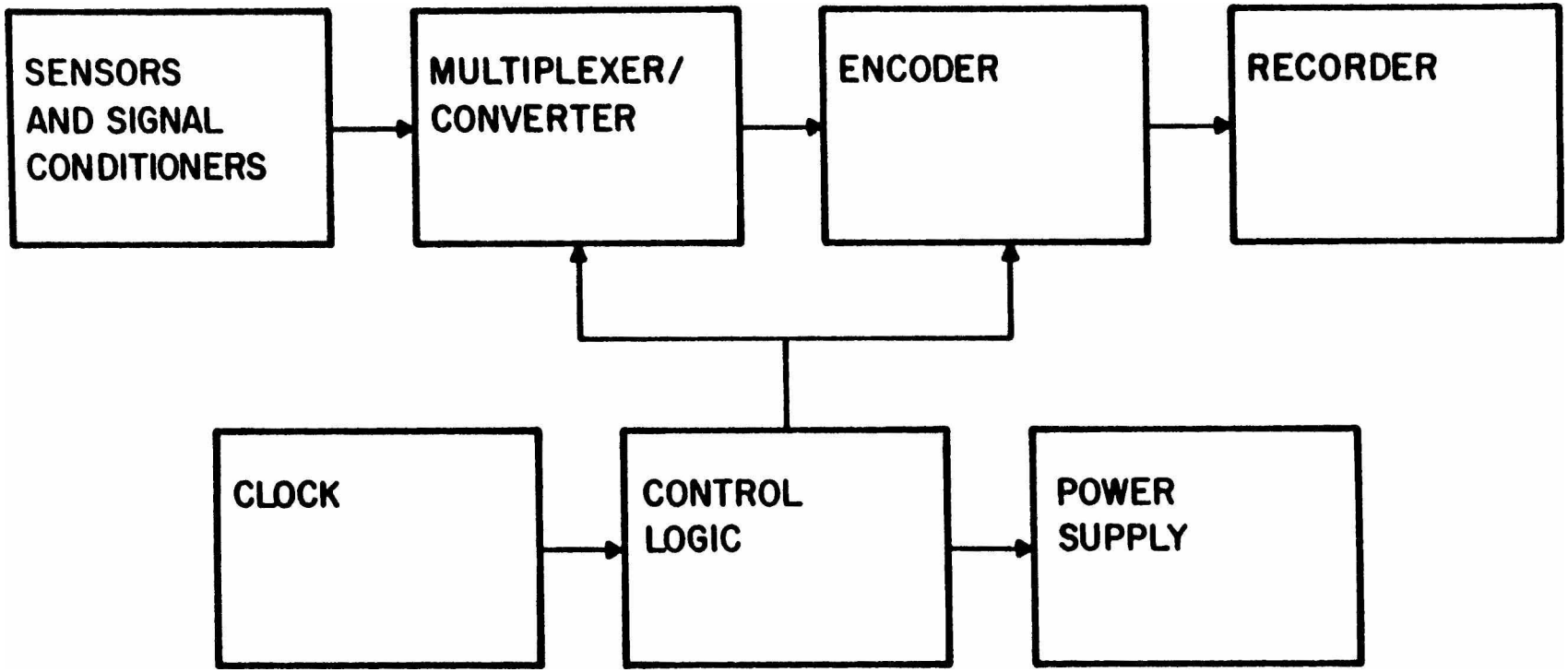

Fig. 1. Block diagram of field unit.

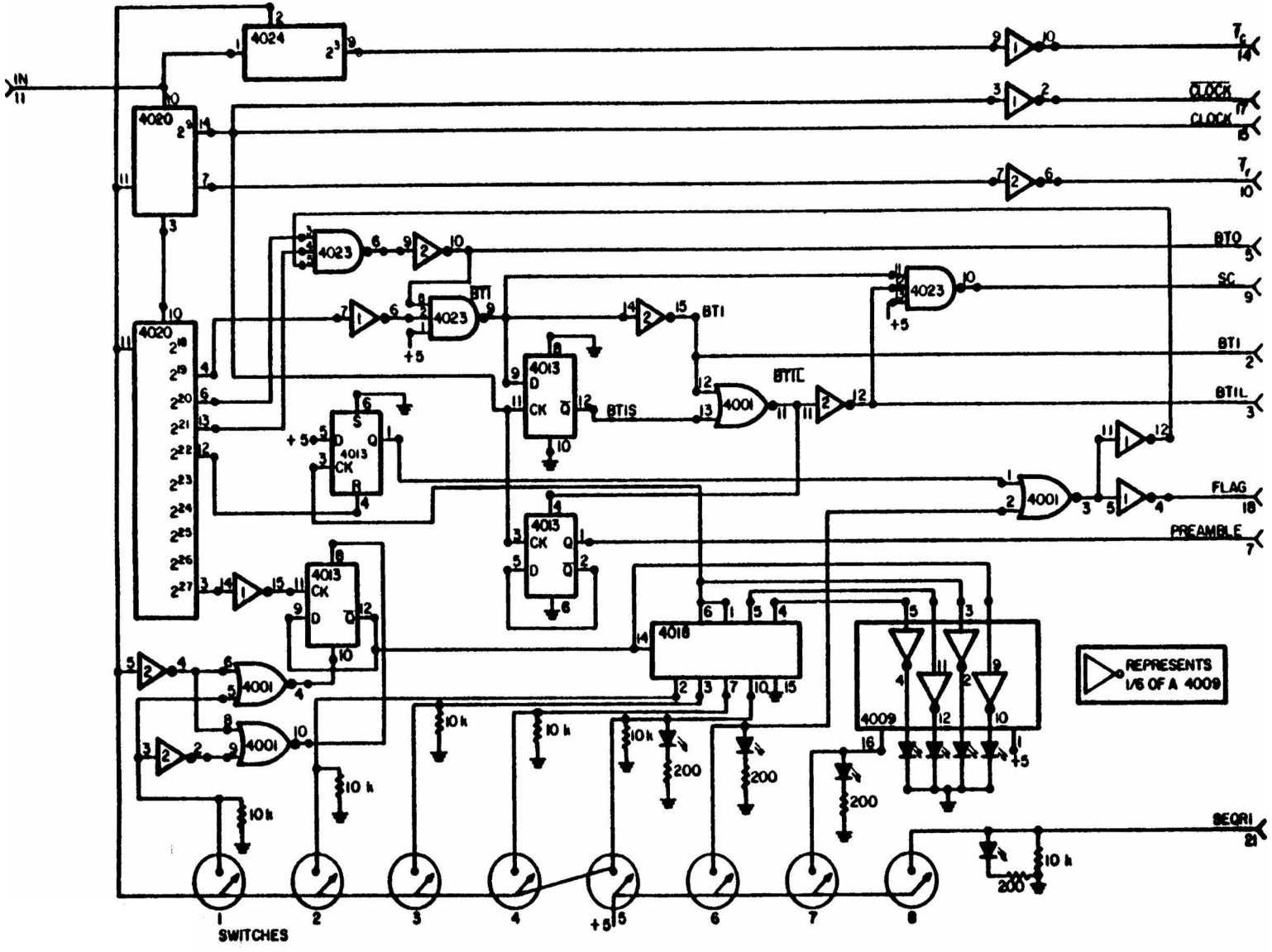

Fig. 2. Control Logic card circuit diagram.

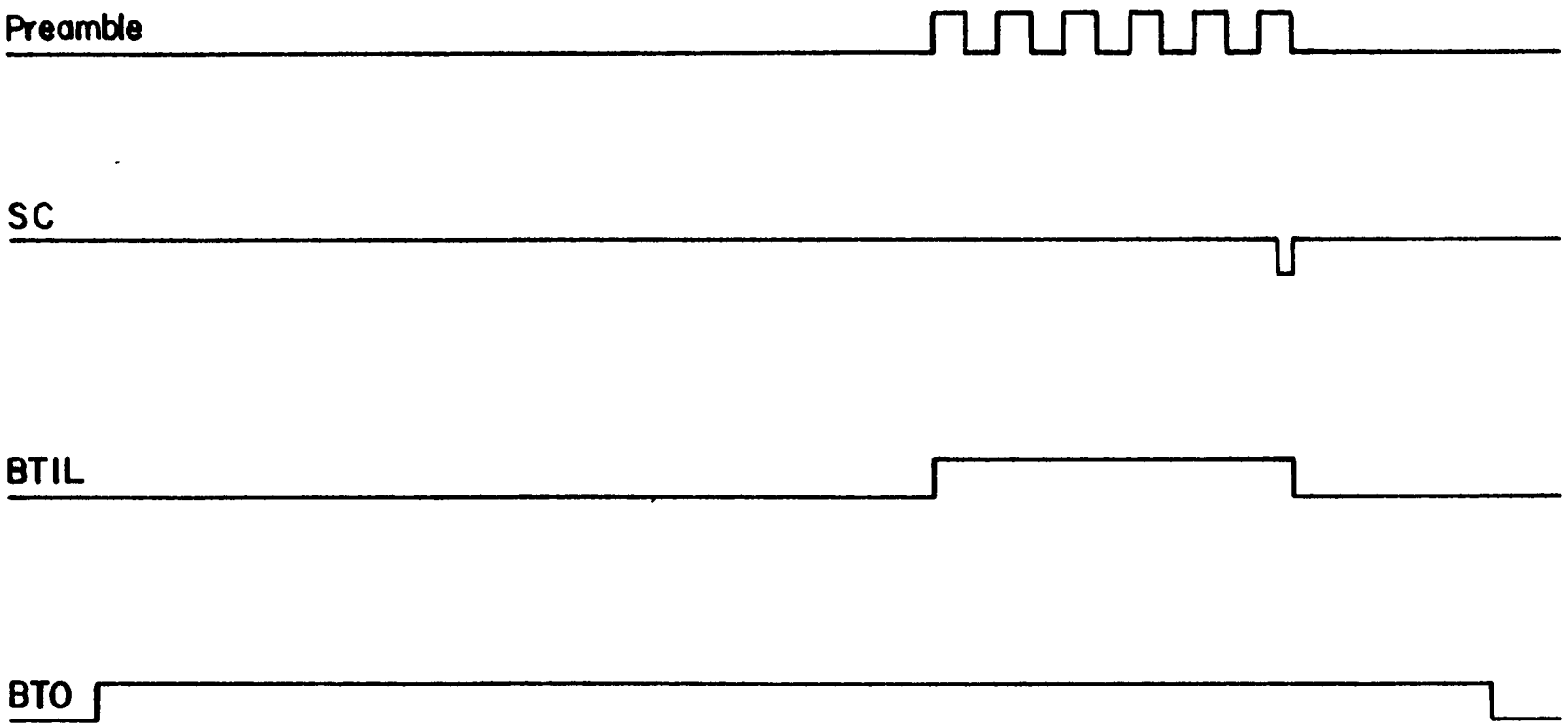

Fig. 3. Data path control-timing diagram.

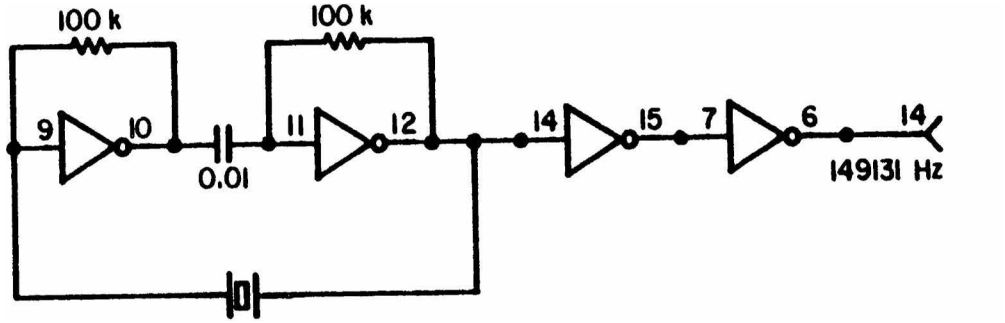

Fig. 4. Crystal-controlled clock oscillator.

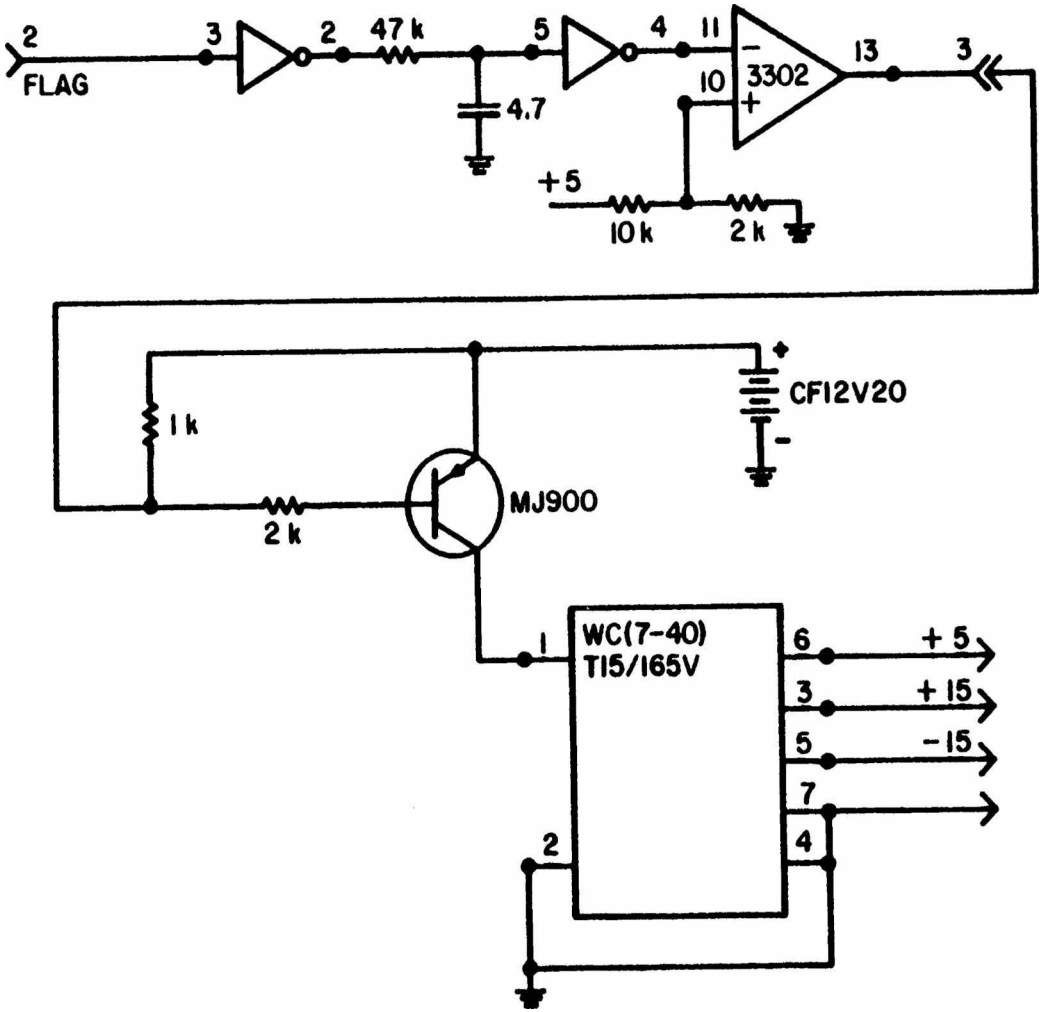

Fig. 5. Switched power supply.

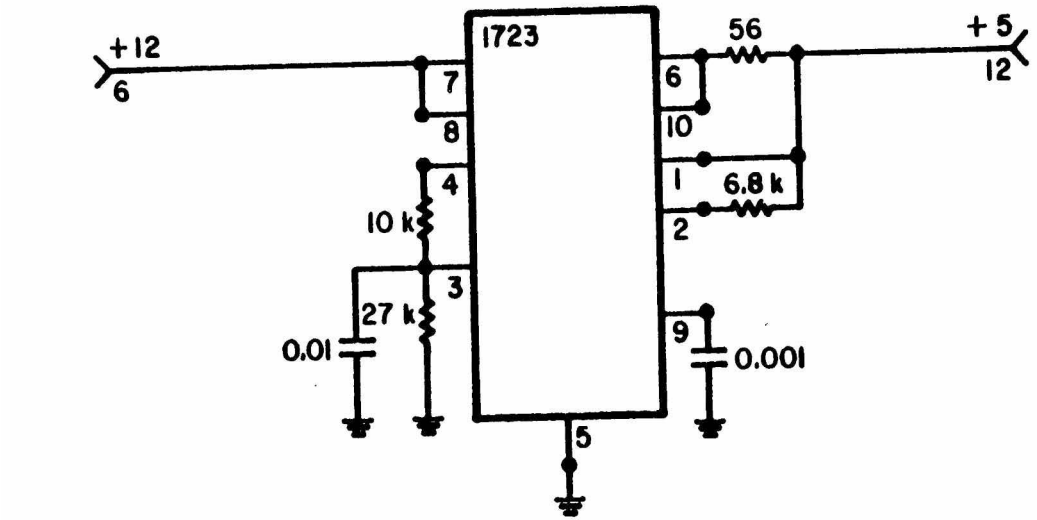

Fig. 6. Continuous power supply.

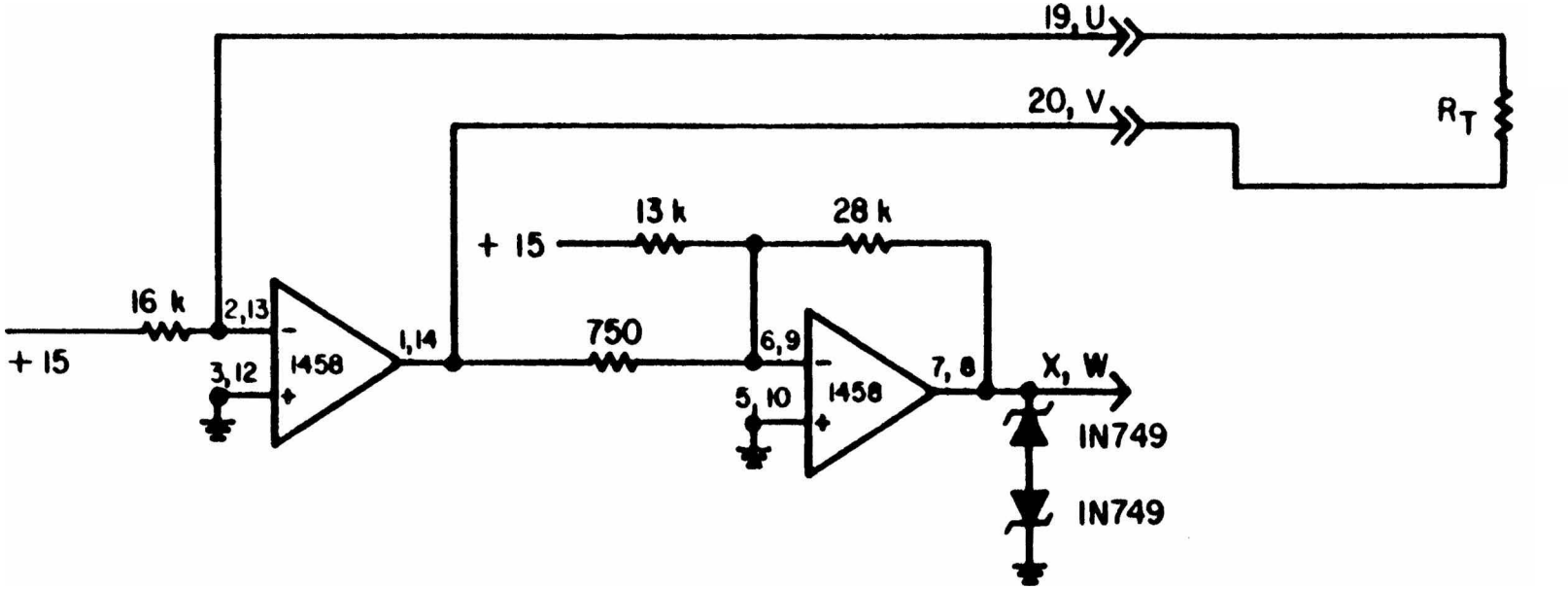

Fig. 7. Temperature measurement circuitry.

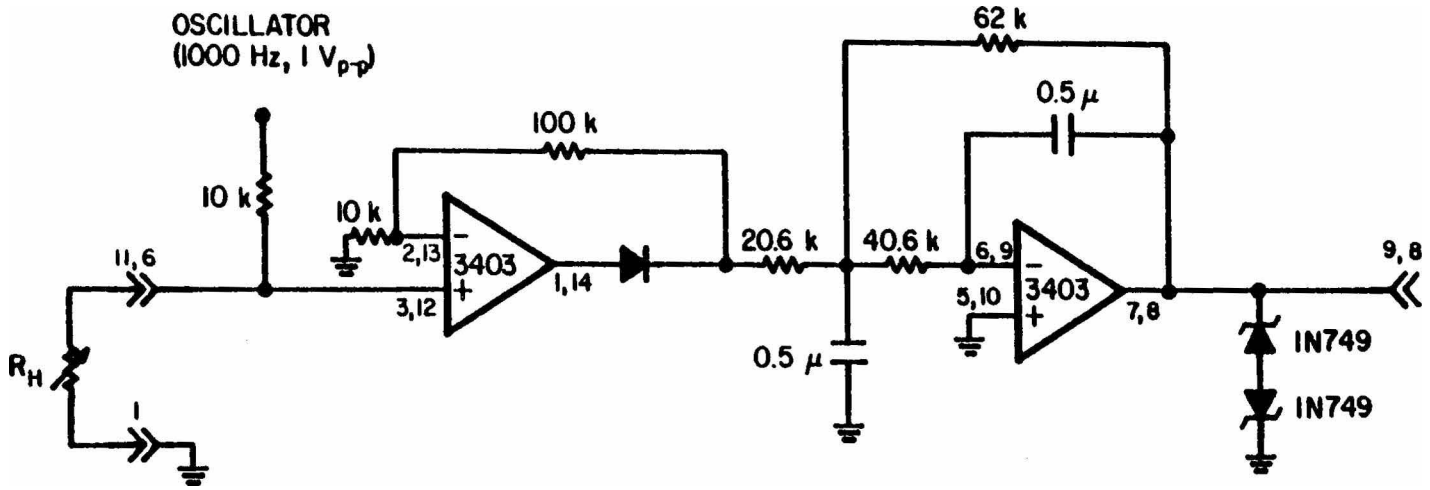

Fig. 8. Relative humidity measurement circuitry.

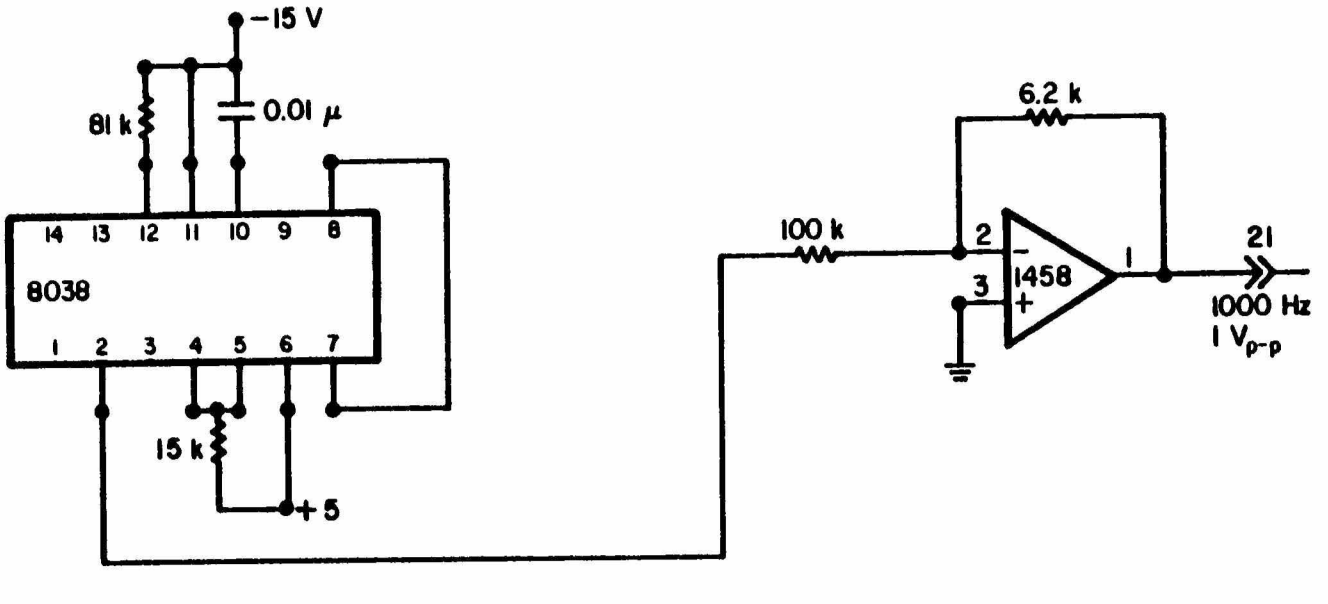

Fig. 9. 1 kHz oscillator.

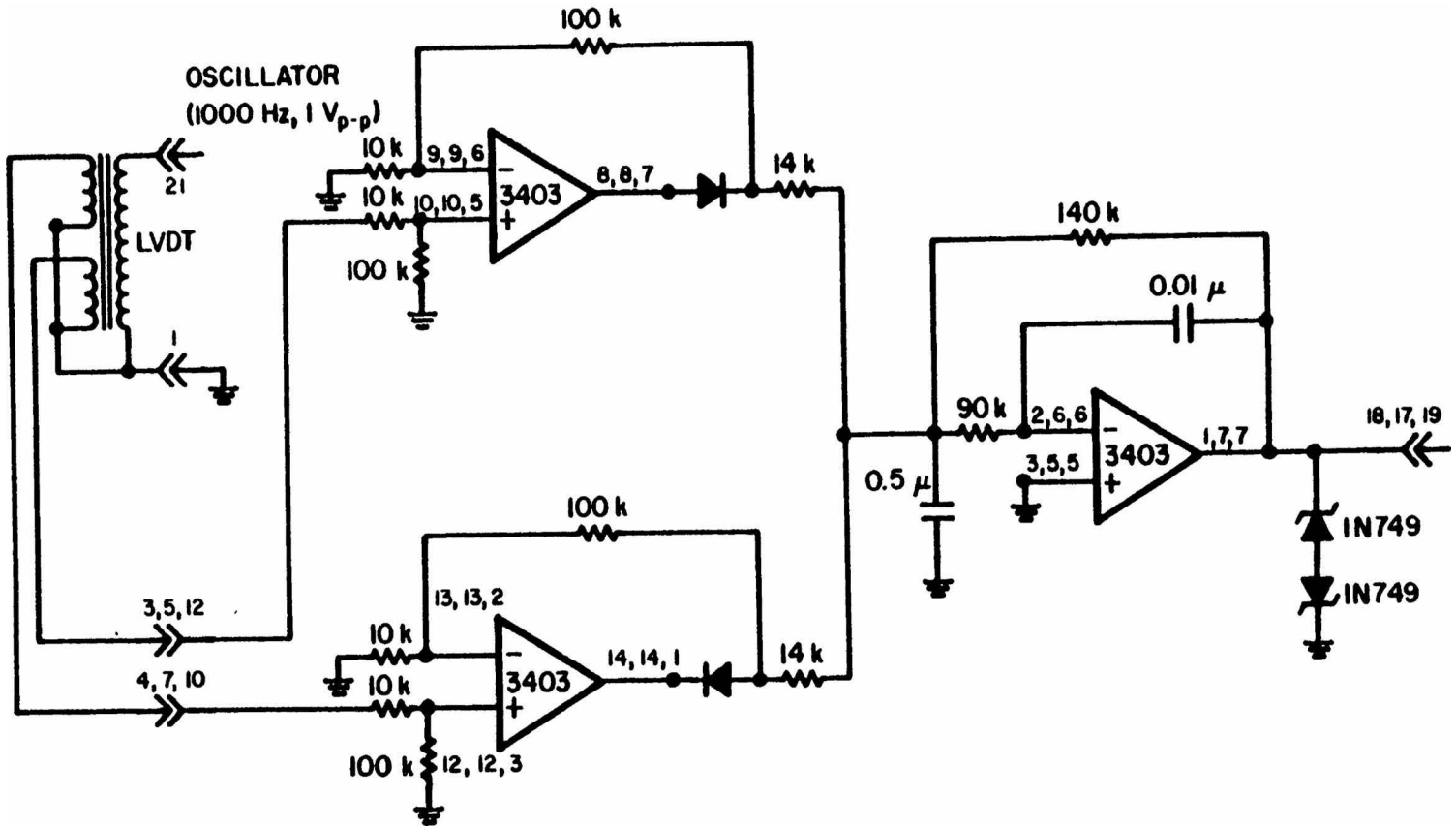

Fig. 10. Liquid level measurement circuitry.

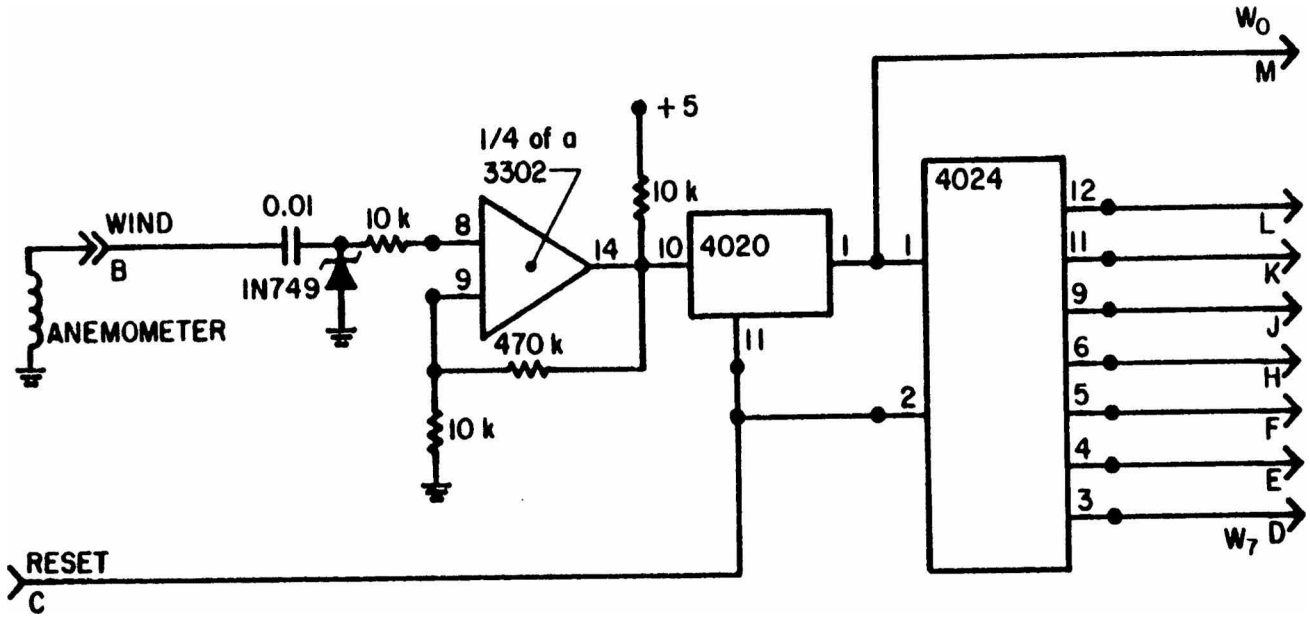

Fig. 11. Total wind measurement circuitry.

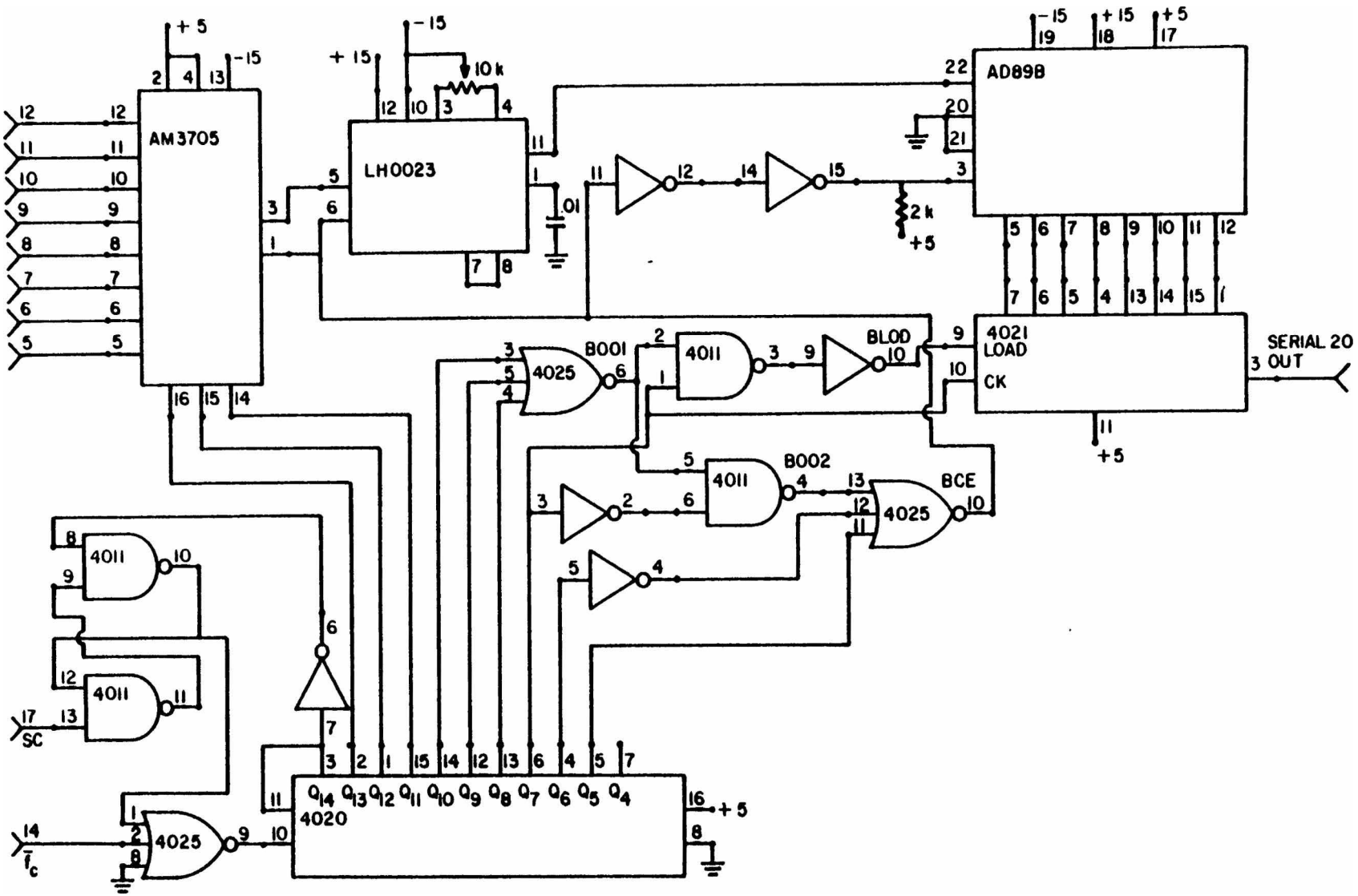

Fig. 12. Multiplexer-converter card circuit diagram.

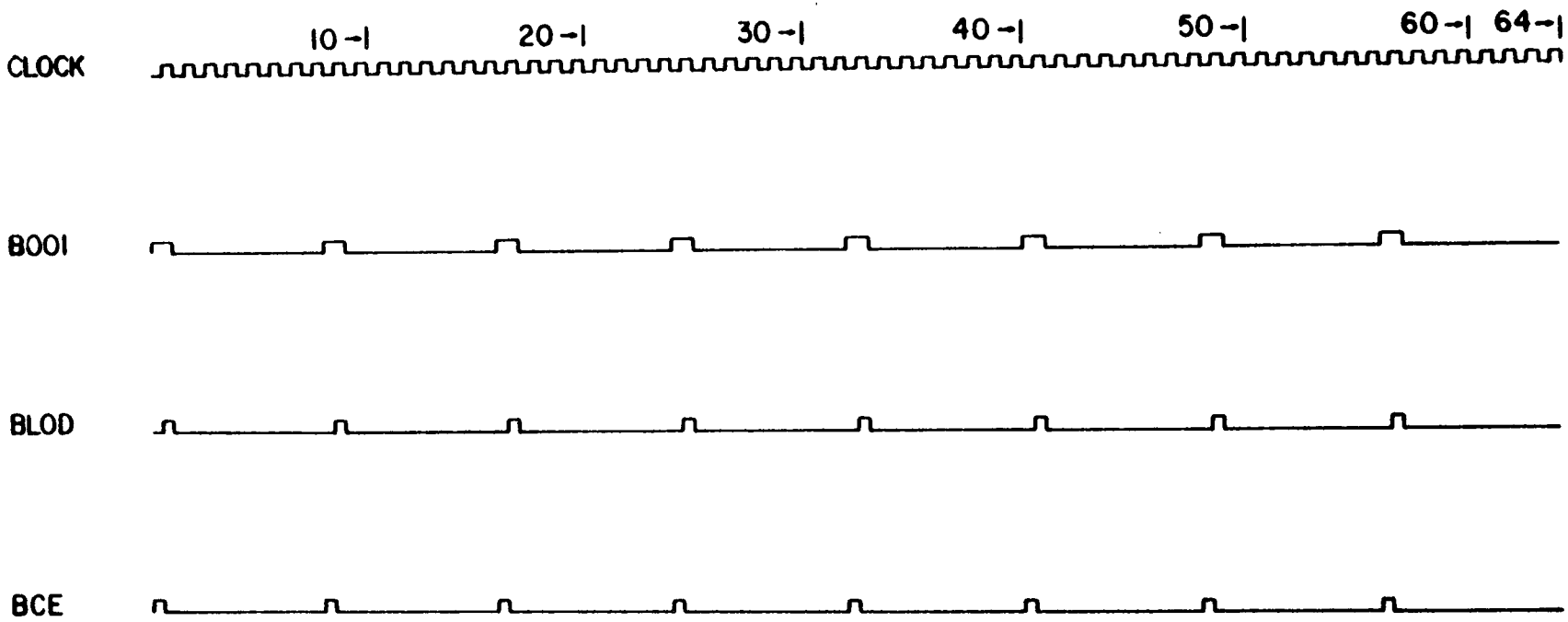

Fig. 13. Timing diagram for a complete sample-convert sequence.

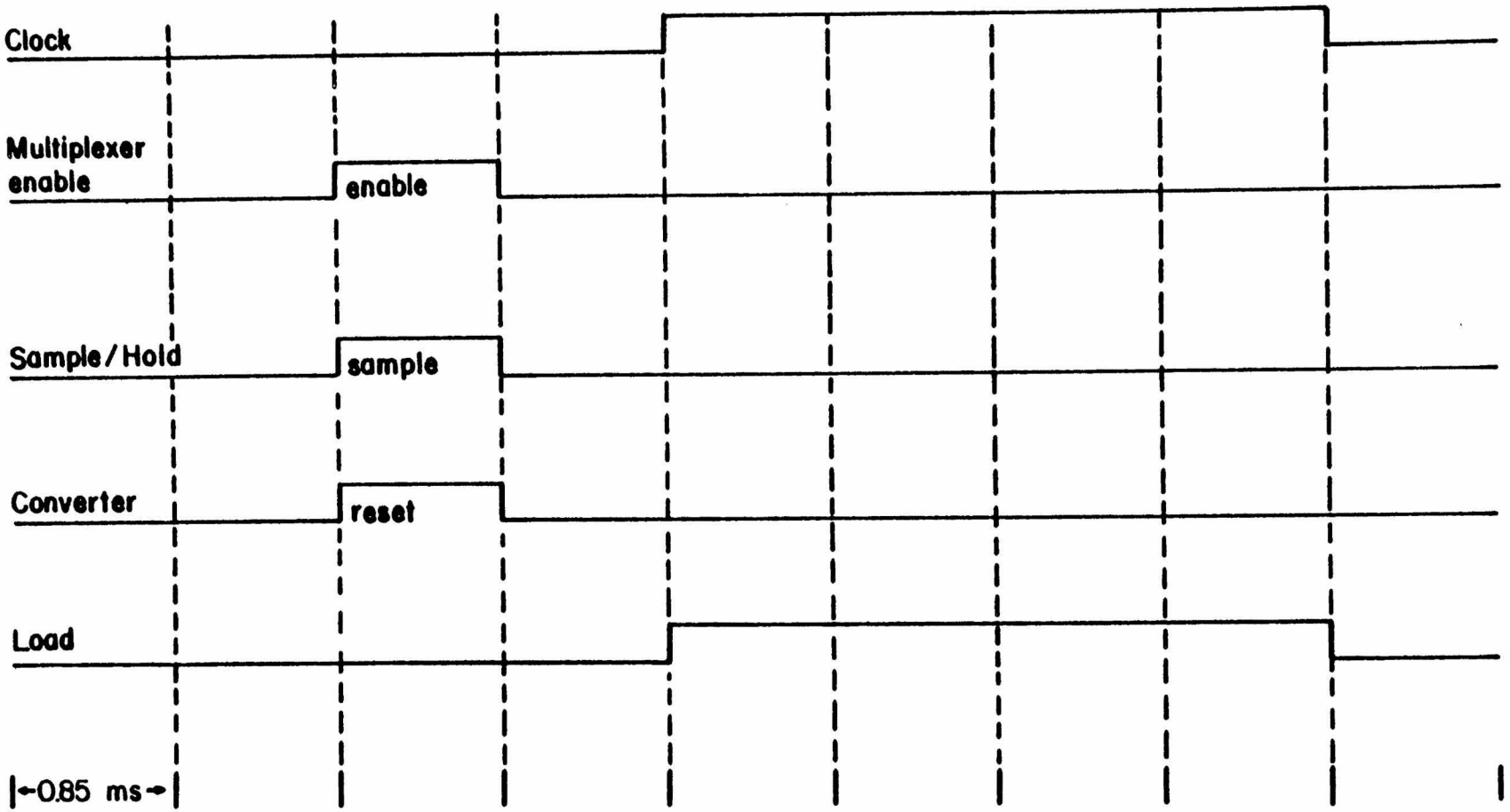

Fig. 14. Timing diagram for one clock cycle during sample-convert sequence.

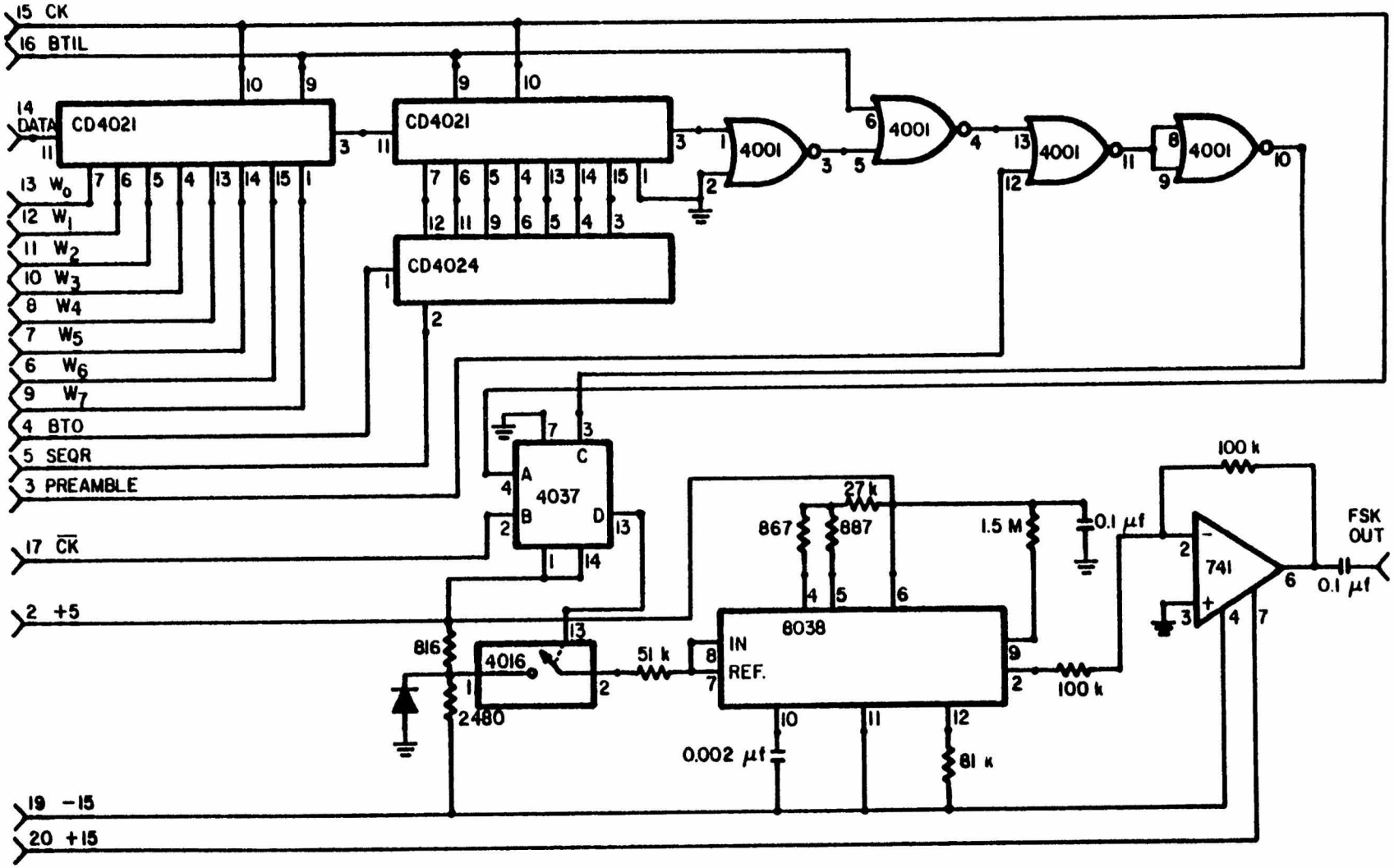

Fig. 15. Encoder card circuitry.

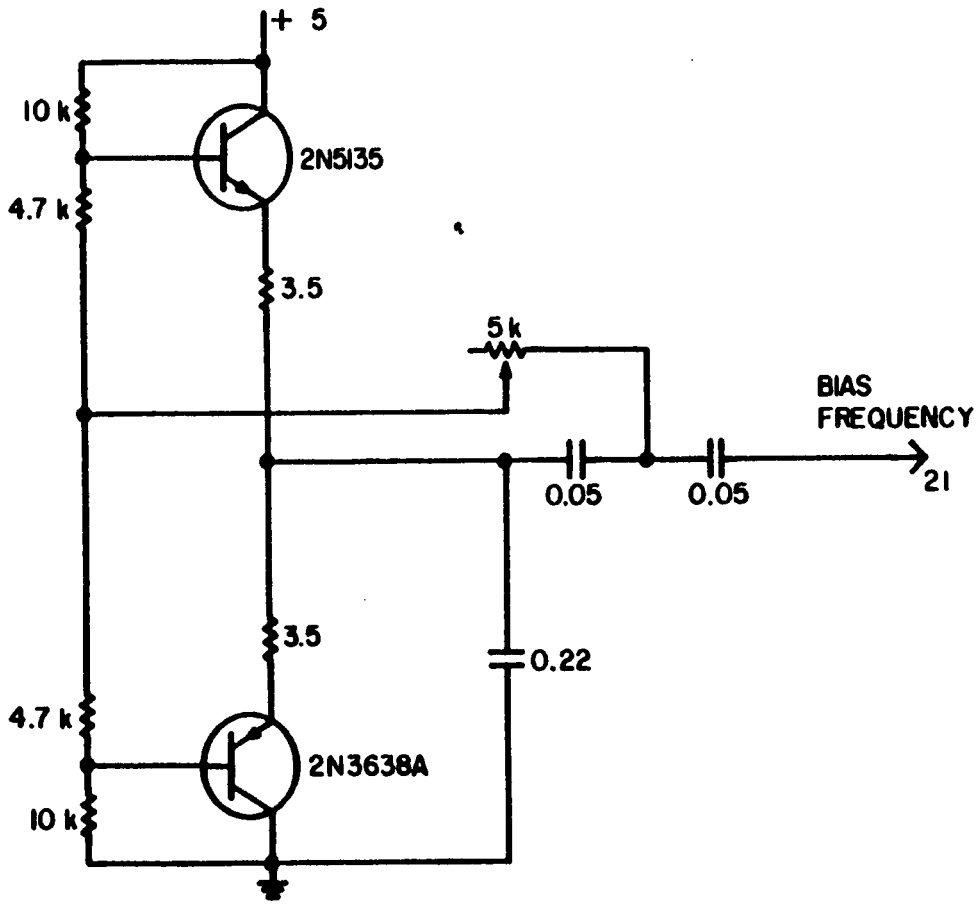

Fig. 16. Record bias oscillator.

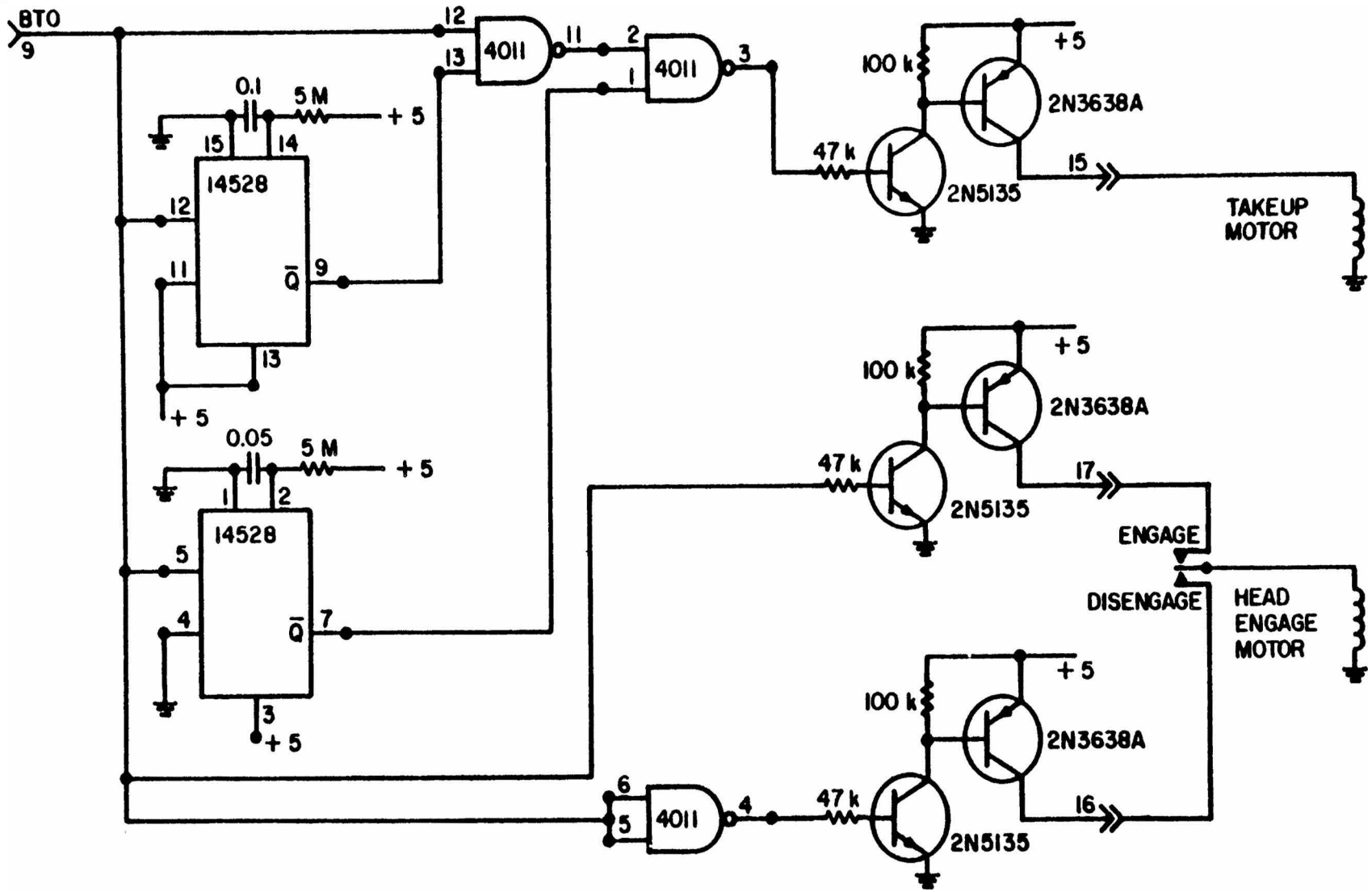

Fig. 17. Tape recorder motor-control circuitry.

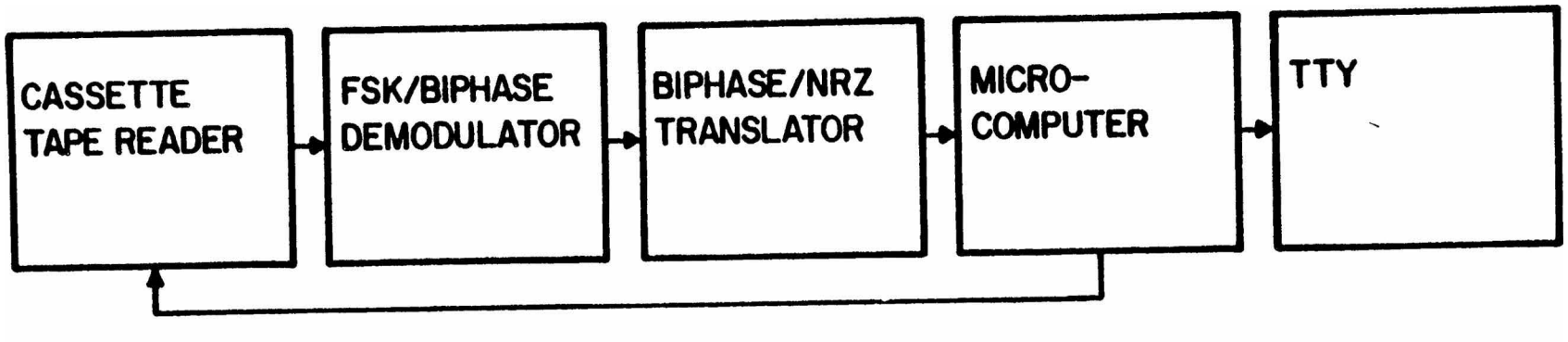

Fig. 18. Block diagram of laboratory unit.

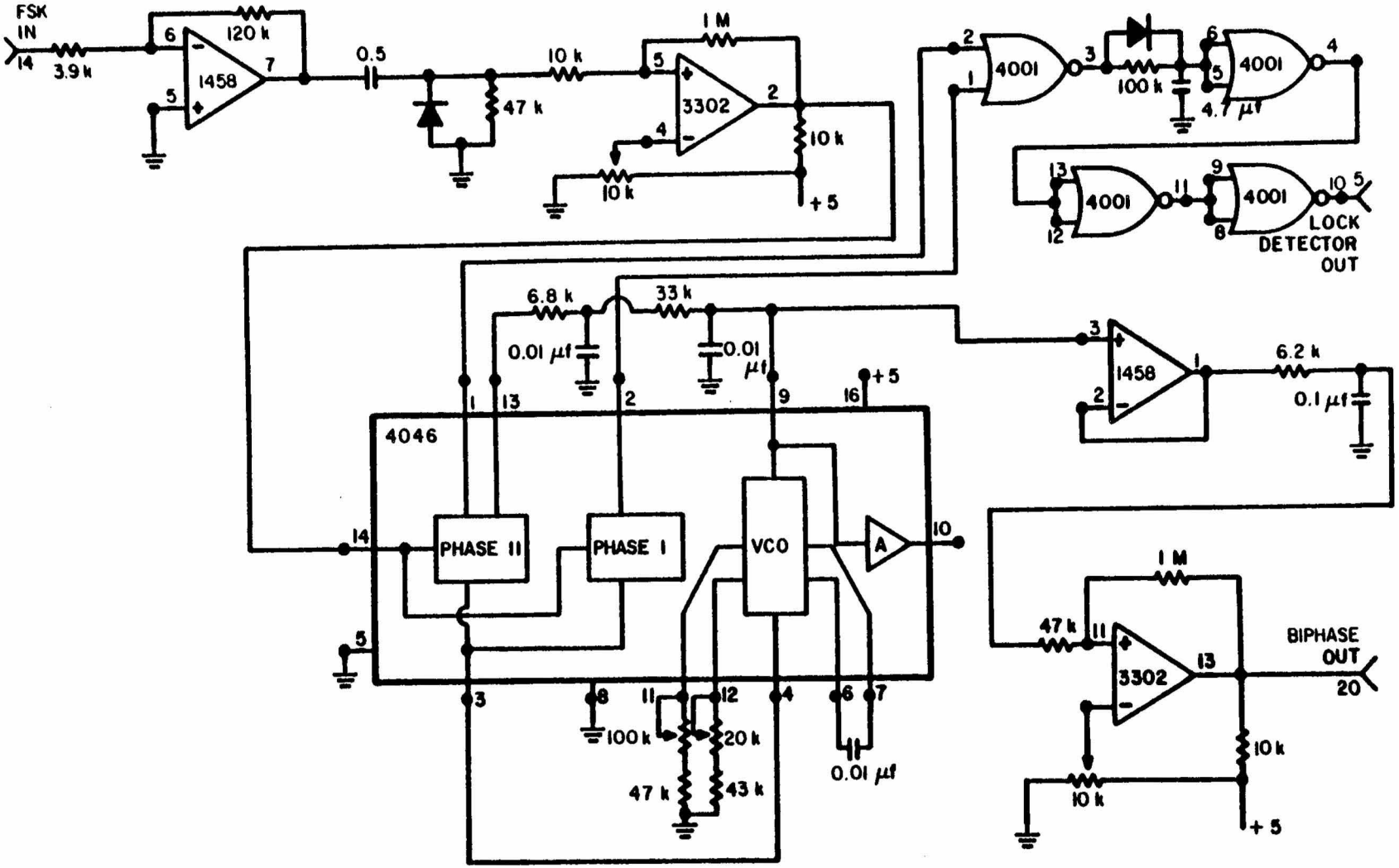

Fig. 19. Demodulator card circuit diagram.

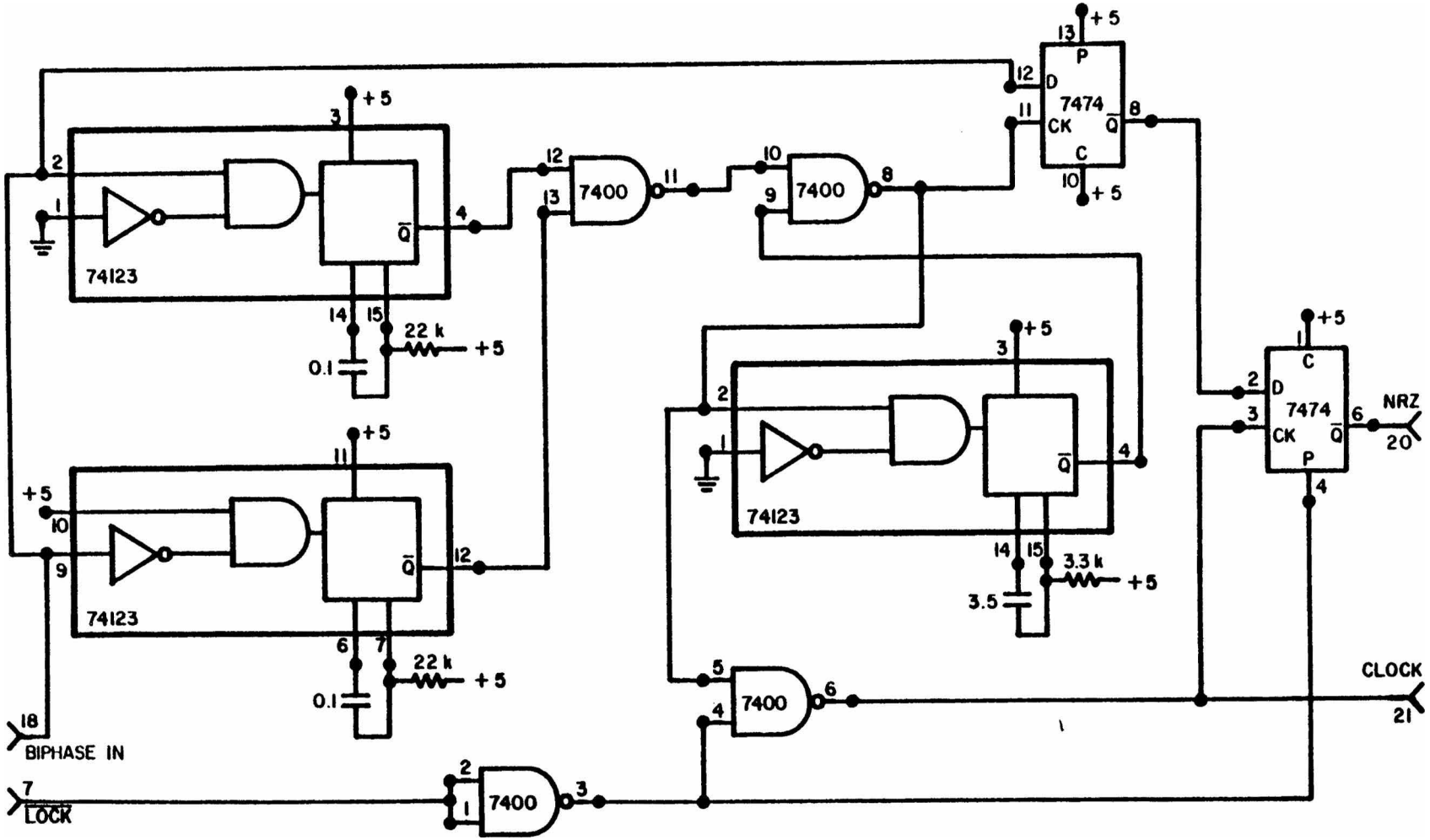

Fig. 20. Translator card circuit diagram.

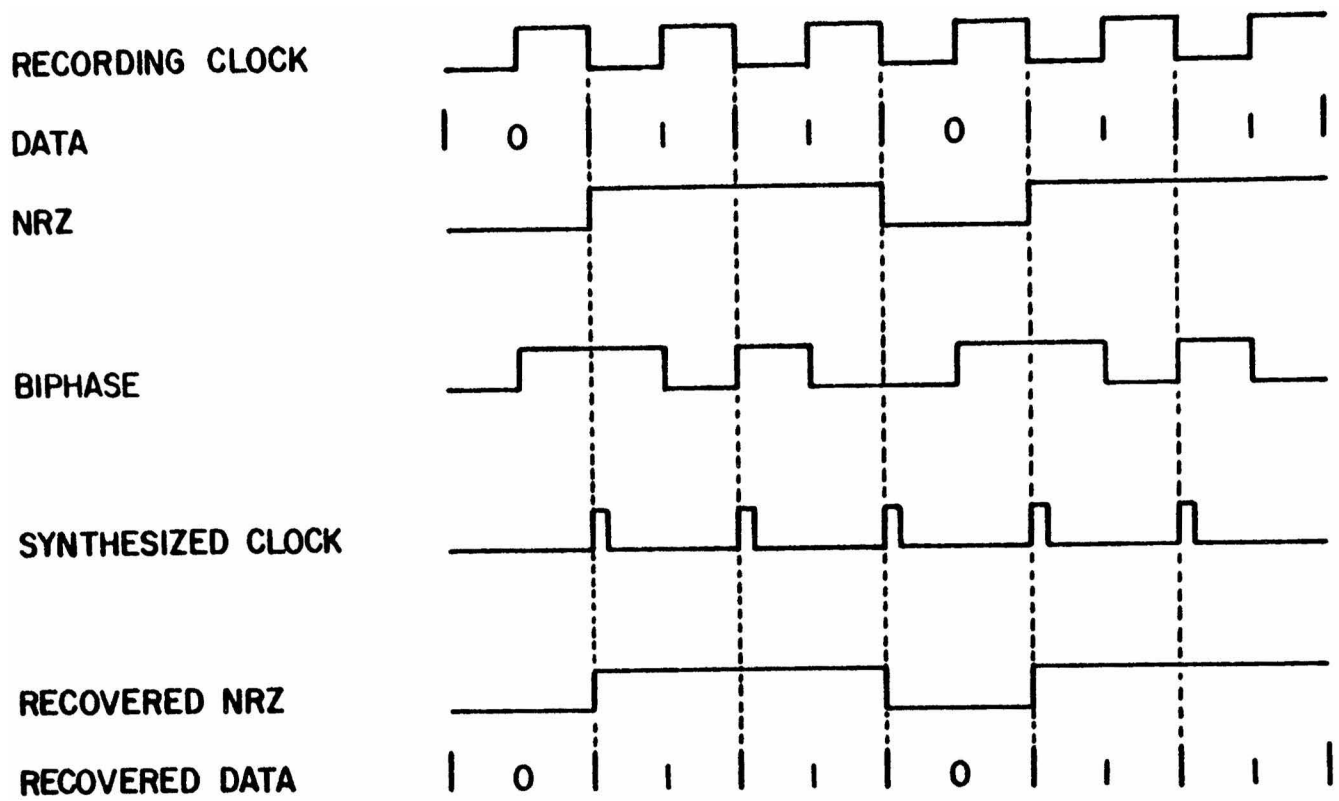

Fig. 21. Timing diagram for biphase decoding.

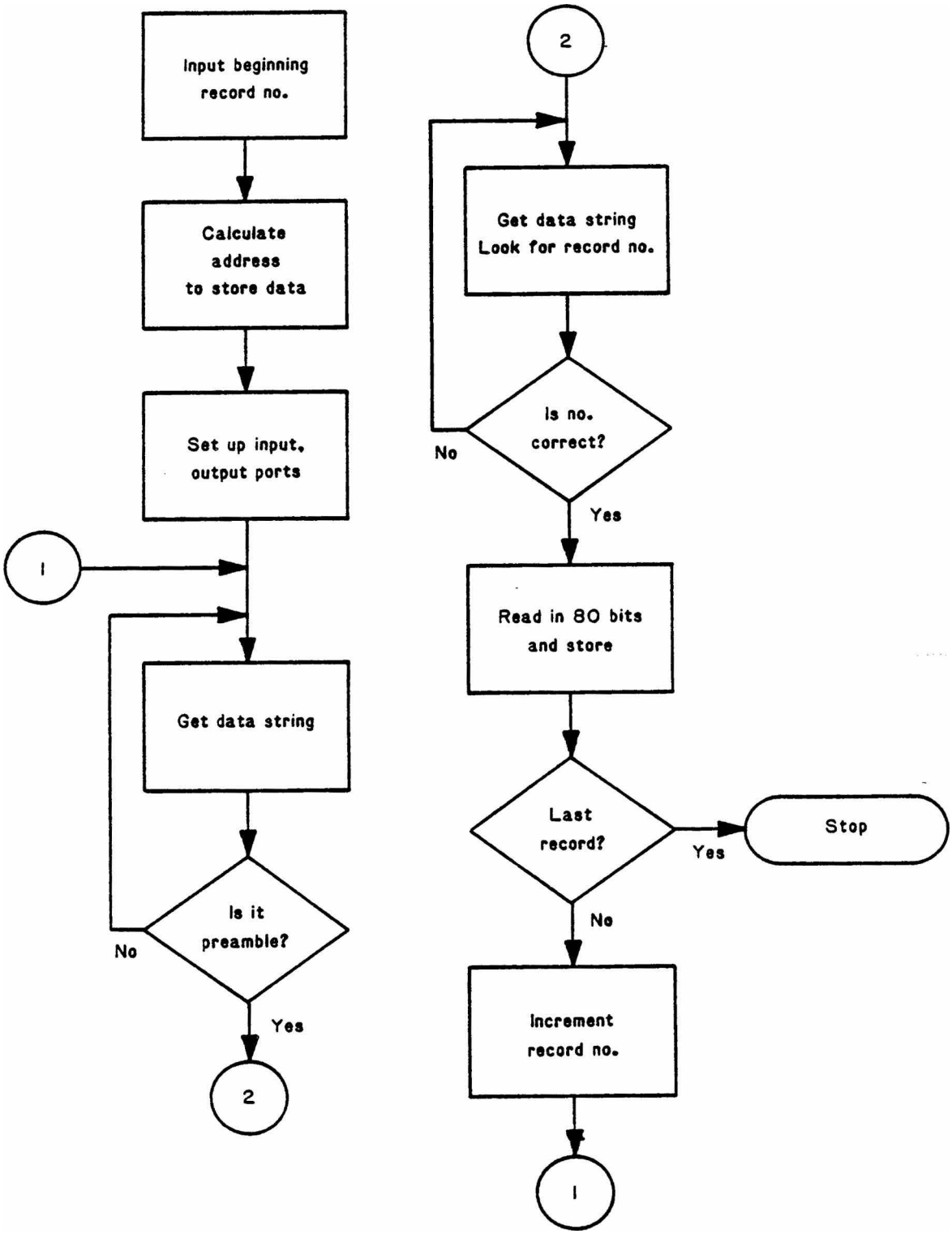

Fig. 22. Block diagram of program to read data tapes and store the binary data in memory.

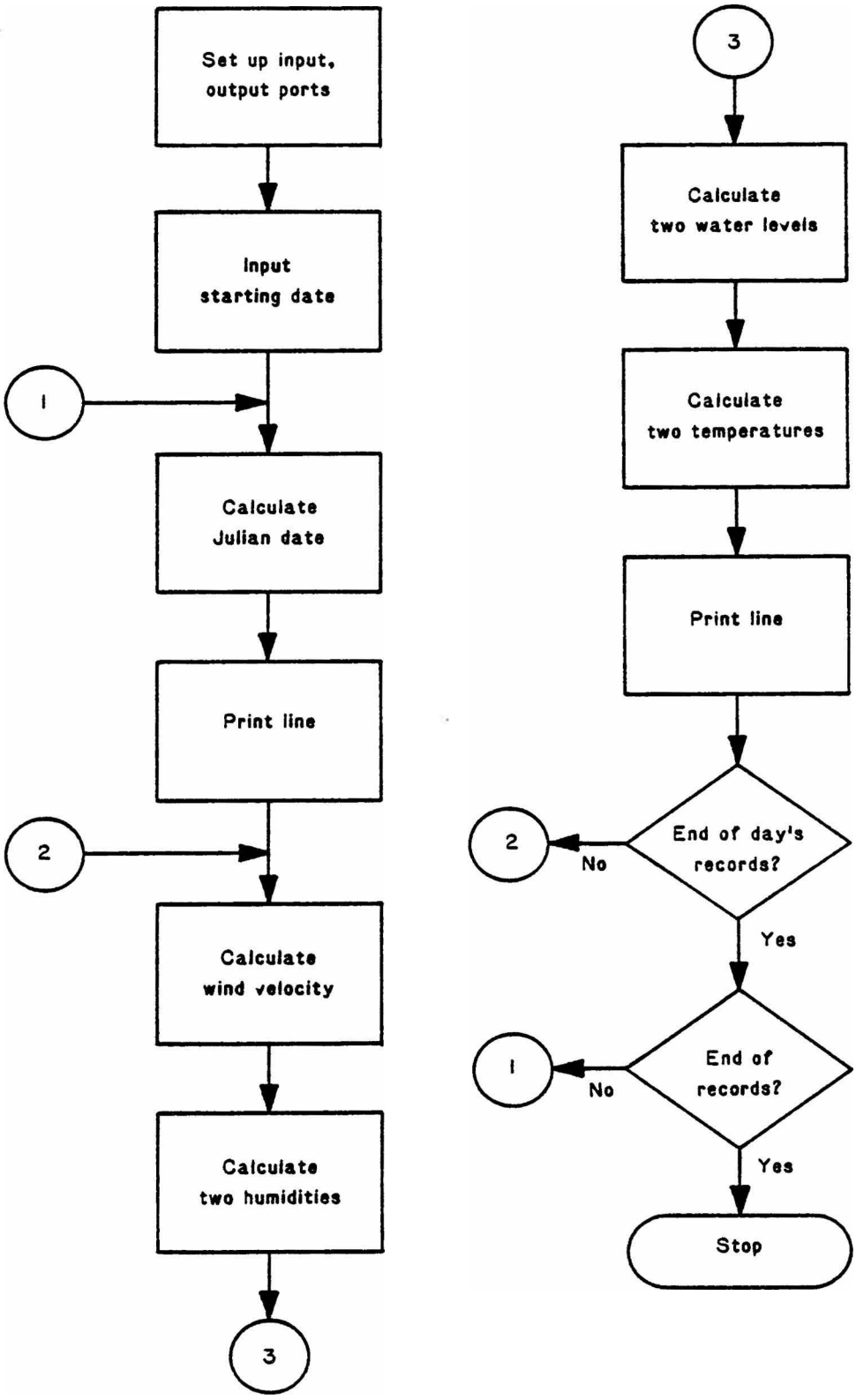

Fig. 23. Block diagram of program to convert the binary data to engineering units.

Fig. 24. Photograph of field installation.

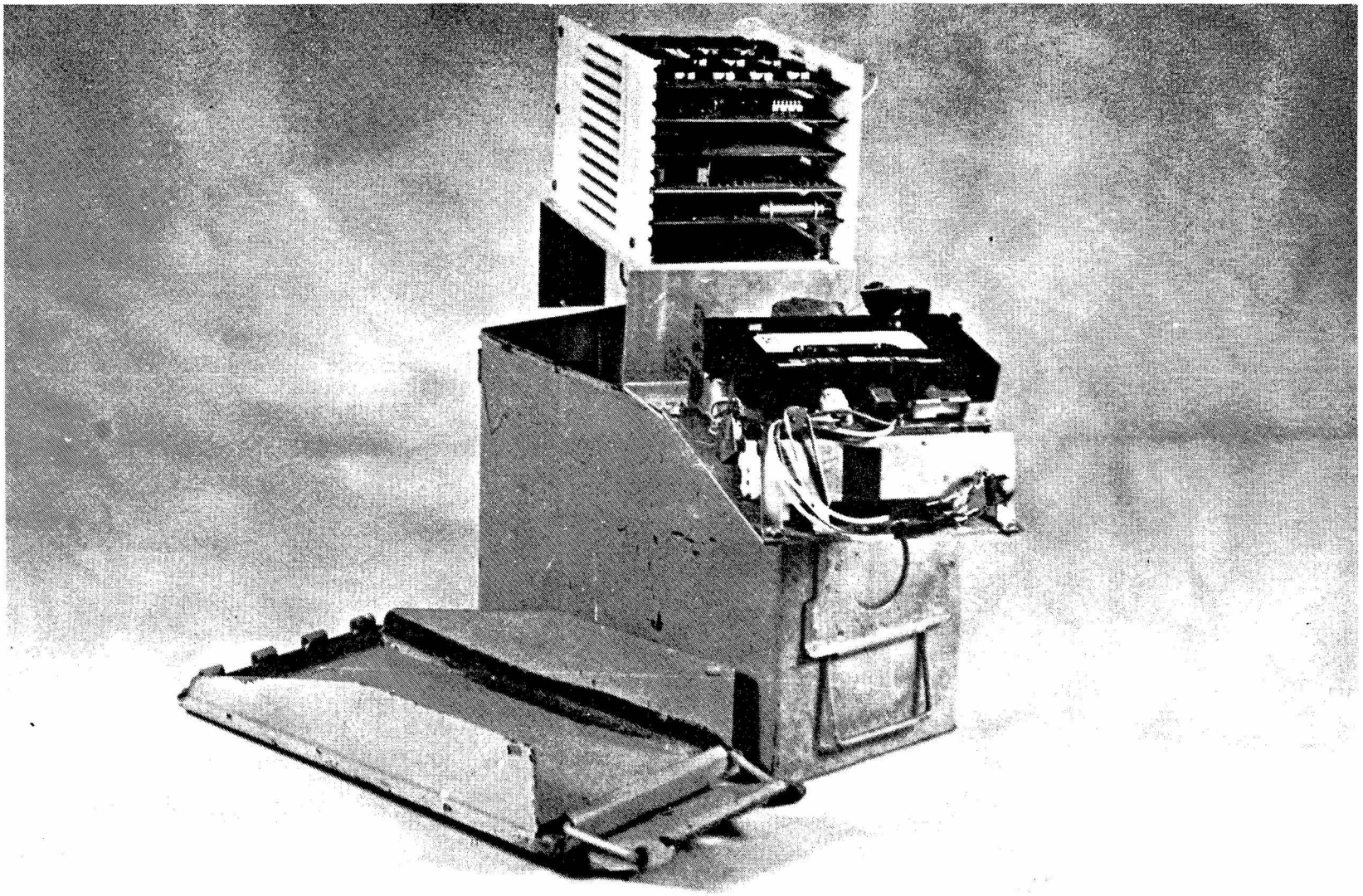

Fig. 25. The instrumentation package.

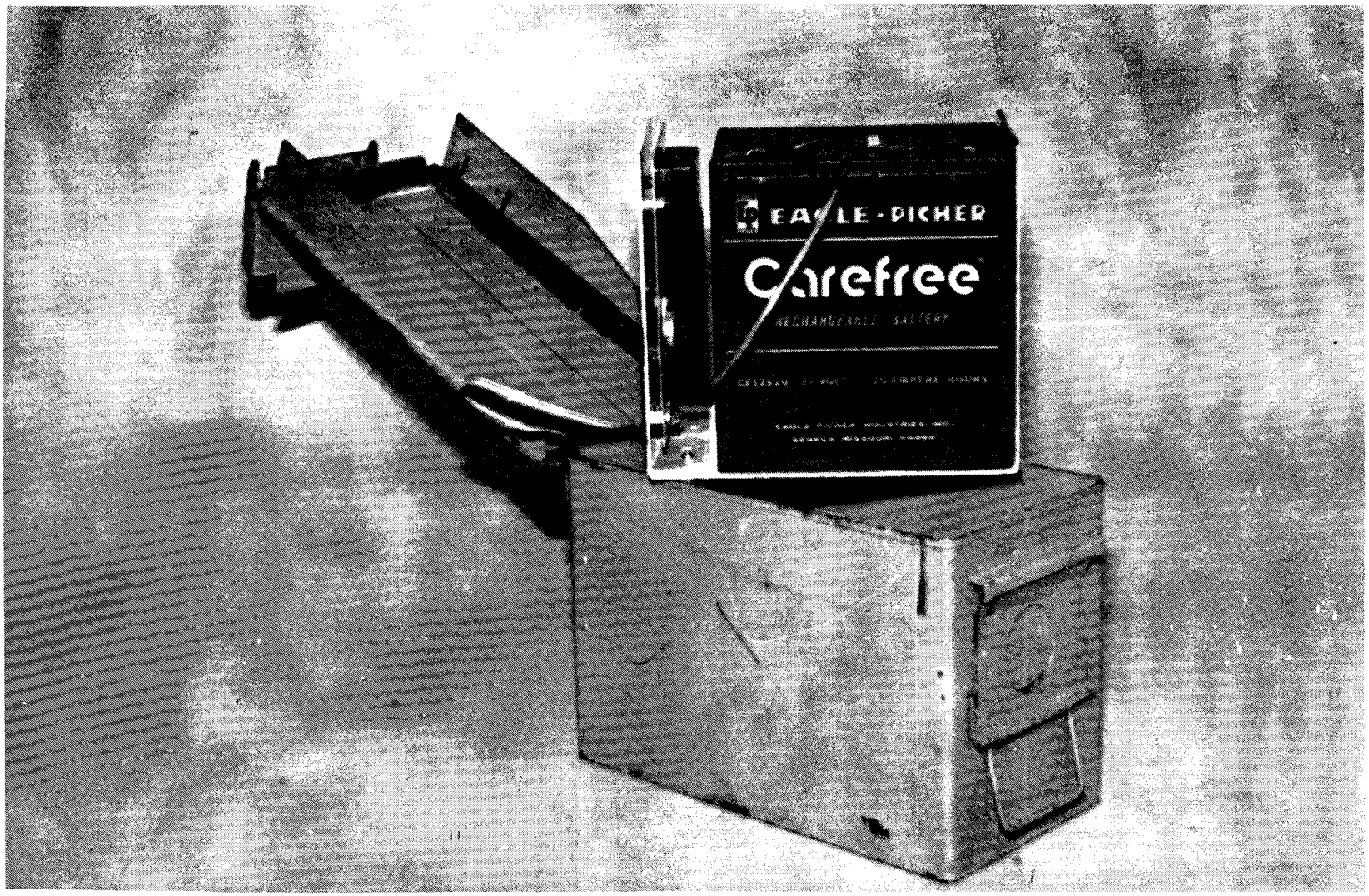

Fig. 26. The power supply package.