Electrothermal Simulation of Large-Area Semiconductor Devices

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ABSTRACT

The lateral charge transport in thin-film semiconductor devices is affected by the sheet resistance of the various layers. This may lead to a non-uniform current distribution across a large-area device resulting in inhomogeneous luminance, for example, as observed in organic light-emitting diodes (Neyts et al., 2006). The resistive loss in electrical energy is converted into thermal energy via Joule heating, which results in a temperature increase inside the device. On the other hand, the charge transport properties of the device materials are also temperature-dependent, such that we are facing a two-way coupled electrothermal problem. It has been demonstrated that adding thermal effects to an electrical model significantly changes the results (Slawinski et al., 2011).

We present a mathematical model for the steady-state distribution of the electric potential and of the temperature across one electrode of a large-area semiconductor device, as well as numerical solutions obtained using the finite element method.

1. INTRODUCTION

In a large-area semiconductor device, such as a solar cell or module, the electric charge generated inside the device due to light absorption needs to be transported towards the edges of the device in order to produce electric current. In a typical thin-film device this lateral charge transport is affected by the sheet resistance, which increases as the film thickness decreases. Thus electrical losses occur in thin-film devices, especially far from the edges. The usual way for decreasing these losses is to add metallic structures to the top electrode – busbar electrodes with additional grid lines are commonly employed, and they can be seen in most solar panels installed today. These additional structures improve the charge collection. However, a higher coverage of the top electrode by non-transparent metal will also decrease the transmission of light, which should be high for a solar cell of course.

During the electrode design process, ways have to be found to sufficiently increase the charge collection while maintaining a low coverage by non-transparent material. This is where simulation software becomes useful: it can assist the user in exploring the trade-off between charge transport and optical properties of an electrode when adding metallic structures. Various device designs can be evaluated using simulation, and the number of

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expensive trial-and-error stages during device fabrication can be reduced. The above explanations for solar cells may be repeated in an analogous way for organic light-emitting diode (OLED) devices.

The new software Laoss by Fluxim AG [1] was developed for the simulation of large-area semiconductor devices and may thus assist the user in the electrode design process. Potential new features for the Laoss software are being implemented and assessed in a prototype within the "Large Area Organic Semiconductor Software" (LAOSS) project funded by the Swiss Commission for Technology and Innovation.

In this article, we shall present a model extension developed within this project, where we added a thermal model to the already available electrical model. The extended (electrothermal) model takes into account the transformation of electrical energy into thermal energy due to the sheet resistance, as well as the heat transfer inside the device. In addition to the electro-optical design questions raised above, the extended model will also allow the user to investigate the influence of thermal properties on the device performance. For example, it can be determined how hot the device will get during operation and how the heat can be effectively dissipated in order to prevent the thermal breakdown of the device.

We shall describe this electrothermal model in Sec. 2. We briefly discuss its discretization and present some numerical results in Sec. 3.

2. ELECTROTHERMAL MODEL

A typical thin-film semiconductor device consists of multiple layers of different functional materials. In an organic light-emitting diode (OLED) device, for example, these are stacked emissive and conductive layers, which are placed between electrode layers (anode and cathode). Both charge transport and heat transfer occur in this stack, as illustrated in Fig. 1.
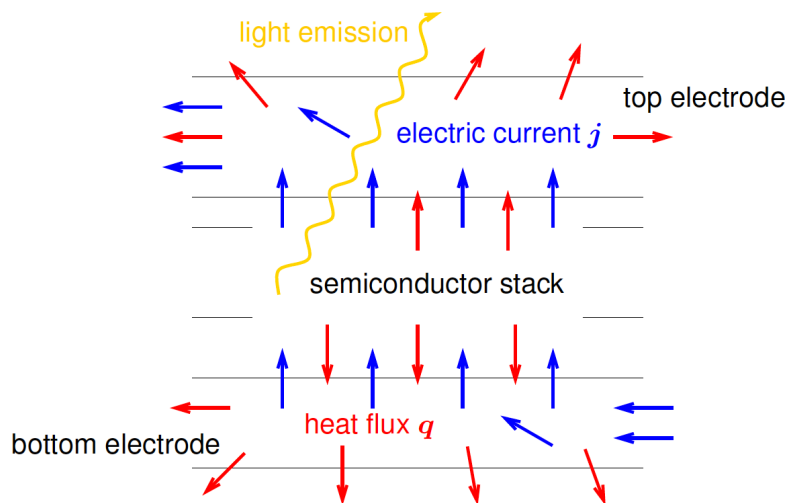

Figure 1: Vertical cross section of an OLED (organic light-emitting diode) device consisting of different functional organic semiconductor materials between two electrode layers. Both charge transport and heat transfer occur in this stack; they are indicated by blue and red arrows, respectively.

The mathematical modeling process used here follows the standard procedure of combining differential forms of continuity equations for

- the total charge density $[\mathrm{Cm^{-3}}]$ and the electric current density, $\mathbf{j}$ $[\mathrm{Am^{-2}}]$, as well as for
- the thermal energy density $[\mathrm{Jm^{-3}}]$ and the heat flux density, $\mathbf{q}$ $[\mathrm{Wm^{-2}}]$,

with the constitutive equations

$$\mathbf{j} = -\sigma \nabla \psi \ \text{(Ohm's law) and} \ \mathbf{q} = -\lambda \nabla T \ \text{(Fourier's law)} \tag{1}$$

In eq. (1), ψ $[\mathrm{V}]$ and T $[\mathrm{K}]$ denote the electric potential and the temperature, respectively, whereas σ $[\mathrm{Sm^{-1}}]$ and λ $[\mathrm{W(mK)^{-1}}]$ denote the electrical and thermal conductivities, respectively, of the materials.

The three-dimensional (3D) mathematical model thus obtained is subsequently reduced

- by assuming that the electric current and the heat flux are predominantly vertical within the semiconductor stack (cf. Fig. 1) and
- by averaging in the vertical direction within the electrodes.

Similar model reduction steps were taken in [2, 3]. The details of our model reduction process are beyond the scope of this article, and we shall report on them elsewhere at a later time. The model reduction yields a coupled 1D-2D model, which captures the important features of a real device and which is computationally efficient at the same time, because its discretization (Sec. 3) requires much less degrees of freedom than the discretization of a full 3D model.

In this article, the coupled 1D-2D model is further simplified by assuming a constant electric potential $\psi_0 := 0$ V and a constant (ambient) temperature $T_0 := 300$ K in the bottom electrode, such that only the 2D equations in the top electrode remain in the model. It then takes the form of a system of two coupled second-order partial differential equations in two space dimensions for the (vertically averaged) electric potential $\psi(x, y)$ $[\mathrm{V}]$ and temperature $T(x, y)$ $[\mathrm{K}]$ in the top electrode,

$$-\mathrm{div}\left(R_{\mathrm{Wel}}^{-1} \nabla \psi\right) = f_{\mathrm{el}}(\psi, T), \quad R_{\mathrm{Wel}} := (\sigma d)^{-1} \ [\Omega / \mathrm{W}], \tag{2}$$

$$-\mathrm{div}\left(R_{\mathrm{Wth}}^{-1} \nabla T\right) = f_{\mathrm{th}}(\psi, T), \quad R_{\mathrm{Wth}} := (\lambda d)^{-1} \ [\mathrm{KW^{-1}} / \mathrm{W}], \tag{3}$$

with the electrode layer thickness d $[\mathrm{m}]$ and with the electrical and thermal sheet resistances $R_{\mathrm{Wel}}(x, y), R_{\mathrm{Wth}}(x, y)$. The square symbols W are used here to avoid confusion with the electrical and thermal bulk resistances, which also have the units Ω and

KW^{-1}, respectively. The ratio $\dfrac{R_{\mathrm{Wel}}}{R_{\mathrm{Wth}}} = \dfrac{\lambda}{\sigma}$ is usually proportional to the temperature by

the Wiedemann-Franz law [4] – here we assume temperature-independent conductivities, however, for simplicity. Therefore, the coupling between eqs. (2) and (3) occurs via the source/sink terms on the right-hand sides only, where

- $f_{\mathrm{el}}(x, y, \psi(x, y), T(x, y))$ $[\mathrm{Am}^{-2}]$ denotes the local net electric source current density, and where

- $f_{\mathrm{th}}(x, y, \psi(x, y), T(x, y))$ $[\mathrm{Wm}^{-2}]$ denotes the local net heat source power density.

The following effects have been included in these source/sink terms so far:

- the charge transport between the semiconductor stack and the top electrode (in f_{el}). This is usually described by temperature-dependent current-voltage characteristics, in which the current density in the semiconductor stack, $j_s(\psi - \psi_0, T)$ $[\mathrm{Am}^{-2}]$, is given as a function of the voltage across the stack (potential difference $\psi - \psi_0$). It can be derived from an Arrhenius-like conductivity law as in [5], from the Steinhart-Hart equation [6], or from measurement data [7]. Notice that in our current implementation the temperature dependence is not yet included in the current-voltage characteristics. Therefore, at this point, we consider a one way coupling (electrical →thermal) only.

- the generation of heat inside the top electrode (in f_{th}). This is due to Joule heating and thus proportional to $R_{\mathrm{Wel}}^{-1} |\nabla \psi|^2$ $[\mathrm{Wm}^{-2}]$.

- the loss of heat in the top electrode (in f_{th}). This is due to heat transfer towards adjacent layers, such as the semiconductor stack below the top electrode or the glass substrate above the top electrode. In this model we use thermal transmittances U_s, U_t $[\mathrm{W(m^2 K)^{-1}}]$ to describe the heat transfer through the semiconductor stack and through the glass substrate, respectively.

- the heat transfer between the semiconductor stack and the top electrode (in f_{th}). Here the thermal energy generated in the semiconductor stack (due to Joule heating) is assumed to flow in equal parts towards the top and bottom electrodes.

The coupled 1D-2D model obtained after reduction is illustrated in Fig. 2. Eqs. (2), (3) need to be completed with boundary conditions at the edges of the top electrode, in order to obtain a well-posed problem. Here we use the following boundary conditions:

- For the charge transport (eq. (2)) we prescribe the electric potential on one edge and we assume zero electric current through the remaining edges.

- For the heat transfer (eq. (3)) the heat flux through the edges is assumed to be proportional to the temperature difference $T - T_0$ (where T_0 denotes the ambient temperature), with a heat transfer coefficient h $[\mathrm{W(m^2 K)^{-1}}]$.

The complete coupled 1D-2D electrothermal model is discretized using the finite element method, as described in the next section.

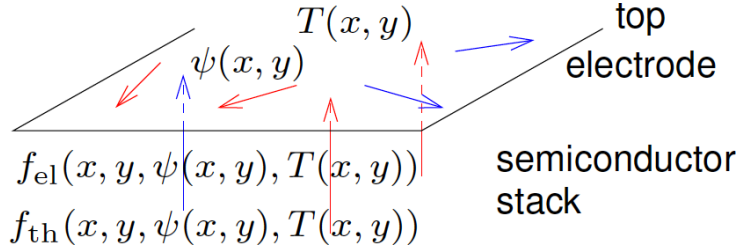Figure 2: Illustration of the coupled 1D-2D model (eqs. (2), (3)) obtained after reduction of a full 3D model. Blue arrows indicate charge transport whereas red arrows indicate heat transfer. ψ and T denote the (vertically averaged) local electric potential and temperature in the top electrode, respectively, and f_{el} and f_{th} denote the local net electric source current density and local net heat source power density, respectively.

3. DISCRETIZATION AND SIMULATION RESULTS

The mathematical model for the charge transport and heat transfer in the top electrode of a thin-film semiconductor device (described in Sec. 2) is discretized using the finite element method: For a given set of basis functions, $\Phi = \{\phi_1, \phi_2, \ldots, \phi_N\}$, with $N \in \yen$ degrees of freedom, we write

$$\psi(x,y) = \sum_{i=1}^{N} \psi_i \phi_i(x,y), \quad T(x,y) = \sum_{i=1}^{N} T_i \phi_i(x,y), \tag{4}$$

with unknown coefficients $\psi_i, T_i \in \mathrm{i}$, $i = 1, 2, \ldots, N$. Plugging (4) into the variational formulation of (2), (3) (together with the boundary conditions) yields a coupled system of 2N nonlinear equations for the vectors $\mathbf{\psi} = (\psi_1, \psi_2, \ldots, \psi_N)^\top$, $\mathbf{T} = (T_1, T_2, \ldots, T_N)^\top \in \mathrm{i}^N$ containing these coefficients:

$$\mathbf{F}_{\mathrm{el}}(\mathbf{\psi}, \mathbf{T}) = \mathbf{0} \tag{5}$$

$$\mathbf{F}_{\mathrm{th}}(\mathbf{\psi}, \mathbf{T}) = \mathbf{0} \tag{6}$$

where the entries in the functions $\mathbf{F}_{el}, \mathbf{F}_{th}$ depend on the choice of the basis $\boldsymbol{\Phi}$. The system of nonlinear equations (5), (6) can be solved using Newton's method, for example.

In the simplest case, which we have chosen here, the two-dimensional domain of the top electrode is discretized with triangles (cf. Fig 3d), and a nodal basis consisting of piecewise linear functions is chosen [8].

First we present results from simulations with the electrical model only – they are illustrated in Fig. 3. We consider square devices of different areas and with two different electrode designs, namely

- devices without metal structures added to the electrode (Figs. 4a, 5a, 6a) and
- devices with a busbar electrode and two additional metal fingers (Figs. 4b, 5b, 6b).

For all those devices we prescribe the potential at one edge of the top electrode (marked in red in Figs. 3d, 4a, 4b), and we assume zero electric current through the remaining edges of the top electrode (marked in blue in Figs. 3d, 4a, 4b). For any given value ψ_b [V] of the electric potential at the red boundary segment the difference $\psi_b - \psi_0$ [V] is called the applied voltage. Computation of the total outward electric current through the red boundary segment from the solution of (5), (6) yields the current-voltage characteristic of the device, which takes into account electrical losses due to the sheet resistance. This is in contrast to the current-voltage characteristic of the semiconductor stack (j_s), which does not take this effect into account.

Multiplying the total current by the applied voltage and dividing by the device area finally yields the power per area, which is shown in Fig. 3a for all devices without metal structures. Clearly the maximum power per area decreases as the device area increases, which illustrates the adverse effect of the sheet resistance on the performance of large-area devices. Notice also that the maximum power point shifts both vertically and horizontally as the device area changes. In Fig. 3b we illustrate that the use of a busbar electrode with additional metal fingers may improve the performance of a 5cm X 5cm device: the device with the busbar electrode has a slightly higher maximum power per area than the device without metal structures (maximum power per area 13Wm^{-2} at 0.235 V compared to 12Wm^{-2} at 0.225 V in this example), although the former device has a smaller area for the transmission of light due to the coverage by non-transparent metal (Fig. 3c indicates that no power is produced underneath the metal parts). This illustrates that some loss in light absorption due to coverage by non-transparent material may be acceptable if the charge collection is improved at the same time. Notice that the metal structure in this example was chosen arbitrarily and has not been optimized in any way; therefore, the 9 % improvement achieved here is not maximal. Fig. 3d shows a typical finite element mesh with roughly 1400 vertices used to discretize the electrode with the metal fingers: adaptive mesh refinement [9] has been used for the calculation of the device current-voltage characteristics; it ensures that additional degrees of freedom are placed only where required.

In the following calculations much finer finite element meshes with roughly 85,000 vertices were used for an increased accuracy of the scalar fields shown in Figs. 4–6. In Fig. 4 we show the electric potential [V] ψ in two 5cm X 5cm devices with and without metal structures. Here the electrical sheet resistance inside the metal is 10 times lower than in the other electrode material. According to Ohm's law (1) the electric current flows in the direction

of decreasing electric potential. A comparison of Figs. 4a and 4b shows that the electric current will flow towards the metal fingers if available, which illustrates that they are beneficial for charge collection.
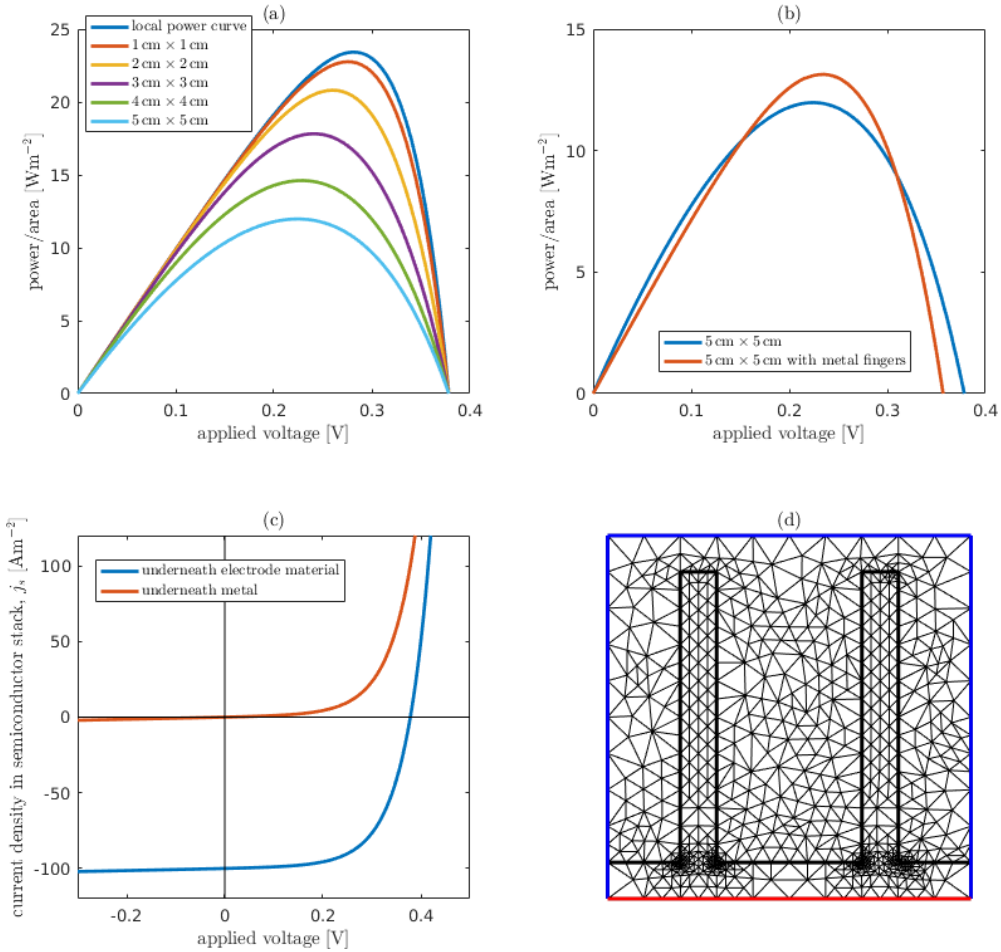

Figure 3: Electrical simulation results: (a) power per area for square devices without metal structure, (b) power per area for two square devices of the same area with and without metal fingers, (c) current-voltage characteristics of the semiconductor stack underneath the electrode material and underneath the metal finger, (d) a typical adaptively refined triangular mesh for the simulation of a square device with metal structures.

From the electrical simulation result we may now determine the thermal energy generated by Joule heating. Together with the thermal losses described earlier in Sec. 2, we obtain the net heat source power density f_{th}, which is shown in Fig. 5.

A comparison of Figs. 5a and 5b shows that both the range and spatial distribution of the net heat source power density are quite different for the two devices: while most of the

heating takes place near the current outlet for the device without metal structures (Fig. 5a), there is very little heating (and even some net thermal loss) in the busbar of the device with metal structures. The heating is very strong, on the other hand, near the junction between the busbar and the metal fingers as well as close to the metal structures in general. The rather different heating patterns observed here are expected to cause different temperature distributions.

The temperature distributions at maximum power in the two devices are shown in Fig. 6.
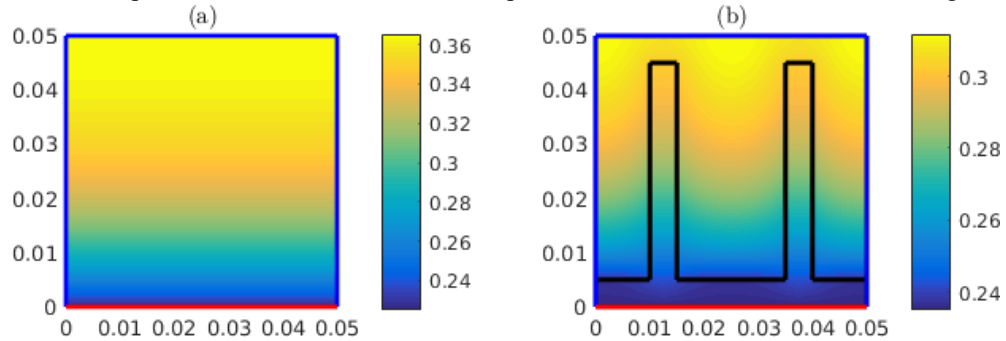

Figure 4: Electric potential at maximum power inside an electrode without metal structures (a) and in a busbar electrode with additional metal fingers (b). The unit of length is [m].
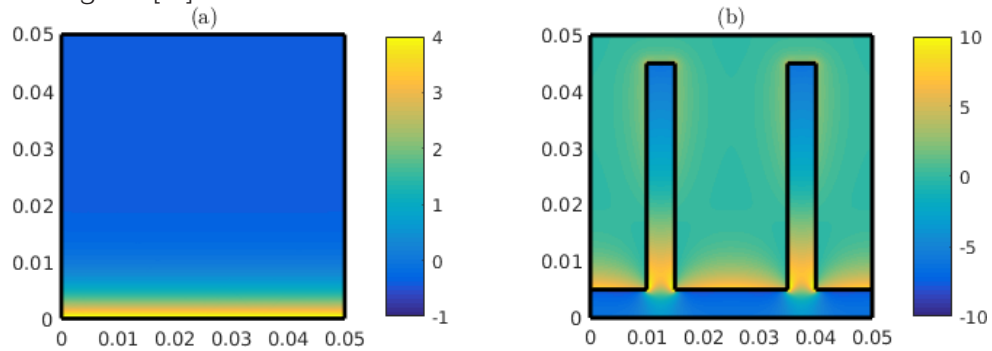

Figure 5: Net heat source power density [Wm^{-2}] at maximum power inside an electrode without metal structures (a) and in a busbar electrode with additional metal fingers (b). The unit of length is [m].
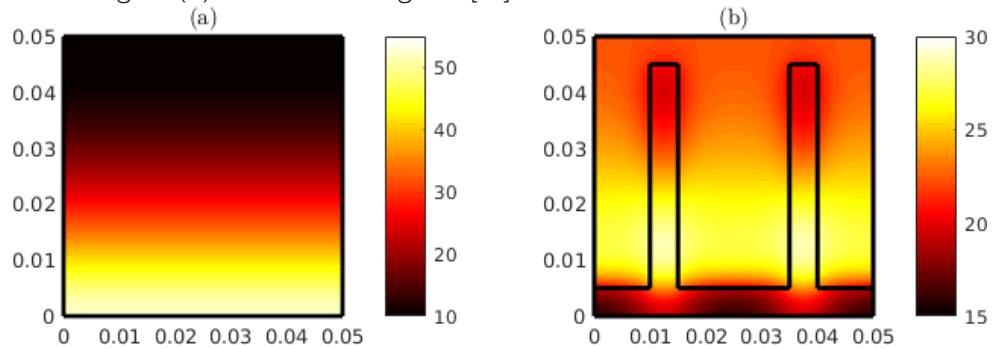

Figure 6: Temperature above ambient, $T-T_0$ [K], at maximum power inside an electrode without metal structures (a) and in a busbar electrode with additional metal fingers (b). The unit of length is [m].

Again, the temperature ranges and spatial distributions are rather different between the two devices: The temperature near the current outlet of the device without metal structures is more than 50 degrees above ambient temperature, whereas the maximum temperature for the device with metal structures is only about 30 degrees above ambient temperature. According to Fig. 6b there are hotspots near the junctions between the busbar and the metal fingers. Because the heat flows in the direction of decreasing temperature (1), it will flow predominantly inward from the current outlet in the device without metal structures, whereas the heat flow is more complicated in the device with metal structures. We expect that the different heat flux directions in these devices will have interesting consequences when the fully coupled electrothermal model is used for simulations in the near future.

4. CONCLUSIONS

We have presented an electrothermal model for large-area thin-film semiconductor devices. The coupled 1D-2D approach used here allows us to keep the number of degrees of freedom in a discretization low compared to a full 3D model.

We have presented numerical results using a one-way coupling (electrical → thermal) which illustrate that large-area device simulation software is extremely useful for evaluating different device designs. Using such software we can answer questions such as

- what is the maximum power point of the device?
- how hot will the device get during operation?
- how should the electrodes be designed for optimal device performance?
- in what way does the encapsulation affect the device performance?
- how can we effectively dissipate the heat in order to prevent thermal breakdown of the device?
- what is the effect of combining several devices in larger modules?

and many more.

We will thus continue to develop our prototype within the LAOSS project to include, among other things,

- the two-way coupling of the electrical and thermal models and
- variable electric potential and temperature in both the top and bottom electrodes.

Also within the LAOSS project the electrothermal model presented here is being validated using large-area devices fabricated by CSEM SA and by the Zurich University of Applied Sciences. We will report on the model developments and experimental validation work elsewhere in due time.

ACKNOWLEDGEMENT

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