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Analysis of negative capacitance and self-heating in organic semiconductor devices

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In admittance spectroscopy of organic semiconductor devices, negative capacitance values arise at low frequency and high voltages. This study aims at explaining the influence of self-heating on the frequency-dependent capacitance and demonstrates its impact on steady-state and dynamic experiments. Therefore, a one dimensional numerical drift-diffusion model extended by the heat equation is presented. We calculate the admittance with two approaches: a Fourier method that is applied to time domain data and a numerically efficient sinusoidal steady state analysis (S^3A), which is based on the linearization of the equations around the operating point. The simulation results coincide well with the experimental findings from reference [H. Okumoto and T. Tsutsui, Appl. Phys. Express **7**, 061601 (2014)] where the negative capacitance effect of an organic device becomes weaker with better cooling of the structure. Linking the frequency- and time-domain with the Fourier approach supports an effortless interpretation of the negative capacitance. Namely, we find that negative capacitance originates from self-heating induced current enhancement. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4916981]

I. INTRODUCTION

The influence of self-heating on the device performance has been recognized as a major issue in large-area OLEDs.[1,2] Different remedies were taken to reduce the heat generation on the anode caused by the resistive material. For example, metal grids were added on top of the anode to decrease the potential drop leading to more homogeneous potential, current, temperature, and light distributions.[3] However, in small organic devices heat generation has only recently been of concern.[4]

In order to characterize an organic semiconductor device, a number of different techniques are available and commonly performed. In admittance spectroscopy, negative capacitance values are often observed at high bias and low frequency and have started a controversial debate. Negative capacitance measurements are well known from Si diodes. Numerous explanations[5] (and references therein) are named as origin or the negative capacitance is considered a parasitic measurement effect.[6] First occurrence of negative capacitance in organic LEDs dates back about a decade.[7,8] In general, the same structure also exhibits positive capacitance at different measurement conditions such as frequency, applied voltage, or temperature. A wide range of origins for the negative capacitance have been brought forward for organic semiconductor devices.[9–13]

Most of the references investigating negative capacitance are limited to bipolar devices and do not analyze the occurrence in hole-only devices (HODs) or electron-only devices (EODs). Little work has been dedicated to unipolar devices so far. For instance, Refs. 14 and 15 report the fabrication and measurement of HOD and EOD exhibiting negative capacitance. The authors attribute the observed negative capacitance effects to interfacial states. Only recently self-heating has been identified as another origin for the negative capacitance in organic semiconductor devices by Okumoto and Tsutsui[16] for a HOD and bipolar device. Self-heating of the device changes the capacitance value of the structure, even in the case of a small device. In Ref. 16, adding a copper block on top of the HOD led to a reduced negative capacitance value indicating that the device temperature plays an important role.

In this paper, we demonstrate the influence of self-heating in the organic semiconductor with the aid of an extended one dimensional numerical drift-diffusion model on the steady-state current-voltage curve, dark injection transient currents experiment, or also called transient space-charge limited current (T-SCLC) and, most importantly, on the admittance spectroscopy. We will shed light on the occurrence of the negative capacitance in single carrier devices. Furthermore, we attempt to establish a link between the time and the frequency domain to ease the interpretation of the negative capacitance. Therefore, we simulate in the frequency domain a negative capacitance and check in the time domain if we can find indications leading to a negative capacitance value.

II. METHODS

A. Mathematical model

To model the electrical part of a hole-only device, we apply a one dimensional drift-diffusion model[17] that includes the Poisson equation (1) for the hole density p and the potential ψ

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$$\nabla \cdot (\epsilon_0 \epsilon_r \nabla \psi) = q(-p), \tag{1}$$

$$J_p = -qp\mu\nabla\psi - qD\nabla p, \tag{2}$$

$$\nabla \cdot J_p + q\frac{\partial p}{\partial t} = 0. \tag{3}$$

The vacuum permittivity is denoted by ϵ_0, the relative permittivity by ϵ_r, and the elementary charge by q. Furthermore, the continuity equation (3) with the current density J_p (2) is solved where the mobility of the organic semiconductor is given by μ.

For simplicity, we assume fixed charge carrier densities at the anode (4) and cathode (5). For a device with thickness L and with N_0 the number of sites, we write

$$p(0) = N_0, \tag{4}$$

$$p(L) = N_0 \exp\left(-\frac{qV_{bi}}{kT}\right), \tag{5}$$

where the built-in voltage is denoted by V_{bi}.

The classical drift-diffusion model (1)–(3) is only solved in the organic material layer of the hole-only device as shown in Fig. 1.

The electrical model is extended by the heat equation (6), where the temperature is given by T. We assume that heat transfer in the device takes place by thermal conduction and that thermal exchange with the surrounding is based on convection and thermal radiation. The heat transfer is calculated for the entire domain of the hole-only device. The heat source term $J_p^2/(q\mu p)$ is restricted to the organic semiconductor layer. The heat source therein is given by Joule heating,[18] which is proportional to the electrical resistance of the material. In the other layers, there is no heat source, only heat conduction. In the continuity equation for heat conduction

$$c\rho\frac{\partial T}{\partial t} = \nabla \cdot (k\nabla T) + \frac{J_p^2}{q\mu p}, \tag{6}$$

the parameter c stands for the specific heat capacity, ρ for the density, and k for the thermal conductivity.

For the thermal part, we use convective and radiative boundary conditions. The heat flux density F is calculated from the heat transfer coefficient h and the ambient temperature T_{ref}, further the emissivity is given by ϵ and the Stefan-Boltzmann constant by σ

$$F = -k\nabla T = -h(T - T_{ref}) - \epsilon\sigma(T^4 - T_{ref}^4). \tag{7}$$

We assume the same temperature for the convective air flow as for the ambient.

Note that we assume a temperature independent mobility μ, whereas the diffusion D increases with an enhanced temperature since D is proportional to the temperature T

$$D = \frac{kT}{q}\mu. \tag{8}$$

We are aware that organic semiconductors in general exhibit a temperature dependent mobility but as we show here, that does not have to be employed to explain negative capacitance. In the remainder of this paper, we will denote the one dimensional drift-diffusion model (1 to 3) with 1D-DD and the extended model (1 to 3 and 6) with 1D-EDD.

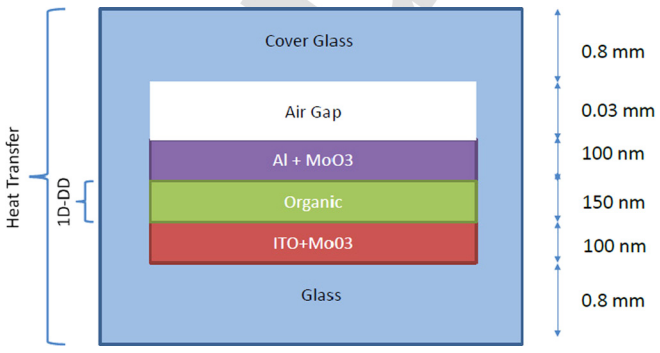

FIG. 1. Structure of HOD and thickness of layers. The heat equations are solved on the entire device domain, while the drift-diffusion model is only solved in the organic layer.

B. S^{3}A and Fourier simulation method

In this section, we introduce two different approaches for calculating the admittance of a sample device. For the sample device with all parameters given in Table I, we only consider the organic semiconductor layer at a constant device temperature of 300 K and solve the 1D-DD model. At a later stage, we also apply the methods to the 1D-EDD model.

The admittance $Y = \frac{I^{ac}}{V^{ac}}$ requires the determination of the ac current response I^{ac} to a harmonic voltage modulation $V^{ac} = V_{offset} + V_0\cos(\omega t)$. The frequency-dependent admittance

TABLE I. Material parameters for all simulations.

Thermal[25]

Material	Density [kg/m^3]	Heat capacity [J/(kgK)]	Conductivity [W/(Km)]
Glass	2.6×10^3	8.2×10^2	3.0
ITO	7.2×10^3	3.4×10^2	8.0
Organic	1.2×10^3	1.7×10^3	2.0×10^{-1}
Al	3.9×10^3	9.0×10^2	2.0×10^1
Air gap	1.2	1.0×10^3	2.5×10^{-2}

Electrical

Material	Mobility [m^2/(Vs)]	Site density [m^{-3}]	Relative permittivity
Organic	5×10^{-10}	1×10^{26}	3

Boundary conditions

B.C	Parameter	Value	Units
Thermal	h	10/50	W/(m^{2}K)
	ϵ	0.92	
Electrical	V_{bi}	0.6	V

can then by decomposed into the conductance G and capacitance C according to $Y(\omega) = G(\omega) + i\omega C(\omega)$.

The first approach is the S^{3}A. In Ref. 22, a more detailed description of the method is given and was used previously.[22–24] We first solve the steady-state equations for V_{offset} and linearize the system of equations around this operating point to get the ac equations. For each frequency ω, we solve the linear ac equations and calculate thereof the admittance $Y(\omega)$.

In the second approach, the transient current response $I(t)$ to a small voltage step ΔV is monitored and Fourier transformed. This leads to the following expression for the capacitance C and conductance G as elaborated in detail in Ref. 5:

$$C(\omega) = C_{geom} + \frac{1}{\Delta V}\int_0^\infty \delta j(t)\cos(\omega t)dt, \tag{9}$$

$$G(\omega) = G(0) + \frac{\omega}{\Delta V}\int_0^\infty \delta j(t)\sin(\omega t)dt. \tag{10}$$

The transient current density $\delta j(t)$ is defined as

$$\delta j(t) = I(t) - I(\infty), \tag{11}$$

so that $\delta j(t) \to 0$ in the steady-state limit $(t \to \infty)$.

Applying the formula for the capacitance (9) and conductance (10) to the transient current response to a small voltage step as shown in Fig. 2, we can calculate the capacitance C and conductance G of the sample device. The transient current response in Fig. 2 shows according to Ref. 21 a cusp at

$$t_{DI} = 0.786\frac{L^2}{\mu(V - V_{bi})}. \tag{12}$$

This formula can be useful for mobility determination.

A comparison between the two methods is displayed in Fig. 3. In the work of Ref. 19, the value of $0.75C_{geom}$ is obtained below the transit frequency. Note that capacitance in our case is slightly enhanced due to diffusion which was neglected in Ref. 19, but we have previously shown[20] that the low-frequency capacitance reaches values of $0.8C_{geom}$ (not simply $0.75C_{geom}$) because the numerical model considers

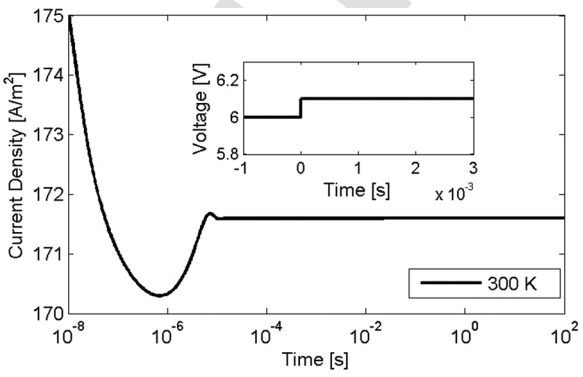

FIG. 2. The current density response over time is shown. A cusp is found and eventually the steady-state is reached. In the inset, the small voltage step is displayed.

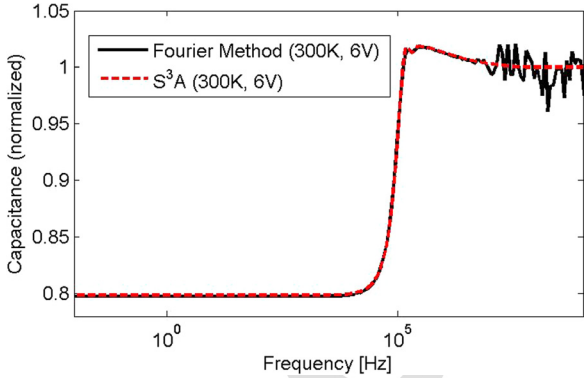

FIG. 3. The capacitance is calculated with two approaches: the black line represents the S^3A solution, while red stands for the Fourier method. At high frequency, the accuracy of the Fourier method is clearly limited.

charge diffusion, too. The negative differential susceptance $-\Delta B = -\omega(C(\omega) - C_{geom})$ yields a maximum at f_{max} due to the transit time effect leading to

$$\mu = 1.85\frac{L^2 f_{max}}{(V - V_{bi})}. \tag{13}$$

Comparing the two methods shows that the Fourier method is less accurate at high frequencies as the accuracy is dependent on the size of the time step Δt in the transient current response ($\Delta t \ll 2\pi f_{high}^{-1}$). Moreover, the applied voltage step ΔV must be small in order to be in the linear regime of the device, yet big enough to get an accurate numerical current resolution.

Despite the fact that the S^{3}A provides superior numerical accuracy, the Fourier method allows for an effortless interpretation of the negative capacitance effects in the time-domain. We have now two methods at hand that allow for the determination of the capacitance C and conductance G. The two methods will be applied in Sec. IV.

III. STATIONARY SIMULATIONS

First of all, we turn to steady-state simulations and compare the results of the 1D-DD and 1D-EDD model. All parameters are given in Table I.

In a first step, we perform the most common characterization technique and calculate the current-voltage curve for the 1D-DD model for a constant device temperature of 300 K. This result is shown as the black line in Fig. 4. In a next step, we extend the model by the heat equation on the entire domain and recalculate the current-voltage curve (allowing for self-heating of the device) and obtain the red curve (1D-EDD). At high voltage, self-heating clearly enhances the current. A change in temperature enhances diffusion (see Eq. (8)) and leads to more carriers in the device. Thus, the current increases.

In Fig. 5, the temperature profile of the entire device at 6 V is displayed at steady-state. We notice that the air gap is mainly responsible for the temperature difference in the device. The inset shows the temperature distribution of the electrodes and the organic layer as indicated by the arrow in

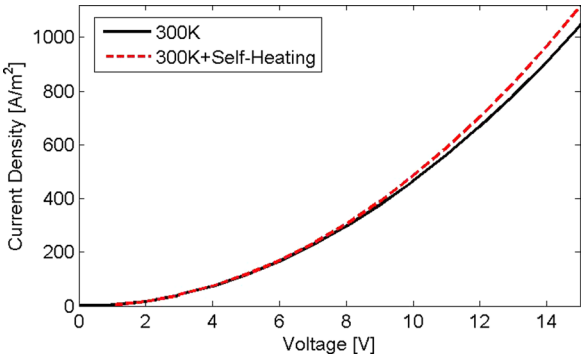

FIG. 4. Current-voltage curves for constant temperature in the device (black) and extended model with self-heating (red). Self-heating rises the current at high voltage.

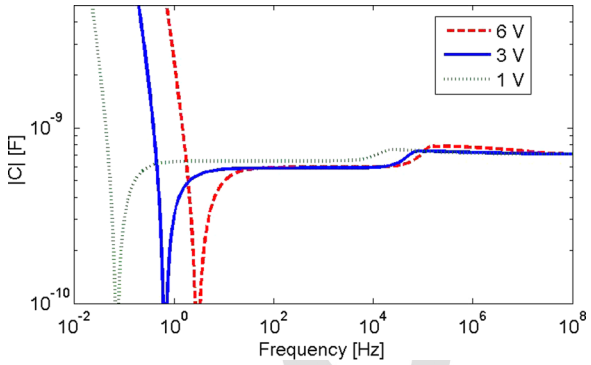

FIG. 6. The absolute value of the capacitance of the 1D-EDD model for different voltages. Including the heat equation leads to a considerable change in the capacitance at low voltage. At low bias, the effect is decreasing.

Fig. 5. Joule heating leads to the enhanced temperature in the organic layer.

IV. TRANSIENT SIMULATIONS

The difference between the two models becomes even more distinct when we look at time-dependent measurements and simulations. Calculating the capacitance for the 1D-DD model leads to the well known curve for a HOD as shown in Fig. 3 or Refs. 22–24. The capacitance step at around 10^5 Hz can be related to the charge carrier mobility.[22] Namely, at higher frequency the capacitance approaches the geometric capacitance of the device. Solving the 1D-EDD model with heat transport changes the result vastly. At low frequency and high bias, negative capacitance values are found as shown in Fig. 6. The capacitance step remains at the same position for the same applied voltage independent of self-heating. In Fig. 6, the capacitance values for different applied voltages are displayed for the 1D-EDD model. The higher the applied bias, the more pronounced is the negative capacitance effect.

In order to compare the effect of cooling in our model with measurements in Ref. 16, we calculate the capacitance of a HOD with thickness 150 nm as displayed in Fig. 7. By changing the value for the convective cooling parameter h (see 7), we can simulate the effect of a copper block and get an excellent agreement with measurement as shown in Fig. 4 of Ref. 16. Cooling makes the device less inductive. The thermal parameters for the simulation are taken from Ref. 25.

The simulations can capture the features of the measurements. Without the copper block, the capacitance becomes increasingly negative with lower frequency and only flattens at around 10^{-3} Hz. Cooling the device flattens the capacitance curves at around 10^{-2} Hz. The two situations show that self-heating can lead to a negative capacitance, even in a hole-only device. To shed light on the source of the negative capacitance, we calculate the transient response for the 1D-DD and 1D-EDD model. In terms of physics, this implies that in the first case the device temperature remains constant and in the second case self-heating is included. In Fig. 8, the transient current density responses are shown for a voltage step of 0.1 V. The current density values of the top curve are higher due to self-heating. Both curves show a transit-time cusp at t_{DI} regardless of self-heating. This is in agreement with the top curve which, however, still increases after several orders of magnitude in time after the cusp. The heat generated in the organic layer is conducted through the device increasing the overall temperature, which again leads to a higher current density in the organic layer. This is a slow thermal process and the final steady-state current density

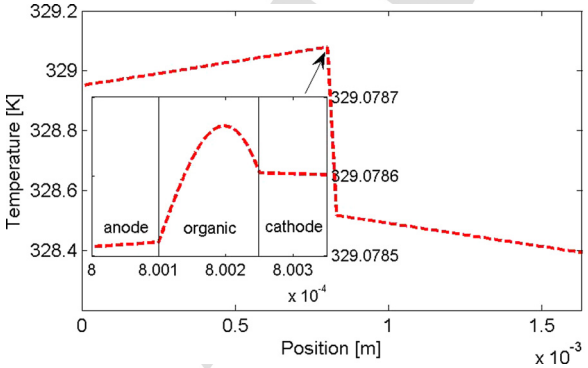

FIG. 5. For an operating voltage of 6 V, the temperature distribution over the entire device is shown in steady state. The biggest temperature drop is over the air gap between the cathode and the encapsulation. The arrow indicates the electrodes and organic layer. They are zoomed in the inset. Joule heating acts as a heat source in the organic material. The generated heat is then transferred to the electrodes.

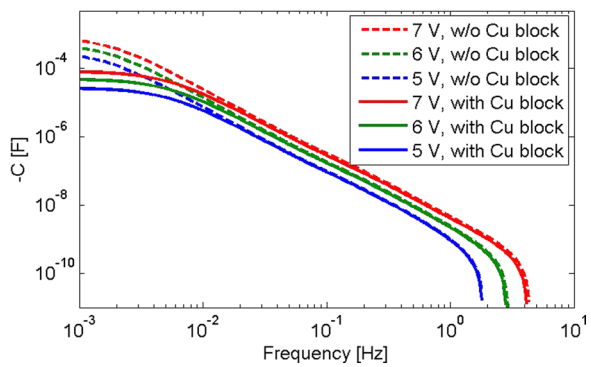

FIG. 7. Simulation of measurement features for different voltages and with and without the copper block. The cooling is modeled by changing the convective cooling boundary conditions. Cooling leads to smaller absolute capacitance values.

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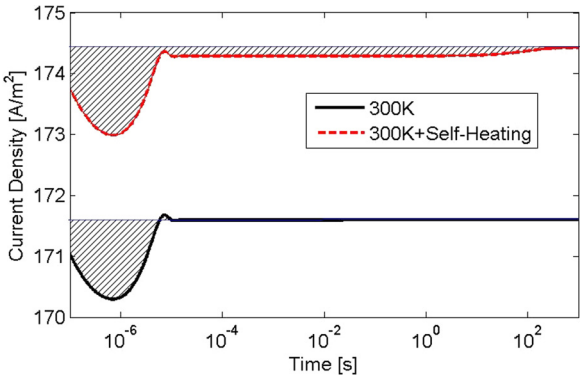

FIG. 8. Current density response for the 1D-DD and the extended 1D-EDD model to a voltage step of 0.1 V at an operating voltage of 6 V. The blue line represents the steady-state value and the reference level for the integral in Eq. (14) for the two cases. In the case of self-heating, the shaded area under the reference line is significantly bigger resulting in a negative capacitance value.

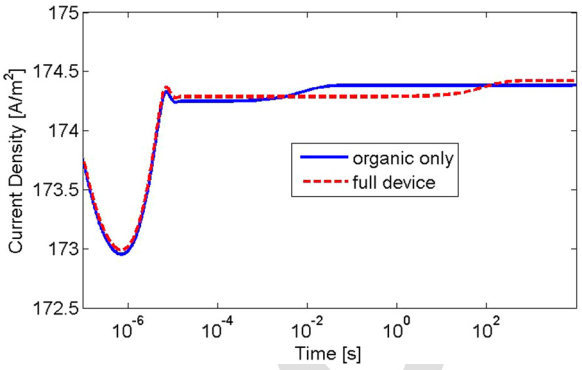

FIG. 9. The simulated transient response to a voltage step of 0.1 V at an operating voltage of 6 V is shown for two assumptions of the thermal modeling domain. If the modeling domain only contains the organic semiconductor layer then the self-heating induced current rise occurs within milliseconds. However, if the entire device including the glass substrate is included in the thermal model domain, then the characteristic time scale for the self-heating-induced current rise occurs at approx. 100 s after turn on, which is a realistic warm up period often observed in experiment. The time of the dark injection transient cusp is determined by the drift-diffusion model and thus identical for both assumptions of the thermal model domain.

value is only reached after a while, approx. 10^2 s here. Transforming the data from the time domain to the frequency domain according to Eq. (9) reproduces the negative capacitance effect nicely for the device with self-heating. The absolute value of the capacitance is shown in Fig. 6 for different voltages. The curve corresponding to Fig. 8 is at 6 V, while the curve without self-heating corresponds to Fig. 3. To understand the negative capacitance occurrence, Ershov[5] has pointed out that for low frequencies formula (9) can be approximated by

$$C(0) = C_{geom} + \frac{1}{\Delta V}\int_0^\infty \delta j(t)dt. \qquad (14)$$

This implies that the integral that we add to the geometrical capacitance C_{geom} only depends on the transient current response with respect to its steady-state value as indicated with the blue line. The shaded area for the 1D-DD is mainly under the blue line leading to a negative contribution. It is responsible for the reduction of the geometric capacitance to a value of approximately $0.8C_{geom}$ in Fig. 3. The shaded area under the blue line is clearly bigger in the case of self-heating leading to an even more negative capacitance contribution such that expression (14) turns negative. Note that we used a logarithmic time scale in Fig. 8 and the initial contribution to the dark injection transient cusp is relatively small in comparison to the rest of the shaded area. With this approach, we can easily classify a device with respect to negative capacitance from its transient current density response. The temperature increase due to self-heating enhances the current density order of magnitudes later in time, which is thus responsible for the negative capacitance effect.

In order to investigate the resulting time scale for heating, in Fig. 9 the simulated transient current density response is simulated for two distinct thermal model assumptions. The case of a thermal model including the entire device domain with the glass substrate is compared to a case where a reduced thermal model domain only including the organic semiconductor layer is considered. If the entire device including the glass substrate is included in the thermal model domain, then the characteristic time scale for the self-heating-induced current rise is approx. 100 s after turn on. The size of the simulation domain changes the observed time lag when the self-heating starts. The larger the simulation domain, the longer it takes to heat up and the hotter the device becomes. This is in agreement with the characteristic time t_{char}

$$t_{char} = \frac{L_{tot}^2}{k_e/(c_e\rho_e)}, \qquad (15)$$

for the heat equation. The total device thickness of all layers and glass is denoted by L_{tot} and the effective thermal materials parameters have a subscript e. As expected, the dark injection transient time cusp remains at the same position for the two devices. Comparing the capacitance of the two devices leads thus to a different frequency where the negative capacitance effects set in as shown in Fig. 10. The encapsulation of an organic device is thus crucial for its electrical performance and can change the negative capacitance

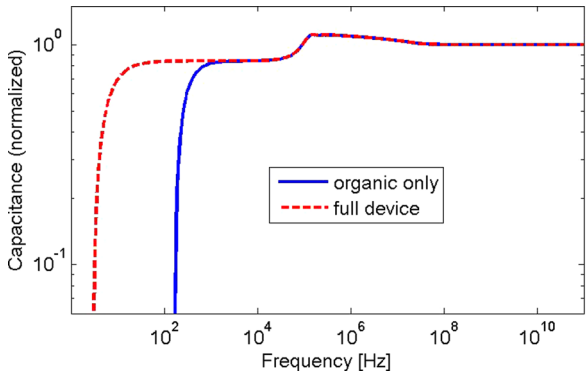

FIG. 10. The corresponding frequency-dependent capacitances to the transients in Fig. 9 are shown. For the more realistic thermal modeling domain including the glass substrate, the drop in capacitance (leading eventually to negative values) occurs at smaller frequencies, then in the simplified thermal model where only the organic semiconductor is considered.

behavior. Depending on the measurement regime, some scientists may claim that negative capacitance does not even occur, but changing the frequency range, the total device thickness or material around the organic semiconductor may reveal a negative capacitance effect. As indicated in Eq. (15), the characteristic time depends on the total thickness of all layers L_{tot} and on the thermal properties of all layers involved.

V. CONCLUSIONS

To identify and understand the origin of negative capacitance in organic semiconductor devices, the 1D-DD model of the organic semiconductor layer has been extended by the heat equation on the entire domain. With this model that includes Joule heating as heat source in the semiconductor layer, negative capacitance effects in single carrier devices were investigated. As opposed to large-area devices where the heat generation of the electrodes is considered, we focus on the self-heating in the organic semiconductor layer.

The model demonstrates the effect of self-heating in terms of the current voltage curve, but more importantly and distinctively, in dynamic characterization. We emphasize that our conclusions were drawn from a model in 1D and there is no need to resort to 3D. The model agrees very nicely with measurements from Ref. 16. Previously, other explanations as trap dynamics, interfacial states, recombination, etc., were named as origin of negative capacitance. These effects, however, would not be affected by adding a copper block on top of the device and could not reproduce a negative capacitance effect by simulation. The 1D-DD model extended by heat conduction allows for a comprehensive and consistent description of charge transport taking all major physical processes into account as opposed to simpler models such as presented in Ref. 16 or equivalent circuit models.[14,15]

With the aid of the Fourier method, an accessible explanation of the negative capacitance has been presented which allows for an interpretation in the time domain, which is generally more intuitive than the frequency domain.

The analysis, however, has been restricted to a trap-free unipolar, single layer sample with constant mobility and simplified boundary conditions. As a next step, a quantitative comparison between measurement and simulation is desired. The model can be further improved by including a temperature-dependent mobility model. In unipolar samples, the negative capacitance effect might be overshadowed by adding trap states if they act on a similar time scale. Trap states usually enhance the capacitance at low frequency,[22] while self-heating lowers the capacitance. The signature of trap states in the current voltage curve would lead to a reduction of the current density. In the DITC, a decay after the transient-time cusp represents the trapping process.

The simulations show the importance of self-heating in small devices and confirm self-heating as origin of negative capacitance. Depending on the structure of the samples, this might lead to undesired effects in the performance. Heat dissipation should be taken into account when fabricating organic semiconductor devices and be considered in any electrical characterization technique regardless of dc, ac, or transient.

In conclusion, it is crucial to model the heat generation and transport in organic semiconductor devices in order to obtain accurate simulation results at typical operating conditions, i.e., current densities of organic semiconductor devices. So far, the role of self-heating, especially in small devices, has been underestimated. It is very likely that our findings are not restricted to organic semiconductor devices but would hold for wider classes of materials and devices.

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