Flexible Silicon Photonic Transmitter with Segmented Modulator and 32 nm CMOS Driver IC

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Abstract: We present a novel silicon photonic transmitter including 90nm CMOS segmented modulator co-packaged with low power 32nm CMOS driver IC. Optical equalization is demonstrated for the first time with the multi-segment Mach-Zehnder modulator at 22Gb/s.
OCIS codes: (130.4110) Modulator; (250.3140) Integrated optoelectronic circuits.

1. Introduction

Recently silicon photonics which leverages the widely deployed complementary metal-oxide semiconductor (CMOS) technology has been acquiring attention for optical communications in datacenters as well as access and metro networks. With the advantages of building on top of the long history of CMOS technology, silicon photonics would potentially provide a low cost, large scale integration, power efficient and small footprint solution [1,2] to cope with the exponential increase in data traffic. At the same time, there is a requirement to drive down power consumption of the electrical integrated circuit (IC) in the optical transceiver for higher power efficiency of the optical link. In this paper we present a novel transmitter design, which employs a silicon segmented Mach-Zehnder modulator (MZM) wire-bonded to a low power multi-channel 32nm CMOS driver IC. The segmented MZM structure allows equalization (EQ) to be performed in the optical domain, with demonstrated improvements in the BER performance of the optical link. Without the EQ, an error floor is observed at 22Gb/s while with the EQ error free ($BER<10^{-12}$) transmission has been achieved. The work here couples the advantages of segmented modulators—which reduce the device capacitance seen by each driver segment enabling extended modulation bandwidth—with the advantages of a novel EQ scheme that is demonstrated here. Whereas a segmented modulator driven by an equalized driver IC typically requires a driver with significantly more bandwidth than the modulating device, the scheme demonstrated here provides an equalized optical waveform that can overcome bandwidth limitations in the link, while employing drivers and devices with more evenly matched bandwidths.

2. Driver IC and segmented modulator design

The 6-channel driver IC was fabricated in IBM's 32nm SOI CMOS technology. Each channel has a similar architecture to the single-channel driver reported in [3], but modified for lower power and to achieve a better interface with the modulator. The input RF signal drives a first stage of cross-coupled CMOS inverters that amplify the signal to swing from V_{SS} to V_{DD} (1V). Subsequently, the level shifter provides two outputs swinging from V_{SS} to V_{DD} and from V_{DD} to V_{DD2} (2V). These outputs drive a single stacked CMOS inverter chain. The 2-V_{pp} output differential signal of each channel will then drive each segment of the silicon modulator in a push-pull configuration. Each channel's core circuits occupy 20µm×100µm. The segmented MZM was fabricated in IBM developed CMOS Integrated Nano Photonics technology [2]. The modulator has six isolated 200µm-long PN phase shifters in each arm and the measured capacitance of each segment including the pad was about 130fF.

3. Experiments and Results

The experiment setup is illustrated in Fig. 1. The segmented MZM modulator and 6-channel driver IC were wire-bond co-packaged on a custom printed circuit board (PCB). A pattern generator is employed to generate a PRBS-7 sequence. The signal is then split into six streams and amplified to provide sufficient driving signal to 6 channels of the driver IC. Electrical phase shifters are used to finely control the delay of the driving signals. The differential output of each channel of the IC drives each segment of the modulator in push-pull configuration. A distributed feedback (DFB) laser is used to provide input light at a wavelength of 1310nm. A polarization controller is placed before the modulator. The light is edge-coupled to the silicon modulator through single-mode tapered-lensed fibers positioned with 3-axis precision stages. DC biases are provided to the PCB through ribbon cables. V_{DD} is biased at 1V while V_{DD2} is biased at 2V. A source-meter is employed to bias the cathode of the modulator at 2.5V. Output

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light from the modulator is tapped 1% for power monitoring, while 99% passes through an optical amplifier (OA). The amplified signal then goes through a variable optical attenuator (VOA) and a 50/50 coupler before entering a reference receiver, which is a commercial 43Gb/s receiver with integrated trans-impedance amplifier (TIA). The differential electrical output signal from the receiver is then fed into the BER tester and the sampling scope. A signal generator is deployed to provide external clock for the pattern generator, the BER tester and scope trigger.

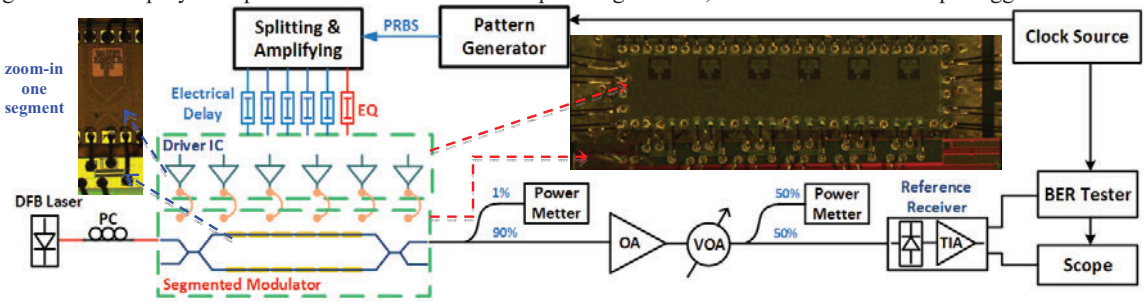

Fig. 1. Experiment setup with the inset micrographs of the silicon photonic transmitter including segmented modulator and CMOS driver IC.

To investigate the effects of optical EQ, five segments of the segmented modulator are driven by the same pattern with matched delay while the sixth segment is driven with reversed pattern and tuned delay to obtain feed-forward EQ. By trading-off the optical extinction ratio of the transmitted signal, optical EQ would provide a more open eye that yields improvement in receiver sensitivity and jitter [4]. That is illustrated by the eye diagrams at 22Gb/s in Fig. 2(right) when the EQ is turned off and on. Measured extinction ratio (with 5Gb/s signal) is reduced from 2.2dB to 1.8dB when EQ is turned on. However, as shown in the jitter and BER measurement results in Fig. 2(left, center), the optical EQ significantly improved the jitter and receiver sensitivity of the link. At 22Gb/s, without EQ, the bathtub curve at -3dBm received power in Fig. 2(left) is closed. When turning on the EQ, jitter measurement shows an open bathtub curve yielding estimated 0.21UI eye-opening at BER=10^{-12} with 9.4ps deterministic jitter and 30ps random jitter. The BER versus optical modulation amplitude (OMA) curves in Fig. 2(center) clearly confirm this improvement. Without EQ, an error floor appears at 10^{-10} while with EQ, error free back-to-back transmission can be achieved with BER=10^{-12} at −7dBm OMA. The CMOS driver IC consumed low power at 105mW, with a corresponding power efficiency of 4.8pJ/bit.

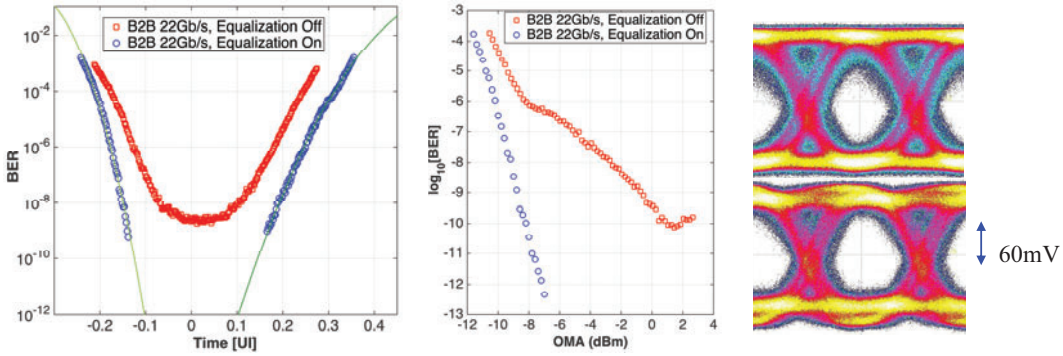

Fig. 2. Jitter measurement at -3dBm received power (left) and receiver sensitivity (center) of segmented modulator at 22 GB/s without/with optical EQ; Eye diagrams at 0dBm received power without (upper-right) and with (lower-right) optical EQ.

4. Conclusion

In this paper, we reported a silicon photonics segmented modulator fabricated with 90nm CMOS technology. The silicon modulator was driven by a 6-channel 32nm CMOS driver IC wire-bonded in the same package. Error free transmission up to 22Gb/s was achieved with optical EQ. The transmitter further provides flexibility in varying the EQ's tap weight by altering the ratio of segments devoted to main and equalizing signals (5:1 here). Moreover the proposed transmitter configuration could be employed to generate signals with multilevel modulation format such as PAM-4, as has been demonstrated [5]. That shows the potential of a flexible silicon photonics transmitter for fast-reconfigurable agile optical networks.

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