Article

Design of Single Phase SiC Bidirectional DC-AC Converter with Low-Cost PLL for Power Factor Correction

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Abstract: The paper presents the design stages of a single-phase Silicon Carbide bidirectional DC-AC converter. This includes the LCL filter design responsible to meet grid connection requirements. A 3kW laboratory prototype of the power converter is built employing a low-cost phase locked loop and its results are presented. The design of the low-cost phase locked loop and its implementation are depicted in some detail.

Keywords: SiC bidirectional AC-DC converter; inverter; variable frequency; PLL; LCL filter

1. Introduction

Nowadays, society has a big interest in topics involving sustainability and energy efficiency mainly due to environmental concerns, [1]. This is observed on the increasing number of electric vehicles and their interaction with the grid, [1]. It is also seen in micro, medium and big scale renewable energy applications with and without energy storage systems, [2]. On a political level, this is shown with various funds and measures aimed at encouraging the investment in these themes. Most of these applications use electronic power converters, which has led to recent developments in the technology of semiconductor devices originating wide band gap semiconductors, [3]. The most promising devices from this group are Silicon Carbide (SiC) and Gallium Nitrite (GaN) devices. Compared to the traditional Silicon (Si) semiconductors, wide band gap devices support higher current densities, higher switching frequency and higher operation temperatures, [4,5]. This contributes to more compact and efficient power converters decreasing the size of passive devices such as inductors and capacitors, [6]. This paper presents a simple design approach for a SiC bidirectional DC-AC converter that permits the charge and discharge of a battery bank to the AC grid with unity power factor used for a grid connected Telecom Energy Storage application. Inductor design, AC filter design and the controller principles are also treated. A 3kW converter prototype is implemented in the laboratory and its results presented.

2. SiC Bidirectional DC-AC Converter Control Principles

The topology analyzed in this work is a non-isolated bidirectional DC-AC converter, with unity power factor, presented on Figure 1.

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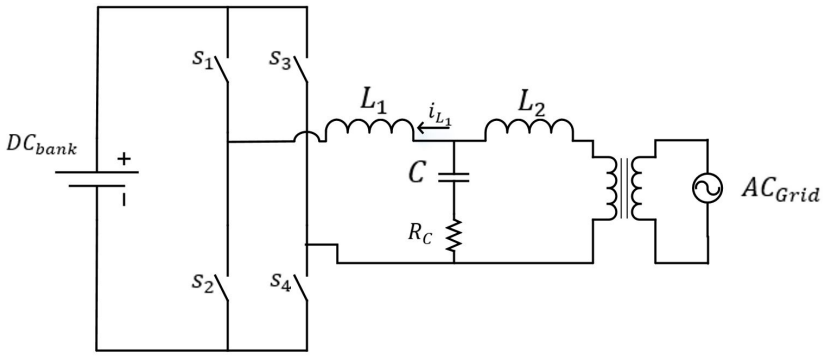

Figure 1. Proposed DC-AC Circuit topology

2.1. Output LCL Filter

Grid connected power electronic converters have Power Quality requirements. This is translated into keeping the Total Harmonic Distortion (THD) lower than 5%, according to IEEE 519-1992 standard. This is accomplished using a filter between the switches and the grid.

The filter has a big influence on the converter's size, cost and performance. It's possible to reduce its size using higher switching frequencies, which is one of the reasons why wide band gap semi-conductors contribute to smaller and more efficient power converters.

On the other side, exploring the switches at their maximum frequency all the time will lead to excess switching losses. For this reason, variable switching frequency is used on this work. This is done by controlling the current on the inductor L_1 within a hysteresis window, as seen on Figure 2.

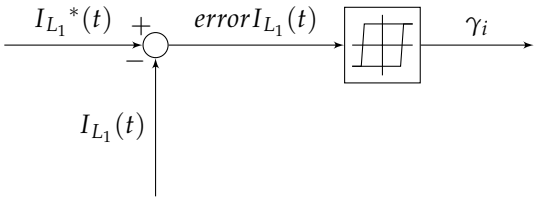

Figure 2. Inverter control block diagram

THD is calculated by (1), where I_{50Hz} is the pretended grid's current and $I_{n^{th}_{sw}}$ is the n^{th} harmonic of the ripple current which is due to the current hysteresis control window. Although choosing a very small hysteresis error window width would result in a low THD, it would require a very high switching frequency or a very large filter inductor. So there's a trade-off between to minimizing the THD, keeping the switching frequency within feasible values to limit the switching losses and maintaining the inductor with a compact size, [7].

$$THD = \frac{\sqrt{\sum_{n=1}^{\infty} I^2_{n^{th}_{sw}}}}{I_{50Hz}} \tag{1}$$

To summarize, the semiconductor's maximum switching frequency and the need to maintain THD low by keeping the current hysteresis window small obligates a certain inductance value for L_1.

Since this work is applied for telecom energy storage systems, and this usually happens at low DC voltages (typically 48V), a 3kVA single phase transformer is used for grid connection. This transformer has a short circuit inductance that combined with the grid's inductance represents the second inductor on the LCL filter, L_2.

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It's then possible to obtain a 3rd order filter by adding a capacitor, with value C, between the inductors and the grid. LCL filter's natural frequency, ω_0, is given by (2). It's important to maintain the filter's natural frequency within a tenth of the minimum switching frequency and ten times higher than the grid's frequency (50Hz). In order to be stable, this kind of filters need a damping resistance, usually connected in series with inductor, L_2, or with the capacitor, C. Since the current passing to the grid is large in this application, the choice to use the resistance in series with the capacitor is made. The LCL filter transfer function with the capacitor series resistance is given by (3), where v_i is the full bridge input pulsed voltage to the filter, i_2 is the grid's current on the low voltage side of the transformer, L_1, L_2, C and R_C are the filter parameters shown on Figure 1. These parameters are calculated using (4), (5) and (6). L_2 is measured, it is the short-circuit impedance of the transformer plus the line inductance seen from the low voltage side of the transformer. Table 1 presents the values used for these calculations during this research work.

$$\omega_0 = \sqrt{\frac{L_1 + L_2}{L_1 \cdot L_2 \cdot C}} \tag{2}$$

$$\frac{i_2}{v_i} = \frac{\frac{sR_C C+1}{L_1 L_2 C}}{s\left(s^2 + s\frac{R_C(L_1+L_2)}{L_1 L_2} + \frac{L_1+L_2}{L_1 L_2 C}\right)} \tag{3}$$

$$L_1 = \frac{U_{DC}}{2 \cdot \Delta i_{L_1} \cdot f_{sw}} \tag{4}$$

$$C = \frac{L_1 + L_2}{L_1 L_2 {\omega_0}^2} \tag{5}$$

$$R_C = 2 \cdot \zeta \cdot \omega_0 \cdot \frac{L_1 L_2}{L_1 + L_2} \tag{6}$$

Table 1. Filter Parameters

Parameter	Value
U_{DC}	64V
Δi_{L_1}	6.8A
L_1	48µH
L_2	32µH
C	220µF
R_C	0.45Ω
ω_0	15386 rad/s
ζ	$\sqrt{2}/2$

2.2. Inductor Design

Inductors are of great impact on the size, cost and efficiency of a power converter[6][9]. With the improvements in the semiconductors devices, it's of great importance the effects of higher frequency on the inductor losses. The higher the frequency, higher the inductor core and winding losses[10]. Power inductors aren't exactly off-the-shelf components, each system has its own needs. In this section, it's presented the power inductor design procedure for a prototype application.

The power inductor design starts with the choice of the core material. This should be addressed carefully since there are several materials available and all have their pros and cons, the right choice depends on the design priorities and specifications, [11]. Core suppliers for each specific core give the inductance factor. The inductance is then calculated using (7), where N is the number of wire turns and A_L is the core inductance factor. It's important to note that in cores with gaps, A_L needs to be

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adjusted to include the gap effects, also it's important to take into account the core saturation, which leads to a lower value of inductance.

$$L = N^2 \cdot A_L \tag{7}$$

There are a number of methods to calculate inductor's core loss, some extremely complex and only applicable for certain conditions, [9]. Core suppliers usually make available a set of curves for each material at specific frequencies, with straightforward formulas that can predict the core losses for applications similar to the one treated in this article.

For power inductors, the high-frequency effects on the windings must be taken into account. These high-frequency effects result in extra losses and are due to the skin and proximity effects that are manifested by changing the current density inside the conductor's section, [10,12].

The total winding losses for the application treated in this work is given by (8), where R_{50Hz} is the wire resistance at $50Hz$ that is very close to the DC resistance, I_{50Hz} is the pretended $50Hz$ current on the inductor, $R_{n^{th}sw}$ is the wire resistance for the n^{th} harmonic due to switching frequency, and $I_{n^{th}sw}$ is the n^{th} current harmonic due to switching.

$$P_{winding} = R_{50Hz} I_{50Hz}^2 + \sum_{n=1}^{\infty} R_{n^{th}sw} I_{n^{th}sw}^2 \tag{8}$$

2.3. Phase Locked Loop

A Phase Locked Loop (PLL) is a control system that compares an input signal with a signal generated by a voltage controlled oscillator (VCO) to produce a multiplied, divided or a synchronous signal [8]. This circuit is typically used in frequency demodulators and its block diagram configuration is presented on Figure 4, as described in [8]. For this work, the PLL will be implemented in software in order to obtain a low-cost grid synchronization tool to allow the control of active power and an unity power factor.

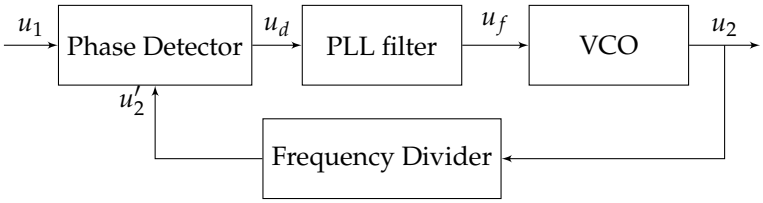

Figure 3. Typical PLL blocks diagram.

As a synchronization application, the frequency divider block isn't applicable since the required input and the output frequencies are the same. This simplification allows Figure 4.

The phase detector block is responsible for giving as output the signal, u_d, which is proportional to the difference between the phases of the input signal, u_1, and the feedback signal, u_2. The PLL filter controls the PLL response. The filter's output signal, U_f, is integrated by the VCO block generating a ramp that symbolizes the grid's phase angle. This output angle signal is also used to generate a sinusoid wave for feedback. This way it's possible to know exactly the grid's phase angle and produce the reference of current needed to control active and reactive power exchange with the grid.

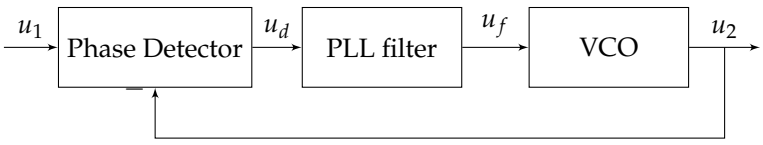

Figure 4. Typical PLL blocks diagram for synchronization applications.

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During the PLL design it is necessary to make the assumption that the PLL is in locked mode, this means that the frequencies of the input signal, ω_1, and feedback signal, ω_2 are the same. This consideration facilitates the multiplication between the squared input signal, u_1 , and the sinusoidal feedback signal u_2, given in (9), where θ_1 is the input signal's phase angle and θ_2 is the feedback signal's phase angle.

$$u_d = \frac{2 \cdot U_1 \cdot U_2}{\pi} \left(\sin\left(\theta_1 - \theta_2\right) + harmonicterms\right) \tag{9}$$

Ignoring the harmonics terms and considering the low difference between the angles, when the PLL is in locked mode, is possible to simplify the $sin(\theta_1 - \theta_2)$ as $\theta_1 - \theta_2$ (10). This simplification is the linearized model of the phase detector where the inputs are the angles (input and feedback) and not the voltage signals, as shown in Figure 5 [13].

From (10) it's possible to obtain the phase detector block gain, k_d , given by (11), [13], where U_1 is the square wave amplitude, and U_2 is the feedback wave amplitude.

$$u_d = \frac{2 \cdot U_1 \cdot U_2}{\pi} (\theta_1 - \theta_2) \tag{10}$$

$$K_d = \frac{2 \cdot U_1 \cdot U_2}{\pi} \tag{11}$$

For the filter block, a proportional–integral filter (PI) is chosen because of its pole on origin which improves angle response[13]. The filters block transfer function is given by (12), where τ_1 and τ_2 are the PI filter parameters. The VCO transfer function is given by (13), being K_0 the VCO gain.

$$\frac{U_f(s)}{U_d(s)} = \frac{1 + s \cdot \tau_2}{\tau_1 \cdot s} \tag{12}$$

$$\frac{K_0}{s} \tag{13}$$

The complete PLL block diagram is shown on Figure 5.

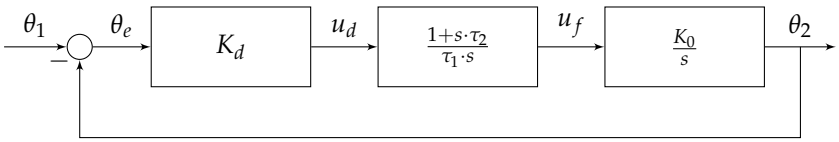

Figure 5. PLL block diagram for design

It's possible to obtain the open loop, $G(s)$, and the closed loop, $\frac{\theta_o(s)}{\theta_i(s)}$, transfer functions, given respectively by (14) and (15).

$$G(s) = K_d \cdot \frac{1 + s \cdot \tau_2}{\tau_1 \cdot s} \cdot \frac{K_0}{s} = \frac{\frac{K_d \cdot K_0 \cdot \tau_2}{\tau_1} \cdot s + \frac{K_d \cdot K_0}{\tau_1}}{s^2} \tag{14}$$

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)} = \frac{\frac{K_d \cdot K_0 \cdot \tau_2}{\tau_1} \cdot s + \frac{K_d \cdot K_0}{\tau_1}}{s^2 + \frac{K_d \cdot K_0 \cdot \tau_2}{\tau_1} \cdot s + \frac{K_d \cdot K_0}{\tau_1}} \tag{15}$$

The closed loop transfer function is very similar to a well known equation on systems control theory given by (16), where ζ is the system damping coefficient and ω_n its natural frequency.

$$\frac{2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \tag{16}$$

Comparing the terms from (15) to (16) it's possible to make the assumptions given by (17) and (18).

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$$\frac{K_d \cdot K_0 \cdot \tau_2}{\tau_1} = 2 \cdot \zeta \cdot \omega_n \tag{17}$$

$$\frac{K_d \cdot K_0}{\tau_1} = \omega_n^2 \tag{18}$$

Using $K_0 = 100$, $\zeta = \frac{\sqrt{2}}{2}$, $\omega_n = \frac{2 \cdot \pi \cdot 50}{10}$ (10 AC grid cycles), it's then calculated K_d, τ_1 and τ_2, see Table 2.

Table 2. PLL design parameters

Parameter	Value
ζ	0.707
ω_n	31.415
U_1	1
U_2	1
K_0	100
K_d	0.637
τ_1	0.065
τ_2	0.045

The simulation results obtained using MATLAB® (The MathWorks Inc., Natick, MA, USA) simulation enviroment are presented on Figure 6.

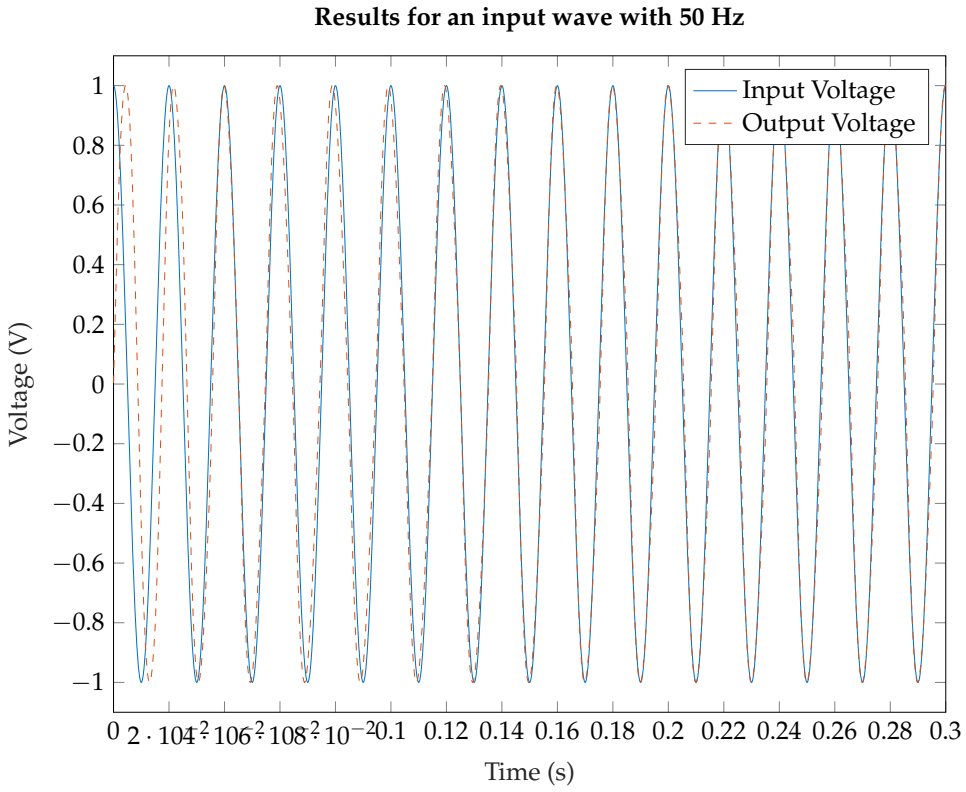

Figure 6. PLL simulation results

The multiplier phase detector has a problem resultant from the multiplication of the two signals (input and feedback), this is the introduction of harmonics in the signal U_d, given in (9) [13]. In order to attenuate these harmonics, it's typically used a complex or heavy computing algorithm as an orthogonal signal generator [14] or a notch filter [15]. The use of notch filter, in this case, is not

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possible because a notch filter is a very tight band rejection filter, this would only reduce one harmonic component, leaving the others. In the case of an orthogonal signal generator, this option needs a very large floating point variables, and with a low-cost FPGA, the variable size and the number of nodes are limited. Because of this, the final implementation was a 2nd order low-pass filter, presented on Figure 7, implemented with two 1st order filters in cascade to reduce the coefficient variable sizes. This filter is applied to the sine wave generated for reference with a cutoff frequency of 50Hz to allow this frequency and block part of the 2nd harmonic (100Hz) and from there on. For convenience, it was implemented an input on the filter's block, θ^*, to enable shifting the output sinusoidal wave, u_{PLL}, in reference to the grid's voltage.

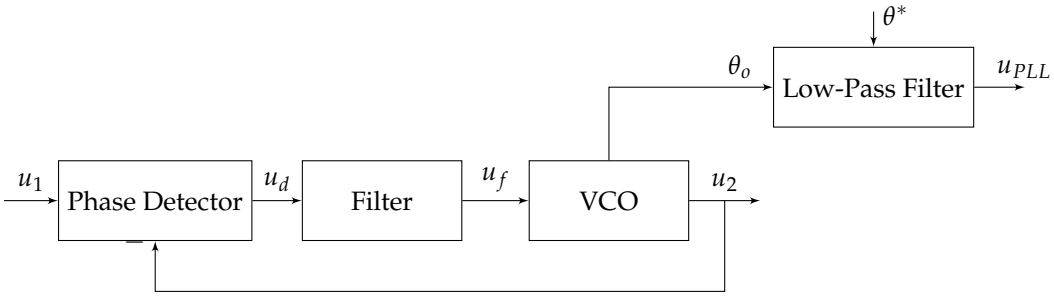

Figure 7. Laboratory implementation in time domain

Discretization

Discretization is the process to transform a continuous transfer function into a discrete transfer function. There are a few discretization methods [16], in this work, the chosen was the trapezoidal integration, the mathematical formulation is given by (19). Applying this transformation the continuous transfer functions are converted into the discrete domain. The PI filter mathematical formulation in this domain is given in (20), where T_s is the sampling time and the b_0,b_1 and a_1 the discrete filter coefficients.

$$s \to \frac{2}{T_s} \cdot \frac{z-1}{z+1} \tag{19}$$

$$\frac{U_f(z)}{U_d(z)} = \frac{b_0 + b_1 \cdot z^{-1}}{1 + a_1 \cdot z^{-1}} = \frac{\frac{(T_s+2\cdot\tau_2)}{2\cdot\tau_1} + \frac{(T_s-2\cdot\tau_2)}{2\cdot\tau_1} \cdot z^{-1}}{1 + (-1) \cdot z^{-1}} \tag{20}$$

For the low-pass filter used to attenuate the unwanted harmonics, applying the same transformation, (21) becomes (22), where ω_c is the filter cutoff frequency.

$$F_{PB}(s) = \frac{\omega_c}{s + \omega_c} \tag{21}$$

$$F_{PB}(z) = \frac{b_0 + b_1 \cdot z^{-1}}{1 + a_1 \cdot z^{-1}} = \frac{\frac{(T_s\cdot\omega_c)}{2+T_s\cdot\omega_c} + \frac{(T_s\cdot\omega_c)}{2+T_s\cdot\omega_c} \cdot z^{-1}}{1 + (\frac{-2+T_s\cdot\omega_c}{2+T_s\cdot\omega_c}) \cdot z^{-1}} \tag{22}$$

The simulation results obtained in the discrete domain are shown on Figure 8.

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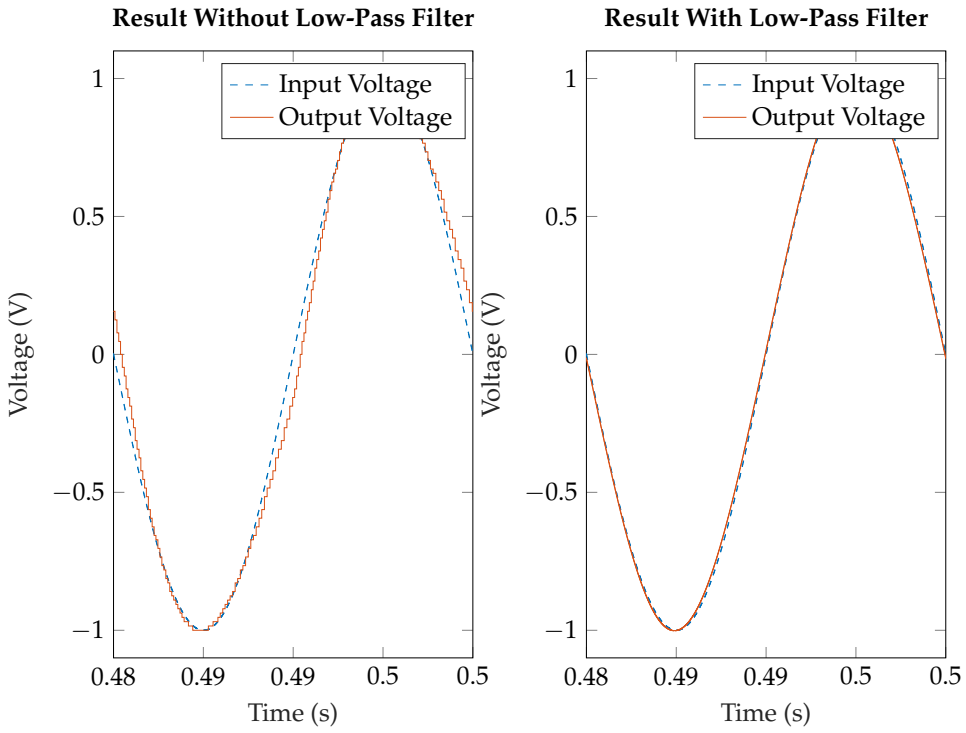

Figure 8. Results for a 50 Hz sinusoidal input waveform (the input voltage showed represents the grid voltage, the PLL see an square waveform in the input)

3. Laboratory Implementation

3.1. Laboratory Setup

A 3kW experimental prototype of the topology proposed is built. This prototype uses 300A SiC MOSFETs capable of switching at 100kHz, which are a few times higher than the Si-IGBTs equivalent, due to lower switching losses, higher output current capability and significantly lower current de-rating at higher switching frequencies. The energy storage is made using Lithium Iron Phosphate (LiFePO4) batteries at 64V of nominal voltage. The objective is to control the power flow between the grid and the battery bank with unity power factor. Figure 10 shows the prototype's power setup, while Figure 11 presents the control electronics setup that uses a low-cost Field Programmable Gate Array (FPGA), Spartan® 3 (Xilinx Inc., San Jose, CA, USA). Table 3 presents the components specifications used in the prototype.

Table 3. Devices Specifications

Component	Brand	Main Specs
SiC Mosfets	Cree	300A, 1200V, 100kHz
Battery Bank	Calb	64V, LiFePo4
Transformer	n/a	$32V_{RMS} - 230V_{RMS}$, $L_2 = 32\mu H$
Inductor	Core from Magnetics Inc.	$48\mu H$
Capacitors	CDE Cornell Dubilier	$220\mu F$
Resistors	n/a	0.45Ω
Current Sensor	LEM	$200A_{peak}$, DC $100kHz$
FPGA	Xilinx	Spartan 3, 125MHz

According to (2) and Table 3, The filter's natural frequency is $2450Hz$ and its Bode Diagram is given on Figure 9.

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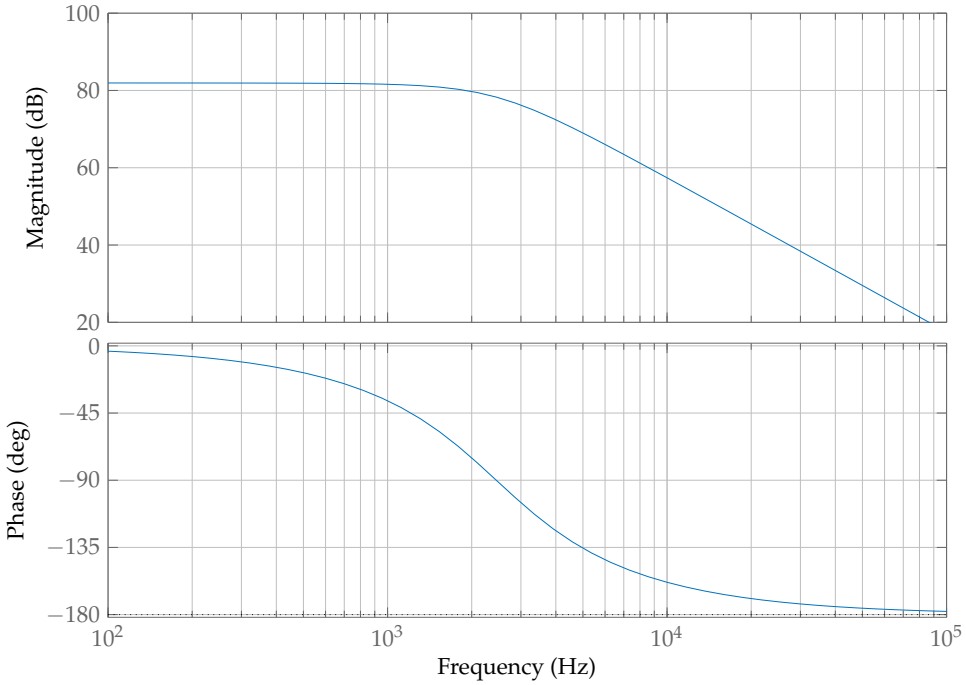

Figure 9. Filter LCL

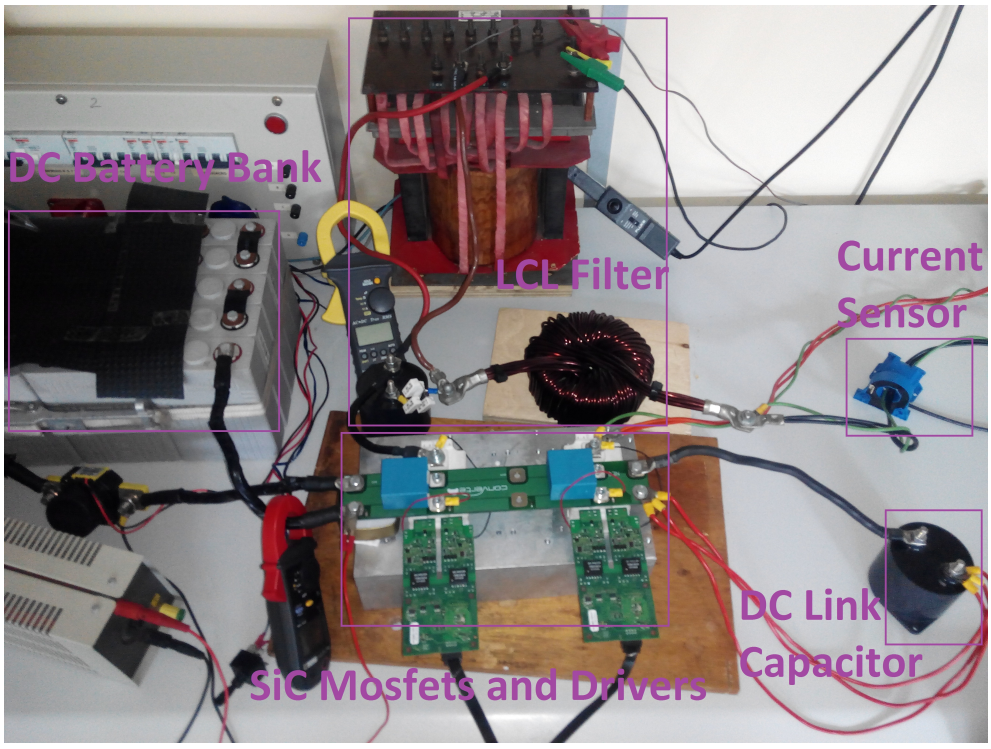

Figure 10. Single-phase SiC bidirectional DC-AC converter power circuit.

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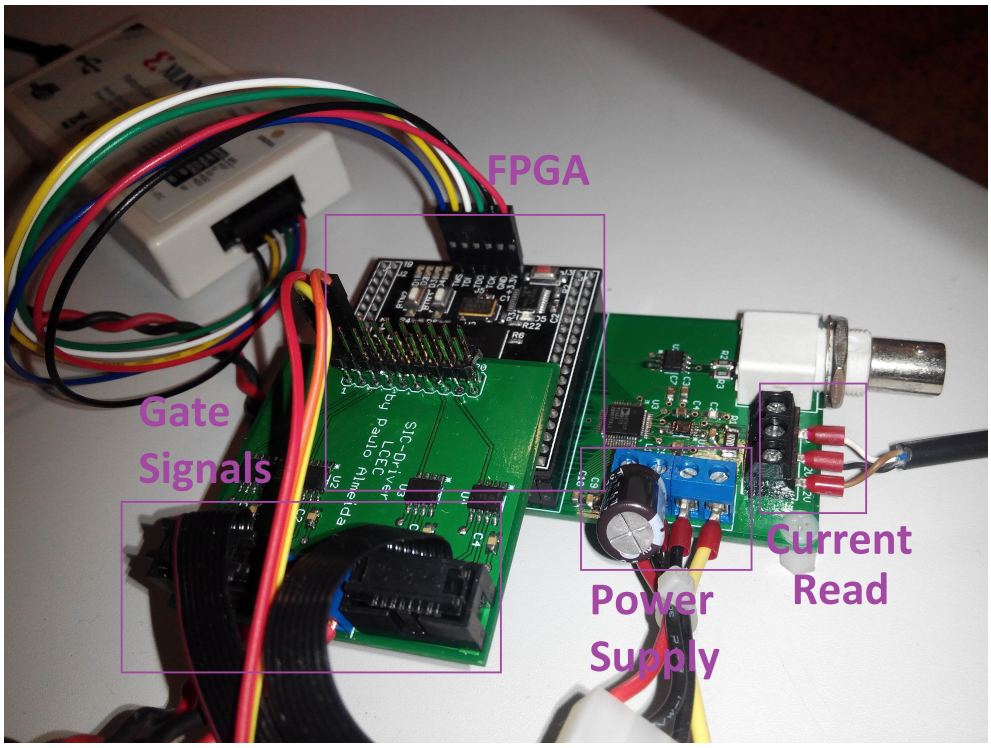

Figure 11. Data acquisition, processing and output generation setup.

3.2. Phase Locked Loop Implementation

For this research work, it's was given importance to build a low-cost PLL to synchronize with the grid, but also it was taken into the possibility the use of this PLL to synchronize with different types of waveforms, such as the square and sinusoidal waveforms for future works. Therefore, the multiplier phase detector block was selected and it can be adapted to different waveforms just by adjusting the gains, [13]. Since the integrated circuit used as processor in this work is a FPGA, all the PLL components are implemented in software and just the AC grid voltage was converted into a square wave with the circuit shown on Figure 12. This way the FPGA receives a binary signal that is zero when the grids voltage is positive and one when grids voltage is negative. Note that this signal is isolated by an optocoupler to prevent damaging the FPGA and keep the circuit's cost low. This signal after processing is transformed in signal u_1 seen in Figure 7.

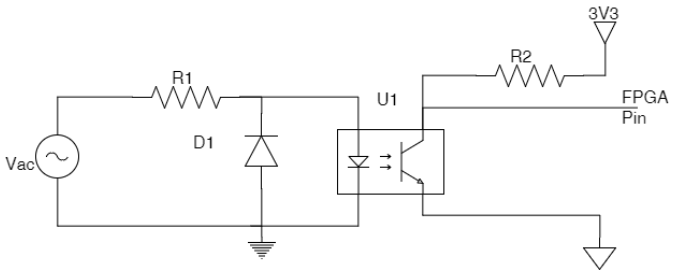

Figure 12. Implemented circuit to detect positive grid voltage.

3.3. Laboratory Results

The experimental results were taken at 2kW and 3kW charging the batteries, see Figures 13 and 14, and then injecting energy on the grid, see Figures 15 and 16. On these experimental results, the current signal is given by channel 4, while the voltage grid is given by channel 1(at the secondary side of the transformer, $32V_{RMS}$). Although the current waveform at 2kW has a bigger THD than

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operating at 3kW, that is expected because the current at grid frequency is lower, while the ripple stays the same, the THD still is less than 5% fulfilling the network requirements.

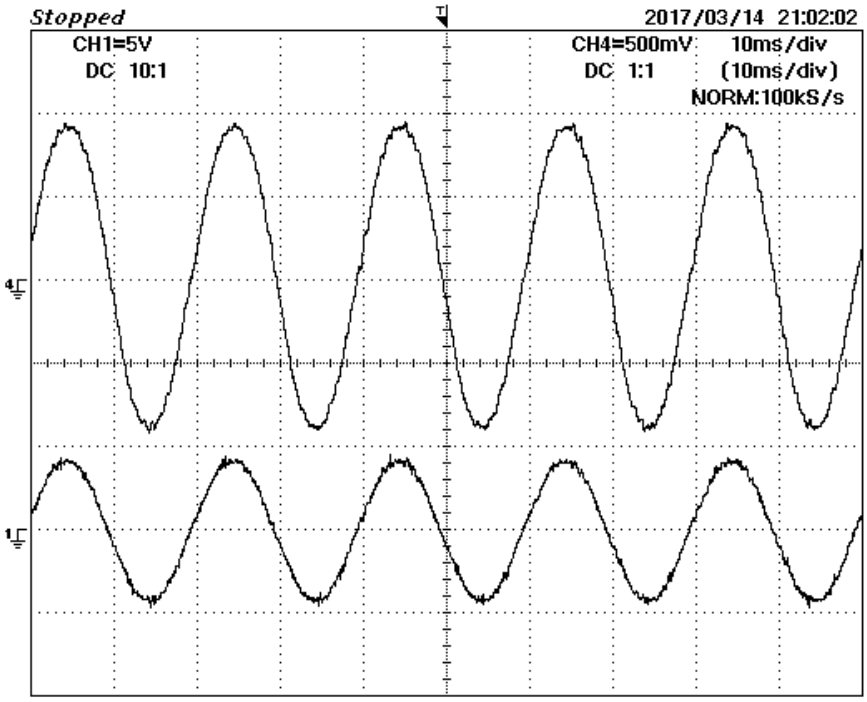

Figure 13. Experimental results charging the batteries at 2kW on transformer secundary side ($32V_{RMS}$ side). CH1: Grid Voltage ($50V/div$); CH4: Grid Current ($50A/div$).

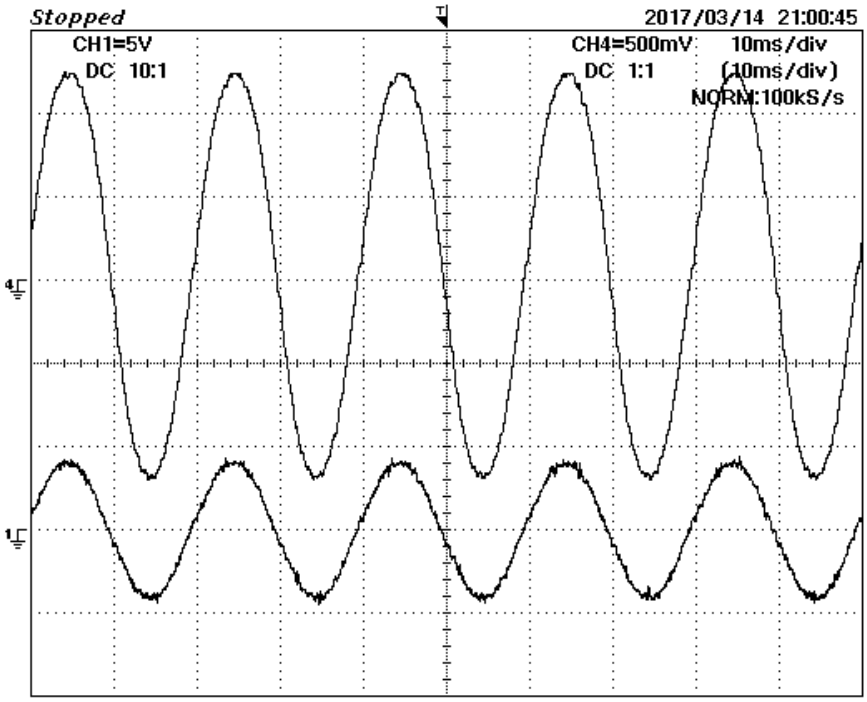

Figure 14. Experimental results charging the batteries at 3kW on transformer secundary side ($32V_{RMS}$ side). CH1: Grid Voltage ($50V/div$); CH4: Grid Current ($50A/div$).

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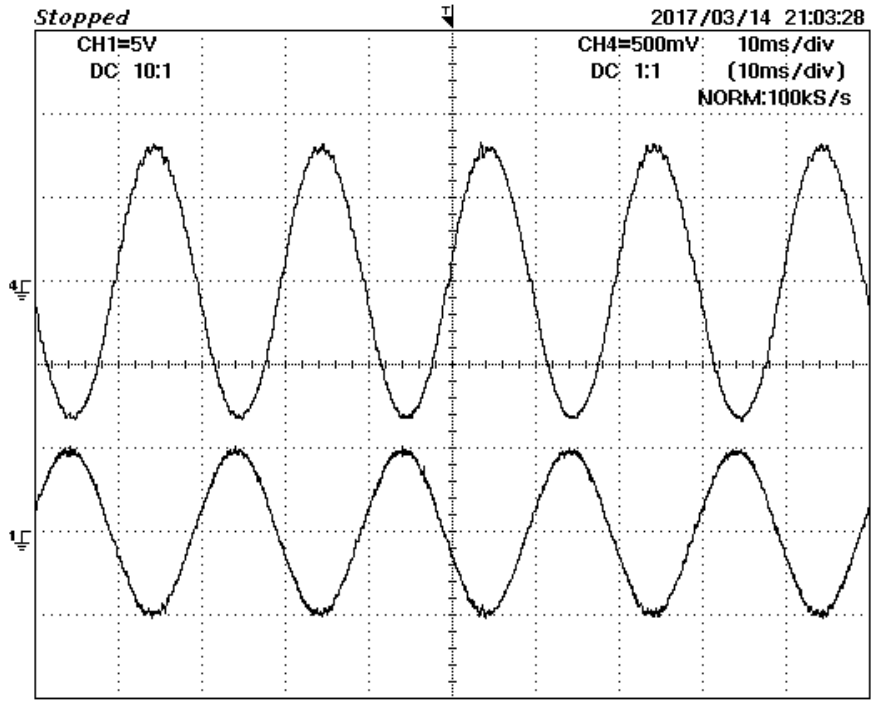

Figure 15. Experimental results injecting 2kW on transformer secundary side ($32V_{RMS}$ side). CH1: Grid Voltage ($50V/div$); CH4: Grid Current ($50A/div$).

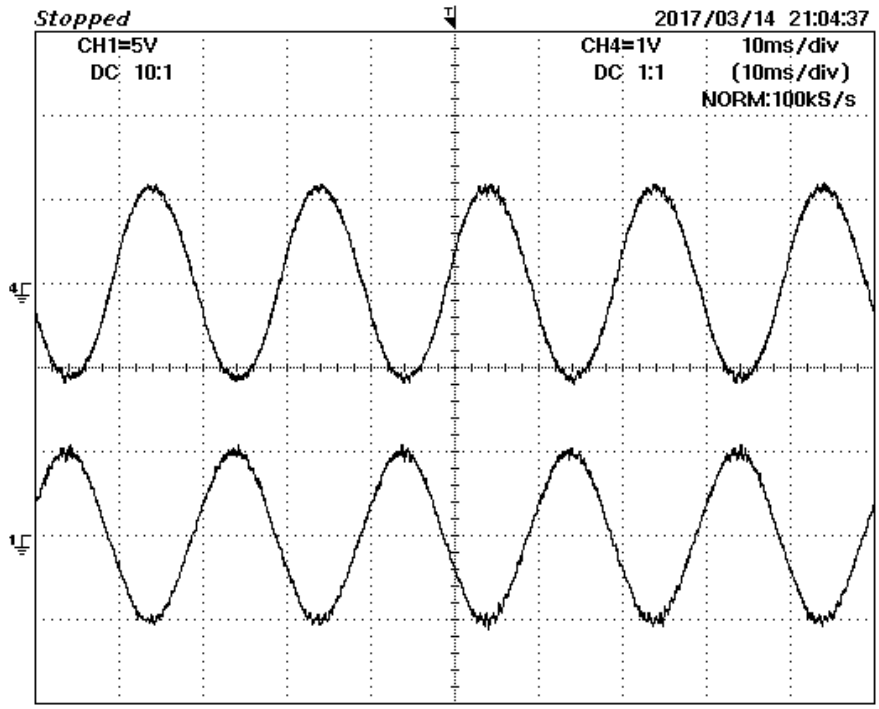

Figure 16. Experimental results injecting 3kW on transformer secundary side ($32V_{RMS}$ side). CH1: Grid Voltage ($50V/div$); CH4: Grid Current ($100A/div$).

4. Conclusions

This paper presented the implementation and control of a DC-AC converter with unity power factor with a brief description of inductor design, LCL filter and phase locked loop theory for grid synchronization. It has been introduced the control principles for a variable switching frequency converter and the trade-offs that must be done between system efficiency, filter size and cost while still accomplish the THD limits imposed by legislation. A Converter prototype was built on laboratory, connected to the grid through a $32V_{RMS}$ to $230V_{RMS}$ transformer. Laboratory results have been obtained charging the batteries and injecting power on the grid at 2kW and 3kW which correspond to high currents due to the low voltage level. The measured currents presented THD below 5%, therefore meeting the standard requirement.

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Author Contributions: Alexandre Bento design and build the LCL filter, build the single-phase SiC bidirectional DC-AC converter, performed the experiments, analyzed the data and wrote the major part of the manuscript. Sérgio André built the PLL circuit, performed its low-level FPGA programming and wrote about the low-cost PLL. Ricardo Luís helped in the high-level FPGA programming and in the experiments. José Fernando Silva supervised the research, providing guidance and key suggestions. All the authors revised and approved the publication of the paper.

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