Realization of Integrable Low-Voltage Companding Filters for Portable System Applications

THESIS

Submitted to

University of Kashmir

In partial fulfillment of the requirements for the award of the degree of

DOCTOR OF PHILOSOPHY

In

ELECTRONICS

By

FAROOQ AHMAD KHANDAY

Under the Supervision of

Prof. N. A. SHAH

March 2013

Postgraduate Department of Electronics and Instrumentation Technology

University of Kashmir

Abstract

Undoubtedly, today's integrated electronic systems owe their remarkable performance primarily to the rapid advancements of digital technology since 1970s. The various important advantages of digital circuits are: its abstraction from the physical details of the actual circuit implementation, its comparative insensitiveness to variations in the manufacturing process, and the operating conditions besides allowing functional complexity that would not be possible using analog technology. As a result, digital circuits usually offer a more robust behaviour than their analog counterparts, though often with area, power and speed drawbacks. Due to these and other benefits, analog functionality has increasingly been replaced by digital implementations.

In spite of the advantages discussed above, analog components are far from obsolete and continue to be key components of modern electronic systems. There is a definite trend toward persistent and ubiquitous use of analog electronic circuits in day-to-day life. Portable electronic gadgets, wireless communications and the widespread application of RF tags are just a few examples of contemporary developments. While all of these electronic systems are based on digital circuitry, they heavily rely on analog components as interfaces to the real world. In fact, many modern designs combine powerful digital systems and complementary analog components on a single chip for cost and reliability reasons. Unfortunately, the design of such systems-on-chip (SOC) suffers from the vastly different design styles of analog and digital components. While mature synthesis tools are readily available for digital designs, there is hardly any such support for analog designers apart from well-established PSPICE-like circuit simulators. Consequently, though the analog part usually occupies only a small fraction of the entire die area of an SOC, but its design often constitutes a major bottleneck within the entire development process.

Integrated continuous-time active filters are the class of continuous-time or analog circuits which are used in various applications like channel selection in radios, anti-aliasing before sampling, and hearing aids etc. One of the figures of merit of a filter is the dynamic range; this is the ratio of the largest to the smallest signal that can be applied at the input of the filter while maintaining certain specified performance. The dynamic range required in the filter varies with the application and is decided by the variation in strength of the desired signal as well as that of unwanted signals that

are to be rejected by the filter. It is well known that the power dissipation and the capacitor area of an integrated active filter increases in proportion to its dynamic range. This situation is incompatible with the needs of integrated systems, especially battery operated ones. In addition to this fundamental dependence of power dissipation on dynamic range, the design of integrated active filters is further complicated by the reduction of supply voltage of integrated circuits imposed by the scaling down of technologies to attain twin objective of higher speed and lower power consumption in digital circuits. The reduction in power consumption with decreasing supply voltage does not apply to analog circuits. In fact, considerable innovation is required with a reduced supply voltage even to avoid increasing power consumption for a given signal to noise ratio (S/N). These aspects pose a great hurdle to the active filter designer.

A technique which has attracted the attention of circuit designers as a possible route to filters with higher dynamic range per unit power consumption is "companding". Companding (compression-expansion) filters are a very promising subclass of continuous-time analog filters, where the input (linear) signal is initially compressed before it will be handled by the core (non-linear) system. In order to preserve the linear operation of the whole system, the non-linear signal produced by the core system is converted back to a linear output signal by employing an appropriate output stage. The required compression and expansion operations are performed by employing bipolar transistors in active region or MOS transistors in weak inversion; the systems thus derived are known as logarithmic-domain (log-domain) systems. In case MOS transistors operated in saturation region are employed, the derived structures are known as Square-root domain systems. Finally, the third class of companding filters can also be obtained by employing bipolar transistors in active region or MOS transistors in weak inversion; the derived systems are known as Sinh-domain systems.

During the last several years, a significant research effort has been already carried out in the area of companding circuits. This is due to the fact that their main advantages are the capability for operation in low-voltage environment and large dynamic range originated from their companding nature, electronic tunability of the frequency characteristics, absence of resistors and the potential for operations in varied frequency regions.

Thus, it is obvious that companding filters can be employed for implementing high-performance analog signal processing in diverse frequency ranges. For example, companding filters could be used for realizing subsystems in: xDSL modems, disk drive read channels, biomedical electronics, Bluetooth/ZigBee applications, phase-locked loops, FM stereo demodulator, touch-tone telephone tone decoder and crossover network used in a three-way high-fidelity loudspeaker etc.

A number of design methods for companding filters and their building blocks have been introduced in the literature. Most of the proposed filter structures operate either above 1.5V or under symmetrical (±1.5V) power supplies. According to data that provides information about the near future of semiconductor technology, International Technology Roadmap for Semiconductors (ITRS), in 2013, the supply voltage of digital circuits in 32 nm technology will be 0.5 V. Therefore, the trend for the implementation of analog integrated circuits is the usage of low-voltage building blocks that use a single 0.5-1.5V power supply.

Therefore, the present investigation was primarily concerned with the study and design of low voltage and low power Companding filters. The work includes the study about: the building blocks required in implementing low voltage and low power Companding filters; the techniques used to realize low voltage and low power Companding filters and their various areas of application.

Various novel low voltage and low power Companding filter designs have been developed and studied for their characteristics to be applied in a particular portable area of application. The developed designs include the N-th order universal Companding filter designs, which have been reported first time in the open literature. Further, an endeavor has been made to design Companding filters with orthogonal tuning of performance parameters so that the designs can be simultaneously used for various features. The salient features of each of the developed circuit are described. Electronic tunability is one of the major features of all of the designs. Use of grounded capacitors and resistorless designs in all the cases makes the designs suitable for IC technology. All the designs operate in a low-voltage and low-power environment essential for portable system applications.

Unless specified otherwise, all the investigations on these designs are based on the PSPICE simulations using model parameters of the NR100N bipolar transistors and

BSIM 0.35µm/TSMC 0.25µm /TSMC 0.18µm CMOS process MOS transistors. The performance of each circuit has been validated by comparing the characteristics obtained using simulation with the results present in the open literature.

The proposed designs could not be realized in silicon due to non-availability of foundry facility at the place of study. An effort has already been started to realize some of the designs in silicon and check their applicability in practical circuits. At the basic level, one of the proposed Companding filter designs was implemented using the commercially available transistor array ICs (LM3046N) and was found to verify the theoretical predictions obtained from the simulation results.

Dedicated

To my Parents

CERTIFICATE

This is to certify that Mr. FAROOQ AHMAD KHANDAY has worked under my supervision for the Thesis entitled, "*Realization of Integrable Low-Voltage Companding Filters for Portable System Applications*" and the work is truly commendable of consideration for the award of the degree of Doctor of Philosophy in Electronics.

It is further certified that

(i). The Thesis embodies the work of the candidate.

(ii). The candidate worked under my supervision for the period required under statues.

(iii). The candidate has put in the required attendance in the Department.

(iv). The conduct of the candidate remained very good during the period of the research.

(Prof. N. A. Shah)
Supervisor
Department of Electronics and Instrumentation Technology
University of Kashmir
Srinagar-190006

CANDIDATE'S DECLARATION

I hereby declare that the work presented in this Thesis "*Realization of Integrable Low-Voltage Companding Filters for Portable System Applications*" in partial fulfillment of the requirements for the degree of **Doctor of Philosophy** and submitted in the Department of Electronics and Instrumentation Technology, Faculty of Applied Sciences and Technology, University of Kashmir, Srinagar, has entirely been done by me under the supervision of **Prof. N. A. Shah**.

I, further, declare that the work contained in the thesis is the original research work conducted by me and has not been submitted in part or full, to any other University or Institute for the award of any degree.

(FAROOQ AHMAD KHANDAY)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Prof. N. A. Shah)
Supervisor
Department of Electronics and Instrumentation Technology
University of Kashmir
Srinagar-190006

The Ph. D. Viva-voce examination of Mr. Farooq Ahmad Khanday, Research Scholar, has been held on…….

Supervisor **Head of the Department** **External Examiner**

Acknowledgements

I would like to start by thanking God for giving me the strength to overcome the many difficulties that life has thrown at me, and for making possible many things that seemed at first to be impossible. Next, there are no words to express what I feel towards my family. My father, mother, and sisters have always been there to offer me their love and my brothers have always encouraged and supported me. In addition, I would like to acknowledge people who have contributed to this work and helped me during the whole period of study and research.

The first person I want to thank is my guide, Professor Nisar A. Shah. I want to thank him not only because of his broad knowledge and his profound insights, but also because of his decent, warm, sensitive and caring personality. He gave me a promising and significant research area, strong encouragement and full support. I would like to thank him for his trust and confidence in me and his appreciation of my work.

I wish to present special thanks to Prof. C. Psychalinos, Associate Professor, Patras University, Greece, who gave me a lot of support during the course of my research work. He spent an enormous amount of time to help me to solve the testing problems and work on the circuits.

I wish to thank Prof. M. Mustafa, Dr. M. T. Banday, Mr. S. A. Parah, Dr. J. A. Sheikh, Er. Mueed Hafiz, Er. Rouf-Ul-Alam Bhat, Mr Javeed Iqbal and other faculty members and research scholars for their valuable discussions during the course of the work. Finally, I also thank technicians of the Departmental Laboratories for supporting the work.

(FAROOQ AHMAD KHANDAY)

KU, March 2013

CONTENTS

TABLE OF CONTENTS *Page No.*

TABLE OF CONTENTS *Page No.*

TABLE OF CONTENTS ***Page No.***

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF TABLES

LIST OF TABLES

NOMENCLATURE

AC	Alternating Current
A/D	Analog to Digital
AIC	Analog Integrated Circuit
ANN	Artificial Neural Networks
AP	Allpass
BE	Base Emitter
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BP	Band Pass
BS/BR	Band Stop/Band Reject
BSIM	Berkeley Short-Channel IGFET Model
BTL	Bipolar Translinear Loop
BW	Bandwidth
C	Capacitance
CCII	Current Conveyor Second Generation
CW	Clockwise
CCW	Counter-clockwise
CFA	Current Feedback Amplifier
CM	Current Mode
CMOS	Complementary Metal Oxide
CNN	Cellular Neural Network
D/A	Digital to Analog
dB	Decibel
DC	Direct Current
DR	Dynamic Range
DSP	Digital Signal Processing
E Cell	Exponential Transconductance Cell
E+ Cell	Positive Exponential Transconductance Cell
E- Cell	Negative Exponential Transconductance Cell
EEG	Electro-Encephalography
ELIN	Externally Linear and Internally Nonlinear
EXP	Exponential operator
FBD	Function Block Diagram
FDM	Frequency Domain Multiplexing
FLF	Follow-The-Ladder-Feedback

NOMENCLATURE

FM	Frequency Modulation
FOM	Figure of Merit
FT	Filter Topology
FTFN	Four Terminal Floating Nullor
GHz	Gigahertz (10^9)
GM	Geometric-Mean
G_m-C	Transconductance capacitance
GTL	Generalized Translinear Loop
HP	High Pass
HPN	High Pass Notch
IC	Integrated Circuit
IF	Intermediate-Frequency
IMD3	Third Order Intermodulation Distortion
ITRS	International Technology Roadmap for Semiconductors
I_S	Saturation Current
I-V	Current to Voltage
K	Boltzman's Constant
KCL	Kirchoff's Current Law
kHz	Kilo Hertz
KVL	Kirchoff's Voltage Law
L	Inductance
LC	Inductance Capacitance
LCR	Inductance Capacitance Resistance
LD	Log Domain
LOG	Logarithmic operator
LP	Low Pass
LPN	Low Pass Notch
LT	Linear Transformation
LTI	Linear and Time-Invariant
LV	Low Voltage
m	Modulation Index
MFB	Multifunction Biquad
MFF	Multi-Function Filter
MHz	Megahertz (10^6)
MIMO	Multiple-Input-Multiple-Output

NOMENCLATURE

MISO	Multiple-Input-Single-Output
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSFET-C	Metal Oxide Semiconductor Field Effect Transistor-Capacitance
MTL	MOS Translinear Loop
MV	Mean Variance
mV	Millivolt
mW	MilliWatt
nA	Nano-Ampere
nW	Nano-Watt
OA	Operational Amplifier
OTA	Operational Transconductance Amplifier
P	Power Dissipation
pF	Pico-Farad
PSPICE	Personal Simulation Computer Programme with Integrated Circuits Emphasis
Q	Quality factor
q	Electron Charge
R	Resistance
RC	Resistance Capacitance
RF	Radio Frequency
RL	Resistance Inductance
RLC	Resistance Inductance Capacitance
SC	Sinh-Cosh
SD	Sinh-Domain
S/D	Squarer/Divider
SFG	Signal Flow Graph
Si	Silicon
SIFO	Single-Input-Four-Output
SIMO	Single-Input-Multiple-Output
SINH	Hyperbolic Sin operator
$SINH^{-1}$	Inverse Hyperbolic Sin operator
S/N or SNR	Signal to Noise Ratio
SOC	Systems-On-Chip
SQ	Square operator

NOMENCLATURE

SRD	Square-Root-Domain
SQRT	Square-Root operator
SQRD	Square-Root-Divider
STD	Standard Deviation
T	Temperature
TAM	Trans-Admittance Mode
TDCNN	Temporal-Derivative-Cellular-Neural-Network
TDM	Time Domain Multiplexing
THD	Total Harmonic Distortion
TIM	Trans-Impedance Mode
TL	Translinear loop
TSMC	Taiwan Semiconductor Manufacturing Company
V_{BE}	Base emitter voltage
V_{CC}/V_{DD}	Positive Supply Voltage
V_{CE}	Collector Emitter Voltage
V_{DS}	Drain Source Voltage
V_{EE}/V_{SS}	Negative Supply Voltage
V_{GS}	Gate Source Voltage
V-I	Voltage to Current
VM	Voltage Mode
VOA	Voltage Operational Amplifier
V_T	Thermal Voltage
V_{TH}	Threshold Voltage
VLSI	Very Large Scale Integration
WIMOSFET	Weak Inversion Metal Oxide Semiconductor Field Effect Transistor
W/L	Aspect Ratio of MOSFET
xDSL	Digital Subscriber Line (of any type)
ω_0	Resonant/Pole frequency
^0C	Degree Celcius
μ	Mobility
μA	Micro-Ampere
μm	Micro-Meter

CHAPTER-1

Low-Voltage Low-Power Analog Design

An Introduction

INTRODUCTION

1. 1. State-of-the-Art Low-Voltage Low-Power Analog Design and its Applications

Undoubtedly, the remarkable performance of contemporary integrated electronic systems is attributed to the rapid advancements achieved in digital technology. The main advantage of digital circuit design is its abstraction from the physical details of the actual circuit implementations. Furthermore, digital circuitry is comparatively insensitive to the variations in the manufacturing process and the operating conditions. Consequently, digital circuits frequently offer a more robust behaviour than their analog counterparts, albeit often with area, power and speed drawbacks. Last but not the least, digital designs allow functional complexity that may not be possible in analog technology based circuits. Due to these and other benefits, analog functionality has been increasingly replaced by digital implementations.

In spite of the trends discussed above, analog components are far from obsolete. In fact, a closer look reveals that they are key components of modern electronic systems. There is a definite trend toward pervasive and ubiquitous use of electronic circuits in everyday life. In fact, analog circuits are needed in many VLSI systems such as filters, D/A and A/D converters, voltage comparators, current and voltage amplifiers, etc. Moreover, new applications continue to appear where new analog topologies have to be designed to ensure the trade-off between speed and power requirements. Wearable and Biomedical Electronics, wireless communications and the widespread application of RF tags are just some examples of current developments. While all of these electronic systems are based on digital circuitry, but they heavily rely on analog components as interfaces to the "real", i.e. analog world. In fact, many modern designs combine powerful digital systems and complementary analog systems on a single chip for cost and reliability reasons.

Further, the rapid improvement of circuit functionality has only been possible due to dramatic increase in the achievable integration densities. The corresponding permanent shrinkage of realizable circuit structures, however, is a mixed blessing. While it is desirable from the integration point of view, but it promotes more and more nonlinear physical phenomena which have only had minor impact so far. Therefore, many simplifying assumptions no longer hold, which complicates the

design of electronic circuits. In fact, not only the analog domain is affected, but digital design is also increasingly becoming aware of physical effects.

Therefore, the development of monolithic VLSI technology, has led to renewed interest in analog circuit design, especially concerning integrated circuits. The main aim of analog integrated circuits (AICs) is to satisfy circuit specifications through circuit architectures with the required performance. Thus, the Low-voltage (LV) low-power (LP) AICs design has been the focus of the contemporary research, especially in the areas of portable systems where a low voltage single-cell battery with longer lifetime has to be used. Portable and miniaturized system-on-chip applications exhibit an increasing demand in the microelectronics market and, particularly, in the biomedical field with products such as hearing aids, pacemakers or implantable sensors. System portability usually requires battery supply, except in some special cases such as RF-powered telemetry systems. Unfortunately, battery technologies do not evolve as fast as applications demand, so the combination of battery supply and miniaturization often turns into a low-voltage and/or low-current circuit design problem. In particular, these restrictions affect more drastically the analog part of the whole mixed system-on-chip. As a result, specific analog circuit techniques are needed to cope with such power supply limitations.

A short description of the specific circuit approaches for low-voltage operation is listed below:

Rail-to-Rail includes all strategies oriented to extend the signal voltage range up to the available room between supply rails. Most of them are mainly based on the redesign of the input and output stages in order to increase their linear range **[1-5]**.

Multistage stands for multiple but simple cascaded stages instead of single cascoded structures. Efforts are then focused on their frequency stabilization with nested compensating loops **[6, 7].**

Bulk-Driven strategies make use of the MOSFET local substrate as an active signal terminal to obtain lower equivalent threshold voltages **[8, 9]**.

Supply Multipliers bypass the low-voltage restriction by performing a step-up conversion of supply voltage through charge pumps **[10-17],** typically from 1.5V to 3V.

The said low-voltage techniques have the following drawbacks:

- ✓ All the low-voltage strategies except those using supply multipliers are actually partial solutions since they are addressed mainly to the design of operational amplifiers only.
- ✓ The bulk-driven option is also in opposition to general anti-latch-up rules of any standard CMOS process.
- ✓ Although supply multipliers are the only global and perhaps the most used solution for very low-voltage operation, they need large capacitive components, take an important Si area overhead and exhibit high extra current consumption, which make them not suitable for small package and low-current applications.

In a similar way, the main circuit techniques for low-current consumption applications are enumerated as follows:

Adaptive Biasing is based on non-static current bias to optimize consumption according to signal demands. Bias dynamics are defined either by local positive feedback **[18, 19]** or by feedforward **[20, 21]** controls.

Subthreshold Biasing of classic topologies by operating their MOS transistors in the weak inversion region at very low-current levels **[22].**

In addition to the techniques mentioned above, LV LP AICs have been achieved by substituting traditional voltage-mode techniques by the current-mode techniques, which have the recognized advantage to overcome the gain-bandwidth product limitation. Therefore, many current-mode techniques came into existence and Companding-mode design is one such technique for AICs.

1.2. Active Filter Design: An Introduction

An electric filter is a two port frequency selective network that shapes the spectrum of the input signal in such a manner that desired frequency content is achieved in the output signal. It is used to separate, pass or suppress a group of signals from a mixture of signals. The applications of filters are to eliminate contamination such as noise in communication systems and to separate relevant frequency components from irrelevant frequency components. Filters are also used to detect and demodulate signals in radio and television. Another important application is to band-limit signals before sampling and to convert discrete time signals into

continuous time signals. Filters are also employed for improving quality of audio equipment, conversion of time-domain multiplexed (TDM) signals into frequency domain multiplexed (FDM), speech synthesis, equalization of transmission lines and cables, and numerous other applications.

In the systems that interface with real word, the processed signal would be measured with unwanted noise. A filter is usually used to get rid of the unwanted noise and to reject the surrounding interface. Thus, filters are important blocks for specified frequency of signals and are essential for many applications. They can be used to band-limit signals in wireline and wireless communication systems. These filters operate on continuous-time fashion because the systems interface with real analog world. Fig. 1.1 shows the operating frequency ranges of the filter for various applications.

Integrated filters can in general be classified into two types: Analog and Digital, which in turn can be classified into various types as depicted in Fig. 1.2. The analog filters process the continuous data rather than the digital data for digital filters. The analog filters can be further divided into passive and active filters. The elements of a passive filter are passive which includes resistors, capacitors, inductors, and transformers. Other passive elements like distributed RC components and quartz crystals are also used. On the contrary, active filters include active devices with or without lumped passive components. The active devices can range from single transistors to integrated controlled sources such as Operational Amplifier (OA), and more exotic devices, such as the Operational Transconductance Amplifier (OTA), Current Conveyor (CC) and its variants, Current Feedback Amplifier (CFA), Four Terminal Floating Nullor (FTFN) etc. A large area is required for the construction of passive filter, while active filters are more suited for CMOS technology.

The Active-RC and Switched-Capacitor filters are suitable only for low to medium frequency applications. For high frequencies, the settling problem of amplifiers would affect the filter performance since very wide bandwidth and high unity-gain frequency are hard to achieve. For systems in the GHz range, LC filters are a better choice since the required values of L and C are small. However, Q enhancement is needed for LC filters because of low inductor quality factors. The Gm-C filters, which operate on open loop topology, would be sufficient for low to high frequency range. Thus, the Gm-C architecture can be implemented for various

applications. However, the performance of Gm-C filter is highly dependent on the performance of the transconductor. Another issue is the automatic tuning of circuit pertinent performance factors. The frequency response and the quality factor should be maintained owing to process, supply voltage and temperature variations. Thus, a high performance automatic tuning circuit is required for continuous-time active filters.

1.2.1. Filter Classification

Depending upon the type of separation, filters are classified as Low Pass (LP), High Pass (HP), Band Pass (BP), Band Stop (BS), and Allpass (AP).

Depending upon the "roll off" of magnitude response in the transition band, filters are classified as first order, second order and High-order. The order of a filter is an integer number, which defines the complexity of the filter. In filters, the order of the filter is the highest power of s in denominator of its transfer function. The order of the filter can be estimated from the number of reactive elements it contains. Depending upon the type of filter approximations, filters are classified as Butterworth, Chebyshev-1, Chebyshev-2, Elliptic etc.

Depending upon the nature of input and output signals, filters are classified as Voltage-Mode (VM), Current-Mode (CM), Trans-Impedance Mode (TIM) and Trans-Admittance Mode (TAM).

In order to increase the speed of circuits for analog signal processing and to decrease the supply voltages of integrated circuits, designers devote their attention to the so-called current mode. It means-simply speaking – that the individual circuit elements should interact by means of currents not voltages **[23]**. In this mode of circuit description the input and output are both taken in the current form rather than in voltage form. CM signal processing can be defined as the processing of current signals in an environment where voltage signals are irrelevant in determining circuit performance. This may be the case in which circuits are designed to operate with low impedance nodes such that the voltage swings are small and time constants are short. Choosing low impedance levels, sufficiently small voltages can be achieved with the aim to eliminate the influence of Miller's capacitance and other non-idealities. In CM circuit, current is used as the active variable in preference to voltage, either throughout the whole circuit or only in certain critical areas.

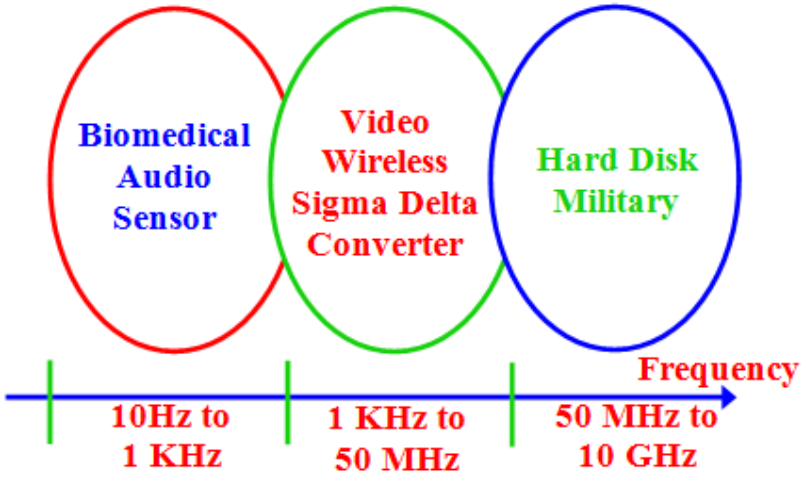


Fig. 1.1: *The operating frequency ranges of filter for various applications.*

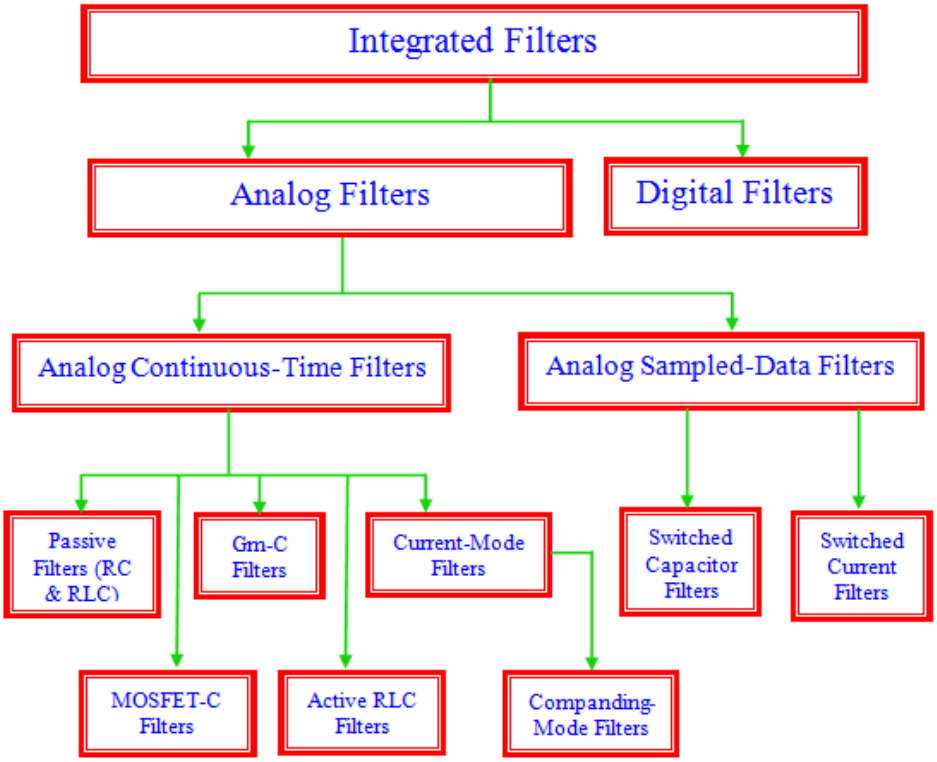


Fig. 1.2: *Classifications of Integrated Filters.*

For many years, electronic engineers seem to have been subconsciously persuaded that the world is voltage dominated; that amps are somehow subservient to volts. In electronic circuit design this is somewhat surprising, since both bipolar and field effect transistors are essentially devices exhibiting controlled output currents. The idea of voltage domination is reinforced by the fact that manufacturers produce a

wide range of integrated amplifiers whose aim is to reproduce a controlled voltage output from a voltage input. Circuits marketed for the purpose of controlling current are much less useful vis-à-vis the performance of a typical integrated transconductance amplifier not withstanding early introduction of 741 OA. This lapse is unfortunate, since experience has shown that current mode circuits synthesized from standard voltage operational amplifiers (VOAs) can produce better system performance than the original VOAs used in an equivalent voltage mode operation.

Recent advances in integrated circuit technologies aimed at state-of-the-art analog IC design are now able to explore the potential of current-mode analog signal processing, providing attractive and elegant solutions for many circuit and system problems. In addition to current conveyors themselves, such circuits range from voltage-to- current converters through translinear circuits and current-mode rectifiers to neural computation and many new amplifier topologies. For many of the applications, current-mode approach enables achievement of superior performance, even in cases where circuits have been synthesized from voltage-mode components due to the lack of suitable alternatives.

The current-mode circuits possess the following potential advantages compared with voltage-mode ones:

A. **Higher bandwidth capability:** bipolar junction transistors and field effect transistors are both current output devices. A key performance feature of the current-mode processing is inherent wide bandwidth and as current amplifier the transistor is useful almost up to its bandwidth f_T. The stray capacitances can be usefully employed as gain element at higher frequencies **[24]**, whereas they limit the bandwidth in voltage-mode circuits.

B. **Higher operating speed:** the shrinking dimensions of integrated circuit techniques lead to circuits whose parasitics are predominately capacitive. Current-mode circuit can achieve high speed signaling at low impedance internal nodes and low voltage swing due to minimal capacitive charging and discharging.

C. **Low circuit complexity for analog arithmetic computations:** in the current domain, computations like addition and subtraction can be performed directly by joining the terminals at a single node. With the current mirror structure, the basic functions of inversion, scaling and summation can be implemented conveniently. In contrast to the voltage-mode counterpart, this needs an operational amplifier for

realizing the same functions. It is clear that current-mode realization possesses low circuit complexity and the possibility of low power consumption.

D. Greater operating dynamic range: as the shrinking device feature size of integrated technology, the supply voltage has to be reduced in order to ensure device reliability. The reduced voltage supply levels result in reduced dynamic range. An attempt to overcome this problem is simply to change the signal representation from a voltage to current. In this way the signal range is no longer directly restricted by the supply voltage but dependent on the impedance level chosen by the designer **[25].**

1. 3. Background and Motivation

Frequency filtering networks are among the most important and widely used electronic devices, with numerous applications in analog, digital, and mixed-signal consumer products. Filters generally fall into three broad categories: fully digital, sampled-data and continuous-time. Digital filters are suited for lower frequency applications and are becoming more and more popular, as they can be easily incorporated inside the DSP core of an integrated circuit. Sampled-data filters use sampling techniques to realize analog filtering. This technique is ideally beneficial for data converters. Sample-data filters usually use MOS technology which allows them to be integrated on the same chip as the digital circuit. Continuous-time filters play an important role in filter design; no other type of filter can be used when dealing with high-frequency, low-voltage systems. Consequently, analog filters have become the most popular choice for the wireless industry.

Integrated continuous-time active filters are the class of continuous-time or analog circuits which are used in various applications like channel selection in radios, anti-aliasing before sampling, and hearing aids etc. One of the figures of merit of a filter is the dynamic range; this is the ratio of the largest to the smallest signal that can be applied at the input of the filter while maintaining certain specified performance. The dynamic range required in the filter varies with the application and is decided by the variation in strength of the desired signal as well as that of unwanted signals that are to be rejected by the filter. It is well known that the power dissipation and the capacitor area of an integrated active filter increases in proportion to its dynamic range **[26]**. This situation is incompatible with the needs of integrated systems,

especially battery operated ones. In addition to this fundamental dependence of power dissipation on dynamic range, the design of integrated active filters is further complicated by the reduction of supply voltage of integrated circuits imposed by the scaling down of technologies to attain twin objective of higher speed and lower power consumption in digital circuits. The reduction in power consumption with decreasing supply voltage does not apply to analog circuits. In fact, considerable innovation is required with a reduced supply voltage even to avoid increasing power consumption for a given signal to noise ratio (S/N). These aspects pose a great hurdle to the active filter designer.

A technique which has attracted attention as a possible route to filters with higher dynamic range per unit power consumption is *companding* **[27, 28].** Traditionally companding has been applied to memoryless systems with a dynamic range limited channel (e.g. in telephony). The key idea is to ensure that the signal in the channel stays sufficiently above noise. To ensure this, pre-amplification is applied. However, it is necessary to avoid overloading the channel as well and for this reason, large signals are pre-amplified by much smaller amounts than small signals. Thus the entire dynamic range of input signals is amplified by appropriate amounts depending on their strength so that they are near the top of the channel's dynamic range. To restore the output of the channel to the original input levels, the opposite, i.e. small gain for small signals and large gain for large signals is applied. Depending on whether the gain is made to depend on the instantaneous value or the average value of the signal, the companding can be called "Instantaneous" or "Syllabic" respectively **[29]**.

Merely substituting a filter in place of the channel with either type of input and output amplifiers described above results in a system that is not linear and time-invariant between its input and output. This general problem of applying companding to filters while maintaining input-output linearity and time-invariance has been solved earlier **[28, 30-32].** Several practical implementations have been published as well. While some of them have significantly improved dynamic range per unit power consumption compared to traditional active filters, it is thought that companding can do much better. It is in fact hoped that companding filters can be realized with lower power consumption per dynamic range than *passive RC/RLC* filters which are

assumed to be operating at the fundamental lower limit **[26]** of power consumption for a given dynamic range.

1.4. History and state of the art of Companding filters

Instantaneous companding has been studied in detail during the last three decades. The earliest form of externally linear and internally nonlinear (ELIN) instantaneous companding filters, dubbed "Log-Domain (LD)" filters due to their use of logarithmic nonlinearity of diodes date back to 1978 **[33]**. The motivation was not companding, but wide tuneability of filter parameters. **[31]** presented a compact realization of first-order LD filters using translinear loops **[34, 35]** and through the use of class-AB circuits for high dynamic range, connected them to the concept of companding filters introduced in **[27]**. To date, LD filters have been the most thoroughly investigated species of companding filters. LD filters received a systematic treatment in **[32]** in which they were shown to be synthesizable using exponential mappings of state variables in the state equations of linear filter prototypes. Since then, several papers dealing with their analysis and synthesis based on the LC ladder simulation **[36, 37]**, one-one substitution or use of new cells **[38, 39]** or analysis of translinear circuits **[40]** have been published. A state space formulation for class-AB LD filters, which are a class of filters capable of large dynamic range, was presented in **[41]**. **[42]** presented a LD filter with syllabic companding. This was however still based on the formulation of **[43]**. **[44]** presented a technique for syllabic companding using dynamic biasing that is unique to LD filters and is much simpler to implement than **[42]**. The potential increase in the dynamic range of syllabically-companding filters was illustrated in **[45]**. **[46]** presented a class-AB LD filter in BiCMOS technology which outperformed most published filters in terms of dynamic range per unit power consumption by a large factor. **[47]** deals with programmable LD filters. The critical issues related with the design of LD filters such transistor Non-idealities and DC stability, are addressed in **[48-52]**. The above are a few examples of the published works in the area of LD filters. LD filters at very high frequencies of hundreds of MHz to a GHz are explored in **[51, 52]**. The field of LD multifunction or universal filter design is almost untouched and is one of the present research trends in the LD design. In **[53]** a 1st-order LD multifunction filter is given. In **[54]**, the micro-power LD universal biquad is discussed. Both methods mentioned above for the

realization of LD multifunction filters cannot be extended to high-order multifunction filters as their cascade leads to single-function filters. In **[55]** a systematic approach is given which can be extended to high-order LD multi-function filter design. In **[56]** a MISO LD multifunction filter is given. Besides this, steadfast endeavour is carried out on the realization of high-order LD filters **[57, 58]**, high-order multifunctional filter design and improved building blocks **[59, 60].** In **[61-63]** high-order multifunctional filter design is given.

The concept of "*LD filtering*" has been extended to the MOS transistors in weak-inversion, due the fact that a similar I–V exponential relationship holds. A number of *LD filter* realizations using MOS transistors have been presented in the literature. This is achieved by a direct transformation of the corresponding implementations based on bipolar transistors, into MOS transistors realizations using component-to-component substitution **[64]**. The main drawbacks of these topologies are the increased effect of transistor mismatches and the limited speed of operation, both originated from the operation mode of the MOS transistor. In order to overcome the above imperfections a new subclass of translinear filters, named "*Square-Root-Domain (SRD) filters*," was introduced. In this case, the main concept is based on the well-known quadratic I–V relationship for the MOS transistor operated in saturation and on the MOS translinear principle. A number of SRD circuits, including integrators, oscillators, etc., were presented in the literature **[65]–[71]**. Second-order SRD lowpass and/or bandpass filter topologies have been already published in the open literature **[70, 72–76].** Besides, a novel n-th order follow-the-leader feedback (FLF) SRD filter topology is introduced in **[77]**.

The final class of instantaneous companding filters is called Sinh-Domain (SD) filter obtained through the inverse of the hyperbolic sine function realized by translinear loops formed by bipolar transistors in active region or MOS transistors in weak inversion. SD filtering is an important technique for realizing analog filters with inherent class-AB nature. This is originated from the fact that the required current splitting is simultaneously realized with the compression of the linear input current and its conversion into a non-liner voltage. This is not the case in the LD filters, where a pseudo class-AB operation is realized by establishing two identical class-AB signal paths and employing a current splitter at the input of the whole filter. The produced intermediate output currents are then subtracted in order to derive the final

output of the filter. Besides, SD filtering offers the benefits of companding circuits like electronic adjustment of their frequency characteristics because the realized time-constants are controlled by a dc current and capability of operation under a low-voltage environment. Compared with their corresponding LD and SRD counterparts, SD offer more power efficient filter realizations but price that may be paid is an increased circuit complexity **[32, 78-85]**.

1.5. Companding filter design for portable system applications

With the inception of companding filters, researchers continuously worked on their applications and the endeavor is still in vogue. Since from the last two decades, there is an incredible attraction towards portable system applications, the companding filters were driven by the same force and a number of companding filter applications for the portable systems came into existence. The companding filters work on the compression-expansion principle and the compression/expansion operators are Log/Exponential or Square-root/Square or $Sinh^{-1}$/Sinh provided by either the BJTs operating in active region or MOSFETs operating in weak inversion or saturation regions. So, the exactness of the companding filters is restricted to that of the compression-expansion operators. Unfortunately, the I-V relationships corresponding to the compression-expansion operators of the mentioned devices remain valid for low (SRD/SD) to high (LD/SD) frequencies only. However, the companding filters found many applications in the said frequency range. Towards this end, the companding filters were effectively used in the Biomedical and low frequency applications **[86-92]**. Mentioning few of them, companding filters were used to: design Cardiac Sense Amplifier for Pacemakers **[93],** circuit which mimics the oscillations observed during the biochemical process of glycolysis due to the phosphor fructokinase enzyme **[94],** gain control circuits and filters for Hearing aids and Cochlear Implant Channels **[83, 95-98].** In addition, companding filters were used to design circuits for: Passive Telemetry **[99],** Electret Microphones **[100],** Audio Filter **[101]** and DECT cordless transmit path applications **[102].** Moreover, companding filters were used in telecommunication applications to reject the undesired image signals, caused by the down-conversion operation in low Intermediate-Frequency (IF) radio transceiver architectures **[103, 104].**

Furthermore, during the last three decades, owing to large application area, a significant amount of research has been carried in the artificial neural networks

(ANNs) and Cellular Neural Networks (CNNs). The key features of neural networks are asynchronous parallel processing, continuous-time dynamics, and global interaction of network elements. Unfortunately, most of these features are not met by their software designs. Therefore, there has been considerable interest in the hardware based designs of ANNs and CNNs **[105, 106].** Towards this end, companding filters were used to give the LV LP designs of Neuron models **[107-110].** Last but not the least, companding filters have been used to design complex Temporal-Derivative-Cellular-Neural-Networks (TDCNNs). TDCNN initiates time derivative 'diffusion' between CNN cells for non-separable spatiotemporal filtering applications, where the input to the CNN is an image that changes over time **[111].**

1.6. Thesis Outline

This thesis will describe the synthesis of low-voltage low-power companding filters and their possible applications in the portable systems. The contents of this work have been organized as follows:

Chapter 1 presents an overview of the low-voltage low-power analog integrated circuits and their applications, context of the work and its motivations.

Chapter 2 presents a review of companding filters. The three main classifications of the companding filters i.e. LD, SRD and SD, are fully discussed. Towards this end, the operators and building blocks required to design three classifications are discussed in detail and the translinear principle used to implement these blocks is also discussed.

Chapter 3 discusses the six techniques used to implement the companding filters. The steps to obtain a companding filter through either of these techniques are discussed in detail. Most of the techniques are concluded with the introduction of the contributions in the various International Journals of repute.

Chapter 4 includes conclusions of the thesis and scope for future work.

CHAPTER-2

Companding Filters

An Introduction

COMPANDING FILTERS

2.1. Introduction

Consumer Electronics industry is driving the IC technology and designers towards low-voltage and low-power technologies, in order to accommodate the strong requirements of portable equipment such as mobile phones, portable computers and so on. This situation is particularly affecting the analog circuitry where the voltage level reduction has a clear impact on the dynamic range of the circuits if traditional architectures and design styles are maintained. Thus, alternative design techniques must be developed in order to cope with all these problems. The other side of the theory is that Analog signal processing can be impaired by 'noise' of various kinds, which can or cannot be random (device noise, power-supply noise, chip substrate noise, etc.). The problem is especially acute in high Q filters, in which high gain paths exist from internal points to the output. Large capacitors and transistors are needed in order to keep thermal and 1/f noise, respectively, at a low level. Thus, trying to design low noise, high Q filters on a small chip area can be a frustrating endeavour.

Current-mode approaches deserve particular mention **[23]** since they provide a large dynamic range for the currents, considered now as processing variables, while maintaining reduced voltage swings, being accompanied by an increase in circuit bandwidth. Another independent, but compatible, approach is given by the so called "Companding". Companding describes the linearization mechanism in which the signals are first compressed to an intermediate integration node and then subsequently expanded after being processed. The distinct characteristic of the technique is that it is the large-signal transfer function of the filter that is linearized, not the individual transconductance or active resistive elements as would be the case in more classical and MOSFET-C based filters. Companding systems thus perform an externally Linear and Time-Invariant (LTI) operation on the signal, even though internally this is not the case; these systems can thus be considered as a particular case of ELIN systems **[28]**.

2.2. Companding techniques

Depending upon how gain is dependent on the signal, we have two special companding techniques as follows:

A. The input amplifier includes nonlinearity whose slope (equivalently, the small signal gain) decreases as the input increases. The output amplifier should have the opposite behaviour. This case, where the output of the amplifier is a nonlinear function of the instantaneous value of the input is termed instantaneous companding.

B. Alternatively, the input and output amplifiers can have characteristics of the form $y = gx$ with a variable gain g. The gain of these amplifiers is made to depend on the input signal. If the gain is made to depend on the instantaneous value of the input signal, this case reduces to instantaneous companding described above. A distinct situation occurs when the gain is made to depend on an average measure of the input signal strength (e.g. the envelope or the root-mean-square value). This case is termed syllabic companding.

Companding in telephony (A-law or μ-law **[29]**) is an example of instantaneous companding. Dolby noise reduction system used in tape recorders is an example of syllabic companding.

Instantaneous companding has been studied in detail and various techniques of instantaneous companding have been reported in the literature. Besides, the companding filtering techniques i.e. "LD", "SRD" and "SD" used in this thesis are all the instantaneous companding techniques.

Before discussing companding filtering techniques in detail, let us first have a brief review of the translinear theory which is the essence of most of the companding filtering circuits**.**

2.2.1. Translinear Principle

The translinear Loop (TL) circuit principle was originally formulated as a practical means of implementing nonlinear signal processing functions by analog circuits designed from bipolar transistors operating in active region or MOSFETs operating in weak inversion region **[32]**. Later on, the concept was extended to the analog circuits designed from MOSFETs operating in saturation region **[65, 112]**. The TL concept applies to devices having transconductance linearly proportional to an electrical variable such as current or voltage. For the class of devices having transconductance linearly proportional to current, we have

$$\frac{dI}{dV} = g = AI \tag{2.1}$$

Integrating, we obtain

$$I = Be^{AV} \tag{2.2}$$

This is the exponential current-voltage characteristic of bipolar transistors operating in active region or MOSFETs operating in weak inversion region with I the Collector/drain current and V the base-emitter/gate-source voltage.

The second class of devices has transconductance linear with voltage. Therefore

$$\frac{dI}{dV} = g = AV \tag{2.3}$$

Again integrating, we obtain

$$I = \frac{A}{2}V^2 + B \tag{2.4}$$

When taking the integration constant B equal to zero, Equation (2.4) represents MOSFETs operating in saturation, with I the drain current and V the gate-source drive voltage "V_{GS} - V_{TH}".

Thus, the generalized translinear Loop (GTL) circuits have inputs and outputs in the form of currents and their primary functions arise from the exploitation of the proportionality of transconductance to an electrical variable in certain electronic devices so as to result in fundamentally exact, temperature-insensitive algebraic transformations. When the electrical variable referred to is a current and the devices are bipolar transistors, the circuits are called Bipolar-Translinear Loop (BTL) circuits. Alternatively, when the electrical variable is a voltage/Current, the devices are MOSFETs operating in saturation/ MOSFETs operating in weak inversion region, the circuits are called MOS translinear Loop (MTL) circuits. Systematic techniques for the analysis and synthesis of TL circuits have been developed **[35]**, **[113]**. Useful applications have been found such as wide-band current amplifiers **[114]**, four-quadrant multipliers **[115]**, triangle-wave-to-sine-wave convertors **[116]**, high-frequency rms-to-dc convertors **[117]**, improved class-AB power output stages **[118]**, and many others **[35]**.

The TL principle has been extended to achieve a wide range of temperature insensitive algebraic functions. To illustrate the principle, we can begin with two

similar examples of BTL and MTL loops given Figs. 2.1 (a) and 2.1(b) respectively. Let us first analyze the loop given in Fig. 2.1 (a), applying Kirchhoff's voltage law around the loop, it follows that

$$\sum_{CW} V_{BE} = \sum_{CCW} V_{BE} \tag{2.5}$$

Where the subscripts cw and ccw indicate the devices connected clockwise and counterclockwise in the loop, respectively.

Using, the exponential I-V relationship of BJT in active region, we can write

$$\sum_{CW} V_T \ln\left(\frac{I_C}{I_S}\right) = \sum_{CCW} V_T \ln\left(\frac{I_C}{I_S}\right) \tag{2.6}$$

In a monolithic process where transistors are implemented in close proximity, it is generally valid to assume equal thermal voltage of all junctions. Therefore, we can write

$$\sum_{CW} \ln\left(\frac{I_C}{I_S}\right) = \sum_{CCW} \ln\left(\frac{I_C}{I_S}\right) \tag{2.7}$$

Rearranging (2.7) results in

$$\prod_{CW}\left(\frac{I_C}{I_S}\right) = \prod_{CCW}\left(\frac{I_C}{I_S}\right) \tag{2.8}$$

Since, "I_S" is the representation of transistor area, (2.8) can also be written as

$$\prod_{CW}\left(\frac{I_C}{A}\right) = \prod_{CCW}\left(\frac{I_C}{A}\right) \tag{2.9}$$

The last equation is called the BTL principle. To summarize, it is re-stated as follows**:**

"For any closed loop comprising any number of pairs of clockwise and counter clockwise forward-biased BJT BE-junctions, the product of currents for the elements in one direction is proportional to the corresponding product in the opposite direction. The factor of proportionality depends solely on the device geometry, and is essentially insensitive to process and temperature variations".

Using the same principle, as an example, the circuit of Fig. 2.2(a) can be used as a squarer divider network with output current given by **[119]**:

$$i_3 = \frac{i_1^2}{i_2} \tag{2.10}$$

Next, Let us analyze the loop given in Fig. 2.1 (b), applying Kirchhoff's voltage law around the loop, it follows that

$$\sum_{CW} V_{GS} = \sum_{CCW} V_{GS} \tag{2.11}$$

Using, the square I-V relationship of MOSFET in saturation (neglecting the effects of mobility reduction and channel length modulation effects), we can write

$$\sum_{CW}\left[V_{TH} + \sqrt{\frac{I_D}{K}}\right] = \sum_{CCW}\left[V_{TH} + \sqrt{\frac{I_D}{K}}\right] \tag{2.12}$$

Where V_{TH} is the threshold voltage and $K = \frac{1}{2}\mu_0 C_{ox}(W/L)$ is the transconductance parameter of MOSFET.

Assuming well-matched threshold voltages (monolithic construction and uniform temperature) and neglecting body effect allows the threshold voltages to be dropped. Also, the parameters μ and C_{ox}, will then be common and can be canceled. Thus (2.12) reduces to

$$\sum_{CW}\sqrt{\frac{I_D}{(W/L)}} = \sum_{CCW}\sqrt{\frac{I_D}{(W/L)}} \tag{2.13}$$

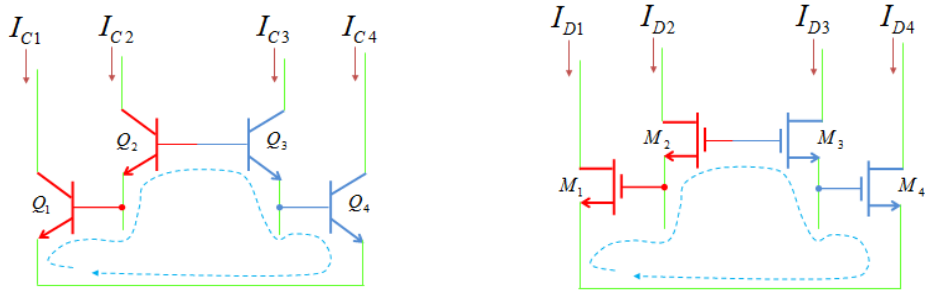
Where W/L is the temperature and process-independent aspect ratio determined by the designer.

The last equation is called the MTL principle. To summarize, it is re-stated as follows**:**

"For any closed loop comprising any number of pairs of clockwise and counter clockwise GS regions of saturated MOSFETs, the sum of root currents for the elements in one direction is proportional to the corresponding sum of root in the opposite direction. The factor of proportionality again depends solely on the device geometry, and is essentially insensitive to process and temperature variations".

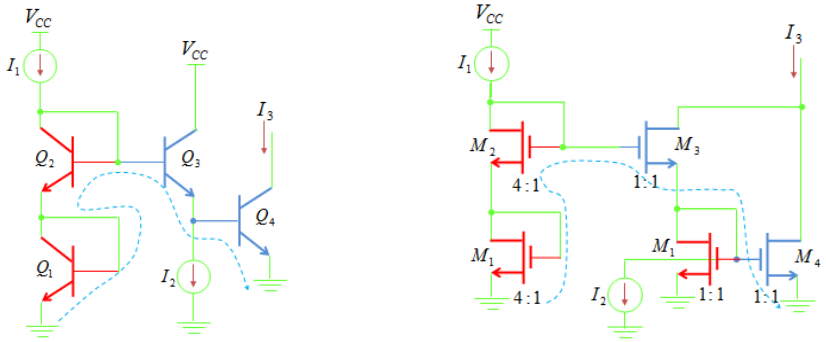
Again, using the same principle, as an example, the circuit of Fig. 2.2(b) can be used as a squarer/divider/multiplier network with output current given by **[65]:**

$$i_3 = \frac{i_1^2 + i_2^2}{2i_2} \tag{2.14}$$



(a) (b)

Fig. 2.1: *Translinear Loops: (a) BTL and (b) MTL.*



(a) (b)

Fig. 2.2: *Translinear Loops implementing useful functions of Squarer/Divider/Multiplier.*

2.3. Companding Filter Techniques

Low-voltage operation and electronic adjustment of frequency characteristics are the current requirement for realizing analog filters and an endeavor of achieving these goals thus gained a significant research effort **[120–125]**. Companding filters are an interesting subclass of analog filters with potential for low-voltage operation and electronic tuning capabilities **[27, 126]**. The main concept of the companding filtering is the following: the linear input current is initially converted to a non-linear compressed voltage and, as a next step, is processed by a companding core. The resulted compressed output voltage is then expanded and simultaneously converted into a linear current. The compression of the input current could be performed by the following ways:

A. through the logarithmic V–I relationship of bipolar transistor in active region or MOS transistor in weak inversion; the derived filters are known in the literature as Log-Domain (LD) filters **[32, 36, 49, 50, 57, 58, 127]**,

B. through the square-root V–I relationship of MOS transistor in strong inversion; the derived filters are known as Square-Root Domain (SRD) filters **[73, 128–130]**, and

C. through the inverse of the hyperbolic sine function realized by translinear loops formed by bipolar transistors in active region or MOS transistors in weak inversion; the derived filters are known as Sinh-Domain (SD) filters **[78, 80, 131, 132]**.

The response of three compression operators corresponding to a shifted sinusoidal waveform is given in Fig, 2.3.

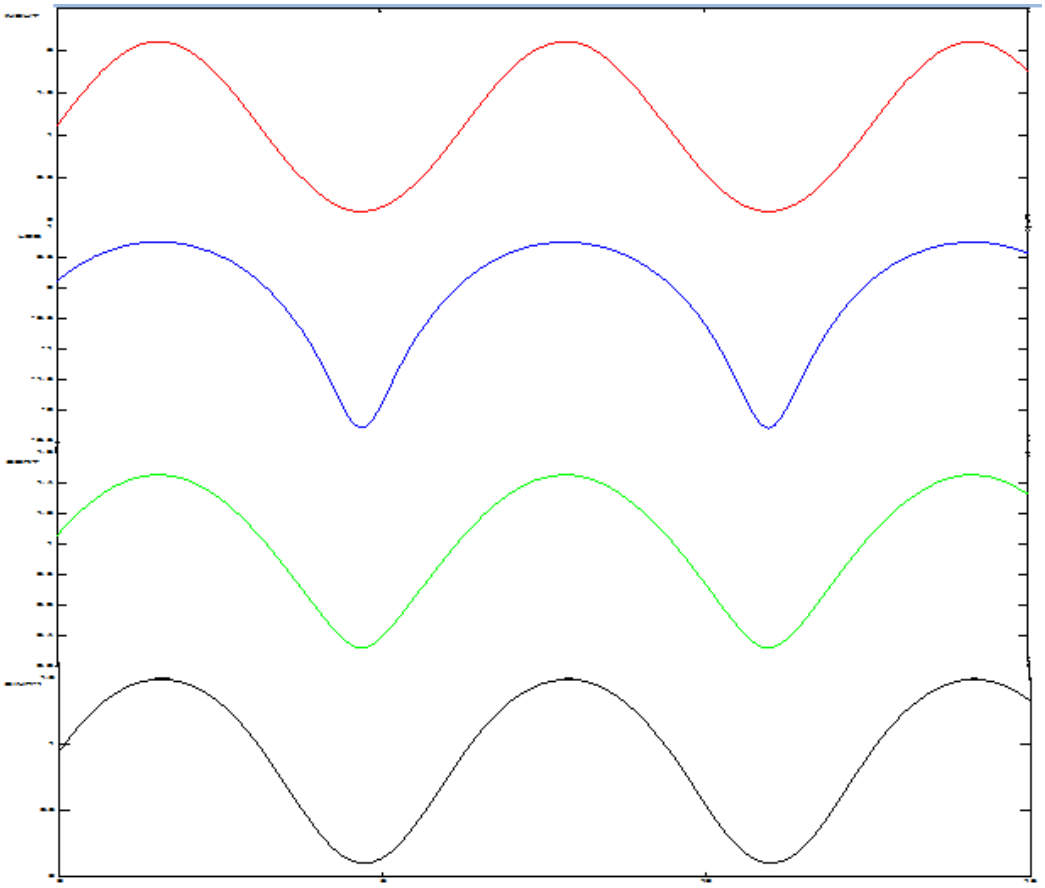


Fig. 2.2: *Response of three compression operators corresponding to a shifted sinusoidal waveform.*

2.3.1. Log-Domain (LD) Filtering

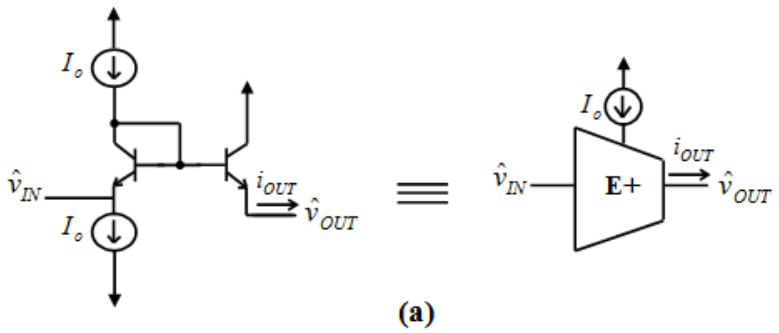
The concept of LD filtering was first introduced in the 1970's **[33]**. LD filters are a particular subclass of instantaneous companding systems that use Logarithmic (LOG) and Exponential (EXP) functions for compression and expansion **[34]** respectively. This makes it possible for LD circuits to operate with very low supply voltage without sacrificing the dynamic range. Also, these filters contain low impedance nodes along the signal path, which can be exploited to achieve greater bandwidths. LD filters are thus receiving interest in literature and substantial progress has been made in simplifying the processes of synthesis and analysis. The basic building blocks of the LD filtering are Log and Exponential operators, Lossy and Lossless Integrators, and, algebraic summation/subtraction blocks. These blocks have been designed using PNP and NPN transistors or NPN transistors alone in the literature. But, most of the proposed filters have been designed using all NPN transistors as they render the filters convenient for monolithic integration. Therefore, only NPN based design of the said blocks will be discussed in the following section.

2.3.1.1. All NPN Transistor Exponential Transconductor Cells

A positive and a negative all NPN transistor exponential transconductor cells (usually named E cells), with their associated symbols, are shown in Figs. 2.4 (a) and (b), respectively. The output current in both topologies is given by **[133]**.

$$i_{out} = I_o . e^{(\hat{v}_{IN} - \hat{v}_{OUT})/V_T} \tag{2.15}$$

Where V_T is the thermal voltage and I_O is a DC current.



(a)

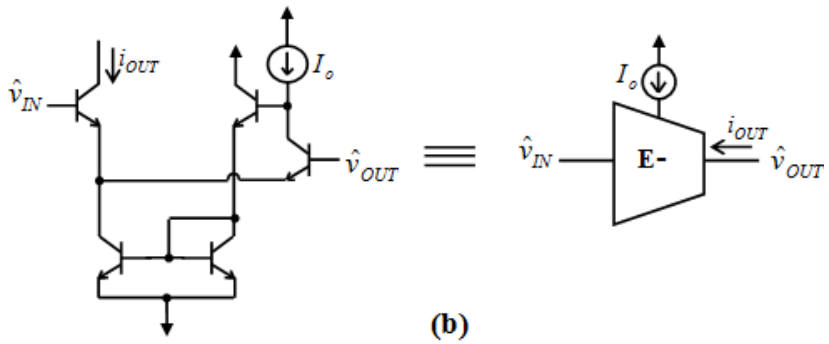


Fig. 2.4: *All NPN transistorized representation of transconductance cells and the symbols used in the Thesis: (a) Positive transconductance cell. (b) Negative transconductance cell.*

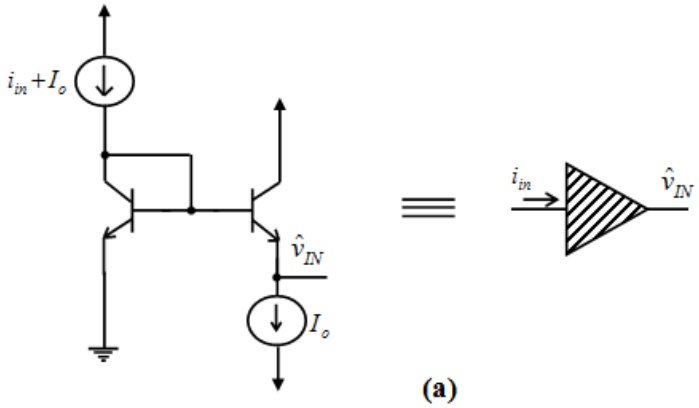
2.3.1.2. LOG and EXP Operators

By employing the E+ cell in Fig. 2.4, the realization of LOG and EXP operators is given in Figs. 2.5 (a) and (b), respectively. The Figs. 2.5 (a) and (b) are described by the following operators respectively **[36].**

$$\hat{v}_{IN} = LOG(i_{in}) \equiv V_T.\ln\left(\frac{i_{in}+I_o}{I_o}\right) \tag{2.16}$$

$$i_{out} = EXP(\hat{v}_{OUT}) \equiv I_o.e^{\hat{v}_{OUT}/V_T} - I_o \tag{2.17}$$

It is worth to note here that the compressed voltages have been marked with a circumflex (^) throughout the thesis.



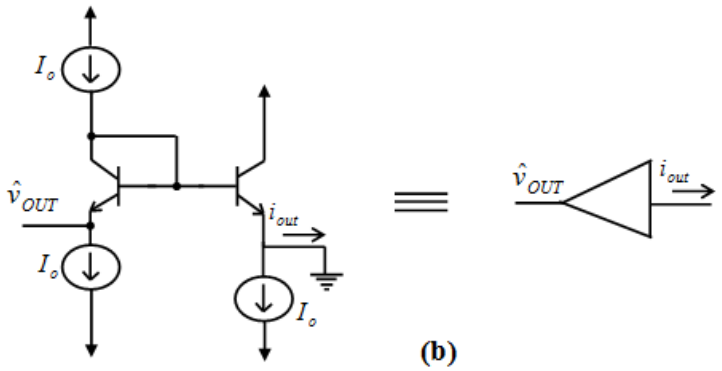


Fig. 2.5: *Realization of the LD operators (a) LOG operator and (b) EXP operator.*

2.3.1.3. LD Integrators

LD integrators are the heart of the LD filtering technique. Combining the two LD cells of Fig. 2.4, and adding a capacitor, the LD two-input integrator (lossless) is formed as shown in Fig. 2.6 (a). Applying KCL at node P, we can write

$$\hat{C}.\frac{d\hat{v}_{OUT}}{dt} = I_o e^{\frac{\hat{v}_{IP}-\hat{v}_{OUT}}{V_T}} - I_o e^{\frac{\hat{v}_{IN}-\hat{v}_{OUT}}{V_T}} \tag{2.18}$$

Where $\hat{v}_{IP}$, $\hat{v}_{IN}$ and $\hat{v}_{OUT}$, denote the LD positive input, negative input, and output, respectively. Multiplying through by $e^{\hat{v}_{OUT}/V_T}$ and applying the chain rule will result in

$$\frac{V_T}{I_o}.\hat{C}.\frac{d}{dt}\left\{I_o e^{\frac{\hat{v}_{OUT}}{V_T}} - I_o\right\} = \left\{I_o e^{\frac{\hat{v}_{IP}}{V_T}} - I_o\right\} - \left\{I_o e^{\frac{\hat{v}_{IN}}{V_T}} - I_o\right\} \tag{2.19}$$

Defining the pair of inverse LOG and *EXP* mappings as given in (2.16) and (2.17), we can rewrite Equation (2.19) as

$$EXP(\hat{v}_{OUT}) = \frac{I_o}{V_T}.\frac{1}{\hat{C}}.\int\{EXP(\hat{v}_{IP}) - EXP(\hat{v}_{IN})\}dt \tag{2.20}$$

There are two points that worth paying attention to: (i) As revealed from (2.20), the bias current I_o can be viewed as to "scale" the capacitor. It is this factor that accounts for the electronic tunability of this integrator and the LD filters. (ii) According to (2.20}, both positive and negative integrators can be obtained by setting negative or positive inputs to ground respectively.

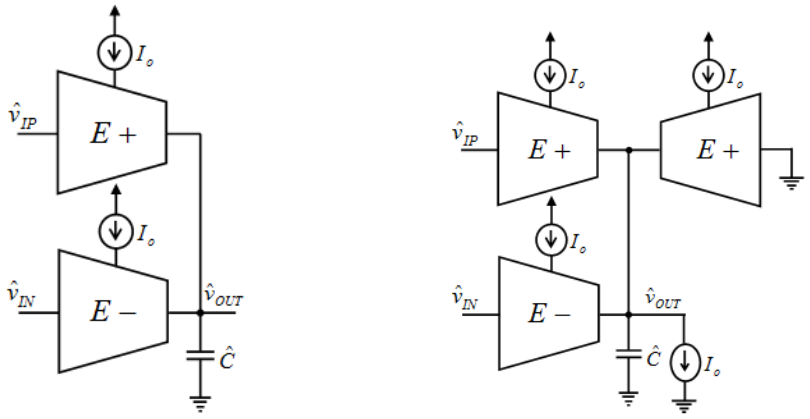


Fig. 2.6: *Exponential transconductor cell representation of: a) two-input lossless integrator. b) two-input damped (lossy) integrator.*

The LD two-input damped (lossy) integrator is shown in Fig. 2.6 (b), where the grounded positive transconductance cell is added to ensure DC stability **[48, 50, 62]**. Following the same procedure, the input-output relationship of the damped integrator can be given as:

$$EXP(\hat{v}_{OUT}) = \frac{I_o}{V_T} \cdot \frac{1}{\hat{C}} \cdot \int \{EXP(\hat{v}_{IP}) - EXP(\hat{v}_{IN}) - EXP(\hat{v}_{OUT})\} dt \tag{2.21}$$

In Laplace domain, the input-output relationships of the LD two-input lossless and lossy integrators can be respectively given by Equations (2.22) and (2.23)

$$\frac{i_{out}}{i_{ip} - i_{in}} = \frac{EXP(\hat{v}_{OUT})}{EXP(\hat{v}_{IP}) - EXP(\hat{v}_{IN})} = \frac{(g_m/\hat{C})}{S} = \frac{1}{S\tau} \tag{2.22}$$

$$\frac{i_{out}}{i_{ip} - i_{in}} = \frac{EXP(\hat{v}_{OUT})}{EXP(\hat{v}_{IP}) - EXP(\hat{v}_{IN})} = \frac{(g_m/\hat{C})}{S + (g_m/\hat{C})} = \frac{1}{S\tau + 1} \tag{2.23}$$

Where $g_m = (I_o/V_T)$, is the transconductance of the exponential cell and $(g_m/\hat{C})$ is the reciprocal of integrator's time-constant.

2.3.1.4. LD Summation/Subtraction Blocks

Also, the required LD amplifier–summer block is presented in Fig. 2.7. Applying KCL at the output node, it is obtained that

$$I_o = a_1 I_o . e^{\frac{(\hat{v}_{IN1}-\hat{v}_{OUT})}{V_T}} + a_2 I_o . e^{\frac{(\hat{v}_{IN2}-\hat{v}_{OUT})}{V_T}} - a_3 I_o . e^{\frac{(\hat{v}_{IN3}-\hat{v}_{OUT})}{V_T}} \tag{2.24}$$

Multiplying both sides of Equation (2.24) with the term $e^{\hat{v}_{OUT}/V_T}$ and after some algebraic manipulation, this can be expressed as follows:

$$\begin{aligned} I_o . e^{\frac{\hat{v}_{OUT}}{V_T}} - I_o = a_1 \left(I_o . e^{\frac{\hat{v}_{IN1}}{V_T}} - I_o \right) + a_2 \left(I_o . e^{\frac{\hat{v}_{IN2}}{V_T}} - I_o \right) \\ - a_3 \left(I_o . e^{\frac{\hat{v}_{IN3}}{V_T}} - I_o \right) + I_o (a_1 + a_2 - a_3 - 1) \end{aligned} \tag{2.25}$$

The last term on the right side of Equation (2.25) leads to DC instability **[48, 50, 62]**. For $a_1 + a_2 = (a_3 + 1)$ and using Equation (2.17), Equation (2.25) can be written as

$$EXP(\hat{v}_{OUT}) = a_1 . EXP(\hat{v}_{IN1}) + a_2 . EXP(\hat{v}_{IN2}) - a_3 . EXP(\hat{v}_{IN3}) \tag{2.26}$$

From Equation (2.26), it is concluded that the circuit in Fig. 2.7 implements a LD Amplifier-Summer/Subtractor.

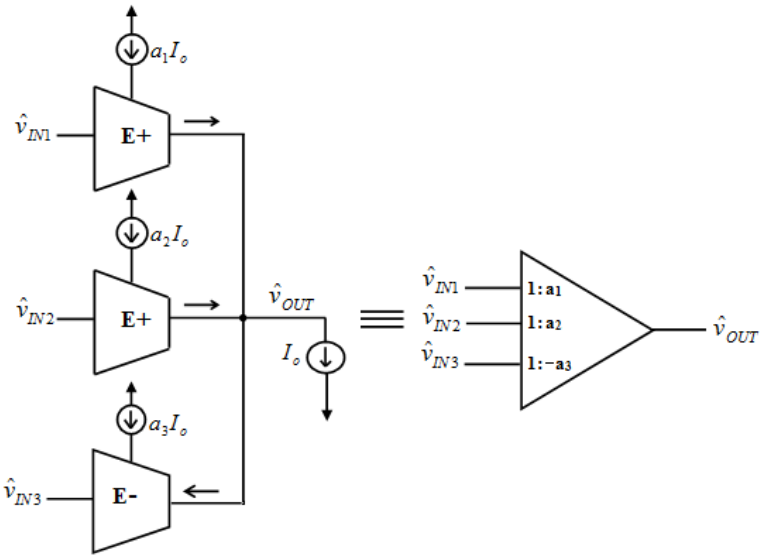


Fig. 2.7: *LD amplifier-Summer/Subtractor and the symbol used in the Thesis.*

2.3.2. Square-Root-Domain (SRD) Filtering

Many researchers, in the recent years, have endeavoured to develop companding circuits which include LD circuits **[50, 52, 55, 57-60, 62, 63, 134].** However, in most of the IC fabrication technologies, owing to the modern trend of digital CMOS processes, the more economical MOSFET implementation of LD circuits is adopted. To meet such demand and change, LD circuits were designed using weak inversion MOSFETs. The circuits, however, are sensitive to threshold voltage matching, and the bandwidth becomes restricted due to its limited operation that is merely within the kHz range. The problems encountered in the above method were solved by using MOS transistors operated in the strong inversion; the resulted circuits are known as SRD circuits, due to the quadrature I-V characteristic of MOS transistor in strong inversion region **[135, 66-70, 73, 75-77, 128-130, 136-139].** SRD filtering is a very attractive technique for realizing continuous-time filters with capability of low-voltage operation and electronic tuning of their frequency characteristics. These benefits are originated from the companding nature of SRD filters and the realization of time-constants by dc currents **[27, 65, 67, 126, 135, 136].** The basic building blocks of the SRD filtering are Square (SQ) and Square-Root (SQRT) operators, Lossy and Lossless Integrators, and, algebraic summation/subtraction blocks. Therefore, SRD design of the said blocks will be discussed in the following section.

2.3.2.1. SRD Operators

Like LD filters, SRD filters are ELIN systems and analogous to Log and EXP operators, the complementary SQ and SQRT operators are used in order to maintain the linear behavior of the whole system. The physical implementation of the SQ and SQRT operators is shown in Figs. 2.8(a) and 2.8(b).

Using the well-known quadratic *I–V* characteristics for the drain current of a MOS transistor, operated in the saturation region, the *SQ* operator of Fig. 2.8(a) is defined as:

$$SQ(\hat{v}) = \frac{K}{2}(\hat{v} - V_{TH})^2 - I_O \tag{2.27}$$

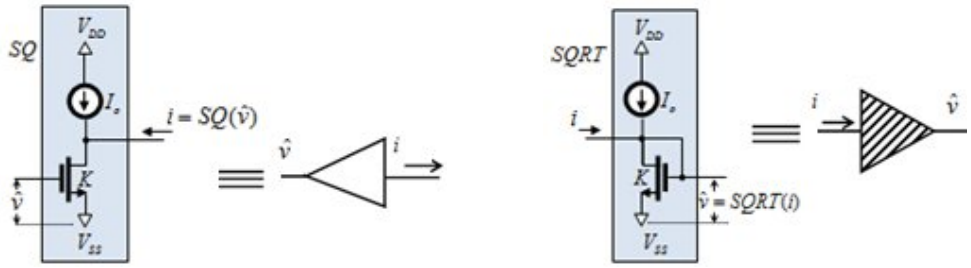
Where SQ ($\hat{v}$) represents a current ***i*** that flows into a MOS transistor, $\hat{v}$ is the gate–source voltage, $K = \mu_o C_{ox}(W/L)$ the transconductance parameter, and V_{TH} the threshold voltage, while I_0 is a constant dc current.

The *SQRT* operator is defined as the inverse of the *SQ* operator and thus

$$SQRT(i) = \sqrt{\frac{2(i + I_O)}{K}} + V_T \tag{2.28}$$

Where SQRT (***i***) represents the gate-source voltage of a diode connected MOS transistor, driven by a current $i + I_0$. The *SQRT* operator can thus be physically implemented using the circuit shown in Fig. 2.8(b).

From equations (2.27) and (2.28), it is obvious that the above operators are complementary i.e. SQ (SQRT (*i*)) = *i*. The functions that describe these operators are basically the traditional quadratic and square root functions, with a few constants added for their physical implementation.



(a) **(b)**

Fig. 2.8: *Realization of the SRD operators. (a) SQ operator. (b) SQRT operator.*

2.3.2.2. SRD Integrators

Unless specified otherwise, integrators have been designed by employing only the Square-Root-Divider (SQRD) block given in Fig. 2.9 **[140, 141]** instead of conventional Geometric-Mean (GM) and squarer/divider (S/D) blocks. The output current of the topology in Fig. 2.9 is given by Equation (2.29) as

$$i_z = \sqrt{\frac{I_0}{i_y}}.i_x \tag{2.29}$$

where I_0 is a dc current. An attractive characteristic of the topology in Fig. 2.9 is that the minimum supply voltage requirement is equal to $V_{TH}+2V_{DS,sat}$, where $V_{DS,sat}$ is the saturation voltage of a MOS transistor. As a result, the proposed SRD filters will be

fully compatible with nowadays' industry demands for systems with low-voltage operation capability. Another benefit is that the realization of SRD integrators using the cell in Fig. 2.9 offers a significant reduction of the circuit complexity in comparison with the corresponding topologies where geometric mean and squarer/divider cells have been utilized **[66-77, 130, 135-141]**.

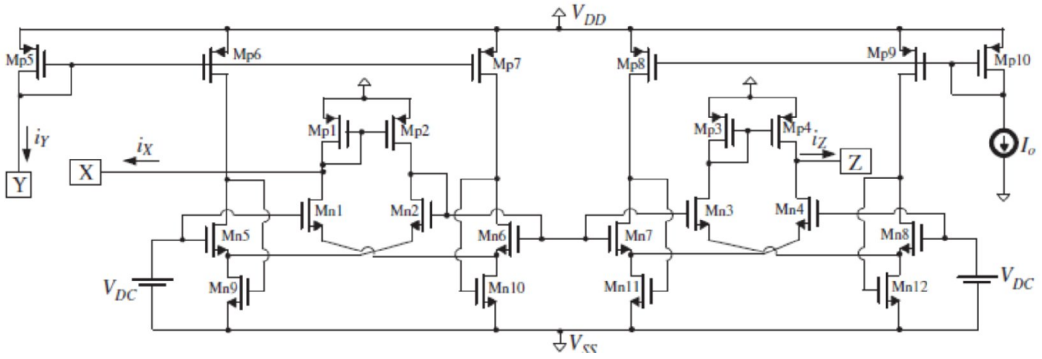


Fig. 2.9: *Square root divider cell **[140, 141].***

A typical configuration of a SRD two-input lossless integrator, constructed from SQRD block is demonstrated in Figure 2.10 (a). The current that flows through the capacitor $\hat{C}$ is given by

$$i_c = \hat{C}\frac{d\hat{v}_{OUT}}{dt} = \sqrt{\frac{I_0}{\frac{K}{2}(\hat{v}_{OUT} - V_{TH})^2}}\left[\frac{K}{2}(\hat{v}_{IP} - V_{TH})^2 - \frac{K}{2}(\hat{v}_{IN2} - V_{TH})^2\right] \tag{2.30}$$

After some algebraic manipulations, (2.30) can be written as

$$\frac{\hat{C}}{\sqrt{2kI_0}}\frac{d\left[\frac{K}{2}(\hat{v}_{OUT} - V_{TH})^2 - I_0\right]}{dt} = \left[\frac{K}{2}(\hat{v}_{IP} - V_{TH})^2 - I_0\right] - \left[\frac{K}{2}(\hat{v}_{IN2} - V_{TH})^2 - I_0\right] \tag{2.31}$$

Defining the pair of inverse SQ and *SQRT* mappings as given in Equations (2.27) and (2.28), we can rewrite Equation (2.31) as

$$\hat{\tau}.\frac{d}{dt}SQ(\hat{v}_{OUT}) = SQ(\hat{v}_{IP}) - SQ(\hat{v}_{IN}) \tag{2.32}$$

Where $\hat{\tau} = \dfrac{\hat{C}}{\sqrt{2kI_0}}$ is the time constant of SRD integrator. Thus, an equivalent resistor with a value $\hat{R} = 1/\sqrt{2kI_0}$ is realized by the SRD integrator which can be

electronically controlled through the dc current I_0. As a result, the realized time-constants in the SRD can be also adjusted through that dc current.

The SRD two-input damped (lossy) integrator is shown in Fig. 2.10 (b). Following the same procedure, the input-output relationship of the damped integrator can be given as:

$$SQ(\hat{v}_{OUT}) = \frac{\sqrt{2kI_0}}{\hat{C}} \cdot \int \{SQ(\hat{v}_{IP}) - SQ(\hat{v}_{IN}) - SQ(\hat{v}_{OUT})\} dt \tag{2.33}$$

In Laplace domain, the input-output relationships of the SRD two-input lossless and lossy integrators can be respectively given by Equations (2.34) and (2.35)

$$\frac{i_{out}}{i_{ip} - i_{in}} = \frac{SQ(\hat{v}_{OUT})}{SQ(\hat{v}_{IP}) - SQ(\hat{v}_{IN})} = \frac{(g_m / \hat{C})}{S} = \frac{1}{S\tau} \tag{2.34}$$

$$\frac{i_{out}}{i_{ip} - i_{in}} = \frac{SQ(\hat{v}_{OUT})}{SQ(\hat{v}_{IP}) - SQ(\hat{v}_{IN})} = \frac{(g_m / \hat{C})}{S + (g_m / \hat{C})} = \frac{1}{S\tau + 1} \tag{2.35}$$

Where $g_m = \sqrt{2kI_0}$, is the transconductance of the SQRD cell and $(g_m / \hat{C})$ is the reciprocal of integrator's time-constant.

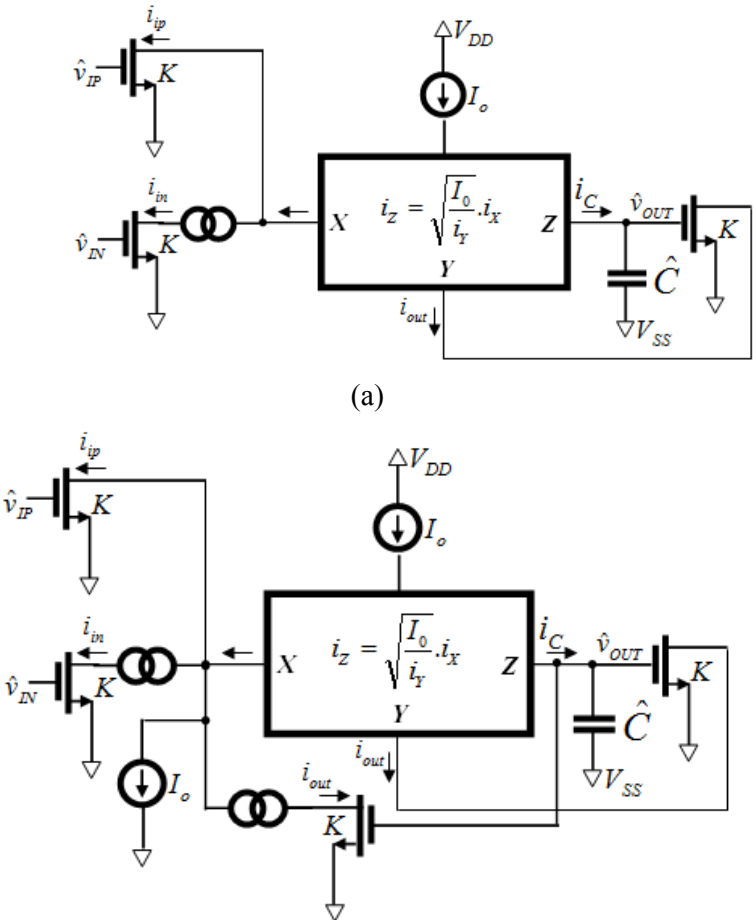
2.3.2.3. SRD Summation/Subtraction Blocks

The realization of an SRD algebraic summation block with a weighted input is that given in Fig. 2.11. Applying the KCL at the output node, it is derived that

$$\frac{K}{2}(\hat{v}_{OUT} - V_{TH})^2 = \frac{K}{2}(\hat{v}_{IN1} - V_{TH})^2 - a\left[\frac{K}{2}(\hat{v}_{IN2} - V_{TH})^2 - I_0\right] \tag{2.36}$$

Using equations (2.27) and (2.36), it is easily derived that

$$SQ(\hat{v}_{OUT}) = SQ(\hat{v}_{IN1}) - a.SQ(\hat{v}_{IN2}) \tag{2.37}$$



(a)

(b)

Fig. 2.10: *SRD Integrators. (a) Two-input SRD lossless integrator. (b)Two-input SRD lossy integrator.*

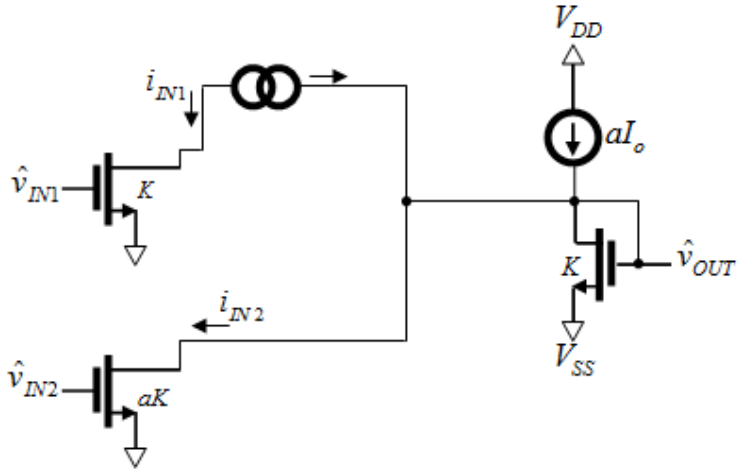


Fig. 2.11: *SRD algebraic summation block with weighted input.*

2.3.3. Sinh-Domain (SD) filtering

Sinh-Domain (SD) filtering is an important technique for realizing analog filters with inherent class-AB nature. This is originated from the fact that the required current splitting is simultaneously realized with the compression of the linear input current and its conversion into a non-liner voltage. This is not the case in the LD filters, where a pseudo class-AB operation is realized by establishing two identical class-AB signal paths and employing a current splitter at the input of the whole filter. The produced intermediate output currents are then subtracted in order to derive the final output of the filter. In addition to the aforementioned feature, SD filters also offer the capability for electronic adjustment of their frequency characteristics because the realized time-constants are controlled by a dc current. Because of the companding nature, SD filters also allow the capability of operation under a low-voltage environment. Compared with their corresponding LD and SRD counterparts, SD offer more power efficient filter realizations but the price paid may be an increased circuit complexity **[32, 78-85]**. Like LD and SRD filtering, the basic building blocks of the SD filtering are Sinh and Sinh^{-1} operators, Lossy and Lossless Integrators, and, algebraic summation/subtraction blocks. Therefore, SD design of the said blocks will be discussed in the following section.

The main building block for designing SD filters is the non-linear Sinh-Cosh (SC) transconductor cell. Since, the proposed SD filters have been designed using BJTs (BiCMOS) in active region and MOSFETs in weak inversion region, both types of designs are discussed here.

2.3.3.1. Weak Inversion MOSFET (WIMOSFET) based SD Filter Design

2.3.3.1.1. WIMOSFET based SD operators

The weak inversion MOSFET (WIMOSFET) based SC cell is given in Fig. 2.12 **[84]**. Utilizing the translinear principle and performing a routine algebraic analysis, it can be easily obtained that the output currents are given by the following equations

$$i_{out1} = 2I_o.\sinh\left(\frac{\hat{v}_{IN}}{U_T}\right) \tag{2.38}$$

$$i_{out2} = 2I_o.\cosh\left(\frac{\hat{v}_{IN}}{U_T}\right) \tag{2.39}$$

Where U_T = n V_T, n is the subthreshold slope factor of a WIMOSFET and V_T is the well known thermal voltage.

The corresponding S cell with an inverted output is shown in Figure 2.12(b).

Using Equation (2.38) and inspecting the topology in Fig. 2.13(a), it is readily obtained that the voltage ($\hat{v}_{IN}$) at its non-grounded terminal is given by Equation (2.40). That is, a linear input current is converted into a compressed voltage. In addition, from the configuration in Fig. 2.13 (b) and the employment of Equation (2.38), it is derived that the expression in Equation (2.41) is realized. In other words, the topology in Fig. 2.13 (b) performs an expansion of a compressed voltage and simultaneously a conversion of it into a linear current. Consequently, the topologies in Fig. 2.13 perform two complementary operations as those described by $SINH^{-1}$ and SINH operators introduced in Equations (2.40) and (2.41), respectively.

$$\hat{v}_{IN} = SINH^{-1}(i_{in}) = U_T.\sinh^{-1}\left(\frac{i_{in}}{2I_o}\right) \tag{2.40}$$

$$i_{out} \equiv SINH\left(\hat{v}_{OUT}\right) = 2I_o.\sinh\left(\frac{\hat{v}_{OUT}}{U_T}\right) \tag{2.41}$$

Another important block that is required for realizing SD filters is two-quadrant multiplier/divider block. A conceptual diagram of a two-quadrant class-AB multiplier/divider block is that depicted in Fig. 2.14(a), whereas in Fig. 2.14 (b) the notation of this block is given. It is constructed from two one-quadrant multipliers **[79]** and an appropriate splitter of the current i_1 in order to achieve a two-quadrant operation. The realization of the multiplier is that shown in Fig. 2.14 (c). The one quadrant multipliers are constructed from transistors M_{n1}–M_{n4} and M_{p1}–M_{p4}, respectively. The translinear loop formed by transistors M_{n5}–M_{n6} and M_{p5}–M_{p6} establishes that the outputs of the splitter are given by the expressions $i_{1p} = \left(i_1 + \sqrt{i_1^2 + 4i_0^2}\right)/2$ and $i_{1n} = \left(-i_1 + \sqrt{i_1^2 + 4i_0^2}\right)/2$. Taking also into account the following condition: i_{1p}–i_{1n} = i_1, it can be easily obtained that the output current is given by the following equation

$$i_{out} = I_o.\frac{i_1}{i_2} \tag{2.42}$$

Using the building blocks presented in this section, the topologies of the corresponding SD integrators will be presented in the following section.

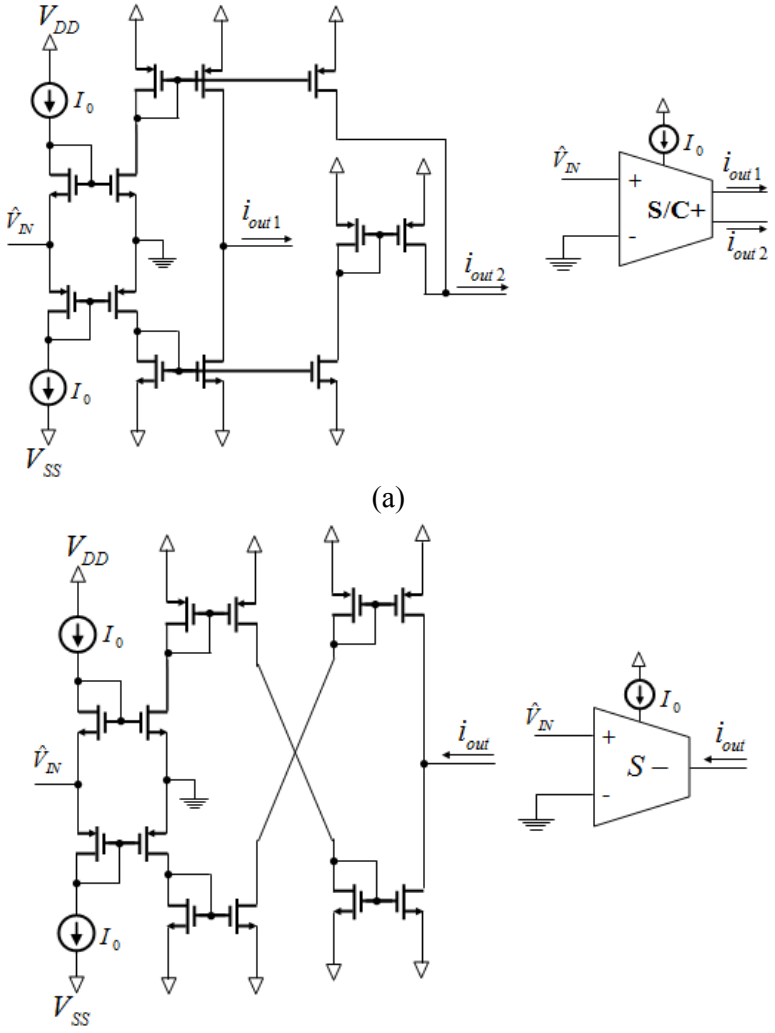


Fig. 2.12: *WIMOSFET SC transconductors: (a) positive SC transconductor cell; (b) Employed Symbol of positive SC transconductor cell (c) negative Sinh transconductor cell; and (d) Employed Symbol of negative Sinh transconductor cell.*

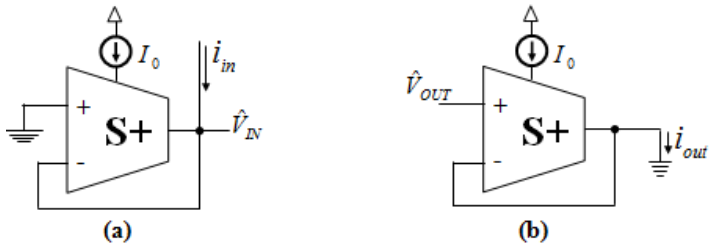


Fig. 2.13: *Realization of the WIMOSFET SD operators: (a) SINH^{-1} and (b) SINH.*

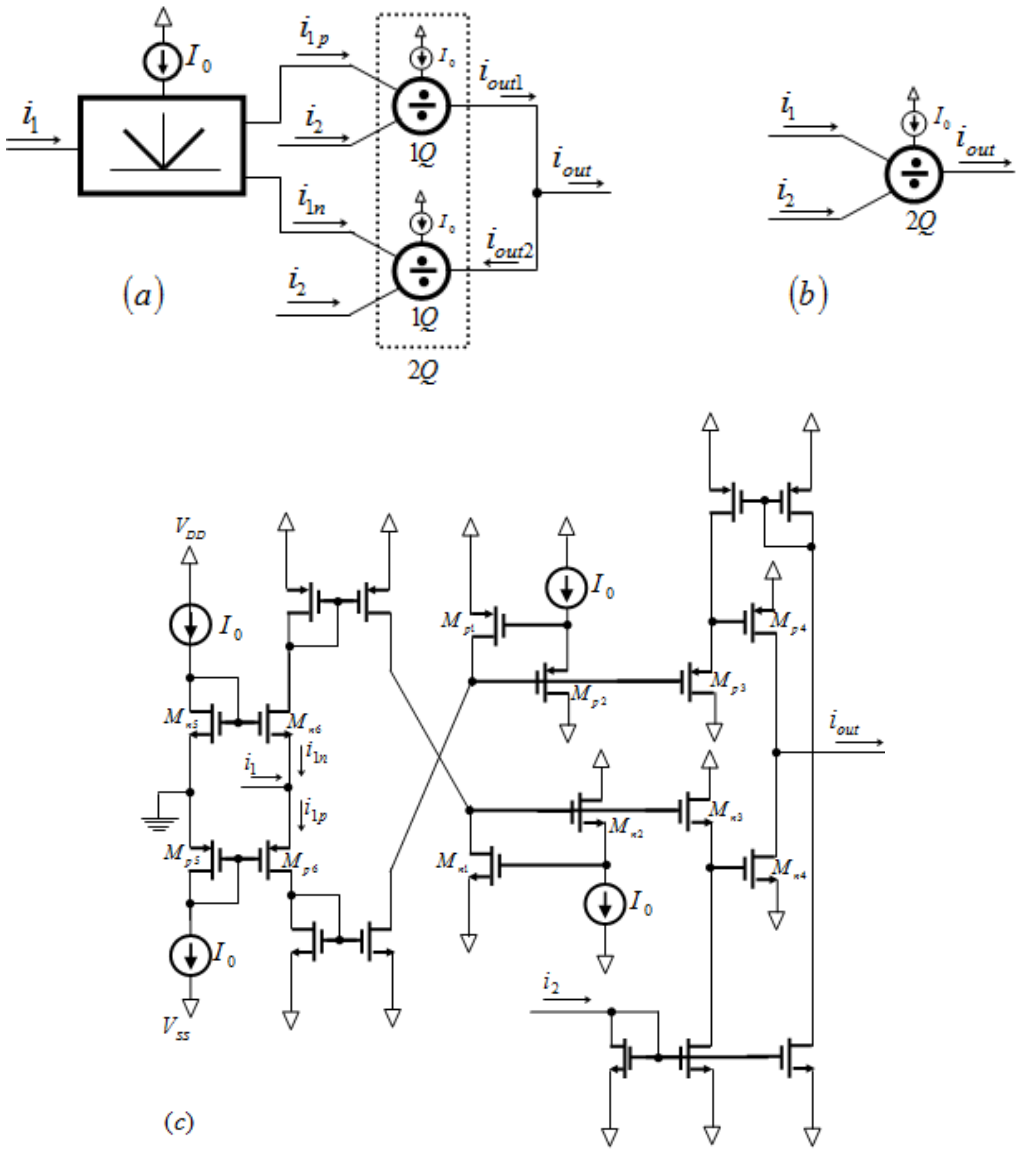


Fig. 2.14: *WIMOSFET Two-quadrant multiplier/divider: (a) Conceptual representation; (b) Employed Symbol; and (c) Topology.*

2.3.3.1.2. WIMOSFET SD Integrators

A typical configuration of a WIMOSFET SD two-input lossless integrator, constructed from blocks mentioned is demonstrated in Fig. 2.15(a). The current that flows through the capacitor $\hat{C}$ is given by

$$i_C = \hat{C}\frac{d\hat{v}_{OUT}}{dt} = 2I_o.\frac{\sinh\left(\frac{\hat{v}_{IP}}{U_T}\right) - \sinh\left(\frac{\hat{v}_{IN}}{U_T}\right)}{\cosh\left(\frac{\hat{v}_{OUT}}{U_T}\right)} \tag{2.43}$$

After some algebraic manipulations, Equation (2.30) can be written as

$$\frac{\hat{C}U_T}{2I_o}.\frac{d\left[2I_o.\sinh\left(\frac{\hat{v}_{OUT}}{U_T}\right)\right]}{dt}=2I_o.\sinh\left(\frac{\hat{v}_{IP}}{U_T}\right)-2I_o.\sinh\left(\frac{\hat{v}_{IN}}{U_T}\right) \tag{2.43}$$

Defining the pair of inverse SINH^{-1} and *SINH* mappings as given in (2.40) and (2.41), we can rewrite Equation (2.43) as

$$\hat{\tau}.\frac{d}{dt}SINH\left(\hat{v}_{OUT}\right)=SINH\left(\hat{v}_{IP}\right)-SINH\left(\hat{v}_{IN}\right) \tag{2.44}$$

Where $\hat{\tau}=CU_T/2I_o$, is the time-constant in SD.

The WIMOSFET SD two-input damped (lossy) integrator is shown in Fig. 2.15 (b). Following the same procedure, the input-output relationship of the damped integrator can be given as:

$$SINH\left(\hat{v}_{OUT}\right)=\frac{2I_o}{\hat{C}U_T}.\int\{SINH(\hat{v}_{IP})-SINH(\hat{v}_{IN})-SINH(\hat{v}_{OUT})\}dt \tag{2.45}$$

In Laplace domain, the input-output relationships of the SD two-input lossless and lossy integrators can be respectively given by Equations (2.46) and (2.47)

$$\frac{i_{out}}{i_{ip}-i_{in}}=\frac{SINH\left(\hat{v}_{OUT}\right)}{SINH\left(\hat{v}_{IP}\right)-SINH\left(\hat{v}_{IN}\right)}=\frac{\left(g_m/\hat{C}\right)}{S}=\frac{1}{S\tau} \tag{2.46}$$

$$\frac{i_{out}}{i_{ip}-i_{in}}=\frac{SINH\left(\hat{v}_{OUT}\right)}{SINH\left(\hat{v}_{IP}\right)-SINH\left(\hat{v}_{IN}\right)}=\frac{\left(g_m/\hat{C}\right)}{S+\left(g_m/\hat{C}\right)}=\frac{1}{S\tau+1} \tag{2.47}$$

Where $g_m=\frac{2I_o}{U_T}$, is the transconductance of the SC cell and $\left(g_m/\hat{C}\right)$ is the reciprocal of integrator's time-constant.

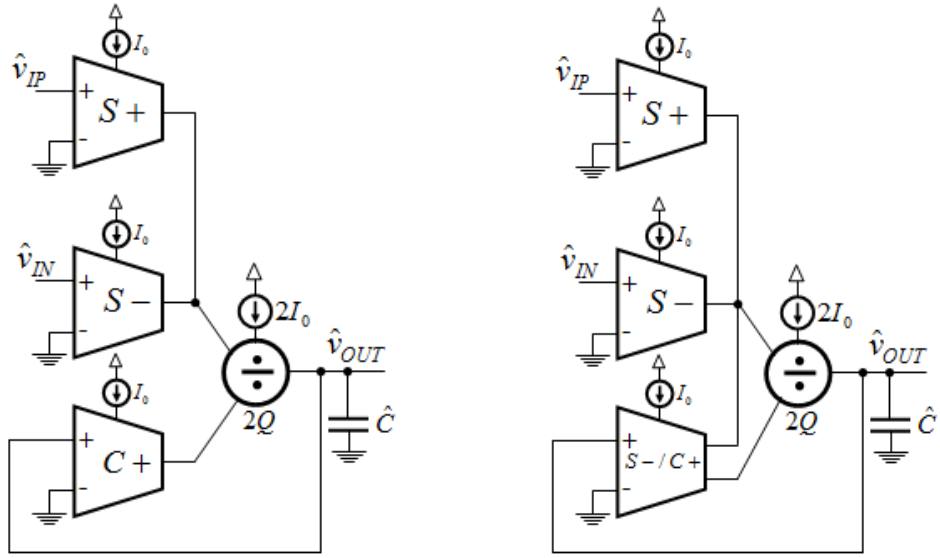
2.3.3.1.3. WIMOSFET SD Summation/Subtraction Block

The realization of WIMOSFET SD algebraic summation block with a weighted input is that given in Fig. 2.16. Applying the KCL at the output node, it is derived that

$$2I_o.\sinh\left(\frac{\hat{v}_{OUT}}{U_T}\right)=2I_o.\sinh\left(\frac{\hat{v}_{IN1}}{U_T}\right)-a.2I_o.\sinh\left(\frac{\hat{v}_{IN2}}{U_T}\right) \tag{2.48}$$

Using Equation (2.41), Equation (2.48) can be written as

$$SINH\left(\hat{v}_{OUT}\right)=SINH\left(\hat{v}_{IN1}\right)-a.SINH\left(\hat{v}_{IN2}\right) \tag{2.49}$$



(a) (b)

Fig. 2.15: *WIMOSFET SD Integrators. (a) Two-input SD lossless integrator. (b)Two-input SD lossy integrator.*

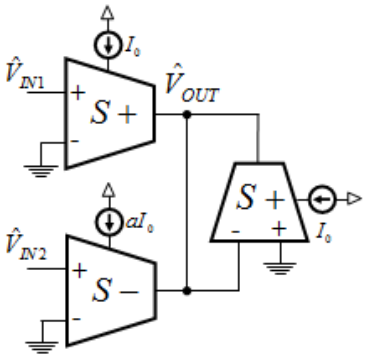


Fig. 2.16: *WIMOSFET SD algebraic summation/subtraction block with weighted input.*

2.3.3.2. BiCMOS based SD Filter Design

2.3.3.2.1. BiCMOS SD operators

The BiCMOS SC cell is given in Fig. 2.17(a) **[85]**. The cell provides hyperbolic-sine and cosine outputs, given by the expressions in Equations (2.50) and (2.51) respectively

$$I_S = 2I_o \sinh\left(\frac{\hat{\upsilon}_{IN+} - \hat{\upsilon}_{IN-}}{V_T}\right) \tag{2.50}$$

$$I_C = 2I_o \cosh\left(\frac{\hat{\upsilon}_{IN+} - \hat{\upsilon}_{IN-}}{V_T}\right) \tag{2.51}$$

where I_o is a dc current, V_T is the thermal voltage (≅26mV @ 27°K), $\hat{\upsilon}_{IN+}$ and $\hat{\upsilon}_{IN-}$ are the voltage at the non-inverting and inverting inputs, respectively.

The corresponding cell with an inverted Sinh output is shown in Figure 2.17(b).

Fig. 2.17 can be used to implement SINH and SINH^{-1} complementary operators described by Equations (2.52) and (2.53) respectively as shown in Fig. 2.18.

$$\hat{\upsilon} = SINH^{-1}(i) = V_{DC} + V_T \cdot \sinh^{-1}\left(\frac{i}{2I_o}\right) \tag{2.52}$$

$$i \equiv SINH\left(\hat{\upsilon}\right) = 2I_o \cdot \sinh\left(\frac{\hat{\upsilon} - V_{DC}}{V_T}\right) \tag{2.53}$$

where V_{DC} is a dc voltage.

In addition, BiCMOS SC cell can be used to implement two-quadrant multiplier/divider block as shown in Fig. 2.19 **[85]** where the output current is given by Equation (2.42).

2.3.3.2.2. BiCMOS based SD integrators

A typical configuration of a BiCMOS SD two-input lossless integrator, constructed from blocks mentioned is demonstrated in Fig. 2.20(a). The current that flows through the capacitor $\hat{C}$ is given by

$$\hat{C}\frac{d\hat{\upsilon}_{OUT}}{dt} = \frac{2I_o \sinh\left(\frac{\hat{\upsilon}_{IP} - V_{DC}}{V_T}\right) - 2I_o \sinh\left(\frac{\hat{\upsilon}_{IN} - V_{DC}}{V_T}\right)}{2I_o \cosh\left(\frac{\hat{\upsilon}_{OUT} - V_{DC}}{V_T}\right)} \tag{2.54}$$

After some algebraic manipulations, Equation (2.54) can be written as

$$\frac{\hat{C}V_T}{2I_o}.\frac{d\left[2I_o.\sinh\left(\frac{\hat{v}_{OUT} - V_{DC}}{V_T}\right)\right]}{dt} = 2I_o.\sinh\left(\frac{\hat{v}_{IP} - V_{DC}}{V_T}\right) - 2I_o.\sinh\left(\frac{\hat{v}_{IN} - V_{DC}}{V_T}\right) \tag{2.55}$$

Defining the pair of inverse SINH^{-1} and *SINH* mappings as given in Equations (2.52) and (2.53), we can rewrite Equation (2.55) as Equation (2.44).

Where $\hat{\tau} = CV_T / 2I_o$, is the time-constant in SD.

The corresponding equation for damped BiCMOS integrator of Fig. 2.20(b) and the Laplace domain equations of Lossless and Lossy integrators will be same as Equations (2.45), (2.46) and (2.47) respectively.

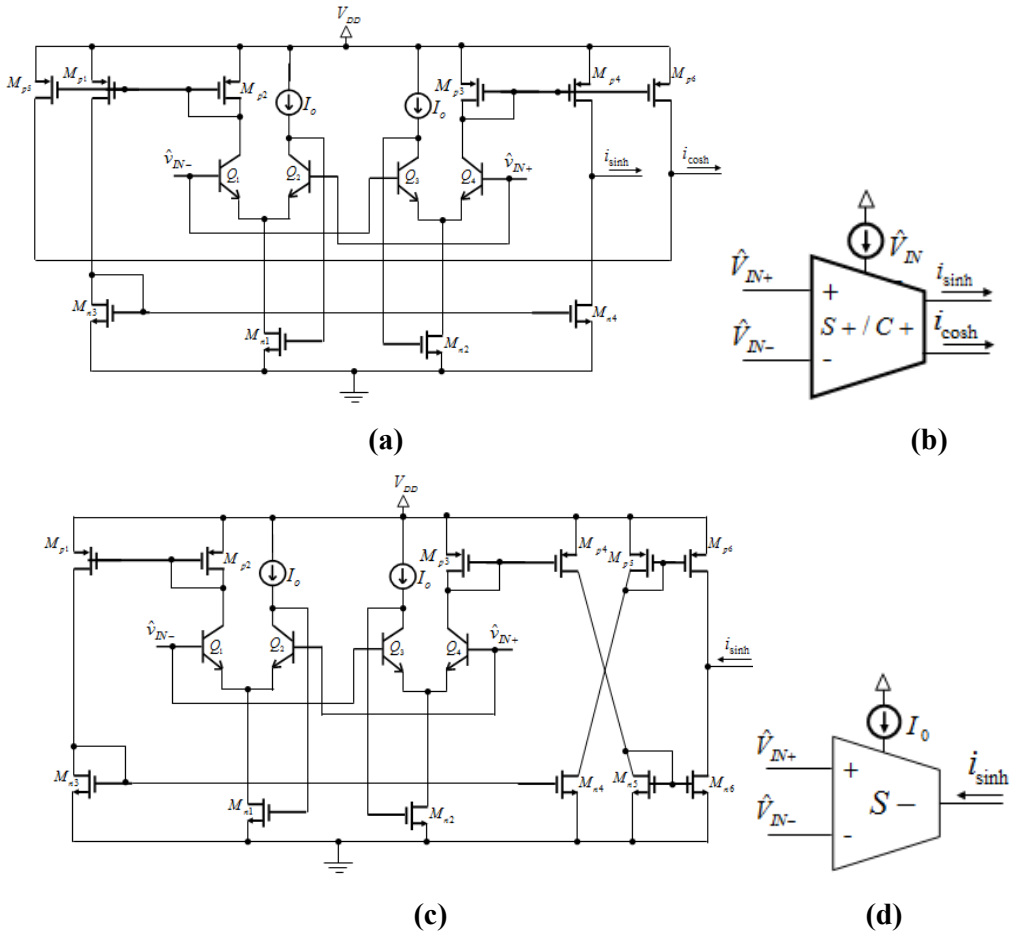


Fig. 2.17: *BiCMOS SC transconductors: (a) positive SC transconductor cell; (b) Employed symbol of positive SC transconductor cell (c) negative Sinh transconductor cell; and (d) Employed symbol of negative Sinh transconductor cell.*

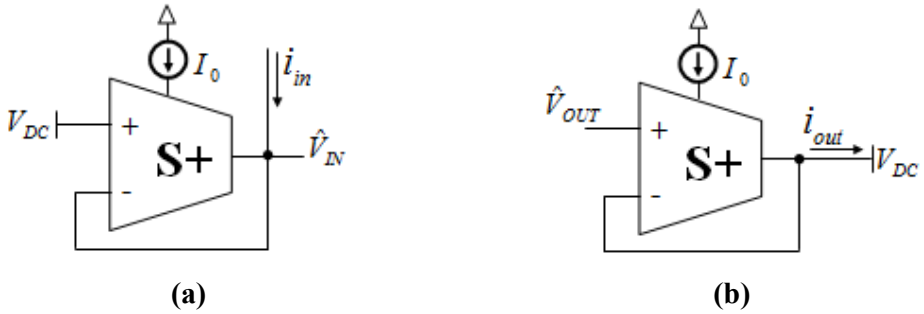


Fig. 2.18: *Realization of the BiCMOS SD operators: (a) SINH^{-1} and (b) SINH.*

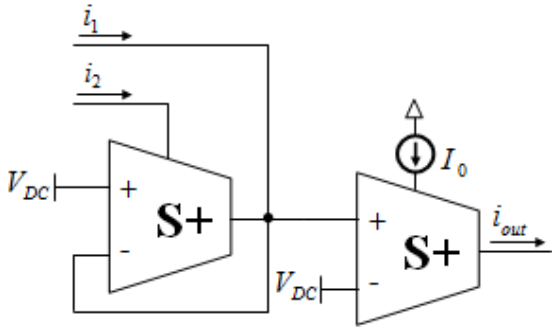
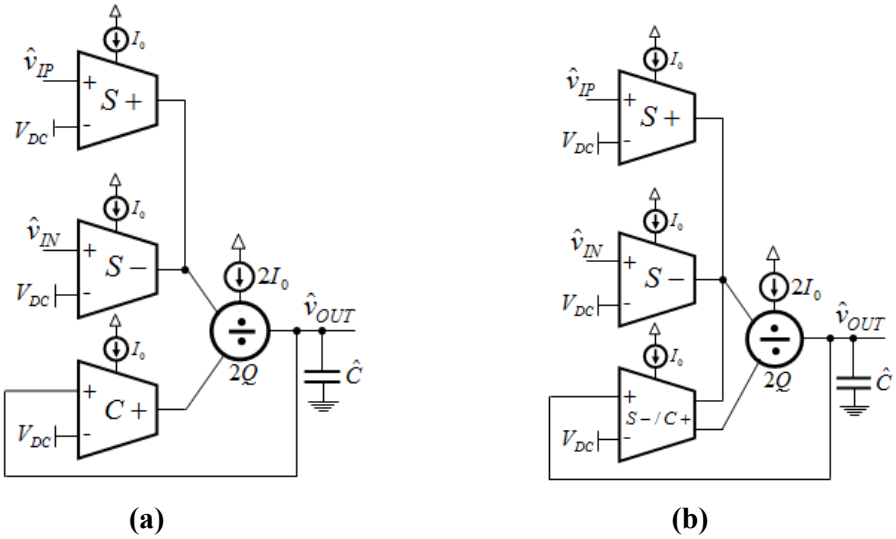


Fig. 2.19: *BiCMOS Two-quadrant multiplier/divider* ***[85]****.*



(a) **(b)**

Fig. 2.20: *BiCMOS SD Integrators. (a) Two-input SD lossless integrator. (b)Two-input SD lossy integrator.*

2.3.3.2.3. BiCMOS SD Summation/Subtraction Block

The realization of BiCMOS SD algebraic summation block with a weighted input is that given in Fig. 2.21. Applying the KCL at the output node, it is derived that

$$2I_o.\sinh\left(\frac{\hat{v}_{OUT}-V_{DC}}{V_T}\right)=2I_o.\sinh\left(\frac{\hat{v}_{IN1}-V_{DC}}{V_T}\right)-a.2I_o.\sinh\left(\frac{\hat{v}_{IN2}-V_{DC}}{V_T}\right) \quad (2.56)$$

Using Equation (2.53), Equation (2.48) can be written as

$$SINH(\hat{v}_{OUT})=SINH(\hat{v}_{IN1})-a.SINH(\hat{v}_{IN2}) \quad (2.57)$$

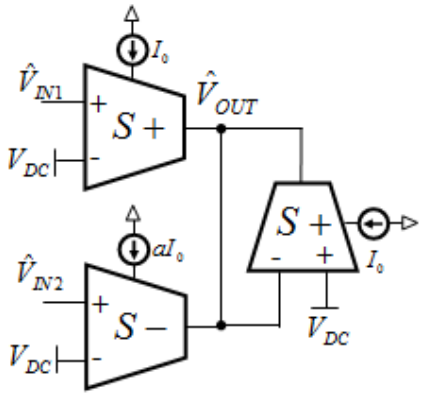


Fig. 2.21: *BiCMOS SD algebraic summation/subtraction block with weighted input.*

2.4. Summary

The chapter started with discussion of companding techniques including LD, SRD and SD techniques of filter synthesis. The building blocks required to implement companding filters were fully investigated. Translinear circuits are the base of companding circuits and were also discussed in detail.

CHAPTER-3

Synthesis Methods of Companding Filters

An Introduction

SYNTHESIS METHODS OF COMPANDING FILTERS

3.1. Introduction

With regards to the design of companding filters, a number of systematic methods have been introduced in the literature as under:

i) The ***Function Block Diagram (FBD) or Signal Flow Graph (SFG) Synthesis method*** that simulates the operation of the passive prototype filter and transposes to the corresponding one in the companding-domain by employing an appropriate set of complementary operators **[36, 41, 58, 61-63, 77, 84, 90-92, 129, 139, 142 etc.].**

ii) The ***Linear Gm-C Filter Transposition Synthesis Method of Companding Filters*** in which the linear *gm-C* filter that simulates the operation of the passive filter is transposed to the companding-domain by using appropriately configured non-linear transconductor cells **[38, 50, 57, 132 etc.].**

iii) The ***Exponential State-Space Synthesis Method of Companding Filters*** in which the state-space operational description of the passive prototype filter is mapped to the corresponding companding filter **[41, 66, 128 etc.].**

iv) The ***Linear Transformation (LT) Synthesis Method of Companding Filters*** in which passive prototype filter is divided into small two-port networks and each small network is then transformed into companding-mode network and subsequently connected to form a Companding filter **[51, 52, 130, 143 etc.].**

v) The ***Component Substitution Synthesis Method of Companding Filters*** in which the elements of the passive prototype filter are substituted by appropriate companding blocks which implement the corresponding relationships and subsequently connected to form a Companding filter **[59, 73, 85, 127, 129 etc.].**

vi) The ***Wave Synthesis Method of Companding Filters*** in which the corresponding LC passive prototype filter is split into two-port subnetworks that are considered resistively terminated at both ports. Each port is fully described by using the wave variables, defined as incident and reflected waves. Accordingly, these two-port subnetworks are described by using the scattering parameters. The linear SFG that corresponds to the scattering parameters matrix description of the elementary two-port subnetwork is then transposed to the corresponding companding-domain SFG, by employing the set of complementary operators **[49, 137].**

Among the above six synthesis methods of companding filters, only first four methods will be discussed in the following section as the various proposed circuits which are Published/Accepted/Under-review fall only under these synthesis techniques. It is worth to mention here that the work is under progress for the design of proposed circuits under later two categories as well.

3.1.1. Functional Block Diagram (FBD) Synthesis Method of Companding Filter Design

The FBD method is most frequently used for designing companding filters. The method can be followed by either of two ways. The First technique is the indirect one in which LC ladder is first converted into an FBD using operational simulation and the linear FBD is then subsequently translated into the corresponding Companding FBD using the specific steps. The second technique is the direct one in which we can directly start from translating the applied FBD of a particular problem into the corresponding Companding FBD.

3.1.1.1. Indirect Method

One of the most popular filter synthesis techniques is the method of operational simulation of LC ladders. This method finds the active circuit realization that mimics the internal *i-v* relationships of the individual *L* and *C* elements in the LC network. The benefits are many-fold. Widely accepted by the design community, lossless doubly-terminated LC ladders that are designed to deliver maximum possible power to the load exhibit low passband sensitivity to the inevitable process and element variations. The resulting circuit has a one to one correspondence to its passive LC ladder predecessor. This promotes physical understanding about the functionality of various parts of the resulting circuit. Designers can tell from inspection which part of the circuit is implementing integrations, scaling or summation etc. The companding filter synthesis by operational simulation of LC ladder involves the following steps:

A. Finding an LC ladder that meets the design specifications.

B. Deriving the corresponding FBD from the LC prototype.

C. Modifying the FBD to its companding-domain equivalence by:

i) Placing *Expander* and *Compressor* blocks in front and behind each integrator respectively.

ii) Placing *Expander* and *Compressor* blocks at the filter output and input respectively.

D. Map the companding-domain integrator circuit onto the companding-domain FBD.

Notice that by performing step C, we are transforming the filter FBD from the linear-domain into the companding-domain, while ensuring overall linear input-to-output relationship. The following example demonstrates the conversion of a 2nd-order low-pass LC ladder into the corresponding LD filter using the blocks mentioned in section 2.3.1.

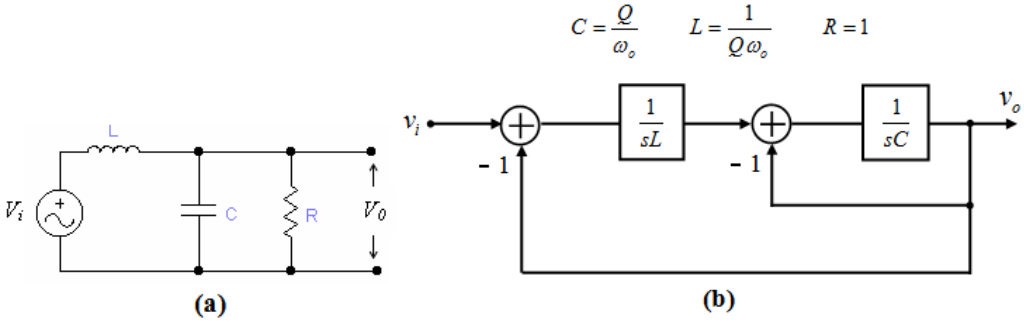
3.1.1.1.1. Design Example

It begins with finding the passive prototype as shown in Fig. 3.1 (a), followed by deriving the corresponding linear FBD as shown in Fig. 3.1 (b)) **[144, 145]** and the achieved LD FBD as shown in Fig. 3.1 (c) using the above steps, and finally, the LD filter circuit as shown in Fig. 3.19(d). This filter will ideally realize the transfer function,

$$\frac{I_{out}}{I_{in}} = H(s) = K.\frac{\omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \tag{3.1}$$

Where $\omega_o = \frac{1}{\sqrt{LC}}$ $Q = R.\sqrt{\frac{C}{L}}$ (3.2)

and K (=1) denotes the filter dc gain. The simulation results of the LC ladder of Fig. 2.1(a) with R = 1Ω, C = 1μF and L = 10μH and that of LD counter part of Fig. 3.1(d) with $V_{CC} = -V_{EE} = 1.5V$, $I_0 = 25\mu A$, $C_1 = 9.61nF$, $C_2 = 0.961nF$ and using the parameters of the AT&T CBIC-R NR100N NPN transistor **[32]** given in Table 3.1, is shown in Fig. 3.2.



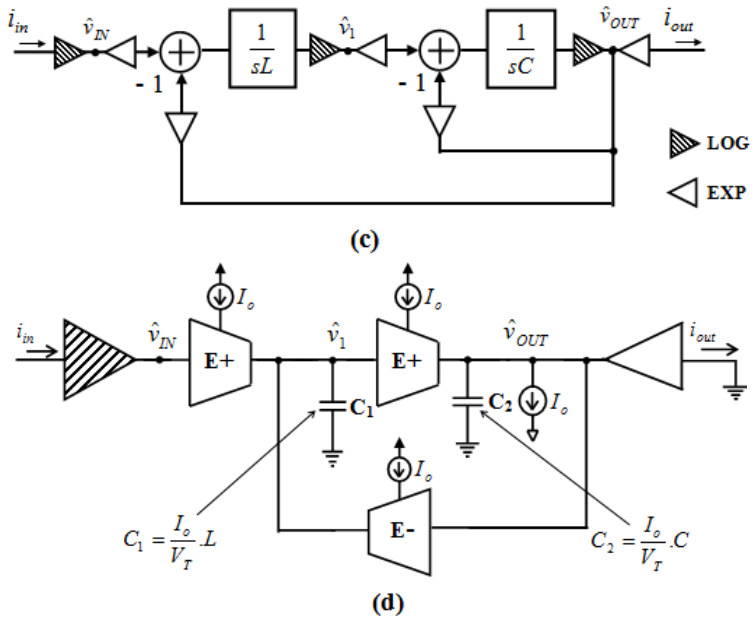
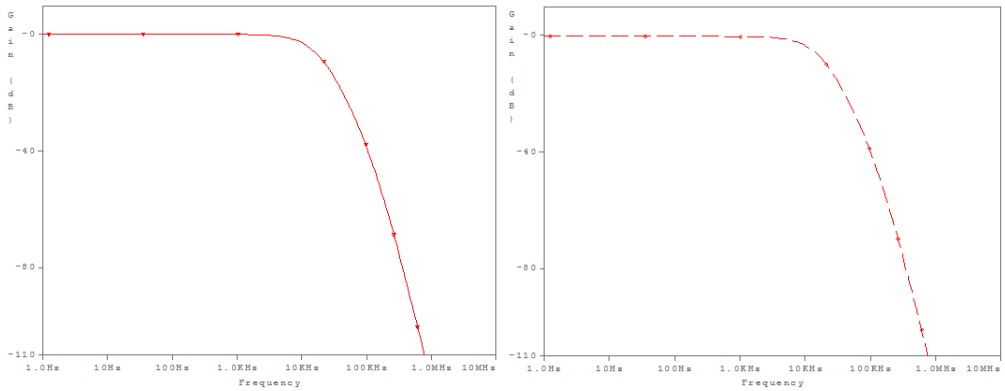


Fig. 3.1: *Synthesis of lowpass LD biquad: (a) Passive prototype (b) the linear SFG (c) the corresponding LD SFG, and (d) the final LD filter.*



(a) ***(b)***

Fig. 3.2: *Simulation Results of: (a) Passive prototype of Fig. 3.1(a). (b) LD filter of Fig. 3.1(d).*

NR100N - 1X NPN TRANSISTOR					
.MODEL NXI NPN	RB=524.6	IRB=0	RBM=25	RC=50	RE=1
+IS=121E-18	CJC=0.983E-13	XTI=2	XTB=1.538	BF=137.5	NF=1
+ IKF=6.974E-3	TF=0.425E-9	NR=1	NE=1.713	BR=0.7258	VAR=10.73
+ISE=36E-16	TR=0.425E-8	NC=2	VAF=159.4	ISC=0	VJE=0.5
+IKR=2.198E-3	CJE=0.214E-12	MJE=0.28	EG = 1.206	VJC=0.5	MJC = 0.3

Table 3.1: *The model parameters of NR100N NPN transistor used for PSPICE simulations.*

3.1.1.2. Direct Method

As discussed earlier, direct method starts from the FBD itself. The following examples demonstrate: (1) the proposed Multiple-Input-Multiple-Output (MIMO) Universal filter; (2) the proposed generic Single-Input-Multiple-Output (SIMO) universal filter topology of arbitrary order and type, leading to four optimal FLF configurations, which has received a lot of appreciation from the distinguished corners as suggested by the fact that the LD version of one of its configuration stands in the top cited articles in one of the Wiley's leading journal of the world since 2009; (3) the proposed Multiple-Input-Single-Output (MISO) universal filter topology of arbitrary order and type; (4) the proposed universal biquadratic filter for low frequency applications. The implementation of such filters with multifunction feature find applications in phase-locked loops, FM stereo demodulator, touch-tone telephone tone decoder and crossover network used in three-way high-fidelity loudspeakers, and, Biomedical Electronics and most of these are embedded in the portable systems **[146].**

3.1.1.2.1. Proposed MIMO universal filter [J2]

The FBD and the transposed LD FBD of the proposed MIMO universal filter is shown in Fig. 3.3 and Fig. 3.4 respectively. An examination of the FBD of the proposed LD MIMO universal filter given in Fig. 3.4 reveals that it has been configured around lossless integrator and addition/subtraction blocks with appropriate feedbacks from their outputs. The realized input-output relationships of the filter are given by:

$$i_{out1} = EXP\left\{\hat{V}_{out1}(s)\right\} = \left\{EXP\left(\hat{V}_{i3}\right)s^2 - \frac{1}{K\tau_2}EXP\left(\hat{V}_{i2}\right)s + EXP\left(\hat{V}_{i1}\right)\omega_0^2\right\}\Big/\Delta$$
$$i_{out1} = \left\{(i_{i3}).s^2 - \frac{1}{K\tau_2}(i_{i2}).s + .\omega_0^2.(i_{i1})\right\}\Big/\Delta \quad (3.3)$$

$$i_{out2} = EXP\left\{\hat{V}_{out2}(s)\right\} = \left\{s.\frac{1}{\tau_2}\left[EXP\left(\hat{V}_{i2}\right) + EXP\left(\hat{V}_{i3}\right)\right] + K\omega_0^2.\left[EXP\left(\hat{V}_{i3}\right) - EXP\left(\hat{V}_{i1}\right)\right]\right\}\Big/\Delta$$
$$i_{out2} = \left\{s.\frac{1}{\tau_2}(i_{i2} + i_{i3}) + K\omega_0^2.(i_{i3} - i_{i1})\right\}\Big/\Delta \quad (3.4)$$

$$i_{out3} = EXP\left\{\hat{V}_{out3}(s)\right\} = \left\{s^2.\left[EXP\left(\hat{V}_{i2}\right) + EXP\left(\hat{V}_{i3}\right)\right] + s.\frac{K}{\tau_1}.\left[EXP\left(\hat{V}_{i3}\right) - EXP\left(\hat{V}_{i1}\right)\right]\right\}\Big/\Delta$$
$$i_{out3} = \left\{s^2(i_{i2} + i_{i3}) + s.\frac{K}{\tau_1}(i_{i3} - i_{i1})\right\}\Big/\Delta \quad (3.5)$$

$$i_{out4} = EXP\left\{\hat{V}_{out4}(s)\right\} = \left\{s.\frac{K}{\tau_1}.\left[EXP\left(\hat{V}_{i1}\right) - EXP\left(\hat{V}_{i3}\right)\right] + \omega_0^2.\left[EXP\left(\hat{V}_{i1}\right) + EXP\left(\hat{V}_{i2}\right)\right]\right\} \Big/ \Delta$$
$$i_{out4} = \left\{s.\frac{K}{\tau_1}(i_{i1} - i_{i3}) + \omega_0^2.(i_{i1} + i_{i2})\right\} \Big/ \Delta \quad (3.6)$$

$$i_{out5} = EXP\left\{\hat{V}_{out5}(s)\right\} = \left\{Ks^2.\left[EXP\left(\hat{V}_{i1}\right) - EXP\left(\hat{V}_{i3}\right)\right] + s.\frac{1}{\tau_2}\left[EXP\left(\hat{V}_{i1}\right) + EXP\left(\hat{V}_{i2}\right)\right]\right\} \Big/ \Delta$$
$$i_{out5} = \left\{Ks^2.(i_{i1} - i_{i3}) + s.\frac{1}{\tau_2}(i_{i1} + i_{i2})\right\} \Big/ \Delta \quad (3.7)$$

Where

$$\Delta = s^2 + \frac{1}{K\tau_2}s + \omega_o^2 \quad (3.8)$$

and LOG and EXP operators are as per Equations (2.16) and (2.17) respectively.

Also ω_0 and Q of each filter responses is given as follows:

$$\omega_0 = \sqrt{\frac{1}{\hat{\tau}_1\hat{\tau}_2}} \quad (3.9)$$

$$Q = K\sqrt{\frac{\hat{\tau}_2}{\hat{\tau}_1}} \quad (3.10)$$

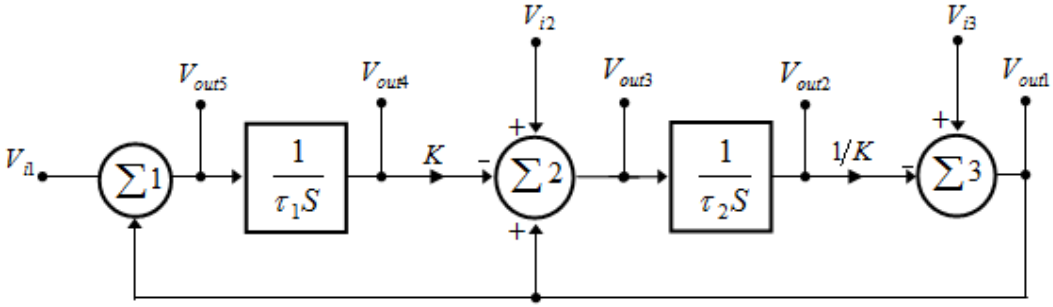


Fig. 3.3: *FBD of the proposed MIMO universal filter*

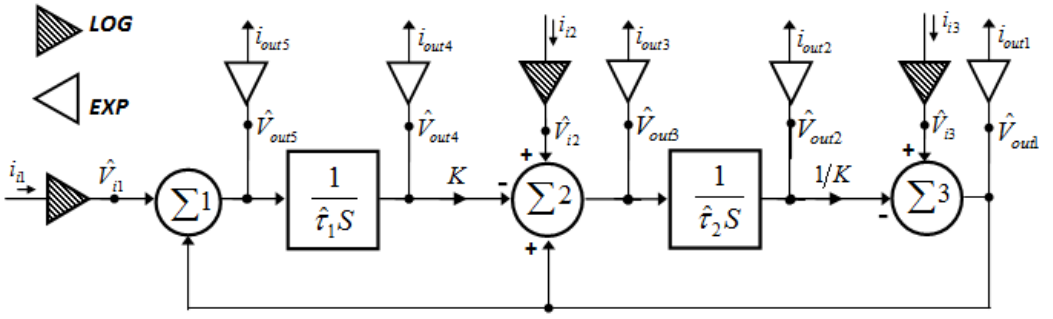


Fig. 3.4: *Transposed LD FBD of the proposed MIMO universal filter of Fig. 3.3.*

The filter responses obtained from Equations (3.3)-(3.7) are given in Table 3.2 corresponding to selection of currents i_{i1}, i_{i2} and i_{i3}. An examination of Table 3.2 reveals that the proposed filter is simultaneously universal MISO and SIMO and no matching condition is required to be imposed for obtaining any of the responses.

The LD MIMO depicted in Fig. 3.5 has been constructed using LOG and EXP blocks, lossless integrator blocks and addition/subtraction blocks demonstrated in section 2.31. The expressions for ω_o and Q corresponding to Equations (3.9) and (3.10) have been obtained by using time constant relationship of LD integrator and are given by:

$$\omega_0 = \frac{I_o}{V_T}\sqrt{\frac{1}{C_1 C_2}} \tag{3.11}$$

$$Q = K\sqrt{\frac{C_2}{C_1}} \tag{3.12}$$

It is obvious from Equations (3.11) and (3.12) that ω_o and Q are electronically tuneable in an independent manner. The former through *Io*, while the latter through K factor which can be made proportional to a current or ratio of currents by connecting LOG and EXP blocks in cascade.

Input currents			**Responses Available at output node currents**				
i_{i1}	i_{i2}	i_{i3}	i_{out1}	i_{out2}	i_{out3}	i_{out4}	i_{out5}
i_{in}	0	0	NI-LP	I-LP	I-BP	NA	NA
0	i_{in}	0	I-BP	NI-BP	NI-HP	NI-LP	NI-BP
0	0	i_{in}	NI-HP	NA	NA	I-BP	I-HP
i_{in}	0	i_{in}	NI-BS	NA	NA	NA	NA
i_{in}	i_{in}	i_{in}	AP	NA	NA	NA	NA

Note:- *NA: Not Applicable, NI: Non-Inverting, I: Inverting, i_{in}: Input current*

Table 3.2: *Standard 2nd-order filter functions obtained for five outputs by carefully selecting the input currents i_{i1}, i_{i2} and i_{i3}.*

3.1.1.2.1.1. Simulation and Experimental Results

To verify the theoretical results, the proposed LD MIMO universal biquad depicted in Fig. 3.5 was designed for $V_{CC} = -V_{EE} = 1.5$ *V*, $I_o = 5$ *μA and* $C_1 = C_2 = 63.66$*pF* which yield pole frequency $(f_C) = 500$ *KHz*. The NPN transistors in cell implementations are

simulated using the parameters of the AT& T CBIC-R NR100N NPN transistor. The frequency behaviour of the filter was evaluated by performing large-signal transient analysis using the PSPICE simulator, with modulation index factor $m=i_{peak}/I_o = 50\%$ and the magnitude responses obtained are given in Figs 3.6(a)-3.6(e).

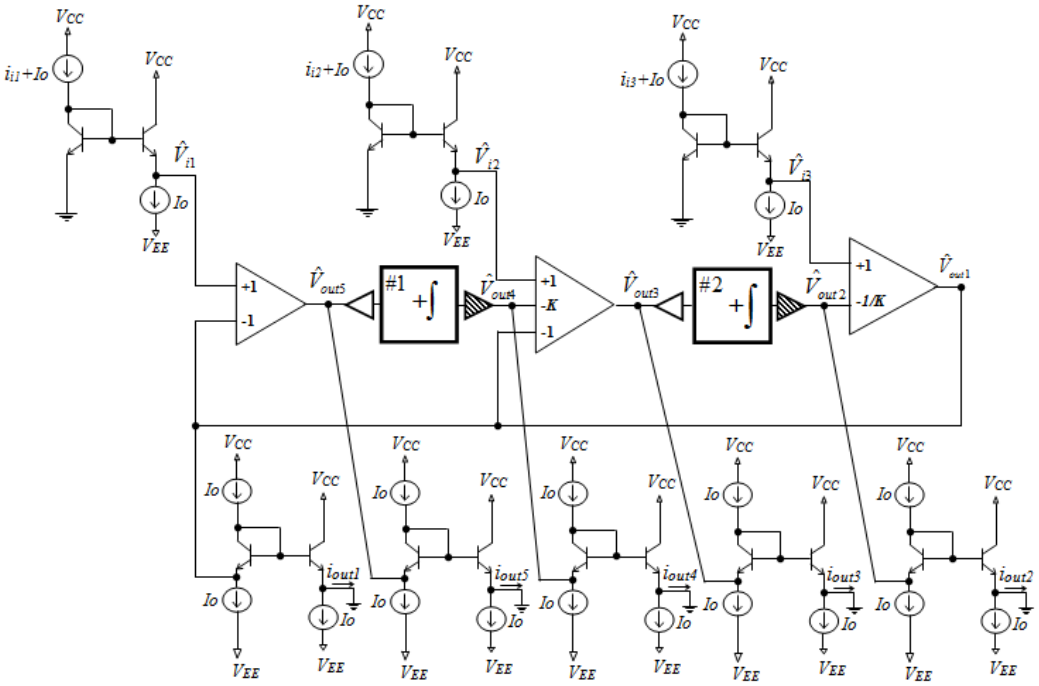
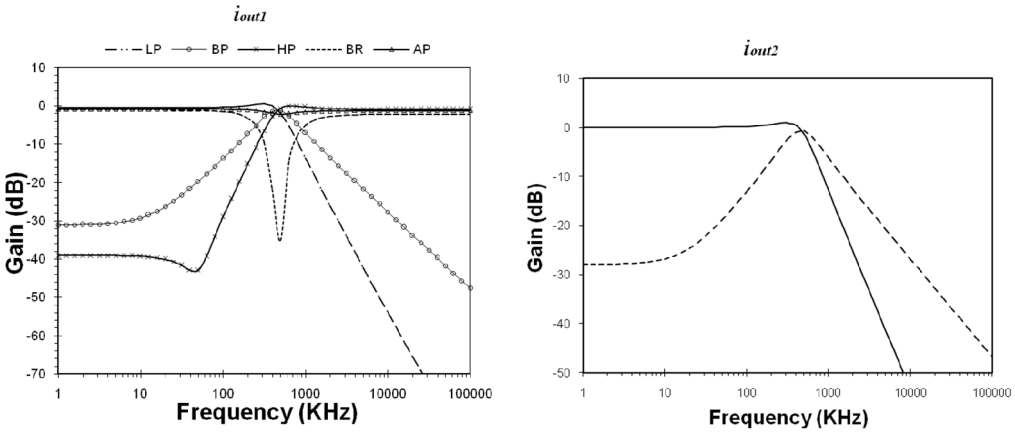


Fig. 3.5: *Proposed LD MIMO universal filter.*



(a) (b)

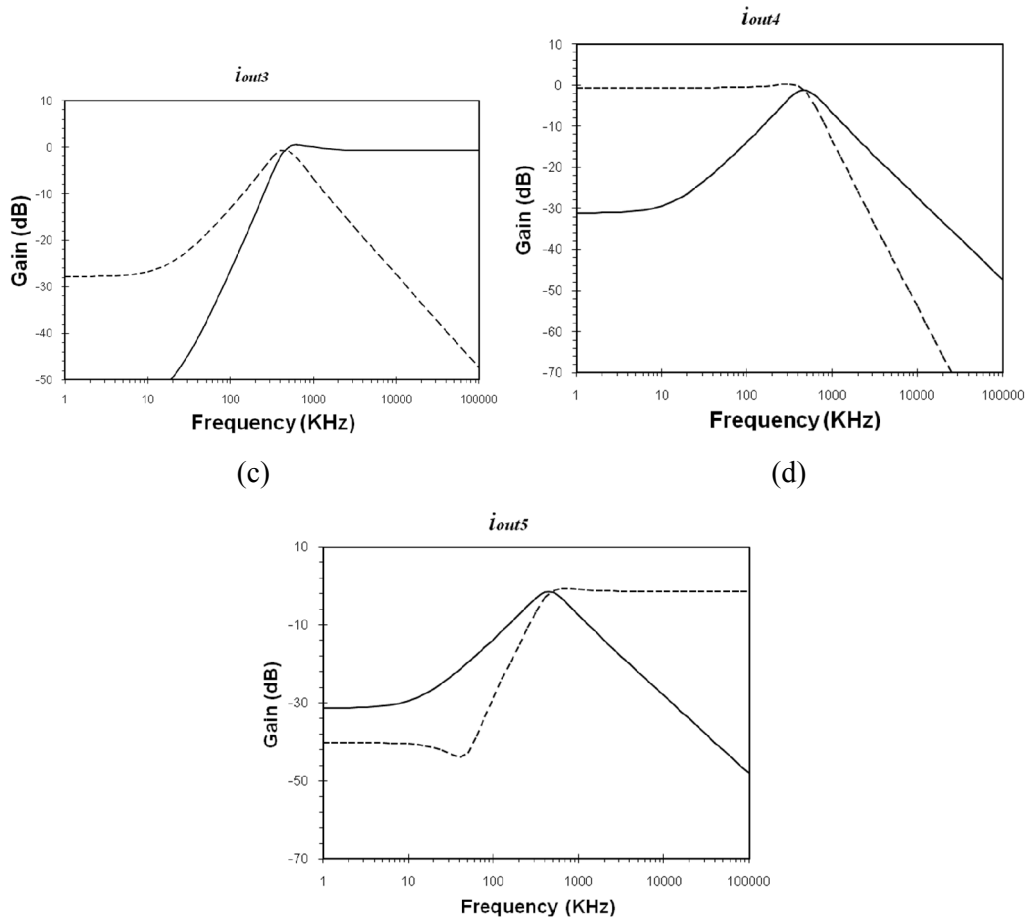


Fig. 3.6: *Simulated magnitude responses of standard filter functions of proposed MIMO universal filter in Fig. 3.5. (a) i_{out1}, (b) i_{out2}, (c) i_{out3}, (d) i_{out4}, (e) i_{out5}.*

The electronic tuneabilty of ω_0 is demonstrated in Fig. 3.7. In addition, the gain of the filter responses is electronically controllable through the dc bias current of the corresponding expansion stages which is depicted in Fig. 3.8. The independent electronic adjustment of ω_0 and Q corresponding to Equations (3.11) and (3.12) is demonstrated in Fig. 3.9.

The THD analysis usually considered for deriving distortion analysis is not appropriate. By applying an input signal close to the fundamental frequency at the input of a filter, the corresponding harmonics usually fall into stopband and, thus, an underestimation of the non-linearity at the output of the filter will be achieved. The problem is usually prominent in case of BP responses. Thus, more practical way for evaluating the non-linear performance is to perform the well-known 3rd-order inter-

modulation distortion (IMD3) test. Therefore, to study the non-linear behaviour of proposed filter for LP response (i_{out1}), IMD3 test was employed. Accordingly two closely spaced tones 100 kHz and 110 kHz, which fall in the passband of the LP response, were applied at the input of the filter. The simulated value of distortion at full-scale input signal (m = 100 %) for the output was found to be -55.8 dB. Fig. 3.10 depicts the simulated IMD3 response as a function of the modulation index factor. The noise of the filter was integrated over a 2 MHz range and the simulated rms value of the output noise current was computed to be 131 nA. The achieved dynamic range at 0.1 % distortion level was 49.1 dB. In addition, the power consumption for proposed filter was calculated as 3.32 mW. Assuming 1 % deviation vis-a-vis Gaussian distribution, Monte Carlo analysis with 100 runs was conducted for the variations of the transistor mismatches, integrating capacitors and bias currents. The derived simulated values from the proceeding sensitivity analysis were found to be 0.008 and 9.898 KHz respectively for standard deviation of the maximum gain and the cut-off frequency. These values verify low sensitivity and good linearity features of the filter.

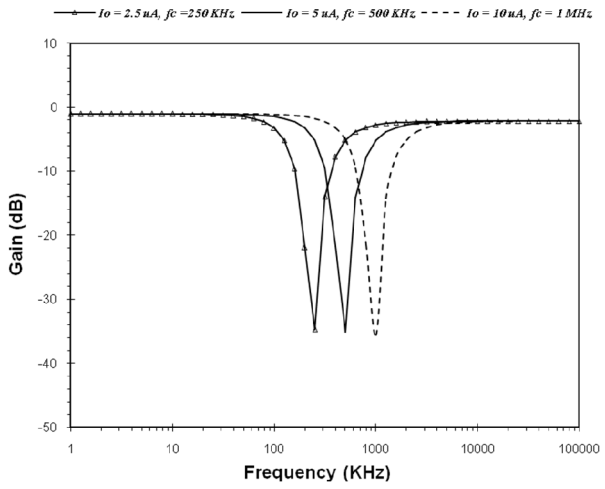


Fig. 3.7: *Demonstration of the electronic tunability of frequency characteristics of the proposed MIMO filter.*

To verify the circuit operation in practice, the proposed MIMO universal filter was implemented in a bread-board realization, using commercially available transistor arrays (LM3046N). Fig. 3.11 shows a photograph of the breadboard circuit. Subsequently, the circuit was tested practically for frequency response. Fig. 3.12

shows the measured frequency response with $I_o = 157\ \mu A$ and $C_1 = C_2 = 0.1\ \mu F$ which yield resonance frequency $(f_C) = 10\ KHz$. From the measured response, we can notice that even in worst (breadboard) realization, the response fairly corresponds to simulation results.

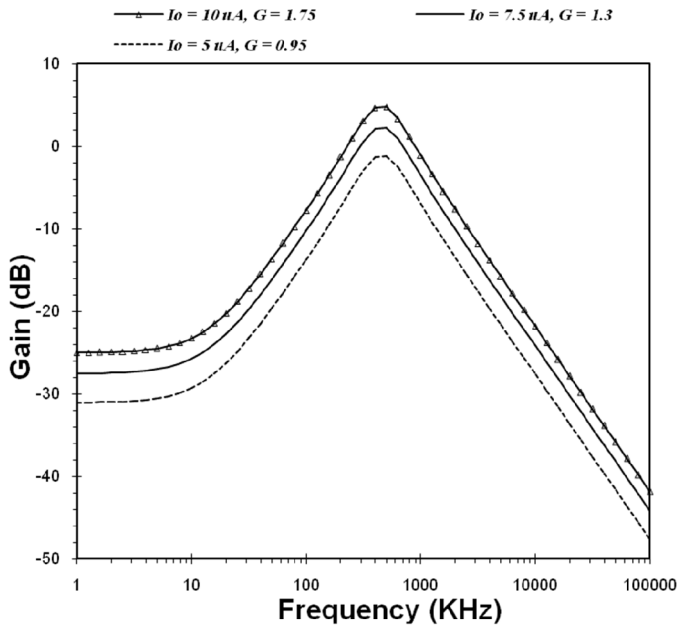


Fig. 3.8: *Demonstration of the electronic tunability of gain characteristics of the proposed MIMO filter.*

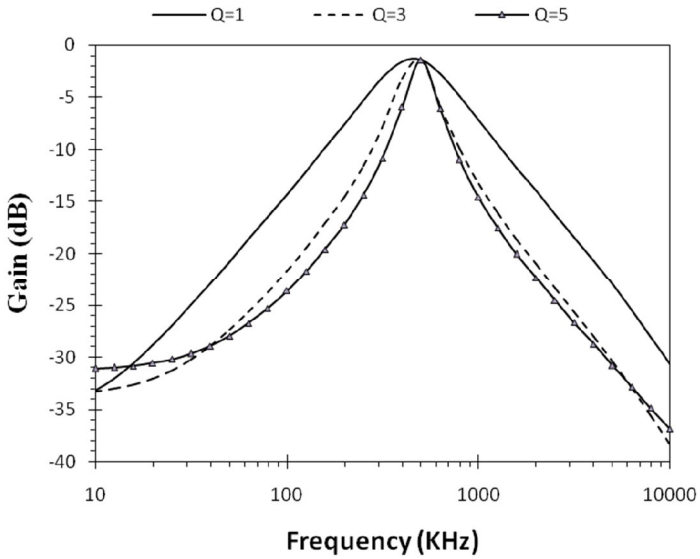


Fig. 3.9: *Demonstration of the independent adjustment of ω_0 and Q of the filter.*

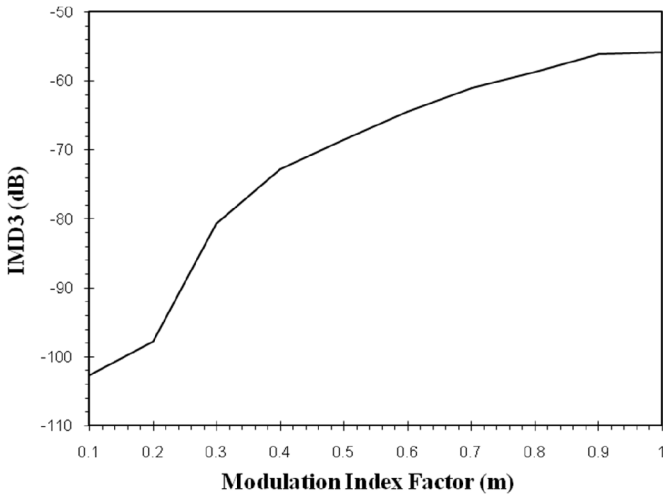


Fig. 3.10: *Linear performance of the LP filter function (i_{out1}) of MIMO universal filter.*

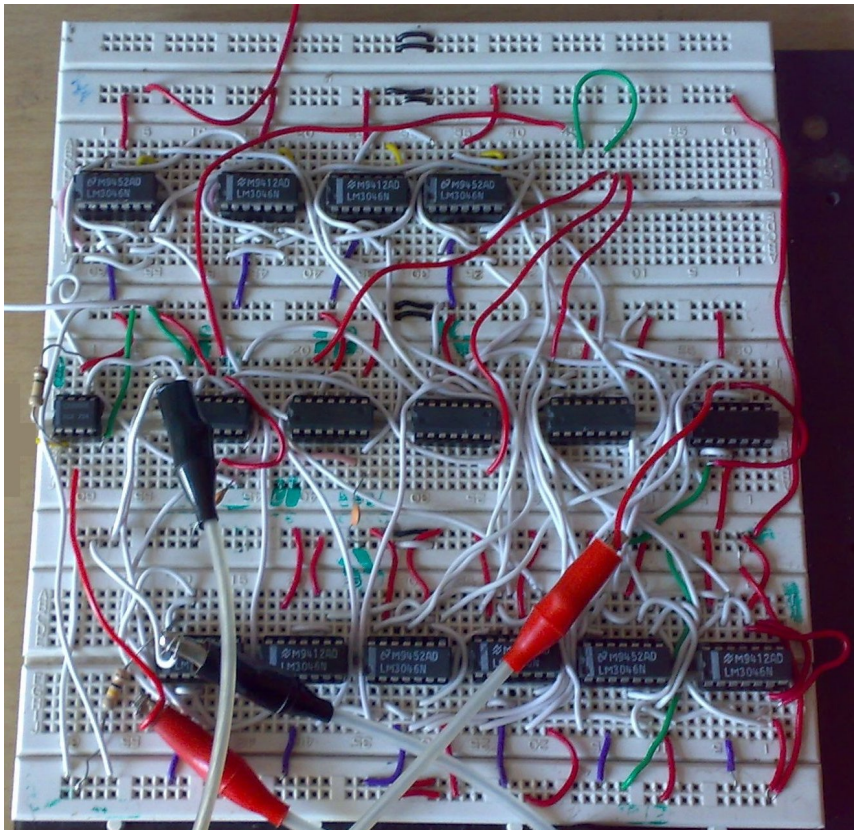


Fig. 3.11: *Bread-board realization of the MIMO universal filter.*

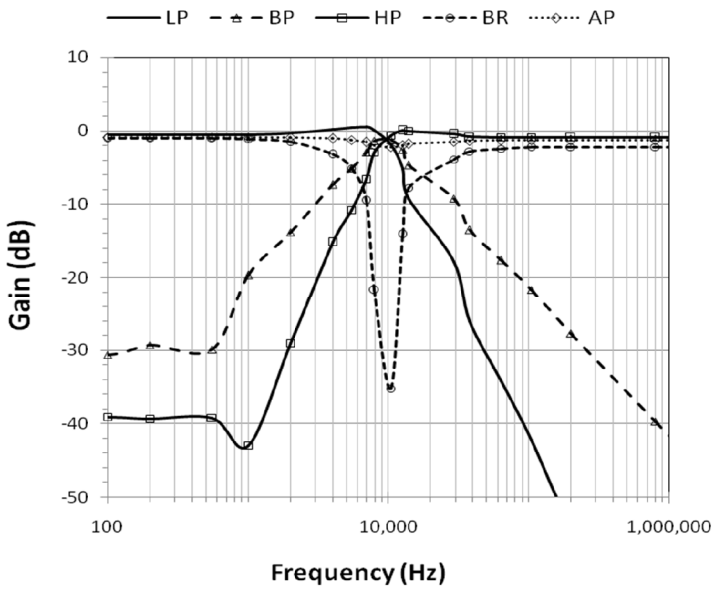


Fig. 3.12: *Measured frequency response of the MIMO universal filter for a 50 μA (peak value) input signal.*

3.1.1.2.2. Proposed Arbitrary-Order Universal Filter Topologies [J5]-[J8], [J11]

3.1.1.2.2.1. Single-Input-Multiple-Output (SIMO) Universal Filters

3.1.1.2.2.1.1. All-pole filters

Functional block diagrams (FBDs) of an arbitrary even and odd order all-pole filter based on the Follow-the-Leader Feedback (FLF) multiple-loop topology are depicted in Figs. 3.13(a) and 3.13(b), respectively.

Defining the product of the time constants τ_1, τ_2, . . . , τ_j as $\tau_1.\tau_2.....\tau_j \equiv 1/b_{n-j}$ (j = 1, 2, . . . , n), the derived highpass (HP), lowpass (LP) and bandpass (BP) transfer functions are given by (3.13)–(3.15), respectively

$$H_{HP}(s) = \frac{v_{HP}}{v_{in}} = -\frac{s^n}{s^n + b_{n-1}s^{n-1} + - - - - - - - + b_1 s + b_0} \tag{3.13}$$

$$H_{LP}(s) = \frac{v_{LP}}{v_{in}} = \pm\frac{b_0}{s^n + b_{n-1}s^{n-1} + - - - - - - - + b_1 s + b_0} \tag{3.14}$$

$$H_{BP(n-j)}(s) = \frac{v_{BP(n-j)}}{v_{in}} = \pm\frac{\pm b_{(n-j)}s^{(n-j)}}{s^n + b_{n-1}s^{n-1} + - - - - - - - + b_1 s + b_0} \tag{3.15}$$

$$j = 1,2,.....n-1$$

According to (3.15), a symmetrical BP filter function is derived for j = n/2 in the case of an even-order filter, while all the other BP filter functions BP (n – j) realized in the case of an odd-order filter could be considered as asymmetrical.

An examination of Fig. 3.13 reveals, that it consists of lossless integrators, arranged one after the other with feedbacks from their outputs to the summation block. Depending on the type of integrator, their order of sequence and type of feedback, as many as four stable filter configurations can be obtained from FBD which are discussed hereunder:

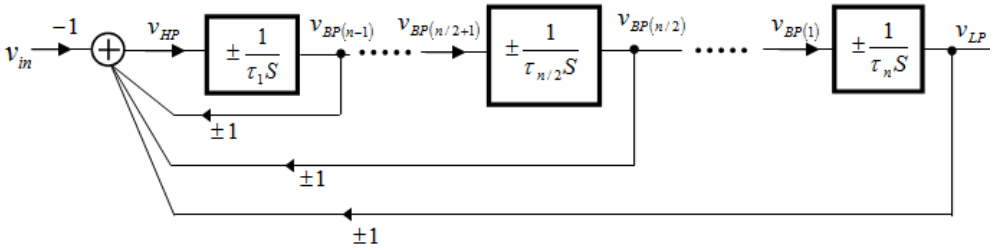
Filter Topology 1 (FT1): Non-inverting lossless integrator followed by inverting lossless integrator with positive and negative feedbacks from their respective outputs.

Filter Topology 2 (FT2): Non-inverting lossless integrators are arranged one after the other with negative feedbacks from their outputs.

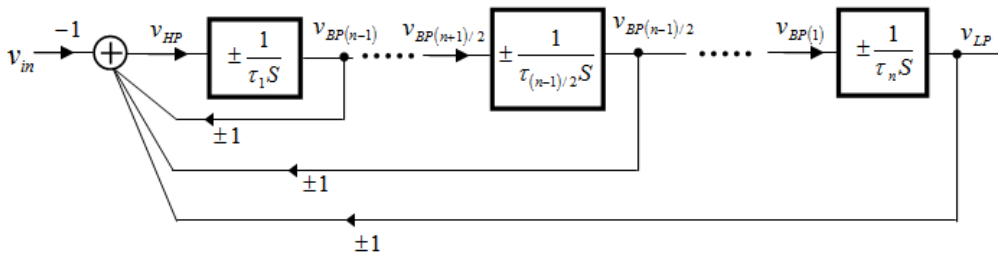
Filter Topology 3 (FT3): Inverting lossless integrator and Non-inverting lossless integrator arranged one after the other with positive feedbacks from their outputs.

Filter Topology 4 (FT4): Inverting lossless integrators are arranged one after the other with positive and negative feedbacks taken alternately from their outputs.

The order of the filter and its configuration determines the non-inverting or inverting mode of the transfer function as summarized in Table 3.3. It is worth to mention here that it is very important to know the mode of every output in each configuration as it determines how they will be involved in algebraic summation to achieve BS and AP filtering functions discussed in the next section. In addition, the four configurations presented above are the only achievable stable designs from the generic SIMO design as is demonstrated for 2nd–order in Table 3.4.



(a)



(b)

Fig. 3.13: *FBDs of the Generic SIMO all-pole FLF filter topologies: (a) Even Order and (b) Odd Order.*

Order	Filter Topology 1				Filter Topology 2				Filter Topology 3				Filter Topology 4			
	LP	BP1	BP2	BP3	LP	BP1	BP2	BP3	LP	BP1	BP2	BP3	LP	BP1	BP2	BP3
1	I	NA	NA	NA	I	NA	NA	NA	NI	NA	NA	NA	NI	NA	NA	NA
2	NI	I	NA	NA	I	I	NA	NA	NI	NI	NA	NA	I	NI	NA	NA
3	NI	NA	NI	I	I	NA	I	I	I	NA	NI	NI	NI	NA	I	NI
4	I	NI	NA	NA	I	I	NA	NA	I	NI	NA	NA	I	I	NA	NA
5	I	NA	NI	NI	I	NA	I	I	NI	NA	I	NI	NI	NA	NI	I
6	NI	NI	NA	NA	I	I	NA	NA	NI	I	NA	NA	I	NI	NA	NA
7	NI	NA	I	I	I	NA	I	I	I	NA	I	I	NI	NA	I	NI
8	I	I	NA	NA	I	I	NA	NA	I	I	NA	NA	I	I	NA	NA
9	I	NA	I	NI	I	NA	I	I	NI	NA	NI	I	NI	NA	NI	I
10	NI	I	NA	NA	I	I	NA	NA	NI	NI	NA	NA	I	NI	NA	NA
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .

Table 3.3: *Signs (Non-Inverting or Inverting) of the filter functions (HP is Inverting in all Configuration). (NA: Not Applicable, I: Inverting, NI: Non-Inverting, BP1: $BP_{(n/2)}$, BP2: $BP_{(n+1)/2}$, BP3: $BP_{(n-1)/2}$).*

3.1.1.2.2.1.2. Filters with finite transmission zeros

The derivation of filters with finite transmission zeros could be achieved using the FBD given in Fig. 3.14. According to the FBD in Fig. 3.14 (a), which is valid for an even-order filter, the bandstop (BS) filter function is given by the expression in Equation (3.16) as

$$H_{BS}(s)=\frac{v_{BS}}{v_{in}}=-\left[H_{HP}(s)\pm H_{BP(n-2)}(s)\pm H_{BP(n-4)}(s)\pm\ldots\pm H_{BP(2)}(s)\pm H_{LP}(s)\right] \tag{3.16}$$

Using the expressions in Equations (3.13)–(3.15), the above transfer function could be alternatively written as in Equation (3.17)

$$H_{BS}(s)=\frac{v_{BS}}{v_{in}}=\frac{s^n+b_{n-2}s^{n-2}+b_{n-4}s^{n-4}+\ldots+b_2s^2+b_0}{s^n+b_{n-1}s^{n-1}+-------+b_1s+b_0} \tag{3.17}$$

The allpass (AP) filter function is given by the expression used in Equation (3.18) as

$$H_{AP}(s)=\frac{v_{AP}}{v_{in}}=-\left[\pm H_{BP(n-1)}(s)\pm H_{BP(n-3)}(s)\pm\ldots\pm H_{BP(1)}(s)+H_{BS}(s)\right] \tag{3.18}$$

Using the expressions in Equations (3.15) and (3.17), the above transfer function could be alternatively written as in Equation (3.19)

$$H_{AP}(s)=\frac{v_{AP}}{v_{in}}=-\frac{s^n-b_{n-1}s^{n-1}+b_{n-2}s^{n-2}+\ldots+b_2s^2-b_1s+b_0}{s^n+b_{n-1}s^{n-1}+-------+b_1s+b_0} \tag{3.19}$$

Mode of Integrators*		Type of Feedback#		HP Transfer Function	Stability Status~
I_1	I_2	F_1	F_2		
NI	NI	+	+	$\frac{s^2}{s^2-\frac{s}{\tau_1}-\frac{1}{\tau_1\tau_2}}$	U
NI	I	+	-		
I	NI	-	-		
I	I	-	+		
NI	NI	+	-	$\frac{s^2}{s^2-\frac{s}{\tau_1}+\frac{1}{\tau_1\tau_2}}$	U
NI	I	+	+		
I	NI	-	+		
I	I	-	-		
NI	NI	-	+	$\frac{s^2}{s^2+\frac{s}{\tau_1}-\frac{1}{\tau_1\tau_2}}$	U
NI	I	-	-		
I	NI	+	-		
I	I	+	+		
NI	NI	-	-	$\frac{s^2}{s^2+\frac{s}{\tau_1}+\frac{1}{\tau_1\tau_2}}$	S
NI	I	-	+		
I	NI	+	+		
I	I	+	-		

Table 3.4: *Table demonstrating that the four configurations presented are the only stable ones.*

*I_1: First Integrator after Summation, I_1: Second Integrator after Summation, NI: Non-Inverting, I: Inverting.

#F_1: Feedback from first integrator, F_2: Feedback from second integrator.

~U: Unstable, S: Stable.

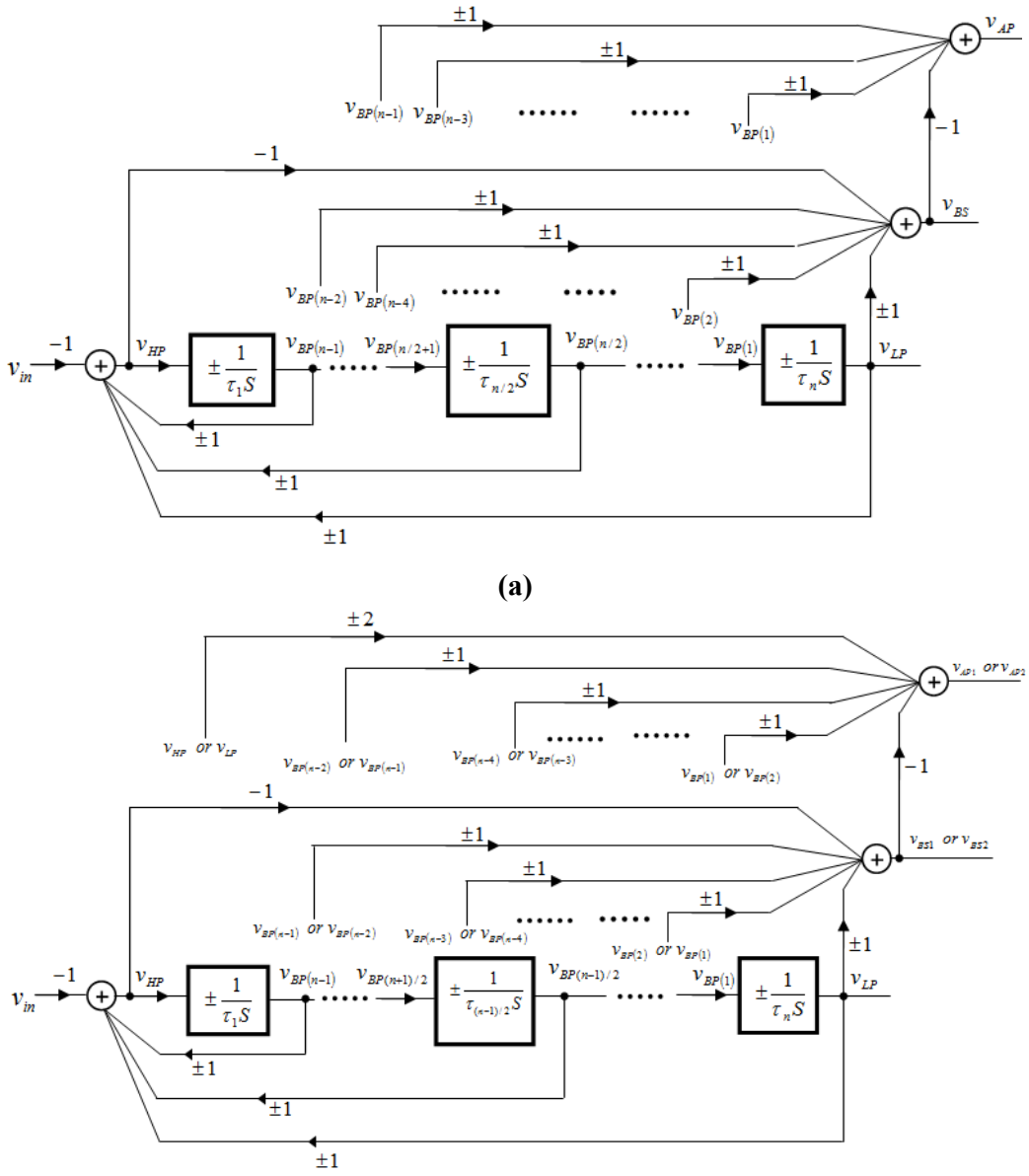


Fig. 3.14: *FBDs of the Generic SIMO all-pole FLF filter topologies with finite transmission zeros: (a) Even Order and (b) Odd Order.*

According to the FBD shown in Fig. 3.14(b), the derivation of an odd-order BS filter with finite transmission zeros could be achieved by the following ways:

(a) According to the formula in Equation (3.20)

$$H_{BS1}(s)=\frac{v_{BS1}}{v_{in}}=-\left[H_{HP}(s)\pm H_{BP(n-1)}(s)\pm H_{BP(n-3)}(s)\right.$$
$$\left.\pm\ldots\pm H_{BP(2)}(s)\pm H_{LP}(s)\right] \qquad (3.20)$$

and the resulting filter will be denoted as BS1.

(b) According to the formula in Equation (3.21)

$$H_{BS2}(s)=\frac{v_{BS2}}{v_{in}}=-\left[H_{HP}(s)\pm H_{BP(n-2)}(s)\pm H_{BP(n-4)}(s)\pm\ldots\pm H_{BP(1)}(s)\pm H_{LP}(s)\right] \tag{3.21}$$

and the resulting filter will be denoted as BS2.

Using Equations (3.13)–(3.15), (3.20) and (3.21), the corresponding filter functions could be alternatively expressed by Equation (3.22) and Equation (3.23), respectively

$$H_{BS1}(s)=\frac{v_{BS1}}{v_{in}}=\frac{s^n+b_{n-1}s^{n-1}+b_{n-3}s^{n-3}+\ldots+b_2s^2+b_0}{s^n+b_{n-1}s^{n-1}+-------+b_1s+b_0} \tag{3.22}$$

$$H_{BS2}(s)=\frac{v_{BS2}}{v_{in}}=\frac{s^n+b_{n-2}s^{n-1}+b_{n-4}s^{n-3}+\ldots+b_1s^2+b_0}{s^n+b_{n-1}s^{n-1}+-------+b_1s+b_0} \tag{3.23}$$

Having available the BS1 and BS2 filter functions, the corresponding AP filter function could be alternatively derived by the formulas given by Equation (3.24) and Equation (3.25)

$$H_{AP1}(s)=\frac{v_{AP1}}{v_{in}}=-\left[2H_{HP}(s)\pm H_{BP(n-2)}(s)\pm H_{BP(n-4)}(s)\pm\ldots\pm H_{BP(1)}(s)+H_{BS1}(s)\right] \tag{3.24}$$

$$H_{AP2}(s)=\frac{v_{AP2}}{v_{in}}=-\left[\pm 2H_{LP}(s)\pm H_{BP(n-1)}(s)\pm H_{BP(n-3)}(s)\pm\ldots\pm H_{BP(2)}(s)+H_{BS2}(s)\right] \tag{3.25}$$

Using Equations (3.13)–(3.15), and Equations (3.22)-(3.25), the corresponding filter functions could be alternatively expressed by Equation (3.26) and Equation (3.27), respectively

$$H_{AP1}(s)=\frac{v_{AP1}}{v_{in}}=\frac{s^n-b_{n-1}s^{n-1}+b_{n-2}s^{n-2}+\ldots+b_2s^2-b_1s+b_0}{s^n+b_{n-1}s^{n-1}+-------+b_1s+b_0} \tag{3.26}$$

$$H_{AP2}(s)=\frac{v_{AP2}}{v_{in}}=-\frac{s^n-b_{n-1}s^{n-1}+b_{n-2}s^{n-2}+\ldots+b_2s^2-b_1s+b_0}{s^n+b_{n-1}s^{n-1}+-------+b_1s+b_0} \tag{3.27}$$

3.1.1.2.2.2. Multiple Input Single Output (MISO) Universal Filter

FBD of MISO Universal filter topology of arbitrary order is depicted in Fig. 3.15. The derived transfer function is given by Equation (3.28)

$$v_{out} = \frac{(-1)^n .s^n .S(n).v_{in} + \left[\sum_{i=0}^{n-1} \frac{s^i}{\prod_{j=1}^{n-i} \hat{\tau}_j} .(-1)^i .S(i)\right] v_{in}}{s^n + \sum_{i=0}^{n-1} \frac{s^i}{\prod_{j=1}^{n-i} \hat{\tau}_j}} \tag{3.28}$$

Again defining the product of the time constants $\tau_1, \tau_2, ..., \tau_j$ as $\tau_1.\tau_2.....\tau_j \equiv 1/b_{n-j}$ (j = 1, 2, . . . , n), Equation (3.28) can be alternatively written as

$$v_{out} = \frac{\left\{(-1)^n .s^n .S(n) + (-1)^{n-1} .b_{n-1} .s^{n-1} .S(n-1) + (-1)^n .b_{n-2} .s^n .S(n-2) + ... + (-1)^n .b_1 .s^n .S(1) + (-1)^n .b_2 .s^n .S(0)\right\} v_{in}}{s^n + b_{n-1}s^{n-1} + - - - - - - - + b_1 s + b_0} \tag{3.29}$$

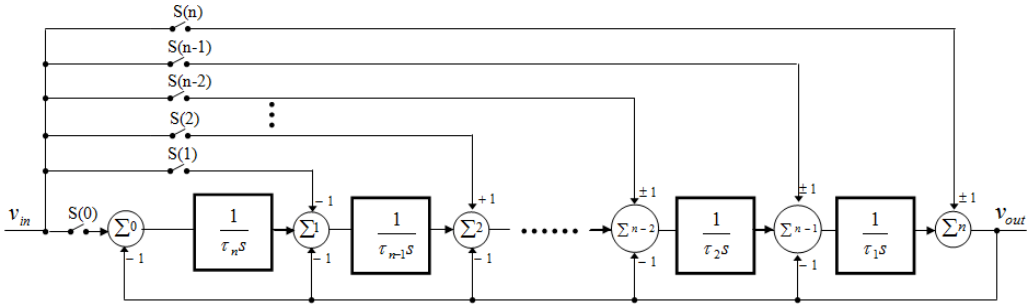


Fig. 3.15: *FBD of the MISO Universal filter topology.*

From Equation (3.29), it is revealed that the five different generic filtering functions can be obtained from the universal filter structure shown in Fig. 3.15 by the following specifications:

- **i)** Low-pass: Close $S(0)$, but open all other $S(i)$.
- **ii)** Band-pass: Close $S(n/2)$ when n is even or close $S((n \pm 1)/2)$ when n is odd, but open all other $S(i)$.
- **iii)** High-pass: Close $S(n)$ but open all other $S(i)$.
- **iv)** Notch: Close both $S(0)$ and $S(n)$ but open all other $S(i)$.
- **v)** All-pass: Close all of the switches.

3.1.1.2.2.3. LD design [J5]-[J7]

The LD design of the proposed filter (SIMO) has been published in **[J5]-[J7].** It is worth to mention here that the results of Lowpass (LP), Bandpass (BP) and Highpass (HP) were only presented in the said publications (FT1-FT4 corresponds to, Multi-Function Filter (MFF), MFF1-MFF4).

To transpose Generic FBD to its LD counterpart, the LD blocks mentioned in section 2.3.1 were used. The following step together with the ones mentioned at the start of this section were followed for the LD transposition:

- ✓ dc stabilize the circuit by applying the rules contained in **[50]** according to which at least one pair of E+ and E− cells must have their outputs connected to each capacitor node and the sum of dc bias currents of E+ cells with their outputs connected at a node should be equal to the corresponding sum of dc bias currents of E− cells with their outputs connected at the same node.

Following the mentioned steps, we obtain the transposed Generic FBD of the LD MFF filter topology depicted in Fig. 3.16. The transfer functions in Equations (3.13-3.15) are now expressed as

$$H_{HP}(s)=\frac{EXP(\hat{v}_{HP})}{EXP(\hat{v}_{in})}=-\frac{s^n}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.30}$$

$$H_{LP}(s)=\frac{EXP(\hat{v}_{LP})}{EXP(\hat{v}_{in})}=\pm\frac{b_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.31}$$

$$H_{BP(n-j)}(s)=\frac{EXP(\hat{v}_{BP(n-j)})}{EXP(\hat{v}_{in})}=\pm\frac{\pm\hat{b}_{(n-j)}s^{(n-j)}}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0},\quad j=1,2,.....n-1 \tag{3.32}$$

3.1.1.2.2.3.1. Simulation results

To verify the validity of the proposed design, 5th-order LD MFF of each configuration depicted respectively in Figs. 3.17(a)-3.17(d) were constructed for $V_{CC} = V_{EE} = 1.5$ V, $I_o = 25$ μA and $C = 15.9$ *pF* which yield cut-off/centre frequency $(f_C) = 10$ *MHz*. The NPN transistors in cell implementations are simulated using the NR100 model parameters of Table 3.1. The frequency behaviour of the filter was evaluated by performing large-signal transient analysis using the PSPICE simulator, with

modulation index factor $m=i_{peak}/I_o$ = 50%. The small deviations, caused by bipolar transistor imperfections, have been compensated by following the procedure suggested in **[48].** The values of the compensation factors were: $K_{RE} = 0.999$, $K_{RB} = 0.996$, $K_\beta = 0.986$, $K_{1VA} = 1$, $k_{2VA} = 0.99$, $f_\beta = 0.00019$, and $f_{VA} = 0.0013$. Also, the DC bias currents for the final stage of the filter are multiplied by a factor 1.0086. The compensated magnitude responses of 5th order LD MFF topologies are given in Figs. 3.18(a)-3.18(d). The electronic tunability of cut-off frequency and gain of MFFs has been verified for different values of the bias current as shown in Fig. 3.19.

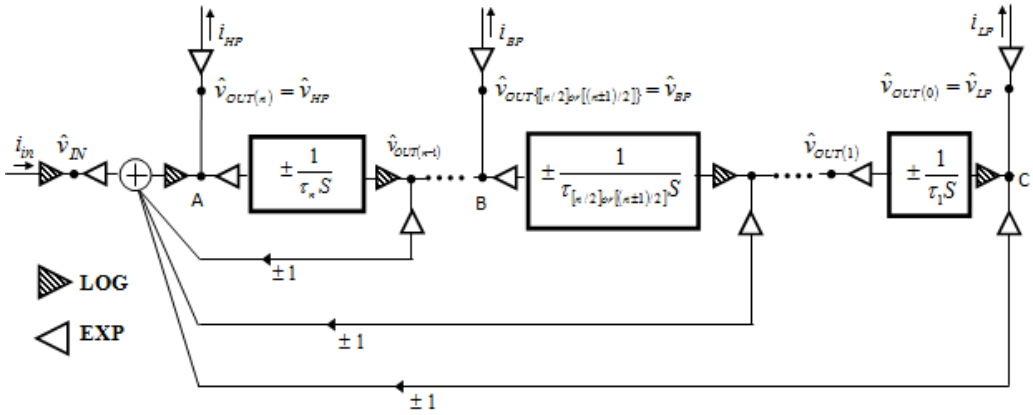


Fig. 3.16: *Transposed MFF topology of the filter in Fig. 3.13 into LD.*

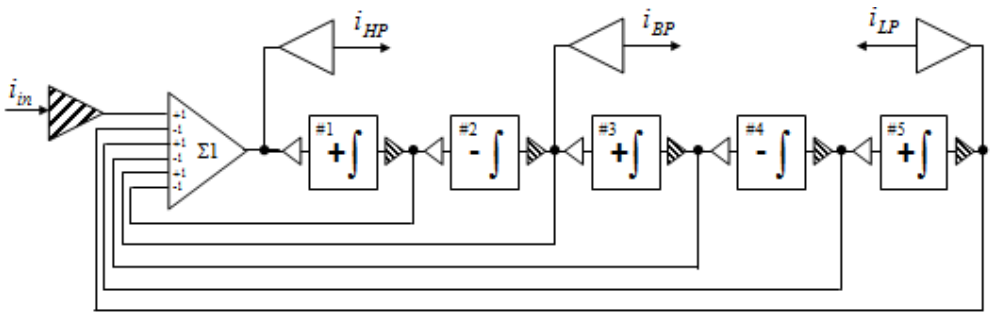
A comparative study of the proposed circuits was carried out on the basis of usually used parameters of non-linear behaviour, number of components, sensitivity and power consumption.

To study the non-linear behaviour of proposed SD universal biquadratic filter topology, IMD3 (for LP response) test was employed. For this purpose two closely spaced tones 3 MHz and 3.2 MHz, which fall in the passband of the LP response, were applied at the input of each of the filters. The simulated values of distortion at m = 100 for the biquads are given in Table 3.5.

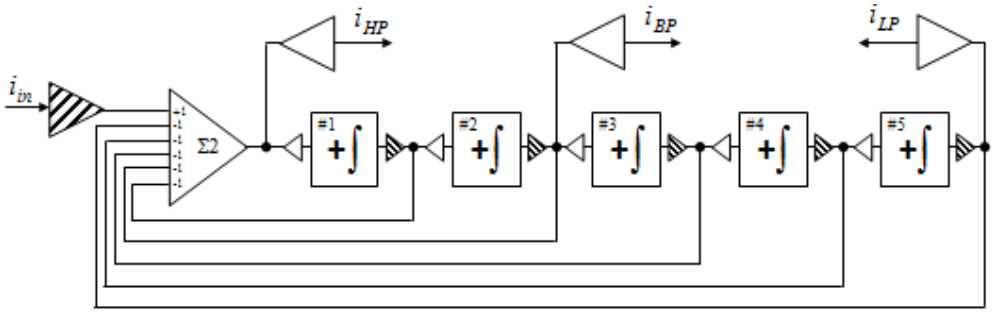
Also, the simulated IMD3 responses as a function of the modulation index factor, is given in Fig. 3.20. Further, Table 3.5 also contains computed data about simulated rms values of the output noise currents integrated over 20 MHz range, dynamic ranges (DR) at 0.3 % distortion level, number of devices required and static power consumption. For obtaining sensitivity graph, Monte Carlo analysis with 100 runs assuming 1 % deviation (with Gaussian distribution) was carried out with respect to the variations of the transistor mismatches, integrating capacitors and bias currents.

From this graph the values of standard deviation (STD) and mean variance (MV) of the maximum gain and cut-off frequency were calculated as given in Table 3.6.

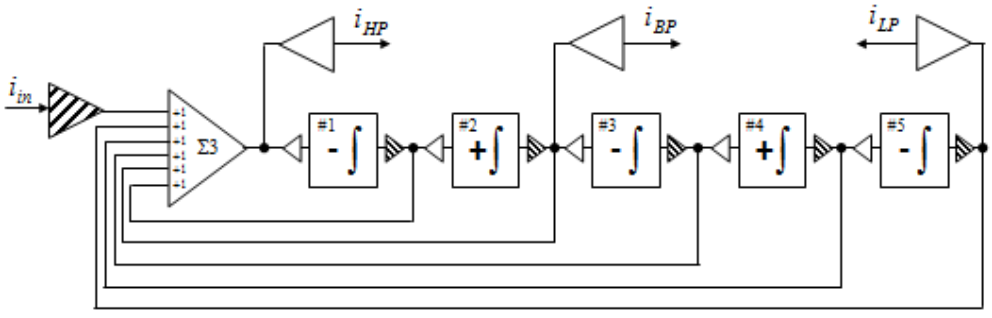
The results of Tables 3.5 and 3.6 reveal that each design has different performance for different set of parameters, thereby, facilitating application specific selection of MFF design. Further one can see from the comparative study that MFF1 is better design as most of its performance factors are superior vis- a-vis other designs.



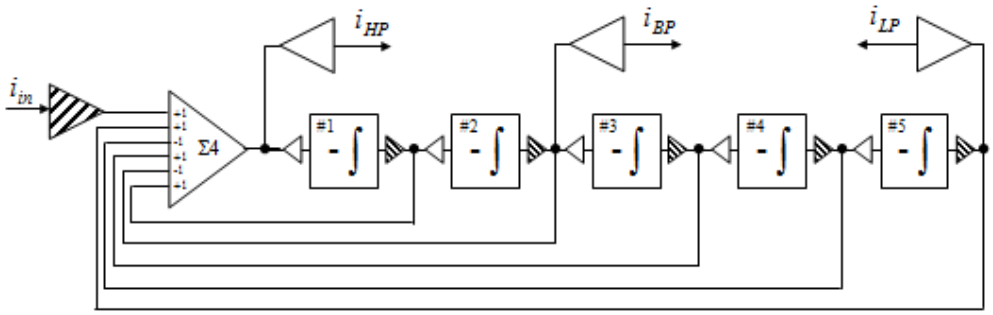
(a)



(b)



(c)



(d)

Fig. 3.17: *Topologies of the 5th-order generic LD MFF of Fig. 3.16. (a) MFF1 (b) MFF2 (c) MFF3 (d) MFF4.*

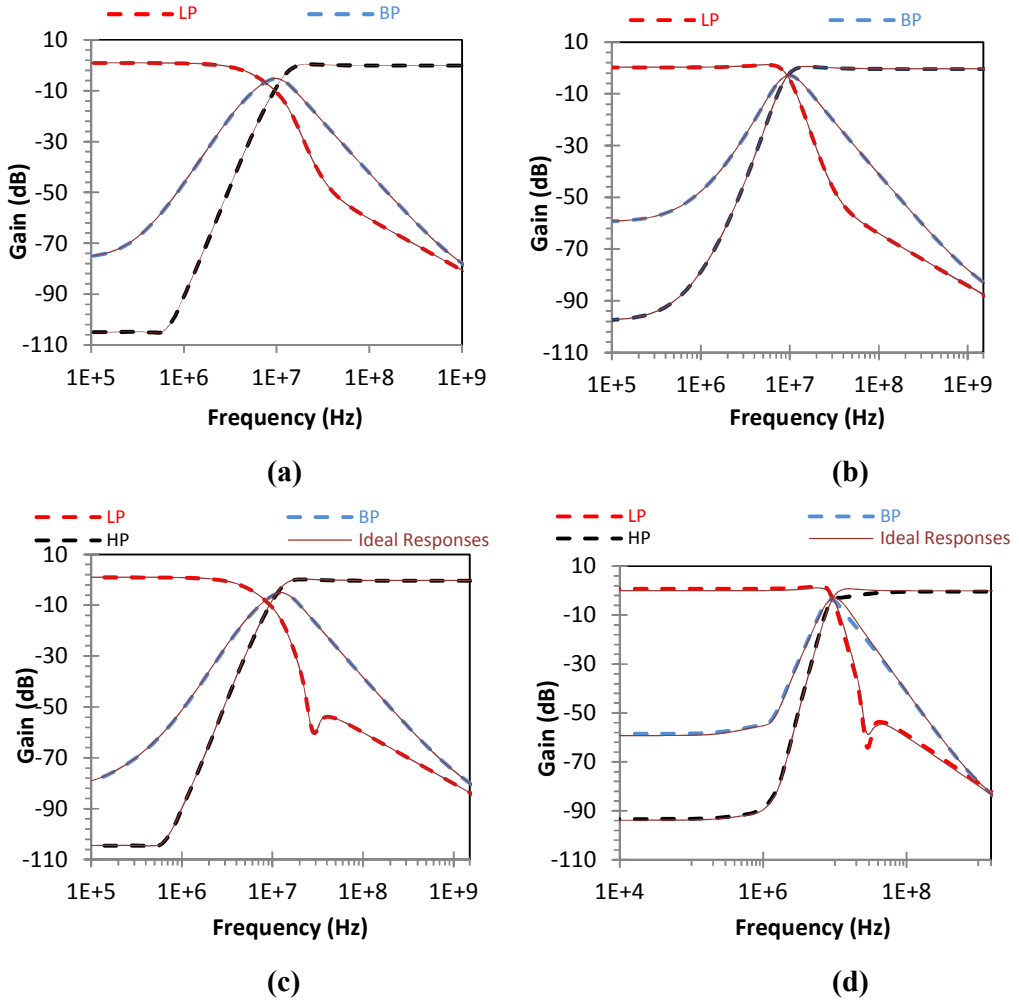


Fig. 3.18: *Simulated magnitude responses of standard filter functions of MFFs of Fig. 3.17. (a) MFF1 (b) MFF2 (c) MFF3 (d) MFF4.*

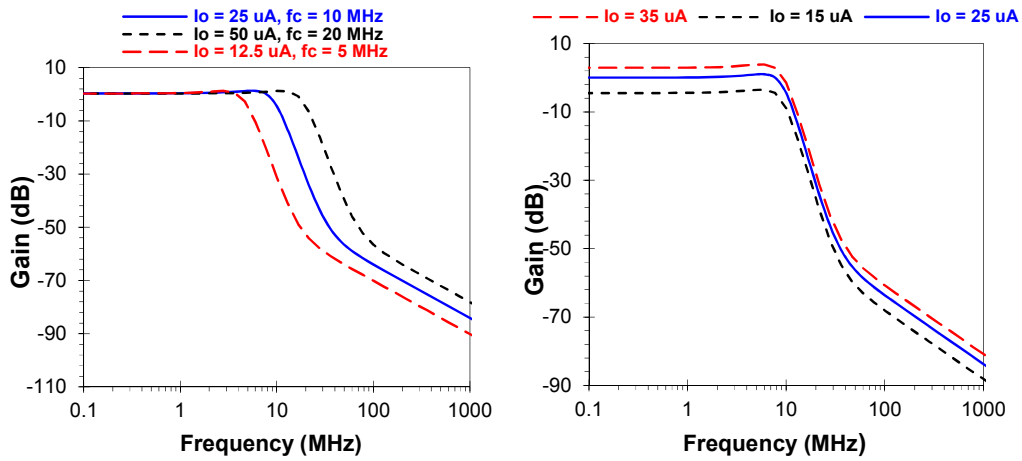


Fig. 3.19: *Demonstration of electronic tunability of cut-off frequency and gain of MFFs.*

MFF/Par.	IMD3. at m=100%	*rms* output I_{noise} (nA)	DR @ 0.3% IMD3 level (dB)	No. of Components		Static Power Consumption (mW)
				Tr.	Cs	
MFF1	-49 dB	230	36.82	66	38	3.62
MFF2	-45.9 dB	240.1	35.24	72	36	3.76
MFF3	-41 dB	250.3	33.75	60	40	3.48
MFF4	-47.8 dB	236.4	35.82	60	40	3.43

Table 3.5: *Comparison of nonlinearity, component count and power dissipation of MFFs of Fig. 3.17.*

MFF	Gain		Cut-off Frequency		IMD3 at m=100%	
	STD	MV	STD	MV	STD	MV
MFF1	0.0078	0.96	0.252 MHz	9.82 MHz	1.53 dB	-47.7 dB
MFF2	0.0087	0.95	0.284 MHz	9.8 MHz	1.65 dB	-44.5 dB
MFF3	0.0095	0.94	0.288 MHz	9.81 MHz	1.72 dB	-39.4 dB
MFF4	0.0095	0.94	0.292 MHz	9.78 MHz	1.84 dB	-46.1 dB

Table 3.6: *Statistical simulation results about the frequency behaviour of the LP filter functions of LD MFFs of Fig. 3.17.*

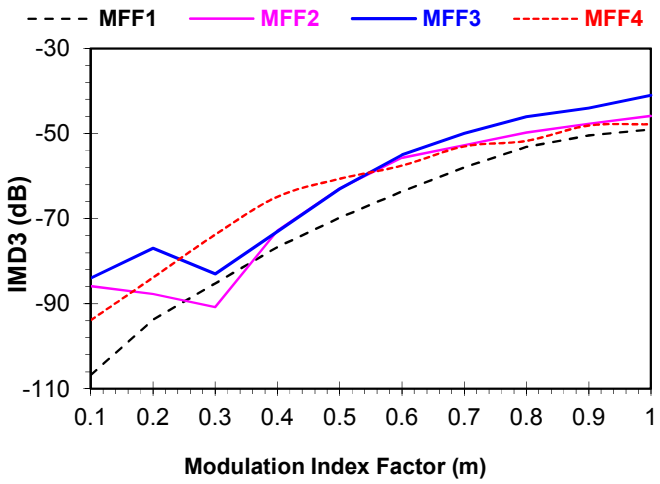


Fig. 3.20: *Linear performance of the LP filter functions of 5th-order LD MFFs of Fig. 3.17.*

3.1.1.2.2.3.2. Comparison

The various advantages offered by the topologies can be best depicted by comparing the LD MFF design with the LD universal/multifunction filters. After a careful look on the literature, **[53, 54]** were found**.** Out of these, **[54]** will be a better choice for comparison. Hence, the 2nd-order versions of MFF2 and **[54]** were implemented using transconductor cells of **[136]** and the model parameters of the NR100N**.** In addition, the following values $V_{CC} = -V_{EE} = 1\,V,\ I_o = 25\,\mu A$ *and* $C = 1.59\,nF$ yield cut-off/centre frequency as $f_C = 100\,KHz$. To study the nonlinear behavior of the designs, IMD3 of LP responses of both the designs was measured. For this purpose, a two-tone test was performed using closely spaced tones 20 KHz and 22 KHz (2% of cut-off frequency) which fall within the pass band of the filters. IMD3 responses of both the designs are drawn in Fig. 3.21. The simulated values of distortion at full-scale input signal ($m = 100\%$) for both the designs are given in Table 3.7. The noise was integrated over 1 MHz range and the simulated rms value of the output noise at LP outputs for both the designs is given in Table 3.7. Also, the signal-to-noise ratio (SNR) versus the modulation index factor (i.e. the ratio of the signal's amplitude to the bias current: $m = i_{peak} / I_O$) for both the designs is plotted in Fig. 3.22. It is worth to mention that the noise values for the two designs were very close to each other as given Table 3.7 and thus SNR versus modulation index factor appears to be a single plot. The achieved DR at 0.2% distortion level for both the designs is given in Table 3.7. To see the effect of variations of the integrating capacitors and bias

currents, the sensitivity comparison for the designs were made. Monte Carlo analysis with 100 runs assuming 5% deviation (with Gaussian distribution) was carried out with respect to the variations of the integrating capacitors and bias currents. The results are plotted in Fig. 3.23. As is evident from the Monte Carlo simulation, design reported in **[54]** show more insensitivity toward both absolute and relative variations in the process parameters around the cut-off frequency than the proposed design. A comparison in terms of component count between the two designs was made and the number of transistors, capacitors and current sources required for 2nd, 4th and 6th-order filters of both the designs (for same filter functions) are given in Table 3.8. It is evident from the results that the increase in the number of components for the order to get increased by two is more in the design reported in **[54]** vis-à-vis the proposed design. The total static power dissipation of the 2nd, 4th and 6th –order filters of both the designs is given in Table 3.8. In addition, for high-order design using design methodology reported in **[54]**, we can cascade the biquads reported in it. But then the overall filter will contain single filter function in contrast to the proposed design which contains all the proposed filter functions irrespective of the order of the filter. Also, the odd-order filter design is not possible with the design of **[54].** Thus, on the basis of above discussion we can conclude that the proposed design offers several advantages over the design reported in **[54].**

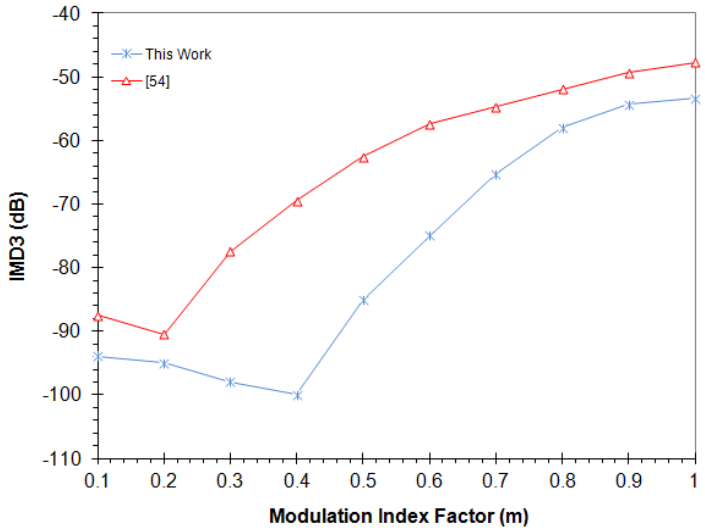


Fig. 3.21: *Third-order intermodulation distortion (IMD3) versus modulation index factor response of biquads of proposed topology and Reference* ***[54].***

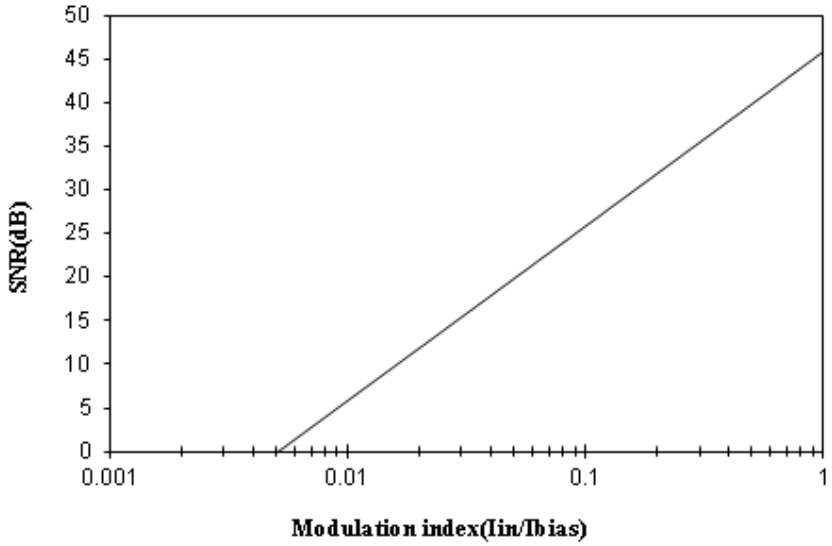
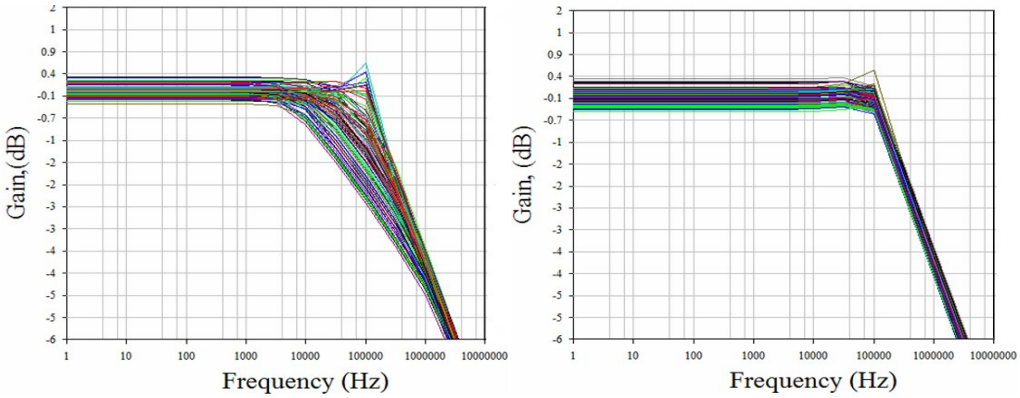


Fig. 3.22: *SNR versus modulation index factor of biquads of proposed design and Reference* ***[54].***



(a) (b)

Fig. 3.23: *Sensitivity of LD filters on integrating capacitor and bias current variations. (a) Reference* ***[54]*** *design. (b) Proposed design.*

Circuit	Distortion at m=1	Output noise	DR @ 0.2% Distortion
This work	-53.37 dB	128 nA	45.7 dB
Reference [54]	-47.75 dB	129 nA	42.6 dB

Table 3.7: *Comparison of non-linearity between the proposed design and Reference* ***[54].***

Circuit	Order	No. of Components			Total Static Power Dissipation
		Transistors	Current Sources	Capacitors	
This work	2nd	31	23	2	2.38 mW
	4th	55	31	4	3.74 mW
	6th	79	39	6	5.1 mW
Reference [54]	2nd	44	22	2	2.8 mW
	4th	70	32	4	4.3 mW
	6th	96	42	6	5.8 mW

Table 3.8: *Comparison of component count and power dissipation between the proposed design and Reference* ***[54].***

3.1.1.2.2.4. SRD design [J8], [J11]

In order to transpose the FBDs in Figs. 3.14 and 3.15 to the corresponding ones into the SRD, the SRD blocks discussed in section 2.3.2 were used. Following the same steps as for LD conversion with exception of using SRD blocks, the transposed FBDs of the SRD SIMO FLF and MISO filter topologies are demonstrated in Figs. 3.24 and 3.25 respectively. The transfer functions in Equations (3.13–3.15, 3.17, 3.19, 3.22, 3.23, 3.26, 3.27 and 3.28) are now expressed as

$$H_{HP}(s)=\frac{SQ(\hat{v}_{HP})}{SQ(\hat{v}_{in})}=-\frac{s^n}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.33}$$

$$H_{LP}(s)=\frac{SQ(\hat{v}_{LP})}{SQ(\hat{v}_{in})}=\pm\frac{b_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.34}$$

$$H_{BP(n-j)}(s)=\frac{SQ(\hat{v}_{BP(n-j)})}{SQ(\hat{v}_{in})}=\pm\frac{\pm\hat{b}_{(n-j)}s^{(n-j)}}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0}, \quad j=1,2,.....n-1 \tag{3.35}$$

$$H_{BS}(s)=\frac{SQ(\hat{v}_{BS})}{SQ(\hat{v}_{in})}=\frac{s^n+\hat{b}_{n-2}s^{n-2}+\hat{b}_{n-4}s^{n-4}+...+\hat{b}_2 s^2+\hat{b}_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.36}$$

$$H_{AP}(s)=\frac{SQ(\hat{v}_{AP})}{SQ(\hat{v}_{in})}=-\frac{s^n-\hat{b}_{n-1}s^{n-1}+\hat{b}_{n-2}s^{n-2}+...+\hat{b}_2 s^2-\hat{b}_1 s+\hat{b}_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.37}$$

$$H_{BS1}(s)=\frac{SQ(\hat{v}_{BS1})}{SQ(\hat{v}_{in})}=\frac{s^n+\hat{b}_{n-1}s^{n-1}+\hat{b}_{n-3}s^{n-3}+...+\hat{b}_2 s^2+\hat{b}_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.38}$$

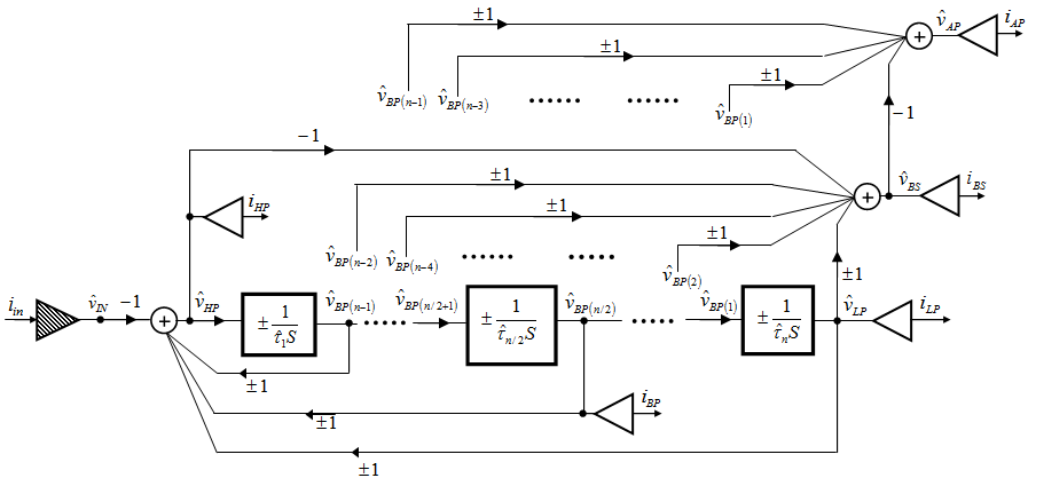
$$H_{BS2}(s)=\frac{SQ(\hat{v}_{BS2})}{SQ(\hat{v}_{in})}=\frac{s^n+\hat{b}_{n-2}s^{n-1}+\hat{b}_{n-4}s^{n-3}+...+\hat{b}_1 s^2+\hat{b}_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.39}$$

$$H_{AP1}(s)=\frac{SQ(\hat{v}_{AP1})}{SQ(\hat{v}_{in})}=\frac{s^n-\hat{b}_{n-1}s^{n-1}+\hat{b}_{n-2}s^{n-2}+...+\hat{b}_2 s^2-\hat{b}_1 s+\hat{b}_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.40}$$

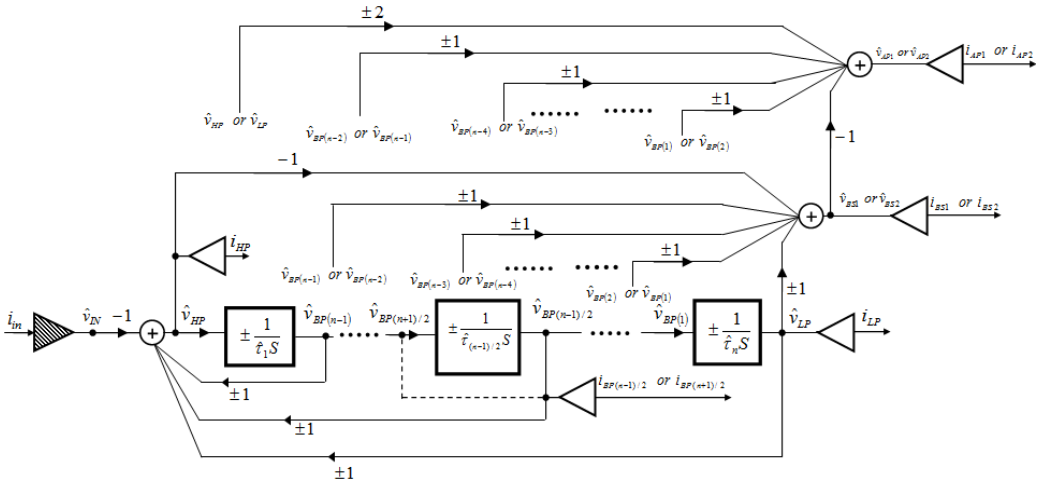
$$H_{AP2}(s)=\frac{SQ(\hat{v}_{AP2})}{SQ(\hat{v}_{in})}=-\frac{s^n-\hat{b}_{n-1}s^{n-1}+\hat{b}_{n-2}s^{n-2}+...+\hat{b}_2 s^2-\hat{b}_1 s+\hat{b}_0}{s^n+\hat{b}_{n-1}s^{n-1}+-------+\hat{b}_1 s+\hat{b}_0} \tag{3.41}$$

Where $\hat{b}_{n-j}\equiv 1/\hat{\tau}_1.\hat{\tau}_2.....\hat{\tau}_j$ (j = 1, 2, . . . , n),

$$SQ(\hat{v}_{OUT}) = \frac{s^n.S(n).SQ(\hat{v}_{IN}) + \left[\sum_{i=0}^{n-1} \frac{s^i}{\prod_{j=1}^{n-i} \hat{\tau}_j}.(-1)^i.S(i)\right] SQ(\hat{v}_{IN})}{s^n + \sum_{i=0}^{n-1} \frac{s^i}{\prod_{j=1}^{n-i} \hat{\tau}_j}} \quad (3.42)$$



(a)



(b)

Fig. 3.24: *Transposed topologies of the Generic SIMO all-pole FLF filter topologies with finite transmission zeros of Fig. 3.14 into SRD: (a) Even Order and (b) Odd Order.*

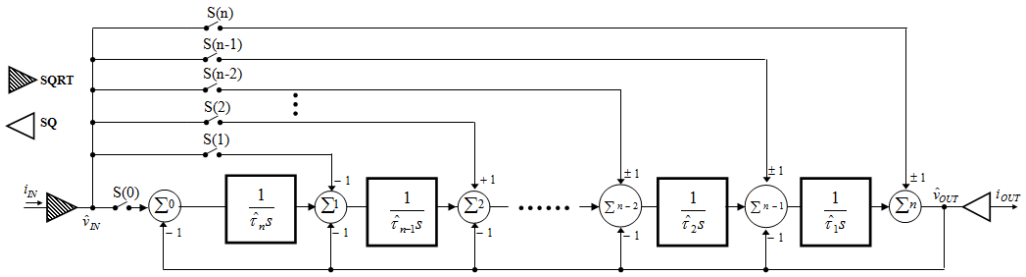


Fig. 3.25: *Transposed topology of MISO Universal filter topology of Fig. 3.15 into SRD.*

3.1.1.2.2.4.1. Simulation Results

The performance of the SRD SIMO and MISO universal filter topologies has been evaluated by employing the PSPICE software. For this purpose, the square root divider block given in Fig. 2.8 will be employed in simulations. In addition, according to Equation (3.42) and the conditions concerning the input currents, three digital control bits b_i (i = 0, 1, 2) are required to select one of the five filter transfer functions in case of 3rd and 4th-order MISO universal filter. Therefore, the switch status condition provided in Table 3.9 has to be followed in order to derive the appropriate filter functions. One possible implementation of the establishment of the required switching scheme is shown in Fig. 3.26.

A single power supply voltage V_{DD} = 1.5V (V_{SS}=0) is employed for biasing all the stages of the universal filter topologies of Figs. 3.24 and 3.25, while the dc current I_0 is chosen to be equal to 5 µA. In the square root divider block of Fig. 2.8, the dc voltage V_{DC} has been chosen equal to 900 mV. Having available the technology parameters provided by the BSIM 0.35-µm CMOS process, the MOS transistor aspect ratios of the cell in Fig. 2.8 are summarized in Table 3.10. The aspect ratio of PMOS transistors employed in summation blocks was 120µm/2µm. Due to the fact that the aspect ratios of NMOS transistors employed in integration, summation and

compression/expansion blocks were chosen to be 1.3μm/2μm, the equivalent SRD resistor in the expression of time constants in the SRD, given by the formula $\hat{R} = 1/\sqrt{2KI_0}$, was 38.1 kΩ.

As a design example, the 3rd and 4th-order universal filters were designed in each of the SIMO and MISO configurations as shown in Figs. 3.27, 3.28 and 3.29. The capacitors for 3rd–order filter were chosen as $\hat{C}_1 = 20.3pF, \hat{C}_2 = 40.3pF$ *and* $\hat{C}_3 = 85pF$ and that of 4th–order filter were chosen as $\hat{C}_1 = 15.81pF, \hat{C}_2 = 31.26pF, \hat{C}_3 = 53.5pF$ *and* $\hat{C}_4 = 104.65pF$. With above values of equivalent resistor and capacitors, resonant frequency f_0 = 105.55 KHz for 3rd-order SIMO filter and 102.8 KHz for 4th-order SIMO filter. The dc power dissipations for the universal filter topologies of Figs. 3.27, 3.28 and 3.29 were as given Table 3.11. With $i_{in} = 2\mu A$, the simulated frequency responses of 3rd and 4th order SIMO and MISO universal filters of Figs. 3.27, 3.18 and 3.29 are given in Figs. 3.30, 3.31 and 3.32 respectively.

Monte Carlo analysis with 100 runs assuming 5% deviation (with Gaussian distribution) was carried out with respect to the variations of the integrating transistor mismatches, capacitors and bias currents. The results are plotted in Figs. 3.33, 3.34 and 3.35. The simulated values of standard deviations of the maximum gain and center frequency are given in Table 3.11.

To study the non-linear behaviour of the proposed SIMO and MISO universal filters, 3rd-order IMD3 test was employed. Accordingly two closely spaced tones which fall in the passbands of their BP responses were applied at the input of the filter. The rms values of the output currents, at 1% distortion level are given in Table 3.11. Integrating the noise over a 150 kHz range, the simulated rms values of the

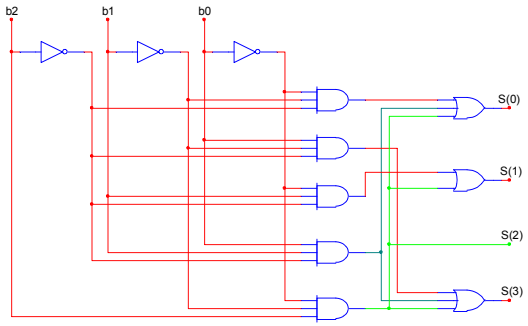
noise output current for all the cases are also given in Table 3.11. The predicted DR, at distortion level 1%, would be as that given in Table 3.11.

The performance of the proposed SIMO and MISO universal filter topologies have been compared, in terms of power efficiency, with the 2nd-order SIMO and MISO universal LD **[147]** and SRD **[139]** filter topologies. For this purpose, the Figure of Merit (FOM) given by Equation (3.43), would be employed

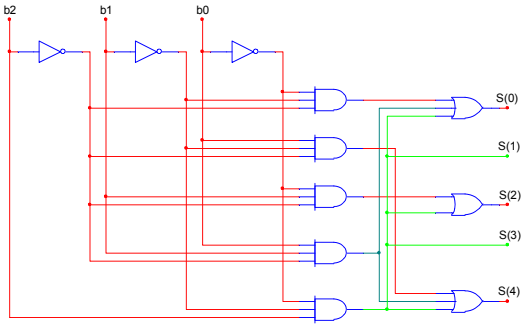
$$FOM = \frac{P}{n \cdot f_o \cdot (DR)} \tag{3.43}$$

where P is the power dissipation of the filter, n is the number of poles, f_o is the cut-off frequency, and DR is the dynamic range.

The derived comparison results are summarized in Table 3.12, where it could be concluded that the proposed SIMO and MISO universal filter topologies offer more power efficient designs than the reported. In addition, from Table 3.12, it could readily be obtained that the MISO universal filter topology offers a more power efficient design than that of the SIMO universal filter configurations.

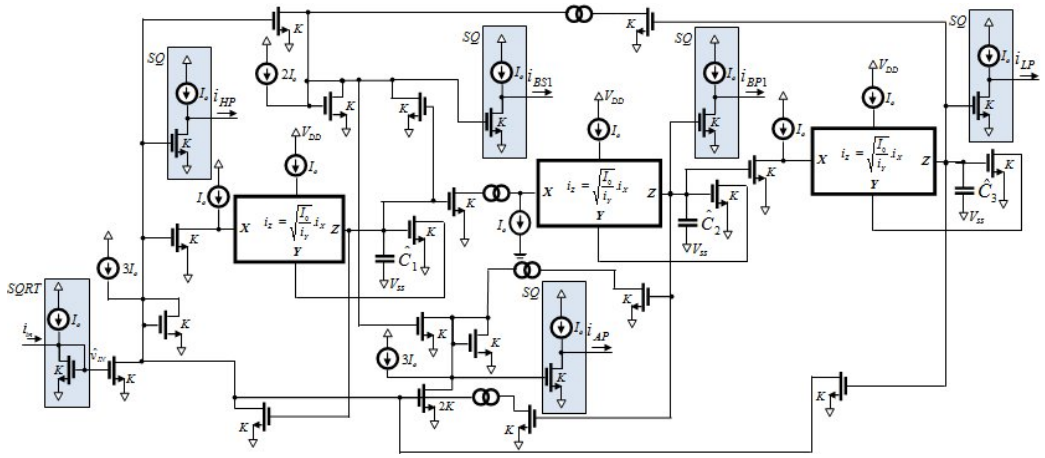


(a)

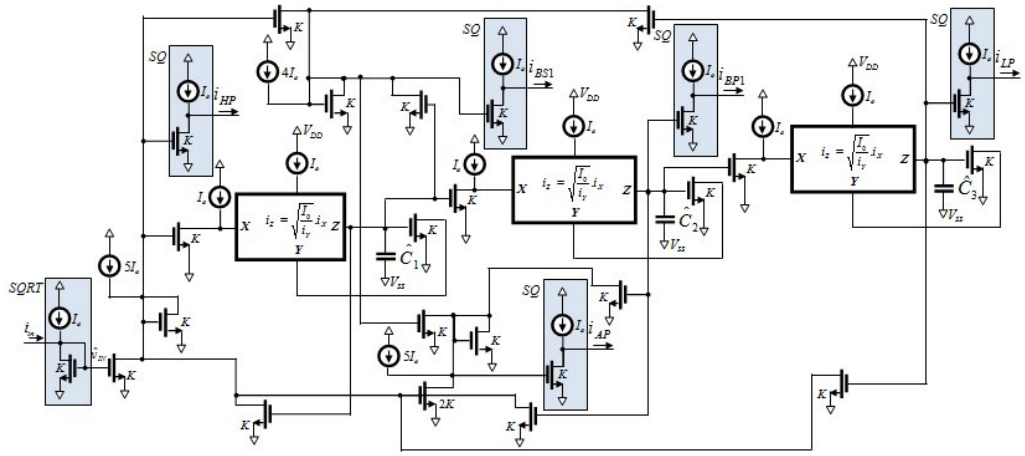


(b)

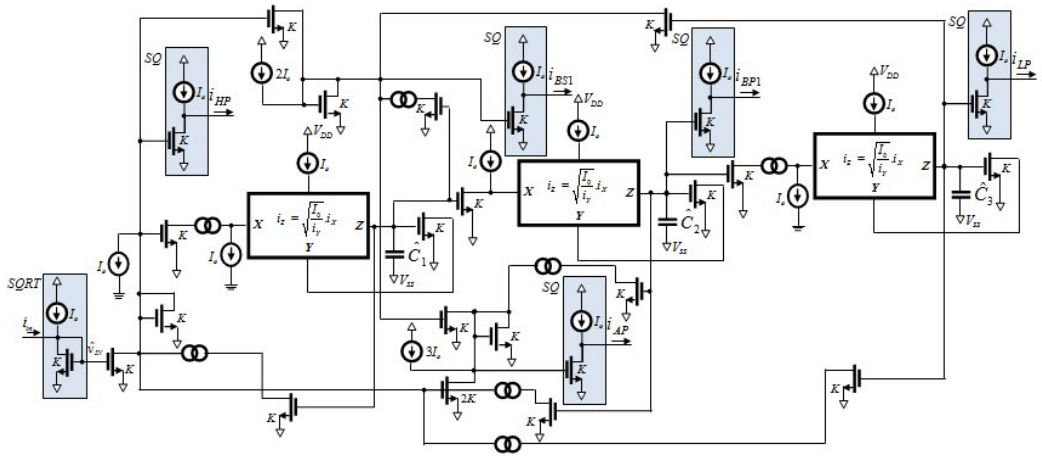
Fig. 3.26: *Circuit schemes for filter function selection in 3rd and 4th–order MISO universal topologies.*



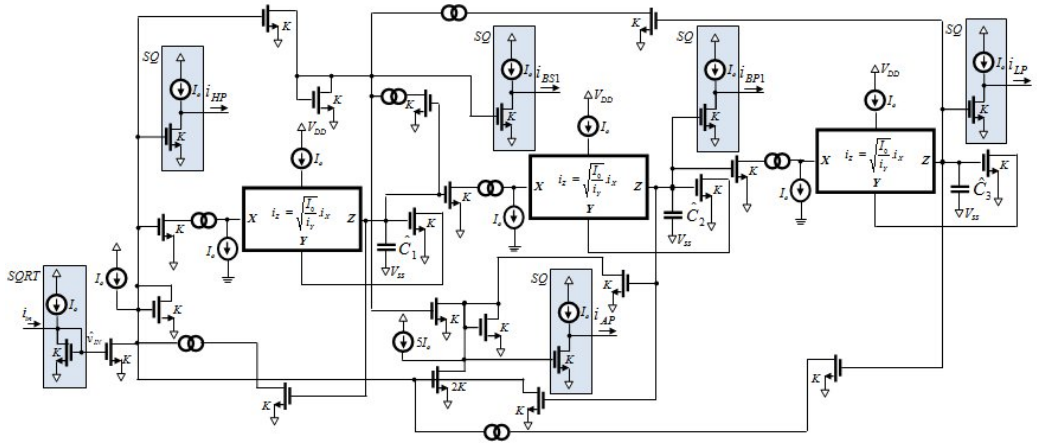
(a)



(b)

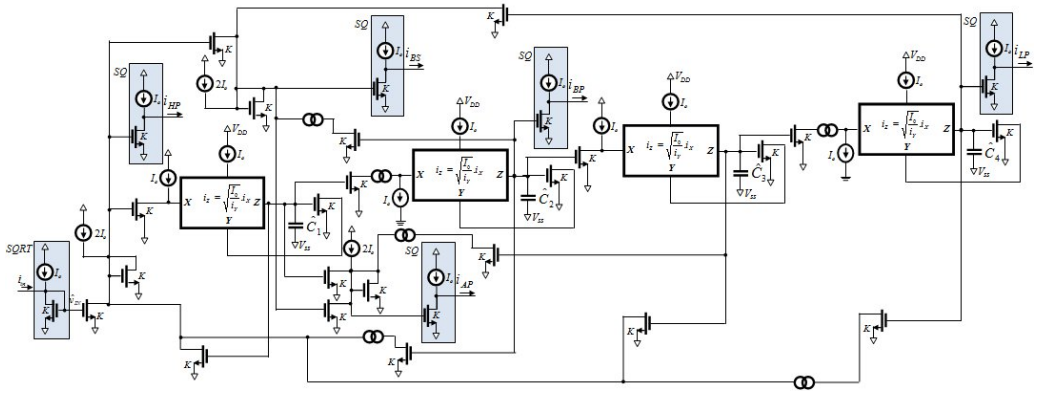


(c)

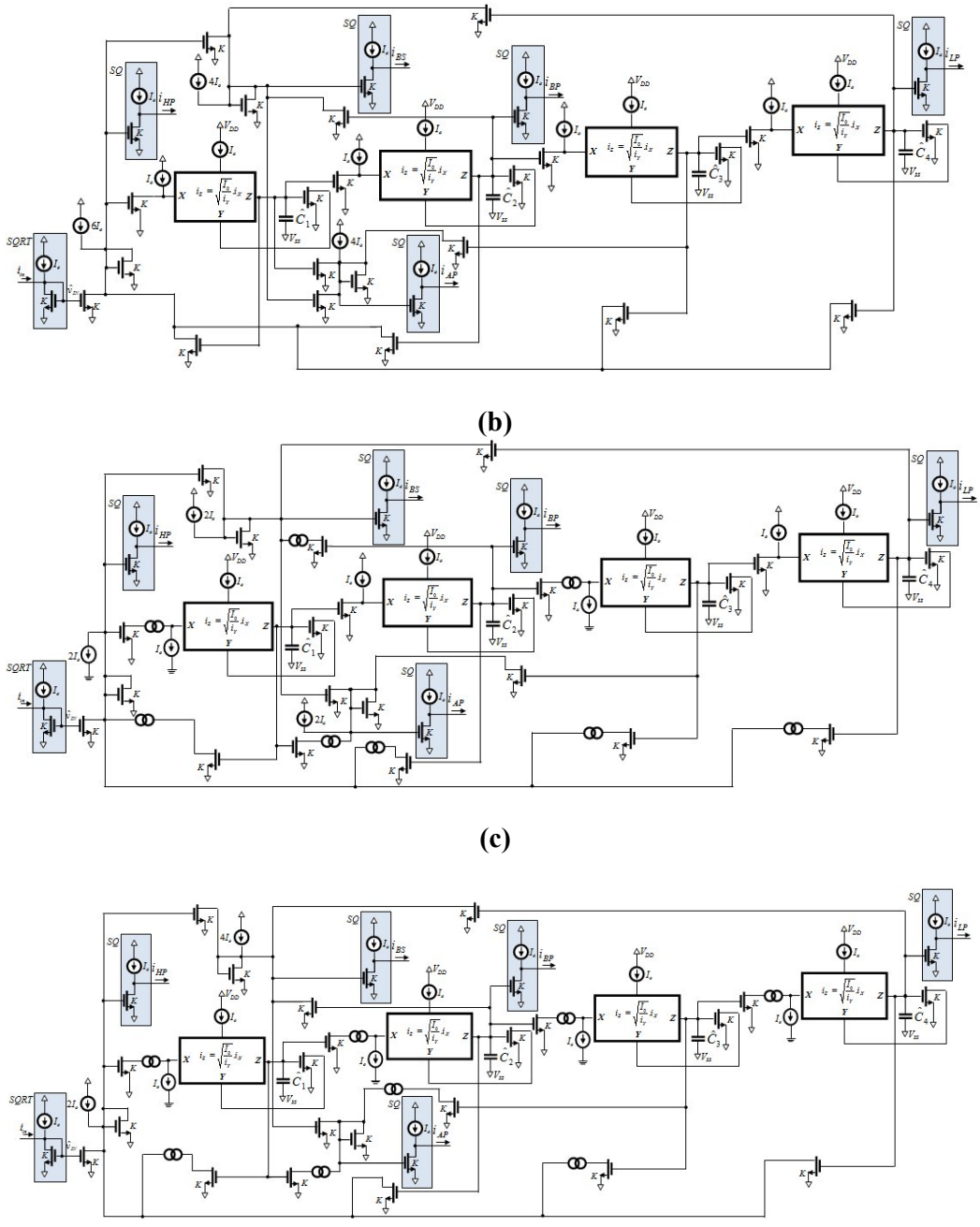


(d)

Fig. 3.27: *3rd–order SRD SIMO universal topologies: (a) FT 1, (b) FT 2, (c) FT 3, and (d) FT 4.*



(a)

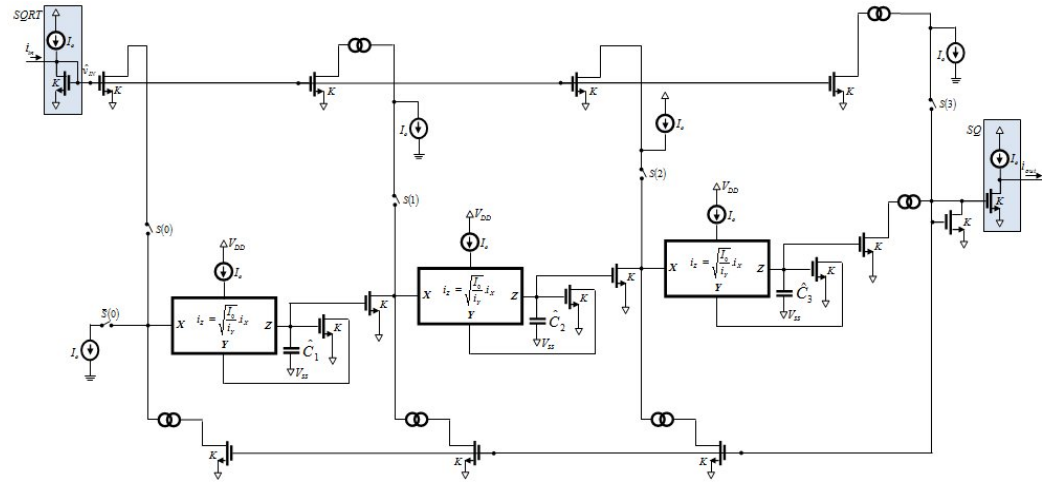


(b)

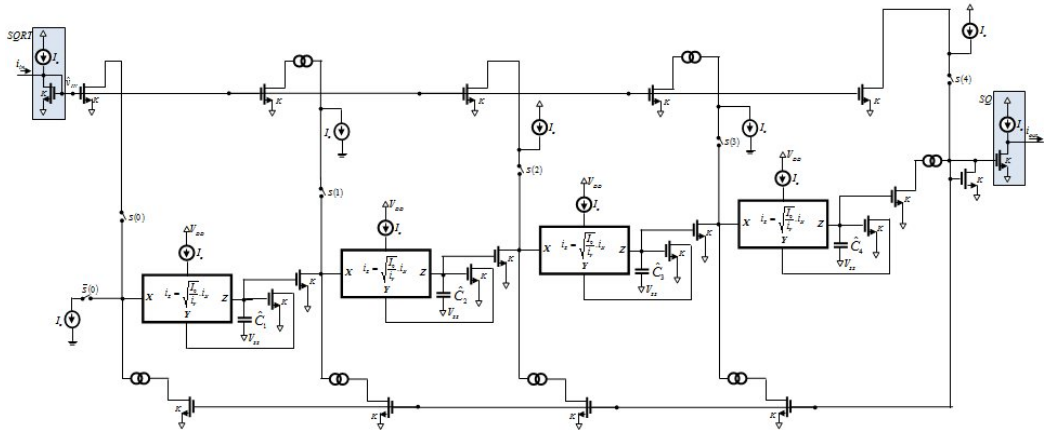
(c)

(d)

Fig. 3.28: *4[th]–order SRD SIMO universal filter topologies: (a) FT 1, (b) FT 2, (c) FT 3, and (d) FT 4.*

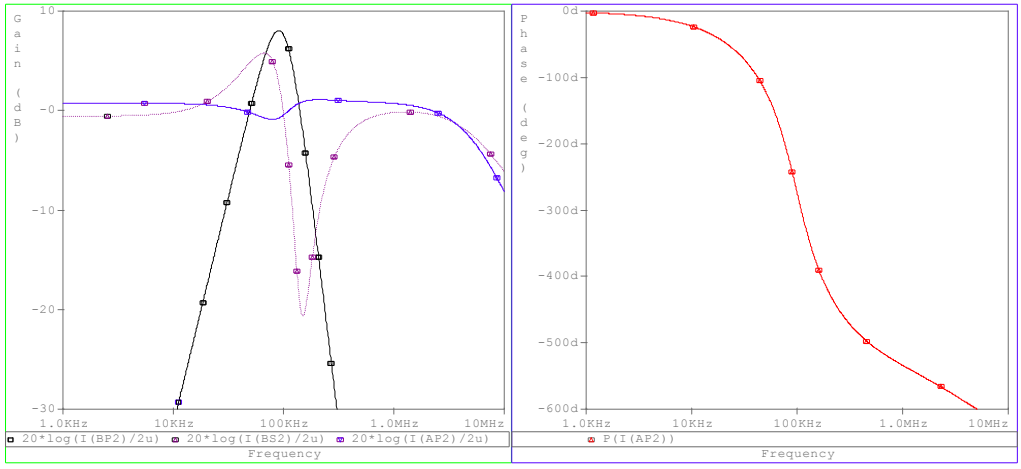


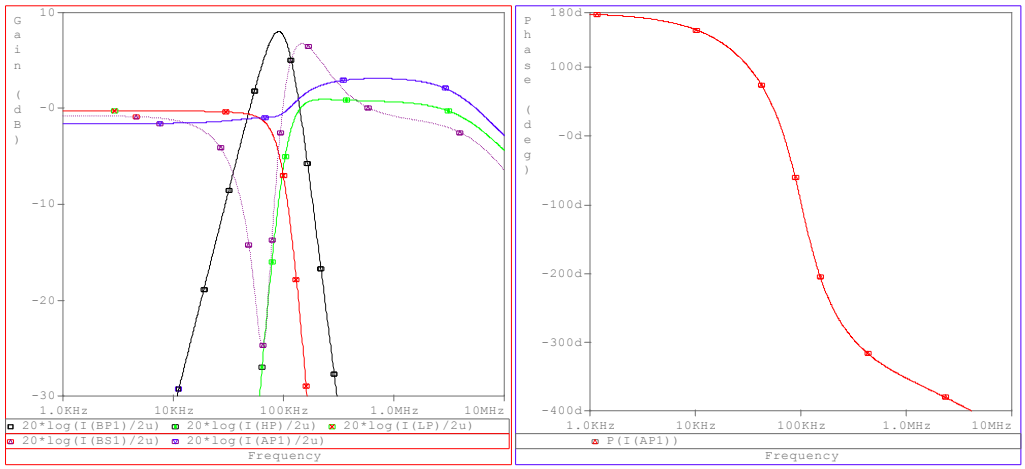
(a)



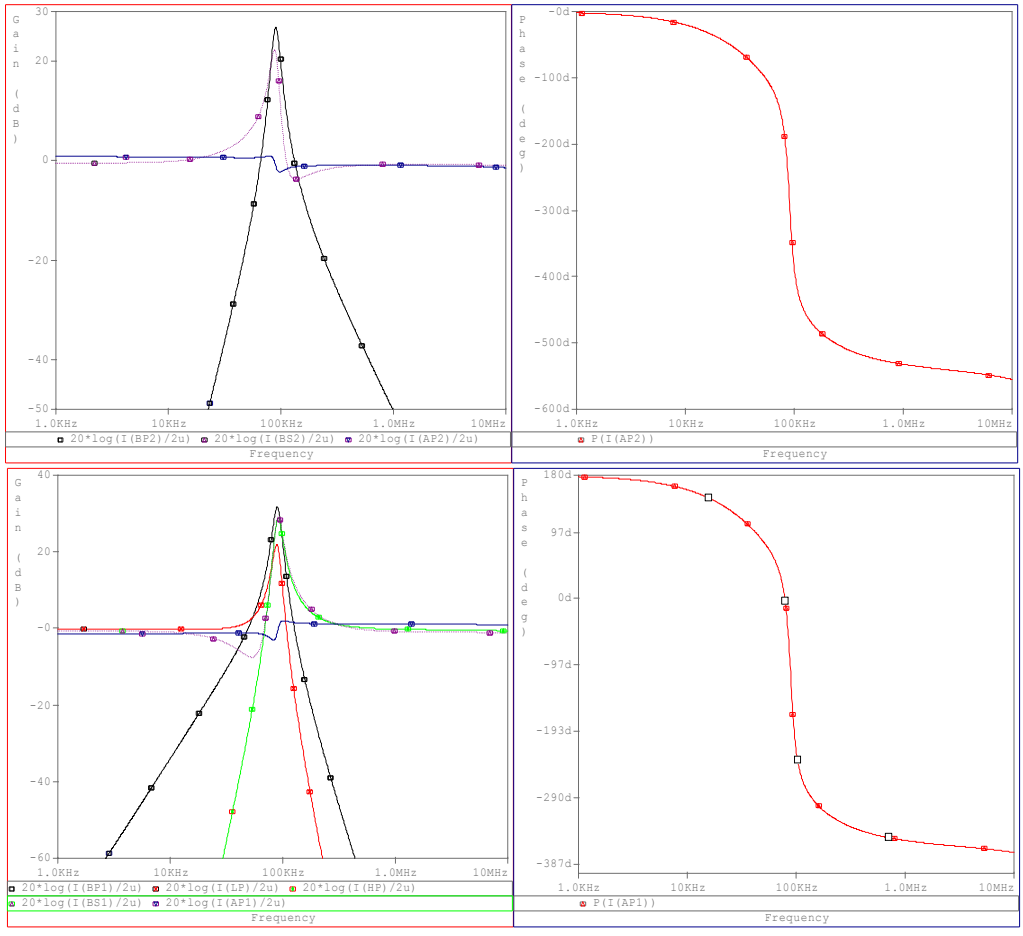
(b)

Fig. 3.29: *3rd and 4th–order SRD MISO universal filter topologies.*

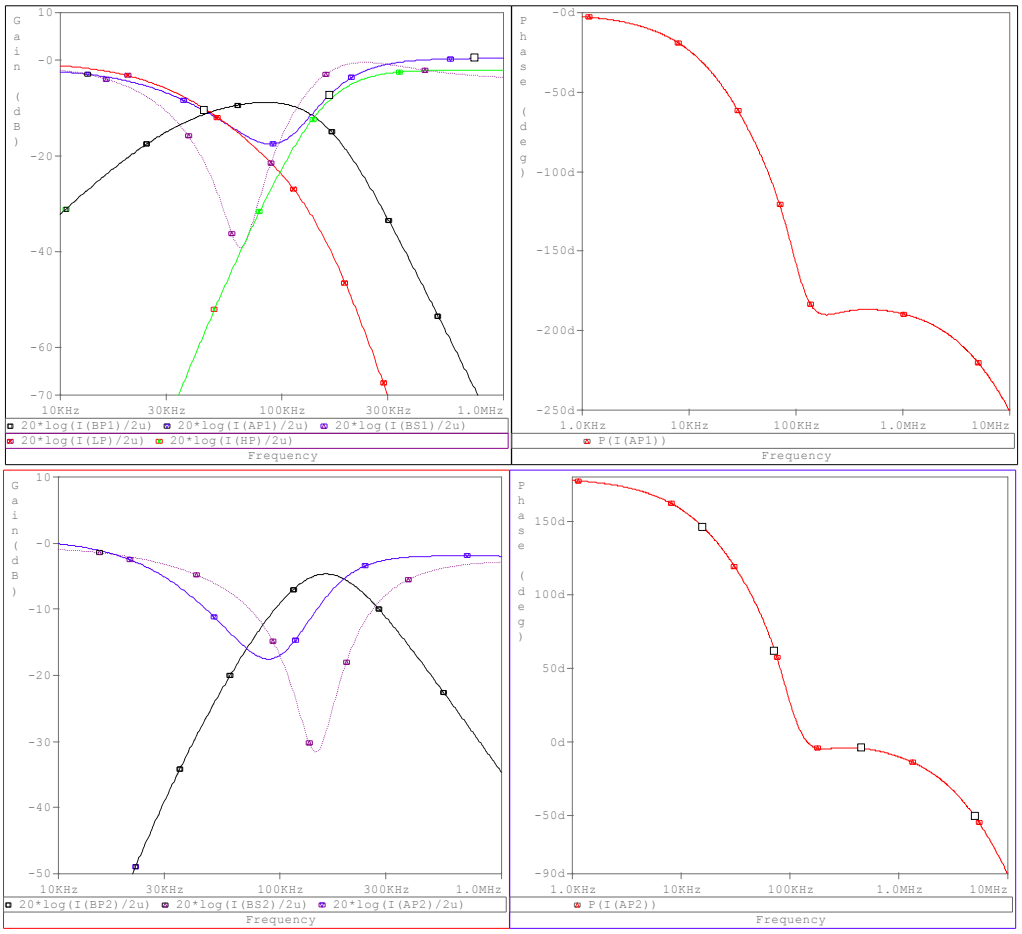



Gain (dB)
10
-0
-10
-20
-30
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
20*log(I(BP1)/2u)
20*log(I(HP)/2u)
20*log(I(LP)/2u)
20*log(I(BS1)/2u)
20*log(I(AP1)/2u)
Frequency
Phase (deg)
180d
100d
-0d
-100d
-200d
-300d
-400d
P(I(AP1))
Frequency

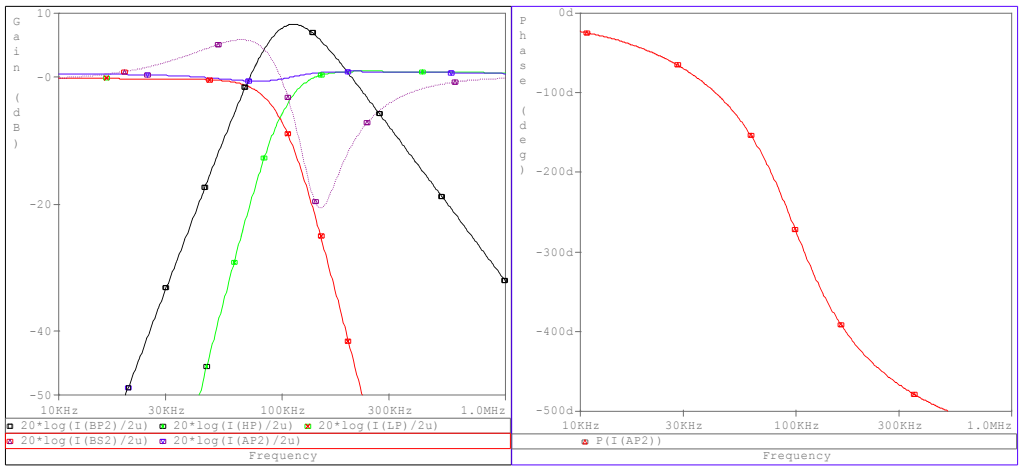
(a)

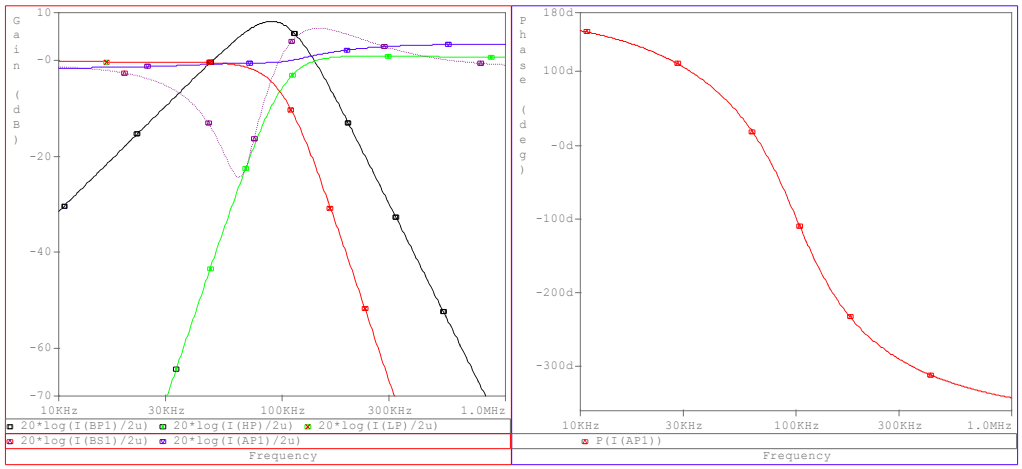

Gain (dB)
30
20
0
-20
-40
-50
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
20*log(I(BP2)/2u)
20*log(I(BS2)/2u)
20*log(I(AP2)/2u)
Frequency
Phase (deg)
-0d
-100d
-200d
-300d
-400d
-500d
-600d
P(I(AP2))
Frequency
Gain (dB)
40
20
-0
-20
-40
-60
20*log(I(BP1)/2u)
20*log(I(LP)/2u)
20*log(I(HP)/2u)
20*log(I(BS1)/2u)
20*log(I(AP1)/2u)
Frequency
Phase (deg)
180d
97d
0d
-97d
-193d
-290d
-387d
P(I(AP1))
Frequency

(b)


Gain (dB)
10
-0
-20
-40
-60
-70
10KHz
30KHz
100KHz
300KHz
1.0MHz
20*log(I(BP1)/2u)
20*log(I(AP1)/2u)
20*log(I(BS1)/2u)
20*log(I(LP)/2u)
20*log(I(HP)/2u)
Frequency
Phase (deg)
-0d
-50d
-100d
-150d
-200d
-250d
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
P(I(AP1))
Frequency
Gain (dB)
10
-0
-10
-20
-30
-40
-50
10KHz
30KHz
100KHz
300KHz
1.0MHz
20*log(I(BP2)/2u)
20*log(I(BS2)/2u)
20*log(I(AP2)/2u)
Frequency
Phase (deg)
150d
100d
50d
0d
-50d
-90d
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
P(I(AP2))
Frequency

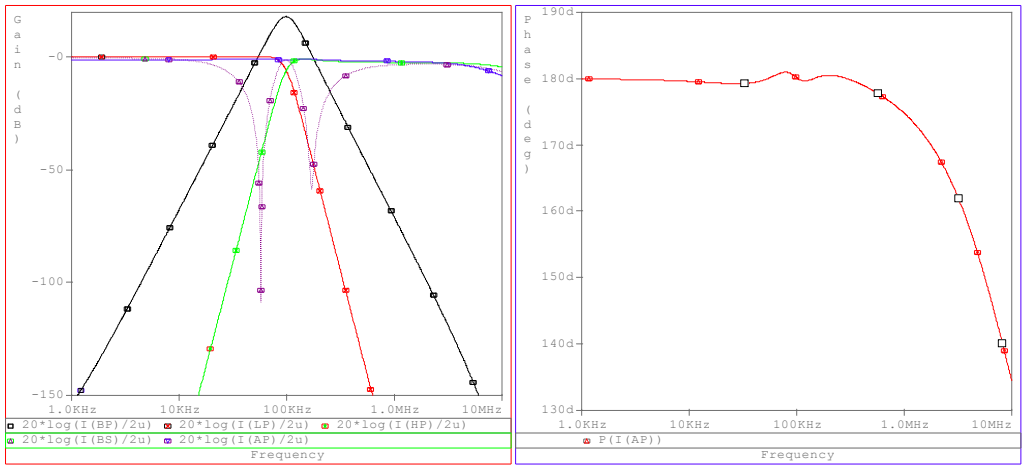
(c)


Gain (dB)
10
-0
-20
-40
-50
10KHz
30KHz
100KHz
300KHz
1.0MHz
20*log(I(BP2)/2u)
20*log(I(HP)/2u)
20*log(I(LP)/2u)
20*log(I(BS2)/2u)
20*log(I(AP2)/2u)
Frequency
Phase (deg)
0d
-100d
-200d
-300d
-400d
-500d
10KHz
30KHz
100KHz
300KHz
1.0MHz
P(I(AP2))
Frequency

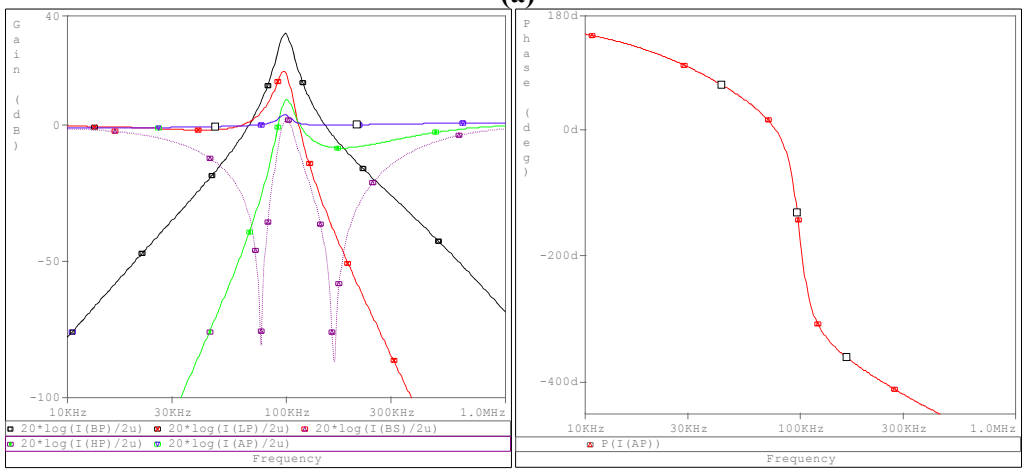


(d)

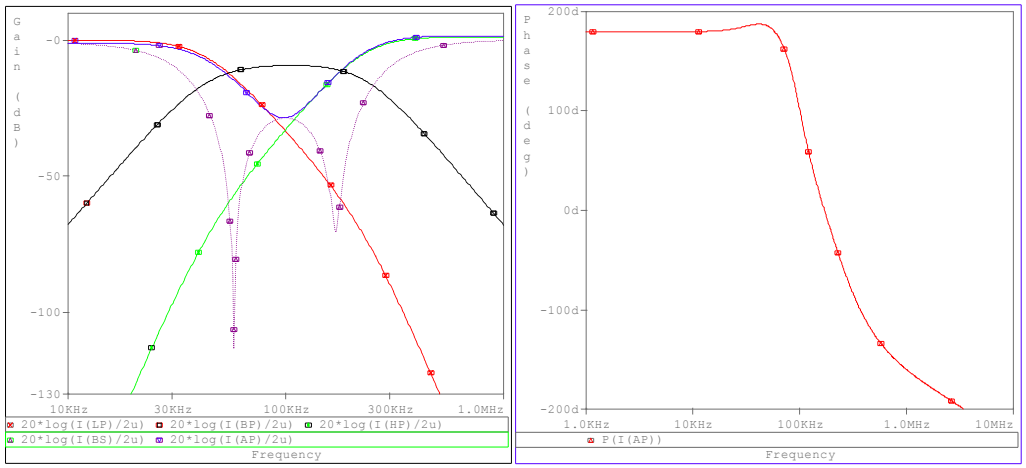
Fig. 3.30: *Simulated magnitude and phase responses of the 3rd–order SIMO universal filter topologies. (a) FT 1, (b) FT 2, (c) FT 3, and (d) FT 4.*



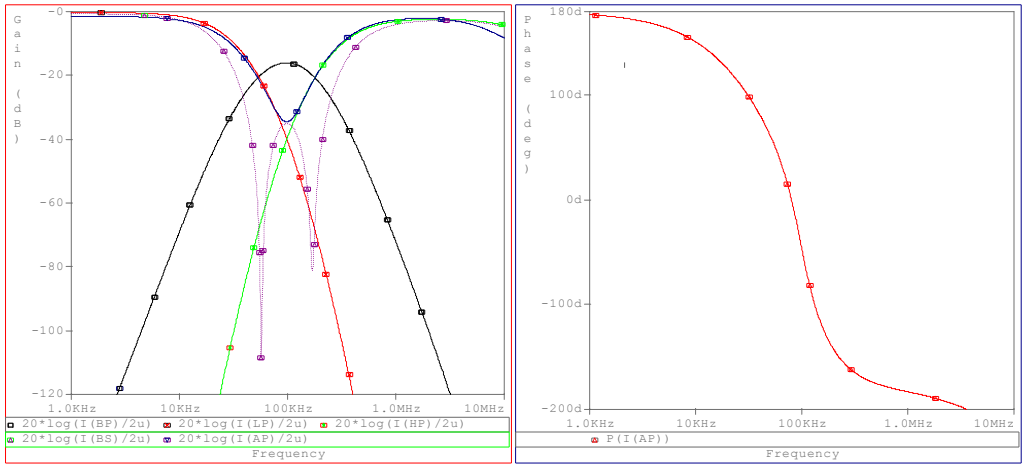
(a)



(b)

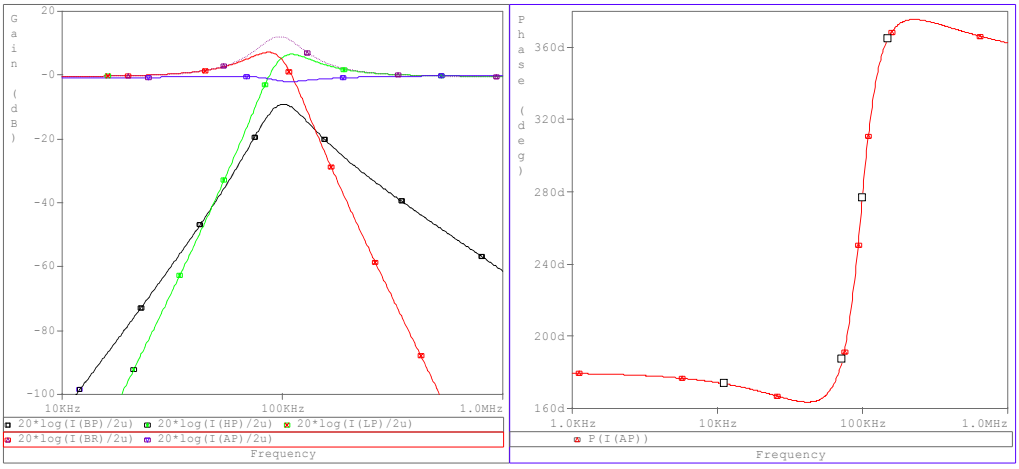


(c)

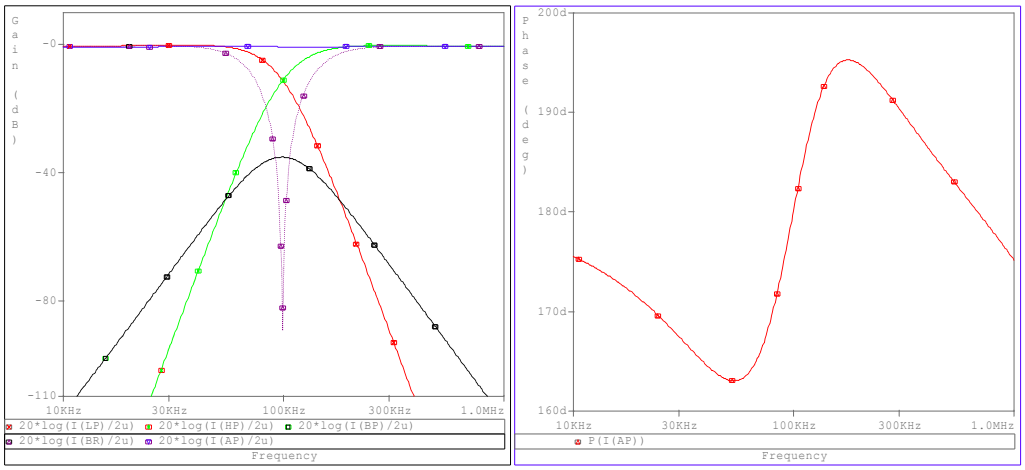


(d)

Fig. 3.31: *Simulated magnitude and phase responses of the 4th–order SIMO universal filter topologies. (a) FT 1, (b) FT 2, (c) FT 3, and (d) FT 4.*

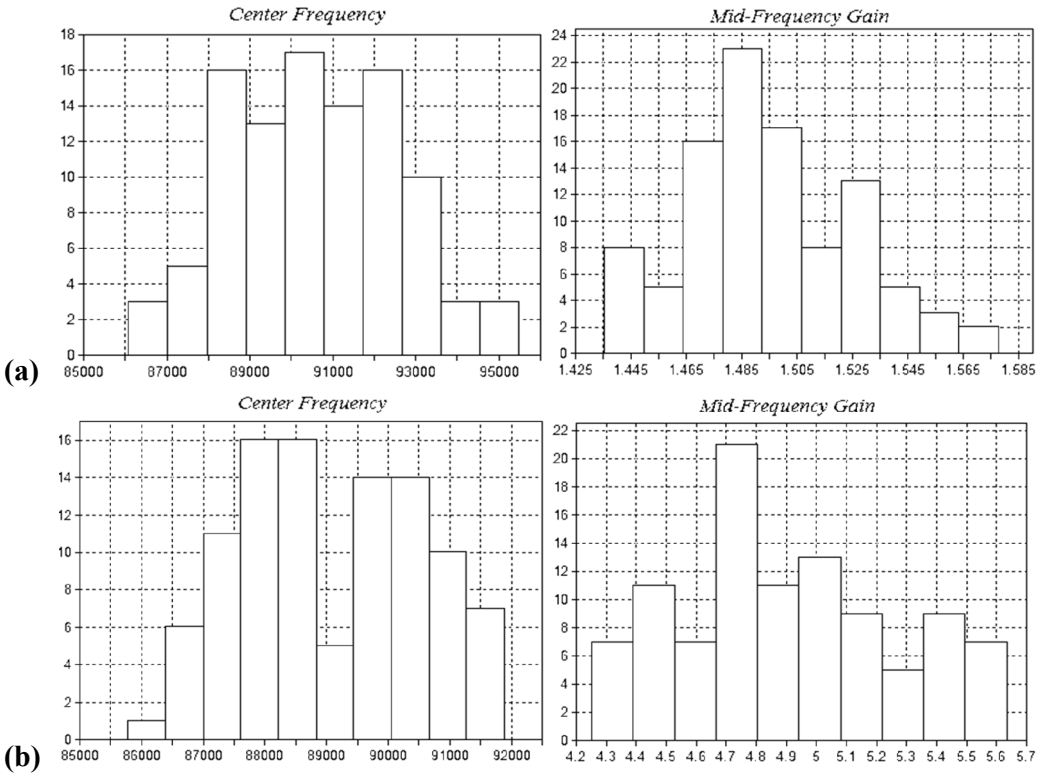


(a)



(b)

Fig. 3.32: *Simulated magnitude and phase responses of the MISO universal filter topologies. (a) 3rd–order; and (b) 4th–order.*



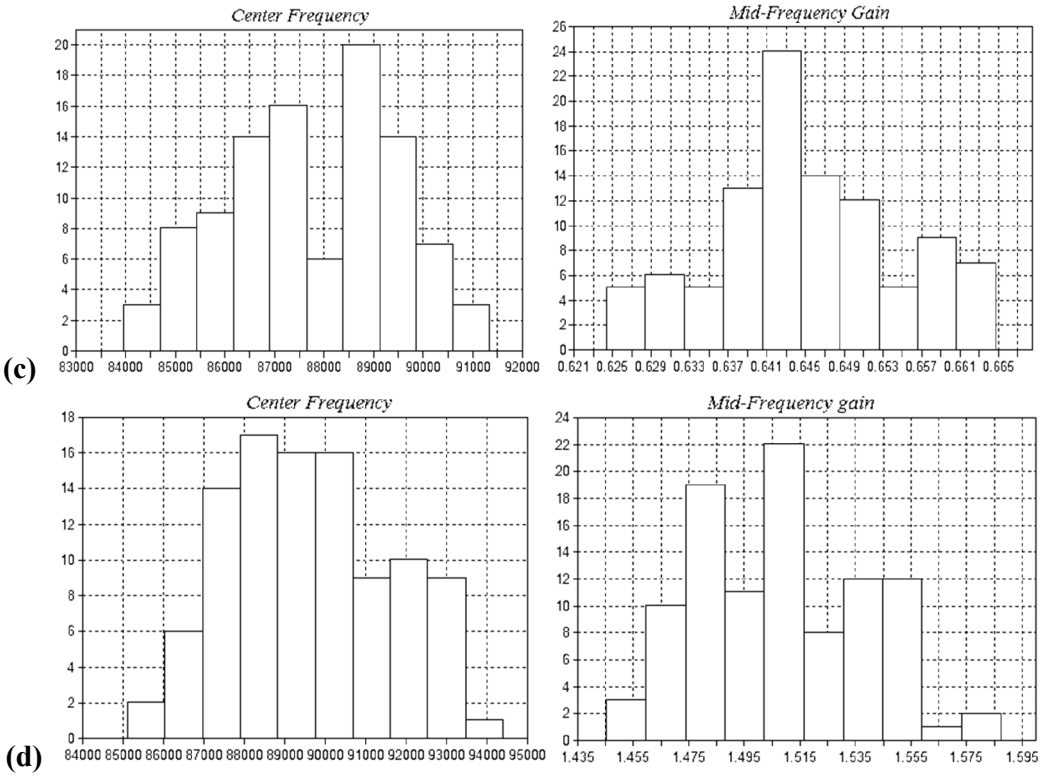
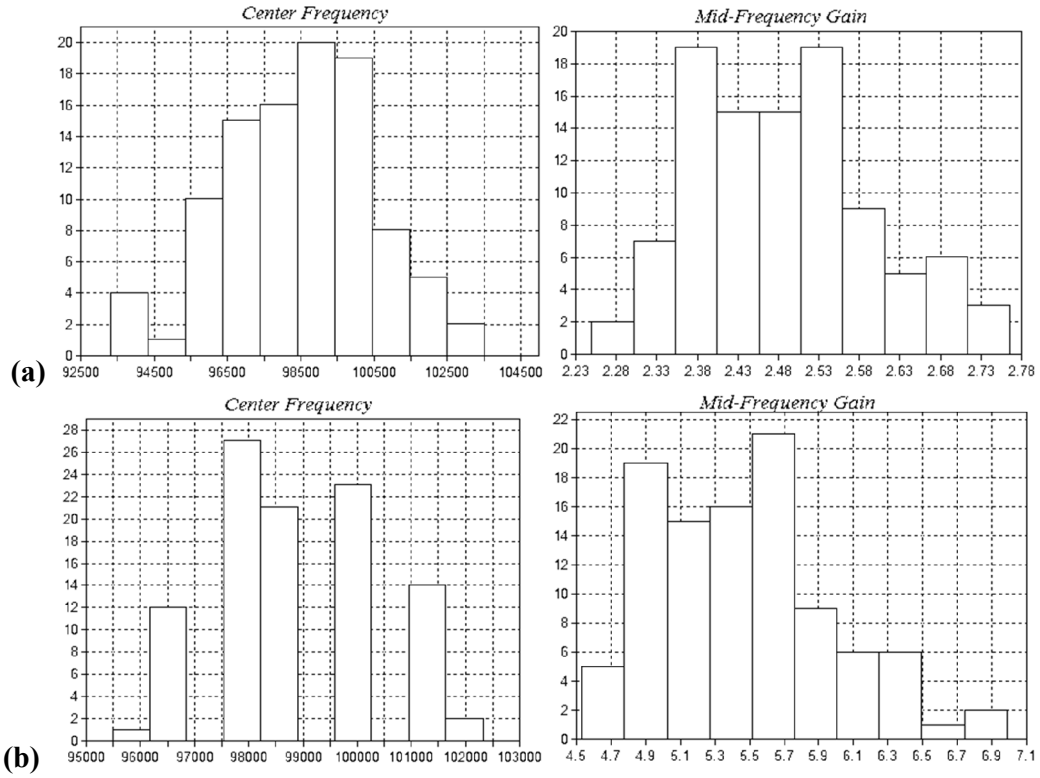


Fig. 3.33: *Sensitivity of the 3rd–order SIMO universal filter topologies with capacitor Transistor and bias current variations. (a) FT 1, (b) FT 2, (c) FT 3, and (d) FT 4.*



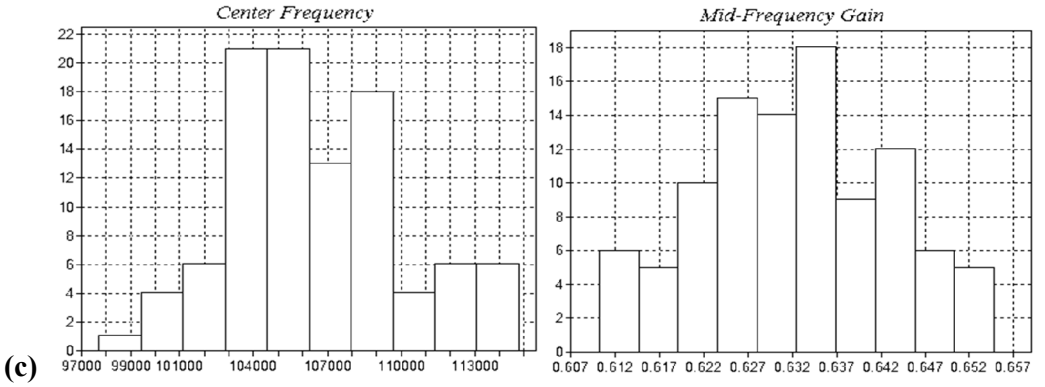
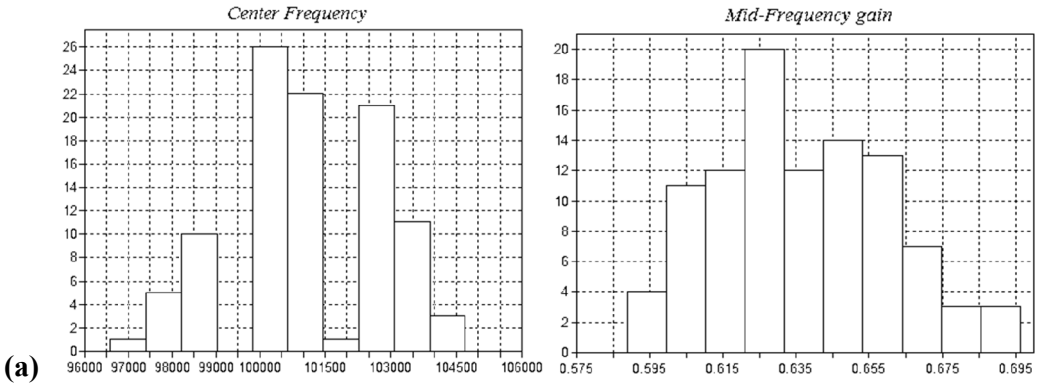
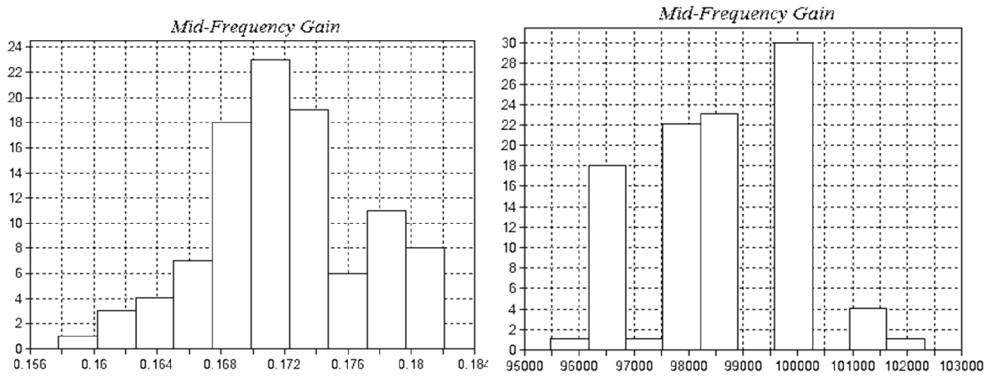


Fig. 3.34: *Sensitivity of the 4th–order SIMO universal filter topologies with capacitor Transistor and bias current variations. (a) FT 1, (b) FT 2, (c) FT 3, and (d) FT 4.*





(b)

Fig. 3.35: *Sensitivity of the MISO universal filter topology with capacitor Transistor and bias current variations. (a) 3rd–order; and (b) 4th–order.*

Control bits ($b_2b_1b_0$)	3rd–order MISO Universal Filter				4th–order MISO Universal Filter					Filter Function
	S(0)	S(1)	S(2)	S(3)	S(0)	S(1)	S(2)	S(3)	S(4)	
000	1	0	0	0	1	0	0	0	0	LP
001	0	0	0	1	0	0	0	0	1	HP
010	0	1/0	0/1	0	0	0	1	0	0	BP
011	1	0	0	1	1	0	0	0	1	BS
100	1	1	1	1	1	1	1	1	1	AP

Table 3.9: *Switch status condition for 3rd and 4th-MISO universal filter topologies.*

Transistor	(W/L)
M_{p1}- M_{p7}	200µm/2µm
M_{p8}- M_{p10}	20µm/2µm
M_{n1}- M_{n4}	24µm/2µm
M_{n5}- M_{n8}	48µm/2µm
M_{n9}- M_{n12}	24µm/2µm

Table 3.10: *Aspect ratio of the MOS transistors of the geometric-mean block in Fig. 2.8.*

Performance factor	SIMO							
	3rd-Order				4th-Order			
	FT1	FT2	FT3	FT4	FT1	FT2	FT3	FT4
Power supply voltage	1.5V	1.5V	1.5V	1.5V	1.5V	1.5V	1.5V	1.5V
Bias current	5µA	5µA	5µA	5µA	5µA	5µA	5µA	5µA
Power dissipation	358µW	355µW	371uW	387µW	439µW	424µW	438uW	456µW
Total capacitance (pF)	145.6	145.6	145.6	145.6	205.22	205.22	205.22	205.22
rms Ampl. @ THD level 1%	2.66µA	2.74µA	2.63µA	2.58µA	2.52µA	2.57µA	2.53µA	2.51µA
rms value of output noise	1.11nA	1.86nA	1.50nA	1.13nA	2.49nA	2.11nA	3.39nA	5.80nA
Dynamic range (dB)	67.6	63.4	64.9	67.2	60.1	61.7	57.5	52.7
Std. dev. Of Mid-Freq. gain	2.21k	1.47k	1.69k	2.19k	2.23k	1.53k	3.58k	1.42k
Std. dev. Of Center Freq. f_o	30.05m	351.9m	9.54m	30.51m	109.2m	516.9m	10.6m	6.37m

(a)

Performance factor	MISO	
	3rd-Order	**4th-Order**
Power supply voltage	1.5V	1.5V
Bias current	5µA	5µA
Power dissipation	258uW	334uW
Total capacitance (pF)	145.6pF	205.22
rms Ampl. @ THD level 1%	2.68uA	2.58uA
rms value of output noise	1.049nA	2.344nA
Dynamic range (dB)	68.2	60.8
Std. dev. of Mid-Freq. gain	1.71k	1.41k
Std. dev. of Center Freq. f_o	24.17m	5.0483m

(b)

Table 3.11: *Performance comparison results for the proposed universal filter topologies (a) SIMO and (b) MISO.*

Filter Topology		Figure of Merit (pJ)
Reference **[139]**	SIMO	1.95
	MISO	0.90
Reference **[147]**	SIMO	3.315
	MISO	9.246
Proposed 3rd-order SIMO Universal filter topologies	FT1	0.552
	FT2	0.898
	FT3	0.801
	FT4	0.627
Proposed 4th-order SIMO Universal filter topologies	FT1	1.1
	FT2	0.88
	FT3	1.38
	FT4	2.70
Proposed MISO Universal filter topologies	3rd-order	0.33
	4th-order	0.77

Table 3.12: *Comparison results with the already published companding topologies.*

- ***It is worth to mention here the SD design of the proposed Generic universal filter topologies of Figs. 3.4 and 3.5 is under process and will be completed in the near future.***

3.1.1.2.3. A low voltage and low power SD universal biquadratic filter for low frequency applications [J4]

3.1.1.2.3.1. Design Procedure of SD Universal Biquadratic Filter

The FBD of the proposed SD universal biquadratic filter is demonstrated in Fig. 3.36, where the realized transfer functions are described by Equations (3.44)–(3.48)

$$H_{HP}(s)=\frac{SINH(\hat{v}_{HP})}{SINH(\hat{v}_{IN})}=\frac{s^2}{s^2+\frac{K}{\hat{\tau}_1}s+\omega_0^2} \tag{3.44}$$

$$H_{LP}(s)=\frac{SINH(\hat{v}_{LP})}{SINH(\hat{v}_{IN})}=\frac{\omega_0^2}{s^2+\frac{K}{\hat{\tau}_1}s+\omega_0^2} \tag{3.45}$$

$$H_{BP}(s)=\frac{SINH(\hat{v}_{BP})}{SINH(\hat{v}_{IN})}=\frac{\frac{K}{\hat{\tau}_1}s}{s^2+\frac{K}{\hat{\tau}_1}s+\omega_0^2} \tag{3.46}$$

$$H_{BR}(s)=\frac{SINH(\hat{v}_{BR})}{SINH(\hat{v}_{IN})}=\frac{s^2+\omega_0^2}{s^2+\frac{K}{\hat{\tau}_1}s+\omega_0^2} \tag{3.47}$$

$$H_{AP}(s)=\frac{SINH(\hat{v}_{AP})}{SINH(\hat{v}_{IN})}=\frac{s^2-\frac{K}{\hat{\tau}_1}s+\omega_0^2}{s^2+\frac{K}{\hat{\tau}_1}s+\omega_0^2} \tag{3.48}$$

where the variable *K* denotes a scaling factor.

The resonant frequency (ω_0) and the Q factor of the filter are given by Equations (3.49) and (3.50) as

$$\omega_0=\frac{1}{\sqrt{\hat{\tau}_1.\hat{\tau}_2}} \tag{3.49}$$

$$Q=\frac{1}{K}.\sqrt{\frac{\hat{\tau}_1}{\hat{\tau}_2}} \tag{3.50}$$

After examining Equations (3.49) and (3.50), it is clear that the resonant frequency (ω_0) and Q factor of the filters could be independently adjusted by the scale factor *K*.

From Fig. 3.36 it is clear that to realize SD FBD of the universal filter, SD lossless integrator and summation/Subtraction blocks are required which have been already presented in section 2.3.3.

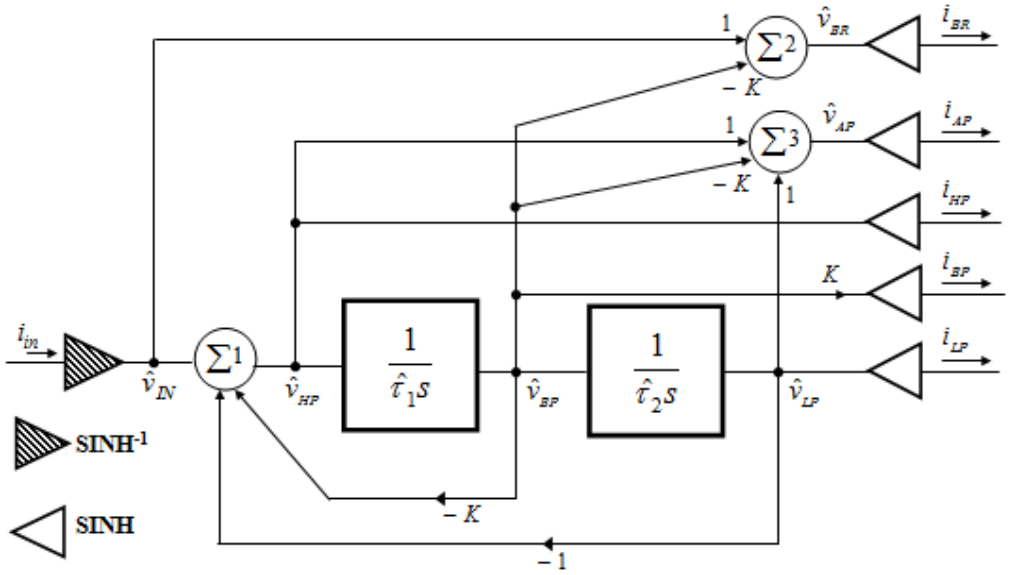


Fig. 3.36: *FBD of the proposed SD Universal biquadratic filter.*

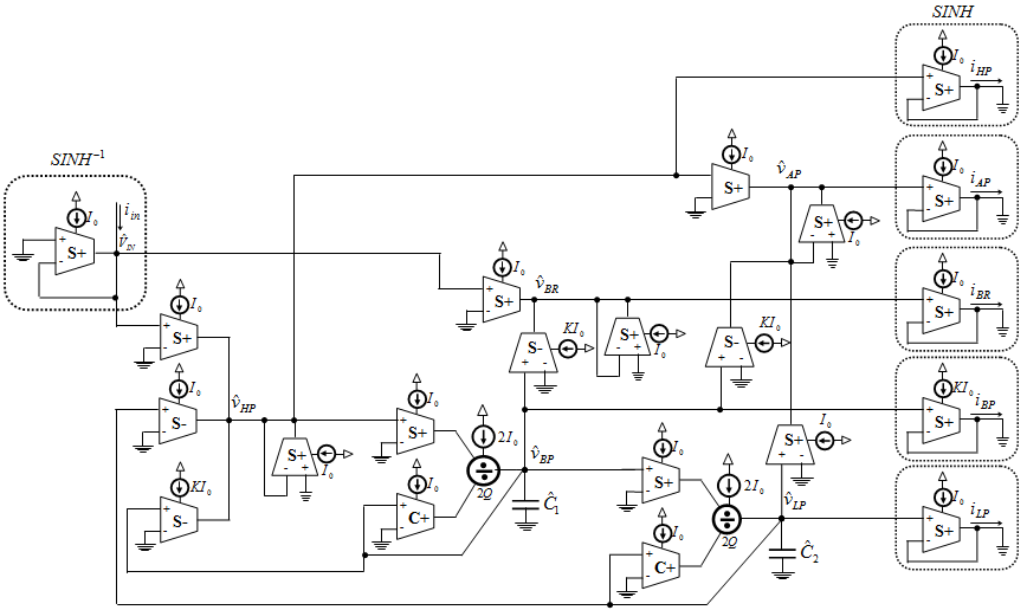


Fig. 3.37: *Topology of the proposed SD Universal Biquadratic filter.*

3.1.1.2.3.2. Simulation Results

In order to confirm the validity of the proposed design, a SD counterpart of universal biquadratic filter in Fig. 3.36, using the building blocks mentioned in section 2.3.3 was designed and the derived SD universal biquadratic filter is depicted in Fig. 3.37.

The evaluation of the performance of the filters has been done using the PSPICE Software. In addition, the transistor models with technology parameters

provided by the TSMC 0.18-µm CMOS process were employed in simulations. The aspect ratio of both NMOS and PMOS transistors that construct the translinear loops in S and C cells was chosen to be 8 µm / 8 µm, whereas the aspect ratios of the other NMOS and PMOS transistors were 8 µm / 8 µm and 80 µm / 8 µm, respectively. A symmetrical supply voltage equal to ± 0.75 V has been chosen, while the dc current I_0 was 100 pA. The dc power dissipation for the filter was 19.2 nW. The frequency response with a cut-off frequency f_0 = 13 Hz, which is typical for EEG application, was realized.

EEG is a method to measure brain waves by recording the electrical movements along the head scalp by the firing of neurons within the brain **[148].** The electrical activity is recorded through highly conductive electrodes attached to the heads surface and sends the signals into EEG machine. The recording can be done in several different conditions depending on the objective. Most of the time, EEG is used in medical practice to diagnose epilepsy, brain death, coma, and some other abnormal activities in brain. In the early stage, EEG was used to detect brain tumors and focal brain disorders **[149].**

Several different rhythmic oscillations can be classified to define brain activities. Five major brain waves (Alpha, Beta, Delta, Gamma, and Theta waves) define most the brain activities with three additional minor bands (Kappa, Lambda, and Mu waves) as the complements **[150].** The classification is based on the operating frequency range of each wave and the state of the sample, in this case, human biological sample. Table 3.13 shows the characteristic of major and minor bands.

Therefore, considering that n = 1.32 and $\hat{\tau} = CU_T / 2I_o$, for the above value of cut-off frequency f_0 = 13 Hz, the values of capacitors were chosen 75.3 pF. The simulated magnitude response of the SD universal biquadratic filter is therefore given in Fig. 3.38. Fig. 3.39 shows the phase response of AP output. Fig. 3.40 shows the time-domain response of the AP output. A sine-wave input at a frequency of 13 Hz with modulation index factor m = 50 % was applied to the filter. This causes a 38.16 ms time delay at the AP output corresponding to 178.60 phase difference which is close to the theoretical value (180^0).

The electronic tunability of the proposed SD universal biquadratic filter topology concerning its frequency characteristics is demonstrated by performing simulations of its frequency response at different levels of current I_0. The derived

responses for f_0 = 5 Hz, 13 Hz, 35 Hz are simultaneously plotted in Fig. 3.41, where it can be verified the capability for electronic tuning of the proposed SD universal biquadratic filter. For above values of frequencies, I_0 was varied from 38.4 pA-269.2 pA. The feature for orthogonal adjustment between the resonant frequency and Q factor offered by the proposed filter has been verified through the plot depicted in Fig. 3.42. In Fig. 3.42, the BP filter responses, obtained for K = 0.33, 0.5 and 1, are demonstrated. According to Equation (3.50), the theoretically predicted values of Q were 3, 2 and 1. The obtained values from the plot in Fig. 3.42 were 2.88, 1.92 and 0.95 respectively. Due to the fact that the center frequency of the BP filters remains unaffected during the tuning of Q, it is obvious that this is an orthogonal procedure with regards to the tuning of ω_0.

Band	Frequency (Hz)	Amplitude (μV)	Individuals State
Alpha	8 – 13	20 - 60	Relaxed, closed eyes
Beta	13 – 40	2 – 20	Excited mental/ physical
Delta	0.5 – 3.5	20 – 200	Deep sleep normal person
Theta	4 – 7	20 - 100	Drowsiness in young adults
Gamma	36 – 44	3 - 5	Sensory stimuli
Kappa	10	N/A	Thinking
Lambda	N/A	20-50	Visual image
Mu	8-13	N/A	Sensori motor cortex

Table 3.13: *Brain waves classification* ***[150].***

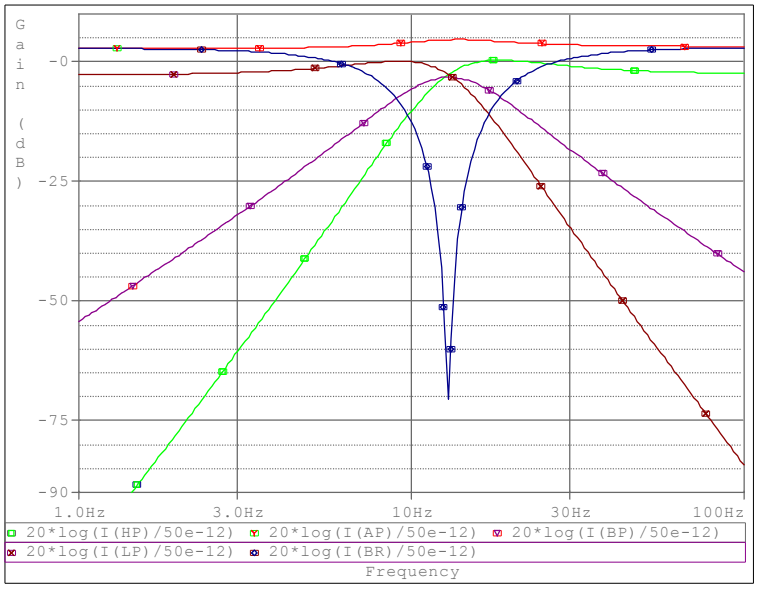


Fig. 3.38: *Simulated frequency responses of the proposed SD Universal biquadratic filter of Fig. 3.37.*

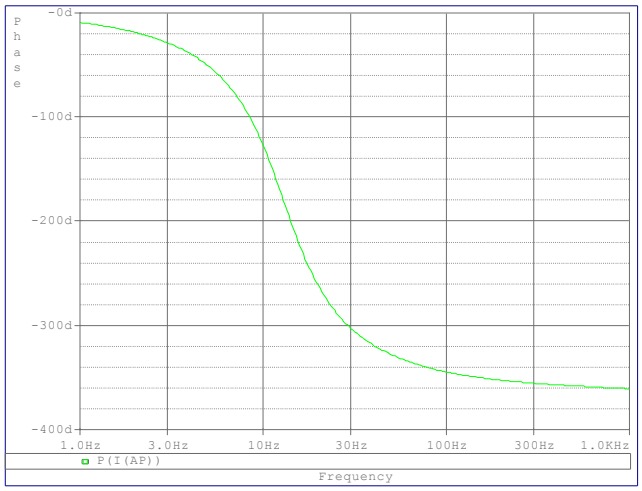


Fig. 3.39: *AP Phase response of the filter of Fig. 3.37.*

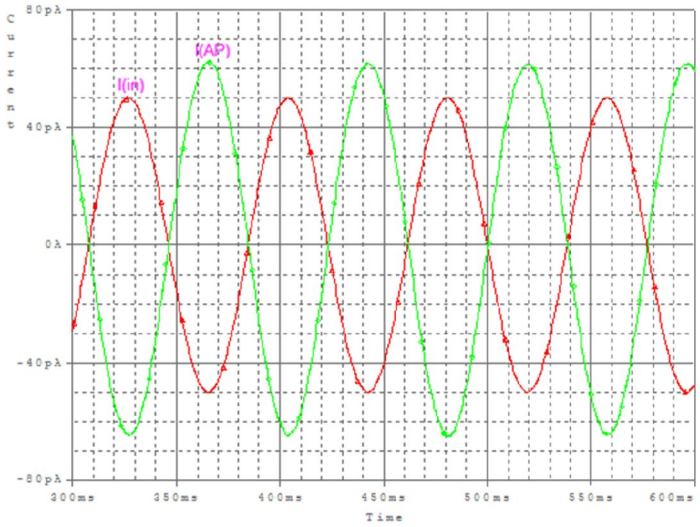


Fig. 3.40: *Time-domain responses of the input and AP output of the filter of Fig. 3.37.*

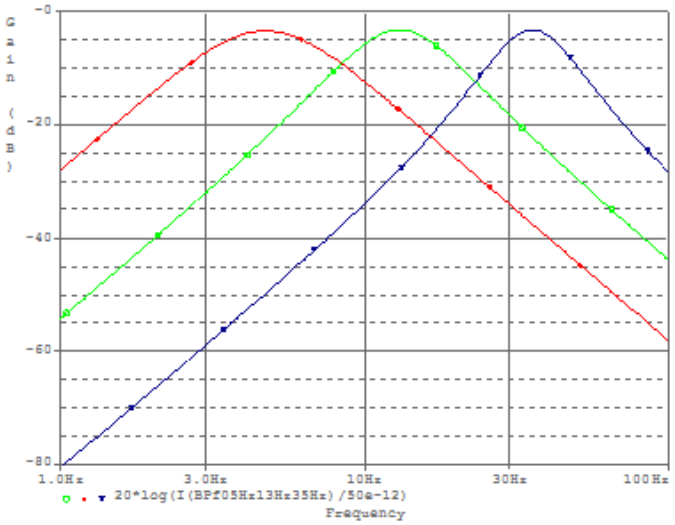


Fig. 3.41: *Demonstration of the electronic tunability of frequency characteristics.*

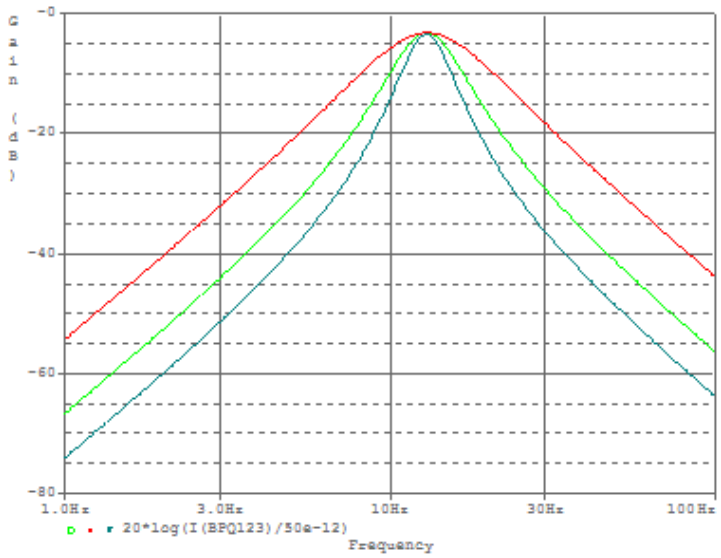


Fig. 3.42: *Demonstration of the independent tunability of ω_0 and Q.*

The nonlinear behaviour of the SD biquad for LP response was carried out employing IMD3 test. For this purpose two closely spaced tones 11 and 12 Hz, which fall in the passband of the BP response, were applied at the input of the filter. The simulated IMD3 versus modulation index factor is plotted in Fig. 3.43. The simulated rms value of input signal amplitude for 1 % distortion level was 60.9 pA.

Integrating the noise over a 50 Hz range, the calculated rms value of the noise was 0.067 pA. The SNR versus modulation index factor is plotted in Fig. 3.44. The predicted dynamic range (DR), at distortion level 1%, would be equal to 59.17 dB.

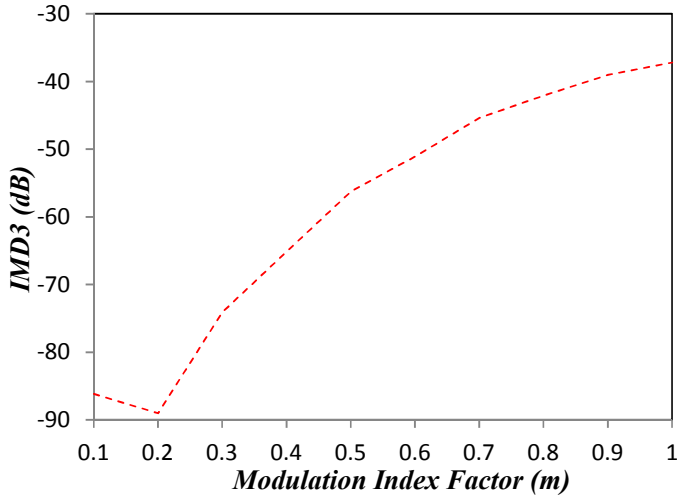


Fig. 3.43: *Nonlinear performance of the proposed SD universal biquadratic filter of Fig. 3.37.*

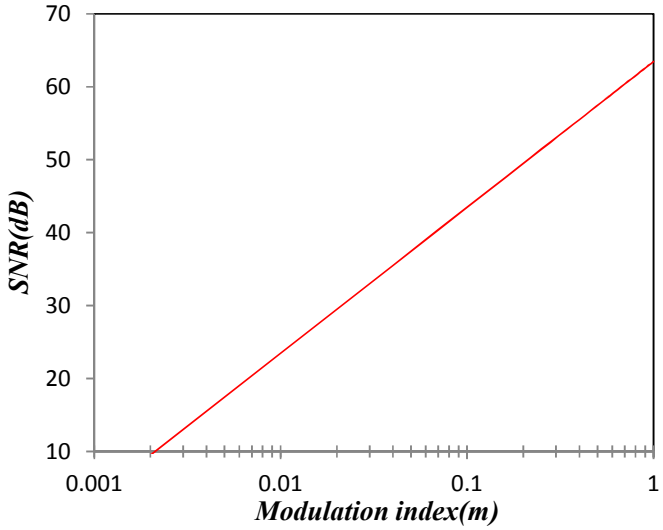


Fig. 3.44: *Simulated SNR versus modulation index factor.*

The proposed biquadratic filter was designed using LD and SRD and Operational Transconductance Amplifier (OTA) derived according to **[151]** as well. The performance of the proposed SD biquadratic filter has been compared with those of the corresponding LD, SRD and OTA-Based designs. An estimation of the power efficiency of the filters is given by utilizing the FOM given by Equation (3.43).The derived results are summarized in Table 3.14 where it could readily be obtained that the proposed SD biquadratic filter offers: more power efficient design, better sensitivity performance and less Capacitance than that of the corresponding LD, SRD and OTA based designs. Besides, more importantly has low bias and power dissipation values.

Performance factor	LD Design	SRD Design	OTA Design [151]	Proposed
Power supply voltage	1.5V	1.5V	±0.75V	±0.75V
Bias current	25µA	5µA	5nA	100pA
Power dissipation	3.46mW	209uW	424nW	19.2nW
Total capacitance (pF)	24.5uF	643nF	1.71nF	150.6pF
rms Ampl. @ THD level 1%	13.6uA	2.62uA	72.1mV	60.9 pA
rms value of output noise	33.6nA	7.13nA	346.9uV	0.067 pA
Dynamic range (dB)	52.14	51.3	46.35	59.17
Std. dev. of Mid-Freq. gain	1.7086m	202.3774u	474.3u	392.7014u
Std. dev. of Center Freq. f_o	269.89m	286.4307m	324.7m	274.69m
FOM	329nJ	21.9nJ	78.5pJ	0.813pJ

Table 3.14: *Performance comparison results for the proposed SD biquadratic filter.*

3.1.2. Linear Gm-C Filter Transposition Synthesis Method of Companding Filters

A method to build companding filters from existing G_m-C filters was given in **[38].** The approach enables the filter designer to simply transform the standard G_m-C filters to Companding Filters. Companding-domain filter can be synthesized using the Gm-C Filter Transposition method by the following procedures:

a) Starting by first choosing the traditional G_m-C filter with the required transfer function as the prototype filter.
b) All the linear transconductance blocks employed in the original filter will be replaced by the non-linear transconductance blocks.
c) To achieve the linear current-mode filter, the appropriate non-linear transconductors must be added to the input and output terminals of the filter obtained at step b.
d) Determine the values of companding-domain parameters corresponding to prototype filter.

Observing the procedure, the obtained filter will be ELIN filter.

Without going into details of Gm-C Filter Transposition method which could be easily found from the open literature, the following example, demonstrating the proposed synthesis approach for single-input-four-output (SIFO) multi-function LD biquad, explains the Gm-C Filter Transposition method comprehensively.

3.1.2.1.Synthesis of SIFO Electronically Tunable LD multi-function Biquad [J10]

3.1.2.1.1. Design of LD multi-function Biquad

3.1.2.1.1.1. Method

To begin with let us consider the transfer function of 2nd-order HP filter as given hereunder:

$$T_{HP}(s) = \frac{Ks^2}{b_2 s^2 + b_1 s + b_0} \tag{3.51}$$

Where K is a gain determining constant and coefficients b_0–b_2 determine the type of filter (Butterworth, Chebyshev).

$$T_{HP}(s) = \frac{(K/b_2)}{1 + (b_1/b_2)(1/s) + (b_0/b_2)(1/s^2)} \tag{3.52}$$

Equation (3.52) can be rearranged as:

$$T_{HP}(s)=\frac{G}{1+c_1(1/s)+c_2(1/s^2)} \tag{3.53}$$

Where G = gain at infinity and $c_1=(b_1/b_2)$ and $c_2=(b_0/b_2)$

$$T_{HP}(s)=\frac{G}{1+H(s)} \tag{3.54}$$

Where

$$H(s)=c_1(1/s)+c_2(1/s^2) \tag{3.55}$$

Equation (3.55) can be rearranged as:

$$H(s)=\left\{\left(1+\frac{1}{a_2 s}\right).\frac{1}{a_1 s}\right\} \tag{3.56}$$

Where

$$a_1=\frac{1}{c_1}, \qquad a_1.a_2=\frac{1}{c_2} \tag{3.57}$$

The complete FBD of 2nd -order HP Filter is then as shown in Fig. 3.45, where the dash line enclosed block represents the feedback transfer function H(s) with two summers combined into one.

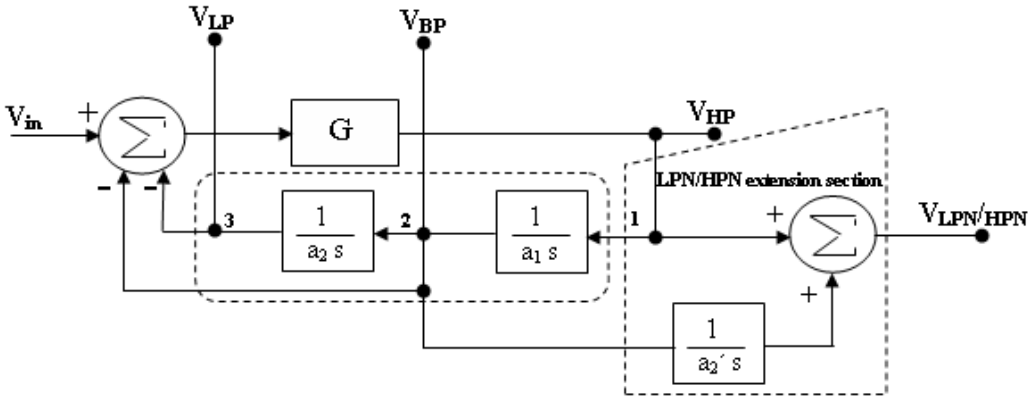


Fig. 3.45: *FBD representation of proposed multi-function biquadratic filter.*

3.1.2.1.1.1.1. LP filtering function

The general transfer function of LP filter is

$$T_{HP}(s)=\frac{K_1}{b_2 s^2+b_1 s+b_0} \tag{3.58}$$

Equation (3.58) can be rearranged as:

$$T_{HP}(s)=\frac{1}{K_2 s^2}.\frac{Ks^2}{b_2 s^2+b_1 s+b_0} \tag{3.59}$$

Where $(K/K_2) = K_1$.

Thus, LP filtering function can be obtained by dividing the transfer function of HP filtering function by s^2 or by integrating the HP filtering function 2-times. From Fig. 3.45, it is then clear that LP filtering function will be available at node 3.

3.1.2.1.1.1.2. BP filtering function

The general transfer function of 2nd – order BP filter is

$$T_{HP}(s) = \frac{K_3 s}{b_2 s^2 + b_1 s + b_0} \tag{3.60}$$

(3.60) can be rearranged as:

$$T_{HP}(s) = \frac{1}{K_4 s} \cdot \frac{K s^2}{b_2 s^2 + b_1 s + b_0} \tag{3.61}$$

Where $(K/K_4) = K_3$.

Thus, BP filtering function can be obtained by dividing the transfer function of HP filter function by s or by integrating the HP filter transfer function. From Fig. 3.45, it is clear that BP filtering function will be available at node 2.

3.1.2.1.1.1.3. LPN/HPN filtering function

The two uncommon filtering functions, LPN and HPN, are revisited in this work **[144, 152-154]**. To calculate the transfer functions of these filtering functions, let us consider the transfer functions of 2nd-order HP and LP filters based on the design discussed above, as given below

$$T_{HP}(s) = \frac{G s^2}{s^2 + \frac{s}{a_1} + \frac{1}{a_1 a_2}} \tag{3.62}$$

$$T_{HP}(s) = \frac{G/a_1 a_2}{s^2 + \frac{s}{a_1} + \frac{1}{a_1 a_2}} \tag{3.63}$$

If we integrate the output at node 2 by a separate integrator $\left(1/a_2' s\right)$, then the output of this integrator will be a LP filtering function given by

$$T_{HP}(s) = \frac{G/a_1 a_2'}{s^2 + \frac{s}{a_1} + \frac{1}{a_1 a_2}} \tag{3.64}$$

$$T_N(s) = T_{HP}(s) + T_{LP}'(s) = \frac{G\left(s^2 + 1/a_1 a_2'\right)}{s^2 + \frac{s}{a_1} + \frac{1}{a_1 a_2}} \tag{3.65}$$

In our case of LD filters $a_n = (C_n V_T)/I_o$, so

(i). If $\left(1/a_1 a_2'\right) > \left(1/a_1 a_2\right)$ or $a_2' < a_2$, then $T_N(s)$ will be the transfer function of LPN filter as discussed in **[144, 152-154].**

(ii).If $\left(1/a_1 a_2'\right) < \left(1/a_1 a_2\right)$ or $a_2' > a_2$, then $T_N(s)$ will be the transfer function of HPN filter as discussed in reference **[144, 152-154].**

Thus Equation (3.65) represents the combined transfer function of LPN and HPN filtering functions. The LPN/HPN extension is then as shown in Fig. 3.45.

Equation (3.65) can be expressed as:

$$T_N(s) = \frac{G\left(s^2 + \omega_n^2\right)}{s^2 + \frac{\omega_o}{Q} s + \omega^2} \tag{3.66}$$

As discussed above then $\omega_n > \omega_o$ for LPN and vice-versa for HPN, where ω_n is the notch frequency of LPN/HPN filtering function and ω_o is the cut-off/centre frequency of LP/HP/BP filtering function. ω_n and ω_o have a_1 as a common term and two independent terms a_2' and a_2 respectively. Thus, the cut-off frequency of LP/HP/BP can be varied independent of notch frequency of LPN/HPN and vice-versa

The G_m-C representation of the proposed multifunction filter is shown in Fig. 3.46. The actual G_m-C representation will be without current–voltage converter (I/V) and voltage–current (I/V) converters shown in Fig. 3.46. The I/V and V/I converters are required to extract the resultant of input and feedbacks currents representing HP filtering function, without disturbing the operation of the entire circuit. The intermediate voltage is then the voltage representation of HP filtering function as shown in Fig. 3.46. The I/V and V/I converters should have unit transfer ratios (impedance and admittance or resistance or conductance) but if they have non-unity transfer ratios, the overall transfer function will be same, only there will be change in the gain G. The above discussed G_m-C representation of the design can be transposed into LD filter representation as discussed in **[38]**. In order to make the design DC

stabilized, the rules discussed in **[50]** were followed. The LD representation of the proposed LD multi-function biquad is shown in Fig. 3.47. In this representation, the HP filtering function is extracted by separating 1st capacitor by a transconductance cell **[54].**

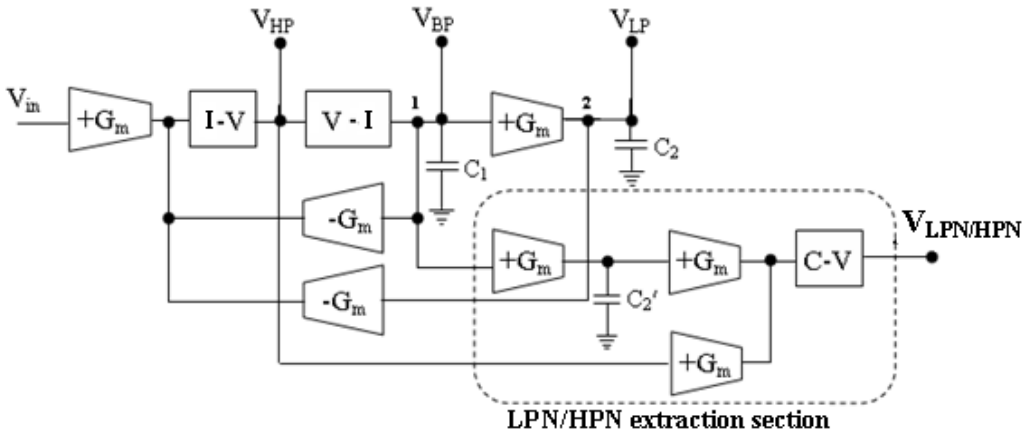


Fig. 3.46: *Gm-C representation of proposed multi-function biquad.*

3.1.2.1.1.3. Simulation Results

The performance of the proposed LD multi-function biquad, shown in Fig. 3.47 was evaluated through simulation results using PSPICE. For this purpose, the magnitude responses of multi-function filter with cut-off frequency as f_C =50 KHz were simulated. The power supply voltages were chosen to be $V_{CC} = -V_{EE}$ = 1.5V, and the bias currents were I_O=25uA. The capacitor values for C_1 and C_2 were taken as 3.18 nF. The value of C_2' used in the LPN/HPN notch extension section was chosen as 35 nF for HPN and 2 nF for LPN leading to the respective notch frequencies of 15 KHz and 63.3 KHz. The simulated magnitude responses using ideal and practical transistors are respectively plotted in Figs. 3.48(a) and 3.48(b). All the NPN transistors in cell implementations are simulated using the parameters of the AT& T CBIC-R NR100N NPN transistor.

In order to verify the DC stability of the proposed approach, transient analysis was done. For this purpose, a sinusoidal input current with modulation index factor (i.e. the ratio of the signal's amplitude to the bias current: $m=i_{peak}/Io$) equal to 60% and a frequency equal to 20 KHz was applied to multi-function filter , the simulated input-output current waveforms are plotted in Fig. 3.49. The non-linear behaviour of the multi-function biquad was also studied. For this purpose, the THD of the multi-function filter having cutoff frequency set to 50 kHz has been measured for each of

the outputs. For HP and HPN, the negligible difference was found between their distortion characteristics and was thus represented by only one characteristic. Similarly, the distortion characteristics of LP and LPN filtering functions were represented by only one characteristic. For LP filtering function, THD was measured at 30 KHz, for BP filtering function, THD was measured at 50 kHz and for HP filtering function THD was measured at 100 KHz. The simulated plots of THD versus modulation index factor are shown in Fig. 3.50 and the values of input current at 1% THD value and the values of THD at m = 1 for each of the outputs are summarized in Table 3.15. The noise performance of the multi-function LD filter was also studied. For this purpose, the noise of the filter was integrated over a 3 MHz range and the signal-to-noise ratio (SNR) versus the modulation index factor is plotted in Fig. 3.51. The negligible differences were found between the noise performances of various outputs. The achieved dynamic range (DR), at 1% distortion level, was calculated for each of the outputs and is summarized in Table 3.15. The overall dynamic range was taken as the worst case of HP/HPN filtering function being operating at high frequencies and is given as 38.3 dB.

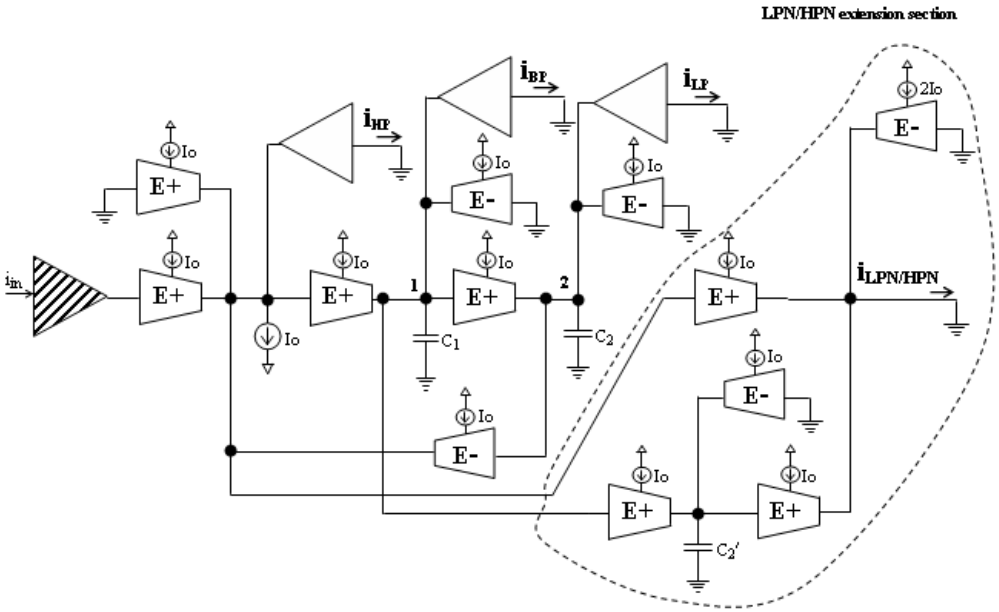
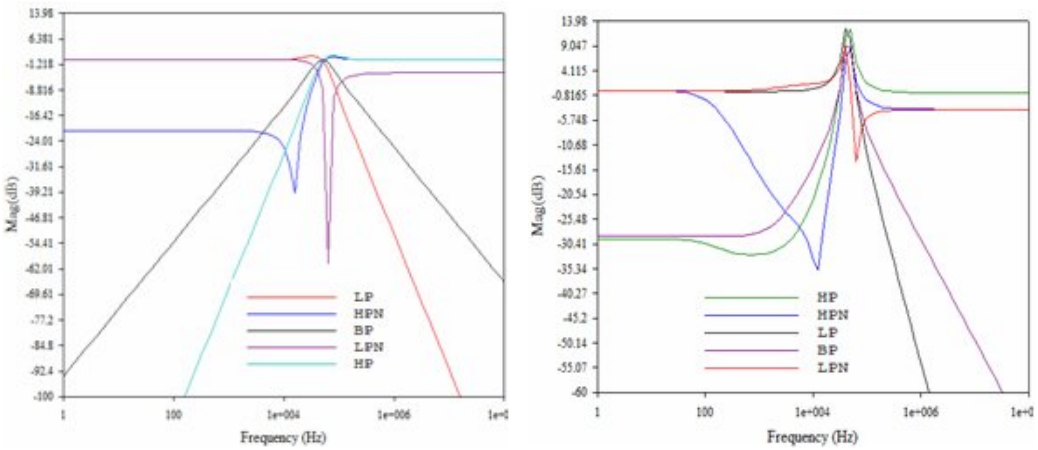


Fig. 3.47: *LD representation of proposed multi-function biquad.*



(a) **(b)**

Fig. 3.48: *Magnitude response of proposed LD multi-function biquad (a) Using ideal transistors (b) Using practical transistors.*

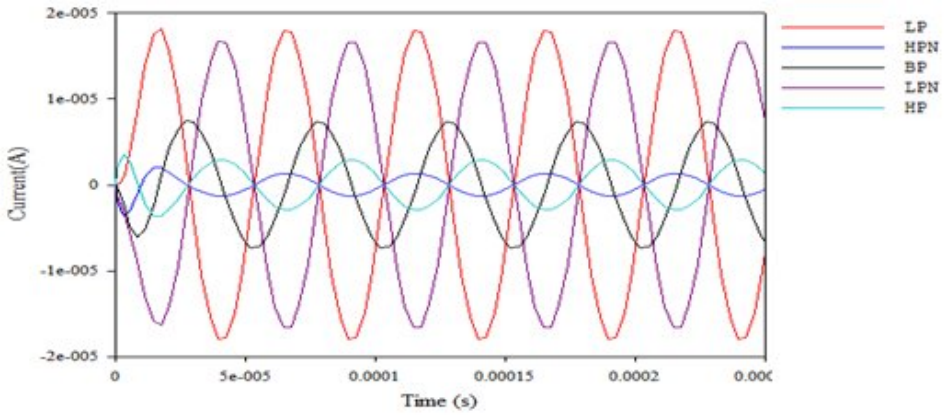


Fig. 3.49: *Simulated input-output current waveforms of proposed LD multi-function biquad.*

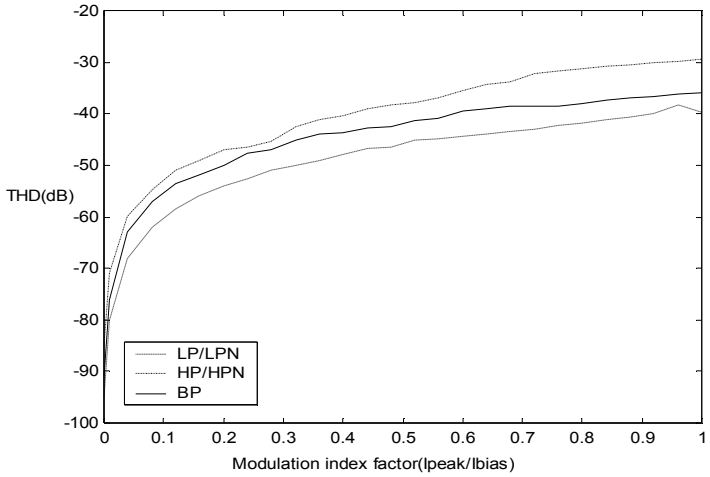


Fig. 3.50: *Total harmonic distortion (THD) versus modulation index factor (Ipeak/Ibias).*

In order to verify the electronic tunability, the bias currents were given three values as 25 μA, 50 μA and 75 μA and the frequency responses for each of the outputs are shown in Fig. 3.52(a)-3.52(e). From the responses, it was observed that for the above three values of bias current, the cut-off/centre frequencies comes out approximately 50 KHz, 100 KHz and 150 KHz respectively. Thus, the approach has linear dependence of cut-off/centre frequencies over the bias current. To verify the independent tuning of notch frequency of LPN/HPN, the components constituting a_2 and $a_2^{'}$ were varied independently. For this purpose, first the $C_2^{'}$ was varied by giving it three values as 35 nF, 55 nF and 75 nF and C_2 was kept fixed at 3.18 nF and the resultant frequency responses are shown in Fig. 3.53(a). Secondly, the C_2 was varied by giving it three values as 3 nF, 9 nF and 15 nF and $C_2^{'}$ was kept fixed at 35 nF and the resultant frequency responses are shown in Fig. 3.53(b). It is worth to mention that as the information regarding the cut-off/centre frequency of LP/HP/BP is also contained in the LPN/HPN responses, it is sufficient to observe the LPN/HPN response. That is why only the HPN responses are shown in figures. From the responses, it is clear that the notch frequency of LPN/HPN and the cut-off/centre frequency of LP/HP/BP can be varied independent of each other.

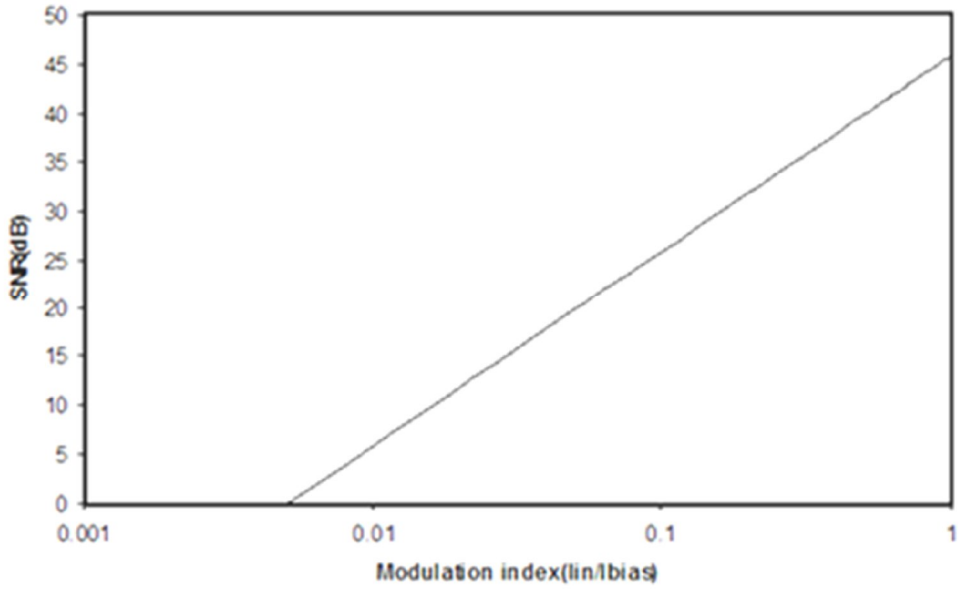
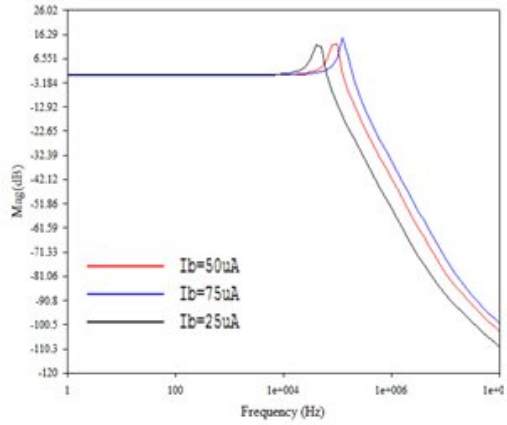


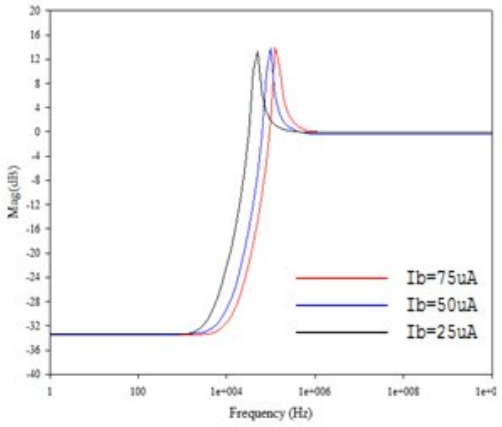
Fig. 3.51: *Signal to noise ratio (SNR) versus modulation index factor (m).*

Calculations	LP/LPN Output	BP Output	HP/HPN Output
Value of input current for 1% THD	23uA	14.4uA	10.5uA
Value of THD at m=1	36dB	-34.6dB	-29.4dB
Dynamic range	45dB	41.6dB	38.3dB

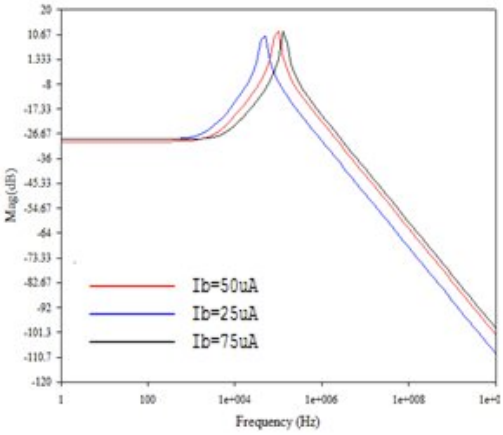
Table 3.15: *Simulated values of input current at 1% THD, THD at m=1 and dynamic range for each of the three outputs.*



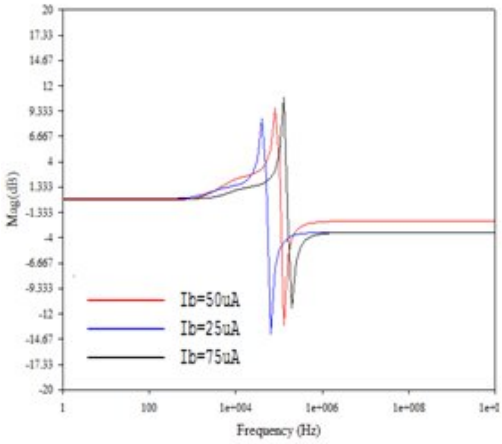
(a)



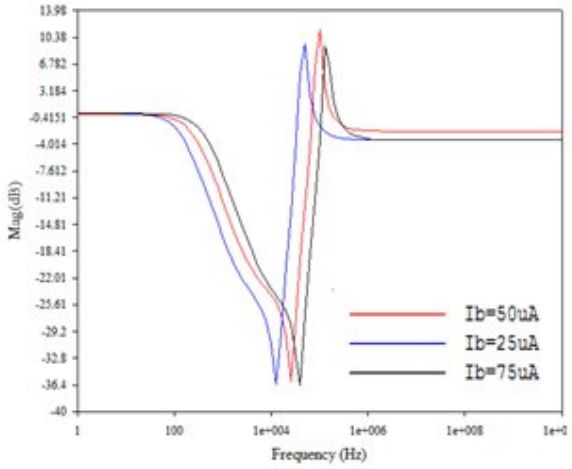
(b)



(c)

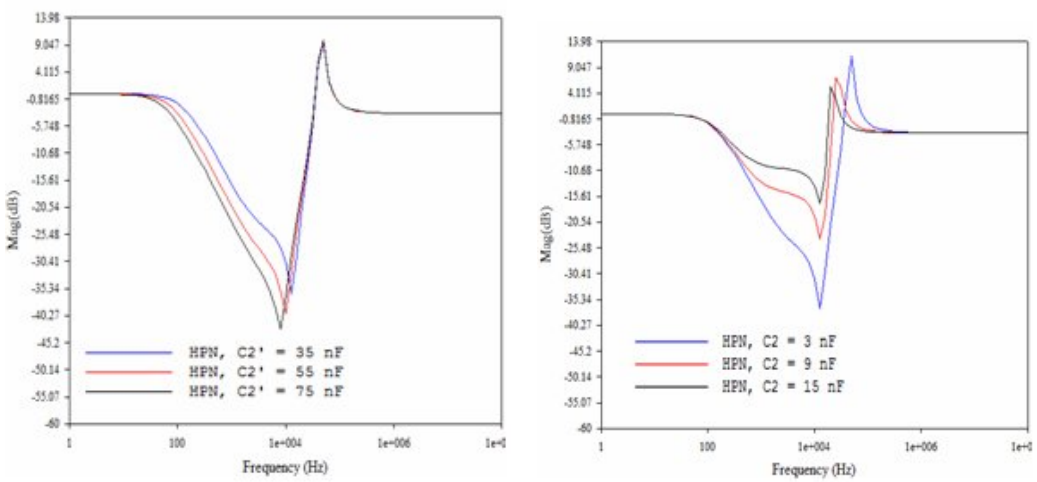


(d)



(e)

Fig. 3.52: *Magnitude responses showing the electronic tunability of the proposed LD multi-function biquad. (a) LP (b) HP (c) BP (d) LPN (e) HPN.*



(a) ***(b)***

Fig. 3.53 *Magnitude responses showing the independent tuning of notch and cut-off/centre frequency (a) Fixed cut-off/centre frequency and varying notch frequency. (b) Fixed notch frequency and varying cut-off/centre frequency.*

3.1.3. Exponential State-Space Synthesis Method of Companding Filters

All known analog filter types may be derived and synthesized starting from linear state space models. By applying linear or nonlinear mappings to the variables, one may derive circuit realizations. Of course, such derivations may require considerable creativity, as evidenced by the many techniques developed by those who have been responsible for the evolution of filter synthesis as we now know it. The universal applicability of state space methods to filter synthesis provides an invaluable tool for the unification of the many approaches introduced over the years. This unification provides not only elegance, but also a means for comparison amongst the many realizations.

Companding filter can be synthesized using the state-space method by the following procedures:

a) Starting with the transfer function of the prototype filter, State-space equations satisfying the transfer function are found (as mentioned above, considerable creativity may be required to find the State-space equations).
b) State-space equations are appropriately transformed into companding-domain.
c) The companding-domain State-space equations are synthesized using appropriate companding-domain blocks.
d) Determine the values of companding-domain parameters corresponding to prototype filter.

Without going into details of state-space synthesis method, the following example, demonstrating the proposed synthesis method for the design High-order Allpass filters using Novel Low-Voltage Current-Mode SRD low-order Allpass Filters, explains the state space method comprehensively.

3.1.3.1. Synthesis of High-order Allpass filters using Novel Low-Voltage Current-Mode SRD low-order Allpass Filters [J15]

3.1.3.1.1. Proposed Low-Voltage Current-Mode SRD AP filter Design

3.1.3.1.1.1. First-Order AP Filter

A first-order AP filter transfer function can be written as follows:

$$H(s) = k\frac{s\tau - 1}{s\tau + 1} \tag{3.67}$$

Where τ is the time constant of the filter and k is the gain or loss throughout the frequency response. Equation (3.67) can be decomposed to the following:

$$H(s) = k - \frac{2k}{s\tau + 1} \tag{3.68}$$

The second term in the right hand side of Equation (3.68) is the transfer function of first-order low-pass (LP) filter and can be represented by state space equations as shown below:

$$\begin{aligned} \dot{x} &= -\frac{x}{\tau} + 2k\frac{u}{\tau} \\ y &= x \end{aligned} \tag{3.69}$$

As the state variables are node voltages, then substitute x = V_1 and u = U in Equation (3.69) leads to Equation (3.70)

$$\begin{aligned} \dot{V}_1 &= -\frac{V_1}{\tau} + 2k\frac{U}{\tau} \\ y &= V_1 \end{aligned} \tag{3.70}$$

Multiplying by a constant C on both sides of Equation (3.70), we have

$$\begin{aligned} C\dot{V}_1 &= -C\frac{V_1}{\tau} + 2kC\frac{U}{\tau} \\ y &= V_1 \end{aligned} \tag{3.71}$$

For a MOSFET in saturated region, the drain current is given by

$$I_{DS} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)\left(V_{GS} - V_{TH}\right)^2 = \beta\left(V_{GS} - V_{TH}\right)^2 \tag{3.72}$$

Where β is the transconductance parameter, V_{Gs} is the gate to source voltage and V_{TH} is the threshold voltage of the MOSFET. Defining new currents I_1, I_U and I_o given by

$$\begin{aligned} I_1 &= \beta\left(V_1 - V_{TH}\right)^2 \Rightarrow V_1 = \sqrt{\frac{I_1}{\beta}} + V_{TH} \\ I_U &= \beta\left(U - V_{TH}\right)^2 \Rightarrow U = \sqrt{\frac{I_U}{\beta}} + V_{TH} \end{aligned} \tag{3.73}$$

$$I_o = \frac{C^2}{\tau^2\beta} \Rightarrow \tau = \frac{C}{I_o\beta} \tag{3.74}$$

And after some manipulations, the state space equations become

$$\begin{aligned} C\dot{V}_1 &= 2k\sqrt{I_o I_U} - \sqrt{I_o I_1} + I_T(2k-1) \\ y &= V_1 \end{aligned} \tag{3.75}$$

Where $$I_T = \frac{CV_{TH}}{\tau} = V_{TH}\sqrt{I_o \beta} \tag{3.76}$$

Equation (3.75) is the complete derivation of the first order LP filter. An examination of Equation (3.75) reveals that, it needs two square-root circuits, a load capacitor, some current mirrors, two additional DC bias current sources and two n-type MOSFETs. From Equation (3.75), it is clear that for the implementation of the proposed LP filter, the square-root circuit is needed and is therefore given in Fig. 3.54 **[77, 155].** The complete circuit diagram of the proposed first-order AP filter as per the Equations (3.68) and (3.75) is then as shown in Fig. 3.55.

3.1.3.1.1.2. Second-Order AP Filter

The second-order AP filter transfer function can be written as follows:

$$H(s) = k\frac{s^2\tau^2 - \frac{s\tau}{Q} + 1}{s^2\tau^2 + \frac{s\tau}{Q} + 1} \tag{3.77}$$

Equation (3.77) can be decomposed to the following:

$$H(s) = \frac{Y(s)}{U(s)} = k - \frac{2k\frac{s\tau}{Q}}{s^2\tau^2 + \frac{s\tau}{Q} + 1} \tag{3.78}$$

The second term in the right hand side of Equation (3.78) is well known transfer functions of second order BP filter. By following the similar procedure introduced in the previous section, the complete derivation of the second-order BP filter is:

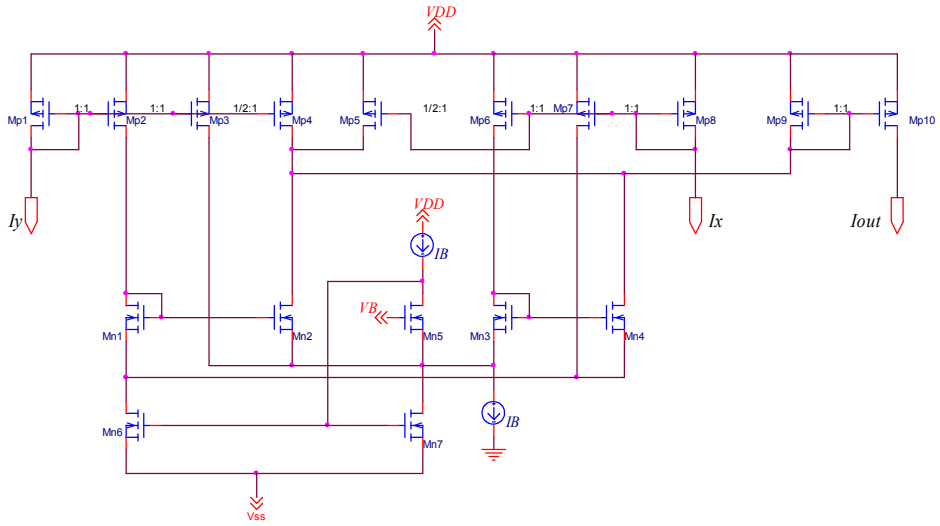
$$\begin{aligned} C\dot{V}_1 &= -\sqrt{I_o I_2} - I_T \\ C\dot{V}_2 &= \sqrt{I_o I_1} - \frac{\sqrt{I_o I_2}}{Q} + 2k\frac{\sqrt{I_o I_U}}{Q} + I_S \\ y &= V_2 \end{aligned} \tag{3.79}$$

Where

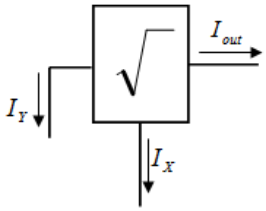
$$I_S = I_T\left(1 + \frac{2k}{Q} - \frac{1}{Q}\right) \tag{3.80}$$

Implementation of Equation (3.79) in circuit form needs three square-root circuits, two grounded capacitors, several current mirrors, three additional DC bias current sources and three n-type MOSFETs. The proposed second-order AP filter obtained as per Equations (3.78) and (3.79) is then as given in Fig. 3.56.

Moreover, a high-order AP filter can be implemented by cascading low-order (first order and second order) AP filters and the same has been verified in the simulated results.



(a)



$$I_{out} = \sqrt{I_X I_Y}$$

(b)

Fig. 3.54: *(a) Low-voltage current square-root (geometric-mean) cell (b) the employed symbol.*

3.1.3.1.1.3. Simulation results

In order to verify the theoretical predictions discussed in section 3.1.3.1.1., the proposed low-order AP circuits shown in Figs. 3.55 and 3.56 were simulated using TSMC 0.25 µm CMOS process parameters. For both the filters, the aspect ratios of transistors used in current mirror are W/L = 20µm/2 µm and those used in square-root circuit are given in Table 3.16.

With $V_{DD} = 1.5\ V$, $C_1 = C_2 = 56.27\ pF$, $I_0 = 5\mu A$, the simulated value of the pole frequency was 100 KHz. Figs. 3.57 and 3.58 depict the simulated magnitude and phase responses of the first order and second-order AP filter respectively. Furthermore, the simulated frequency responses of LP and BP filters, being the inherent building blocks of the low-order AP filters and high-order AP filters are shown in Fig. 3.59. In addition, the simulated frequency responses of high-order AP filter designs are shown in Fig. 3.60. To demonstrate the electronic tunability of the proposed circuits, I_0 was varied and the achieved results for 1.25 µA, 5 µA and 20 µA are shown in Fig. 3.61. In addition, the performance of the proposed AP filters was evaluated through the performance factors of linearity, noise, and mismatching. The obtained results are summarized in Table 3.17.

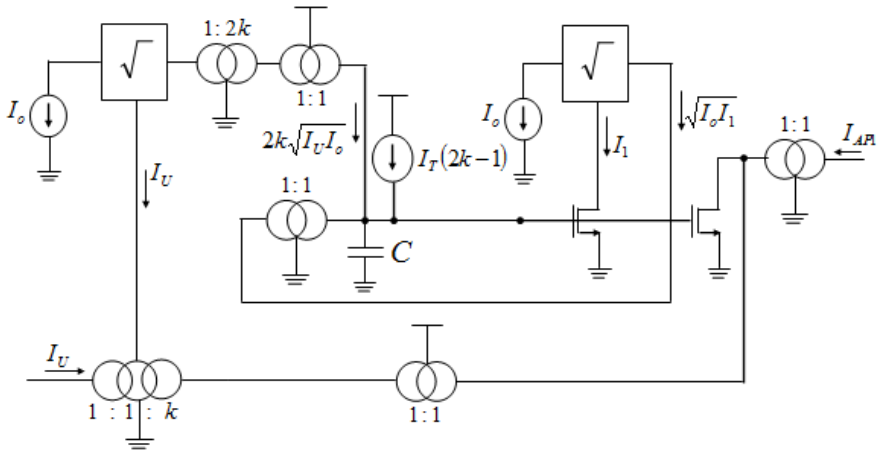


Fig. 3.55: *Proposed low-voltage SRD design of first-order AP filter.*

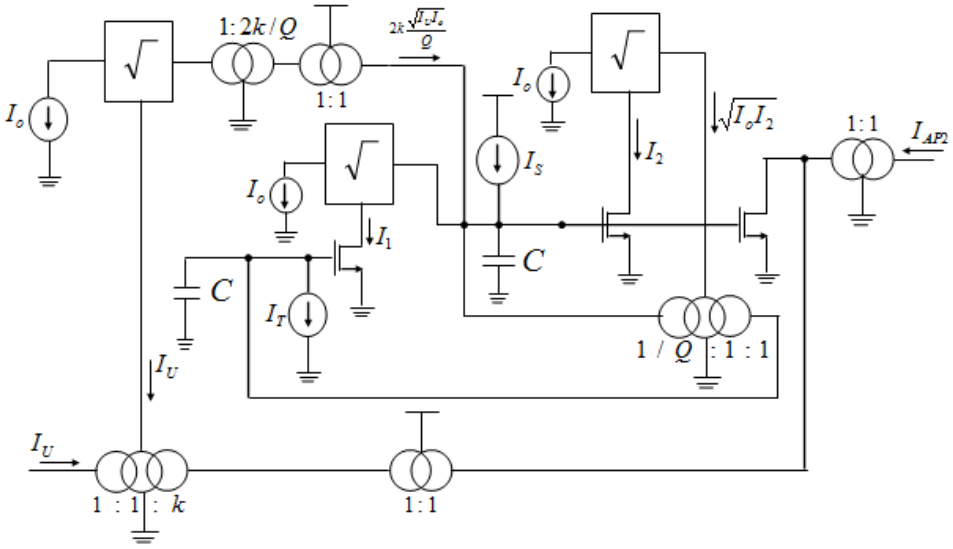
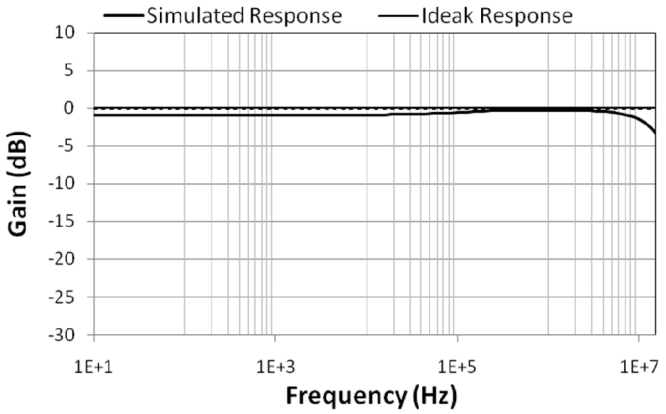
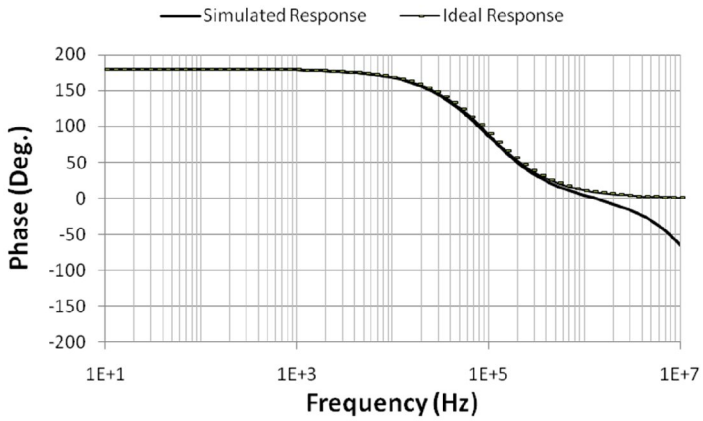


Fig. 3.56: *Proposed low-voltage SRD design of second-order AP filter.*

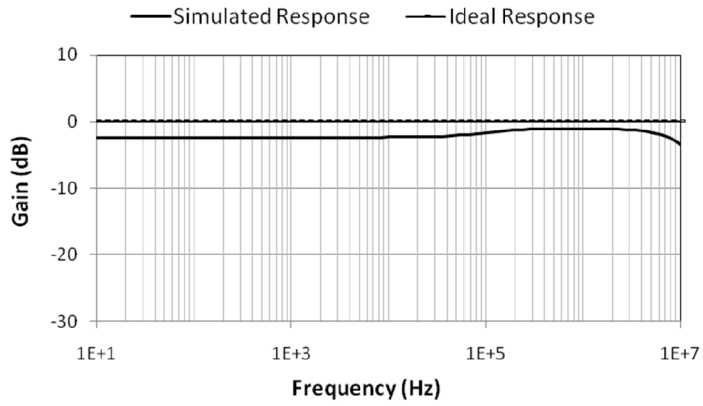


(a)

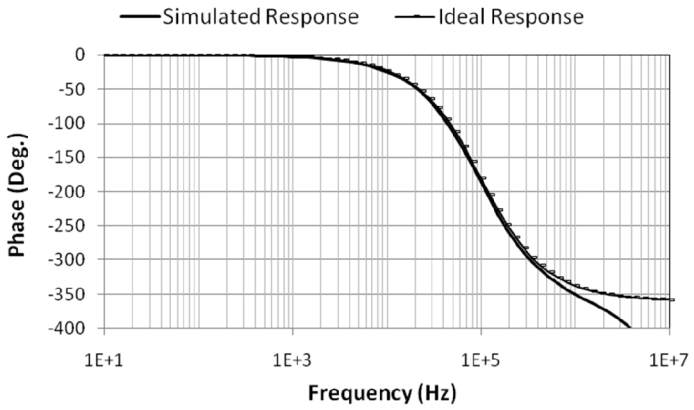


(b)

Fig. 3.57: *Simulated Responses of first-order AP filter (a) Magnitude Response (b) Phase Response.*



(a)



(b)

Fig. 3.58: *Simulated Responses of second-order AP filter (a) Magnitude Response (b) Phase Response.*

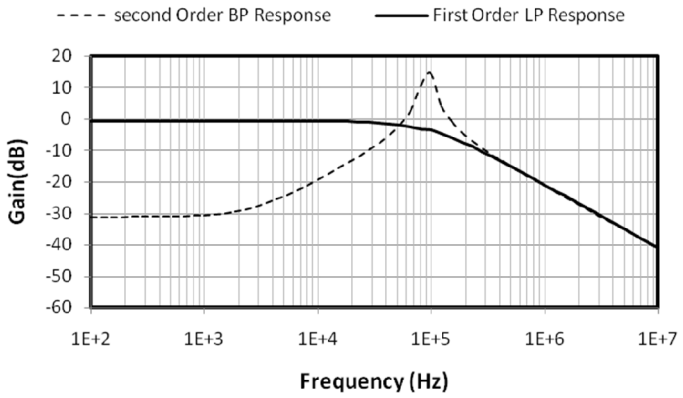


Fig. 3.59: *Simulated Magnitude Responses of first-order LP filter and second-order BP filter.*

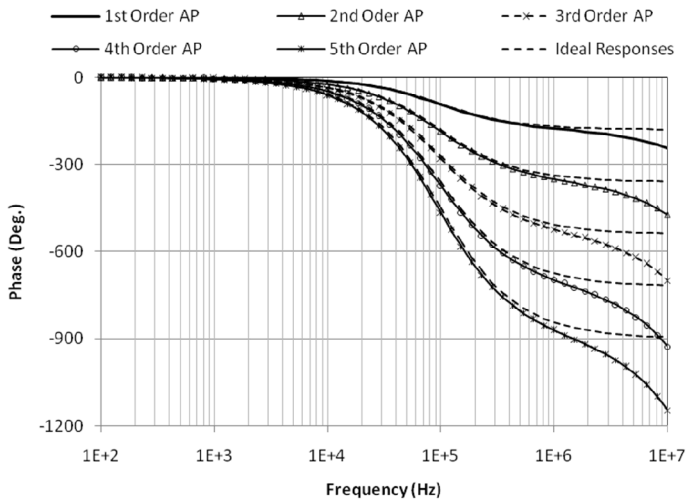


Fig. 3.60: *Simulated Phase Responses of High-order AP filters.*

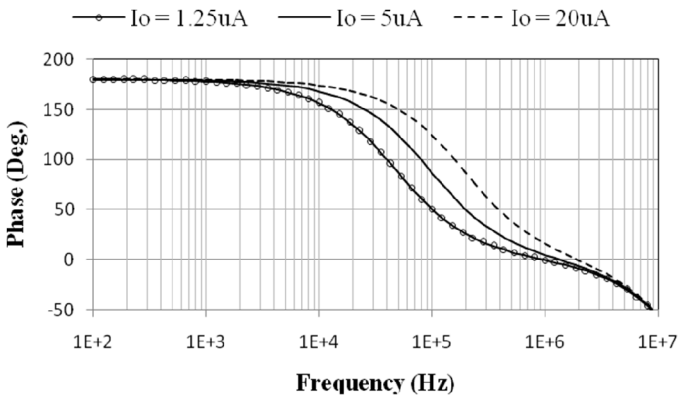


Fig. 3.61: *Demonstration of electronic tunability of the proposed AP designs.*

Transistor	W/L (µm/µm)
M_{p1}-M_{p3}	11.6/2
M_{p4}	5.8/2
M_{p5}	14/2
M_{p6}-M_{p10}	28/2
M_{n1}-M_{n4}	3.6/2
M_{n5}	20/2
M_{n6}-M_{n7}	30/2
M_{n8}-M_{n9}	10/2

Table 3.16: *Aspect ratio of the MOS transistors of the geometric Mean Blocks.*

Performance Factors	Values		
	1st Order AP	2nd Order AP	5th Order AP
Power Dissipation	250µW	475µW	1.03mW
Dynamic range	49.2dB	48.7dB	47.1dB
Sensitivity of ωo	76.4KHz	79.4KHz	83.5KHz

Table 3.17: *Results of performance factors for the proposed AP filters.*

3.1.4. Linear Transformation Synthesis Method of Companding Filters

In the Linear Transformation (LT) Synthesis Method of Companding Filters, the passive prototype filter is divided into small two-port networks and each small network is then transformed into companding-mode network and subsequently connected to form a Companding filter. Companding-domain LT filter can be synthesized from the passive prototype by the following procedures:

a) Each passive prototype filter is split into two-port subnetworks.
b) The transfer function of each two-port subnetwork is found and is appropriately transformed into companding-domain.
c) The companding-domain transfer function is synthesized using appropriate companding-domain blocks.
d) The passive prototype transfer function is replaced with their corresponding companding-domain transfer function and neighboring sections are connected with the cross-cascade interconnection.
e) The values of companding-domain parameters corresponding to passive parameters are determined.

3.1.4.1. Sinh-Domain (SD) Linear Transformation (LT) filters [J1]

Following the above consideration, an LT passive filter can be divided into the two-port subnetworks as given in Table 3.18. In order to perform filtering in the Sinh-Domain, the variables of the linear $u-y$ domain will be transformed into nonlinear variables in the $\hat{U}-\hat{Y}$ Sinh-domain. This can be achieved by utilizing the $SINH^{-1}$ *and* $SINH$ operators of Equations (2.40) and (2.41). Employing these operators, the proposed passive to SD substitution scheme is demonstrated in Table 3.18.

The corresponding expressions that describe the substitutions of the subnetworks from linear u-y domain to nonlinear $\hat{U}-\hat{Y}$ SD are also given in Table 3.18. $SINH(\hat{Y})=y,\quad SINH(\hat{U})=u=i_s,\quad SINH(\hat{U}_1)=u_1\quad SINH(\hat{U}_2)=u_2$. The linear-domain time constants in all rows are given by either of the formulas: $\tau=RC$ or $\tau=L/R$. The realized SD time constant for all rows is given by the expression: $\hat{\tau}_i=\hat{C}_iU_T/2I_0$. That is, the realized time-constants can be adjusted through the dc current *Io* and thus can be used to compensate cut-off frequency deviation caused by the MOS transistors imperfections. Concluding, the proposed substitution scheme offers a quick procedure

for deriving high-order SD filters. This is due to the fact that, having available the realization of SD FBDs in Table 3.18, just one step must be followed in order to obtain the corresponding SD filter structure. The realization of the SD FBDs in Table 3.18 will be discussed in the next Section, where the fundamental SD blocks will be introduced.

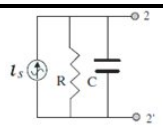
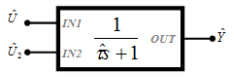
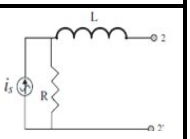
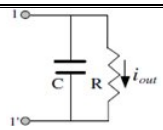
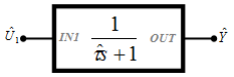
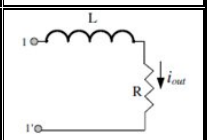
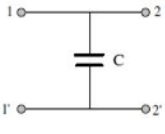
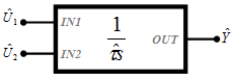
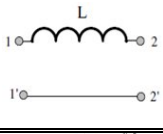
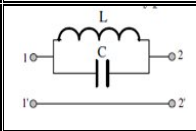
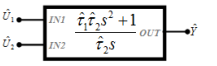
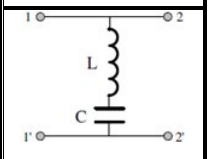
Row No.	Passive Prototype	Linear u-y domain Expressions	Sinh-Domain LT Equivalent	$\hat{U}-\hat{Y}$ Sinh-Domain Expressions
1.		$y=\frac{1}{\tau_i s+1}(u-u_2)$ $i=1,2$		$SINH(\hat{Y})=\frac{1}{\hat{\tau}_i s+1}[SINH(\hat{U})-SINH(\hat{U}_2)]$ $i=1,2$
2.				
3.		$y=\frac{1}{\tau s+1}(u_1)$		$SINH(\hat{Y})=\frac{1}{\hat{\tau}s+1}[SINH(\hat{U}_1)]$
4.				
5.		$y=\frac{1}{\tau_i s}(u_1-u_2)$ $i=1,2$		$SINH(\hat{Y})=\frac{1}{\hat{\tau}_i s}[SINH(\hat{U}_1)-SINH(\hat{U}_2)]$ $i=1,2$
6.				
7.		$y=\frac{\tau_1\tau_2 s^2+1}{\tau_2 s}(u_1-u_2)$		$SINH(\hat{Y})=\frac{\hat{\tau}_1\hat{\tau}_2 s^2+1}{\hat{\tau}_2 s}[SINH(\hat{U}_1)-SINH(\hat{U}_2)]$
8.				

Table 3.18: *Proposed substitution scheme for the derivation of SD LT filters.*

3.1.4.2. Realization of the Proposed SD LT Equivalents

By a simple inspection in the FBDs of rows 1–8 it is concluded that SD integrator configurations and resonator block must be available. Because of the fact that the SD integrator blocks were discussed in section 2.3.3, only, resonator block will be discussed as follows:

In order to realize the required function described by the FBDs in rows 7–8 of Table 3.18, the topology in Fig. 3.62 is proposed. Applying the KCL at node A the derived expression is given by:

$$2I_o = 2I_o \frac{I_o Sinh\left(\hat{U}_1\right) - I_o Sinh\left(\hat{U}_2\right) + I_o Sinh\left(\hat{V}_1\right) + I_o Cosh\left(\hat{Y}\right)}{I_o Cosh\left(\hat{Y}\right)} \tag{3.81}$$

After some algebraic manipulations and using Equation (2.41), the above expression could be alternatively rewritten as

$$-SINH\left(\hat{V}_1\right) = \left[SINH\left(\hat{U}_1\right) - SINH\left(\hat{U}_2\right)\right] \tag{3.82}$$

Similarly applying KCL at nodes B and C, the derived expressions are respectively given by:

$$SINH\left(\hat{V}_2\right) = -\frac{1}{s\hat{\tau}_2}\left[SINH\left(\hat{V}_1\right)\right] \tag{3.83}$$

$$SINH\left(\hat{V}_1\right) = -\frac{s\hat{\tau}_2}{s^2\hat{\tau}_1\hat{\tau}_2 + 1}\left[SINH\left(\hat{Y}\right)\right] \tag{3.84}$$

Combining Equations (3.82)–(3.84), the derived expression is

$$SINH\left(\hat{Y}\right) = \frac{s^2\hat{\tau}_1\hat{\tau}_2 + 1}{s\hat{\tau}_2}\left[SINH\left(\hat{U}_1\right) - SINH\left(\hat{U}_2\right)\right] \tag{3.85}$$

3.1.4.3. Simulation Results

In order to verify the validity of the proposed technique, a 3rd-order LC ladder lowpass All-pole and elliptic filters shown in Figs. 3.63(a) and 3.63(b) respectively, will be emulated. The SD LT filter topologies derived according to Table 3.18 are depicted in Figs. 3.64(a) and 3.64(b) respectively. The transfer functions corresponding to Figs. 3.63(a) and 3.64(b) are respectively given by

$$\frac{SINH\left(\hat{V}_{OUT}\right)}{SINH\left(\hat{V}_{IN}\right)} = \frac{1}{s^3\hat{\tau}_1\hat{\tau}_2\hat{\tau}_3 + s^2\left(\hat{\tau}_1\hat{\tau}_2 + \hat{\tau}_2\hat{\tau}_3\right) + s\left(\hat{\tau}_1 + \hat{\tau}_2 + \hat{\tau}_3\right) + 2} \tag{3.86}$$

$$\frac{SINH\left(\hat{V}_{OUT}\right)}{SINH\left(\hat{V}_{IN}\right)}=\frac{s^2\hat{\tau}_2\hat{\tau}_3+1}{s^3\left(\hat{\tau}_2\left(\hat{\tau}_1\hat{\tau}_4+\hat{\tau}_3\hat{\tau}_4+\hat{\tau}_1\hat{\tau}_3\right)\right)+s^2\left(\hat{\tau}_1\hat{\tau}_2+2\hat{\tau}_2\hat{\tau}_3+\hat{\tau}_2\hat{\tau}_4\right)+s\left(\hat{\tau}_1+\hat{\tau}_2+\hat{\tau}_4\right)+2} \tag{3.87}$$

The evaluation of the performance of the filters has been done using the PSPICE software. In addition, the transistor models provided by the BISIM 0.35µm process will be employed in simulations. The aspect ratio of both NMOS and PMOS transistors that construct the translinear loops in S and C cells was chosen to be 5µm/5µm, whereas the aspect ratios of the other NMOS and PMOS transistors were 5µm/5µm and 50µm/5µm, respectively.

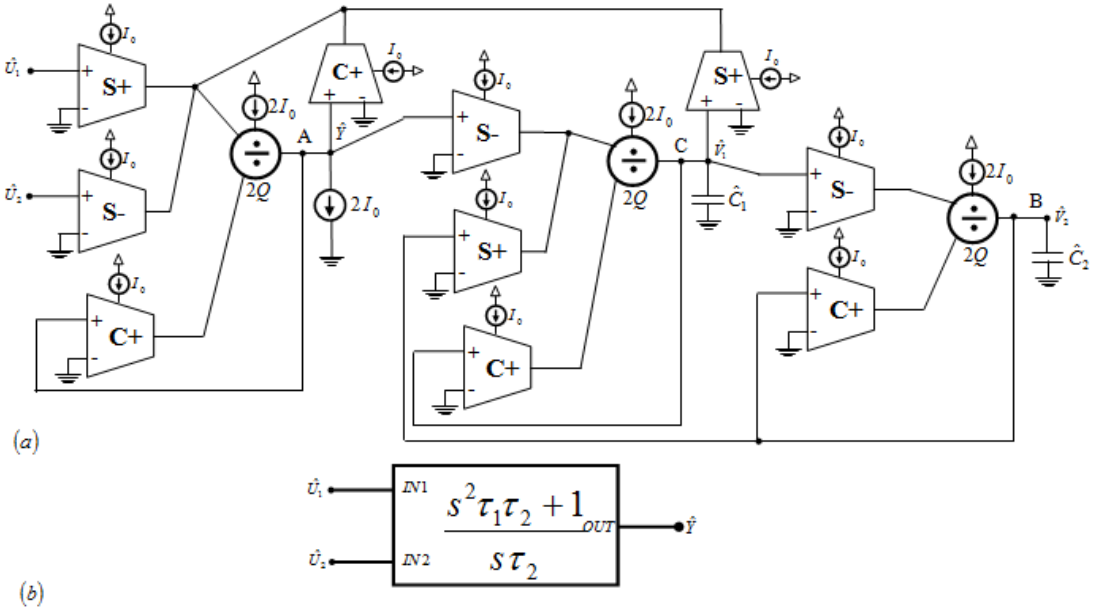


Fig. 3.62: Proposed LT SD equivalent of the LC resonators in Table 3.18.

A symmetrical supply voltage equal to ±0.75V has been chosen, while the dc current I_0 was 100 pA. The dc power dissipation for the filter in Fig. 3.64(a) was 21.1 nW, while for the filter in Fig. 3.64(b) the value was 27.5 nW. A frequency response with cutoff frequency 41 Hz will be achieved in an All-pole filter and cutoff frequency of 27.5 Hz and a passband ripple of 1dB will be achieved in an Elliptic filter. For the above values of cut-off frequency and Passband ripple, the values of capacitors for an All-pole filter were chosen as $\hat{C}_1=\hat{C}_2=\hat{C}_3=30pF$ and that for elliptic filter were chosen as $\hat{C}_1=\hat{C}_4=50pF,\hat{C}_2=\hat{C}_3=20pF$. With modulation index

$\left(m = i_{peak}/I_{bias} = 35\%\right)$, the simulated frequency responses of the SD LT filter topologies are depicted in Fig. 3.65.

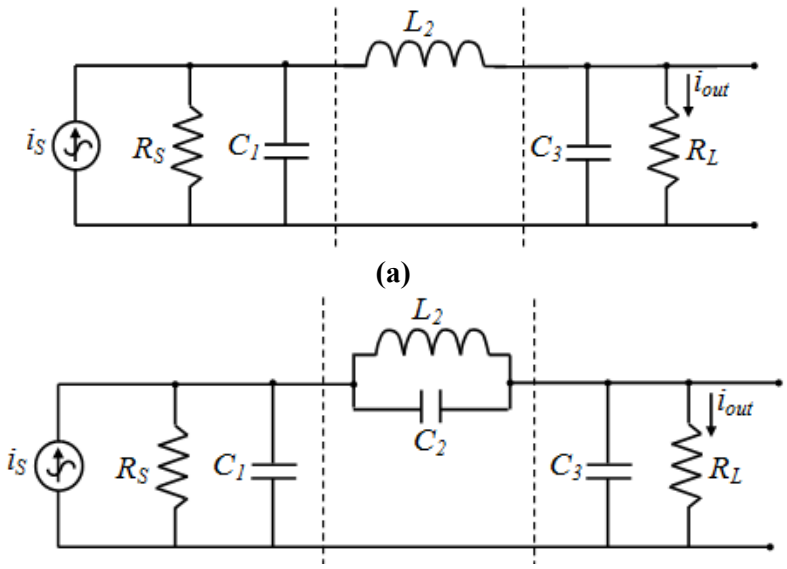


Fig. 3.63: 3rd-order LC ladder lowpass filters, (a) All-pole, and (b) Elliptic.

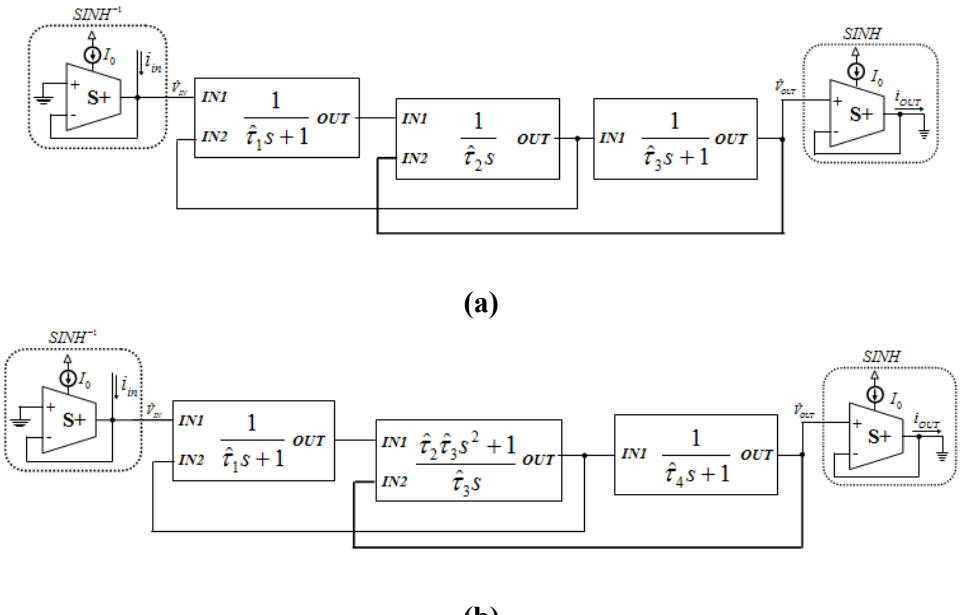
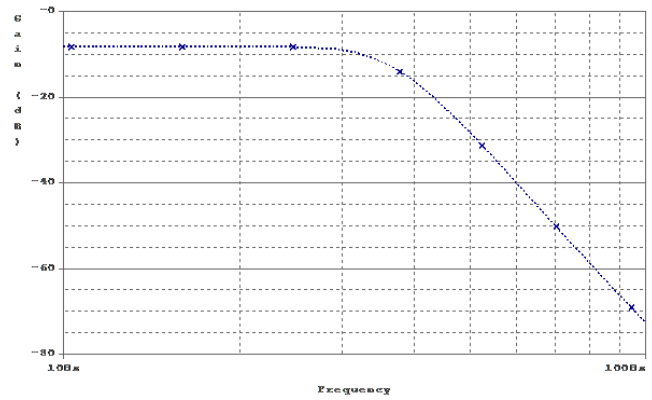
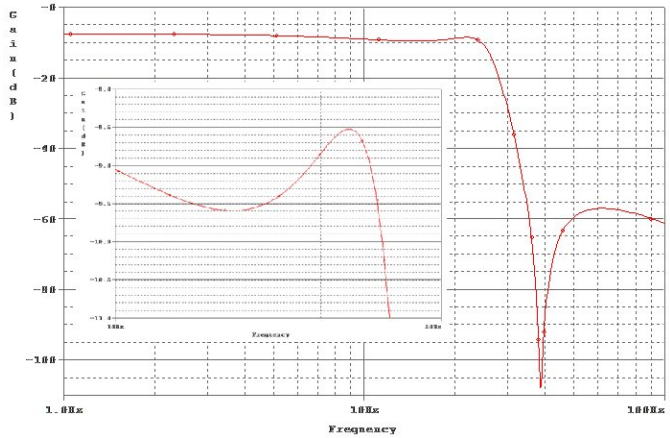


Fig. 3.64: 3rd-order SD LT filter topologies derived according to Table 3.18, (a) All-pole, and (b) Elliptic.



(a)



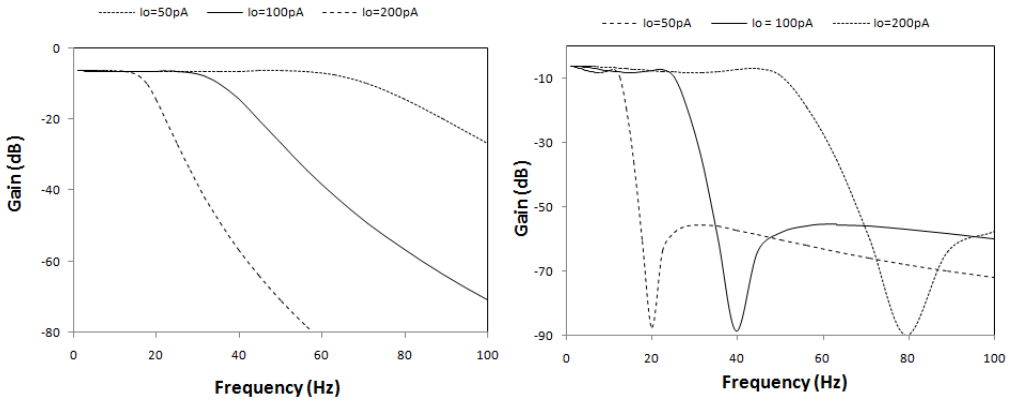
(b)

Fig. 3.65: Simulated frequency responses of the filters in Fig. 3.64. (a) All-pole (b) Elliptic.

In addition, the linear behavior of the outputs of the filter was evaluated through the consideration of their IMD3 performance. For this purpose, two closely spaced tones (i.e. 10–11 Hz) with variable amplitude have been simultaneously applied at the inputs of the filters. Considering the spectrum of the output currents, THD level 1% is observed at an input rms value 1.39 nA for the filter in Fig. 3.64(a) and 1.32 nA for the filter in Fig. 3.64(b). The noise was integrated over a 100 Hz range and the simulated rms value of the input referred noise was 0.56 pA for the filter in Fig. 3. 3.64(a) and 0.59 pA for the filter in Fig. 3.64 (b). Thus, the calculated value of the dynamic range, at 1% distortion level, will be 67.89 dB for the filter in Fig. 3.64(a) and 67 dB for the filter in Fig. 3.64(b). The effects of passive and active elements mismatching in the frequency behavior of the filter have been considered by employing the well-known Monte–Carlo method. The simulated values of standard deviation of the low-frequency gain for the all-pole and elliptic SD LT filter

topologies were 0.07 and 0.074 and that of the cut-off frequency were 0.084 Hz and 0.092 Hz, respectively.

The electronic tunability of the all-pole and elliptic SD LT filter topologies were demonstrated by performing simulations of its frequency response at different levels of current I_o. The derived responses of all-pole and elliptic filter SD LT filter topologies for I_o=50pA, 100pA, and 200pA are simultaneously plotted in Fig. 3.66(a) and Fig. 3.66(b) respectively, where the capability for electronic tuning of the LT SD filters can be verified.



(a) (b)

Fig. 3.66: Demonstration of electronic tunability, (a) All-pole, and (b) Elliptic.

3.2. Summary

In the chapter, six techniques for designing the companding filters were discussed in detail. The simple but novel contributions which fall under four of the six techniques were also presented. The performance of the proposed low-voltage low-power novel designs were presented in detail. It has been the endeavor to directly correlate the applications of the proposed designs in portable systems. Besides, the comparison study of performance parameters of the proposed designs with those reported in the open literature was carried out. Based on the study, it can be noticed that the proposed designs offer the benefits of: **a)** low-voltage low-power suitable for the contemporary technology of monolithic ICs **b)** the modularity of the filter's structure due to the fact that it is exclusively constructed from lossless/lossy integrators and subtraction/summation blocks, **c)** the canonical structures with lesser number of active and passive components **d)** the electronic tunability of frequency characteristics through DC currents **e)** freedom from matching conditions **f)** use of grounded capacitors, required for the absorption of parasitic capacitances and small chip areas is also

present and as a sequel designs are suitable for fabricating in monolithic chip **g)** improved linearity **h)** low power consumption **i)** extended dynamic range, and, **j)** improved power efficiency.

The work carried out in this chapter got recognition by various journals and conferences which published the papers based on the results of this thesis (see list of published, accepted and communicated papers).

CHAPTER-4

Conclusions and Scope for Future Work

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

4.1. Conclusions

This chapter finally summarizes the complete work done during the course of this study. Apart from a breadboard realization of one of the designs, the circuits presented in this Thesis could not be physically realized due to the lack of adequate resources at the place of research. The theoretical behavior of the circuits has only been supported by PSPICE simulation results. However, I expect some funding from our reputed organization in the near future and with the collaboration from Electronics Laboratory, Patras University team, some chip designs of the companding designs will definitely come in the near future.

The present investigation is primarily concerned with the study and design of low-voltage low-power companding filters for portable system applications. The motivation for this study emanated because low-voltage low-power companding filters have gained prominence in recent times due to the advent of mobile communications gadgets and portable electronic systems. New design techniques are proposed for companding filter design to improve upon the features such as Bias, Linearity, sensitivity, power consumption, tunability etc. Some of the low-order deigns have the orthogonal tuning feature. Besides, high-order companding universal filter designs were proposed for the first time in the literature. The work carried out in this thesis got recognition by various journals and conferences which published the papers based on the results of this thesis.

Chapter 1 gives a brief introduction about the significance of low-voltage low-power analog integrated filters, present technologies of their design and the associated complexities in their design. The chapter also includes the motivation for the study and objectives achieved in the thesis.

Chapter 2 presents a review of companding filters. The three main classifications of the companding filters i.e. LD, SRD and SD, are fully discussed. Towards this end, the operators and building blocks required to design three classifications are discussed in detail and the translinear principle used to implement these blocks is also discussed.

Chapter 3 discusses the six techniques used to implement the companding filters. The steps to obtain a companding filter through either of these techniques are discussed in detail. Most of the techniques are concluded with the introduction of the contributions in the various International Journals of repute.

4.2. Suggestions for the future work

Despite much work has been done on low-voltage low-power companding filters and in spite of the fact that wealth of the literature available on the subject, there is still a lot of scope to further this knowledge.

Although PSPICE simulators now have the capability to model the devices as close to the actual parameters, still the simulated results may not be exactly same as the results obtained from the hardware implementations. The first and foremost proposal for further work is to implement the proposed circuits for companding filters in silicon. The proposed designs can then be applied by the real time signal obtained from the live source. This will give the scope for improving the circuit performances.

As the device dimensions of the digital circuits are continuously decreasing, the power supply is also decreased at the same rate to ensure the proper functioning of the devices. According to data that provides information about the near future of semiconductor technology, International Technology Roadmap for Semiconductors (ITRS), the supply voltage for digital circuits for 2013 in 32 nm technology is 0.5 V. To make the companding filters compatible with the digital circuits so that both can be integrated over the same integrated chip, the new companding filters have to be designed with comparable power supplies. Work has already been started to design companding filters about 0.5V supply using MOSFETs in weak inversion region.

Low-voltage low-power companding filters are being designed by employing MOSFETs operating in strong or weak inversion regions. The proper functioning of the companding filters depends on the square or exponential i-v relationship of the MOSFETs in the two regions. The relationship is valid upto to few Hertz to few hundred Kilohertz. Thus, the design focus of the new low-voltage low-power companding filters has to be low frequency applications. Therefore, the utilization of low-voltage low-power companding filters could be exploited in the fields of: Short-range wireless communications; Biomedical Electronics for implantable devices, such as pacemakers, blood flow meters and auditory stimulators; Hardware Neural Network design; Neuromorphic designs etc.

Finally, the new nano-electronic devices in which the i-v relationship is valid at high frequencies as well could be explored for companding filter designs.

Appendix-A

List of Published, Accepted and Communicated Papers

Publications in Journals:

[J1]. **F. A. Khanday**, C. Kasimis, C. Psychalinos and N. A. Shah, "Sinh-Domain Linear Transformation Filters". International Journal of Electronics (Taylor and Francis, UK), http://dx.doi.org/10.1080/00207217.2013.780265,2013. (0020-7217 (Print), 1362-3060 (Online), Impact Factor: 0.44).

[J2]. N. A. Shah and **F. A. Khanday**, "A Multiple-Input-Multiple-Output Log-Domain Universal biquad filter". *Indian Journal of pure and Applied Physics (India), Vol. 50, pp. 928-934, 2012. (ISSN: 0019-5596 (print), 0975-1041 (online); Impact Factor: 0.763 (2011)).*

[J3]. **F. A. Khanday**, C. Psychalinos and N. A. Shah, "Square-Root-Domain Realization of Single Cell Architecture of Complex TDCNN," *Circuits, Systems and Signal Processing, Published Online,* DOI: 10.1007/s00034-012-9503-1 *(ISSN: 0278-081X (print), 1531-5878 (online); Impact Factor: 0.817 (2011)).*

[J4]. **F. A. Khanday** and N. A. Shah, "A Low Voltage and Low Power Sinh-Domain Universal Biquadratic Filter for low frequency Applications". *Turkish Journal of Electrical Engineering and Computer Sciences (Turkey), Accepted for Publication, 10.3906/elk-1203-128,* (ISSN: 1300-0632 (print), 1303-6203 (online); Impact Factor: 0.283 (2011)).

[J5]. N. A. Shah and **F. A. Khanday**, *"A Generic Current Mode Design for Multi-function Grounded capacitor Filters Employing Log-Domain Technique". Journal of Active and Passive Electronic Components (Hindawi Publishing Corporation, USA), Volume 2011 (2011), Article ID 313580, 10 pages doi:10.1155/2011/313580, (ISSN 0882-7516).*

[J6]. N. A. Shah and **F. A. Khanday**, "A DC stabilized log-domain nth-order multifunction filter based on the decomposition of nth-order HP filter function to FLF topology" *International Journal of Circuit Theory and Applications (Wiley and Son's Ltd., UK), Vol. 37, pp. 1075-1091, 2009, DOI: 10.1002/cta.533. (ISSN: 1097-007X, Impact Factor: 1.65 (2011)).*

[J7]. N. A. Shah and **F. A. Khanday**, "Log-domain synthesis of nth-order universal filter". *Analog Integrated Circuits and Signal Processing (USA), Vol. 59, No. 3, pp. 309-315, June, 2009, DOI 10.1007/s10470-008-9258-6. (ISSN: 0925-1030 (print), 1573-1979 (online); Impact Factor: 0.592 (2011)).*

[J8]. E. Stoumpou, **F. A. Khanday**, C. Psychalinos, and N. A. Shah, "A Low-Voltage Square-Root Domain n-th Order Multifunction FLF Filter Topology". *Analog Integrated Circuits and Signal Processing (USA), Vol. 61, No. 12, pp. 315-322, June, 2009, DOI 10.1007/s10470-009-9307-9. (ISSN: 0925-1030 (print), 1573-1979 (online); Impact Factor: 0.592 (2011)).*

[J9]. N. A. Shah and **F. A. Khanday**, "A MISO Electronically Tunable Log-Domain Universal Biquad with Digital Programmability" *Frequenz, Journal of RF Engineering and Telecommunications (Germany), Vol. 69, No. 1-2, pp. 36-41, 2009. (ISSN: 0016-1136; Impact Factor: 0.124 (2011)).*

[J10]. N. A. Shah and **F. A. Khanday**, "Synthesis of SIFO electronically tunable log-domain universal biquad" *Frequenz, Journal of RF Engineering and Telecommunications (Germany), Vol. 68, No. 1-2, pp. 30-36, 2008. (ISSN: 0016-1136; Impact Factor: 0.124 (2011)).*

Accepted for publication/revision in Journals:

[J11]. **F. A. Khanday**, C. Psychalinos and N. A. Shah, "Universal filters of arbitrary order and type employing square-root-domain technique". *International Journal of Electronics (Taylor and Francis, UK), (0020-7217 (Print), 1362-3060 (Online), Impact Factor: 0.44), Accepted for Publication*.

[J12]. K. Roumelioti, C. Psychalinos, **F. A. Khanday**, and N. A. Shah, "1.2V Sinh-Domain Allpass Filter", *International Journal of Circuit Theory and Applications (Wiley and Son's Ltd., UK), (ISSN: 1097-007X, Impact Factor: 1.65), Accepted for Revision.*

[J13]. N. A. Shah and **F. A. Khanday**, "Design of general multifunction biquads and their comparative study using log-domain technique". *J. of Active and Passive Electronic Devices (USA) Accepted for Publication. (*ISSN: 1555-0281 (print); 1555-029X (online)).

[J14]. N. A. Shah and **F. A. Khanday**, "Synthesis of first-order log-domain All-pass/Multifunction filters based on transfer function decomposition, *WSEAS Transactions on Circuits and Systems (USA), Accepted for Publication.*

Publications in Conferences:

[C1]. **F. A. Khanday**, "Low-Voltage Square-Root-Domain Complex Filter for Bluetooth/ZigBee Applications", 8th–JK Science Congress, 15-17 September 2012, University of Kashmir.

[C2]. **F. A. Khanday** and N. A. Shah, "An ultra low power Sinh-Domain multifunction filter for neuromorphic systems and biomedical signal processing", *International Conference on Recent Advances in Electronics and Computer Engineering, 17-18 Dec. 2011, Eternal University, Baru Sahib, HP, India.*

[C3]. **F. A. Khanday** and N. A. Shah, "State-Space Square-root domain transformation of linear passive prototypes", *7th–JK Science Congress, 13-15 October 2011, University of Jammu.*

[C4]. **F. A. Khanday** and N. A. Shah, "Design of low-voltage Sinh-domain multifunction Biquad for low frequency applications", *7th–JK Science Congress, 13-15 October 2011, University of Jammu.*

[C5]. N. A. Shah and **F. A. Khanday**, "A novel Square-Root-Domain Lowpass biquad" *4th–JK Science Congress, 12-14 November 2008, University of Kashmir.*

Appendix-A

Bibliography

[1]. A. A. El-Adawy and A. M. Soliman, "A Low-Voltage Single Input Class AB Transconductor with Rail-to-Rail Input Range". IEEE Transactions on Circuits and Systems-II, Vol. 47, No. 2, pp. 236–242, 2000.

[2]. J. F. Duque-Carrilloet et al., "1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology", IEEE Journal of Solid State Circuits, Vol. 35, No. 1, pp. 33–43, 2000.

[3]. C. Lin and M. Ismail, "Robust Design of LV/LP Low-Distortion CMOS Rail-to-Rail Input Stages", Journal of Analog Integrated Circuits and Signal Processing, Vol. 21, pp. 153–161, 1999.

[4]. Klaas-Jan de Langen and J. H. Huijsing, "Compact Low-Voltage Power-Efficient Operational Amplifier Cells for VLSI", IEEE Journal of Solid State Circuits, Vol. 33, No. 10, pp. 1482–1496, 1998.

[5]. G. Ferri, W. Sansen, and V. Peluso, "A Low-Voltage Fully-Differential Constant-Gm Rail-to-Rail CMOS Operational Amplifier", Journal of Analog Integrated Circuits and Signal Processing, Vol. 16, pp. 5–15, 1998.

[6]. G. Xu et al., "A Low Voltage Fully Differential Nested Capacitance Amplifier: Analysis and Design", In Proceedings of the IEEE International Symposium on Circuits and Systems, Vol. 2, pp. 606–609, 1999.

[7]. S. Setty and C. Toumazou, "N-Folded Cascode Technique for High Frequency Operation of Low Voltage Opamps", Electronics Letters, Vol. 32, No. 11, pp. 955–956, 1996.

[8]. R. Fried and C. Enz, "Nano-Amp, Active Bulk, Weak-Inversion Analog Circuits", In Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 31–34., 1998.

[9]. B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V Op Amps Using Standard Digital CMOS Technology", IEEE Transactions on Circuits and Systems-II, Vol. 45, No. 7, pp. 769–779, 1998.

[10]. G. Dehng et al., "A 900-MHz 1-V CMOS Frequency Synthesizer", IEEE Journal of Solid State Circuits, Vol. 35, No. 8, pp.1211–1214, 2000.

[11]. J. Shin et al., "A New Charge Pump Without Degradation in Threshold Voltage Due to Body Effect", IEEE Journal of Solid State Circuits, Vol. 35, No. 8, pp. 1227–1230, 2000.

[12]. H. Lin, K. Chang, and S. Wong, "Novel High Positive and Negative Pumping", In Proceedings of the IEEE International Symposium on Circuits and Systems, Vol. 1, pp. 238–241, 1999.

[13]. R. St. Pierre, "Low-Power BiCMOS OpAmp with Integrated Current Mode Charge Pump", In Proceedings of the IEEE European Solid-State Circuits Conference, pp. 70–73, 1999.

[14]. J. Wu and K. Chang, "MOS Charge Pumps for Low-Voltage Operation", IEEE Journal of Solid State Circuits, Vol. 33, No. 4, pp. 592–597, 1998.

[15]. T. A. F. Duisters and E. C. Dijkmans, "A -90dB THD Rail-to-Rail Input Opamp Using a New Local Charge Pump in CMOS", IEEE Journal of Solid State Circuits, Vol. 33, No. 7, pp. 947–955, 1998.

[16]. P. Favrat, P. Deval, and M. J. Declercq, "An Improved Voltage Doubler in a Standard CMOS Technology", In Proceedings of the IEEE International Symposium on Circuits and Systems, Vol. 1, pp. 249–252, 1997.

[17]. J. F. Dickson, "On-Chip High-Voltage Generation MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique", IEEE Journal of Solid State Circuits, Vol. 11, No. 3, pp. 374–378, 1976.

[18]. J. Sim et al., "Adaptive Biasing Folded Cascode CMOS OP Amp with Continuous-Time Push-Pull CMFB Scheme", IEICE Transactionson Electronics, Vol. E80-C, No. 9, pp. 1203–1210, 1997.

[19]. M. G. Degraune et al., "Adaptive Biasing CMOS Amplifiers", IEEE Journal of Solid State Circuits, Vol. 17, No. 3, pp. 522–528, 1982.

[20]. R. Klinke, B. J. Hosticka, and H. J. Pfleiderer, "A Very-High-Slew-Rate CMOS Operational Amplifier", IEEE Journal of Solid State Circuits, Vol. 24, No. 3, pp. 744–746, 1989.

[21]. K. Nagaraj, "Slew Rate Enhancement Technique for CMOS Output Buffers", Electronics Letters, Vol. 25, No.19, pp. 1304–1305, 1989.

[22]. E. Vittoz and J. Fellroth, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation", IEEE Journal of Solid State Circuits, Vol. 12, No. 3, pp. 224–231, 1977.

[23]. C. Toumazou, F. J. Lidgey and D. G. Haigh, "Analogue IC design: The current mode approach", Stevenge, U. K.: Peregrinus Ltd, 1990.

[24]. A. F. Arbel, J. E. Bowers and J. Lauch, "Low noise high speed optical receiver for optic fibre system", IEEE Journal of solid state circuits, Vol. 19, pp. 155-157, 1984.

[25]. T. Koulberg, "A CMOS current-mode operational amplifier", IEEE Journal of solid state circuits, Vol. 28, pp. 849-852, 1993.

[26]. E. Vittoz, "Low power low-voltage limitations and prospects in analog design", in R. J. v. d. Plassche, W. M. C. Sansen, and J. H. Huijsing, eds., Analog Circuit Design, Low-Power, Low-Voltage, Integrated Filters and Smart-Power, Kluwer, Boston, 1995.

[27]. Y. P. Tsividis, V. Gopinathan, and L. Toth, "Companding in signal processing", Electronics Letters, Vol. 26, pp. 1331-1332, 1990.

[28]. Y. Tsividis, "Externally linear time-invariant systems and their applications to companding signal processors", IEEE Transaction on Circuits and Systems-II, Vol. 44, No. 2, pp. 65-85, Feb. 1997.

[29]. S. Haykin, "Communication Systems", 3rd edition, John Wiley, 1994.

[30]. E. Blumenkrantz, "Analog floating point technique", Proceedings of IEEE Symposium on Low Power Electronics, San Jose, CA, pp. 72-73, Oct. 1995.

[31]. E. Seevinck, "Companding current mode integrator: a new circuit principle for continuous time monolithic filters", Electronics Letters, Vol. 26, no. 24, pp. 2046-2047, Nov. 1990.

[32]. D. R. Frey, "Log-domain filtering: an approach to current mode filtering", IEE Proc. G 1993, Vol. 140, no. 6, pp. 406-416, Dec. 1993.

[33]. R. W. Adams, "Filtering in the log domain", Preprint #1470 presented at the 63rd AES Conference, New York, NY, May 1979.

[34]. B. Gilbert, "Translinear circuits: a proposed classification". Electronics Letters, Vol. 11, No. 1, pp. 14-16, 1975.

[35]. E. Seevinck, "Analysis and Synthesis of Translinear Circuits". Elsevier, Amsterdam, 1988.

[36]. D. Perry and G. W. Roberts, "Design of log-domain filters based on the operational simulation of LC ladders," IEEE Transaction on Circuits and Systems-II, Vol. 43, pp. 763–773, 1996.

[37]. D. Perry and G.W. Roberts, "Log-domain filters based on LC ladder synthesis", In Proceeding to IEEE international symposium on circuits and systems(ISCAS'1995), Vol. 1, pp. 311-314, 1995.

[38]. J. Mahattanakul and C. Toumazou, "Modular log-domain filters based upon linear Gm–C filter synthesis", IEEE Transactions on Circuits and Systems-II, Vol. 46, No. 12, pp. 1421–1430, 1999.

[39]. E. M. Drakakis, A. J. Payne and C. Toumazou, "Log-domain filtering and the Bernoulli cell". IEEE Transactions on Circuits and Systems-I, Vol. 46, No. 5, pp. 559-571, 1999.

[40]. J. Mulder et al., "General current mode analysis of translinear filters", IEEE Transactions on Circuits and Systems-I, Vol. 44, No. 3, pp. 193-197, 1997.

[41]. D. Frey and A. Tola, "A state space formulation for externally linear class AB dynamical circuits". IEEE Transactions on Circuits and Systems-II, Vol. 46, No. 3, 1999.

[42]. J. Mulder et al., "A syllabic companding translinear Filter", In Proceedings of IEEE International symposium on circuits and systems (ISCAS'1997), Vol. 1, pp. 101-104, Hong Kong, 1997.

[43]. Y. Tsividis, "General approach to signal processors employing companding". Electronics Letters, Vol. 31, No. 18, pp. 1549-1550, 1995.

[44]. D. R. Frey and Y. P. Tsividis, "Syllabically companding Log-Domain filter using dynamic biasing", Electronics Letters, Vol. 33, No. 18, pp. 1506-1507, 1997.

[45]. Y. Tsividis, "Minimizing power dissipation in analogue signal processors through syllabic companding", Electronics Letters, Vol. 35, No. 31, pp. 1805-1807, 1999.

[46]. M. Punzenberger and C. Enz, "A 1.2-V low power BiCMOS class AB log-domain filter", IEEE Journal of Solid State Circuits, Vol. 32, pp. 1968-1978, 1997.

[47]. G. van Ruymbekeet et al., "A BiCMOS programmable continuous-time filter using image-parameter synthesis and voltage companding technique", IEEE Journal of solid state circuits, Vol. 33, No. 3, 1997.

[48]. V. W. Leung, G. W. Roberts, "Effects of transistor non-idealities on high-order log-domain ladder filter frequency responses", IEEE Transactions on Circuits and Systems-II, Vol. 47, No. 5, pp. 373-387, 2000.

[49]. N. Fragoulis, C. Psychalinos and I. Haritantis, "Modular Log-Domain Filters Realized Using Wave Port Terminators", IEEE Transaction on Circuits and Systems-I, Vol. 51, No. 11, pp. 2235-2244, 1995.

[50]. C. Psychalinos, "On the transposition of Gm–C filters to DC stabilized log-domain filters". International Journal of Circuit Theory and Applications, Vol. 34, No. 2, pp. 217–236, 2006.

[51]. M. El-Gamal, R. A. Baki, and A. Bar-Dor, "30-100 MHz NPN-only variable gain class AB companding based filters for 1.2V applications", Proceedings 2000 ISSCC, Vol. 43, pp. 150-151, San Fransisco, Feb. 2000.

[52]. Mourad N. El-Gamal and Gordon W. Roberts, "Very High-Frequency Log-Domain Bandpass Filters". IEEE Transactions on Circuits and Systems-II, Vol. 45, No. 9, pp. 1188-1198, 1998.

[53]. A. Kircaya and U. CAM, "Novel log-domain first-Order multifunction filter", ETRI Journal, Vol. 8, No. 3, pp. 401-404. 2006.

[54]. E. I. El-Masry and W. U. Jie, "CMOS Micro power universal log-domain biquad" IEEE Transactions on Circuits and Systems-I, Vol. 46, No. 3, pp. 389-392, 1999.

[55]. N. A. Shah and F. A. Khanday, "Synthesis of SIFO Electronically Tunable Log-Domain Universal Biquad". Frequenz, Journal of RF Telecommunications, Vol. 68, No. 1-2, pp. 30-36, 2008.

[56]. N. A. Shah and F. A. Khanday, "A MISO Electronically Tunable Log-Domain Universal Biquad with Digital Programmability", Frequenz, Journal of RF Engineering and Telecommunications, Vol. 69, No. 1-2, pp. 36-41, 2009.

[57]. C. Psychalinos, "Realization of log-domain high-order transfer functions using first-order building blocks and complementary operators", International Journal of Circuit Theory and Applications, Vol. 35**,** pp. 17–32, 2007.

[58]. X. Zhang, W. Mekaw and E. El-Masry, "Leap-frog-based synthesis of CMOS micro-power nth-order log-domain filters", In Proceeding IEEE International Symposium on Circuit and Systems (ISCAS'2004), pp. 305-308, 2004.

[59]. C. Psychalinos, "Improved building blocks for log-domain linear transformation filters", In Proceedings of IEEE International Conference on Circuits and Systems (ISCAS), Kos, Greece, pp. 1535–1538, 2006.

[60]. C. Psychalinos, "Log-domain linear transformation filters revised: Improved building blocks and comparison results", International Journal of Circuit Theory and Applications, Vol. 36, pp. 119–133, 2008.

[61]. N. A. Shah and F. A. Khanday, "Log-domain synthesis of nth-order universal filter", Analog Integrated Circuits and Signal Processing (USA), Vol. 59, No. 3, 2009.

[62]. N. A. Shah and F. A. Khanday, "A DC stabilized log-domain n^{th}-order multifunction filter based on the decomposition of n^{th}-order HP filter function to FLF topology", International Journal of Circuit Theory and Applications, Vol. 37, pp. 1075-1091, 2009.

[63]. N. A. Shah and F. A. Khanday, "A Generic Current Mode Design for Multi-function Grounded capacitor Filters Employing Log-Domain Technique", Journal of Active and Passive Electronic Components, Vol. 2011 (2011), Article ID 313580, 10 pages doi:10.1155/2011/313580.

[64]. E. El-Marsy and J. Wu, "Low-voltage micropower log-domain filters", Analog Integrated Circuits and Signal Processing, Vol. 22, pp. 103–114, 2000.

[65]. E. Seevink and R. Wiegerink, "Generalized translinear circuit principle", IEEE Journal of solid state circuits, Vol. 26, pp. 1098–1102, 1991.

[66]. M. Eskiyerli, A. J. Payne, and C. Toumazou, "State-space synthesis of integrators based on the MOSFET square law", Electronics Letters, Vol. 32, pp. 505–506, 1996.

[67]. M. Eskiyerli and A. Payne, "Square-root domain filter design and performance", Analog Integrated Circuits and Signal Processing, Vol. 22, pp. 231–243, 2000.

[68]. J. Mulder et al., "Current-mode companding $\sqrt{x}$ -domain integrator", Electronics Letters, Vol. 32, pp. 198–199, 1996.

[69]. A. J. Lopez-Martin and A. Carlosena, "Geometric-mean based current-mode multiplier/divider", in Proceedings of IEEE International Symposium on Circuits Systems (ISCAS'99), pp. 342–345, 1999.

[70]. A. J. Lopez-Martin and A. Carlosena, "A 3.3 V tunable current-mode square-root domain biquad", In Proceedings of IEEE International symposium on circuits and systems (ISCAS), Geneva, Switzerland, pp. 5–8, 2000.

[71]. , "A systematic approach to the synthesis of square-root domain systems", In Proceedings of IEEE International symposium on circuits and systems (ISCAS), pp. 306–309, 1999.

[72]. A. J. Lopez-Martin and A. Carlosena, "Synthesis of internally nonlinear systems from LTI systems by component-to component substitution and its application to companding", In Proceedings of 42nd IEEE symposium on circuits and systems (MWSCAS) (pp. 976–979), Las Cruces, NM, USA, 1999.

[73]. A. J. Lopez-Martin and A. Carlosena, "Systematic design of companding systems by component substitution", Analog Integrated Circuits and Signal Processing, Vol. 28, pp. 91–106, 2001.

[74]. C. A. De La Cruz-Blas, A. J. Lopez-Martin and A.Carlosena, "1.5 V MOS translinear loops with improved dynamic range and their applications to current-mode signal processing", IEEE Transactions on Circuits and Systems-II, Vol. 50, No. 12, pp. 918–927, 2003.

[75]. C. A. De La Cruz-Blas, A. J. Lopez-Martin and A.Carlosena, "1.5 V square-root domain second-order filter with on-chip tuning", IEEE Transactions on Circuits and Systems-I, Vol. 52, No. 10, pp. 1996–2006, 2005.

[76]. G. J. Yu et al., "Design of square-root domain filters", Analog Integrated Circuits and Signal Processing, Vol. 43, No. 1, pp. 49–59, 2005.

[77]. E. Stoumpou, F. A. Khanday, C. Psychalinos, and N. A. Shah, "A Low-Voltage Square-Root Domain n-th Order Multifunction FLF Filter Topology", Analog Integrated Circuits and Signal Processing, Vol. 61, No. 12, pp. 315-322, June, 2009.

[78]. W. Serdijn et al., "Design of High Dynamic Range Fully Integrable Translinear Filters", Analog Integrated Circuits and Signal Processing, Vol. 19, pp. 223-239, 1999.

[79]. P. Poort et al., "A 1-V class AB translinear integrator for filters applications", Analog Integrated Circuits and Signal Processing, Vol. 21, pp. 79-90, 1999.

[80]. A. Katsiamis, K. Glaros K., E. Drakakis, "Insights and Advances on the Design of CMOS Sinh Companding Filters", IEEE Transactions on Circuits and Systems-I, Vol. 55, pp. 2539-2550, 2008.

[81]. C. Sawigun and W. Serdijn, "Ultra-low power, class-AB, CMOS four quadrant current multiplier, Electronics Letters, Vol. 45, pp. 483-484, 2009.

[82]. C. Kasimis, C. Psychalinos, "0.65 V class-AB current-mode four-quadrant multiplier with reduced power dissipation", International Journal of Electronics and Communications (AEU), Vol. 65, pp. 673-677, 2011.

[83]. E. Pilavaki and C. Psychalinos, "Analog cochlear implant using Sinh-Domain filters", In Proceedings of European Conference on Circuit Theory and Design (ECCTD), pp. 286-289, Aug. 2011.

[84]. C. Kasimis and C. Psychalinos, "Design of Sinh-Domain Filters Using Complementary Operators", International Journal of Circuit Theory and Applications, DOI: 10.1002/cta.769.

[85]. C. Kasimis and C. Psychalinos, "1.2V BiCMOS Sinh-Domain Filters", Circuits Systems and Signal Processing, DOI:10.1007/s00034-011-9379-5.

[86]. L. J. Stotts, "Introduction to Implantable Biomedical", IEEE Circuits and Devices Magazine, pp. 12-18, 1989.

[87]. P. Shoemaker, "A Methodology for Long Time Constant Log-Domain Filters in CMOS", Analog Integrated Circuits and Signal Processing, Vol. 42, pp. 161-178, 2005.

[88]. C. Bartolozzi, S. Mitra and G. Indiveri, "An ultra low power current-mode filter for neuromorphic systems and biomedical signal processing", IEEE, pp. 130-133, 2006.

[89]. Gwo-Jeng Yu, Yu-Jen Tsao and Yu-Shian Lin, "1V Square-Root Domain Low-Pass Filter using Translinear Loop Technology in Biomedical Engineering", Life Science Journal, Vol. 6, No 4, pp. 92-96, 2009.

[90]. F. A. Khanday and N. A. Shah, "An ultra low power Sinh-Domain multifunction filter for neuromorphic systems and biomedical signal processing", International Conference on

Recent Advances in Electronics and Computer Engineering, 17-18 Dec. 2011, Eternal University, Baru Sahib, HP, India.

[91]. F. A. Khanday and N. A. Shah, "Design of low-voltage Sinh-domain multifunction Biquad for low frequency applications", 7th–JK Science Congress, 13-15 October 2011, University of Jammu.

[92]. F. A. Khanday and N. A. Shah, "A Low Voltage and Low Power Sinh-Domain Universal Biquadratic Filter for low frequency Applications". Turkish Journal of Electrical Engineering and Computer Sciences (Turkey), 10.3906/elk-1203-128.

[93]. Andrea Gerosa, Andrea Maniero, and Andrea Neviani, "A Fully Integrated Dual-Channel Log-Domain Programmable Preamplifier and Filter for an Implantable Cardiac Pacemaker", IEEE Transactions on Circuits and Systems—I, Vol. 51, No. 10, pp. 1916-1925, 2004.

[94]. K. I. Papadimitriou and E. M. Drakakis, "CMOS weak-inversion log-domain glycolytic oscillator: a cytomimetic circuit example", International Journal of Circuit Theory and Applications, DOI: 10.1002/cta.1847, 2012.

[95]. W. A. Serdijn et al., "A Low-Voltage Low-Power Fully Integrable Automatic Gain Controll for Hearing Instruments", IEEE Journal of Solid-State Circuits, Vol. 29, No. 8, pp. 943-946, 1994.

[96]. D. Masmoudi et al., "A New Current-Mode Synthesis Method for Dynamic Translinear Filters and its Applications in Hearing Aids", IEEE, pp. 337-340, 1998.

[97]. D. Masmoudi et al., "A New Current-Mode Synthesis Method for Dynamic Translinear Filters and its Applications in Hearing Instruments", Analog Integrated Circuits and Signal Processing, Vol. 22, pp. 221-229, 2000.

[98]. W. Ngamkham et al., "Analog Complex Gammatone Filter for Cochlear Implant Channels", IEEE, pp. 969-972, 2010.

[99]. Qiuting Huang, and Michael Oberle, "A 0.5-mW Passive Telemetry IC for Biomedical Applications", IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, pp. 937-946, 1998.

[100]. A. C. van der Woerd and W. A. Serdijn, "Low-Voltage Low-Power Controllable Preamplifier for Electret Microphones", IEEE Journal of Solid-State Circuits, Vol. 28, No. 10, pp. 1052-1055, 1993.

[101]. W. A. Serdijn et al., "A Low-Voltage Ultra-Low-Power Translinear Integrator for Audio Filter Applications", IEEE Journal of Solid-State Circuits, Vol. 32, No. 4, pp. 577-581, 1997.

[102]. Dominique Python and Christian C. Enz, "A Micropower Class-AB CMOS Log-Domain Filter for DECT Applications", IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, pp. 1067- 1075, 2001.

[103]. C. Psychalinos, "Low-Voltage Log-Domain Complex Filters", IEEE Transactions on Circuits and Systems-I, Vol. 55, No. 11, pp. 3404-3412, 2008.

[104]. F. A. Khanday, "Low-Voltage Square-Root-Domain Complex Filter for Bluetooth/ZigBee Applications", 8th–JK Science Congress, 15-17 September 2012, University of Kashmir.

[105]. J. Misra and I. Saha, "Artificial neural networks in hardware: A survey of two decades of progress", Neurocomputing, Vol. 74, pp. 239–255, 2010.

[106]. G. Indiveri1 et al., "Neuromorphic silicon neuron circuits" Review Article published: Frontiers in Neuroscience, Vol. 5, pp. 1-23, 2011.

[107]. J. Georgiou et al., "An Analogue Micropower Log-Domain Silicon Circuit for the Hodgkin and Huxley Nerve Axon", IEEE, pp. II-286-II-289, 1999.

[108]. T. Serrano-Gotarredona and B. Linares-Barranco, "Log-Domain Implementation of Complex Dynamics Reaction-Diffusion Neural Networks", IEEE Transactions on Neural Networks, Vol. 14, No. 5, pp. 1337-1355, 2003.

[109]. A. van Schaik et al., "A log-domain implementation of the Mihalas-Niebur neuron model", IEEE, pp. 4249- 4252, 2010.

[110]. A. van Schaik et al., "A log-domain implementation of the Izhikevich neuron model", IEEE, pp. 4253- 4256, 2010.

[111]. F. A. Khanday, C. Psychalinos and N. A. Shah, "Square-Root-Domain Realization of Single Cell Architecture of Complex TDCNN," Circuits, Systems and Signal Processing, DOI: 10.1007/s00034-012-9503-1.

[112]. K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation," IEEE J. Solid-State Circuits, Vol. SC-22, pp. 357-365, 1987.

[113]. E. Seevinck, "Synthesis of nonlinear circuits based on the translinear principle," In Proceedings of IEEE International symposium on circuits and systems (ISCAS), pp. 370-373, 1983.

[114]. B. Gilbert, "A new wide-band amplifier technique", IEEE Journal of Solid-State Circuits, Vol. SC-3, pp. 353-365, 1968.

[115]. B. Gilbert, "A precise four-quadrant multiplier with sub-nano second response," IEEE Journal of Solid-State Circuits, Vol. SC-3, pp. 365-373, 1968.

[116]. E. Seevinck and G. H. Renkema, "A 4-quadrant cosine-synthesis circuit," in ISSCC Dig. Tech. Papers, pp. 40-41, 1982.

[117]. R. F. Wassenaar et al., "New techniques for high-frequency rms-to-dc conversion based on a multifunctional V-to-I converter," IEEE Journal of Solid-state Circuits, Vol. 23, pp. 802-815, 1988.

[118]. E. Seevinck, W. de Jager, and P. Buitendijk, "A low-distortion output stage with improved stability for monolithic power amplifiers," IEEE Journal of Solid-State Circuits, Vol. 23, pp. 794-801, 1988.

[119]. Shih-Chii Liu et al., "Analog VLSI: Circuits and Principles", A Bradford Book: The MIT Press Cambridge, Massachusetts London, England, pp. 187-188, 2002.

[120]. N. Pandey, S. Paul and S. Jain, "A new electronically tunable current mode universal filter using MO-CCCII", Analog Integrated Circuits and Signal Processing, Vol. 58, pp. 171–178, 2009.

[121]. S. Minaei, "Electronically tunable current-mode universal biquad filter using dual-X current conveyors", Journal of Circuits, Systems and Computers, Vol. 18, pp. 665–680, 2009.

[122]. R. Saad and A. Soliman, "On the systematic synthesis of CCII-based floating simulators", International Journal of Circuit Theory and Applications, Vol. 38, pp. 935–967, 2010.

[123]. C. Laoudias and C. Psychalinos, "Universal biquad filter topology using low-voltage current mirrors", International Journal of Circuit Theory and Applications, DOI: 10.1002/cta.706.

[124]. B. Metin, K. Pal and O. Cicekoglu, "All-pass filters using DDCC- and MOSFET-based electronic resistor", International Journal of Circuit Theory and Applications, DOI: 10.1002/cta.682.

[125]. M. Ibrahim, S. Minaei and E.Yuce, "All-pass sections with rich cascadability and IC realization suitability", International Journal of Circuit Theory and Applications, DOI: 10.1002/cta.738.

[126]. Y. Tsividis, "On linear integrators and differentiators using instantaneous companding", IEEE Transaction on Circuits and Systems-II, Vol. 42, pp. 561–564, 1995.

[127]. N. Kontogiannopoulos and C. Psychalinos, "Log-domain filtering by simulating the topology of passive prototypes", IEEE Transaction on Circuits and Systems-I, Vol. 52, pp. 2043–2054, 2005.

[128]. C. Psychalinos and S. Vlassis, "A systematic design procedure for square-root domain circuits based on the signal flow graph approach", IEEE Transaction on Circuits and Systems-I, Vol. 49, pp. 1702–1712, 2002.

[129]. C. Psychalinos, "Design of square-root domain filters by substituting the passive elements of the prototype filter by their equivalents", International Journal of Circuit Theory and Applications, Vol. 36, pp. 185–204, 2008.

[130]. E. Stoumpou and C. Psychalinos, "Square root domain linear transformation filters", International Journal of Circuit Theory and Applications, Vol. 39, pp. 719-731, 2011.

[131]. D. Frey, "Exponential state-space filters: a generic current mode design strategy", IEEE Transaction on Circuits and Systems-I, Vol. 43, pp. 34–42, 1996.

[132]. A. Lopez-Martin and A. Carlosena, "Synthesis of sinh systems from Gm-C systems by component to component substitution", Proceedings of the 42nd Midwest Symposium on Circuits and Systems (MWSCAS), Las Cruses NM,U.S.A., pp.287–290, 1999.

[133]. D. R. Frey, "Log-domain filtering for RF applications". IEEE Journal of Solid State Circuits, Vol. 31, No. 10, pp. 1468–1475, 1996.

[134]. G. J. Yuet al., "A low-voltage low-power log-domain band-pass filter, In Proceedings of the IEEE International Symposium on VLSI Technology, Systems and Applications, pp. 219–222, 2003.

[135]. R. Wiegerink, "Analysis and synthesis of MOS translinear circuits", Dordrecht, The Netherlands: Kluwer Academic Publishers Group; pp, 246, 176, 1993.

[136]. A. J, Lopez-Martin and A. Carlosena, "1.5V CMOS companding filter", Electronics Letters, Vol. 38, pp. 1346-1348, 2002.

[137]. C. Psychalinos, "Square-root domain wave filters", International Journal of Circuit Theory and Applications, Vol. 35, No. 2, pp. 131-148, 2007.

[138]. C. Psychalinos, "Square-root domain operational simulation of LC ladder elliptic filters", Journal of Circuits, Systems and Signal Processing, Vol. 26, No. 2, pp.263-280, 2007.

[139]. C. Laoudias, C. Psychalinos and E. Stoumpou, "1.5V square-root domain universal biquad filters", International Journal of Circuit Theory and Applications, DOI: 10.1002/cta.802.

[140]. C. A. De La Cruz-Blas, A. J. Lopez-Martin and A. Carlosena, "Low-voltage nonlinear CMOS transconductors and their application to companding current-mode filters", Analog Integrated Circuits and Signal Processing, Vol. 38, pp. 137–147, 2004.

[141]. C. A. De La Cruz-Blas, A. J. Lopez-Martin and A. Carlosena, "1.5V tunable square root domain filter", Electronics Letters, Vol. 40, pp. 213–214, 2004.

[142]. C. Psychalinos and S. Vlassis, "On the exact realization of log-domain elliptic filters using the signal flow graph approach", IEEE Transaction on Circuits and Systems-II, Vol. 49, pp. 770–774, 2002.

[143]. S. Liu and Y. Liao "Table-based log-domain linear transformation filter", Electronics Letters, Vol.32, pp. 1771–1772, 1996.

[144]. R. Schaumann and M. E. Van Valkenburg, "Design of analog filters", New York: Oxford university press, 2001.

[145]. Kendall Su, "Analog Filters", Kluwer Academic Publishers, New York, Boston, Dordrecht, London, Moscow, Second Edition, 2003.

[146]. L. D. Paarmann, "Design and analysis of analog filters", a signal processing perspective, Kluwer Academic Publishers, 2001.

[147]. C. Psychalinos, "Log-domain SIMO and MISO low-voltage universal biquads", Analog Integrated Circuits and Signal Processing, Vol. 67, pp. 201-211, 2011.

[148]. E. Niedermeyer, F. Lopes da Silva, "Electroencephalography", Williams & Wilkins, Baltimore, MD, pp. 1258, 4th Edition, 1999.

[149]. M. Hamalainen et al, "Magneto-encephalography-Theory, instrumentation, and applications to noninvasive studies of the working human brain", Rev. Mod. Phys., Vol. 65, pp. 413-497, 1993.

[150]. J. L. Andreassi, "Psychophysiology: human behavior and physiological response", New Jersey: Lawrence Erlbaum Associates, 5th Edition, 2007.

[151]. E. D. C. Cotrim and L. H. de Carvalho Ferreira, "An ultra-low-power CMOS symmetrical OTA for low-frequency Gm-C applications", Analog Integrated Circuits and Signal Processing, Vol. 71, pp. 275–282, 2012.

[152]. A. S. Sedra, "Filter theory and design: Active and passive", Portland: Matrix publishers, pp. 23-35, 1978.

[153]. S. A. Boctor, "A novel second-order canonical RC-active realization of high-pass notch filter", IEEE Transaction on Circuits and Systems , Vol. 22(5), pp. 397-404, 1975.

[154]. S. A. Boctor, "Single amplifier functionally tunable Low-pass notch filter", IEEE Transaction on Circuits Systems, Vol. 22(11), pp. 875-881, 1975.

[155]. A. J. Lopez-Martin and A., Carlosena, "Very low voltage MOS translinear loops based on flipped voltage followers", Analog Integrated Circuits and Signal Processing, 2004, 40, 71-74.