Simulation of FinFET Structures

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By

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Under the Guidance of

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C E R T I F I C A T E

This is to certify that the scholar, Mr. Tawseef Ahmad Bhat, has carried out the work embodied in this dissertation entitled *"Simulation of FinFET Structures"* under my supervision. The work presented herewith is suitable for the award of Degree of Master of Philosophy in Electronics. The dissertation has not been submitted elsewhere for M. Phil. or any other degree.

Prof. M. Mustafa

Date: (Supervisor)

.....dedicated to my parents

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Contents

Chapter 1
Introduction

1.1. Preamble:

The intensive downscaling of MOS transistors has been the major driving force behind the aggressive increases in transistor density and performance, leading to more chip functionality at higher speeds. While on the other side the reduction in MOSFET dimensions leads to the close proximity between source and drain, which in turn reduces the ability of the gate electrode to control the potential distribution and current flow in the channel region and also results in some undesirable effects called the short-channel effects. These limitations associated with downscaling of MOSFET device geometries have lead device designers and researchers to number of innovative techniques which include the use of different device structures, different channel materials, different gate-oxide materials, different processes such as shallow trench isolation, source/drain silicidation, lightly doped extensions etc. to enable controlled device scaling to smaller dimensions. A lot of research and development works have been done in these and related fields and more remains to be carried out in order to exploit these devices for the wider applications.

It is worthwhile to mention here that every year, the International Technology Roadmap for Semiconductors (ITRS) [1] issues a report that serves as a benchmark for the semiconductor industry. These reports describe the type of technology, design tools, equipment and metrology tools that have to be developed in order to keep pace with the exponential progress of semiconductor devices predicted by Moore's law. Further, to keep up with the frantic pace imposed by Moore's law, the linear dimensions of transistors have reduced by half every three years.

The continuous scaling down of MOSFET devices has lead to various short channel effects such as Sub-threshold Slope (SS) degradation, Drain Induced Barrier Lowering (DIBL) effect, threshold voltage roll-off. It is because as the dimensions of transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the "short-channel effects (SCE's)" start plaguing MOSFETs. For all practical purposes, it seems impossible to scale the dimensions of classical "bulk" MOSFETs below 20nm due to various SCE's that impinge the device characteristics [2].

Scaled planar bulk MOSFETs and PDSOI MOSFETs rely on gate oxide thickness reduction and higher channel doping to avoid SCE's, but the use of a thinner gate oxide increases the gate-to-channel capacitance and direct tunnelling current through the gate dielectric prevents further scaling of the gate oxide thickness. The use of high channel doping concentrations reduces carrier mobility and increases Gate Induced Drain Leakage (GIDL). Furthermore at higher channel doping, due to randomness and discrete nature of dopant atoms, the same macroscopic doping profiles differ microscopically. For devices with minimized geometry, both the fluctuation in the number of channel dopants and their placement may cause significant device-to-device performance variation [3].

Strained channel devices have also been used to boost the carrier mobility and performance of CMOS even at aggressively scaled channel lengths, wherein the mechanical stress is developed by the insertion of a foreign atom in the silicon such as germanium, changing the original lattice parameter. Besides strained devices increasing the drive current due to higher mobility, the material band gap, E_g is affected by stress that modifies the energy levels. This variation changes directly the intrinsic carrier concentration and Fermi level resulting in the threshold voltage that in general is smaller as that in unstrained devices [4].

Efforts are on to have a high-k gate dielectric. But this "high-k gate dielectric" search is not a simple effort. It has mostly yielded materials with poor thermal stability and/or a large number of interface traps when used with silicon. While some high-k dielectrics such as Ta_2O_5, ZrO_2, etc have been found to have good thermal stability, they have other problems such as an undesirable band alignment with respect to silicon's band gap, in a way that worsens the gate direct-tunneling current. While there have been some commendable successes involving the conventional planar MOSFET it is felt to be a difficult task nevertheless to continue with the conventional planar MOSFET at future technology nodes[5].

The first integrated circuit transistors were fabricated on "bulk" silicon wafers. At the end of 1990, it became apparent that significant improvements can be gained by switching to a new type of substrate, called SOI (Silicon-On-Insulator) in which the transistors are made in a thin silicon wafer sitting on top of silicon dioxide layer. SOI technology brings about improvements in both circuit speed and power consumption. In the early 2000's major semiconductor companies, including IBM, AMD and Freescale,

began manufacturing microprocessors using SOI substrates on an industrial scale. SOI devices offer advantage of reduced parasitic capacitances and enhanced current drive [2].

In a continuous effort to eliminate the more critical SCE's, conventional single gate transistors were replaced by the more efficient structural variant, Multiple Gate Field Effect transistors (MuGFETs). These devices utilize two or more gate electrodes and an ultra thin, fully depleted semiconductor body [2]. MuGFETs are the best promising device structures that outperform the conventional single gate transistors by providing near ideal sub-threshold slope, higher transconductance and minimized short-channel effects. Hisamoto et al. introduced the DELTA fully DEpleted Lean-channel TrAnsistor in 1989 [6], [7] which is the first fabricated double gate SOI MOSFET after T. Sekigawa and Y. Hayashi published the first article on double gate MOS (DGMOS) transistor in 1984. FinFET, which is considered as the most viable implementation of the MuGFET structure for controlling SCE's, evolved from the same DELTA structure and is widely open for research and development in order to follow the Moore's law and ITRS roadmap for the future generations. FinFET based circuits have been demonstrated in many IC's such as digital logic, SRAM, DRAM and flash memories [8], [9].

1.2. FinFET Basic Structure:

The term FinFET was coined by University of California, Berkeley researchers (Profs. Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor) to describe a non-planar, double-gate transistor built on an SOI substrate. In spite of its double-gate structure, the FinFET is close to its root, the conventional MOSFET in layout and fabrication [10]. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The gate actually covers the silicon fin or body along its three sides: the top side and the two lateral sides. The top channel is more or less deactivated by using a thicker oxide or nitride, leading to a double-gate (DG-FinFET) or a triple-gate (TG-FinFET) structure. The basic three dimensional schematic structure of FinFET is as shown in Fig. 1.1.

FinFET is called so because its structure contains the ultra-thin vertical channel that resembles with the fins of a fish, surrounded by gate along its three sides. In the given FinFET structure, TiN is the metal gate, SiO_2 + HfO_2 is used as oxide gate stack and the fin body is usually made of silicon which acts as channel. Various geometrical parameters of FinFET as specified in Fig. 1.1 are transistor channel length or gate length,

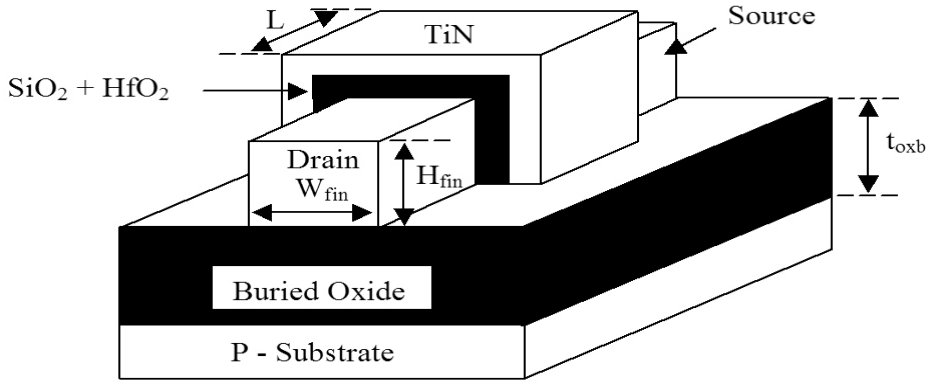


Fig. 1.1. Schematic representation of a FinFET indicating the main

(L), Equivalent Oxide Thickness (EOT), fin height (H_{fin}), buried oxide thickness (t_{oxb}), fin width (W_{fin}) of the device. In case of triple gate FinFET, fin width is also referred as fin thickness (T_{fin}). Gate length is the main device parameter for various technology nodes. Surrounded gate FinFETs with sub 5nm gate length have been reported to be fully functional [11], [12]. It is worthwhile to mention that device width or electrical width 'W' of a FinFET is taken as '2 H_{fin}+W_{fin}'. 'W' as defined is indeed the width of the gate region that is in touch with (i.e, in control of) the channel in the fin (albeit with a dielectric in between), applies for a triple gate FinFET. If the top gate of the device is not present or its effect is deactivated by using a thick oxide at the top surface of fin, then the term W_{fin} is not included in the definition for device width. The advantage of increasing the fin height instead of fin width W_{fin} is that one can increase the effective channel width without increasing the planar area to increase the device on-current, but not beyond some limits as it can prove detrimental for various short channel effects SCEs [13],[14]. Thus area efficiency is maximised as compared to conventional SOI or bulk devices. The etched fin needs to be narrow for good control of the channel potential by the gate, and at the same time high quality of the etched surfaces is needed to reduce surface scattering. Furthermore, the value of parasitic gate resistance and capacitances depend on the geometry of the structure, namely, number of fins, fin-height and fin spacing, and when the total device width is divided over several fins, the FinFET with the channel width distributed over the smaller number of taller fins will have lower parasitics and better frequency-performance than the one with a larger number of shorter fins [15].

In current usage the term FinFET has a less precise definition. Among microprocessor manufacturers, AMD, IBM, and Motorola describe their double-gate development

efforts as FinFET development whereas Intel avoids using the term to describe their closely related tri-gate architecture [16]. In the technical literature, FinFET is used somewhat generically to describe any fin-based, multigate transistor architecture regardless of number of gates.

1.3. Multiple-Gate MOSFET Structures, A Brief Review:

Multiple-Gate MOSFET structures provide potential advantages such as higher integration density, lower short-channel effect and near ideal subthreshold slope. It has become possible to increase the dive current in these non-planar MOSFET structures while at the same time scaling down the device dimensions well below in the nanometre regime. Silicon-on-Insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (double-, triple- or quadruple- gate devices). It is worth noting that, in most cases, the term “double gate”

Table 1.1. Device names found in the literature [2].

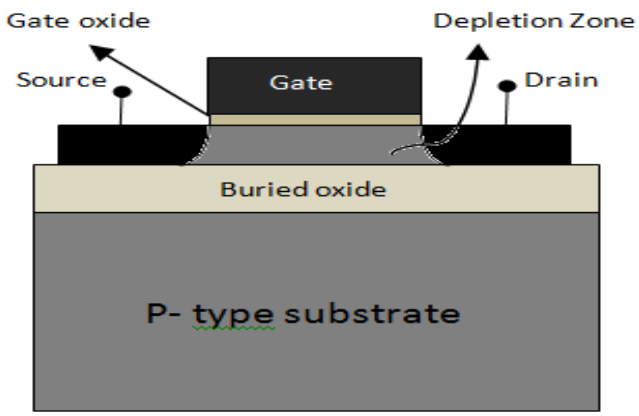
Acronym	Also known as
MuGFET (Multiple-Gate FET)	Multi-gate FET, Multigate FET
MIGFET (Multiple Independent Gate FET)	Four-terminal (4T) FinFET
Triple-gate FET	Trigate FET
Quadruple-gate FET	Wrapped-Around Gate FET Gate-All-Around FET Surrounding-Gate FET
FinFET	DELTA (fully DEpleted Lean channel TrAnsistor)
FDSOI (Fully Depleted SOI)	Depleted Silicon Substrate
PDSOI (Partially depleted SOI)	Non-Fully Depleted SOI
Volume Inversion	Bulk Inversion
DTMOS (Dual Threshold Voltage MOS)	VTMOS (Varied Threshold MOS) MTCMOS (Multiple Threshold CMOS) VCBM (Voltage-Controlled Bipolar MOS) Hybrid Bipolar-MOS Device

refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term “triple gate” is used for a single gate electrode that is folded over three sides of the transistor. One remarkable exception is the MIGFET (Multiple

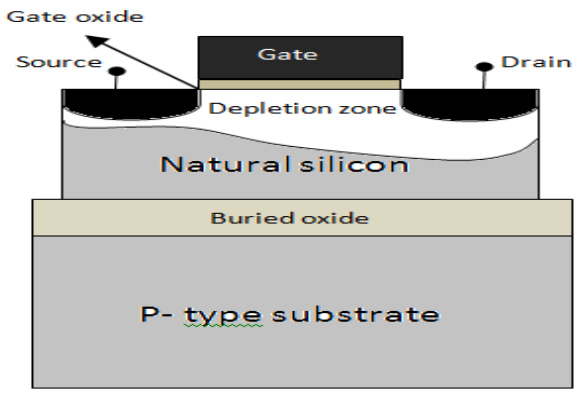
Independent Gate FET) where two separate gate electrodes can be biased with different potentials. It is also worth pointing out that one device may have several different names in the literature (Table 1.1).

1.3.1. Single-Gate SOI MOSFET Structure:

In silicon on insulator (SOI) technology, MOSFETs are realized in a thin layer of silicon sitting on top of an insulator, usually SiO_2, called "buried oxide". The thickness of silicon film typically ranges between 50 and 200nm, while the buried oxide thickness usually ranges between 80 and 400nm. If the silicon film is thin enough the depletion zone below the gate extends all the way through the buried oxide, and the device is said to be "fully depleted" (Fig. 1.2 A). If this is not the case the transistor is "partially depleted" (Fig. 1.2 B) [17].



(A)



(B)

Fig. 1.2. (A) Fully Depleted SOI MOSFET; (B) Partially Depleted MOSFET

The first SOI transistor dates back to 1964. These were partially depleted devices fabricated on silicon-on-sapphire (SOS) substrates [18],[36]. SOS technology was successfully used for numerous military and civilian applications [19] and is still being used to realize commercial HF circuits in fully depleted CMOS [20–22]. Once the first SOI substrates (the insulator is now silicon dioxide) were available for experimental MOS device fabrication, partially depleted technology the natural choice derived from SOS experience. Partially depleted CMOS continues to be used nowadays and several commercial IC manufacturers have SOI products and product lines such as high performance microprocessors and memory chips. The low-voltage performance of PDSOI devices can be enhanced by creating a contact between the gate electrode and the floating body of the device. Such a contact improves the subthreshold slope, body factor and current drive, but limits the device operation to sub-1V supply voltages [23-31]. Fully depleted SOI devices have a better electrostatic coupling between the gate and the channel. This results in a better linearity, subthreshold slope, body coefficient and current drive. FDSOI technology is used in a number of applications ranging from low-voltage, low-power to RF integrated circuits [2].

1.3.2. Double-Gate SOI MOSFET Structure:

Double gate MOSFETs are ideal devices for electrostatic integrity and ultimate scaling of MOSFET structures well below in the nanometre regime. The front and back inversion of channel induce volume inversion which brings enhanced drain current and transconductance. The total inversion charge in double gate MOSFET structure is twice the inversion charge in single gate mode. The subthreshold slope is more ideal, 60mV/dec at room temperature. The essential point is that the minority carriers flow in the middle of the fin and experience less surface scattering effect, hence improving mobility [78]. The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi 1984 [32]. That paper shows that one can obtain significant reduction of short-channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (Xi). Using this configuration, a better control of the channel depletion region is obtained than in a “regular” SOI MOSFET, and, in particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel [33]. As mentioned earlier in this chapter, the first fabricated double-gate SOI MOSFET was the “fully Depleted Lean-channel TrAnsistor

(DELTA, 1989)" [6], where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin" (Fig. 1.3). The DELTA gate effectively controls the channel potential from both sides and induces ultra thin SOI effects vertically. DELTA is excellent for ULSI applications. No Isolation area is necessary because DELTA is isolated vertically. The DELTA structure uses vertical surface for current conduction. Still the current direction is the same as that for a conventional planar-MOSFET device. Thus DELTA offers both consistency with conventional MOSFETs and good scalability as a 3-D device [6]. The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin [34-38]. The hard mask is used to prevent the formation of parasitic inversion channels at the top corners of the device.

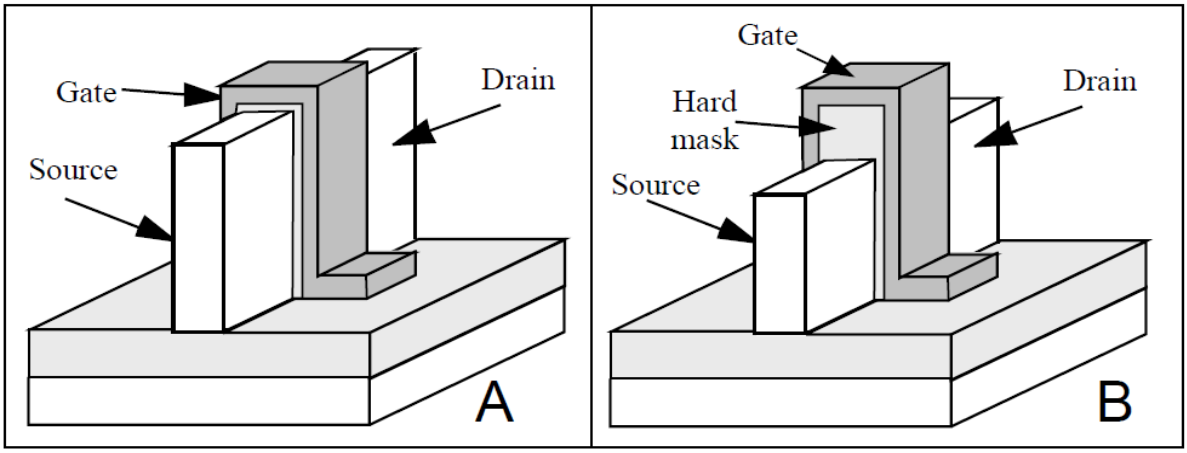


Fig. 1.3. Examples of double-gate MOS structure: (A) DELTA MOSFET, (B): FinFET [2].

Other implementations of vertical-channel, double-gate SOI MOSFETs include the "Gate-All-Around device" (GAA) [39], the Silicon-On-Nothing (SON) MOSFET [42-44], the Multi-Fin XMOS (MFXMOS) [45], the triangular-wire SOI MOSFET [46] and the Δ-channel SOI MOSFET [47].

The GAAC FinFET is a planar MOSFET with the gate electrode wrapped around the channel region. The GAAC FinFET device provides the best gate electric field control as it has a virtually "infinite" number of gates, with all gates in close proximity to the channel and enhanced electrostatic control from the gate electrode over the charge carriers in the channel [40]. Silicon-on-nothing (SON) technology has been proposed as an alternative solution for advanced scaling. It combines the advantages of FD-

MOSFETs (excellent subthreshold slope and mobility, no floating-body effects, and other) with those of bulk silicon (lower series resistances and better heat dissipation). In addition, SON provides a good control of the silicon film thickness, fringing fields, and halo profiles which are basic ingredients for advanced scalability [41]. Ultranarrow and ideal rectangular cross section silicon(Si)-Fin channel double-gate MOSFETs (FXMOSFETs) have successfully been fabricated for the first time in [45] using [110]-oriented silicon-on-insulator (SOI) wafers and orientation-dependent wet etching. In that paper, the experimental results have shown transconductance as high as 700µs/µm, almost ideal subthreshold swing, 64mV/dec and an effective suppression of short channel effects. The Si-Fin channel with smooth [111]-oriented sidewalls has been found suitable to realize a high-performance FXMOSFET. Nano-scale silicon MOSFETs with narrow wire channels on SOI substrates have been presented in [46]. It has been mentioned that the triangular wire MOSFET can suppress the short channel effect more than conventional single-gate SOI MOSFETs. Furthermore the wire-channel MOSFETs narrower than 10 nm exhibit quantum confinement effects at room temperature. The MIGFET (Multiple Independent Gate FET) is a double-gate device in which the two gate electrodes are not connected together and can, therefore, be biased independently with different potentials [48-52]. The main feature of the MIGFET is that the threshold voltage of one of the gates can be modulated by the bias applied to the other gate [2]. A novel application using MIGFET is signal modulation. A simple square law mixer can be formed using a single MIGFET. This MIGFET signal modulation circuit reduces transistor counts and rail-to-rail transistor stack, making it possible to design compact low power mixers.

1.3.3. Triple-Gate SOI MOSFET Structure:

In order to maximize on-currents per chip area, multi-gate structures with non-planar gates such as FinFET or triple-gate transistors are favourable. The continuous reduction of buried oxide (BOX) thickness to reduce the total amount of buried oxide charges and to increase heat dissipation leads to a substantial influence of substrate bias on the subthreshold behavior. Triple-gate MOSFETs can strongly reduce this effect. The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides (Fig. 1.4). [53] Implementations include the quantum-wire SOI MOSFET [54-55] and the trigate MOSFET [56-57]. The Electrostatic Integrity of triple-gate MOSFETs can be improved by extending the sidewall portions of the gate electrode to some depth in the

buried oxide and underneath the channel region (Π-gate device [58-59] and Ω-gate device [60-62]). The cross-sectional view of Ω-Gate and Π-Gate MOSFT structures is as shown in Fig. 1.5. From an electrostatic point of view, the Π- gate and Ω-gate MOSFETs have an effective number of gates between three and four. The Π- gate device is simple to manufacture and offers electrical characteristics similar to the much harder to fabricate gate-all-around MOSFET. Omega gate (Ω-gate) MOSFETs can achieve area efficiency by utilising taller fins. Low leakage and low active-power 25 nm gate length CMOSFETs have been demonstrated for the first time with a newly proposed Omega-(Ω) shaped structure, at a conservative 17-19°A gate oxide thickness, and with excellent hot carrier immunity [60]. Further the use of strained silicon, a metal gate and/or high-k dielectric as gate insulator can further enhance the current drive of the device [63-66], [2].

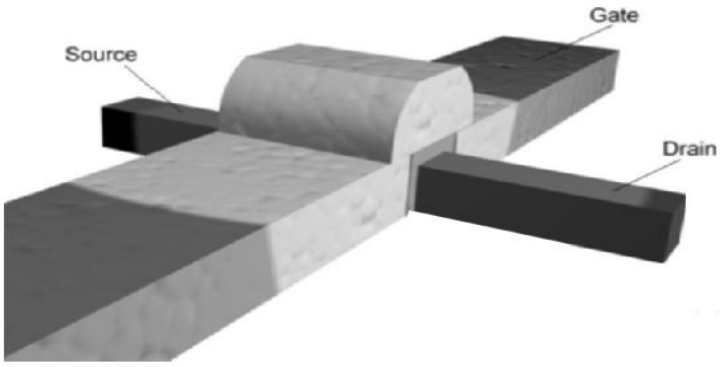


Fig. 1.4. Triple-gate MOSFET [2].

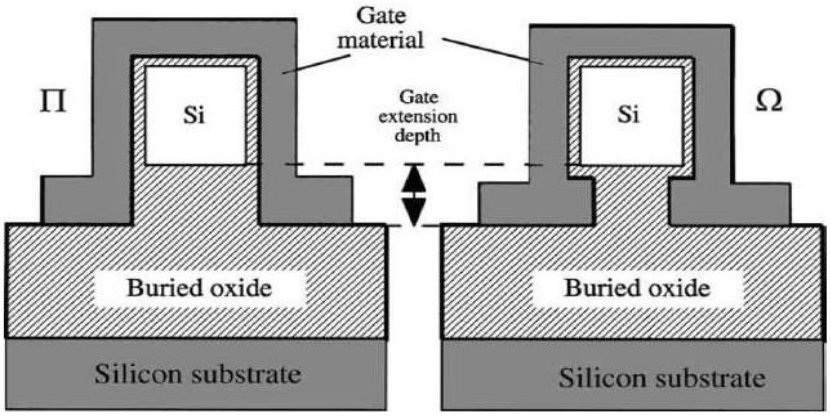


Fig. 1.5. Cross-sectional view of Ω-Gate and Π-Gate MOSFT structures [67].

1.3.4. Surrounding-Gate (Quadruple-Gate) SOI MOSFETs:

Among various MuGFET device structures, the structure that theoretically offers the best possible control of the channel region by the gate, and hence the best possible

Electrostatic Integrity (EI) is the surrounding-gate MOSFET (Fig. 1.6). The first surrounding-gate MOSFETs were fabricated by wrapping a gate electrode around a vertical silicon pillar. This difference in device geometry not only increases the packing density but also leads to better control of gate over the channel potential which in turn results in improved subthreshold characteristics and greater short channel immunity as compared to the single and double gate structures. Such devices include the CYNTHIA device (circular-section device) [68-69] and the pillar surrounding-gate MOSFET (square-section device) [70]. The device characteristics of cylindrical thin-pillar transistor (CYNTHIA) have been calculated in [68] by solving Poisson's equation in cylindrical coordinates. Results obtained have shown that CYNTHIA has three superior features: excellent subthreshold characteristics, enhanced electron mobility, and increased sheet electron concentration. Further it has been mentioned that CYNTHIA is quite an attractive device design for future ultra-high-density LSI's.

The Multi-pillar surrounding gate transistor (M-SGT) has a three-dimensional structure, which consists of the source, gate, and drain arranged vertically. The gate electrode surrounds the crowded multipillar silicon islands. Because all the sidewalls of the pillars are used effectively as the transistor channel, the M-SGT has a high-shrinkage feature. The area occupied by the M-SGT can be shrunk to less than 30% of that occupied by the planar transistor. The small occupied area and the mesh-structured gate electrode lead to the small junction capacitance and the small gate electrode RC delay, resulting in high-speed operation [70].

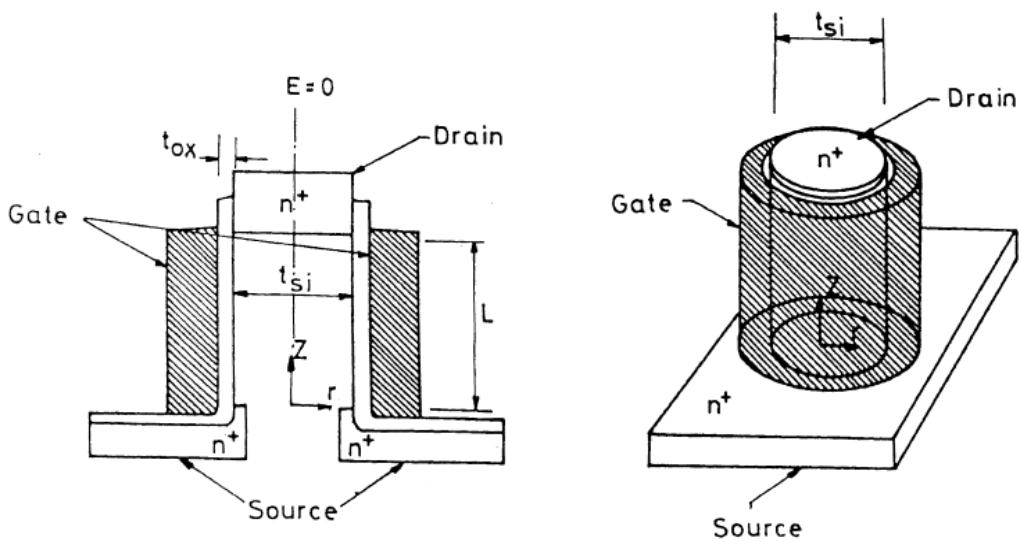


Fig. 1.6. Schematic diagram of a Cylindrical/Surrounding gate MOSFET along with various physical dimensions [77].

More recently, planar surrounding-gate devices with square or circular cross sections have reported [71-72]. To increase the current drive per unit area, multiple surrounding-gate channels can be stacked on top of one another, while sharing common gate, source and drain. Such devices are called the Multi-Bridge Channel MOSFET (MBCFET) [73-74], the Twin-Silicon-Nanowire MOSFET (TSNWFET) [75], or the Nano-Beam Stacked Channels (GAA) MOSFET [76].

1.3.5. Other Multigate MOSFET Structures:

The Inverted T-channel FET (ITFET) combines a thin-film planar SOI device with a trigate transistor (Fig. 1.7A) [79-80]. It comprises planar horizontal channels and vertical channels in a single device. The devices have multi-gate control around these channels. The Inverted T-gate structure has several advantages: the large base helps the fins from falling over during processing; it also allows for transistor action in the space between the fins, which is left unused in other MuGFET configurations. These additional channels increase the current drive. Numerical simulation of an N-channel ITFET reveals different turn-on mechanisms in different parts of the device. The corners of the device turn on first, immediately followed by the surface of the planar regions and the vertical channel. Since each ITFET has about seven corner elements they constitute a significant current to each ITFET device and in a well-designed device can yield substantially more current than a planar device of equivalent area [2].

Due to the fact that SOI wafers have higher wafer cost and higher defect density than bulk Si wafers as well as heat transfer issues, Body-tied double-gate MOSFETs at nanometer scale have been demonstrated and fabricated for the first time in [81]. Implementation of double gate transistors on bulk silicon wafers has been found to be cost effective, while keeping the excellent scalability and performance of SOI double-gate devices. The bulk FinFET is a FinFET made on bulk silicon instead of an SOI wafer. Fins are etched on a bulk silicon wafer and trimmed using an oxidation step. Field oxide is deposited to avoid inversion between the fins (Figure 1.7 B). The smallest bulk-FinFET with 6 nm fin width and with 20nm gate length is demonstrated for the first time. An operational six-transistor SRAM cell has been experimentally demonstrated using bulk FinFET CMOS technology. A cell size of 0.79 μm^2 was achieved in 90 nm technology node, with stable operation at 1.2 V. Static noise margin of 280 mV was obtained at Vcc of 1.2 V [82].

The multi-channel Field Effect Transistor (McFET) is a modified bulk FinFET where a trench is etched in the centre of the fin [83]. The trench is filled by the growth of a gate oxide and the deposition of gate material. This process produces a device having two very thin "twin" fins running from source to drain (Figure 1.7 C).

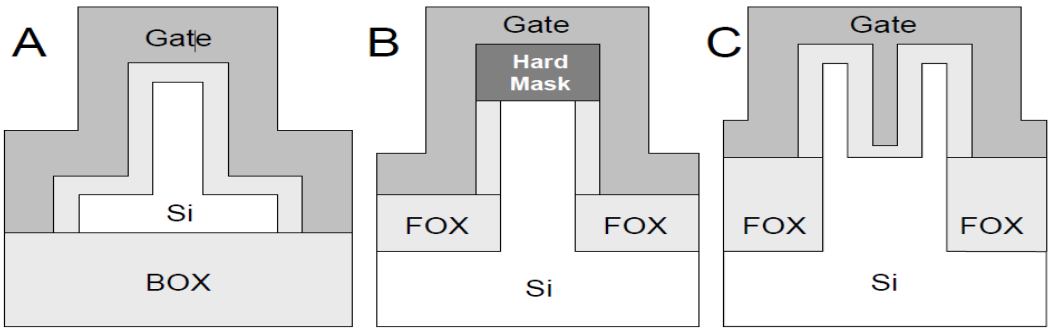


Fig. 1.7. Cross section of (A): Inverted T channel FET; (B): Bulk FinFET; (C): Multichannel Field Effect Transistor. [2]

A novel SRAM cell array McFET was successfully fabricated using highly manufacturable conventional CMOS process in [84]. It has been realized that the McFET is highly effective to utilize the active area, overcoming the lithographical patterning limit. Using McFET structure, drive current was increased 5~6 times with excellent short channel immunity.

1.4. FinFET Technology:

In the past, process complexity posed a serious technological barrier to the development of double-gate devices. In order to improve the very critical short channel effect immunities in the nanoscale MOSFET structures, Hisamoto et. al. proposed a novel "Folded Channel Transistor" structure in the deep-sub-tenth micron regime [85]. The quasi-planar nature of this new variant of the vertical double-gate SOI MOSFET simplified the fabrication process. The special features of the structure are: (1) a transistor is formed in a vertical ultra-thin Si fin and is controlled by a double-gate, which suppresses short channel effects; (2) the two gates are self-aligned and are aligned to the S/D; (3) S/D is raised to reduce the parasitic resistance; (4) new low-temperature gate or ultra-thin gate dielectric materials can be used because they are deposited after the S/D; and (5) the structure is quasi-planar because the Si fins are relatively short. In this structure silicon fins were patterned and etched using 100 keV Electron Beam

lithography and ashing technique. The process demonstrated by Hisamoto et al. yielded n-channel devices with promising performance and scalability.

A self-aligned double gate (SOI) structure scalable to 20 nm gate length has been experimentally demonstrated in [35] using the similar fabrication process flow as described in [85]. The structure can effectively suppress SCE's even with 17-nm gate length. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, desired threshold voltage was achieved for ultrathin body device. The advantages of SiGe gate are the compatibility with poly-silicon gate process and the continuous variability of work function controlled with the germanium concentration. Furthermore the double-gates are self-aligned to each other and to the Source/Drain. Self- alignment is good for reducing the parasitic capacitance and resistance and for control of channel length. The self-aligned process and quasi-planar structure of FinFET are suitable to construct multi-fin transistor for larger channel width.

A simplified fabrication process for sub-60nm FinFET has been demonstrated in [86]. A double-resist process is used to define fins and large-area parameters simultaneously. 250 nm optical G-line resist is patterned first and hard baked at $170^{o}C$; 200nm SAL-601 is subsequently coated and patterned using e-beam exposure providing critical fin dimensions down to 30nm. The two resist patterns are then transferred to the SOI with a single reactive ion etch (RIE). After the silicon fins are etched, 2.5nm sacrificial oxide is grown and removed to improve the fin sidewall surface prior to gate oxidation without seriously undercutting the buried oxide. The Si_xGe_{1-x} composition gate on 1.8 nm SiO_2 layer is chosen to provide the desired threshold voltage. The fabrication process results in lower gate-to-drain capacitance with excellent drive current and limited SCE's down to 50 nm gate length.

A double-gate FinFET with gate length down to 10nm has been fabricated and experimentally demonstrated for scalability and potential performance benefits in [178]. During the experiment, the FinFETs have been fabricated on bonded SOI wafers with a modified planar CMOS process. Although the modified planar CMOS process has added process complexity to the existing planar process but the devices fabricated through such a process resulted in FinFETs that would be strong competitor or successor to classical CMOS. Dual doped (n+/p+) poly-Si gates doped by ion implantations and subsequently activated with RTA have been used as gate electrodes. 193 nm and 248 nm wavelength optical lithography have been used to pattern the Si fin and the gate, respectively. A pattern reduction technique which is able to produce both fin width and gate length down

to sub-10nm dimensions has been utilised. A nitrided-oxide with 17 ^{o}A physical thickness has been used as the gate insulator. Other process features include low-temperature source/drain annealing, NiSi, and Cu metalization. Furthermore the CMOS FinFET inverters (built from multiple-fin transistors) have been fabricated and demonstrated.

For the FinFET, short-channel effects can be suppressed by employing a body thickness which is approximately half of gate length L_g . This is clearly impossible to accomplish with standard lithography technologies when L_g is at the limit of lithography. E-beam lithography has produced 15 nm gates and extreme-ultra-violet (EUV) lithography has generated 38 nm period patterns. But the throughput of e-beam lithography is too low for even research and its uniformity is not yet satisfactory for deep sub-tenth micron gate length fabrication, and EUV lithography is not readily available yet. The uniformity of silicon fin width is especially critical for the FinFET because variation in fin width (W_{fin}) can cause a change in channel potential and sub-bands structures, which governs short-channel behaviour and quantum confinement effects of inversion charges. Further small change of fin width results in large variation of device characteristics for the short gate lengths. Taller silicon fin is desirable because it provides a large channel width. A high fin density is also required to obtain large transistor drive current with good layout area efficiency. Spacer lithography process technology is attractive for overcoming the limits of conventional lithography techniques in terms of pattern fidelity and pattern density. The spacer lithography technology demonstrated in [87] can produce extremely narrow and uniform fin widths. Silicon fin widths down to 6.5nm have been successfully achieved. Sub-60 nm CMOS FinFETs are demonstrated for the first time and show excellent short-channel behaviour. Spacer lithography technology provides for a doubling of fin density, which doubles the drive current for a given lithography pitch. An extremely narrow fin width, beyond the lithographic limit, as well as very uniform fin width can therefore be obtained with this spacer lithography process.

Several critical issues of the FinFET: the effect of the fin size, the influence of the substrate bias, and the transport properties of the different channels were addressed for the first time in [88]. The coupling effect of the lateral, front and back interfaces has been analysed based on the experimental results in FinFETs with various geometries. The devices were fabricated at Motorola, APRDL, using SOI Unibond starting wafers featuring 110 nm thick silicon film and 200 nm thick buried oxide. The fin was defined

by optical lithography. A special trim process was used for further thinning of the fins for well-controlled profiles of 'tall' silicon fins. During the experiment, fin thickness was varied from 0.18 to 10µm, gate length was varied over 0.12 to 10µm range, where as the fin height was kept fixed at 100nm.

Sub-5nm all-around gate FinFETs with 3nm fin width and 14nm fin height were fabricated for the first time in [11]. The device performances were compared and verified by 3D SILVACO simulation. SOI wafers (100) were used as starting material. 100nm silicon film was thinned down to 14nm by using thermal oxidations and HF wet etch. Dual-resist process for a fin and a gate patterning was used to define nanometre features by e-beam lithography and non-critical large-area patterns by optical lithography. After the silicon-fin etch, a sacrificial oxide was grown and removed to alleviate etching damages. 1.4 nm HfO_2 by atomic layer deposition and 2 nm thermal SiO2 were used as gate dielectrics. 30 nm in-situ n+ poly-silicon was deposited for the gate electrode followed by patterning through the dual-resist process. For ultimately scaled transistor, AAG FinFET is known to be the best structure to provide scalability and flexibility in device design.

Because of the limited tunability of threshold voltage, V_t through channel doping in a narrow fully depleted fin, workfunction engineering is crucial for setting the V_t of FinFET devices. Dielectric capping layers have shown potential in modifying the effective work function in high-k/metal gate stacks in planar devices. The possibility of achieving low V_t nMOS FinFET transistors through the use of a La_2O_3 dielectric cap has been investigated for the first time in [89]. FinFET devices were fabricated on a 300mm SOI substrate. Different thicknesses of a thin ALD La_2O_3 capping layer were inserted at different locations in the gate dielectric stack consisting of a 1nm RTO interfacial layer and 2.3nm HfSiO. The high-k stack was topped by a 5nm PE-ALD TiN or 5nm CVD TaN gate electrode. A significant improvement in device performance was shown for thin La_2O_3 capping with CVD TaN electrode.

The first well-behaved inversion-mode InGaAs FinFET with gate length down to 100nm with ALD Al_2O_3 as gate dielectric has been demonstrated in [90]. Using a damage-free sidewall etching method, FinFETs with channel length down to 100 nm and fin width down to 40nm are fabricated and characterized. In contrast to the severe short-channel effect (SCE) of the planar InGaAs MOSFETs at similar gate lengths, FinFET structures have much better electro-static control and show improved Subthreshold slope (SS), Drain Induced Barrier Lowering (DIBL) and Threshold voltage (V_t) roll-off and

less degradation at elevated temperatures. The SCE of III-V MOSFETs is greatly improved by the 3D structure design.

1.5. Short Channel Effects:

The obvious improvements in performance and cost constitute a strong driving force towards smaller dimensions in the fabrication of integrated circuits. As the MOSFET dimensions shrink, they need to be designed properly to preserve the long-channel behaviour as much as possible. As the channel length decreases, the depletion widths of the source and drain become comparable to the channel length and punch-through between the drain and source will eventually occur. Even with the best scaling rules, as the channel length is reduced, departures from long-channel behaviour are inevitable. These departures, the short-channel effects, arise as results of a two-dimensional potential distribution and high electric fields in the channel region. The potential distribution in the channel now depends on both the transverse field (controlled by the gate voltage and the back-substrate bias) and the longitudinal field (controlled by the drain bias). In other words, the potential distribution becomes two-dimensional, and the gradual-channel approximation (i.e, transverse electric field much greater than longitudinal field) is no longer valid. This two-dimensional potential results in many forms of undesirable electrical behaviour. Important electrical parameters as threshold voltage, subthreshold current and transconductance will often be subjected to short channel effects, and hence pushes the device designers towards addressing such undesirable effects in the advanced device structures of nanometre regime.

The short channel effect makes it difficult to maintain a constant threshold voltage while reducing the device dimensions. In short channel devices the threshold voltage becomes a function of both channel length and drain voltage [91]. The reduction of threshold voltage with decreasing channel length and increasing drain voltage is widely used as an indicator of the short-channel effect in evaluating CMOS technologies. This adverse threshold voltage roll-off effect is perhaps the most daunting road block in future MOSFET design. The device minimum acceptable channel length, L_{min} is primarily determined by the threshold voltage roll-off.

The problem associated with the short channel effects is not that devices with different channel lengths have different threshold voltages, since circuit designers typically use only one channel length (the minimum channel length allowed by

processing parameters). Rather the problem is that in short channel devices, small statistical variations in gate length give rise to large variations of threshold voltage, which hurdles integrated circuit manufacturing. The short channel effect, however can be reduced by using shallower junctions and higher substrate doping concentrations, which reduces the extension of source and drain depletion regions in the channel [17].

When scaling rules are not applied to the supply voltage, intense electric fields can develop inside the MOS transistor, especially between the channel pinch-off point and the drain. In an n-channel MOSFET this electric field can accelerate electrons to high speeds. These electrons called “hot electrons” can be stopped by collision events, where the energy released can create electron-hole pairs. These generated electrons can have enough energy to overcome the gate oxide potential barrier and thus be injected into the gate, giving rise to gate current.

Further in the saturation region, the large electric field near the drain substantially accelerates electrons. These electrons can undergo collision events during which energy is released and an electron-hole pair is generated. The generation mechanism is called Impact Ionization. The created electrons are attracted by the positive bias of the drain. The generated holes diffuse towards the ground substrate, giving rise to substrate current. Since both gate current and substrate current are caused by similar mechanisms, transistor designs aim at minimizing the gate current and substrate current simultaneously through various efforts. One such design, called the “lightly doped drain” (LDD) structure, features lighter doping concentrations at the drain junction near the edges of the channel. This helps in reducing the lateral drain electric field and thus reduces impact ionization. The lightly doped portions of Source and drain are commonly called “source and drain extension”.

It is worthy to mention that Drain-Induced Barrier Lowering (DIBL), Gate-Induced Drain Leakage (GIDL), and Reverse Short Channel Effect (RSCE) are the important parasitic effects that are closely related with the short-channel MOS devices. In short channel devices potential barrier at the source can be reduced depending on the drain bias. This reduction of potential barrier reduces the threshold voltage in these device structures. In extreme cases, the potential barrier at the source can become so small that the current between source and drain is no longer controlled by the gate. This phenomenon is called “punch-through” effect.

When a negative gate bias is applied to an n-channel MOSFET, a depletion region can be created in the drain region overlapped by the gate. The effect is also seen when

the drain voltage is positive while the gate is grounded. The depletion region is very thin, and therefore an intense vertical electric field occurs at the drain. Under these conditions electron-hole pairs are generated through band- to-band tunnelling of electrons from the valence band in to the conduction band. The generated holes create a substrate current and the electrons a drain current that increases with increased negative gate bias. Such an undesirable effect is called GIDL effect.

In order to reduce the DIBL effect in very short channel devices, the substrate doping can be increased at the edges of the drain and source junctions. These regions with increased doping concentrations are commonly called “halos”. When channel length is reduced in such structures, the average channel doping concentration increases. This causes threshold voltage to increase when gate length is reduced. The phenomenon is called “reverse short-channel effect”. At shorter channel lengths, however the regular SCE becomes dominant and the threshold voltage drops with reducing channel length.

1.6. Motivation:

In a continuous effort to improve the semiconductor device features while reducing their dimensions well below in the nanometre regime, device designers have proposed and fabricated various novel device structures and process parameter variations in order to follow the predictions of International Technology Roadmap for Semiconductors (ITRS). Nonclassical silicon MOS structures, such as FinFETs, as discussed are replacing the conventional bulk MOS devices because of their capability to attain higher speeds and reduced short channel effects (SCE’s) with the added advantage to design highly integrated CMOS circuits. FinFET structures have been researched since last two decades for its potential to meet the latest technology node requirements as predicted by ITRS. In order to follow the roadmap with the FinFET structures novel structures and processes need to be devised for such a non classical MOS structure. As discussed in this chapter earlier, FinFET structures have been continuously researched with novel structural variants, such as pi- gate, Ω-gate, Gate-All-Around structures. All these efforts aim at improving the characteristics of FinFET structure while reducing the device dimensions to meet the latest technology requirements. FinFETs can enhance drive current of MOS structures and can improve the very daunting SCE’s that affect the device I-V characteristics. In the present work, I-V characteristics of these FinFET structures and the effect of various SCE’s upon the characteristics of FinFETs have been

studied. The I-V characteristics and SCE's of FinFETs have been studied with respect to various scaling and process parameters. Further, an effort has been made to provide valuable conclusions and scope of future study that is possible with these structures.

1.7. Organisation of Dissertation:

The dissertation work has been organised in fallowing seven chapters.

Chapter 1 gives a detailed introduction about different multigate MOS structures and the need to replace conventional bulk MOSFET device structures with the ultrathin body FinFET structures. It introduces about the research problem that has been studied. A brief introduction of various short channel effects that affect FinFET and other multigate structures have been mentioned.

Chapter 2 gives a review of relevant literature that lays a strong foundation for the research work under study. An attempt has been made to cover in brief the stepwise progress of research that has been done from its basic level towards the latest FinFET structures.

Chapter 3 gives an overview of physical modelling approaches that have been developed by various authors for FinFET structures. The modelling of drain current and short channel effects in FinFETs have been reviewed and presented.

Chapter 4 discusses characteristics of various FinFET structures. Effects of scaling parameters and process parameters upon I-V characteristics of these devices has been studied and presented. Transconductance characteristics with respect to various scaling and process parameters has been presented and discussed. The effect of fin size and cross-sectional shape on the output conductance and transconductance of FinFETs as carried out by some authors has also been presented. Furthermore a study based on classical front and back interface coupling effects in thick FinFETs as carried out by some authors has been presented and discussed.

Chapter 5 discusses various short channel effects of FinFET such as DIBL, SS, and V_T-roll-off observed in case of the short-channel devices. A detailed theoretical and simulation study of these effects for the various device structures have been carried out and presented in this chapter. Furthermore the various corner effects in case of triple gate FinFETs as carried out by different authors have been demonstrated.

Chapter 6 gives a comparative simulation study of SCE's in FinFET structures for different channel materials (Si, GaAs, GaSb, GaN). For a given channel material

selected, the effect of gate length and channel width variation on DIBL, SS and threshold voltage roll-off has been studied and presented.

Chapter 7 gives performance evaluation and threshold voltage sensitivity to metal gate work-function in n-FinFET structures for LSTP logic technology. The assessment of various short channel effects on characteristics of FinFET while varying the metal gate work-function has also been studied and presented. It has been proposed that engineering metal gate work-function to adjust the threshold voltage of nanoscale FinFET is the efficient mechanism, because metal gates have the capability to withstand high-k gate dielectric materials that are very much essential for the continuous downscaling of device structures.

Chapter 8 gives a description of simulation tool that has been used in the study of FinFET structures. The advantage of selecting such a simulation tool for the given study has also been demonstrated in the chapter.

Chapter 9 constitutes the last chapter of the dissertation. The chapter gives a conclusion about the research study carried and presents scope of future work that could be taken up to exploit these devices with smaller geometries with better SCE's characteristics.

Chapter 2
Literature Review

As the FinFET technology has shown reduced gate leakage currents, considerable reduction in power consumptions and ability to control the short channel effects over the planar technology, a large number of researchers and designers have been attracted and made a very good study in the field of device simulations and processing technologies of these devices for various applications. FinFET structures have been continuously researched since the vertical ultrathin (< 0.2μm) SOI device structure (DELTA) was proposed and investigated by D. Hisamoto et. al in 1989 [6]. In that paper experimental and simulation results have shown that DELTA offers both consistency with conventional MOSFET and good scalability as a 3-D structure with reduced Short Channel Effects (SCE's). Various researchers have proposed different structural variations and have devised and applied different models and simulation tools for efficiently analysing their characteristics and to improve them with further possible scalability. These simulation tools help device designers to efficiently study the characteristics of the device in advance before their actual fabrication is performed. While simulating device structures in nanometre regime, the main aspects of the study are to improve the drive current of these devices without sacrificing through different short channel effects. Short channel effects are indispensable that impinge the characteristics of device structures at the nanometre scale and hence need to be studied while scaling down the dimensions of FinFET structures. A review of research work carried out on FinFET structures by various researchers since last three decades lays foundation for need of further research, leading to development of novel device structures and techniques for further scaling of device dimensions. In this chapter a review of the relevant literature based on the study of FinFET structures carried out by different authors has been presented.

It is worthwhile to mention here that device simulation of FinFET structures in the nanometre regime using efficient numerical simulation tools or commercially available software packages provide a comprehensive study of the effect of various process variations and physical scaling of different device parameters on short channel effects (SCE's), like Subthreshold Slope (SS), Drain Induced Barrier lowering (DIBL) and threshold voltage roll-off which lead to off-state leakage currents and hence power inefficiency.

Requirements of subthreshold leakage control forces to use higher channel doping as an alternative while scaling the device dimensions of conventional MOS structures into the nanometre regime. It should be mentioned that using this method may lead to undesirable effects such as large junction capacitance and degraded channel mobility. The junction capacitance difficulty can be alleviated by using fully depleted silicon on insulator (SOI) devices [92-94]. FinFET structures which are considered as the best alternatives of conventional bulk or SOI-MOS devices are being researched continuously and different strategies have been worked out to tackle various SCE's and power leakages while scaling down their dimensions much below in the nanometre regime.

Sub 100 nm NMOS [95] and PMOS [96] FinFETs have been previously reported in literature. These double-gate MOSFET structures were demonstrated to robust against SCE's, but they require a complicated fabrication process which yielded large overlap capacitance between the gate and source/drain (S/D) regions. A simpler, more manufacturable process similar to a conventional SOI CMOS process was developed for a quasi planar FinFET structure with much less gate-to-S/D overlap [97]. Sub 20nm gate length CMOS finFETs are demonstrated and novel technologies including fin formation by spacer lithography and raised S/D by selective Ge deposition have been demonstrated. Spacer FinFETs achieve more drive current, for better uniformity of fins and higher device density. Further the subthreshold leakage current for spacer FinFETs is smaller compared with standard FinFETs [98].

The concept of a triple-gate device with sidewalls extending into the buried oxide (more generally called a "π- gate" or "Pi-gate" MOSFET) was introduced in 2001. The proposed device is simple to manufacture and offers electrical characteristics similar to the much harder to fabricate gate-all-around MOSFET [58],[59]. Extending the sidewalls of the gate material in the buried oxide gives rise to a virtual back gate which effectively enhances current drive and shields the back of the channel region from electric field lines from the drain. As a result, DIBL and subthreshold characteristics comparable to those of a quadruple-gate (or GAA) structure are obtained. Further the transconductance and current drive of the double, triple, and quadruple gate structures is approximately two, three and four times that of the single-gate device, as could be expected. More interestingly, the transconductance and current drive of the Pi-gate MOSFET are 3.56 times that of the single-gate device, indicating that the lower part of the gate sidewalls effectively acts as a back gate through lateral field effect in the buried oxide.

A new transistor structure, called Omega Ω-FET, which has the closest resemblance to the Gate-All-Around transistor for excellent scalability, and uses a very manufacturable process similar to that of the FinFET has been proposed in [60]. It has sidewall gates like FinFETs, and special gate extensions under the silicon body, with a gate that almost wraps around the body. In fact, the longer the gate extension, the more the structure approaches the gate-all-around structure [39],[99].

To explore the optimum design space for four different gate structures, simulations were performed with four variable device parameters: gate length, channel width, doping concentration, and silicon film thickness. With an acceptable short channel effects and subthreshold swing, the optimum design space of Pi-gate devices were examined in comparison to double-gate devices. Further it has been shown that the efficiency of the multiple-gate structures depends on the device physical dimensions; for instance, the efficiency of the lateral gates in a triple-gate device decreases as device width is increased, and the gate control of double-gate devices degrades when the silicon film thickness is increased [59].

The abnormal corner effects on channel current in nanoscale triple-gate (TG) MOSFETs have been examined via 2-D numerical device simulations and quasi-2-D analysis of nanoscale TG MOSFETs. From the study it has been shown that the reduced threshold voltage (V_{th}) of the corner regions in the body/channel can be eliminated by leaving the body undoped, and hence relying on a metal gate with proper work function for V_{th} control. The finding adds to the technological and electrical reasons for proposing the use of undoped bodies in nonclassical MOSFETs; the problem of controlling the shape of the corners in the TG device, which is probably not possible, is eliminated [100].

Thin-body silicon on insulator (SOI) transistor structures such as the single-gate (SG) ultra-thin body (UTB) FET and the double-gate (DG) FinFET are attractive for scaling CMOS into the nanoscale regime because of their excellent suppression of off-state leakage current. These advanced structures rely on a thin silicon channel to control short-channel effects, by eliminating any leakage paths far from the gate electrode. A thinner body allows for more aggressive scaling, so that such structures can be easier to scale to sub-50 nm gate lengths as compared to the classic bulk-Si MOSFET structure. It also allows for lower channel doping concentrations to be used, so long as gate-work function engineering techniques are available for adjusting the transistor threshold voltage. Minimization of transistor off-state leakage current is an especially important issue for

low-power circuit applications. A large component of off-state leakage current is gate induced drain leakage (GIDL) current, caused by band-to band tunnelling in the drain region underneath the gate. GIDL current is investigated in thin-body transistors, and found to be significantly lower than in typical bulk-Si MOSFETs. Measured data show that GIDL decreases with decreasing body thickness. This behaviour is attributed to a reduction in transverse electric field and an increase in tunnelling effective mass in the drain region [101].

A study based on the sensitivity of double-gate and FinFET device electrical parameters to process variations was carried out by simulating the device in ISE TCAD in [3]. It has been found that for devices with 20nm nominal gate length and 5nm body thickness, large channel doping concentration is necessary to obtain suitable values of threshold voltage if heavily doped polysilicon gates are used. Because the total volume of the channel region is small, the channel doping in turn will bring uncontrollable V_{th} fluctuations due to the randomness and discrete nature of dopant atoms. Thus, heavily doped polysilicon may not be a viable choice as the gate material. Engineering the gate work function is a more desirable approach to minimize the random dopant effect. Further quantum confinement plays an important role in affecting the performance of devices with small body thickness. As a result, the threshold voltage and current more strongly depend on the body thickness.

Several critical issues of FinFET viz., the effect of fin size, the influence of substrate bias, and the transport properties of different channels were experimentally studied for the first time in [88]. The influence of the fin thickness on short channel and coupling effects has been emphasized. Further it has been shown that classical front and back interface coupling effects still occur in thick FinFETs. In thin devices, the specific architecture of FinFETs can result in the suppression of the back-gate influence. A method has been presented that allows separating the contributions of the various channels in terms of carrier mobilities.

A two-dimensional quantum mechanical modeling has been performed in [102] to simulate a nano-scale FinFET by obtaining the self-consistent solution of coupled Poisson and Schrödinger equations. Calculated current-voltage (IV) curves were carefully compared with experimental data to verify the validity of theoretical work. The transconductance ($g_{m,max}$=380 S/m) has been optimized by varying the silicon fin thickness (T_{fin}) from 10nm to 75nm. Current drivability of FinFET has been investigated by the number of fins used. Calculated Id-Vg curve of single fin FinFET has also been

compared with three and five fins FinFET. It has been verified that the current drivability of multi-fin FinFET is proportional to the number of fins and multi-fin structure is suitable for self aligned and quasi-planner devices.

A self-consistent Quantum Mechanical (QM) approach for the analysis of FinFETs, together with a comparison with the experimental data has been presented in [103]. The simulations have revealed that short-channel effects, like DIBL, threshold voltage roll off can be appreciably suppressed by optimizing the structure of the FinFET with respect to the influence of gate length (L_g) and fin thickness (T_{fin}) on transconductance (g_m). Quantum effects for thin layers are investigated for the electron density by varying T_{fin} and by comparing the simulation results for classical and QM simulation. Simulation results have implied that the FinFET structure is a promising candidate for implementing sub-30nm MOSFETs. Further the simulation results have also shown that a self-consistent solution of the coupled Poisson-Schrodinger equations is mandatory in order to accurately analyze nano-scale structures such as FinFETs.

Due to the strong quantum mechanical confinement in the channel, quantum correction models need to be applied. A comparison of different quantum correction models has been presented and applied to a state-of-the-art three-dimensiona1 device structure. Quantum correction leads to a considerable reduction of the saturation current. The DOS correction model yields reasonable results, but since it does not account for the band bending it must be calibrated for each bias point. Van Dort's model completely fails to reproduce the carrier concentration in the channel [104].

A compact model for threshold voltage of FinFETs based on 2D analytical electrostatic analysis for the cross section of a FinFET, comprising quantum mechanical effects has been presented in [105]. It has been concluded that both gate capacitance and threshold voltage will increase with decreasing fin height or top gate oxide thickness.

A quasi-3D numerical model has been developed for FinFET structure with ultra-thin channel and gate oxide, with the ballistic transport along the channel also accounted for by the application of Non-Equilibrium Greens Function (NEGF) [106]. The model has been found to consider the quantum mechanical effects in all three dimensions. Compared to the quasi-2D simulation of double-gate MOSFETs using NANOMOS, it has been observed that channel electrons are further confined to centre region of the fin together with the rise of the energy of subbands. The model has been suggested to be valid for simulating nanowires with clear physical conception. Using this model, several FinFET structures have been simulated and the device design insight has been acquired.

The results obtained have shown that the nanoscale FinFET devices can work well even when the gate length is below 5 nm.

A three dimensional device simulator ATLAS from SILVACO International [107] has been employed for studying the performance and scaling characteristics of p-channel silicon FinFETs (p-FinFETs) using drift diffusion model. Device short channel effects down to a channel length of 20 nm have been investigated. The results show that the p-FinFET provides good scaling characteristics with the subthreshold slope (SS) increasing from 66mV/dec to 76mV/dec and the drain induced barrier lowering (DIBL) from 17 mV/V to 80 mV/V as the gate length decreases from 80 to 20 nm [108].

Sub-5nm all-around gate FinFETs with 3nm fin width were fabricated for the first time as reported in [11]. The n-channel FinFET of sub-5nm with 1.4nm HfO_2 shows an $I_{d,sat}$ of 497µA/µm at Vg = Vd = 1.0V. The work primarily focuses on feasibility and scalability of sub-5nm All-Around Gate (AAG) FinFET to continue Moore's law beyond sub 5 nm. The characteristics of sub-5nm transistor were verified by using 3-D simulations as well as analytical models. The threshold voltage (V_T) shift by quantum confinement effects becomes significant as fin width (W_{fin}) decreases. For ultimately scaled transistor, AAG FinFET is known to be the best structure to provide scalability and flexibility in device design.

Two dimensional numerical modelling and simulation results with self-consistent solution of the coupled Poisson–Schrödinger equations for multiple-channel FET have been presented in [109]. A Multiple-channel FET is a novel device structure of FinFET wherein center gate is placed at the center of the fin to form a multi-channel. It has been revealed that the drain saturation current ($I_{d,sat}$) of multiple-channel FET at V_d = 0.05 V and V_g = 0.25 V is found to be doubled in comparison to that of the conventional device. Further the calculated transconductance for multiple-channel FET at V_g = -0.2 V and V_d = 0.05 V has been found to be 595 S/m while the transconductance of the conventional device being 300 S/m, which implies the improvement of transconductance by 93%. Simulation results have further revealed that short-channel effects can be appreciably suppressed for multiple-channel FET with respect to the influence of gate length.

Comparison of quantum mechanical and fully classical simulations of FinFETs with commercially available SimuApsys software has been performed in [110]. The simulation results have indicated that the deviation from the classical model becomes more important as the gate oxide, gate length and fin channel-width becomes thinner and the fin channel-doping increases. Gate currents of FinFETs with direct tunneling model

have been well simulated. Because of the ultrathin Si-fin thickness in nanoscale FinFETs, the energy quantization effect becomes evident in the quantum well, which considerably affects electron tunneling significantly, since the current transmission through the potential barrier is influenced by the energy states in the channel quantum well. Gate tunneling current density reduces with the body thickness decreasing with different gate oxides width. Excessive scaling increases the gate current below Fin thickness of 5 nm. The gate current can be dramatically reduced beyond 10^{17} cm^{-3} with the Fin body doping increasing. It has been suggested that the mechanism of gate direct tunneling in very thin silicon layer nanoscale FinFETs must be assessed based on a quantum-mechanical approach to determine the design parameters of future nanoscale FinFETs.

Analytical solution of 3-D Poisson's equation has been used to obtain the subthreshold current and threshold voltage of FinFETs with doped and undoped channels. To model the subthreshold current only the diffusion component has been considered, because in this region of operation, the carrier concentration is low and the drift component of current is negligible. Comparison of the subthreshold current obtained from this diffusion current model with that from the device simulator DAVINCI, which considers both drift and diffusion components was also carried out in the study. The comparison of the two shows an excellent match of the results. Furthermore, the model correctly predicts the variation of subthreshold slope and threshold voltage with device geometry and doping concentration in the silicon fin. The authors have proposed their model to be useful for the design of FinFETs and for circuit simulation purposes [111].

A thorough study based on the coupled solution of Poisson- Schrodinger equation for the corner effects in Pi-gate SOI MOSFETs has been carried out, and the influence of different parameters such as the doping density, silicon-fin dimensions, corner rounding, and gate oxide thickness has been analysed. It has been observed that the extension of corner regions has an inverse dependence on doping concentration and hence a reduction of doping density has been proved to be helpful for preventing the presence of undesirable double threshold voltages. However, it has also been demonstrated that, even when highly doped substrates are used, corner effects can be suppressed as long as the device dimensions are small enough. Moreover, the influence of corner rounding and the reduction of the gate-oxide thickness have also been analyzed. It has been shown that

both corner rounding and gate-oxide-thickness reduction are good techniques to avoid corner effects [112].

Simulation of the FinFET device using Taurus device simulator has been performed in [113] for a detailed numerical analysis of the subthreshold behaviour of FinFET. In that analysis, nickel silicide is used as a gate material. The Inverse Subthreshols Slope (S-factor) has been obtained from the inverse of the slope of the $\ln(I_{DS})$-V_{GS} characteristics for various fin dimensions with the channel length L_g in the range of 20-50 nm and with the fin width T_{fin} in the range of 10-40 nm. It has been observed that the S-factor increases exponentially with decreasing channel length. The rate of the exponential rise increases with increasing the channel thickness. For devices with longer channel lengths, the value of S-factor is close to the ideal value of 60mV/dec. From the simulated S-factor, an empirical relationship using S-factor, L_g and T_{fin} has been obtained. The S-factor calculated from the empirical relationship is in fairly good agreement (within 20%) with the S-factor obtained from the Taurus simulation. Hence the relationship has been proposed to be used as a rule of thumb in determining the S-factor for FinFET devices.

A new body-tied triple-gate fin-type field-effect transistor (bulk FinFET) which has different gate work-functions on the top- and side-channel regions has been studied in [114]. The effect of gate work-function on the characteristics of the bulk FinFETs has been studied through the extensive 3-D device simulation using ATLAS simulator. It has been found that by increasing the top-gate work-function at a fixed side-gate workfunction of the bulk FinFET, threshold voltage (V_{th}) increases and off-state leakage current (I_{off}) reduces significantly without increasing doping concentration of the fin body. The bulk FinFETs with the low body doping and the threshold voltage controlled by midgap-gate work-function show very small dependence on the corner shape, but shows very poor short channel effect (SCE). Furthermore it has been shown that devices with the V_{th} controlled by body doping shows significant corner effect and the effect becomes small as the fin width decreases.

A study on the behavior of the threshold voltage in double-gate, triple-gate and quadruple-gate SOI MuGFETs with different channel doping concentrations has been carried out by Collinge in [115] via three dimensional numerical simulator of Silvaco (Atlas). The results indicate that for double-gate transistors, one or two threshold voltages can be observed, depending on the channel doping concentration. However, in triple- gate and quadruple-gate it is possible to observe up to four threshold voltages due

to the corner effect and the different doping concentration between the top and bottom of the Fin.

SOI and bulk FinFET were analyzed by a three dimensional numerical device simulator and their electrical characteristics were compared for different body doping and bias conditions in [116]. The simulation results show that higher on-state drain current in case of the SOI FinFET is caused by the corner effect, which is effectively doubled in the SOI FinFET compared to the bulk FinFET. Both devices demonstrate good subthreshold characteristics despite high body doping. In order to obtain nearly identical on-state performance in bulk and SOI FinFET, the bulk FinFET body should be lightly doped, or undoped, whereas the threshold voltage should be controlled by the metal gate with mid-gap work function.

A comparison of asymmetric poly-silicon FinFET and TiN gate FinFET with respect to conventional FinFET has been carried out in [117]. Numerical simulations have revealed that the asymmetric poly-silicon FinFET structure and TiN gate FinFET structures exhibit superior threshold voltage (V_{th}) tolerance over the conventional FinFET structure with respect to the variation of fin thickness. For instance, the V_{th} tolerance of the asymmetric poly-Si FinFET were 0.02 V while TiN gate FinFET exhibited 0.015V tolerance for the variation of the fin thickness of 5nm (from 30 to 35 nm) while the conventional FinFET demonstrates 0.12V fluctuation for the same variation of the fin thickness. Furthermore numerical simulation revealed that the threshold voltage (V_{th}) can be controlled within (−0.1 to 0.5V) by the varying of doping concentration of the asymmetric poly-silicon gate region from 1.0×10^{18} to 1.0×10^{20} cm^{-3}.

Independent double Gate (IDDG) FinFET scalable to 10 nm has been presented and validated using well-calibrated SILVACO simulations in [118]. It has been shown that by the use of back gate bias in IDDG FinFETs, novel circuit configurations are possible that utilize less number of transistors and lower power and area compared with the identical circuits designed using the simultaneously driven DG (SDDG) devices. A single IDDG transistor can operate as two transistors with common source and drain terminals. The proposed IDDG-FinFET has a sub threshold slope of 72mV/dec, threshold voltage of 150mV, DIBL of 46mV/V with a minimum threshold voltage roll off. The device parameter analysis carried out in this work can be used as guidelines for the device design by maintaining a subthreshold factor for a given gate length.

A thorough analysis of the scaling issues in double gate underlap FinFET devices with gate lengths of 30 nm has been carried out in [119] using Sentaurus TCAD package for the 2D device simulations. It has been found that gate length scaling severely degrades the device performance, reducing the I_{on}/I_{off} ratio, causing V_{th} roll-off and increasing the DIBL and subthreshold slope. Fin thickness reduction has been found as an important scaling parameter to improve the SCE's and gate leakages at small gate lengths. Although oxide thickness scaling results in better transistor characteristics, but the gate leakage has been found to increase excessively. While evaluating gate leakages, Image force effect has been found to play an important role and its impact can't be neglected. Scaling down of the gate thickness has been found to result in higher drive currents and lower off currents, but gate transconductance and subthreshold slope have been found to degrade. Furthermore increasing the source/drain (S/D) extension lengths has resulted in improvement of the SCE's and has resulted in reduced leakage currents, but the on current has been severely degraded on account of increased fin resistance. Hence suitable optimization of the extension lengths has been proposed as a needed parameter for achieving desired operation.

The authors in [120] have worked upon Trapezoidal FinFET structures for the study of its electrical characteristics. It has been found that Trapezoidal shape FinFET structures present better approximation for FinFET cross sectional shape rather than the design-intended rectangle. The work carried out has analyzed the influence of the FinFET sidewall inclination angle on some relevant parameters for analog design, such as threshold voltage, output conductance, transconductance, intrinsic voltage gain (A_V), gate capacitance and unit-gain frequency, through 3-D numeric simulation. The intrinsic gain is affected by alterations in transconductance and output conductance. The results have shown that both parameters depend on the shape, but in different ways. Transconductance depends mainly on the sidewall inclination angle and the fixed average fin width, whereas the output conductance depends mainly on the average fin width and is weakly dependent on the sidewall inclination angle.

The simulation results have further conveyed that that higher voltage gains are obtained for smaller average fin widths with inclination angles that correspond to inverted trapeziums, i.e. for shapes where the channel width is larger at the top than at the transistor base because of the higher attained transconductance. When the channel top is thinner than the base, the transconductance degradation affects the intrinsic voltage gain.

The electrical characteristics of FinFETs with a TiN/HfO_2 gate stack have been thoroughly studied experimentally and numerically by using 3D device simulations in [121]. The simulations were performed for FinFETs with fin height H_{fin} = 65 nm and fin width, W_{fin} varying from 25 to 875 nm using the drift-diffusion model and Shirahata's mobility model. The results show that the effective work function of the gate stack increases from 4.82 to 5.01eV as the fin width decreases from 875 to 25 nm. The authors have concluded that this shift in effective work function (WF_{eff}) is attributed to a negative interface charge due to different stoichiometry of the top-gate and side-gate interfaces, which affects the TiN/HfO_2 valence band offset and, therefore, the gate dielectric stack effective work function. Optimization of the extension regions under the spacers has been performed for the FinFET with the shorter gate length of L_g = 60 and 30 nm and fin width W_{fin} = 25 nm. The device parameters SS, V_{th}, $I_{d,sat}$ and $I_{d,sub}$ have been calculated with simulations in terms of the extension length and extension doping concentration. The overall results suggest that optimum device performance can be obtained in devices designed with the spacer parameters: $L_{ext} = L_g/2$ for rather long gate devices (L_g = 60 nm) and $N_{ext} = 5 \times 10^{17}$ cm^{-3}. For FinFETs of shorter gate length (L_g = 30 nm), the impact of the extension doping concentration N_{ext} and length L_{ext} on the device parameters SS, V_T and $I_{d,sat}/I_d$, has shown that the optimum spacer length becomes larger compared to the gate length ($L_{ext} \approx 2L_g$ = 60 nm), whereas the extension doping concentration remains the same ($N_{ext} \approx 5\times10^{17}$ cm^{-3}). Therefore, as the gate length becomes shorter, larger extension length is required to suppress more effectively the enhanced SCE's.

Complete 3-D simulations of the devices were performed using SILVACO Atlas TCAD software in [122]. Self-consistent Schrodinger-Poisson with Bohm Quantum Potential model (BQP) has been used for a comparative numerical study of a Body on insulator (BOI) FinFET, a bulk FinFET and an SOI FinFET. The result have shown that, the proposed BOI structure has a saturation current close to that of Bulk FinFET and a DIBL close to that of SOI FinFET. The threshold voltage and subthreshold swing of BOI FinFET can be modulated by varying the length of buried oxide, thus provides a way of fine-tuning threshold voltage without bombarding the channel with dopants. Further it has been concluded that the BOI device can carry as much current as a conventional FinFET while suppressing short channel effects (SCE's) successfully by using localized insulator beneath the channel.

Method for the suppression (and elimination) of corner effects and related kink effect in wide-channel triple-gate bulk FinFETs has been proposed in [123]. As per the method proposed, corner effect can be suppressed by either turning off the corners completely (e.g. implantation with a doping peak value considerably larger than body doping, N_B) or by optimizing corner implantation to obtain the same V_{th} in device's corners as in other parts of the channel. 3D analysis has been performed for both idealized (with square-corner fins) and realistic (with rounded-corner fins) 0.18 µm triple-gate bulk FinFETs. Process and device simulations have shown that the corner implantation is a feasible method which requires no additional masks and can efficiently eliminate the corner effect and remove kink effect from device's transfer characteristics. Obtained threshold voltage shifts were 0.434 and 0.287 V, for the square-corner and rounded-corner FinFET, respectively for body doping of $2e^{18}$ cm^{-3}. Subthreshold swing and DIBL are also significantly improved by corner implantation to values below 95mV/dec and 16mV/V, respectively, due to decreased coupling between the drain and the channel. It has been found that the corners conduct around 25% of the drive current and therefore, turning the corners completely off reduces the on-state current significantly. An optimization procedure of the realistic FinFET has been performed to find the optimum body doping and corner implantation peak values for low-standby power and good saturation performance. It has been determined that the fin–body doping should be approximately $1.1–1.2e^{18}$ cm^{-3} and corner implantation peak $3–5e^{18}$ cm^{-3} to obtain devices with V_{th} around 0.5V and I_{on} around 300 µA without kink effects in transfer characteristics.

The quantum transport model using interpolating wavelet method based on the self-consistent solution of 3-D Poisson-Schrödinger equation has been developed and presented in [124]. It has been seen that the efficiency of the method is better as compared to FDM and FEM methods. The prime focus is to obtain the device characteristics, by numerically solving the 3D Poisson-Schrödinger equations directly until self-consistency is achieved. The subthreshold swing, threshold voltage roll-off, drain current characteristics, enhance the study of various other parameters of the device. Furthermore accurate results have been obtained with significantly reduced computational time.

Chapter 3
Physical Modeling Approaches for FinFET Structures - An Overview

3.1. Introduction:

Multigate transistor structures such as FinFETs are the most promising device structures due to a number of unique features such as ideal subthreshold slope, volume inversion in channel, free-dopant associated fluctuation effects and so on. Their strong electrostatic control over the channel originating from the use of multiple gates reduces the coupling between source and drain in the subthreshold region and it enables the Multigate transistor to be scaled beyond bulk planar CMOS for a given dielectric thickness. Numerous efforts are underway to enable large scale manufacturing of multi-gate FETs. Compact modelling of these advanced device structures serves as a link between process technology and circuit design. It is a concise mathematical description of the complex device physics in the transistor. A compact model maintains a fine balance between accuracy and simplicity. An accurate model stemming from physics basis allows the process engineer and circuit designer to make projections beyond the available silicon data (scalability) for scaled dimensions and also enables fast circuit/device co-optimization. The simplifications in the physics enable very fast analysis of device/circuit behavior when compared to the much slower numerical based TCAD simulations. It is thus necessary to develop a compact model of multi-gate FETs for technology/circuit development in the short term and for product design in the longer term [2]. Analytical models for the estimation of drain current, threshold voltage shift, mobility, and subthreshold leakage current in nanoscale fin-shaped field effect transistor (FinFET) devices have been proposed in literature and the results obtained on the basis of these models have been compared and contrasted with experimental results to validate the accuracy of the proposed device physical models [125].

3.2. Drain Current Modeling:

There have been many efforts to model the drain current for multigate MOS devices. For instance in research publications [162], [163] the authors have used charge sheet models, whereas in [163–171], a constant mobility has been assumed. In this section a brief description of various approaches for modelling drain current of these multigate MOS device structures has been presented.

3.2.1. Continuous Analytical Drain Current Model for Double-Gate MOSFETs:

A continuous, analytic *I–V* model for DG MOSFETs has been derived directly from the Pao-Sah integral without the charge sheet approximation in [137]. It has been shown that the derived analytic solution covers all three regions of MOSFET operations: linear, saturation, and subthreshold, thus maintaining strong continuity between different regions, and yet is completely physics based without the need for ad-hoc fitting parameters.

The model considers an undoped (or lightly doped), symmetric DG-MOSFET. Following Pao–Sah's gradual channel approach [138], Poisson's equation along a vertical cut perpendicular to the Si film takes the following form with only the mobile charge (electrons) term:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q(\psi - V)}{kT}} \tag{1}$$

where q is electronic charge, ε_{si} is the permittivity of silicon, n_i is the intrinsic carrier density, $\psi(x)$ is the electrostatic potential referenced with source drain Fermi level and V is the electron quasi-Fermi potential. An n-MOSFET structure has been considered for model derivation, with the assumption $q\psi/kT >> 1$, so that the hole density is negligible.

Since the current flows predominantly from the source to the drain along the channel direction, the gradient of the electron quasi-Fermi potential is also in the same direction. This justifies the gradual channel approximation that V is constant across the silicon film thickness direction of the DG device. Equation (1) can then be integrated twice to yield the solution [176]

$$\psi(x) = V - \frac{2kT}{q} ln\left[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT} cos\left(\frac{2\beta x}{t_{si}}\right)}\right] \tag{2}$$

where β is a is a constant (of x) to be determined from the boundary condition,

$$\varepsilon_{ox}\frac{V_g - \Delta\Phi - \psi\left(x = \pm\frac{t_{si}}{2}\right)}{t_{ox}} = \pm\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=\pm\frac{t_{si}}{2}} \tag{3}$$

Here ε_{ox} is the permittivity of oxide, V_g is the voltage applied to both gates, t_{si} and t_{ox} are the silicon and oxide thicknesses, and $\Delta\Phi$ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon. In other words, $\Delta\Phi = 0$ for midgap work function gate, $-E_g/2q$ for n^+ poly, and $+E_g/2q$ for p^+ poly, etc. Substituting (2) into (3) leads to

$$\frac{q(V_g-\Delta\Phi-V)}{2kT} - ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right] = ln\beta - \ln[\cos\beta] + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta\tan\beta \quad (4)$$

For a given V_g, β can be solved from (4) as a function of V. Along the channel length, V varies from the source to the drain. So does β. The functional dependence of $V(y)$ and $\beta(y)$ is determined by the current continuity condition which requires the current $I_{ds} = \mu\frac{WQ_i dV}{dy}$ = constant, independent of V or y. Here μ is the effective mobility, W is the device width, and Q_i is the total mobile charge per unit gate area. Integrating $I_{ds}dy$ from the source to the drain and expressing dV/dy as $(dV/d\beta)(d\beta/dy)$, Pao–Sah's integral [139] can be written as

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(V)dV = \mu\frac{W}{L}\int_{\beta_s}^{\beta_d} Q_i(\beta)d\beta \quad (5)$$

where β_s, β_d are solutions to (4) corresponding to V=0 and V=V_{ds} respectively. From Gauss's law, $Q_i=2\varepsilon_{si}(d\psi/dx)_{x=tsi/2}$ [140], which equals $2\varepsilon_{si}$ $(2kT/q)/(2\beta/t_{si})$ $\tan\beta$ using (2). $dV/d\beta$ can also be expressed as a function of β by differentiating (4). Substituting these factors in (5) and carrying out the integration analytically

$$I_{ds} = \mu\frac{W}{L}\frac{4\varepsilon_{si}}{t_{si}}\left(\frac{2kT}{q}\right)^2 \times \int_{\beta_s}^{\beta_d}\left[\tan\beta + \beta\, tan^2\beta + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta\tan\beta\frac{d}{d\beta}(\beta\tan\beta)\right]d\beta$$

$$I_{ds} = \mu\frac{W}{L}\frac{4\varepsilon_{si}}{t_{si}}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta + \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta^2\tan^2\beta\right]\Bigg|_{\beta_d}^{\beta_s} \quad (6)$$

MOSFET characteristics for all regions: linear, saturation, and subthreshold region, can be generated from this continuous, analytic solution. Furthermore it has been verified that *I-V* curves constructed by the analytic model are in complete agreement with 2-D numerical simulation results without fitting terms or parameters.

3.2.2. Non-Charge Sheet Based Surface Potential Plus (SPP) Model for Undoped Symmetric Double-Gate MOSFET:

A non-charge sheet based analytical theory for undoped symmetric double-gate MOSFET has been derived in [141], designated as Surface Potential Plus (SPP).The formulation is based on the exact solution of the Poisson's equation to solve for electron concentration directly rather than relying on the surface potential alone. An exact analytical solution of the electron concentration as an explicit function of the gate voltage and silicon film, thickness valid for all device operation regions has been derived. An expression to model the device I-V characteristics has been formulated and the results have been verified by comparing the model results with AMD double-gate MOSFET's data.

The formulation starts with the solution of 1-D Poisson's equation along to the vertical direction of the silicon channel considering only the mobile charge (electron) density for the undoped body.

$$\frac{d^2\Phi}{dx^2} = \frac{qn}{\varepsilon_{si}} \tag{7}$$

where q is the electronic charge, ε_{si} is the permittivity of silicon, and n is the intrinsic carrier density. According to Boltzmann statistics, the mobile electron concentration can be expressed in terms of potential,

$$n = n_i \exp\left(\frac{q(\Phi - V_{ch})}{kT}\right) \tag{8}$$

Differentiating equation (8) for spatial derivatives of the electron concentration,

$$\frac{d\Phi}{dx} = \frac{kT}{qn}\frac{dn}{dx} \tag{9}$$

$$\frac{d^2\Phi}{dx^2} = \frac{kT}{qn}\frac{d^2n}{dx^2} - \frac{kT}{qn^2}\left(\frac{dn}{dx}\right)^2 \tag{10}$$

Substitution (10) into (7) gives an equation for electron concentration,

$$\frac{kT}{qn}\left[\frac{d^2n}{dx^2} - \frac{1}{n}\left(\frac{dn}{dx}\right)^2\right] = \frac{qn}{\varepsilon_{si}} \tag{11}$$

$$\frac{d^2n}{dx^2} = \frac{1}{n}\left(\frac{dn}{dx}\right)^2 + \frac{q^2n^2}{\varepsilon_{si}kT} \tag{12}$$

This normal differential equation has two mathematical solutions, one is trigonometric function and another is the hyperbolic function, given by,

$$n(x) = \frac{c_0}{cos^2\left[\left(\frac{q^2c_0}{2\varepsilon_{si}kT}\right)^{1/2} x\right]} \tag{13}$$

$$n(x) = \frac{c_0}{cosh^2\left[\left(\frac{q^2c_0}{2\varepsilon_{si}kT}\right)^{1/2} x\right]} \tag{14}$$

For consistent with the common treatment and mathematical simplicity of a model, trigonometric function (13) has been chosen as electron distribution function. Further it has been supposed that at $x=0$, $n(x)=n_0$, equation (14) is further simplified into,

$$n(x) = \frac{n_0}{cos^2\left[\left(\frac{q^2n_0}{2\varepsilon_{si}kT}\right)^{1/2} x\right]} \tag{15}$$

Substitution of (15) into (7) gives the corresponding electrical field and potential distributions in the silicon film, which is give by,

$$\Phi(x) - \Phi_0 = \frac{kT}{q} ln\, cos^{-2}\left[\left(\frac{q^2n_0}{2\varepsilon kT}\right)^{1/2} x\right] \tag{16}$$

$$E(x) - E(x_0) = \left[\frac{2n_0kT}{\varepsilon}\right]^{1/2} tan\left[\left(\frac{q^2n_0}{2\varepsilon kT}\right)^{1/2} x\right] \tag{17}$$

The symmetry of boundary condition of double gate makes the electric field of the centre of the silicon film to be zero. If this centre is chosen as the reference coordinates zero point, then, the surface potential and the surface electric field are given simply, respectively

$$\Phi_s = v_{ch} + \frac{kT}{q} ln\left[\frac{n_0}{n_i} cos^{-2}\left[\left(\frac{q^2 n_0}{2\varepsilon kT}\right)^{1/2} \frac{T_{si}}{2}\right]\right] \tag{18}$$

$$E_s = \left[\frac{2n_0 kT}{\varepsilon}\right]^{1/2} tan\left[\left(\frac{q^2 n_0}{2\varepsilon kT}\right)^{1/2} \frac{T_{si}}{2}\right] \tag{19}$$

The half of the total inversion charge Q_{in} has been obtained as,

$$Qin = q\int_0^{\frac{T_{si}}{2}} n(x)dx \tag{20}$$

Equation (20) gives,

$$Q_{in} = [2\varepsilon n_0 kT]^{1/2} tan\left[\left(\frac{q^2 n_0}{2\varepsilon kT}\right)^{1/2} \frac{T_{si}}{2}\right] \tag{21}$$

In practice, the surface potential, field and carrier concentration are controlled by applying a gate voltage. According to Gauss's law, the total applied gate voltage is,

$$V_G - \Delta\psi_i = \Phi_s + E_{ox} t_{ox} = \Phi_s + \frac{Q_{in}}{\varepsilon_{ox}} t_{ox} \tag{22}$$

where $\Delta\psi_i$ is the work function difference.

The surface potential and inversion charge has been used to obtain the following expression that can give electron concentration at the centre of the silicon channel (n_0) as a function of gate voltage, channel voltage, and silicon film thickness, given by

$$V_G - \Delta\psi_i - v_{ch} = \frac{kT}{q} ln\left[\frac{n_0}{n_i} cos^{-2}\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{\frac{1}{2}} \frac{T_{si}}{2}\right]\right] + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} [2n_0 \varepsilon_{si} kT]^{1/2} tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} \frac{T_{si}}{2}\right] \tag{23}$$

In the *I-V* model derivation, all biases are normalized by kT/q and inversion charge is normalized by $C_{ox}kT/q$. From the inversion charge obtained, expression for *I-V* characteristics of undoped double gate MOSFET have been formulated following the *Pao and Sah's* idea which includes both the drift and diffusion carrier transport components for modelling of drain current [142]. The resulting current expression as obtained in this model is given by,

$$I_{ds} = \frac{\mu w}{L} C_{ox} \left(\frac{kT}{q}\right)^2 \left[\frac{q_s^2 - q_d^2}{2} + (q_s - q_d)\right] \tag{24}$$

As the charge formulation only accounts for half of the channel, the final current of a double-gate MOSFET should be doubled. The results obtained agree well with the *Pao-Sah* current formulation and are physically accurate. The model has been proposed to be

useful in modelling a wide range of devices to be used in nano-CMOS technology and has been verified by AMD double-gate data.

3.2.3. Modeling Based on Pierret and Shields' Type Formulation:

Analytical modeling of drain current model for nanoscale undoped-body symmetric dual-gate MOSFETs based on a fully consistent physical description has been presented in [143]. The model is a fully consistent physical description of diffusion and drift transport, based on a Pierret and Shields' type formulation [145], expressed in terms of surface and center-of-film potentials evaluated at the source and drain ends. The derivation is completely rigorous and is based on a procedure proposed for long-channel bulk SOI MOSFETs presented in [144]. The expression is a continuous description valid for all bias conditions, from subthreshold to strong inversion and from linear to saturation operation. The validity of the model has been ascertained by extensive comparison to exact numerical simulations. The results attest to the excellent accuracy of this formulation.

This formulation of the model has been considered as a starting point to develop improved models for Double Gate (DG) devices. In that context, the model does not intend to account for short-channel effects, carrier confinement energy quantization, interface roughness, ballistic-type transport, mobility degradation, etc. Further for the sake of simplicity, the formulation is based on Maxwell–Boltzmann carrier charge distribution statistics.

As a first step to calculate the electric potentials considering n-MOS structure, the one dimensional poisons equation has been solved in the transverse (body thickness) direction which has resulted in the following two expressions given by,

$$V_{GF} = \psi_s + \frac{\sqrt{2kTn_i\varepsilon_s}}{C_0}\sqrt{e^{-\beta V}\left(e^{-\beta\psi_s} - e^{\beta\psi_0}\right)} \tag{25}$$

$$\psi_s = \psi_0 - \frac{2}{\beta} ln\left\{cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_s}}\, e^{\frac{\beta(\psi_0 - V)}{2}} \frac{t_{Si}}{2}\right]\right\} \tag{26}$$

where V_{GF} is the difference between the gate-to-source voltage and flat-band voltage, $\beta=q/kT$ is the inverse of the thermal voltage, ψ_s is the surface potential $(x= t_{si}/2)$, ψ_0 is the potential extremum at the centre of the silicon film $(x= 0)$, C_0 is the gate oxide capacitance per unit area, ε_s is the permittivity of the semiconductor, t_{si} is the semiconductor film thickness, V is the difference between electron and hole quasi-Fermi

levels along the channel which is the channel voltage equal to *0* at the source and to V_{DS} at the drain.

The above system of two equations (25) and (26) needs to be solved to obtain the surface potential, ψ_s, and the centre-of-film potential extremum, ψ_o, both at the source, $y=0$, and at the drain, $y=L$, ends of the channel. The solution at the source end, with $V = 0$, gives: $\psi_s=\psi_{s0}$ and $\psi_o=\psi_{o0}$. Analogously, solving at the drain end with $V=V_{DS}$ produces: $\psi_s=\psi_{sL}$ and $\psi_o=\psi_{oL}$.

The drain current has been expressed following *Pao and Sah's* idea [140] that including both the drift and diffusion carrier transport components in the silicon film, leads to a current description with smooth transitions between operating regions. The obtained drain current may be expressed as,

$$I_{D=}\mu\frac{W}{L}\int_0^{V_{DS}} Q_I dV \tag{27}$$

where μ is the effective electron mobility, W is the channel width, L is the effective channel length, and Q_I is the total (integrated in the transverse direction) inversion charge density inside the silicon film at a given location, y, along the channel. It is defined by,

$$Q_I \equiv -2q\int_0^{t_{si/2}}(n-n_i)dx = -2q\int_{\psi_0}^{\psi_s}\frac{(n-n_i)}{F}d\psi \tag{28}$$

where n_i is the intrinsic carrier density and F is the electric field.

An equivalent to *Pao–Sah's* equation may be obtained for the SOI-MOSFET by substituting (28) into (27), and remembering that $n >> n_i$

$$I_D = 2\,\mu\frac{w}{L}\int_0^{V_{DS}}\int_{\psi_0}^{\psi_s}\frac{qn}{F}\,d\psi\,dV \tag{29}$$

where the electric field in the semiconductor film is given by

$$F = -\frac{d\psi}{dx} = -\sqrt{\frac{2kTn_i}{\varepsilon_s}}\sqrt{e^{-\beta V}(e^{\beta\psi}-e^{\beta\psi_0})} \tag{30}$$

and

$$n = n_i e^{\beta(\psi-V)} \tag{31}$$

Equation (30) may be written as

$$F = -\sqrt{\frac{2kTn_i}{\varepsilon_s}e^{\beta(\psi-V)}} + \alpha \tag{32}$$

where

$$\alpha = -\frac{2kTn_i}{\varepsilon_s}e^{\beta(\psi_0-V)} \tag{33}$$

is defined as an interaction factor representing the charge coupling between the two gates [175].

Differentiating (31) partially with respect to channel voltage, following the procedure developed by *Pierret and Shields'* [145]

$$\frac{\partial F}{\partial V} = \frac{1}{2F}\frac{d\alpha}{dV} - \frac{1}{F}\frac{qn_i}{\varepsilon_s}e^{\beta(\psi - V)} \tag{34}$$

Substituting equation (31) into (34),

$$\frac{qn}{F} = \varepsilon_s\left(\frac{1}{2F}\frac{d\alpha}{dV} - \frac{\partial F}{\partial V}\right) \tag{35}$$

Further substitution of (35) into (29) gives,

$$I_D = 2\mu_n\frac{W}{L}\varepsilon_s\int_0^{V_{DS}}\int_{\psi_0}^{\psi_{DS}}\left(\frac{1}{2F}\frac{d\alpha}{dV} - \frac{dF}{dV}\right)d\psi dV \tag{36}$$

The drain current equation is further solved analytically and the final expression takes the following form,

$$I_D = \mu\frac{W}{L}\left\{\begin{array}{c} 2C_0\left[V_{GF}(\psi_{SL} - \psi_{S0}) - \frac{1}{2}(\psi_{SL}^2 - \psi_{S0}^2)\right] + \\ 4\frac{kT}{q}C_0(\psi_{SL} - \psi_{S0}) + t_{Si}kTn_i\left[e^{\beta(\psi_{oL} - V_{DS})} - e^{\beta\psi_{oo}}\right] \end{array}\right\} \tag{37}$$

The model has been devised for the drain current modeling of nanoscale undoped-body symmetric dual-gate MOSFETs. The model is a fully consistent physical description of diffusion and drift transport, based on a Pierret and Shields' type formulation, expressed in terms of surface and centre-of-film potentials evaluated at the source and drain ends. The expression is a single explicit analytic equation continuously valid for all bias conditions, from subthreshold to strong inversion and from linear to saturation operation. Further the model accuracy has been demonstrated through extensive comparisons with the exact numerical simulations.

3.2.4. BSIM-CMG and BSIM-IMG Modeling:

Framework for Multi-gate FET modeling may also be handled by categorising them into two categories and introduce a separate model for each category: a common gate model and an asymmetric/independent gate model. The term "common-gate" means that all the gates in the multi-gate FET (double-gate or triple-gate or quadruple-gate FinFET) are electrically interconnected and are biased at the same electrical gate voltage. The common-gate model further assumes that the gate work-functions and the dielectric thicknesses on the two, three or four active sides of the fin are the same. However, the carrier mobilities in the inversion layers on the horizontal and vertical active sides of the fin can be different due to different crystal orientations and/or strain. The asymmetric/independent gate model allows different work-functions and dielectric thicknesses on the top and bottom of the fin. The asymmetric/independent gate model also permits that the two gates can be biased independently [2].

Compact models for multi-gate FETs: BSIM-CMG and BSIM-IMG, have been developed which describe numerous physical effects such as quantum mechanical effect

(QME), poly-depletion effect (PDE), short-channel effect (SCE), mobility degradation and carrier velocity saturation. BSIM-CMG (Berkeley Short-channel IGFET Model-Common MultiGate) models the common-gate multi-gate FETs and BSIM-IMG (BSIM-Independent Multi-Gate) models the independent/asymmetric multi-gate FETs. The expressions derived for terminal currents and charges are continuous, which makes the two models suitable for mixed-signal design. Both the models are accurate, predictive and scalable as demonstrated through extensive 2-D and 3-D TCAD simulations. In the following a brief description of the BSIM-CMG model is presented in this chapter.

BSIM-CMG is a surface potential based model. All electrical variables such as terminal currents, charges and capacitances are derived from the surface potentials at the source and the drain end. The calculation of the surface potentials forms the basis of the model. BSIM-CMG models the effect of finite body doping on the electrical characteristics of a multi-gate FET in Poisson's equation [146]. Starting from a core long-channel symmetric DG-FET framework, the model is extended to triple-gate FinFETs and quadruple-gate FinFETs through 3-D modeling of SCE. The BSIM-CMG model has been successfully used to describe the measured electrical characteristics of SOI FinFETs and bulk FinFETs [147].

The electronic potential in the body has been obtained by solving Poisson's equation in gradual channel approximation which includes both inversion carriers and the bulk charge in the body given by,

$$\frac{\partial^2\psi(x,y)}{\partial x^2} = \frac{qn_i}{\mathcal{E}_{si}} . e^{\frac{q\left(\psi(x,y)-\Phi_{B-V_{ch}(y)}\right)}{kT}} + \frac{qN_A}{\mathcal{E}_{si}} \tag{38}$$

where $\psi(x,y)$ is the electronic potential in the body, $V_{ch}(y)$ is the channel potential ($V_{ch}(0)= 0$ and $V_{ch}(L) =V_{ds}$), N_A is the body doping and

$$\Phi_B = \frac{kT}{q} . ln\left(\frac{N_A}{n_i}\right) \tag{39}$$

Perturbation approach has been used to solve Poisson's equation in presence of significant body doping [146]. Under this approach, the potential in the body can be written as sum of two terms:

$$\psi(x,y) = \psi_1(x,y) + \psi_2(x,y) \tag{40}$$

The first term, $\psi_1(x,y)$, is the potential due to the inversion carriers term in Eq. (38). The second term, $\psi_2(x,y)$, is the perturbation in potential due to body doping term. The body can be fully depleted or partially depleted depending on applied gate bias (V_{gs}),

body doping *(N_A)* and body thickness *(T_{Si})*. The perturbation method yields surface potential in both full depletion and partial-depletion regimes.

In the fully depleted regime, the inversion carriers are spread through the entire body. The contribution of inversion carriers to the potential, $\psi_1(x,y)$, is calculated by neglecting the bulk charge term in Eq. (38).

$$\frac{\partial^2\psi_1(x,y)}{\partial x^2} = \frac{qn_i}{\varepsilon_{si}} . e^{\frac{q(\psi_1(x,y)-\Phi_B-V_{ch}(y))}{kT}} \tag{41}$$

Using the fact that the electric field at the mid-plane is zero for a symmetric common gate FET, Eq. (41) can be integrated twice to obtain $\psi_1(x,y)$.

$$\psi_1(x,y) = \psi_0(y) - \frac{2kT}{q} . ln\left(cos\left(\sqrt{\frac{q^2}{2\varepsilon_s kT}\frac{n_i^2}{N_A} e^{\frac{q(\psi_0(y)-V_{ch}(y))}{kT}}} . \frac{x}{2} \right)\right) \tag{42}$$

where $\psi_0(y)$ is the potential at the centre of the fin body. Substituting Eq. (41) in Eq. (40) yields a second order differential equation in $\psi_2(x,y)$.

$$\frac{\partial^2\psi_2(x,y)}{\partial x^2} = \frac{qni}{\mathcal{E}si} . e^{\frac{q(\psi_1(x,y)-\Phi_B-V_{ch}(y))}{kT}} . \left(e^{\frac{q\psi_2(x,y)}{KT}} - 1 \right) + \frac{qNA}{\mathcal{E}si} \tag{43}$$

Equation (43) is solved to obtain expression for $\psi_2(x,y)$. Then the surface potential at a point '*y*' along the channel is the sum of $\psi_1(x,y)$ and $\psi_2(x,y)$ evaluated at the surface:

$$\psi_s(y) = \psi_1\left(\frac{T_{si}}{2}, y\right) + \psi_2\left(\frac{T_{si}}{2}, y\right) \tag{44}$$

The electric field at the surface can be easily obtained by integrating Eq. (38) once. Gauss's Law at the surface can then be expressed as

$$V_{gs} = V_{fb} + \psi_s(y) + \frac{\varepsilon_{Si}}{C_{ox}} . \sqrt{\frac{2qn_i}{\varepsilon_{si}}\left(\frac{e^{\frac{q\psi_s(y)}{KT}} - e^{\frac{q\psi_0(y)}{KT}}}{\frac{q}{kT}} . e^{\frac{-q(V_{ch}(y)+\Phi_B)}{kT}} + e^{\frac{q\Phi_B}{KT}} . ((\psi_s(y) - \psi_0(y)) \right)} \tag{45}$$

Eq. (45) can be expressed in terms of only one unknown quantity $\psi_0(y)$. Solving Eq. (45) yields $\psi_0(y)$ and hence $\psi_s(y)$ in the fully depleted regime for a given DG-FET structure and a set of external bias voltages.

The *I-V* model is obtained using drift-diffusion formulation without using any charge-sheet approximation [174]. The current flowing through the body of a DG-FET can be written as:

$$I_d = 2.\mu.W.Q_{inv}(y)\frac{dV_{ch}}{dy} \tag{46}$$

where μ is the carrier mobility (assumed position independent), W is the channel width, $Q_{inv}(y)$ is the inversion charge in one half of the body and the factor of two accounts for the front and back channel currents in a symmetric common-gate DG-FET. Finally an

analytical expression for the drain current is formulated. The resulted equation is expressed as difference of two terms evaluated at the source and drain end:

$$I_d = 2.\mu.\frac{W}{L}.(f(\psi_s) - f(\psi_D)) \tag{47}$$

where the function *f(ψs(y))* is given by:

$$f(\psi_s) = \frac{Q_{inv}^2}{2C_{ox}} + 2\frac{kT}{q}Q_{inv} - \frac{kT}{q}\left(5\frac{\varepsilon_{si}kT}{qT_{si}} + Q_{bulk}\right).ln\left(5\frac{\varepsilon_{si}kT}{qT_{si}} + Q_{bulk} + Q_{inv}\right) \tag{48}$$

Eqs. (47 & 48) predict the drain current for a symmetric DG-FET and they together constitute the *I-V* model for BSIM-CMG. The accuracy and predictivity of the *I-V* model has been verified against TCAD simulations without using any fitting parameters. The comparison has been made based on model predicted and TCAD simulated values of I_d for a heavily doped DG-FET ($N_A = 3e18cm^{-3}$). It has been verified that BSIM-CMG can predict very accurate drain current in all the regimes of transistor operation: sub-threshold, linear and saturation. In the next case the validity has been tested over a wide range of body doping. The model has predicted the correct drain current in both fully depleted and partially depleted regimes.

BSIM-IMG models the independent/asymmetric multi-gate FET. Unlike the BSIM-CMG model, BSIM-IMG assumes a lightly doped body in the Poisson equation for simplicity. For an independent/asymmetric multi-gate FET, the threshold voltage of the transistor can be tuned by adjusting the back gate voltage. As a result, a lightly doped body is expected to be used even for a multiple-threshold voltage technology and heavy body doping can be avoided in the thin body. Many of the physical effects models are borrowed from BSIM-CMG model with appropriate changes for an independent gate operation [2].

3.3. Modeling Short Channel Effects (SCE's):

Multi-gate MOSFETs have been found to have highest scaling potential that can be scaled to the shortest channel length possible for a given gate oxide thickness. The advantages of these multi-gate MOSFETs include: ideal 60mV/dec subthreshold slope, scaling by silicon film thickness without high doping, setting of threshold voltage by gate work functions, etc. The key factors that limit how far a multi-gate MOSFET can be scaled come from short-channel effects (SCEs) such as threshold voltage roll-off and drain-induced barrier lowering (DIBL). As far as short-channel effects are concerned, several models have been published based on different approaches of modelling these

SCE's [148-150]. Under this section a brief description of some of the SCE models for multi-gate devices based on the derivation carried out by different authors is presented.

3.3.1. Modeling GIDL Current:

Minimization of transistor off-state leakage current is an especially important issue for low-power circuit applications. A large component of off-state leakage current is gate induced drain leakage (GIDL) current, caused by band-to-band tunneling in the drain region underneath the gate: when there is a large gate-to-drain bias, there can be sufficient energy-band bending near the interface between silicon and the gate dielectric for valence-band electrons to tunnel into the conduction band. GIDL imposes a constraint for gate-oxide thickness scaling because the voltage required causing this band-to-band tunneling leakage current decreases with decreasing gate oxide thickness, and GIDL can pose a lower limit for standby power in memory devices [151]. Band-to-band tunneling is possible only in the presence of a high electric field and when the band bending is larger than the energy band gap, E_g,. The field in silicon at the Si-SiO_2 interface also depends on the doping concentration in the diffusion region and the difference between V_D and V_G, i.e. V_{DG}.

A simple expression for the surface electric field at the dominant tunneling point can be expressed as

$$E_s = \frac{V_{DG}-1.2}{3T_{ox}} \tag{49}$$

where E_s is the vertical electrical field at silicon surface, 3 is the ratio of silicon permittivity to oxide permittivity, and T_{ox} is the oxide thickness in the overlap region. A band bending of 1.2 V is the minimum necessary for tunneling process to occur. The theory of tunneling current predicts [152]

$$J = A.E_s.\exp\left(-B/E_s\right) \tag{50}$$

where A is a pre-exponential parameter, B (typically 23–70MV/cm) is a physically-based exponential parameter.

The measured GIDL is dependent on the drain doping profile (which results in a non-uniform electric field), a transverse electric field, and also the effective mass of tunnelling electrons, each of which is difficult to determine accurately. B was an empirical parameter, therefore used practically as a fitting parameter to match the model with measured data [153-156].

It is worthy to mention that the transverse electric field and potential in the drain region are lower in thin-body MOSFETs as compared to the bulk-Si MOSFET. This reduction is greater for the DG structure than for the SG structure, and the reduction in transverse electric field increases as the body thickness decreases. Since there is no analytical equation available to describe the electric field strength dependence on the body thickness, so in order to investigate GIDL current in ultra-thin body and multigate MOSFET device structures, authors in [151] have investigated the electric field distribution using a 2-D device simulator (MEDICI).

3.3.2. Threshold Voltage and Subthreshold Swing Modeling:

Two key characteristics of a MOSFET that are particularly important to digital applications are threshold voltage and subthreshold swing. As the channel length (L) of a MOSFET is reduced, threshold voltage (V_{th}) typically decreases and subthreshold swing (S) increases, commonly known as short-channel effects (SCE's). Consequently, the ratio of the drive current to the leakage current is substantially reduced, which results in significantly increased stand-by power and/or compromised performance of integrated circuits (IC's). Moreover, the functionality of IC's may be jeopardized by increased susceptibility to process variations [157].

Compact physical short-channel models of subthreshold swing and threshold voltage for undoped symmetric DG MOSFETs that use the same material for both gates have been studied in [158]. In the following subthreshold swing and threshold voltage models as described in [158] are presented.

(a) Threshold Voltage Model:

It has been observed that, in undoped devices, the inversion carrier concentration exceeds that of ionized dopant atoms under threshold conditions [160]. It ramifies the need to take mobile carriers into consideration for threshold voltage calculations. In addition, the conventional way of defining threshold voltage by the surface band bending equal to $2\varphi_B$ becomes irrelevant, where $\varphi_B = (kT/q)\ \ln(NA/n_i)$ with N_A and n_i being the doping concentration and the intrinsic carrier concentration in Si, respectively. To properly address both issues, the 2D Poisson equation with the inversion charge term included,

$$\frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} = \frac{q}{\varepsilon si} n_i \ exp\left(\frac{q\varphi}{kT}\right) \tag{51}$$

is solved in the channel region for the channel potential $\phi(x, y)$ (referenced to the Fermi level) under threshold conditions [161]. The threshold voltage is then defined as the gate voltage at which the sheet density (i.e. integrated density) of inversion carriers at the virtual cathode reaches a value, Q_{TH}, adequate for the turn-on condition. Such a definition is equivalent to the constant-current methodology widely used in both measurement and numerical simulations. The resulting threshold voltage model is obtained as [161],

$$V_{TH} = \Phi_{MS,i} + \eta \frac{kT}{q} \frac{cosh(\theta)}{cosh(\theta/2)} ln\left(\frac{Q_{TH}}{n_i t_{si}}\right) - \left[\frac{cosh(\theta)}{cosh(\theta/2)}\eta - 1\right]\varphi_{0m} \quad (52)$$

where $\Phi_{MS,i}$ is the gate work function referenced to the intrinsic silicon, $\eta = 1 + (2\theta/r)$ $\tanh(\theta)$, $\theta = Bt_{Si}/L$, $B = \pi[1 + 2\exp(-qV_{bi,i}/2kT)\lambda_{Di}/L]^{-1}$, $V_{bi,i} = (kT/q)ln(N_{D/S}/n_i)$, $N_{D/S}$ is the source/drain doping concentration and λ_{Di} is the intrinsic Debye length given as $\lambda_{Di}=(2\varepsilon_{Si}kT/q^2n_i)^{1/2}$. Parameter ϕ_{0m} represents the minimum potential in the $n^{++}-p--n^{++}$ (source–channel–drain) junction without intervention of the gate bias $\phi_{0m} = V_{bi,i} - (2kT/q)\ln([2 + \exp(qV_{bi,i}/2kT)L/\lambda_{Di}]/\pi)$.

The general, short-channel threshold voltage model (52) readily simplifies into a long-channel model for large values of L,

$$V_{TH,long} = \Phi_{MS,i} + \frac{kT}{q} In\left(\frac{Q_{TH}}{n_i t_{si}}\right) \quad (53)$$

The slight semilog dependence of $V_{TH,long}$ on t_{Si} seen in (53), supported by excellent agreement with numerical simulations [161], indicates that the volume inversion effect continues into the near-threshold region. Threshold voltage roll-off ΔV_{TH}, i.e. the difference between short- and long channel threshold voltages, as obtained by (52) and (53) is given by,

$$\Delta V_{TH} = \left(\frac{kT}{q} In \frac{Q_{TH}}{n_i t_{si}} - \varphi_{0m}\right)\left[\eta \frac{cosh(\theta)}{cosh(\theta/2)} - 1\right] \quad (54)$$

It has been found that equation (54) closely agrees with numerical simulations for a variety of device parameter sets [161].

(b) Subthreshold Swing Model:

The two-dimensional (2D) Poisson equation with the ionized dopant term only is analytically solved in the channel region to obtain the channel potential distribution [159]. As a result of device symmetry and the negligible amount of ionized dopant atoms, the potential profile in the channel thickness direction is essentially flat in long-channel DG MOSFETs. The entire channel, therefore, is inverted to the nearly same

degree, known as the volume inversion effect. In short-channel devices, the channel centre has a higher electrostatic potential than anywhere else because of the influence of the source/drain and weakened gate control, and it becomes the leakiest path. The difference between the centre potential and the potential in other locations, however, is very limited. Consequently, the effective conducting path remains in between the channel centre and channel surface, leading to a compact analytical subthreshold swing model [159] given by,

$$S = \left[1 - 2\Gamma_1 \cos\frac{t_{si}}{4\lambda 1} exp\left(-\frac{L}{2\lambda 1}\right)\right]^{-1} \frac{kT}{q} ln10 \tag{55}$$

Where k is the Boltzmann constant, T is the temperature, q is the electron charge and t_{Si} is the channel thickness. The parameter λ_1 is determined by the vertical dimensions

$$\lambda_1 = \frac{1+1/r}{1+\pi/2} t_{si} = \frac{t_{si}+\varepsilon_{Si} t_{ox}/\varepsilon_{ox}}{1+\pi/2} \tag{56}$$

$$\lambda_1 = \frac{1+\sqrt{2}/r}{\sqrt{2}+\pi/2} t_{si} = \frac{t_{si}+\sqrt{2}\varepsilon_{si} t_{ox}/\varepsilon_{ox}}{\sqrt{2}+\pi/2} \tag{57}$$

for $r \leq \pi/2$ and $r > \pi/2$, respectively, where $r = \varepsilon_{ox} t_{Si}/\varepsilon_{Si} t_{ox}$, t_{ox} is the gate oxide thickness, and ε_{ox} and ε_{Si} are the permittivity of the gate oxide and silicon, respectively. The parameter Γ_1 is given as,

$$\Gamma_1 = \frac{2\lambda_1}{t_{si}} \cdot \frac{\sqrt{1+\frac{t_{si}^2}{r^2\lambda_1^2}}}{\left(\frac{1}{r}+\frac{1}{2}+\frac{t_{si}^2}{2r^2\lambda_1^2}\right)} \tag{58}$$

It is clearly seen from equation (55) that the dependence of subthreshold swing on device parameters is primarily given by the ratio of L/λ_1, hence, λ_1 is referred to as scale length. At large values of L/λ_1 corresponding to long-channel designs, subthreshold swing approaches its ideal value of kT/q (*i.e, ~ 60mV/dec at 300K*), as explained by the gate-to-gate capacitive coupling [157]. It increases in short-channel designs with small values of L/λ_1.

Using the new subthreshold swing and threshold voltage models, scaling limits of DG MOSFETs are projected based on three criteria: (1) an excellent turn-off behaviour of $S = 70$ *mV/dec*, (2) a moderate turn-off behaviour of $S = 100$ *mV/dec* and (3) V_{TH} reduction not to exceed 70 mV for 30% L-equivalent reduction from its nominal value [161]. The individual DG MOSFETs with satisfactory turn-off characteristics are feasible with L as short as ~10 nm (~12 nm for $S = 70$ *mV/dec* and ~7 nm for $S = 100$ *mV/dec*). However, adequate control of parameter variations (such as V_{TH}), which is

needed for gigascale integration of these devices, presents the biggest challenge for scaling, allowing L to be reduced only to ~16nm [158].

3.3.3. BSIM-CMG Modeling of SCE's:

BSIM-CMG modeling of SCE's in case of FinFET structures has been presented in [2]. In that model the degree of SCE (V_{th} roll-off, drain-induced barrier-lowering, and subthreshold slope degradation) depends on strength of gate control which is modeled by a characteristic field penetration length $(\lambda=f(T_{ox}, T_{si}))$ derived from quasi 2-D Poisson's equation. The SCE model shows excellent agreements with 2-D TCAD simulation results without the use of any fitting parameters. Good scalability over T_{ox} and T_{si} down to 30nm channel length (L_g) is possible. The SCE model is extended for considering the triple or more gates structures by making $\lambda = f(T_{ox}, T_{si}, H_{fin})$. The SCE model implementation captures the V_{th} roll-off, DIBL and subthreshold slope degradation for short-channel multi-gate FETs simultaneously.

The short-channel behavior is determined by the change in the minmum potential barrier ($\Delta\Psi_m$) inside the conduction channel due to the potential coupling from the drain terminal. Suzuki et al. [162] reported the scaling theory of double-gate MOSFETs by solving the 2-D Poisson's equation of potential inside the conduction channel. $\Delta\Psi_m$ is modelled through a characteristic field penetration length. By linking $\Delta\Psi_m$ to the effective gate bias, this approach is computationally efficient and easily extended to consider QM-effect-induced finite inversion charge thickness.

For the BSIM-CMG and BSIM-IMG models, a sophisticated SCE model based on Suzuki's approach has been developed by considering symmetric/common gate DG-FET structure. The 2-D Poisson's equation in the subthreshold region has been written as:

$$\frac{d^2\psi(x,y)}{dx^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = \frac{qNA}{\varepsilon_{si}} \tag{59}$$

where N_A is body doping. Since the transistor is in subthreshold regime, the inversion carriers are ignored.

In the subthreshold region, the parabolic potential profile has been assumed in the vertical x-axis direction (film thickness direction): [163]

$$\psi(x,y) = C_0(y) + C_1(y).x + C_2(y).x^2 \tag{60}$$

Combined with two boundary conditions at middle of channel (x=0) and channel/dielectric interface ($x=T_{si}/2$ and $x=-T_{si}/2$):

$$\frac{d\psi(x,y)}{dx}\Big|_{x=0} = 0 \tag{61}$$

$$\frac{d\psi(x,y)}{dx}\Big|_{x=\pm\frac{T_{si}}{2}} = \pm\frac{V_g - V_{fb} - \psi_s}{t_{ox}} \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}} \tag{62}$$

where V_g is the gate voltage, V_{fb} the flat band voltage, and Ψ_s is the surface potential. The potential profile $\Psi(x,y)$ is given by

$$\psi(x,y) = \psi_s(y) - \frac{V_g - V_{fb} - \psi_s(y)}{t_{ox}} \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \left(x + \frac{T_{si}}{2}\right) + \frac{V_g - V_{fb} - \psi_s(y)}{t_{ox} t_{si}} \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}} \tag{63}$$

As discussed earlier, the SCE has been determined by the change of minimum potential barrier. In the DG MOSFETs, the minimum potential barrier, which determines the leakage path, is located in the center plane of the channel. The potential at the centre plane of the channel (Ψ_c) is obtained by evaluating equation (63) at $x=0$,

$$\psi_c(y) = \psi_s(y) - \frac{V_g - V_{fb} - \psi_s(y)}{t_{ox}} \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}} \tag{64}$$

The potential profile $\Psi(x,y)$ is then expressed in terms of $\Psi_c(y)$. The resulting expression is substituted in the 2-D Poisson's equation of potential. A differential equation of potential at the centre plane of channel in terms of characteristic field penetration length (λ) is formulated which is given by,

$$\frac{d^2\psi_c(y)}{dx^2} + \frac{V_g - V_{fb} - \psi_c(y)}{\lambda^2} = \frac{qN_A}{\varepsilon_{si}} \tag{65}$$

where,

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \cdot \left(1 + \frac{\varepsilon_{ox} T_{si}}{4\varepsilon_{si} t_{ox}}\right)} \cdot T_{si} \cdot t_{ox} \tag{66}$$

Applying two boundary conditions for $\Psi_c(y)$ where $\Psi_c(y=0)=V_{bi}$ and $\Psi_c(y=L)=V_{bi}+V_{ds}$, one can solve the above Poisson's equation for $\Psi_c(y)$:

$$\psi_c(y) = V_{SL} + (V_{bi} - V_{SL}) \frac{\sinh\left(\frac{L-y}{\lambda}\right)}{sinh\left(\frac{L}{\lambda}\right)} + (V_{bi} + V_{ds} - V_{SL}) \frac{sinh\left(\frac{y}{\lambda}\right)}{sinh\left(\frac{L}{\lambda}\right)} \tag{67}$$

Where

$$V_{SL} = V_g - V_{fb} - \frac{qN_A}{\varepsilon_{si}} \lambda^2 \tag{68}$$

and

$$V_{bi} = 0.56 + \frac{kT}{q} \cdot ln\left(\frac{N_A}{n_i}\right) \tag{69}$$

The minimum point of Φ_c(y) will determine the short-channel behavior and is formulated as:

$$\psi_c(min) = V_{SL} - \frac{V_{ds}^2 \cdot e^{-L/2\lambda}}{\left(e^{L/\lambda} - e^{-L/\lambda}\right)\sqrt{Z_0 Z_L}} + 2\sqrt{Z_0 Z_L} \frac{sinh(L/2\lambda)}{sinh(L/\lambda)} \tag{70}$$

where

$$\left.\begin{aligned} Z_0 &= V_{bi} - V_{SL} \\ \text{and} \quad Z_L &= V_{bi} - V_{SL} + V_{ds} \end{aligned}\right\} \tag{71}$$

The minimum potential barrier $\Psi_c(min)$ is controlled by device geometry, channel doping and drain potential. One can use an effective V_g shift (ΔV_g) in the long-channel model to obtain the same potential barrier for short-channel devices:

$$\Delta V_g = \psi_c(min) - V_{SL} \tag{72}$$

Since the voltage shift is function of gate bias, it captures the change in subthreshold slope simultaneously. The model predicts both V_{th} roll-off and subthreshold degradation simultaneously without the use of any fitting parameters. Furthermore to validate the model accuracy, 2-D TCAD results have been compared with the model predicted results, wherein a very good agreement has been obtained.

For a FinFET with more than two gates, the physical location of the minimum potential barrier (or the path for maximum drain leakage current) is different from that in a DG-FET. The extra electrostatic control from vertical ends (top gate or bottom gate) reduces short-channel effects. The V_{th} roll-off decreases as fin height (H_{fin}) decreases. The most leaky channel path is located at the center bottom of the fin where the electrostatic control from the gate is the weakest. The potential barrier at this most leaky path decreases as fin height increases, resulting in an H_{fin} dependence of short-channel effects.

To model the fin height dependence on short-channel effects, a new characteristic field penetration length λ_{Hfin} is introduced:

$$\lambda_{Hfin} = \sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}} . \left(1 + \frac{\varepsilon_{ox} H_{fin}}{2\varepsilon_{si} T_{ox}}\right) . H_{fin} . T_{ox}} \tag{73}$$

The final characteristic length used in the short-channel model is taken from the average of the two scaling lengths:

$$\lambda_{eff} = \frac{1}{\sqrt{\left(\frac{1}{\lambda}\right)^2 + \left(\frac{a}{\lambda_{Hfin}}\right)^2}} \tag{74}$$

where $a = 0$ for DG-FET, $a = 0.5$ for triple-gate FET, $a = 1$ for surrounding-gate FET. Note that in the case of triple-gate FET, one can also use different oxide thickness in λ and λ_{Hfin} to model the thick SiO_2 layer (hard mask) on top of the fin. By making the characteristic field penetration length as a function of H_{fin}, the DG short-channel model is extended to triple-gate and surrounding-gate FETs. Furthermore the model predicted

results for threshold voltage roll-off characteristics of triple gate FinFET with those of TCAD simulation results have shown a very good agreement.

3.4. Conclusion:

An overview of different physical modeling approaches for multigate MOSFET (FinFET) structures has been presented. Various modeling approaches for drain current and SCE's associated with multi-gate MOSFET structures have been overviewed. To be mentioned, a non-charge sheet based SPP model for undoped symmetric double gate MOSFET has been discussed. The model has been found to agree well with the Pao Sah current formulation and has been proposed to be useful for a wide range of nano-CMOS technology. Modeling based on Pieret and Shields' type formulation for nanoscale undoped body symmetric dual gate MOSFET has been discussed. It has been mentioned that the expression for drain current is explicit analytical equation, continuously valid for all bias conditions, for from subthreshold to strong inversion and from linear to saturation operation. Also the model has been found to agree with the exact numerical simulations. BSIM-CMG model, a surface potential model has been discussed that can accurately predict drain current in all regions of operation: viz; subthreshold, linear and saturation and in both fully depleted and partially depleted regimes. Without using any fitting parameters BSIM-CMG model can give results that are valid against the TCAD simulation results. Theory of GIDL current, caused due to band-to-band tunnelling effects at high fields has been discussed, wherein an expression for GIDL current has been mentioned. A brief description of compact physical short channel models of subthreshold swing and threshold voltage roll-off for undoped symmetric double gate MOSFETs has been presented. Short channel effect modelling for double and triple gate FinFET based on BSIM-CMG has been presented. The model can have excellent agreement with the 2D-TCAD simulation results without using any fitting parameters and good scalabilty of t_{ox} and t_{si} down to 30nm channel. These models can accurately predict the physical behaviour of various multi-gate MOSFET structures which serve as a link between process technology and circuit design. Furthermore to make the future scale integration of multi-gate MOSFET devices possible with the scaling dimensions following the projections of ITRS road map, it becomes necessary to theoretically evaluate the various current voltage (I-V) characteristics and short channel effects (SCE's) of these devices in advance before one could think of developing the technology

for fabrications of these devices and exploring the possibility of using the devices in circuit design applications.

Chapter 4
Characteristics of Various FinFET Structures

4.1. Introduction:

In view of the massive utilisation of FinFETs in the CMOS integrated circuit fabrication, these devices are comprehensively investigated to continue the scaling trend of these advanced device structures for further high scale integration density and reduced chip area. FinFETs are basically an alternative to the conventional MOSFET devices only to continue the scaling trend of MOS devices in order to follow the projections made by ITRS annual reports for future device scaling. The I-V characteristics of FinFETs as expected resemble with the device I-V characteristics of conventional planar MOSFET structures, but the former can be scaled much below in the nanometre scale. FinFET devices can be characterised both as n-channel or p-channel structures as is the case with conventional planar MOSFET devices. As discussed in preceding chapters, FinFET differs from the MOSFET in that it utilises an ultra-thin fin body and a multi-gate architecture for the efficient control of channel potential, enhanced drive current and reduced leakage currents in subthreshold regime. In this chapter a study based on I-V characteristics of FinFET devices and the effect of various scaling and process parameter variations on the device I-V characteristics has been carried out. Results of some experimentally fabricated FinFET structures from various authors have been presented as a reference to study the various I-V characteristics of FinFET. Various FinFET structures whose physical parameters have been undertaken as per the experimentally fabricated FinFET structures from different authors have been simulated. The results generated from the simulation of such structures have been compared for their validity with the results of experimentally fabricated devices, wherein a good agreement has been observed. Transconductance characteristics with respect to scaling parameters have been studied and discussed. The effect of fin size and shapes on the output conductance and transconductance characteristics of FinFETs as carried out by some authors have been presented and discussed. Furthermore a study based on classical front and back interface coupling effects in thick FinFETs as carried out by some authors has been presented and discussed. From this study it has been found that for thick FinFET devices, the coupling between front and back channels is strong and back channel conduction appears, where as in case of thin FinFETs, the back conduction and coupling

effect are reduced. The various electrical characteristics of FinFET based on simulation study have been carried out by undertaking the device structures as per the projections made by ITRS [1].

4.2. I-V Characteristics of Some Experimentally Fabricated FinFET Structures:

Won-Ju Cho has fabricated and studied p-FinFET with gate lengths varying from 20-100nm silicon fin width of 20nm, and the gate oxide of 4nm. The silicon nitride film with 20 nm thickness was deposited to form the sidewall spacer of gate electrode. The substrate doping concentration of 4×10^{18} cm^{-3} has been undertaken as a necessary step to suppress the short-channel effect [177]. Fig. 4.1 shows the subthreshold current

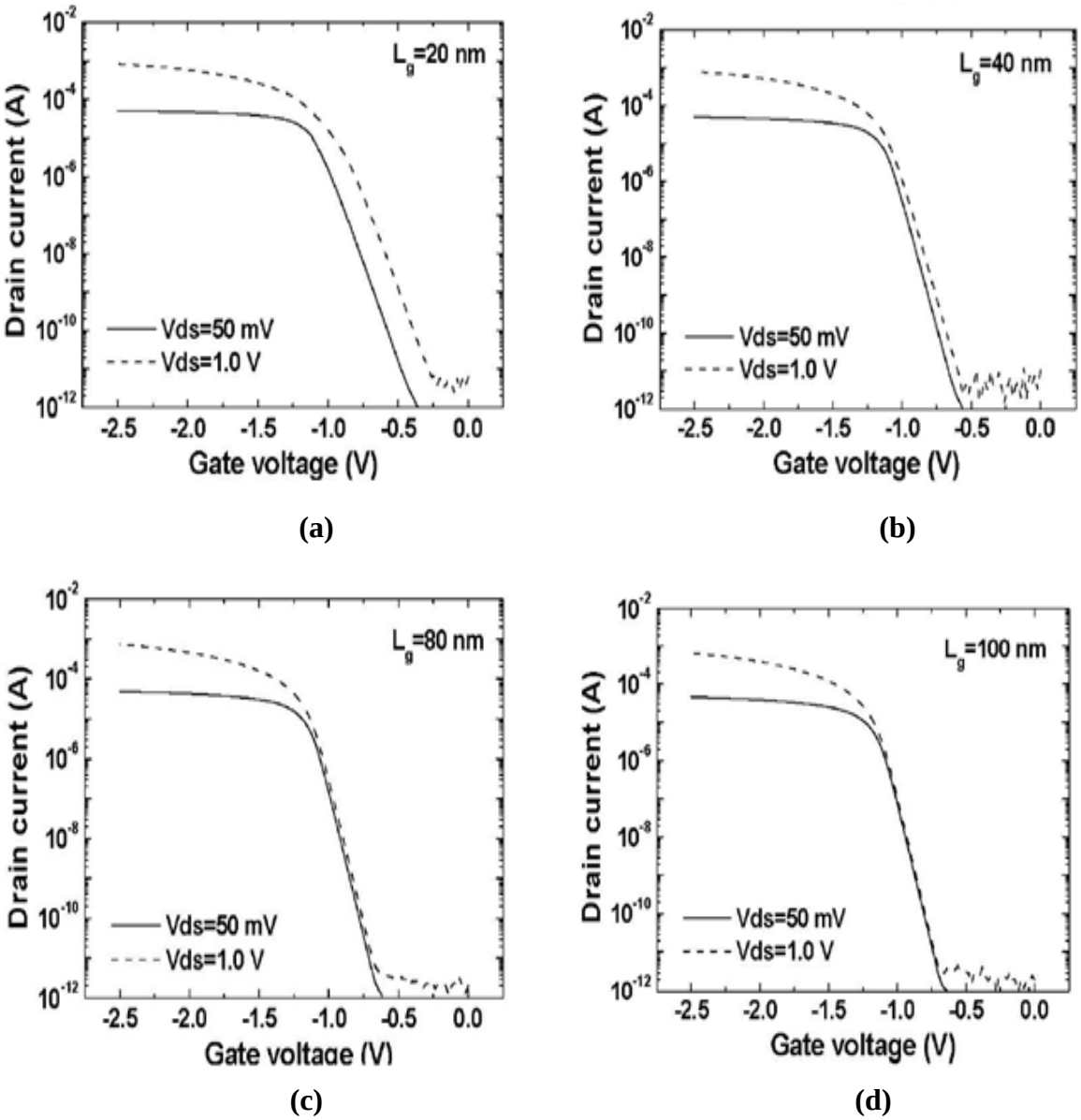


Fig. 4.1. I_d-V_g characteristics of *p*-type FinFETs: (a) L_g = 20nm (b) L_g = 40nm (c) L_g = 80nm (d) L_g = 100nm [177]

characteristics (I_d-V_g) for the p-type FinFET devices as a parameter of gate length, L_g. The results obtained from the fabricated FinFETs with a 100 nm gate length have showed good subthreshold characteristics. The threshold voltage (V_t) and subthreshold swing for this device were -0.96V and 67mV/dec, respectively. The degradation of subthreshold swing, the roll-off of V_t and the increase of drain-induced barrier lowering (DIBL) were observed as the gate length decreases. In the case of 20 nm gate length, the threshold voltage, subthreshold swing and DIBL were -0.83V, 97mV/dec and 190mV/V, respectively. Furthermore it is worth noting that for all variants of gate length from 20 to 100nm, the device on-current is about 10^{-3}A at V_d=1.0V.

Fig. 4.2 shows the measured drain current characteristics (I_d-V_{ds}) as a parameter of

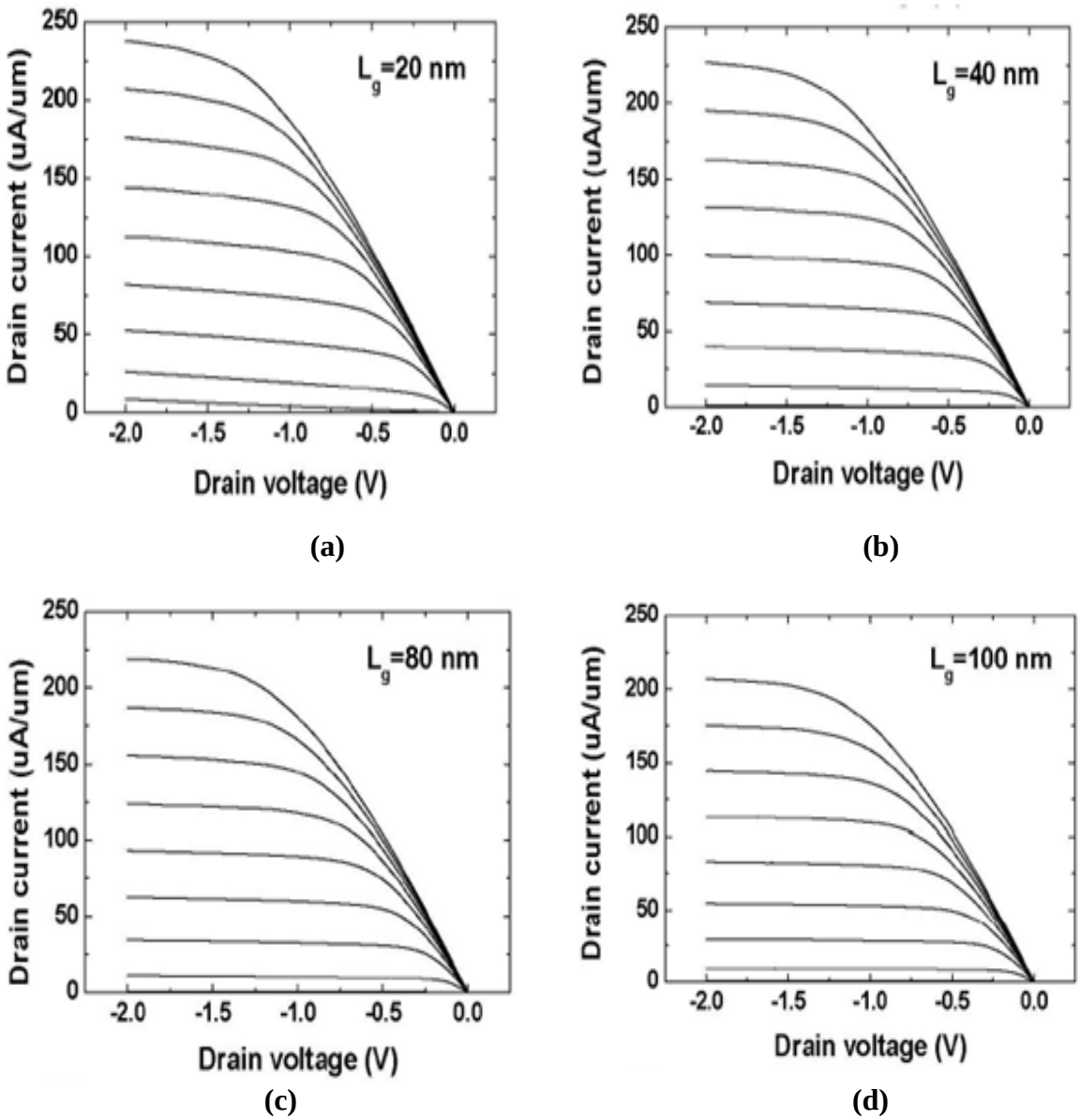
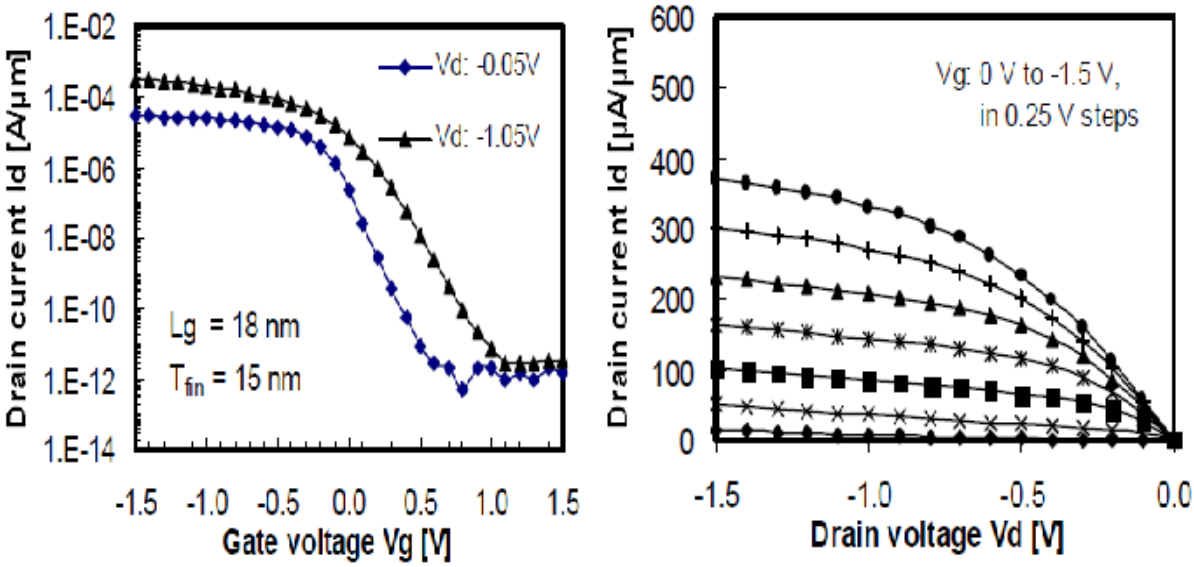


Fig. 4.2. I_d-V_{ds} characteristics of *p*-type FinFETs: (a) L_g = 20nm (b) Lg = 40nm (c) L_g= 80nm (d) L_g = 100nm [177].

gate length, L_g. The increase of drain current with the decrease in gate length, L_g from 100 nm to 20 nm has been observed due to the decrease of channel resistance of the device. However, the short channel effect (SCE) has been slightly observed in the 20 nm gate length FinFET devices.

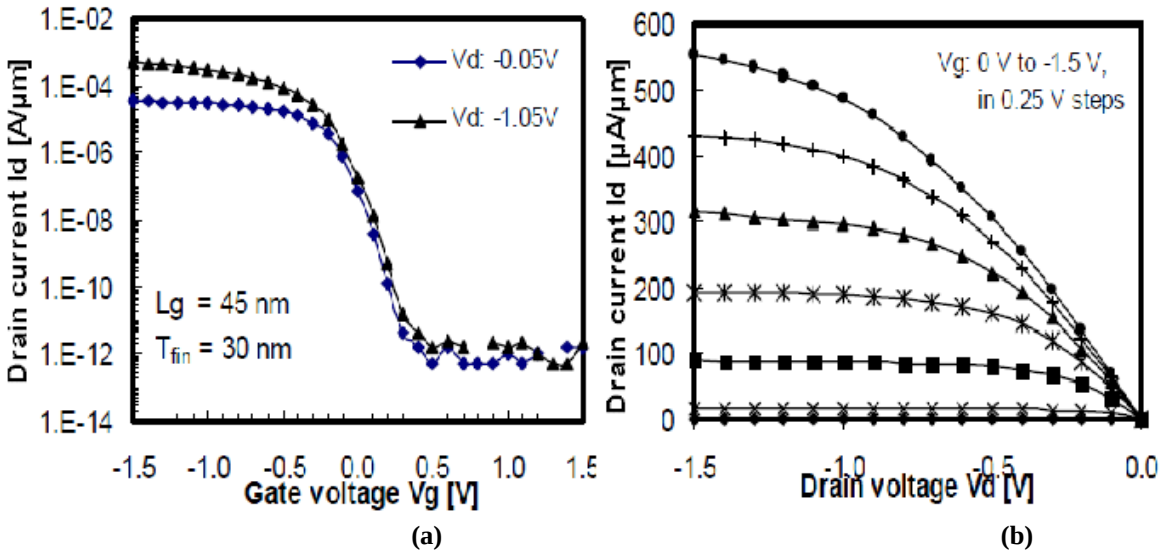
Sub 50-nm p-channel FinFETs were experimentally fabricated in [10], which exhibit good performance characteristics and reduced short channel effects. Heavily doped p-type poly- $Si_{1-x}Ge_x$ (60% Ge) with work function 4.75eV has been used as the gate material, because of its lower resistivity compared to poly-Si gate material doped with the same concentration. These devices were characterized for the fin thickness ranging from 15-30nm, gate oxide of 2.5nm and with a body doping concentration of 10^{16} cm^{-3}. The device I-V characteristics have been calculated for FinFETs of gate length, L_g of 18nm and for 45nm. Fig. 4.3 shows the I-V characteristics of a 18-nm gate length device with a 15 nm-thick Si fin body wherein the saturated drain current, I_{dsat} is 288µA/µm at $V_d = V_g = 1.2$ V. Fig. 4.4 shows the I-V characteristics of a 45-nm gate length device with a 30 nm-thick Si body wherein the $I_{d,sat}$ is 410µA/µm at $V_d = V_g = 1.2$ V.

The experimental data obtained in this experiment [10] closely matches 2-D device simulations that assume simple Gaussian doping profiles and a uniformly doped channel region. Drift diffusion simulation underestimates the current by 15% for the 45nm device. The energy balance model was found to give excellent agreement with experimental data.



(a) **(b)**

Fig. 4.3. I-V characteristics of PMOS FinFET with 18-nm gate length and 15-nm Si fin body: (a) Drain current versus Gate voltage (b) Drain current versus Drain voltage [10].



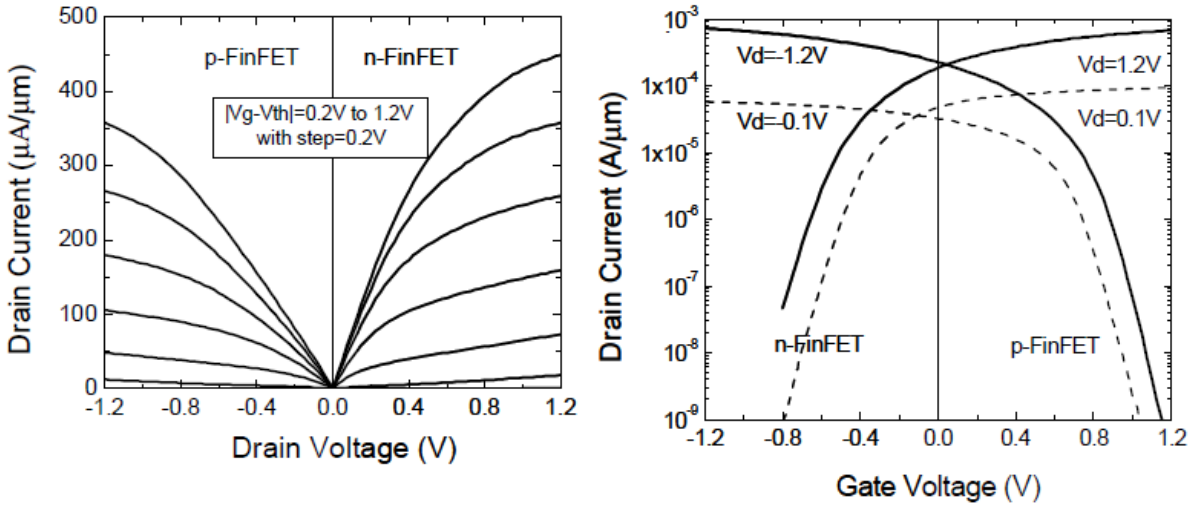
(a) **(b)**

Fig. 4.4. I-V characteristics for 45-nm gate length and 30-nm thick Si body PMOS FinFET device: (a) Drain current versus Gate voltage (b) Drain current versus Drain voltage [10].

Furthermore it has been mentioned in reference [10] that by employing the same simulation model and source-drain diffusion profiles which match experimental results of the 45nm and 18nm devices, the performance of a 10nm FinFET was simulated**.** By aggressively scaling the gate oxide thickness (1.2nm) and the silicon fin width (7nm), a drive current of 347µA/µm, or 694µA/µm**,** depending on the definition of device width, can be achieved while still maintaining low leakage (2.3 or 4.6nA/µm) and minimal short-channel effects. This is due to the excellent short channel behavior of the double-gate MOSFET structure.

The authors Bin Yu *et.al* [178] reported the design, fabrication, performance, and integration issues of double-gate FinFET with the physical gate length being aggressively shrunk down to 10nm and the fin width down to 12nm. A nitrided oxide with 17Å physical thickness was used as the gate insulator. Fig. 4.5 (a) shows I_d-V_d characteristics of the 10nm gate length CMOS FinFETs. The drive currents are 446µA/µm for n-channel FinFET and 356µA/µm for p-channel FinFET, both measured at a gate over-drive of 1V and a V_{dd} of 1.2V. All the currents are normalized by two times the fin height (i.e., the total channel width of a double-gate device). A large V_{dd} is selected due to the thick gate oxide used. Fig. 4.5 (b) is the subthreshold I_d-V_g behaviour for the same devices. In this experiment the threshold voltages are shifted from the desired values due to the use of poly-Si gate and lightly doped channels. The threshold voltage can be fixed by proper channel implant and/or using alternative gate materials

with appropriate work-function. It is to be mentioned at here that for 10nm gate length FinFET, the measured sub-threshold slopes are 125mV/dec for n-channel FinFET and 101mV/dec for p-channel FinFET, respectively. The DIBL's are 71mV/V for n-channel FinFET and 120mV/V for p-channel FinFET, respectively. Thus with the demonstrated scalability and potential performance benefit (under the penalty of adding some fabrication complexity to the existing planar process), the FinFET has been proposed as a strong competitor to classical CMOS.



(a) **(b)**

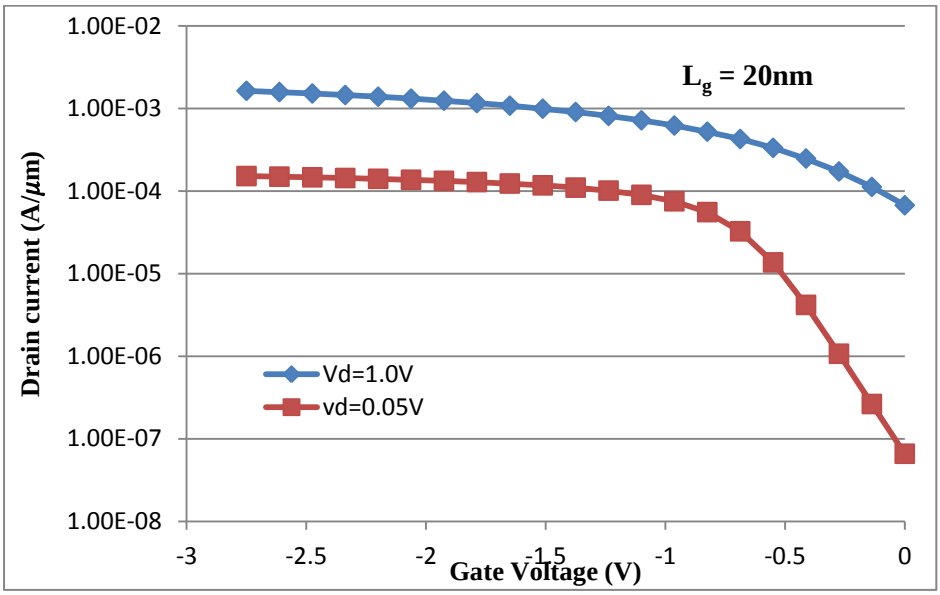
Fig. 4.5. (a) I_d-V_d characteristics of 10nm gate length CMOS FinFET transistors. (b) Subthreshold I_d-V_g behavior of 10nm gate length CMOS FinFET transistors [178].

4.3. Simulation Results of FinFET Devices and Comparison with Experimentally Available Data:

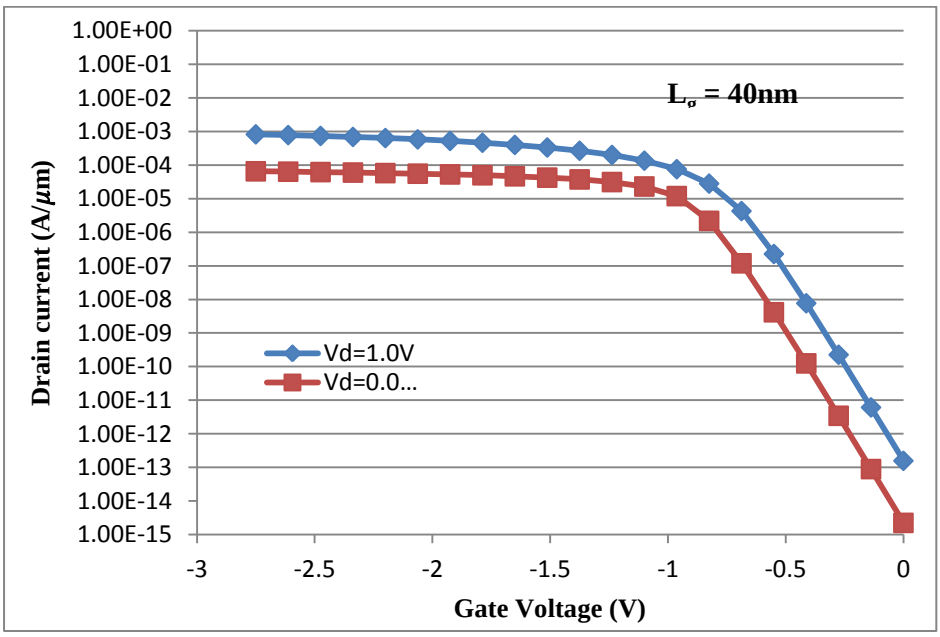
As a part of our present study the computer simulation of various FinFET structures for which the experimental data has been taken from the research work of various authors, has been carried out. A comparison of simulated results of I_d-V_g characteristics with the experimental results as obtained in [177] for the p-FinFET with gate lengths varying from 20-100nm, for a fixed channel width of 20nm and gate oxide thickness of 4nm has been performed. In the simulation set up same physical device parameters have been used as given in [177]. The channel doping concentration has been kept fixed at $4\times10^{18}cm^{-3}$, while as the drain/source doping concentration has been kept fixed at $4\times10^{21}cm^{-3}$. The gate bias has been varied from 0V to -2.75V with a bias step of 0.1375V for the two different drain biases, 0.05V and 1.0V. The device threshold voltage has been defined as the gate voltage for which the drain current equals

0.0001A/μm. Furthermore the device on current has been defined as the drain current that is obtained for gate voltage of -2.75V.

From the simulation results obtained through PADRE device simulator, it can be seen from Fig. 4.7 (a-d) that the device subtheshold characteristics improve as the gate length, L_g is increased from 20 to 100 nm. The degradation in subthreshold behaviour with decreasing gate length, L_g is due to the short channel effect of device while scaling from



(a)



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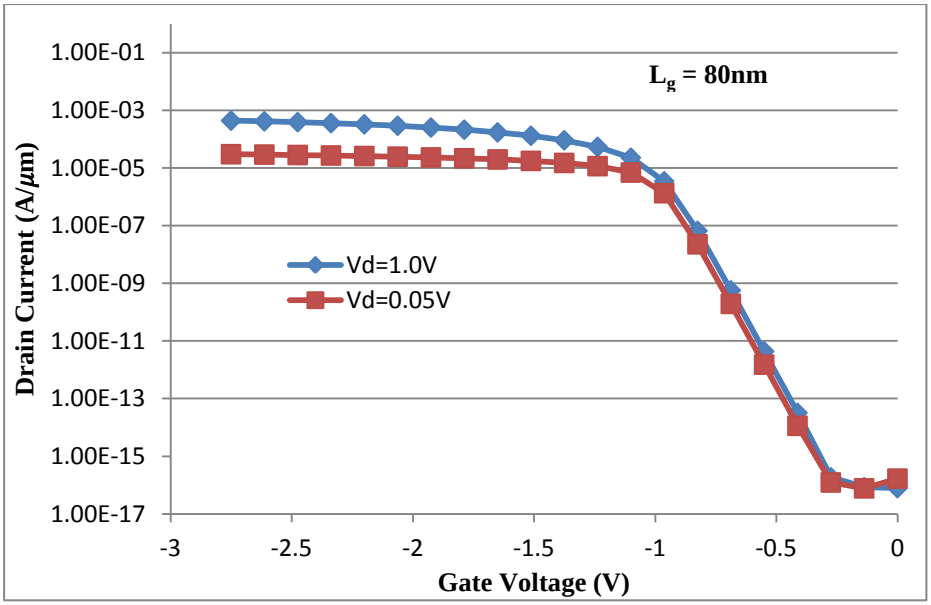
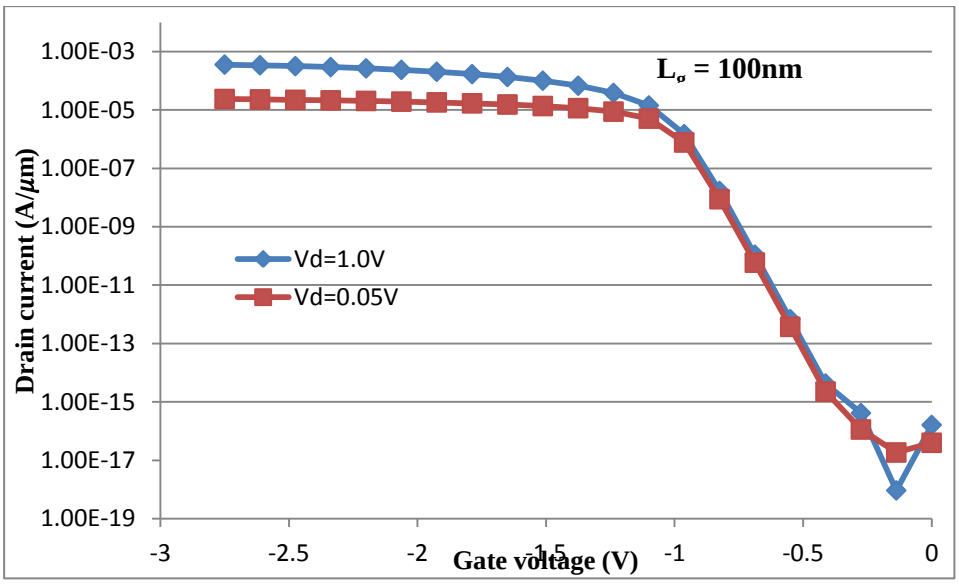


(c)



(d)

Fig. 4.7. Simulated transconductance (I_d-V_g) characteristics of *p*-type FinFETs: (a) L_g=20nm (b) Lg=40nm (c) L_g=80nm (d) L_g=100nm.

100nm to 20nm gate length. The simulated device on current for different gate lengths agrees very well with the experimental results. For instance the device on current as observed for 40nm gate length equals 824μA/μm which is in good agreement with the experimental data.

In the next case of simulation study, the transfer characteristics of FinFET structure with 45nm gate length and 30nm fin thickness have been simulated using the PADRE

simulator. For the simulation setup the oxide thickness has been kept fixed at 2.5nm, while as the body doping concentration has been kept 1e16cm^{-3}, undertaken as per the experimentally fabricated device in reference [10]. The device structure has been simulated for drain bias of -0.05V and -1.05V and for gate bias varied in the range of -1.5V to 1.5V with a step size of 0.1V. A very good agreement of the simulated transfer characteristics with the experimental data is obtained. This can be justified by comparing the resulting simulated device I_d-V_g characteristics of Fig. 4.8 with the experimental characteristics as given in Fig. 4.4 above.

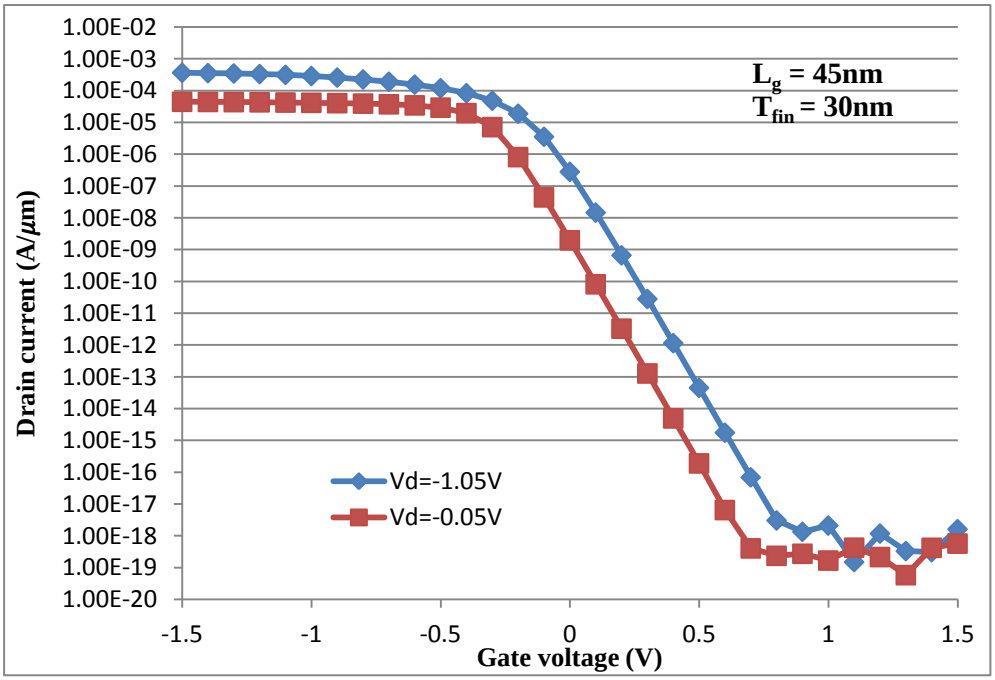


Fig. 4.8. Simulated I_d-V_g characteristics for 45-nm gate length and 30-nm thick Si body PMOS FinFET device.

4.4. Classical Dimensional Effects:

In order to achieve high performance circuits, CMOS is being pushed toward channel lengths much below in the nanometre scale. Several technological approaches have been proposed to overcome the scaling limits imposed by fundamental aspects such as very high doping, inversion layer capacitance, low carrier mobility, etc. SOI technology with ultrathin body and multiple gate architectures is an attractive solution for down scaling. A study of effect of various classical dimensions such as gate length and channel on the I-V characteristics of FinFETs is very important in evaluating the performance of these structures while scaling their dimensions in the nanometre regime. The subthreshold

characteristics depend on channel length and fin thickness. Under this section study of subthreshold characteristics of FinFET with respect to gate length (or channel length) and fin width (or channel thickness) has been presented and discussed.

4.4.1 Transfer Characteristics of FinFET for Different Gate Lengths:

Fig. 4.9 shows the variation of drain current versus gate voltage for different channel lengths ranging from 11nm to 26nm for an n-channel SOI FinFET structure with the parameters following the ITRS projections for the year 2015 [1].

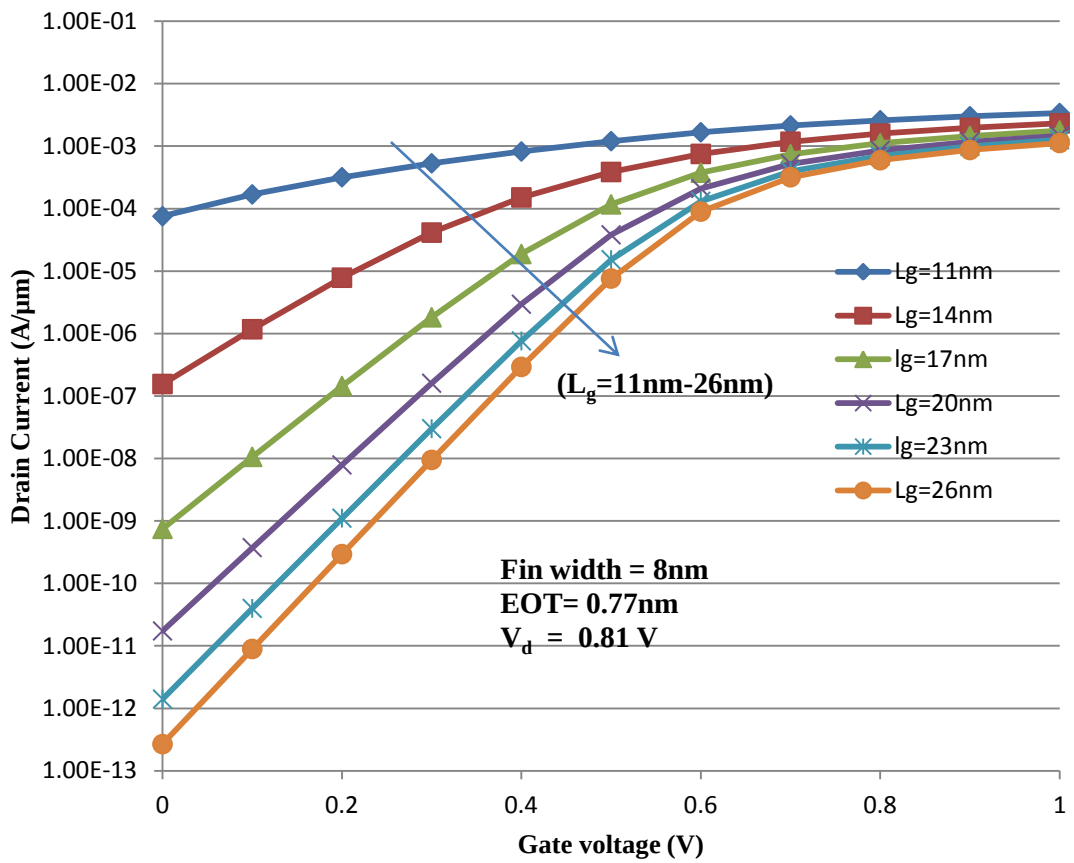


Fig. 4.9. Drain current versus gate voltage in n-channel FinFETs with different channel lengths and fixed fin width of 8nm.

The results obtained have been generated from the PADRE device simulator, wherein the various parameters of the device under taken for the simulation purpose are body or channel width = 8nm, EOT (Equivalent oxide thickness) = 0.77nm and drain bias of 0.81V as projected by ITRS for a multigate MOSFET (MuGFET) structure. The doping concentration for the channel is 7.5e18 cm^{-3} and for source/drain regions, it is 1e22cm^{-3}. From the transfer characteristics shown in figure, it is evident that with the increase in channel length the subthreshold characteristics of the device improve. At 26nm gate length, it is evident that the characteristics approach the long channel

behaviour of the device, with an improvement in subthreshold swing behavior. At smaller gate lengths approaching 11nm, it is seen that conventional short-channel Effects become too severe. It is because as the gate length, L_g decreases, the threshold voltage is lowered and the subthreshold slope degrades due to charge sharing.

4.4.2 Transfer Characteristics of FinFET for Different fin Widths:

A key advantage of SOI devices is the reduction of the short-channel effects when the body thickness or channel width decreases [179-181]. This also applies to FinFETs as illustrated in Fig. 4.10. PADRE simulations have been carried out once again for the same device parameters as described above in order to study the effect of channel or fin width variation on the transfer characteristics of the n-channel FinFET, but this time the channel length is fixed at 17nm. The channel width or fin width is varied in the range of 6nm to 16nm.

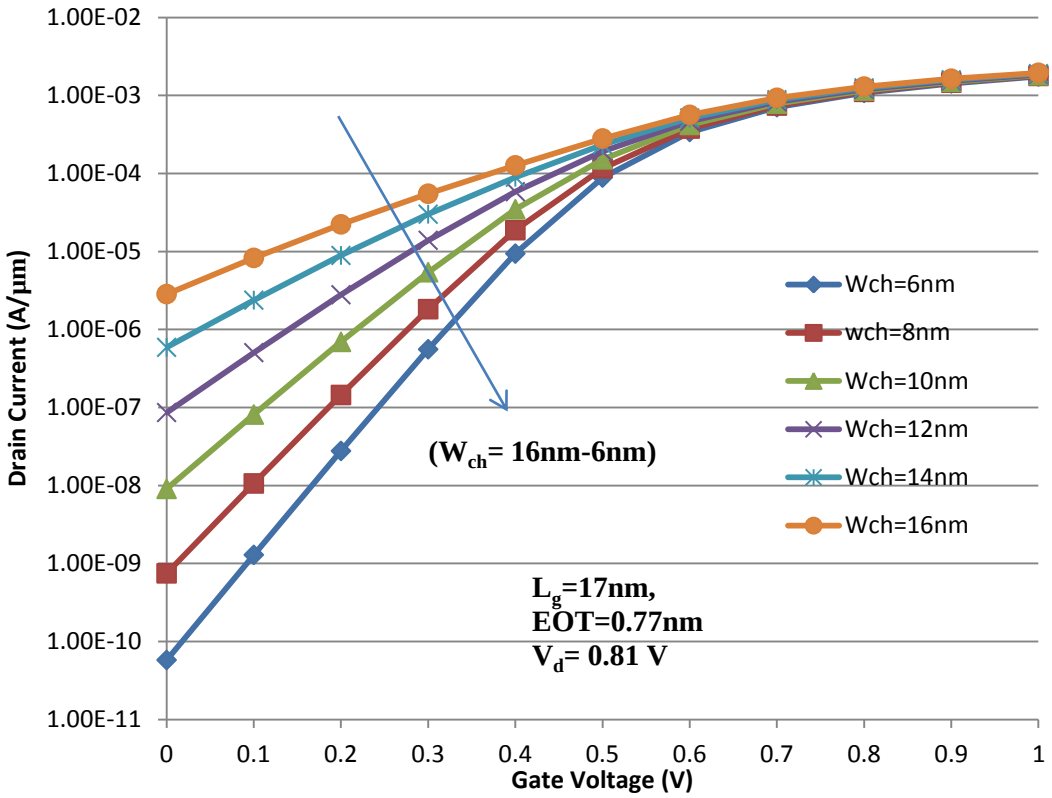


Fig. 4.10. Drain current versus gate voltage in short n-channel FinFET with variable channel width and fixed gate length of 17nm.

From Fig. 4.10, a clear improvement in subthreshold characteristics is observed as the FinFET thickness is reduced: V_{th} increases and the subthreshold slope (SS) becomes steeper. It is because the double gate control of the body potential is reinforced by the

use of thinner fins. These results have been generated by undertaking n-FinFETS. Similar trends are observed for p-channel FinFETs.

4.5. Transfer Characteristics of FinFET for Different Channel Doping Concentrations:

Fig. 4.11 shows the results PADRE simulated transfer characteristics of n-channel FinFET device for different channel doping concentrations. The device parameters undertaken for the simulation study are as per the projections made by ITRS 2010 for the year 2016 [1]. For the device structure undertaken, the gate length L_g is 15.3nm, channel width or body thickness, W_{ch} = 7.5nm, equivalent oxide thickness, EOT = 1.1nm, drain supply voltage V_{ds} = 0.78V and the gate bias, V_{gs} = 0-1 V. Further the device has been simulated for a constant drain source doping of $1\times10^{21}cm^{-3}$, and for the variable channel doping concentration of 3×10^{18} cm^{-3}, 5×10^{18} cm^{-3}, 7×10^{18} cm^{-3}, 9×10^{18} cm^{-3} and $1.1\times10^{19}cm^{-3}$.

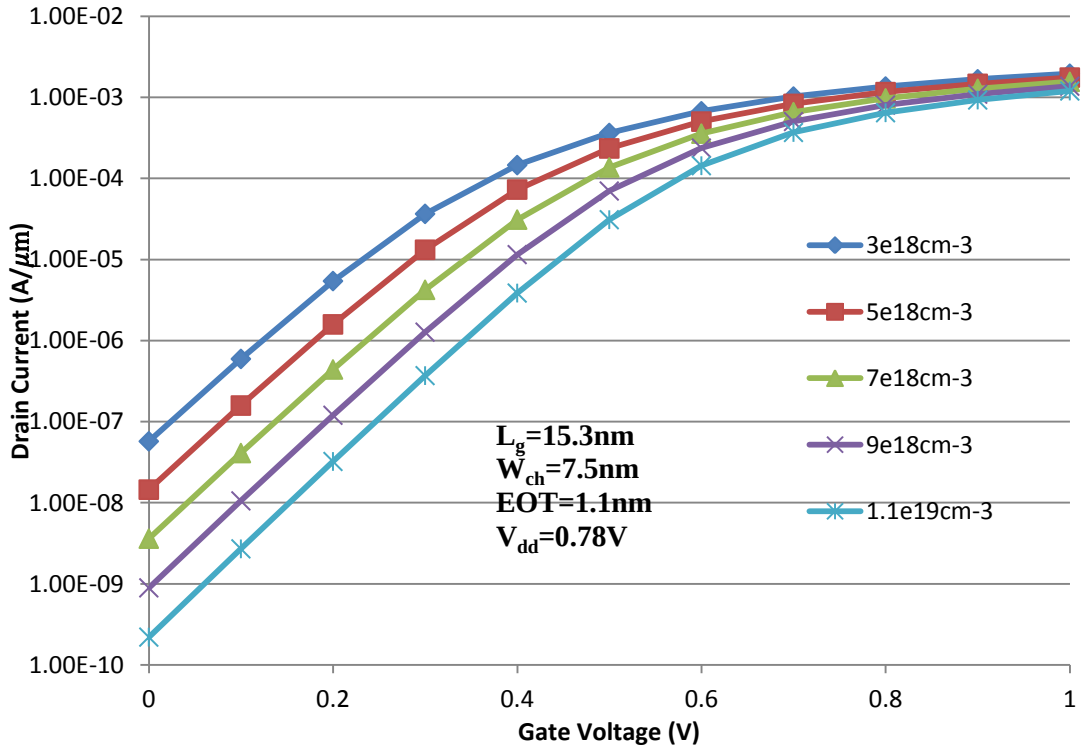


Fig. 4.11. Transfer characteristics of FinFET for different channel doping concentrations

It is seen that for high doping concentrations the on current is reduced but there is an improvement in the subthreshold characteristics of FinFET. Low channel doping increases the on current of device but at the same time there is an increase in the off-state leakages due to early threshold voltage (or threshold voltage roll-off effect) with in

these devices. It is because in case of MOS devices, the increase in channels doping increase the threshold voltage of devices but reduces the carrier mobility of these devices [3].

4.6. Transconductance characteristics of FinFET:

Transconductance is an analog circuit design parameter that relates the drain current to the gate voltage of a MOS device and represents the effectiveness of the drain current control by the gate bias. It describes how efficiently a small signal at the gate terminal is converted into a drain current signal. It is worthwhile to mention that the transconductance of MuGFET device has been found to be slightly lower than that of the bulk MOSFET device mainly due to the high parasitic source/drain resistance [2]. The transconductance characteristics of FinFET device are as shown in Fig. 4.12. These characteristics have been obtained from the PADRE simulation of an experimentally fabricated p-MOS FinFET device in [10]. The various parameters undertaken for the simulation are as per the reference [10], wherein the gate length, L_g=45nm, channel width, W_{ch}=30nm and oxide thickness=2.5nm. The doping concentration in the body has been kept fixed at 1×16 cm^{-3}. Further the device has been simulated for a drain bias of -1.05V and for a gate bias in the range of -1.45V to +1.45V.

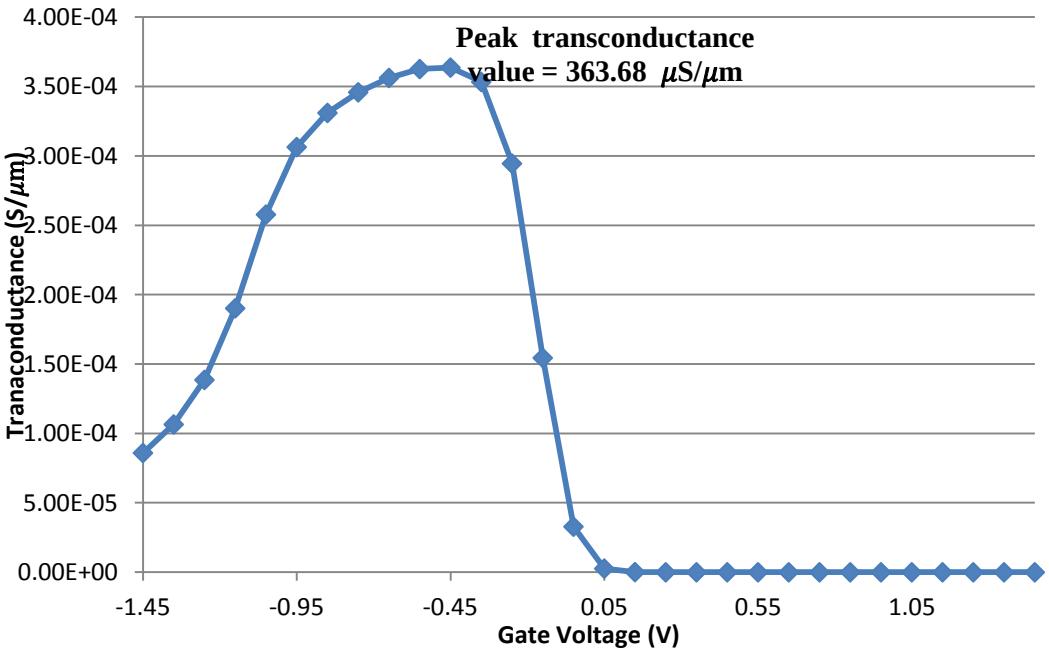


Fig. 4.12. Simulated Transconductance versus Gate voltage of a p-MOS FInFET device.

4.6.1. Effect of Gate Length Variation on Transconductance Characteristics of FinFET:

Fig. 4.13 shows PADRE simulation results of transcoductance versus gate voltage of n-channel FinFET device for various gate lengths (14, 17, 20 and 23nm). The device has been simulated with the parameters taken as per the ITRS-2010 projection report for the year 2015 [1]. The various parameters undertaken for the simulation purpose are channel width, W_{ch}=7.5nm, equivalent oxide thickness, EOT=1.1nm, drain supply voltage of 0.78V and for the gate bias of 0V-1V. Furthermore the channel doping concentration is $1\times10^{17}cm^{-3}$, while as the drain/source doping has been fixed at 1×10^{21} cm^{-3}. It is observed from figure that transconductance decreases with the increase in channel length of FinFET device. This is due to the fact that the carrier mobility in the channel is reduced with the increase in channel length of the device. In case of shorter channel length devices, the carrier mobility is larger which results in higher transconductance and drive current of the device, however the critical short channel effects impinge to deteriorate the device characteristics.

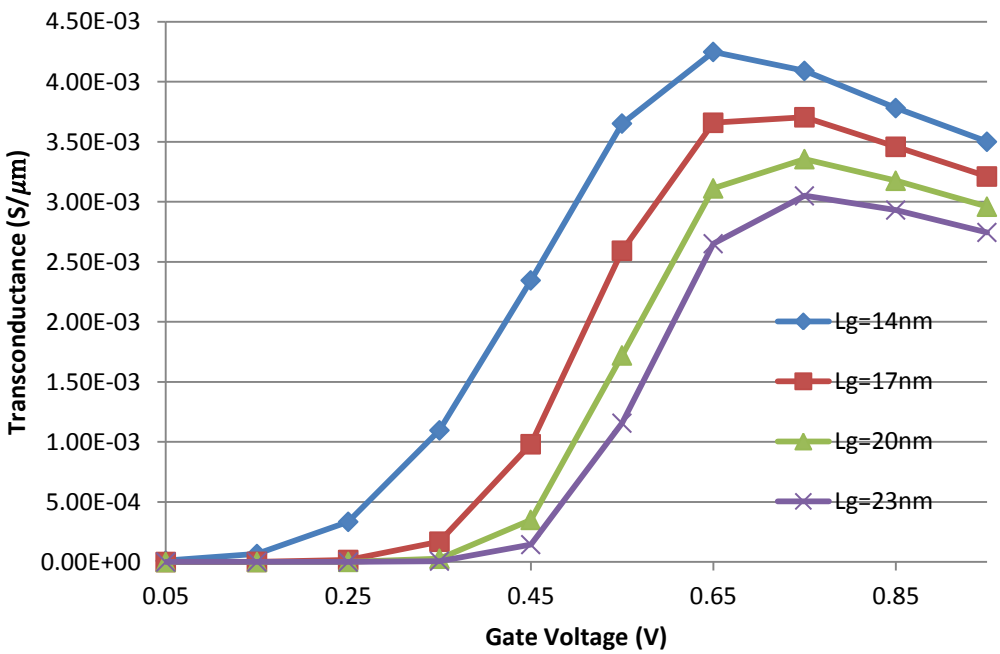


Fig. 4.13. Transconductance versus gate bias for different channel lengths.

4.6.2. Effect of Channel Width Variation on Transconductance Characteristics of FinFET:

Fig. 4.14 shows the PADRE simulation results of transconductance characteristics of n-channel FinFET device for different channel width variations (W_{ch}= 5nm, 8nm, 11nm). The device parameters undertaken for the simulation study are as per the projections

made by ITRS 2010, wherein gate length, L_g = 15.3 nm, Equivalent Oxide Thickness, EOT = 1.1 nm [1]. The device has been simulated for drain supply voltage of 0.78 V and for gate bias of 0 V-1V. Further the device has been simulated for a constant drain source doping of $1\times10^{21}cm^{-3}$, and for a constant channel doping concentration of 1×10^{17} cm^{-3}. From the transconductance plots it is clear that with a decrease in fin width of FinFET, the transconductance degrades. The reason behind it is that with a decrease in fin width of FinFET or ultrathin body devices the large parasitic source drain resistance degrades the device current drive and hence transconductance and mobility [178]. However as discussed earlier a decrease in fin width results in better short channel performance of the device, due to the more effective channel electrostatic control of the device.

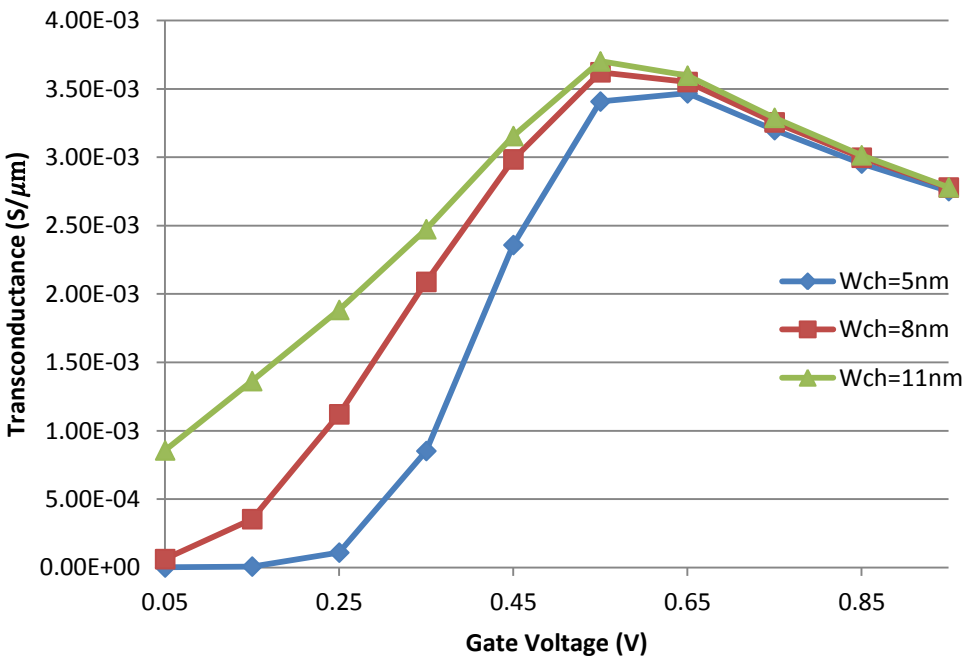


Fig. 4.14. Transconductance versus gate bias for different channel widths.

4.7. Effect of fin Size and Cross-Sectional Shape on Output Conductance and Transconductance of FinFET:

Simulation study of various analog parameters with respect to different fin cross-sectional shapes of triple gate trapezoidal FinFET device has been presented in [120]. Trapezoidal triple gate devices with same average fin widths and cross-sectional areas of fins, but with different inclination angles are obtained in two ways: In the first case, the base width is maintained constant and the top width is ranged. In the second part, the top width is maintained constant and the base width is ranged. The simulated devices are

fully depleted triple-gate FinFETs, with channel doping levels of $N_A = 1\times10^{15}\text{cm}^{-3}$ and $N_A = 1 \times 10^{17}\text{cm}^{-3}$, gate-oxide thickness of 2nm, fin height (H_{Fin}) of 50nm and buried oxide thickness of 100nm. The $W_{\text{Average FinWidth}}$ (W_{AFW}) ranges from 40 nm to 60 nm in devices with the channel length equal to 200 nm and 1 μm, and from 20 nm to 40 nm in devices with the 50nm channel length. The metal gate material (TiN) has been used with a workfunction of 4.63eV. Furthermore the drain current is normalized by the shape factor (W/L).

4.7.1. Output Conductance:

Fig. 4.15 shows the plot of output conductance, g_d versus average fin width, W_{AFW} for V_{DS} = 600 mV. It is observed that output conductance is higher for wider channels. The plot shows that from both sets, the 60 nm W_{AFW} have the highest output conductances. This result is related to the channel susceptibility to the drain potential. The wider is the channel, the smaller is the channel immunity against the potential influence from drain

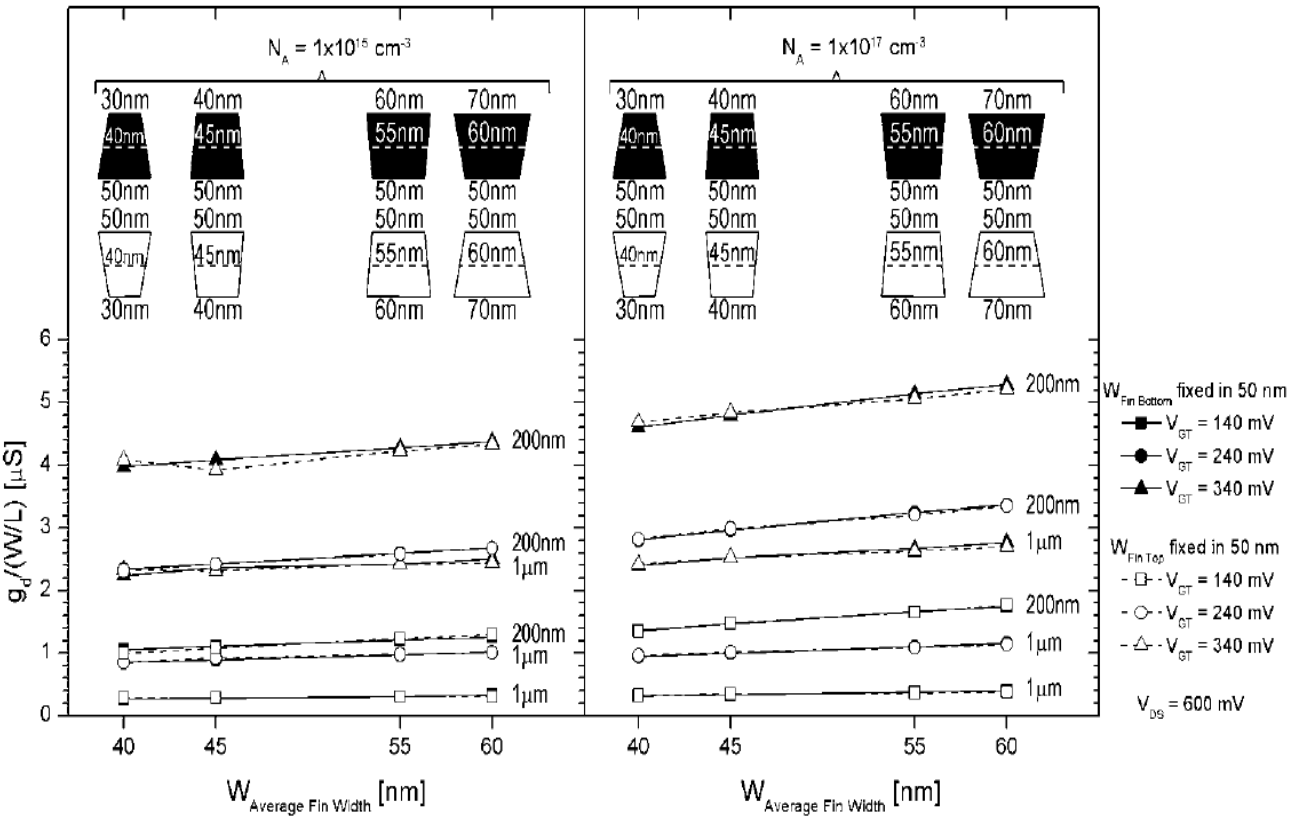


Fig. 4.15. FinFETs output conductance as a function of the average fin width for channel lengths of 200 nm and 1 μm, and for doping concentrations of $N_A = 1\times10^{15}$ cm^{-3} and $N_A = 1\times10^{17}$ cm^{-3} [120].

junction. Comparing both sets, it becomes clear that this parameter is quite independent of the lateral gate inclination angle, for each average fin width. Similar effects can be observed independently if the wider channel part is on the top or at the bottom. This behavior is observed for all overdrive voltages. The g_d values are lower on longer channel (1 μm) devices due to the lower significance of the drain influence region in the total channel length.

4.7.2. Transconductance:

The transconductance has been evaluated for the same devices simulated for the output conductance analysis, with a drain voltage (V_{DS}) bias of 600 mV. Data has been extracted from the derivative of drain current as a function of the gate voltage (g_m = dI_{DS}/dV_{GS}). Fig. 4.16 shows the transconductance as a function of the gate voltage, for undoped (N_A = 1×10^{15} cm^{-3}) and for doped (N_A =1×10^{17} cm−3) devices. Fig. 4.17 shows g_m for the same gate overdrive voltages considered in the output conductance analysis, as a function of W_{AFW}.

Differently to the output conductance (g_d) case, the transconductance is a function of the sidewall inclination angle, what can be observed by comparing both sets, for each W_{AFW}. Transconductance relates the drain current to the gate voltage and represents the effectiveness of the current control by the gate. The conduction charge availability in the channel region is subjected to the electric potential distribution, which is strongly dependent on the boundary conditions. For a long-channel device, there are two main boundaries with constant potentials: the set of gate planes and the substrate plane. Consequently, considering that the substrate is always grounded, the amount of the available conduction charge for a given gate voltage depends on how strongly the channel region is coupled to the gate planes or to the substrate. As the top width is increased, the channel charges become better coupled to the gate and less coupled to the substrate, mainly near the corners, where the corner effect becomes stronger [184], and so, the current will be better controlled by the gate (higher transconductance). As $W_{Fin,top}$ is decreased, the channel is more exposed to the substrate potential, and so the transconductance is degraded. This geometric effect occurs for any doping level, but is stronger for highly doped devices. Devices with longer channels (1 μm) have also been simulated and have presented the same trends.

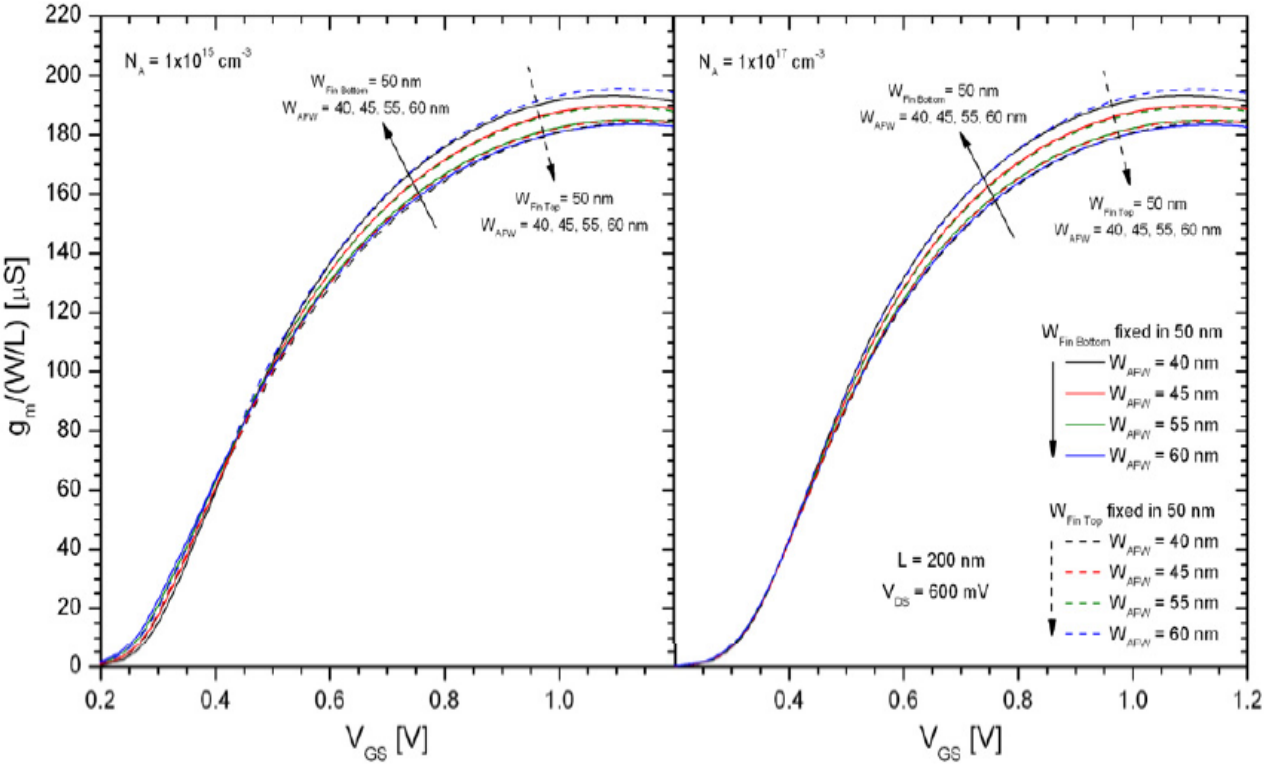


Fig. 4.16. FinFETs transconductance as a function of drain voltage for channel lengths of 200 nm and for doping concentrations of $N_A = 1\times10^{15}$ cm^{-3} and $N_A = 1\times10^{17}$ cm^{-3} [120].

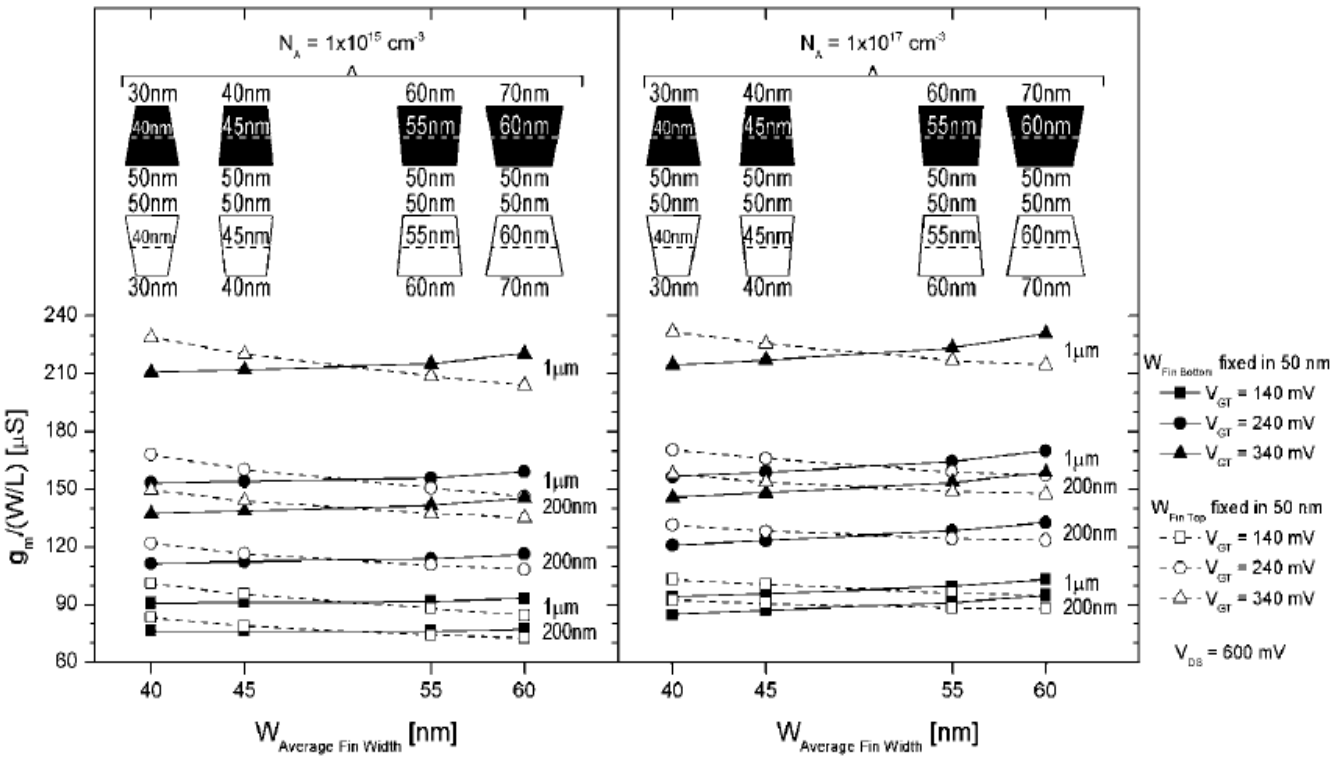


Fig. 4.17. FinFETs transconductance as a function of the average fin width for channel lengths of 200 nm and 1 μm, and for doping concentrations of $N_A = 1\times10^{15}$ cm^{-3} and $N_A = 1\times10^{17}$ cm^{-3} [120].

4.8. Coupling Effects in FinFET (front conduction modulated by the back gate):

The coupling between the front and back gates is a well known phenomenon in fully depleted SOI MOSFETs [182] that allows to studying the properties of the two interfaces. The coupling effect is also visible in FinFETs, where the critical parameter is the fin thickness. A study based on the coupling effects in FinFETs has been carried out in [88], wherein the front channel as well as the two lateral channels is modulated by the back gate. Reciprocally, it is also possible that the back-channel characteristics are modulated by the top gate, enabling differed activation of the four channels.

A FinFET can be operated with two, three and even four channels when the substrate is biased in inversion. In Figures (4.18–4.20), the evolution of the drain current and the transconductance of top gate for different fin thickness and back-gate bias (from 60 to +60 V with 10V step) of an n-channel FinFET with a fixed value of fin height, H_{fin} (≈100nm) has been presented [88]. In these results, it is difficult to de-correlate the front and lateral conduction because they both coexist. There is a clear influence of the back gate: lateral shift of the characteristics and hump on transconductance (g_m) due to the gradual activation of the back channel. In thick devices (Fig. 4.18), the coupling between front and back channels is strong and back channel conduction appears (Fig. 4.18a). The degradation of the transconductance peak, when the back interface is driven into accumulation (Fig. 4.18b), is a natural effect resulting from the increase of the vertical field [183].

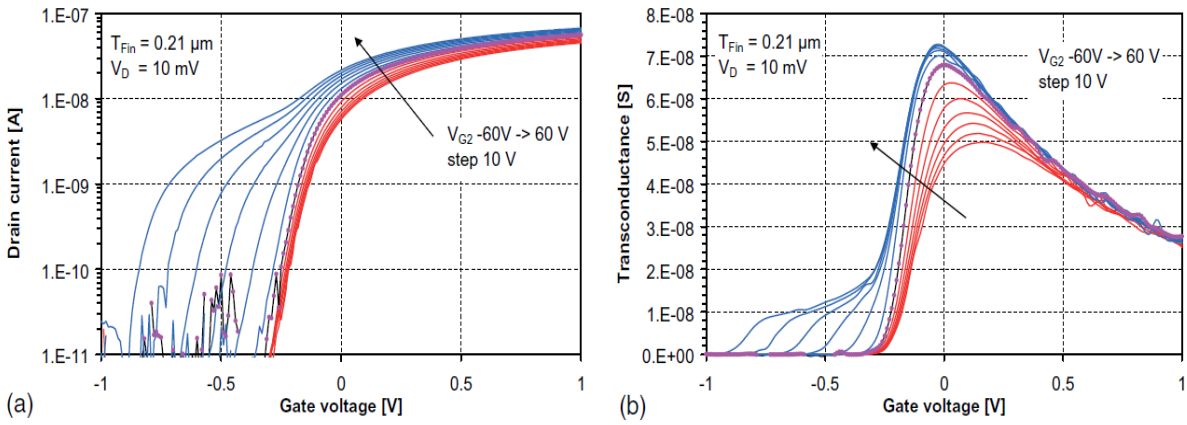


Fig. 4.18. Drain current (a) and transconductance (b) versus top-gate voltage in a relatively thick N-channel FinFET for variable backgate bias (T_{fin}= 0.21 µm, L_{fin} = 10 µm, V_D = 10 mV, V_{G2} = -60 to 60 mV with step 10 V). Coupling effects are strong [88].

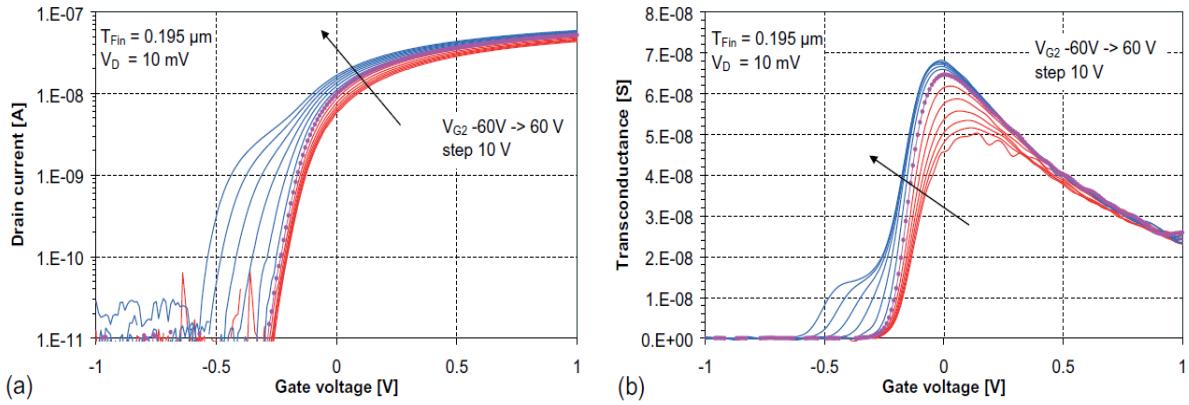


Fig. 4.19. Drain current (a) and transconductance (b) versus top-gate voltage in n-channel FinFET for variable back-gate bias (T_{fin}= 0.195 µm, L_{fin} = 10 µm, V_D = 10 mV, V_{G2} = -60 to 60 mV with step 10 V). Coupling effects are lower than in Fig. 4.18 [88].

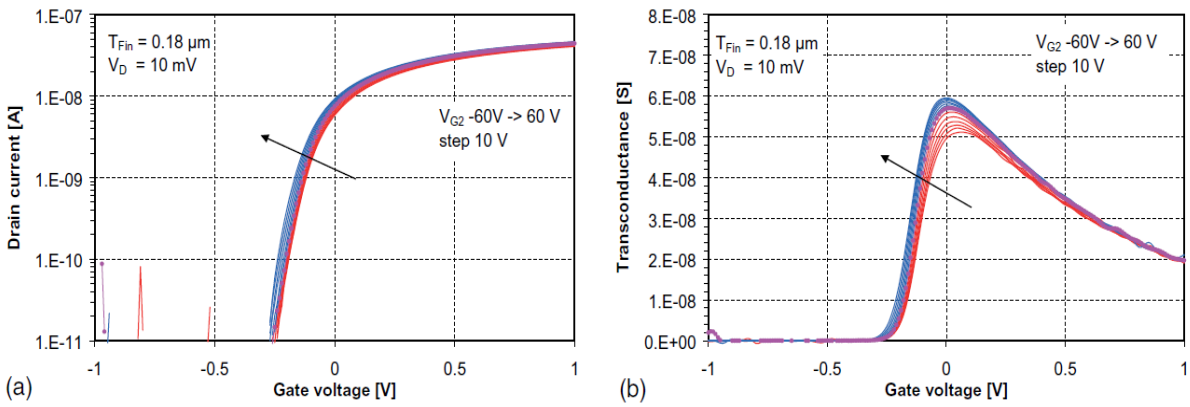


Fig. 4.20. Drain current (a) and transconductance (b) versus top-gate voltage in a relatively thin n-channel FinFET for different backgate bias (T_{fin}= 0.18 µm, L_{fin} = 10 µm, V_D = 10 mV, V_{G2} = -60 to 60 mV with step 10 V). Coupling effects are vanishing [88].

As the fin thickness decreases, the back conduction and coupling effect are reduced: more limited lateral shift (Fig. 4.19a) and transconductance hump (Fig. 4.19b). For the thinnest FinFET (Fig. 4.20a and b), the coupling almost disappears and only the main conductions, lateral and front channels, coexist mixing together. The impact of back-gate bias is strongly lowered due to the reduction of the aspect ratio (fin thickness T_{fin} versus film thickness H_{fin}). The back channel is suppressed (Fig. 4.20a) and the modulation of the transconductance peak (Fig. 4.20b) is limited to 10–15% [88].

These results imply that, in very thin fins, the back gate loses the control of the potential at the film–BOX interface. There are two main reasons: (1) the back surface potential tends indeed to be governed by fringing fields penetrating from the bottom of the lateral gates into the body and BOX. (2) The lateral interfaces being very close to each other, their mutual coupling becomes stronger than the vertical coupling. Hence,

the lateral conduction appears earlier and controls the front and back surface potentials, which tend to de-correlate [88].

4.9. Conclusion:

Theoretical and experimental study of I-V characteristics of various FinFET device structures as carried out by various authors has been presented. Some experimentally fabricated structures have been undertaken for simulation, wherein it has been found that the simulation results obtained are in good agreement with those of experimental results. The effect of various scaling and process parameters on the device I-V characteristics of FinFET has been studied. From the simulation study of I_d-V_d characteristics, it has been found that drain current increases with the decrease in gate length, L_g of the device due to the reduction in channel resistance of the device. An improvement in subthreshold characteristics has been observed as the fin width decreases due to increase in multiple gate control of the device. While studying doping concentration effects, it has been observed that for higher doping concentration of fin body the device on current is reduced but an improvement in subthreshold characteristics is obtained.

Transconductance characteristics have been presented and the effect of gate length and fin thickness on transconductance characteristics have been simulated and presented. It has been observed that transconductance degrades with an increase in gate length due to reduced carrier mobility in long channel devices. An improvement in transconductance characteristics has been observed for wider fin devices due to reduced parasitic source /drain resistance of device.

Effect of fin size and cross sectional shape on output conductance and transconductance of FinFET as carried out by some authors have been presented. From this study, it has been observed that output conductance, g_d values are lower in long channel devices due to lower significance of drain influence region in the total channel length. Furthermore the study of transconductance, g_m with respect to various fin sizes and shapes reveals that for a trapezoidal fin structure, as the top fin width is increased, the channel charges become better coupled to the gate and less coupled to the substrate, and so the current will be better controlled by the gate (higher transconductance). As $W_{Fin,top}$ is decreased, the channel is more exposed to the substrate potential, and so the transconductance is degraded.

Coupling effects in FinFETs, as studied by some authors has been presented. From this study, it has been observed that it is difficult to de-correlate the front and lateral conduction because they both coexist. There is a clear influence of the back gate: lateral shift of the characteristics and hump on transconductance (g_m) due to the gradual activation of the back channel.

Chapter 5
Short Channel Effects (SCE's) in FinFET Structures

5.1. Introduction:

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length of metal–oxide–semiconductor (MOS) devices is reduced to increase both the operating speed and the number of components per chip, the so-called short-channel effects (SCE's) arise.

It has been reported in the article referenced [185] that beyond 20nm logic node, conventional planar transistors could run out of gas. At 14nm, the industry will require a new transistor structure. So in order to keep pace with the scaling trend of transistors next-generation transistor candidates need to switch over to multi-gate MOS (FinFET), fully-depleted silicon-on-insulator (SOI), 3D devices, among others. Despite various fabrication challenges of FinFET (precise etching of fins without surface states, introduction of parasitic capacitances due to 3D structure, over etch time required for removing residues from corners), FinFET has been considered as "strong candidate" beyond 20nm node that has excellent short-channel performance and is being continuously researched to follow projections of ITRS [1]. Furthermore, it is worthy to mention that among the multi-gate transistors, FinFET has been the most widely researched because of its compatibility with the conventional fabrication process.

Various SCE's that impinge the device electrical characteristics in the nanometer regime are: threshold voltage (V_t) roll-off, Drain Induced Barrier Lowering (DIBL) and Subthreshold Slope (SS). Under this chapter, these short channel effects have been first theoretically discussed, following which a study of these short channel effects with respect to various scaling and process parameter variations (gate length, fin width and fin height, channel doping concentration). For the simulation study carried out in this chapter most of the device parameters of FinFET have been taken as per the projections made by ITRS, while only few of them are user defined. Furthermore the corner effects of FinFETs due to parasitic channel conduction around corners of the fin body have been discussed based on the work carried out by some authors in the field. The presence of kink effect in transfer characteristics and the multiple threshold voltages of the FinFET device due to these corner effects have been discussed.

5.2. Threshold Voltage Adjustment:

Threshold voltage is an important parameter in novel MOS device structures which needs to be adjusted carefully as per the requirement of the device application. For instance high speed switching applications require that the threshold voltage should be lower, but at the same time the critical off state leakages can reduce the device performance. On the other hand LSTP logic technology refers to chips of lower-performance, lower-cost consumer type applications, such as consumer cellular telephones, with lower battery capacity and an emphasis on the lowest possible static power dissipation, i.e., the lowest possible leakage or off-current (highest threshold voltage, V_t). There are difficult challenges to keep the leakage current within tolerable range as predicted by ITRS [1], while at the same time maintaining a higher threshold voltage requirement in these device structures. In case of extremely scaled devices, within the tiny volume of the Si channel, even a small variation in the number of impurity atoms will have a very significant impact on the effective doping density. Hence, according to the classical relationship between the threshold voltage and doping density, controlling, V_t very precisely will remain a challenging task and likely become a critical issue due to doping density fluctuation. Furthermore, continuous scaling of classical bulk-Si and partially depleted (PD) SOI MOSFETs requires precise channel doping levels and gradients in order to control short-channel effects [186], [187]. However, whether the classical theory for the dependence of V_t will continue to hold is questionable. Although some researchers have addressed this issue, they mainly focused on the conventional high doping strategy for controlling V_t. To extend the scaling limits for CMOS technologies, advanced fully depleted (FD) SOI and multi-gate MOSFETS with undoped or low-doped ultra-thin body have emerged. Though use of channel doping may not seem to be a preferable scheme to achieve proper device characteristics for advanced devices since a metal gate with proper work function could be more effective and has been demonstrated [188-190], still the unwanted impurity atoms within the small volume of the extremely scaled devices could introduce a substantial variation in effective doping. Therefore, it is still of interest to investigate the doping sensitivity for nanoscale MOS devices.

The threshold voltage expression for advanced MuGFET device structures can be expressed as

$$V_t = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} + v_{in} \qquad (1)$$

where Q_{in} represents charges in the gate dielectric, c_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, Φ_{ms} represents metal-semiconductor work-function difference between the gate electrode and the semiconductor, Φ_f is the fermi potential given by

$$\Phi_f = \frac{kT}{q} ln(\frac{N_D}{n_i}) \qquad (2)$$

where N_D and n_i are donor concentration in channel and intrinsic carrier concentration respectively.

For ultrathin body and lightly doped devices, in addition to N_D, the effect of Q_D and Q_{ss} on threshold voltage, V_t in equation (1) is negligible compared to Φ_f. Further v_{in} is the additional surface potential to $2\Phi_f$ that is needed for ultrathin body devices to bring enough inversion charges in to the channel region of the transistor to reach threshold point. Therefore the work-function of gate electrode is the main parameter for threshold voltage determination in case of MuGFET devices [2].

5.2.1 Threshold Voltage Variation with fin Doping Concentration:

In case of extremely scaled devices like FinFET, the threshold voltage has been found insensitive to channel doping concentration except at very high concentration. S. Xiong and J. Bokor have observed less than a 50mV shift of the threshold due to the channel doping up to 5×10^{18} cm^{-3} for a double-gate device with 20–nm gate length and 5-nm body thickness. On the other hand, excessive impurity concentrations can significantly degrade the mobility of carriers, and that the statistical spread of the threshold voltage could be very large due to random placement of discrete impurities in the channel. PADRE simulation results of threshold voltage variation with channel doping concentration obtained for an n-FinFET with parameters undertaken as per projection report of ITRS-2010 for High Performance logic technology are as shown in Fig. 5.1. To be mentioned, the various device parameters used for the simulation set up are gate length, L_g=17nm, channel width, W_{ch}=8nm, gate oxide thickness, t_{ox}=0.77nm, source/drain doping of 1×10^{22} cm^{-3}.

It is observed from the characteristics that threshold voltage is insensitive to channel doping up to $1\times10^{18}cm^{-3}$ and the variation is almost flat for doping concentrations below 1×10^{18}. As has been already discussed such large doping concentration in case of ultrathin device structures can significantly degrade the mobility of carriers, and the statistical spread of the threshold voltage could be very large due to random placement

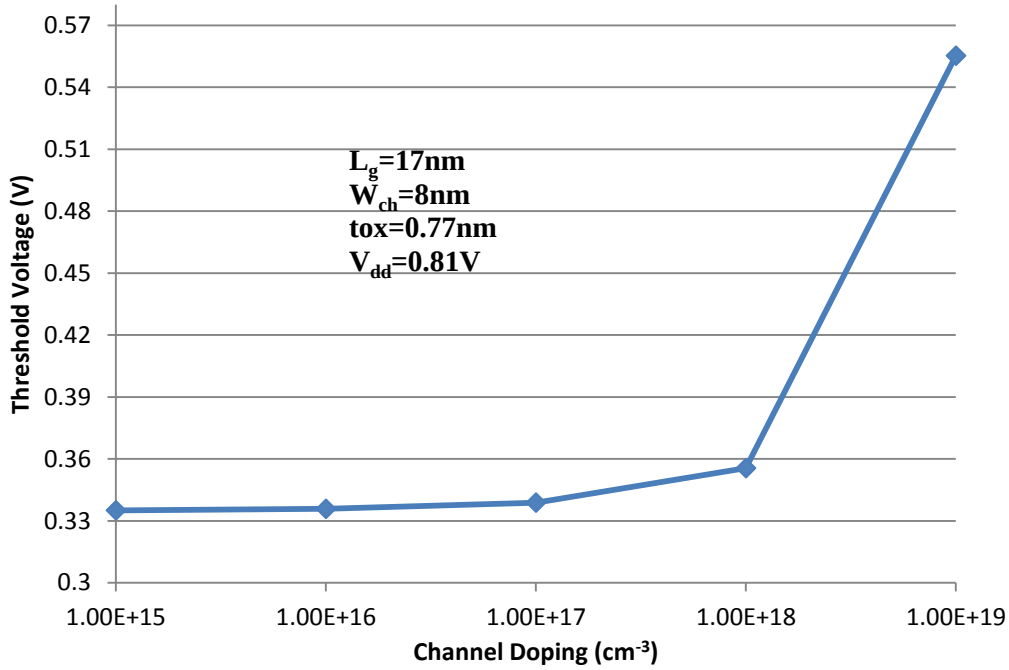


Fig. 5.1. Simulated threshold voltage versus channel doping concentration for n-FinFET.

of discrete impurities in the channel. The same macroscopic doping profiles will differ microscopically. Both the fluctuation in the number of channel dopants and their placement may cause significant device-to-device performance variation.

5.2.2. Bandgap Narrowing Effect Due to Increased Channel Doping in Extremely Scaled MOS Devices:

As discussed in preceding section, in case of extremely scaled MOS devices, the threshold voltage is in fact, insensitive to doping over a wide range of doping density. A study carried out by authors in reference [187] has shown that while studying the fundamental V_t issue and its physical insight into the impact of the doping density on device characteristics, it has been found that such insensitivity is further extended by bandgap narrowing in nanoscale MOSFETs. The authors have examined this insight by performing simulations for double gate (DG) devices of three gate lengths (50, 25 and 10 nm) with different (physical) oxide thicknesses (2, 1.4 and 0.9 nm) and film thicknesses (10, 7 and 5 nm), which were designed to meet the criteria defined in the ITRS roadmap. Fig. 5.2 shows the simulated V_T versus N_A for the symmetrical-gate DG devices. As aforementioned, they are virtually insensitive, especially for low N_A values. In contrast to conventional devices, I_{off} (or V_T) of the DG devices are still reasonable over the range

of very low N_A values (~10^{16} cm^{-3}). More interestingly, V_T of the highly scaled case (10 nm) is virtually insensitive.

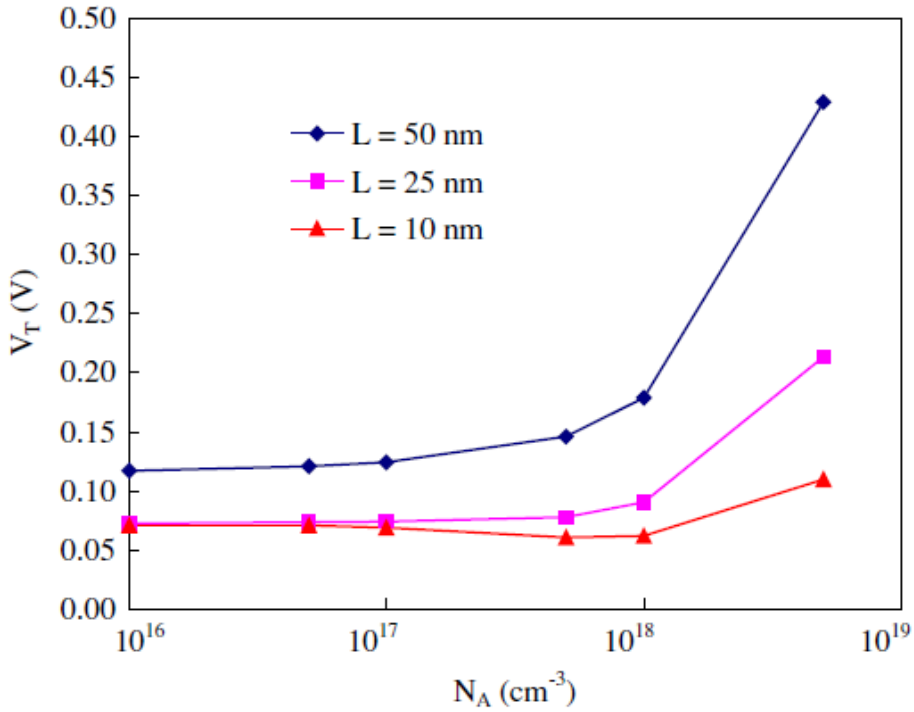


Fig. 5.2. Simulated V_T versus N_A for DG-nMOSFETs (@ V_{DS} = 50 mV). The V_T characteristics are nearly flat (insensitive) for low N_A (<10^{17} cm^{-3}) [187].

In Fig. 5.2, the nonmonotonic V_T of the 10 nm device (slightly lower V_T around N_A of 10^{18} cm^{-3}), which is caused by the counter effect of bandgap narrowing (V_T lowering), is further demonstrated in Fig. 5.3. Due to heavy doping, the shift (ΔE_g) in band edge can be included as variations in the intrinsic concentration n_i as

$$n_{ie} = n_i \exp(\Delta E_g)$$

where n_{ie} is the effective intrinsic concentration. Consequently, the reduced bandgap lowers the required gate voltage for turning on the MOSFET channel, thereby lowering V_T. On the other hand, V_T increases as the doping level increases following the classical doping dependence of V_T. The two opposite V_T –N_A trends result in the nonmonotonic phenomenon of threshold voltage, V_T. Without accounting for bandgap narrowing in the simulation, such a phenomenon disappears, as indicated in Fig. 5.3. In contrast to the 10 nm device, other larger DG devices as well as conventional devices (discussed earlier) do not show obvious nonmonotonic V_T because the classical doping dependence of V_T is overwhelming.

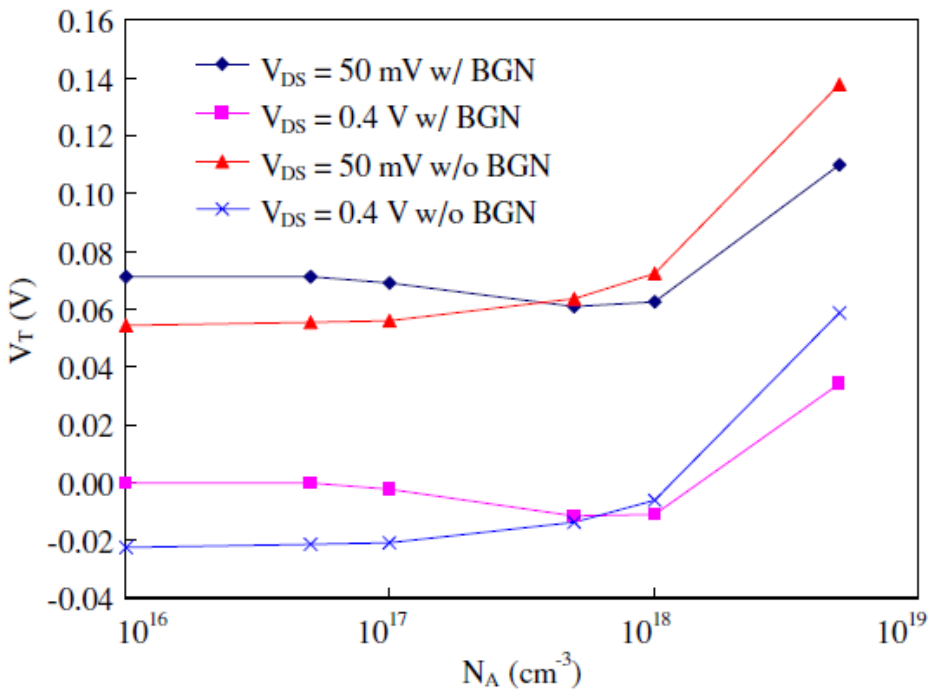


Fig. 5.3. Simulated V_T versus N_A for the 10 nm DG-nMOSFET with and without bandgap narrowing (BGN) included. The results with Band Gap Narrowing show the nonmonotonic N_A dependence [187].

Further it should be noted that, in Fig. 5.3, with bandgap narrowing the predicted V_T is considerably higher for low N_A values than without bandgap narrowing. Such an anomaly is from the bandgap narrowing effects in source/drain; the reduced source/drain bandgap due to the high doping level (2×10^{20} cm^{-3}) tends to increase the source-to-channel barrier (~heterostructure) and hence increases V_T.

5.2.3. Variation of Threshold Voltage with Gate Work-function:

Fig. 5.4 shows plot of threshold voltage variation with gate work-function for an n-FinFET. The various parameters of device structure undertaken for the present study are as per the projection report of ITRS 2010 projected for the year 2015, wherein gate length, L_g = 17nm, channel width, W_{ch} = 8nm, EOT = 0.77nm, body doping = 7.5 × $10^{18}cm^{-3}$. The device has been simulated for drain bias of 0.81V, and for a gate bias of 0-1V. PADRE simulations show that threshold voltage increases with increasing gate work-function. In our simulations we have used a poly-gate with gate work-function varying from 4.46-4.71eV. In fabrication process it is possible to adjust the gate work-function by properly doping the gate material (n^+ in case of n-channel MOS and p^+ in

case of p-channel MOS) to a desired level to attain some given value of gate work-function.

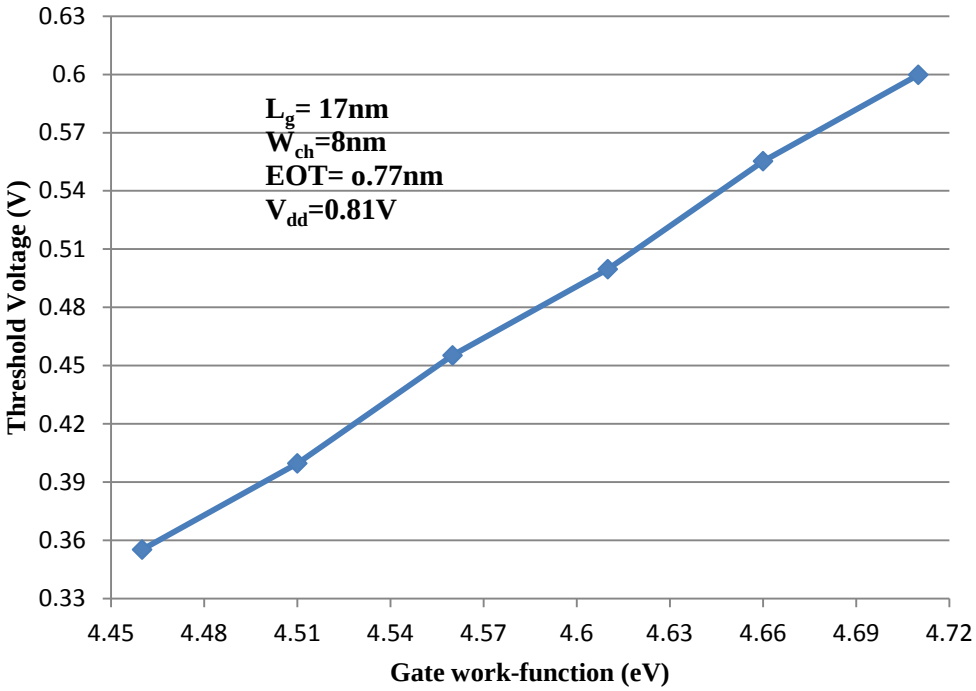


Fig. 5.4. Simulated threshold voltage versus gate work-function in double gate n-FinFET structure.

5.2.4. Effect of Gate Work-function Variation on Threshold Voltage and Device Characteristics:

A new body tied triple gate FinFET(called bulk FinFET) which has different gate work-functions on top- and side-channel regions has been proposed by authors in [114]. The authors have studied the effect of gate work-function on the characteristics of bulk FinFET, wherein it has been found that by increasing the top-gate work-function (Φ_{TG}) at a fixed side-gate workfunction (Φ_{SG}) of the bulk FinFET, threshold voltage (V_{th}) increases and off-state leakage current (I_{off}) reduces significantly without increasing doping concentration of the fin body. The bulk FinFETs with the low body doping and the threshold voltage controlled by midgap-gate work-function has shown very small dependence on the corner shape, but shows very poor short channel effect (SCE). Furthermore, it has been shown that devices with the V_{th} controlled by body doping shows significant corner effect and the effect becomes small as the fin width decreases.

Fig. 5.5 shows drain current–gate voltage (I_d–V_{GS}) characteristics as parameters of Φ_{TG} and $\Phi_{SG.}$ When the Φ_{SG} is 4.17 V, the threshold voltage (V_{th}) and subthreshold slope (SS) slightly increase with increasing the $\Phi_{TG.}$ For a given Φ_{SG} of 4.71V, the V_{th}

decreases significantly as the Φ_{SG} decreases to a value less than 4.71V. In this case, I_{on} is small at even Φ_{TG} of 4.17V because of high V_{th} of the side channel. These characteristics have been rearranged in Fig. 5.6 in terms of V_{th} and SS.

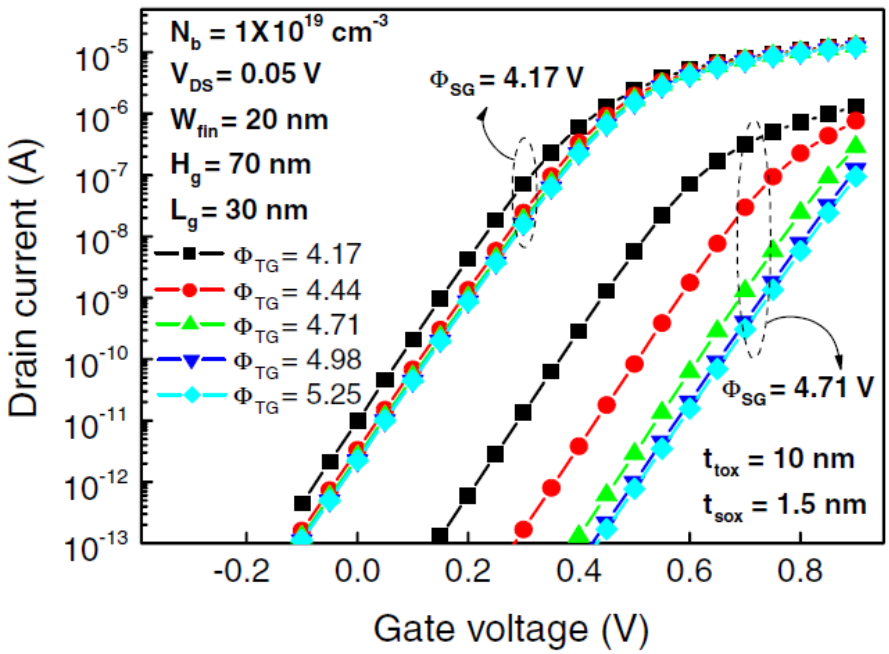


Fig. 5.5. log I_d–V_{GS} of bulk FinFET as parameters of top-gate work-function (Φ_{TG}) and side-gate work-function (Φ_{SG}) [114].

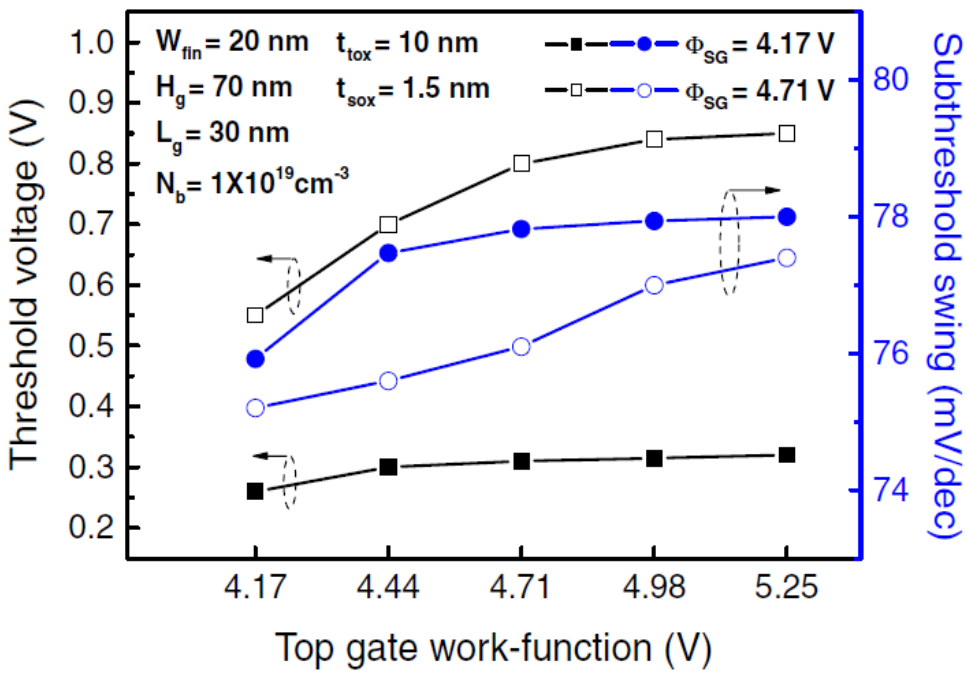


Fig.5.6. V_{th} and SS of bulk FinFET vs Φ_{TG} as a parameter of the Φ_{SG} [114].

At a first glance, it seems that the Φ_{TG} increase gives negative effect on the device performance by increasing SS. But it is not true, and the reason for this effect is that the V_{th} of the corner channel is lower than that of the side channel because the electric field from the top- and the side-gates focus on the corner region. But as Φ_{TG} increases, the V_{th} in the corner region increases, and then the contribution from the side channel device becomes appreciable depending on the Φ_{TG} value. Thus the increase of the SS with increasing Φ_{TG} in Fig. 5.6 means that the contribution from the side channel becomes large in the terminal device characteristics. At a fixed Φ_{SG} of 4.71V in Fig. 5.6, keeping $\Phi_{TG} < \Phi_{SG}$ lowers the V_{th} and increases the I_{off}. These data mean that the Φ_{TG} needs to be larger than ΦSG to guarantee low I_{off} when we use the side channel as a main channel [114].

Fig. 5.7 shows the transconductance, g_m of the bulk FinFET with the body doping concentration of 1×10^{19} cm^{-3}. The figure shows the g_m versus gate bias for given side-gate work-functions of 4.17, 4.44, and 4.71V at a fixed Φ_{TG} of 4.17 V. It is clearly observed that the g_m humps due to the earlier corner channel conduction as represented by dashed circle, when the Φ_{SG} is higher than the Φ_{TG}. For example, n^+ poly-Si top-gate

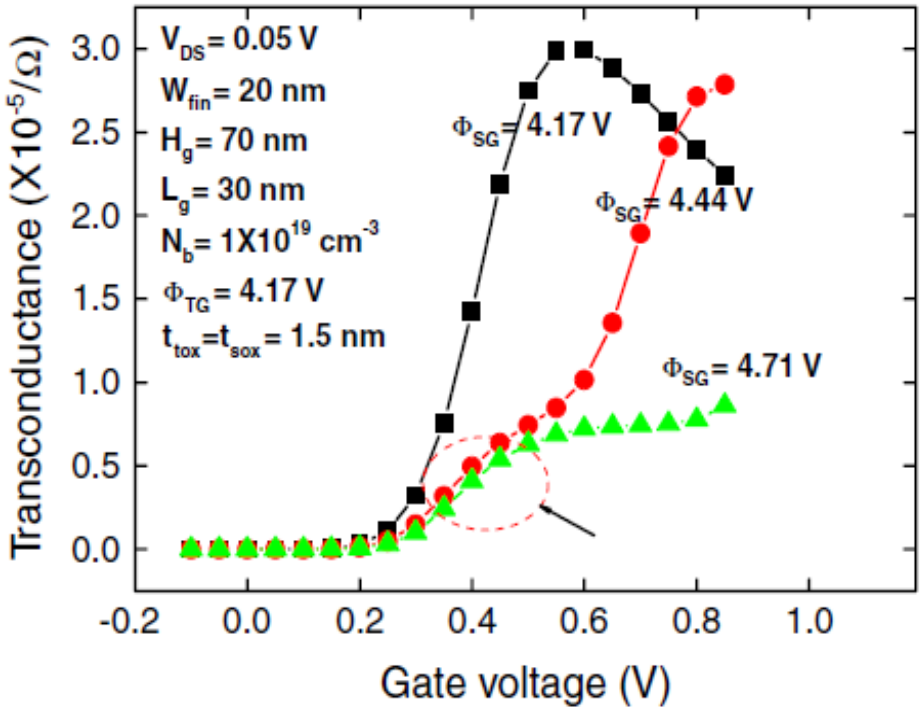


Fig. 5.7. Simulated NMOS transconductance characteristics as a parameter of Φ_{SG} when Φ_{TG} is fixed at 4.71 V [114].

(Φ_{TG}= 4.17 V) makes the V_{th} on the corner region low, so that the corner channel turns on earlier than the main side-channel. The corner channel has lower V_{th} for given Φ_{TG}=Φ_{SG}= 4.17 V, but not clearly observed because the turn-on of the corner channel overlaps more closely with that of the side channel [114].

5.2.5. Threshold Voltage Roll-off with Device Scaling Parameters:

(a) V_{th} Roll-off with Gate Length, Lg of Double Gate n-FinFET:

Fig. 5.8 shows simulation results of threshold voltage roll-off of double-gate n-FinFET with gate length varying from 15.3 nm to 18.8 nm. The device parameters undertaken for the simulation study are as per the projections of ITRS-2010 for LSTP logic technology for the year 2016 [1], wherein channel width, W_{ch} = 7.5 nm, gate-oxide thickness = 1.1nm, fin body doping = $1\times10^{17}cm^{-3}$. Device has been simulated for a drain supply, V_{dd} =0.78V and for a gate bias varying from 0-1V. From the PADRE device simulations, it is observed that threshold voltage rolls-off at lower gate lengths. The threshold voltage has been defined as the gate voltage when the drain current is 0.0001 A/μm. It is because when the distance between drain and source reduces with gate length scaling, the channel potential becomes more affected by the drain electric field encroachment reducing the gate bias requirement to invert the channel [14].

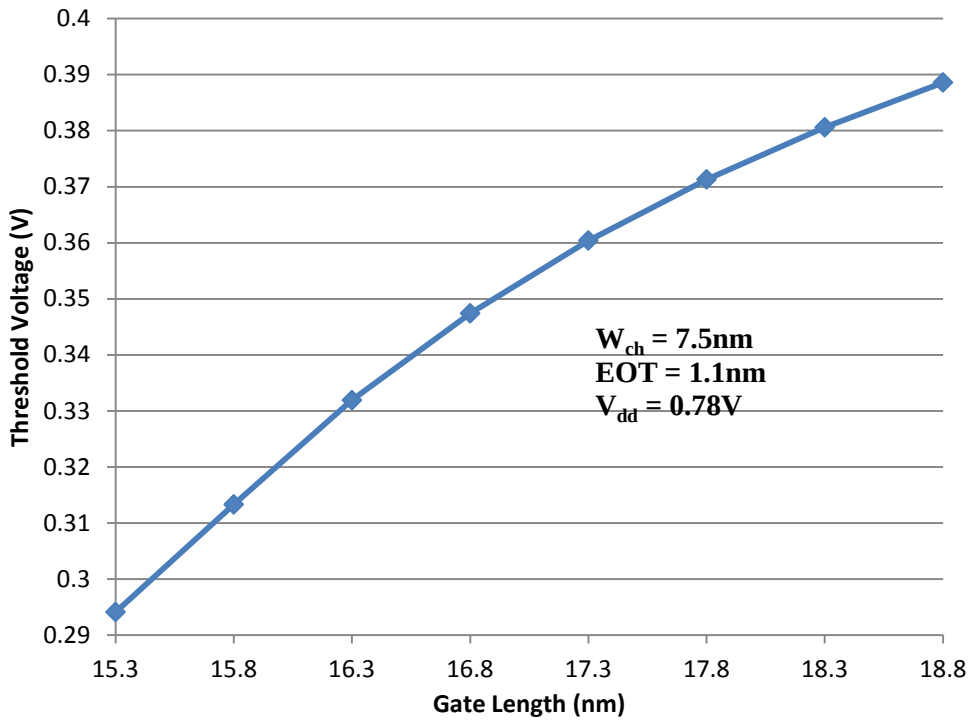


Fig. 5.8. Threshold Voltage versus gate length of DG n-FinFET

(b) V_{th} Roll-off with fin Thickness, T_{fin} of Double Gate n-FinFET:

Fig. 5.9 shows threshold voltage roll-off characteristics of double gate n-FinFET for variable fin thickness, ranging from 12nm to 20nm. For the simulation purpose, the various device parameters follow the projections of ITRS-2010 for HP logic technology [1], wherein various device parameters undertaken are L_g = 17 nm, oxide thickness = 0.77 nm, fin body doping = 7.5×10^{18}. Device has been simulated for a drain supply, V_{dd} = 0.81V and for a gate bias varying from 0-1V. PADRE simulations carried out has shown that threshold voltage is maximum for lower fin thicknesses and rolls-off with increased fin-thickness. It is because as channel width is reduced in the device, the sidewall gates gain better control of the channel region and become more efficient at preventing the encroachment of electric field from the drain on the channel region, which increases the threshold voltage [59].

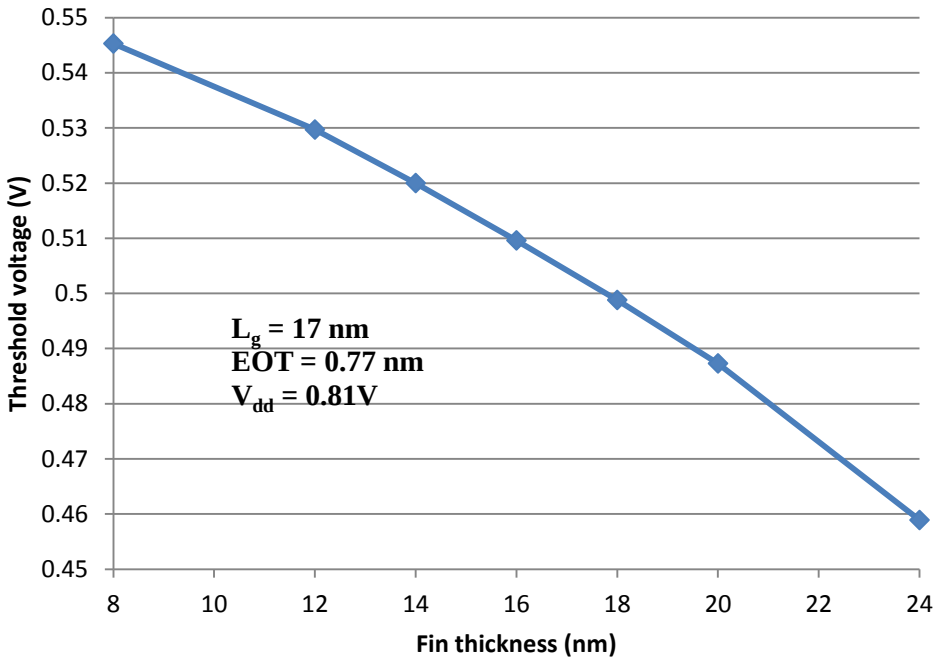


Fig. 5.9. Threshold voltage rool-off with respect to fin thickness in double gate n-FinFET.

(c) V_{th} Roll-off with fin Height, H_{fin} of Triple Gate n-FinFET:

Fig. 5.10 shows threshold voltage roll-off characteristics of triple gate n-FinFET for variable fin height, H_{fin} ranging from 16nm to 28nm. For the simulation purpose, the various device parameters follow the projections of ITRS-2010 for HP logic technology [1], wherein various device parameters undertaken are same as that used in threshold voltage versus fin thickness. Again the device has been simulated for a drain supply, V_{dd}

= 0.81V and for a gate bias varying from 0-1V. PADRE simulations show that threshold voltage rolls-off with an increase in fin height, H_{fin}, which is due to the fact that the top gate loses control over the entire channel region and the two vertical side gates mainly govern current conduction [191]. Therefore, from the viewpoint of controlling SCE's like threshold voltage roll-off, triple gate devices should be designed with lower aspect ratios (H_{fin}/T_{fin}).

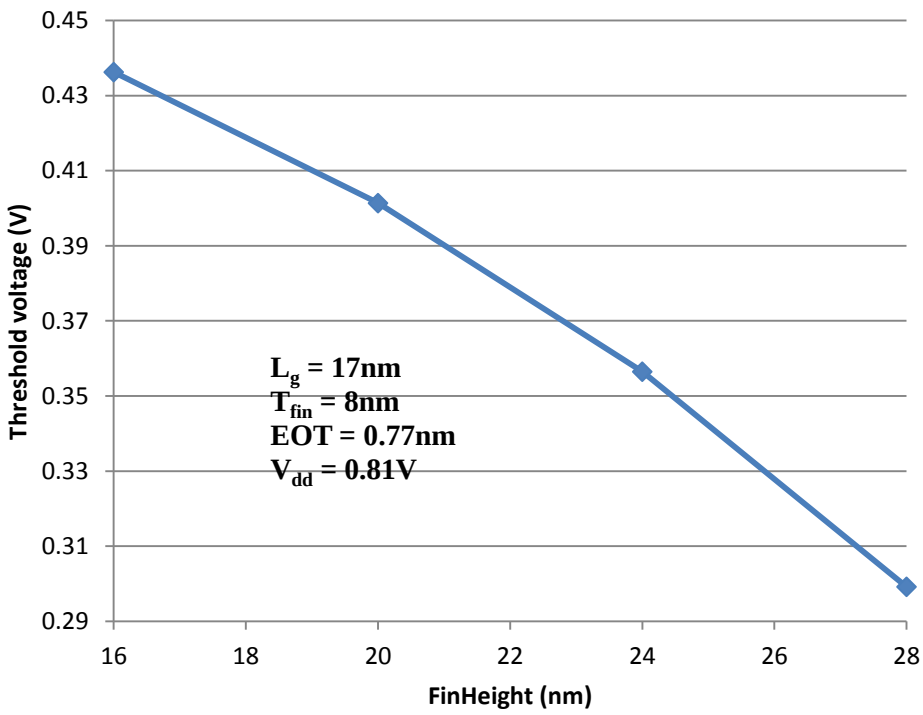


Fig. 5.10. Threshold voltage rolll-off with respect to fin height in triple gate n-FinFET.

5.3. Drain Induced Barrier Lowering (DIBL) and Subthreshold Slope (SS):

In short channel MOS devices, source and drain junctions create depletion regions that penetrate the channel region from both sides of the gate. These depletion regions carry electric fields that penetrate the channel region to a certain distance and 'steal' some of the control of the channel from the gate. When the drain voltage is increased, this penetration is amplified. As a result, the potential in the channel region and the resultant concentration of electrons are no longer controlled solely by the gate electrode but are also influenced by the distance between the source and the drain and by the voltage applied to the drain. There are two observable effects that result from this loss of charge control by the gate: drain-induced barrier lowering (DIBL), which causes the threshold voltage to decrease when the drain voltage increases; and degradation (that is, an

increase) in the subthreshold slope (SS). The effects are additive and both increase the leakage current of the transistors, constituting a serious impediment to further scaling of MOSFETs.

The magnitude of DIBL is usually defined by the following relationships: [17]

$$DIBL = (V_{th})_{Vds=V1} - (V_{th})_{Vds=V2} \qquad \text{(unit: V)}$$

$$DIBL = \frac{(V_{th})_{Vds=V1} - (V_{th})_{Vds=V2}}{V2 - V1} \qquad \text{(unit: mV/V or dimensionless)}$$

When the gate bias is below the threshold and the semiconductor surface is in weak inversion or depletion, the corresponding drain current is called the subthreshold current. The subthreshold region tells how sharply the current drops with gate bias and is particularly important for low-voltage, low-power applications, such as when the MOSFET is used as a switch in digital logic and memory applications. The parameter to quantify how sharply the transistor is turned off by the gate voltage is called the subthreshold swing, SS (inverse subthreshold slope, or simply subthreshold slope), defined as the gate swing required to increase the drain current by one decade. In other words, it can be defined as the gate swing required to reduce the drain current by one decade. It is expressed in millivolts/ decade. The lower the value of SS, the more efficient and rapid the switching speed of the device from the off state to the on state.

The expression for subthreshold slope is given by, [17],[91]

$$S = \left(\frac{kT}{q}\right) \ln(10) \left(1 + \frac{C_D}{C_{ox}}\right)$$

$$S = n \left(\frac{kT}{q}\right) \ln(10)$$

Where *n* is body factor. The closer n is to unity, the sharper is the transition between the transistors off and on states.

Drain Induced Barrier Lowering (DIBL) and subthreshold slope (SS) discussed above are important parameters of nanoscale MOS device and signify the extent to which gate can control the device conduction without off-state leakages.

(a) DIBL and SS Variation with Gate Length, L_g of Double Gate n-FinFET:

Fig. 5.11 shows DIBL and SS variation with the gate length of an n-FinFET. The parameters undertaken for this study have been taken as per ITRS projections for the year 2015 for High Performance Logic requirement. Gate length has been varied from 14nm to 26 nm, body thickness fixed at 8nm, for the drain bias of 0.05 and 0.81V. gate bias has been varied from 0-1V.Further the body doping has been kept uniform at 7.5e18

cm^{-3} with the Drain/source doping at 1e22 cm^{-3}. The PADRE device simulations have shown that both DIBL and SS increase sharply with the decrease in gate length. It is because the drain electric field encroachment on channel region increases for shorter gate-length devices. The gate losses control over channel and the device conduction is now controlled by the drain potential also.

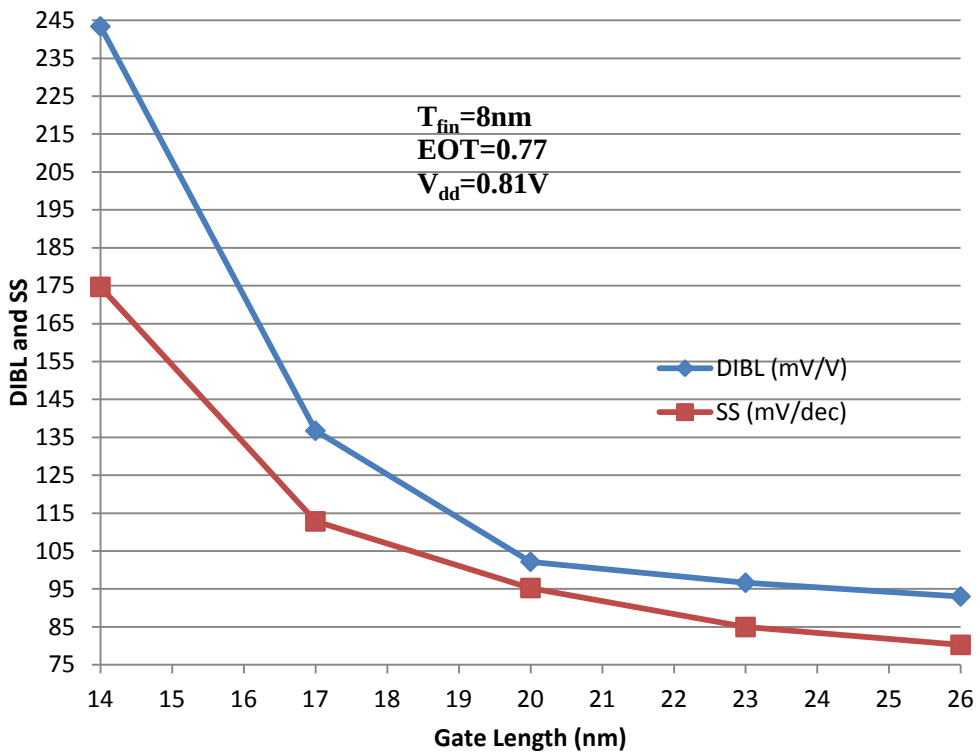


Fig. 5.11. DIBL and SS variation with gate length, L_g of DG n-FinFET.

(b) DIBL and SS Variation with fin Thickness, T_{fin} of Double Gate n-FinFET:

Fig. 5.12 shows variation of DIBL and SS with fin thickness of a double gate n-FinFET with fin thickness varying from 6nm to 14nm. The device structure undertaken for the study has parameters same as that used above for DIBL and SS versus gate length. The resulting characteristics from PADRE simulations reveal that both DIBL and SS increase with increasing fin-thickness. It is because with increasing the fin thickness the vertical self aligned gates weekly control entire channel region of device and drain electric field penetration becomes more effective to control the device conduction. Authors in [192] have experimentally demonstrated that in order to achieve acceptable SS behaviour fin thickness should be such that $T_{fin} < \frac{2}{3} L_g$.

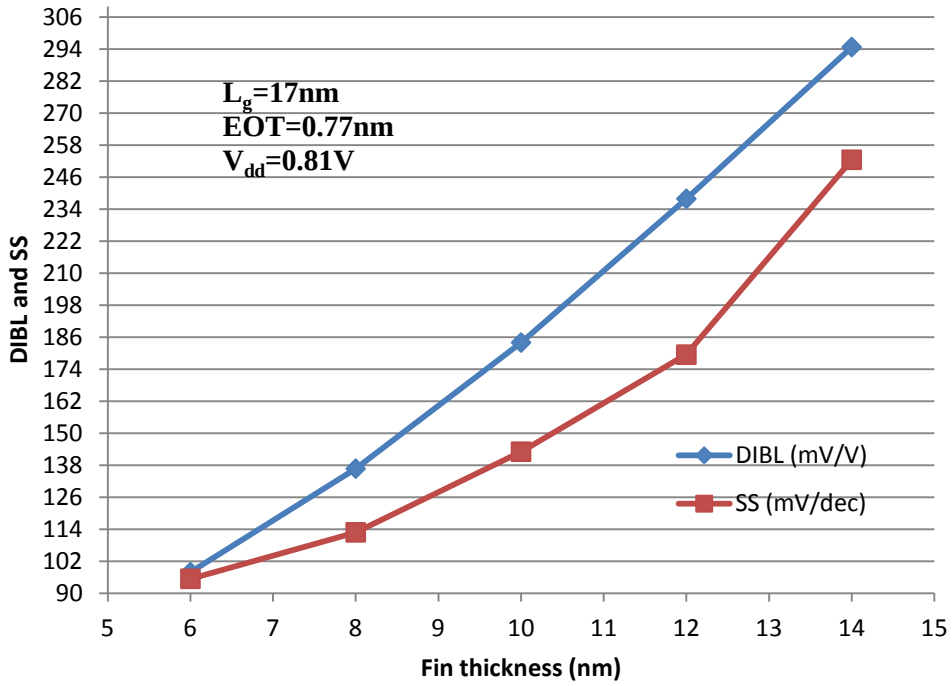


Fig. 5.12. DIBL and SS variation with fin thickness, T_{fin} of DG n-FinFET.

(c) DIBL and SS Variation with fin Height, H_{fin} of Triple Gate n-FinFET:

The variation of DIBL and SS with fin height, H_{fin} of a triple gate n-FinFET has been shown in Fig. 5.13, simulated with the device parameters same as used above for gate length and fin thickness variation (as per ITRS 2010), but this time the simulated device

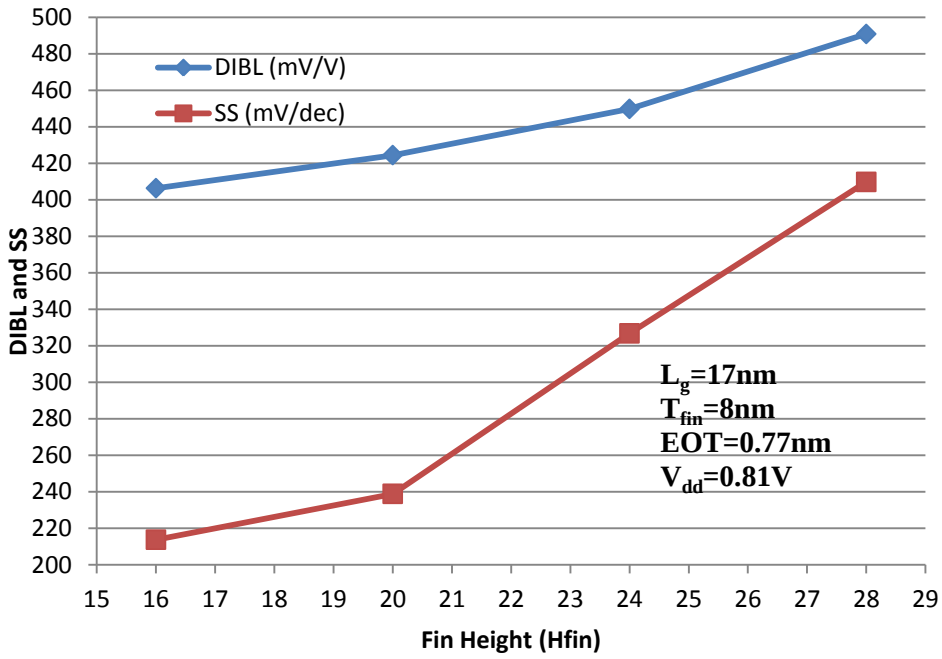


Fig. 5.13. DIBL and SS variation with fin height, H_{fin} of Triple Gate n-FinFET.

has an additional parameter, i.e, fin height, H_{fin}. In this study the fin height has been varied from 16 to 28nm for a fixed gate length and fin thickness of 17 and 8nm. From the PADRE simulation results obtained it is observed that both DIBL and SS increase with increasing fin height. It is because the top gate loses control over the channel with increase in fin height, while as the two lateral gates become the dominant to control the device channel conduction. It is not only the case with DIBL and SS degradation that needs to be discussed here, but the threshold voltage also degrades. It is degradation in SCE's in general [191]. Furthermore it has been recommended that triple gate devices should be designed with lower aspect ratios ($AR=H_{fin}/T_{fin}$) in order to reduce SCE's.

5.4. Corner Effects in FinFET Devices:

Corner effects imply the existence of parasitic channel around fin corners of FinFET devices due to the influence of fringing electric field penetration from coupling of different gates surrounding the fin body towards corners of such multi-gate structures. In these devices channel conduction occurs around the corner regions before the threshold voltage of main channel is reached. Corner effects in FinFETs are known to greatly deteriorate the performance of these devices in the subthreshold region due to parasitic channel conduction. Various techniques have been devised by researchers to tackle this parasitic conduction in FinFET devices. To be mentioned at here, Doyle et al. [193] have reported that device corners have lower threshold voltage than the bulk part of the device. This can cause kink effect which manifests itself as a ''hump" in device's subthreshold characteristics and hence implies a serious technological issue. They have proposed fin-corner rounding as a solution. Fossum et al. [194] have conducted 2D analysis of a multiple-gate SOI structure and concluded that the fin body should be left undoped in order to suppress corner effects. Authors in [123] have investigated the influence of corner effects on device characteristics as a limiting factor in device performance and have presented the corner implantation method to increase the body doping in corner regions as a solution to corner-related effects.

5.4.1. Kink Effect in Transfer Characteristics of Triple Gate FinFETs and its Elimination:

High channel doping in FinFET devices leads to corner effects in these devices which is observed in the form of a hump (kink effect) in the transfer characteristics below the

device's threshold voltage. Fig. 5.14 shows the transfer characteristics of an idealized device with square corners simulated for gate length, L_g= 180nm, fin height, H_{fin}= 250nm, fin width, W_{fin}= 100nm and oxide thickness, T_{ox} = 4nm [123]. The device has been simulated for various body doping concentrations (2×10^{17}, 5×10^{17}, $1\times10^{18}$and $2\times10^{18}cm^{-3}$). Characteristics of devices with body doping, N_B of $1\times10^{18}cm^{-}3$ and $2\times10^{18}cm^{-3}$ have a ''hump" below the device's threshold voltage, i.e. kink effect is observed. For the shift of N_B from $2\times10^{17}cm^{-3}$ to $2\times10^{18}cm^{-3}$ there is a threshold voltage shift of 0.504 V. Device with the highest fin–body doping has a threshold voltage of 0.421 V which is not high enough for low-standby power. Fig. 5.15 shows transfer characteristics of the realistic triple-gate FinFET with rounded corners. Subthreshold characteristics' distortion is less pronounced when compared to the results in Fig. 5.14, i.e. kink effect is reduced. Consequently, threshold voltage-shift is larger for the device with rounded corners when increasing the fin–body doping. There is a 0.674 V shift in threshold voltage between devices with N_B of $2\times10^{17}$and $2\times10^{18}cm^{-3}$. The realistic FinFET with the highest fin–body doping has threshold voltage of 0.576 V, which is adequate for low-standby power applications. Although the structure with rounded corners has an improved immunity to corner effects, there still exists a kink effect for the fin–body doping above 5×10^{17} cm^{-3}. Although this device has an adequate threshold voltage value, kink effect presents a problem for device's turn off capabilities. Namely,

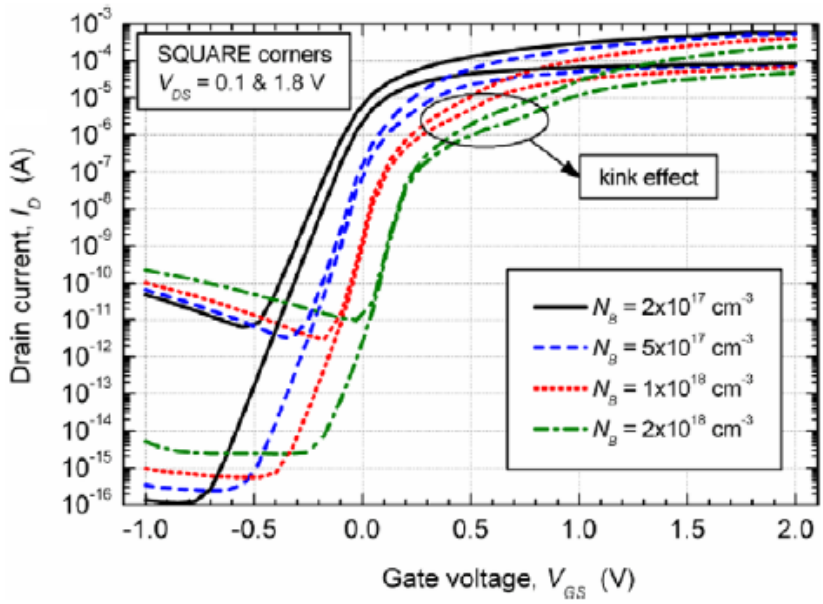


Fig. 5.14. Transfer characteristics obtained for the idealized FinFET with square corners. Devices with higher body doping suffer from severe kink effect; VTH is much lower and SS much higher than expected [123].

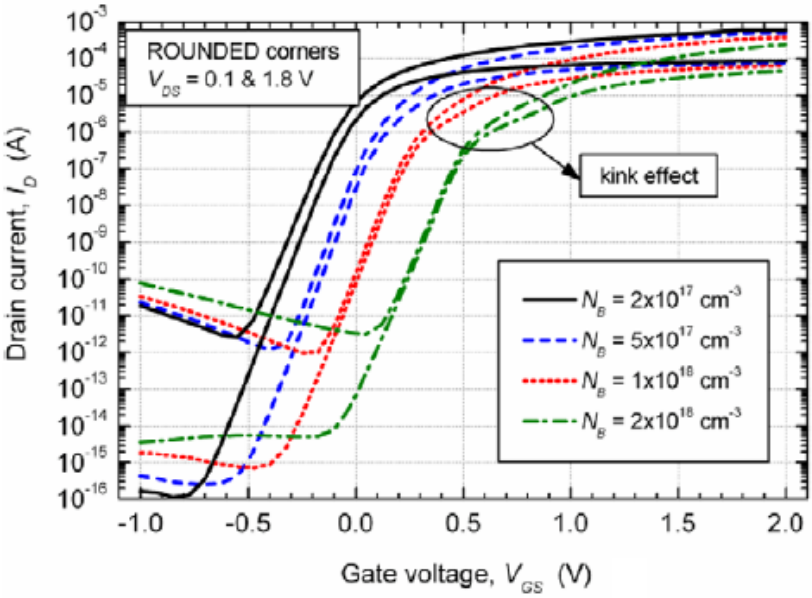


Fig. 5.15. Transfer characteristics obtained for the realistic FinFET with rounded corners. These devices are more immune to corner effect than square-corner FinFETs which is evident from a higher VTH-shift with increasing body doping [123].

kink effect deteriorates subthreshold swing (SS) around threshold voltage (V_{th}) and this reduces device's turn off speed. Therefore, it is necessary to find a systematic solution to corner and kink effect even for realistic FinFETs.

The reason for different immunity to corner effect is the electric field fringing due to coupling between the top gate and the side gate electrodes. In two-dimensional cross-sectional potential distributions for V_{GS} = 0.8 and V_{DS} = 1.8 V shown in Fig. 5.16 potential barrier for the electrons is the highest in the middle of the fin and decreases toward the silicon-oxide interfaces for both devices. Regions with the highest potential, i.e. lowest barrier for electrons, are corner regions since the electrostatic coupling between the top and the side-gate is the strongest in device corners and this causes current flow to be pushed to the corners. Near the silicon dioxide interface the rounded-corner FinFET has lower potential and therefore higher potential barrier for electrons than the square-corner FinFET. Additionally, the difference between the electric potential at the interface under the top gate at the middle of the fin and in the corners is smaller in the realistic FinFETs that in the idealized FinFETs which explains the less pronounced corner effect in the rounded-corner devices.

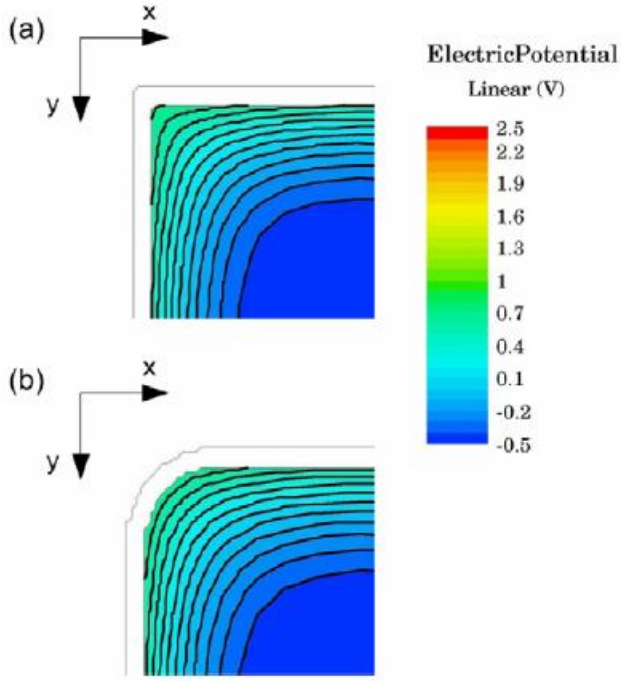


Fig. 5.16. Potential distributions in corner regions obtained at V_{GS} = 0.8 and V_{DS} = 1.8 V for (a) square-corner and (b) rounded-corner FinFET. Rounded-corner devices are more immune to corner effect because the potential barrier for electrons in corner regions is slightly higher in the case of realistic FinFET which increases V_{TH} in device corners [123].

Two main factors arise that determine the magnitude of corner effects: fin width and body doping. In FinFETs at coarser technology nodes corner effects are pronounced and kink effects arise in device's transfer characteristics because the devices are only partially depleted due to wider fins and heavy doping. If high body doping is used for V_{th}-adjustment in state-of-the-art technology nodes, kink effect in transfer characteristics can occur and SS and V_{th} can deteriorate due to corner effect.

To eliminate the kink effect caused due to the corner effect, authors in [123] have proposed the corner implantation scheme as a solution, wherein the threshold voltage in corner regions is increased by increasing the fin–body doping N_B in the corner regions. Corner effect can be suppressed by either turning off the corners completely (e.g. implantation with a doping peak value considerably larger than N_B) or by optimizing corner implantation to obtain the same V_{th} in device's corners as in other parts of the channel.

Corner implantation reduces electric potential in corner regions and the region of lower electric potential extends further from the middle of the fin to the corners. As a consequence of increased potential barrier in corner regions, V_{th} in the corner regions increases and this can clearly be observed in current density plots in Figures 5.17 and 5.18 where the idealized device's corners are completely turned off and there is no current flow in corner regions, whereas the corner conductance in the realistic device is suppressed by corner implantation.

Given that the corner regions are turned off, kink effect should be completely removed from devices' transfer characteristics. This would imply proper V_{th} values and better subthreshold behavior (lower SS and DIBL). On the other side, turning off the corners decreases the conductive part of the total channel width and reduces device's driving capabilities, i.e. the on-state current.

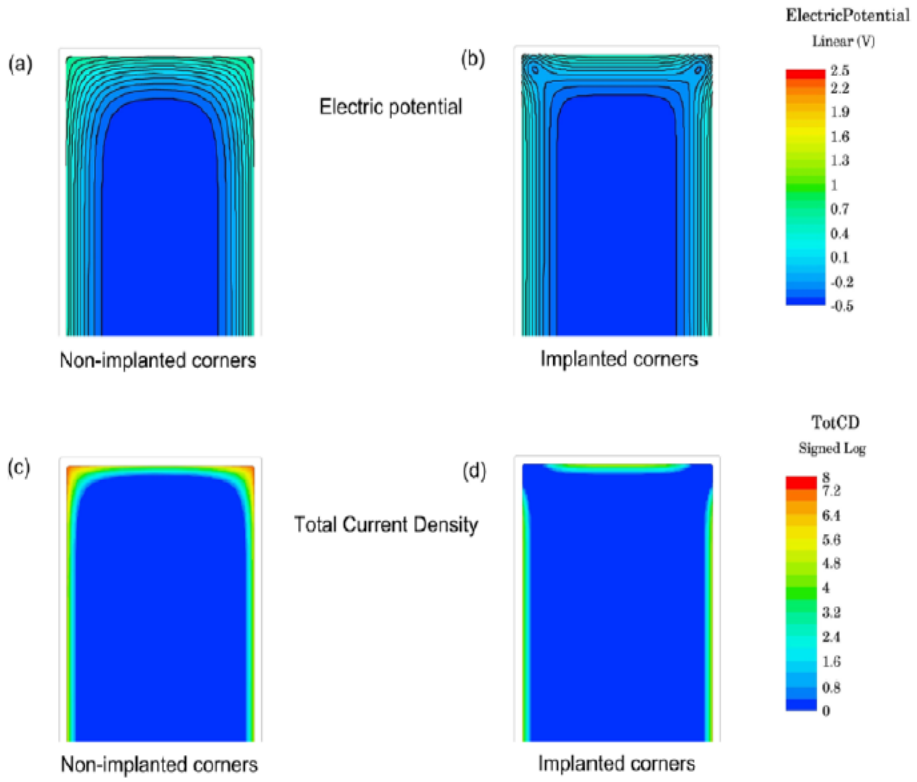


Fig. 5.17. 2D cross-sectional views of the idealized FinFET showing upper part of the fin at the middle of the channel. Potential distributions are presented in (a) and (b), and total current density distributions in (c) and (d). Plots are obtained at V_{GS} = 0.8 and V_{DS} = 1.8 V. It is evident that in idealized devices corner implantation turns off the corners completely [123].

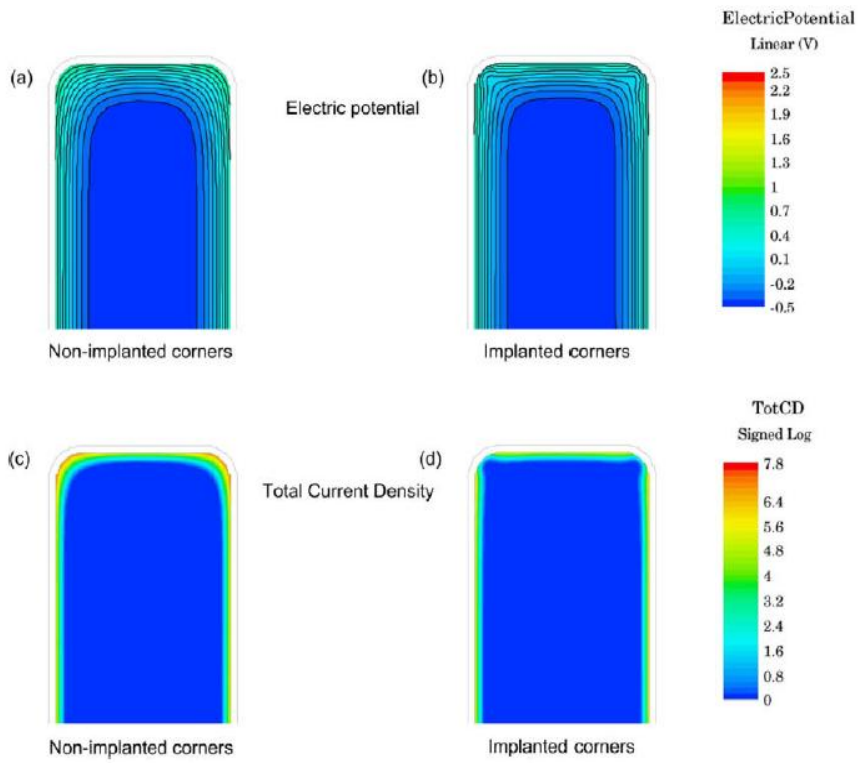


Fig. 5.18. 2D cross-sectional views of the realistic FinFET which show upper part of the fin at the middle of the channel. Potential distributions are shown in (a) and (b) and total current density distributions in (c) and (d). Plots are obtained at V_{GS} = 0.8 and V_{DS} = 1.8 V. In the case of realistic FinFET, conduction in the corners is reduced significantly [123].

5.4.2. Multiple Threshold Voltages Due to Corner Effects:

Another effect that is observed in FinFETs is the existence of multiple threshold voltages due to parasitic channel conductions. The effect has been demonstrated in [115] through 3-D numerical simulations using Silvaco (Atlas). The authors have shown that due to corner effects, there exist more than one peaks in the transconductance characteristics of FinFET devices. These multiple transconductance peaks reflect the presence of more than one threshold voltages which may consist of the threshold voltage of main sidewall gates, top and bottom gates (in case of triple and quadruple gates) and threshold voltage due to corners. All threshold voltages reflect the inversion of channel at various interfaces (sidewalls, top and bottom interfaces) and at the corner regions (top corners, bottom corners) with their threshold at different gate voltages. It has been observed that when the MuGFET transistor presents a uniform doping concentration, the double-gate and quadruple-gate can present up to two threshold voltages ($V_{T,BC}$, $V_{T,SG}$ for double-

gate; $V_{T,TC} \cong V_{T,BC}$ and $V_{T,SG} \cong V_{T,TG} \cong V_{T,BG}$ for quadruple-gate) and the triple-gate can present up to three threshold voltages ($V_{T,TC}$, $V_{T,BC}$ and $V_{T,SG} \cong V_{T,TG}$), both results are observed for higher doping concentration.

As an illustration, Fig. 5.19 shows the transconductance versus gate voltage of a triple gate FinFET device with channel doping concentration, $N_A = 5 \times 10^{19}$ cm^{-3}; gate length, $L_g = 1\mu$m; fin width, W_{fin} = 120 nm; fin height, H_{fin} = 60 nm and drain bias, V_{DS} = 100 mV having threshold voltages: $V_{T,TC}$ = 1.42 V; $V_{T,BC}$ = 2.23 V and $V_{T,SG} = V_{T,TG}$ = 2.98 V.

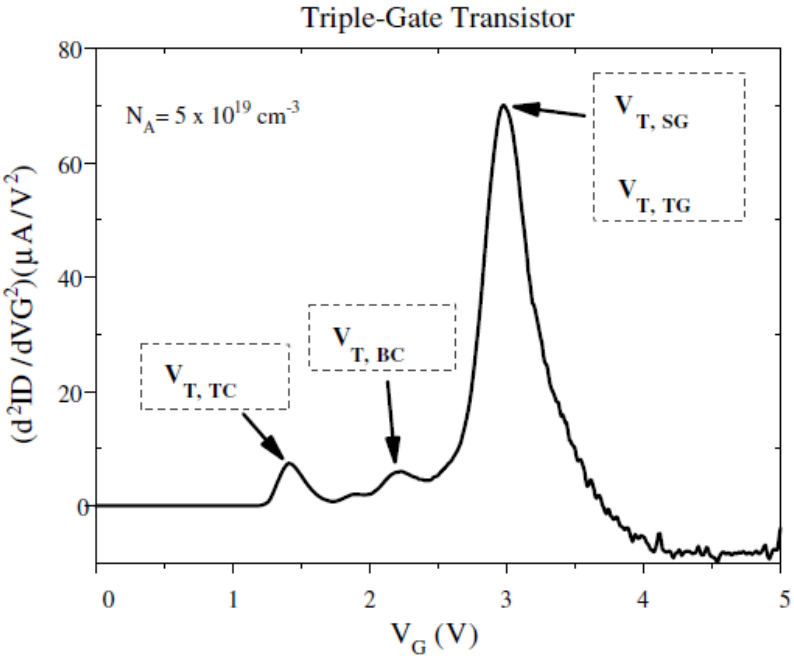


Fig. 5.19. Transconductance (second derivative of the drain current, d^2I_D/dV_G^2) versus gate voltage for triple-gate transistor showing multiple threshold voltages of device [115].

When the channel is divided in two differently doped regions (dual doped) it is possible to observe up to four threshold voltages. In triple-gate this effect is related to the top corners ($V_{T,TC}$), bottom corners ($V_{T,BC}$), sidewalls gates ($V_{T,SG}$) and top gate ($V_{T,TG}$) while in quadruple-gate it is due to bottom corners ($V_{T,BC}$), top corners ($V_{T,TC}$), bottom and sidewalls gates ($V_{T,SG} \cong V_{T,BG}$) and top gate ($V_{T,TG}$) [115].

5.5. Conclusion:

In this chapter various short channel effects (SCE's) related to FinFET devices has been demonstrated with respect to various physical scaling and process parameters of the

devices. To maintain a proper threshold voltage in ultrathin devices like FinFET is a challenging task due to various limitations imposed on the device characteristics. Adjustment of threshold voltage with proper channel doping and gate work-function of FinFETs has been presented through theoretical discussion followed by various simulation results. It is observed that gate work-function engineering should be preferred compared to adjustment through fin body doping as the later has the limitation that it reduces the carrier mobility and presents bandgap narrowing effect in extremely scaled devices. Roll-off characteristics of threshold voltage with channel length, fin thickness and fin height have been presented. It has been shown that threshold voltage rolls-off with gate length scaling due to increased drain influence which reduces the barrier of conduction from source to drain. Roll-off characteristics of threshold voltage versus fin thickness has shown that reducing fin thickness can increase the gate control of device towards channel electrostatics and maintains threshold voltage at higher level. Further it has been presented that threshold voltage rolls-off with increasing fin height of device due to the fact that the top gate loses control over the entire channel region and the two vertical side gates mainly govern current conduction. Two major short channel effects have been discussed along with simulation results for study of their variation with physical scaling parameters of device. Simulation results have shown that DIBL and SS increase sharply with the decrease in gate length which is because the drain electric field encroachment on channel region increases for shorter gate-length devices. Variation of DIBL and SS with respect to fin thickness has shown that both DIBL and SS increase with increasing fin-thickness. It is because with increasing the fin thickness the vertical self aligned gates weekly control entire channel region of device and drain electric field penetration becomes more effective to control the device conduction. Also it has been demonstrated that in order to achieve acceptable SS behaviour fin thickness of device should be such that $T_{fin} < \frac{2}{3} L_g$. Study of DIBL and SS with respect fin height has shown that both DIBL and SS increase with increasing fin height. It is because the top gate loses control over the channel with increase in fin height, while as the two lateral gates become the dominant to control the device channel conduction. It has been mentioned that it is not only the case with DIBL and SS degradation but the threshold voltage also degrades with increasing fin height. It is degradation in SCE's in general. Furthermore it has been recommended that triple gate devices should be designed with lower aspect ratios ($AR=H_{fin}/T_{fin}$) in order to reduce SCE's.

The parasitic corner effects in FinFETs as studied by various authors have been presented and discussed. From these studies it has been found that these corner effects deteriorate the subthreshold behaviour of triple gate FinFET devices due to parasitic channel conduction of these devices. The various corner effects on the characteristics of FinFET as observed by varios authors are: kink effect in the transfer characteristics; multiple threshold voltages of device; hump in the transconductance characteristics. Higher fin body dopings have been reported to show more kink effects compared to lower body dopings. Furthermore it has been discussed that various techniques such as utilizing undoped fin body devices, corner rounding of fins and corner implantation as proposed by various authors can eliminate the corner effects in FinFET devices.

Chapter 6
A Comparative Simulation Study of Short Channel Effects in n-FinFET Structure for Si, GaAs, GaSb and GaN Channel Materials

6.1. Introduction:

Multiple-gate field effect transistors (MuGFETS) [195] have been reported to show excellent short channel effect (SCE) performance to replace their conventional single gate structures. FinFET [67],[2], a viable implementation of multiple gate MOSFET structure has been reported as the most promising candidate to eliminate such short channel effects while maintaining the downscaling of CMOS to follow the projections of ITRS roadmap [1]. FinFET technology is very attractive that suffices device designers to aggressively look for their efficient structural and process variation, leading to a high end research in such nano-dimensional device structures. A self-aligned double gate (SOI) structure scalable to 20 nm gate length has been experimentally demonstrated in [35]. The structure can effectively suppress SCE's even with 17-nm gate length. A double-gate FinFET with gate length down to 10nm has been fabricated and experimentally demonstrated for scalability and potential performance benefits in [178]. During the experiment, the FinFETs have been fabricated on bonded SOI wafers with a modified planar CMOS process. It is observed that further scaling down FinFET device structure will be much more difficult because of various practical limitations, such as gate leakage through hot carrier tunnelling, parasitic resistance and capacitance, DIBL, SS, and threshold voltage roll-off. All these factors put a limit on scaling of the FinFET structures. For the first time 35nm gate length with high-K and strain enhanced transistor technology was introduced [196],[197]. As expected, further improvements in transistor speed and performance while reducing the device dimensions will be possible by using new channel materials in order to comply with the Moore's law and the ITRS road map. Both industry and academia have been investigating alternative device architectures and materials, among which III-V compound semiconductor transistors stand out as promising candidates for future logic applications because their light effective masses lead to high electron mobilities and high on-currents, which should translate into high device performance at low supply voltage [198].

Practical III-V metal-oxide-semiconductor field effect transistors (MOSFETs) remained a dream for more than four decades [198], mainly due to lack of oxide

providing thermodynamically stable interface with low density of bandgap states. Fermi level pinning at the interface is a major problem in III-V based MOSFETs calling for development of technologies for surface passivation. After over 30 years of development of passivation technologies, a significant progress has been achieved, and recently MOSFETs with reasonable performance characteristics have been reported [203]. With the recent progress in the field of surface cleaning combined with atomic layer deposition (ALD), it has been possible to deposit high-quality dielectrics on III–V semiconductors. Ali *et al.* reported on the use of plasma-enhanced ALD to unpin the GaSb/dielectric interface [200]. Merckling *et al.* explored the use of *in situ* deposition of Al_2O_3 on GaSb grown on InP using molecular beam epitaxy and reported density of interface states, D_{it} values in the low $10^{12}/cm^2eV$ range near the valence band [201]. As an attempt to overcome the challenges in fabricating GaSb-MOSFET, A. Nainani *et al.* recently fabricated and studied GaSb-pMOSFET with an atomic layer deposition of Al_2O_3 gate dielectric and a self aligned source/drain formed by ion implantation. [202] The earliest attempt to fabricate MOSFETs on GaSb dates back to 1977, when the MISFET principle was demonstrated in to a new material, GaSb using low temperature pyrolytic-silicon-dioxide as the gate insulator. [199] GaAs exhibits many superior electrical properties compared to silicon, including high electron mobility, a large energy band gap, and easy access to a hetero-structure in microelectronic devices. Selective liquid phase chemical-enhanced oxidation (SLPCEO) process by using metal as the mask (M-SLPCEO) to fabricate n-channel depletion-mode GaAs-nMOSFET has been proposed and demonstrated experimentally in [204], due to its superiority over conventional fabrication process and better device performance. Authors in [205] have demonstrated Liquid-phase deposition of SiO_2 (LPD-SiO_2) is used for the deposition of silicon dioxide (~40 ^oA) on GaAs substrate during GaAs metal–oxide–semiconductor field effect transistors (MOSFET) fabrication with an 8µm gate length and 40µm channel width at a lower process temperature (below 60^oC).Due to their wide band-gap GaN and AlGaN are already established materials for light emitting diodes and lasers [212], and have attracted a lot of interest for applications in high power and high temperature electronics [213]. GaN based MOS transistor can elevate the adverse affects of DIBL and band to band tunnelling (BTBT) due to its wider band-gap. Gallium Nitride (GaN is used as a channel for GaN-HEMT devices due to the fact that: (1) the concentration of the Two Dimensional Electron Gas (2DEG), which is formed between the AlGaN and GaN heterostructure interfaces, is about ten times as large as that of Si

(increasing the amount of drain current). (2) The electron saturation velocity of GaN material is about twice as fast as that of Si (high frequency). (3) The breakdown of the electric field is about ten times larger than that of Si (high breakdown voltage). Furthermore GaN-HEMT device has been developed with a source field plate (SFP) structure that may be used as a high output power amplifier for next-generation base station applications [211].

A systematic study on use of various III-V semiconductors as channel material in FinFET device technology remains yet to be done. In this chapter a comparative study of SCE performance of FinFET by undertaking four different channel materials which consist of Si and three III-V compound semiconductor materials: GaAs, GaSb and GaN to act as channel for a double gate n-channel FinFET. Various properties of these channel materials that we have utilized in our simulation setup are listed in Table 6.1.

Table 6.1. List of various properties of Si, GaAs, and GaSb and GaN at 300K used in simulating the results [206], [207], [208].

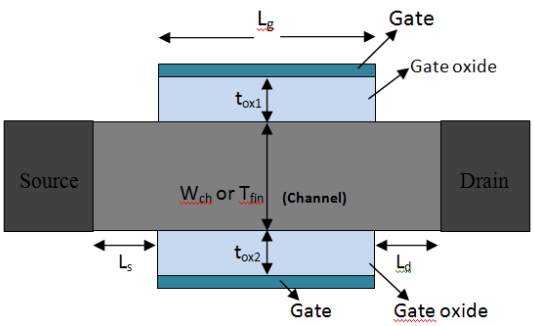
Properties		**Si**	**GaAs**	**GaSb**	**GaN**
Energy band-gap (eV)		1.12	1.424	0.726	3.2
Dielectric constant		11.7	12.9	15.7	8.9
Electron affinity (V)		4.05	4.07	4.06	4.1
Electron effective mass		0.2 m_0	0.041 m_0	0.063 m_0	0.20m_0
Density of states effective mass	Electrons	1.18m_0	0.57m_0	0.6m_0	0.57m_0
	Holes	0.81m_0	0.8m_0	1.5 m_0	0.8m_0
Light-hole effective mass		0.16m_0	0.076m_0	0.05m_0	0.3 m_0
Heavy-hole effective mass		0.49m_0	0.050m_0	0.4m_0	1.4 m_0
Electron mobility (cm^2/V-s)		1450	8500	3000	1000
Hole mobility (cm^2/V-s)		500	400	1000	200
Saturation Velocity (cm/s)	Electrons	$1.0x10^7$	$0.72x10^7$	$1.34\ x10^7$	$0.9x10^7$
	Holes	$0.704x10^7$	$0.9x10^7$	$1.1\ x10^7$	$1.0x10^7$

m_0 = 0.91093897x10^{-30} kg (rest mass of electron)

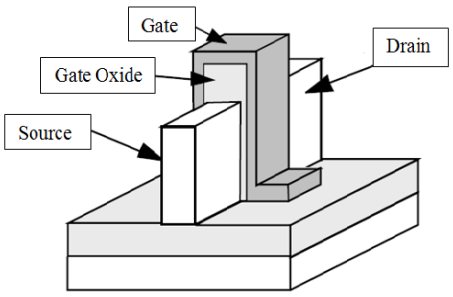
The main aim of this study has been to carry out the systematic study of the SCE's in n-channel FinFET's using the above mentioned materials in order to exploit devices to its best applications. The present work could also help the designers in deciding about the material to be used for fabrication of such devices for a particular application with efficient performance.

6.2. Device Structure and Simulation Methodology:

The device structure of double gate n-channel FinFET structure has been illustrated in Fig. 6.1, which consists of channel length L_g (also called gate length), channel width W_{ch}, which is also referred to as fin width or fin thickness, T_{fin} in case of triple gate FinFET wherein top gate is made active by making the top oxide layer very thin. Further, the oxide is placed on either sides of the side walls of fin and at the top surface of the fin before the gate contact is made. The thickness of the side wall oxide is specified by t_{ox1} and t_{ox2}. In the present study the device structure undertaken for simulation purposes, the gate length has been varied in the range of 40nm to 55nm, channel width from 15nm to 40nm. The oxide thickness has been taken 2nm and kept constant throughout the simulation studies. The drain/source doping 1e20cm^{-3}and channel doping 5e16cm^{-3}. The drain bias has been taken 0.05V and 1V, gate bias varied from 0V to 1V.



(a) *Two Dimensional Double-Gate FinFET structure*



(b) *Quasi-planar three dimensional structure of FinFET on SOI*

Fig. 6.1. Device structure of FinFET

The results presented are based on drift-diffusion model. The model has been used in the present calculations because of the fact that subthreshold characteristics of these devices are diffusion dominated and reflects device characteristics in the subthreshold region well in consistence with the experimentally observed results [81], [209]. It has been reported that quantum mechanical effects become negligible while simulating the transistor structures with lateral dimensions greater than 10nm. In the present study, device simulations have been performed using PADRE simulator from MuGFET [210].

6.3. Simulation Results:

6.3.1. DIBL versus Gate Length and Channel Width:

In order to study the DIBL characteristics with respect to gate length, L_g, the n-FinFET structure has been simulated for various gate lengths ranging from L_g= 40nm to 55nm for a fixed channel width of 30nm and oxide thickness of 2nm. The different channel materials used are Si, GaAs, GaSb and GaN with the material properties as given in Table 6.1. DIBL is a measure of how significantly the potential barrier in the channel, and hence the conduction path between source and drain is controlled by drain bias rather than what should be controlled by gate bias. Generally, DIBL increases sharply with the decrease in gate length of FinFET while as it decreases with the decrease in channel width. It is because the drain influence upon the channel potential increases while decreasing the gate length or increasing the channel width. The DIBL versus gate length is plotted in Fig. 6.2 for the four different materials. From the simulation study carried out in this work, It has been observed that GaAs and GaN-channel FinFET structure offer better DIBL characteristics in comparison with other materials, however for gate lengths less than about 46nm GaN offers better characteristics of DIBL compared with GaAs. In Fig. 6.3 simulation results of DIBL variation with channel width, W_{ch} of FinFET have been presented, wherein the gate length and oxide thickness has been kept constant at 45nm and 2nm respectively. For this study, the channel width has been varied over 20 to 35nm and the devices were again simulated individually for different channel materials (Si, GaAs, GaSb and GaN). From the characteristics obtained, it has been observed that GaN channel-FinFET offers better DIBL characteristics compared with Si, GaSb and GaAs based FinFETs, however for channel width less than about 25nm, the DIBL characteristics are almost same for Si, GaAs and GaN-channel FinFETs. Furthermore

GaSb-channel FinFET offers worst DIBL characteristics in both DIBL versus channel length variation and DIBL versus channel width variation.

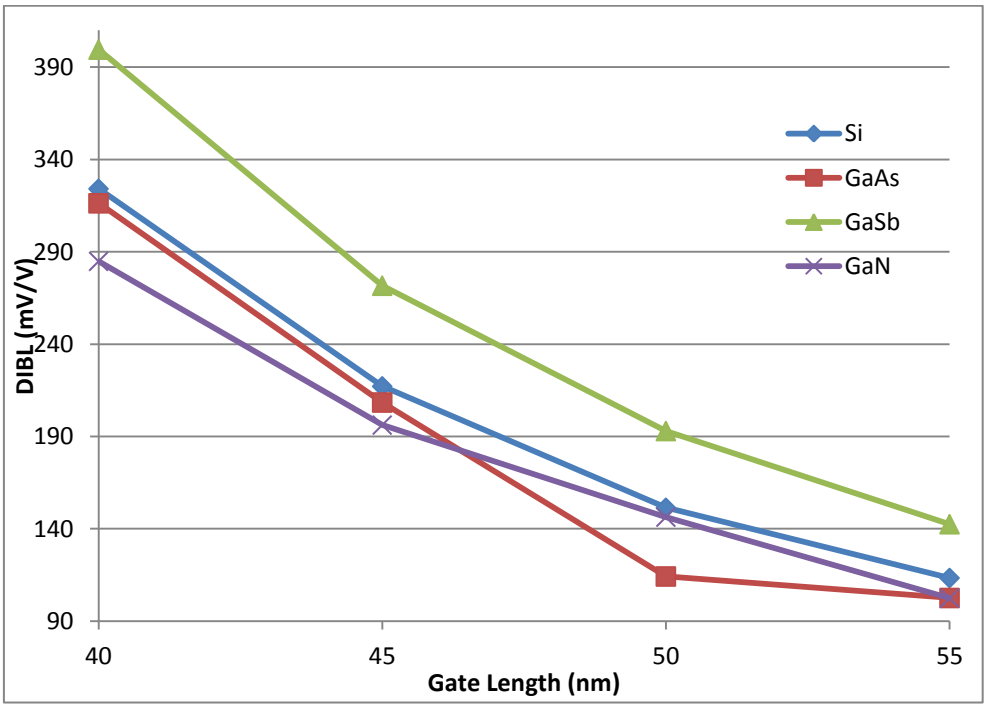


Fig. 6.2. DIBL vs Gate Length, L_g for Si/GaAs/GaSb/GaN channel FinFETs for W_{ch}=30nm and t_{ox1}=t_{ox2}=2nm.

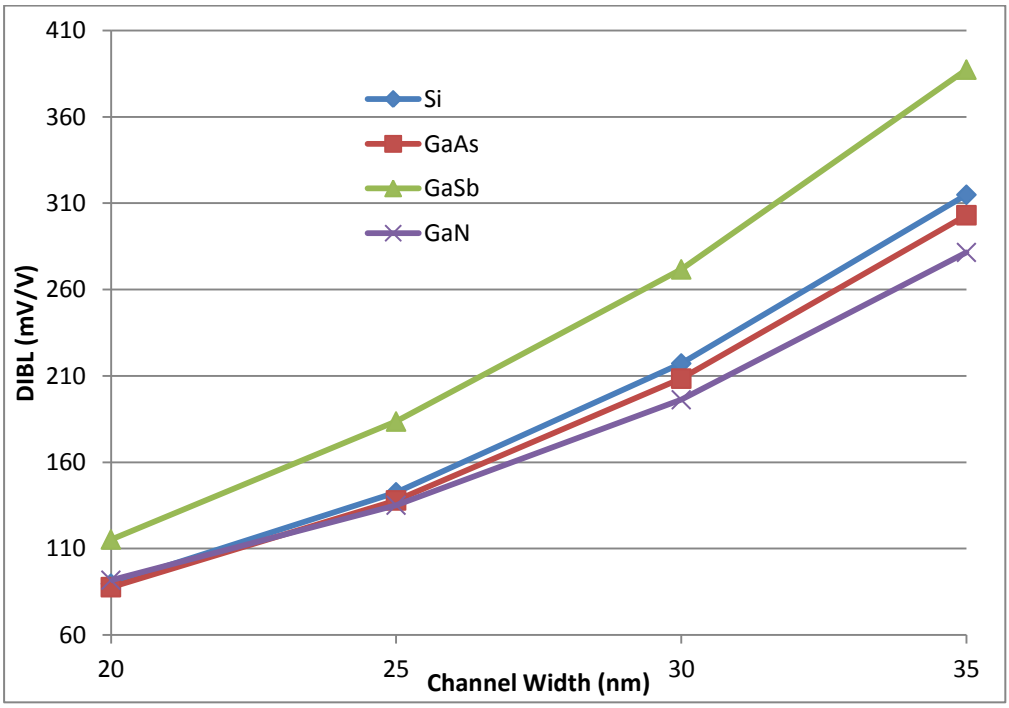


Fig. 6.3. DIBL vs Channel Width, W_{ch} for Si/GaAs/GaSb/GaN channel FinFETs for L_g=45nm and t_{ox1}=t_{ox2}=2nm.

6.3.2. SS versus Gate Length and Channel Width:

Subthreshold characteristics study becomes much more important parameter while decreasing the device dimensions much below in the nanometre regime of operation. It gives insight of the leakage currents associated with the device characteristics. As expected in general, for every different device structure studied, the subthreshold slope increases with the decrease in channel length while as it decreases with the decrease in channel width. The variation of subthreshold slope with gate length, L_g in case of the n-FinFET for different channel materials has been shown in Fig. 6.4 while that with respect to channel width, W_{ch} is plotted in Figure 6.5. For SS study, L_g has been varied from 40 to 55nm while as W_{ch} has been varied from 15 to 35nm. It is clear from the results shown in Fig. 6.4 that Si and GaAs-channel FinFET show almost identical SS characteristics, while as the GaN-channel device offers the better SS characteristics compared with other three materials.

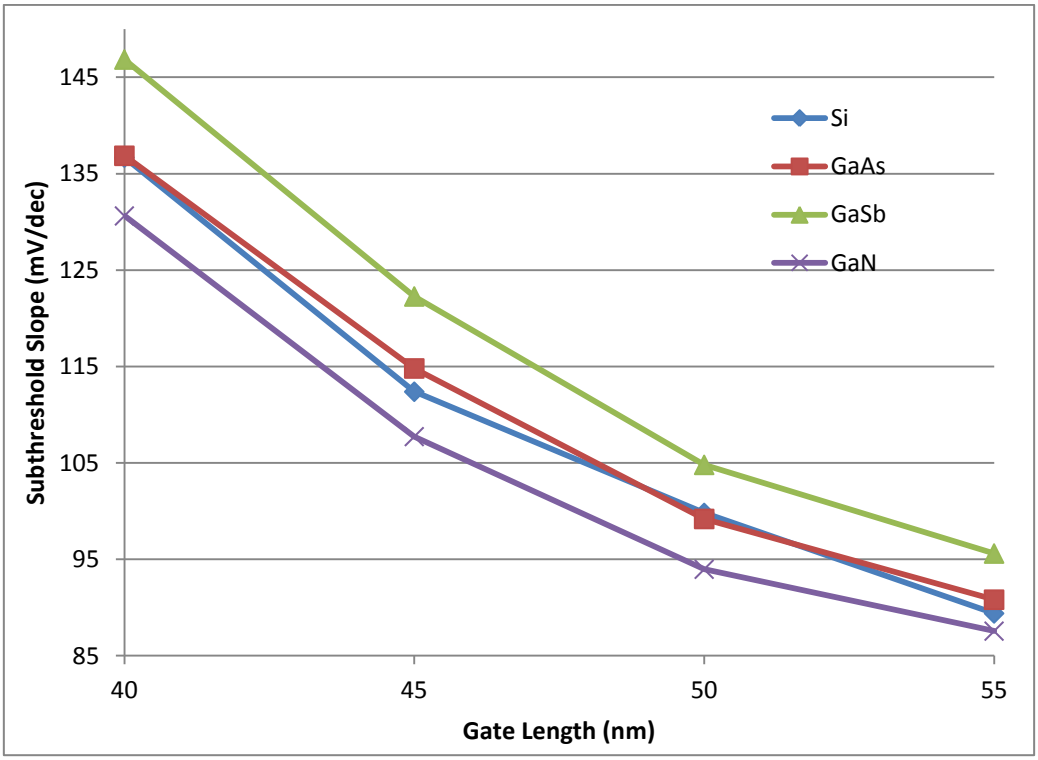


Fig. 6.4. SS vs Gate Length, L_g for Si/GaAs/GaSb/GaN channel FinFETs for W_{ch}=30nm and t_{ox1}=t_{ox2}=2nm.

From the results shown in Fig. 6.5, it is clear that at a channel width of about 18nm the three materials (Si, GaAs and GaSb) exhibit same value of the subthreshold slope. For channel width greater than about 18nm, SS behaviour for Si and GaAs-channel FinFET is almost same throughout the range of simulation study. GaN-channel FinFET has shown

much better SS characteristics compared to other three. Furthermore, it may be pointed out that GASb channel FinFET once again shows the worst SS characteristics compared with other three materials; however for channel width below 18nm, GaSb has good SS characteristics.

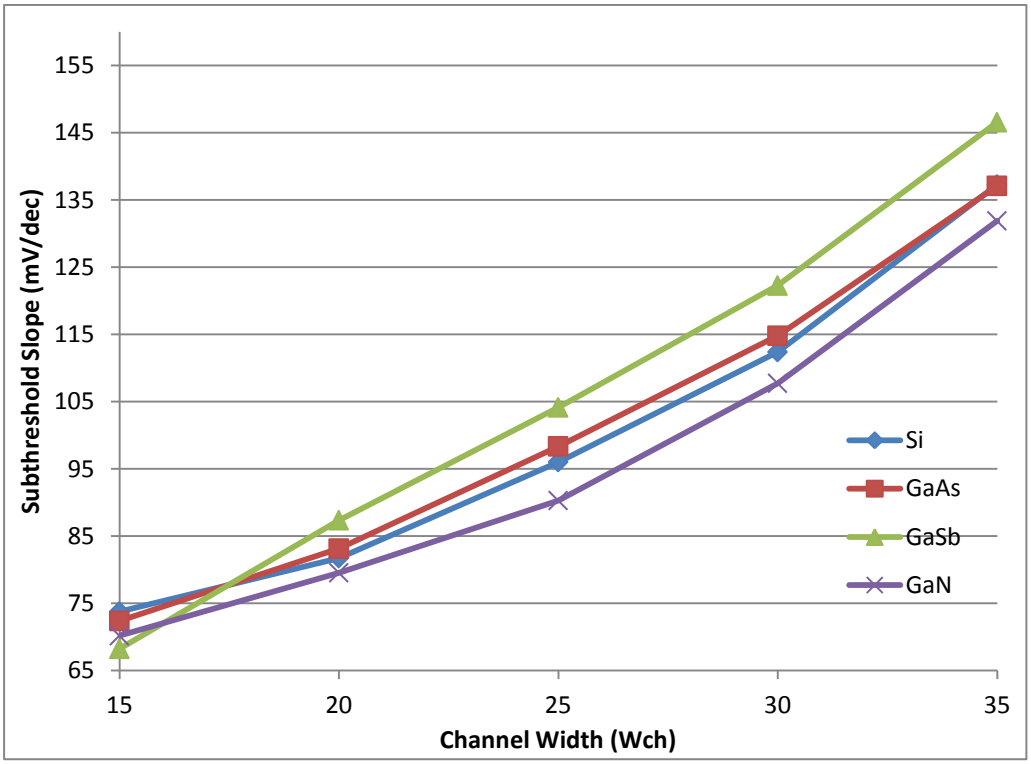


Fig. 6.5. SS vs Channel Width for Si/GaAs/GaSb/GaN channel FinFETs for L_g=45nm and t_{ox1}=t_{ox2}=2nm.

6.3.3. Threshold Voltage versus Gate Length and Channel Width:

Maintaining a proper threshold voltage for a particular device is an important technological parameter, which in case of ultrathin body devices such as FinFETs is adjusted through gate work-function engineering. Further the off-state leakage of a device is associated with the proper adjustment of its threshold voltage, which needs to be higher for low leakages. In order to study the variation of threshold voltage, V_t with respect to L_g and W_{ch}, gate length is varied in the range of 40 to 55nm while as the channel width is varied in the range of 20 to 35 nm.

As the case should be, in general, it is clear that for a given channel material, the threshold voltage rolls off with the reduction in the gate length of the device structure. It is because when the distance between the drain and source is reduced with the reduction in gate length, channel potential becomes more pronounced to drain electric field encroachment, leading to an earlier threshold voltage of gate voltage. Similarly for

smaller channel width devices the two side gates (for the case of a DG FinFET) constitute a strong coupling effect upon the channel electrostatics, leading to a efficiently controlled higher threshold voltage, making the channel less prone to drain potential interference.

Fig. 6.6 illustrates threshold voltage versus gate length variation for Si, GaAs, GaSb and GaN-channel FinFETs. Under the study carried out in Fig. 6.6, the channel width, W_{ch} is kept constant at 30nm, while as the oxide thickness is kept fixed at 2nm. From these characteristics it is clear that the threshold voltage roll-off behaviour of Si-channel FinFET is better in comparison with the other three materials studied.

Fig. 6.7 shows threshold voltage roll-off characteristics studied with respect to fin width or channel width (W_{ch}) for Si, GaAs, GaSb and GaN-channel FinFETs. Under the study carried out in Fig. 6.7, the gate length, L_g is kept constant at 45nm, while as the oxide thickness is kept fixed at 2nm. Again, from the characteristics it is clear that the threshold voltage roll-off behaviour of Si-channel FinFET is better in comparison with the other three materials studied. Further it should be noticed from the Fig. 6.6 and 6.7, that the GaSb channel structure once again shows a worst case for both L_g and W_{ch} variations.

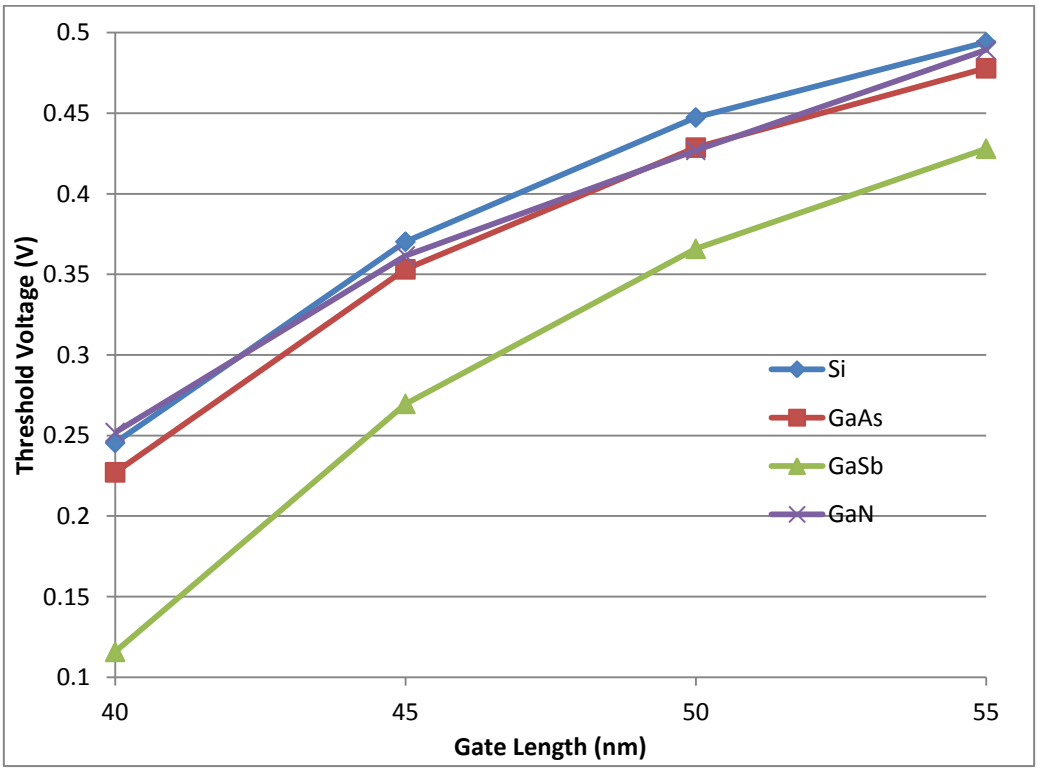


Fig. 6.6. Threshold Voltage vs Gate Length, L_g for Si/GaAs/GaSb/GaN channel FinFETs for W_{ch}=30nm and t_{ox1}=t_{ox2}=2nm.

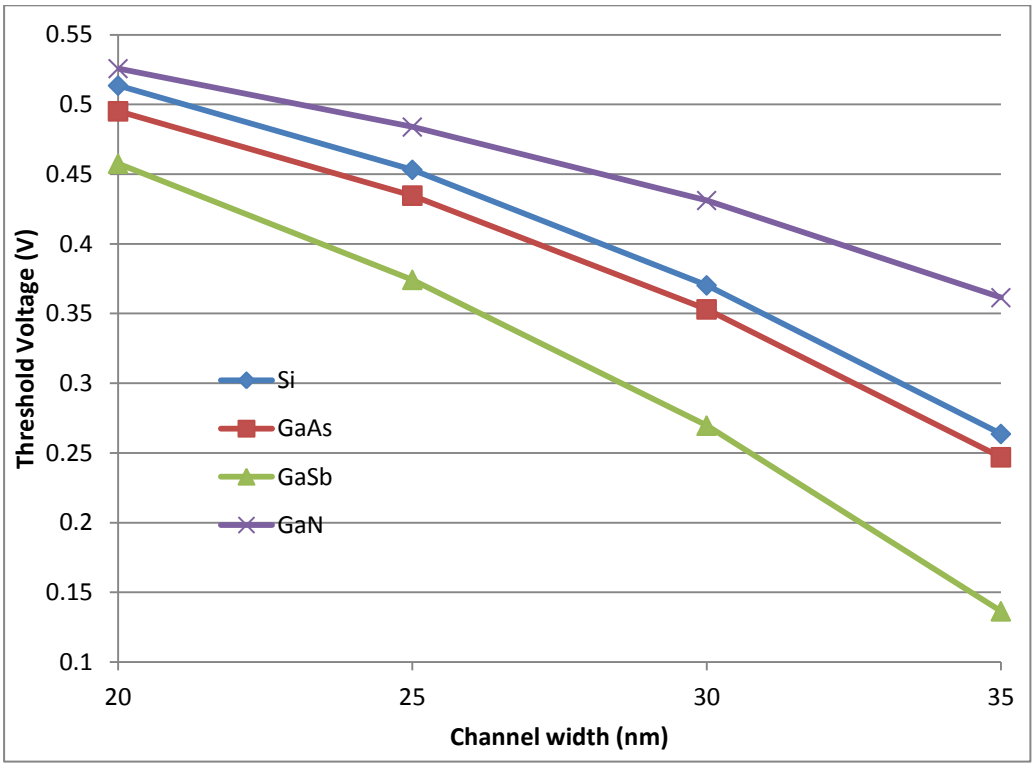


Fig. 6.7. Threshold Voltage vs Channel Width, W_{ch} for Si/GaAs/GaSb/GaN channel FinFETs for L_g=45nm and t_{ox1}=t_{ox2}=2nm.

6.4. Conclusion:

A comparative study of short channel effects viz., DIBL, SS and Threshold voltage roll-off characteristics has been carried out in this chapter for Si, GaAs, GaSb and GaN FinFET devices. The SCE's variation with respect to scaling parameters viz., gate length, L_g and channel width, W_{ch} for these devices have been studied. The results obtained showed that both GaAs and GaN channel devices show better DIBL characteristics with respect to L_g, however for L_g<46nm, GaN FinFET offers better DIBL characteristics with respect to L_g. The DIBL characteristics with respect to W_{ch} show that GaN is better choice, however for W_{ch}<25nm, the DIBL characteristics are almost same for Si, GaAs and GaN FinFET. Study of SS characteristics with respect to L_g and W_{ch} has shown that Si and GaAs FinFET have almost identical SS characteristics with respect to L_g while as GaN FinFET device offers better SS characteristics compared with other three channel materials. At a channel width of 18nm, FinFET devices based on Si, GaAs and GaSb exhibit same value of SS, however, for L_g>18nm, SS behaviour Si and GaAs FinFET is almost same throughout the range of simulation study. Furthermore GaN FinFET has shown better SS characteristics with respect to W_{ch}. Study of threshold voltage roll-off

characteristics has shown that Si channel FinFET has better V_t characteristics with respect to both L_g and W_{ch}. It is worth noting that GaSb FinFET has shown the worst case for all plots, however for W_{ch}<18nm, GaSb has shown good SS characteristics. Based on this simulation study it may be concluded that there is a wide scope of research work that needs to undergo for efficiently selecting a channel material in order to meet the specific requirements of device design for a particular technology node.

Chapter 7
Performance Evaluation and Threshold Voltage Sensitivity to Metal Gate Work-Function in Double-Gate n-FinFET Structures for LSTP

7.1. Introduction:

A very important aspect regarding these FinFET structures is the threshold voltage tuning and its sensitivity to different device parameters. A higher channel doping requirement for the adjustment of threshold voltage may affect the channel mobility of carriers. Further due to random and discrete nature of dopant atoms, the same macroscopic doping profiles differ microscopically. M.-H. Chiang et al. [187] have studied the sensitivity of threshold voltage to channel doping density in extremely scaled MOSFET structures. It has been found that threshold voltage is, in fact, insensitive to doping variation over a wide range of doping density and such insensitivity is further extended by bandgap narrowing in nanoscale MOSFET structures. Device simulations carried out by S. Xiong et al. [3] have shown that threshold voltage is insensitive to channel doping below 1e19 /cm^3. Furthermore increased body doping also leads to corner effects in ultrathin devices like FinFET. Fossum et al. in [100] have conducted 2D analysis of a multiple-gate SOI structure and concluded that the fin body should be left undoped in order to suppress corner effects. A method to suppress the earlier conduction of the corners in the bulk-FinFETs and to achieve a reasonable threshold voltage control with low leakage currents, without increasing the body doping has been proposed in [114]. It has been observed that by increasing the top gate work-function at a fixed side gate work-function of bulk FinFET, threshold voltage increases and off-state leakage current (I_{off}) reduces significantly without increasing doping concentration of fin body. Classical device simulations carried out using Silvaco PISCES in [214] suggest that the optimal gate work-function is such that the gate Fermi level is 0.2eV below (above) the conduction (valence) band edge. Midgap gates have been found inefficient because of severe SCE's. Thus there is a very good scope in engineering the work-function of the gate material in order to get the required threshold voltage in ultrathin body devices like FinFET.

Among the logic technology requirements of MOSFET devices, the LSTP logic technology refers to chips of lower-performance, lower-cost consumer type applications, such as consumer cellular telephones, with lower battery capacity and an emphasis on the lowest possible static power dissipation, i.e., the lowest possible leakage or off-current (highest threshold voltage, V_t). There are difficult challenges to keep the leakage current within tolerable range as predicted by ITRS, while at the same time maintaining a higher threshold voltage requirement in these device structures. Adjustment of threshold voltage through gate work function engineering rather than through channel doping is very efficient because of the limitations imposed on the current drive and mobility in short channel MOS devices. Both poly-silicon and metals have been utilised as gate materials since the evolution of MOS transistor device structures. The aggressive scaling of metal–oxide–semiconductor (MOS) devices requires the implementation of a metal gate in place of conventional polycrystalline silicon (poly-Si) It is because poly-gate devices show a high gate resistance, dopant penetration to channel region, and an increase in equivalent oxide thickness (EOT) due to poly-Si depletion [215]. Metal gates have been found attractive compared to poly-silicon gates since early 1990's due to their chemical stability with the high-k gate dielectric materials. Furthermore it is possible to maintain higher threshold voltages by tuning to a suitable higher metal gate work function while at the same time acquiring high gate stack stability [216-219]. Keeping in consideration the feasibility of gate work-function engineering and the benefits thereof, an imperative study in the field has been carried out. The following sections of the chapter discuss the sensitivity of threshold voltage in case of n-channel double gate FinFET structures with respect to metal gate work-function and investigates the effect of various SCE's on the device performance while at the same time takes care of the required tolerable limit of leakage current (I_{off}) value as predicted by ITRS [1].

7.2. Threshold Voltage Variation and Gate Work-Function Engineering:

The threshold voltage expression for advanced MuGFET device structures can be expressed as [2]

$$V_t = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} + v_{in} \qquad (1)$$

where Q_{in} represents charges in the gate dielectric, c_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, Φ_{ms} represents metal-semiconductor work-function

difference between the gate electrode and the semiconductor, Φ_f is the fermi potential given by

$$\Phi_f = \frac{kT}{q} ln(\frac{N_D}{n_i}) \quad (2)$$

where N_D and n_i are donor concentration in channel and intrinsic carrier concentration respectively.

For ultrathin body and lightly doped devices, in addition to N_D, the effect of Q_D and Q_{ss} on threshold voltage, V_t in equation (1) is negligible compared to Φ_f. Further v_{in} is the additional surface potential to $2\Phi_f$ that is needed for ultrathin body devices to bring enough inversion charges in to the channel region of the transistor to reach threshold point. Therefore the work-function of gate electrode is the main parameter for threshold voltage determination in case of MuGFET devices.

7.3. Device Structure and Simulation Strategy:

A 2-D view of device structure of FinFET is as shown in Fig. 7.1, specifying various device parameters undertaken for simulation study. The structure consists of channel length, L_g (also called gate length), channel width W_{ch}, which is also referred to as fin width or fin thickness, T_{fin} in case of triple gate FinFET, wherein top gate is made active by making the top oxide very thin. Further the thickness of gate oxide material is specified by t_{ox1} and t_{ox2} (or EOT)

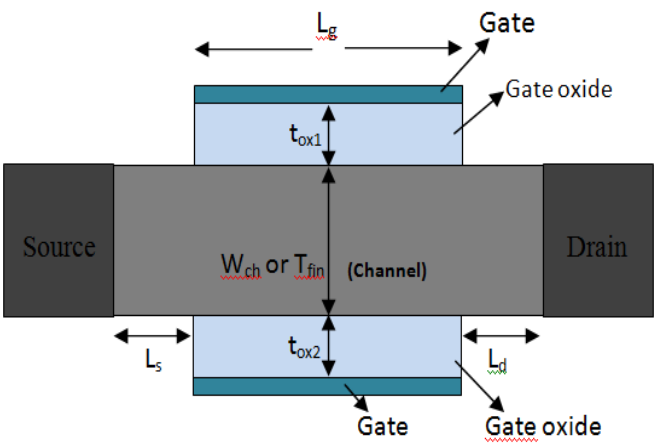


Fig. 7.1. Two Dimensional Double-Gate n-FinFET structure

which is placed on either of the side walls of fin and at the top surface of the fin, before a gate contact is made. The various parameters of device structure undertaken for the present study are as per the projection report of ITRS-2011 update for LSTP technology,

projected for the year 2015. Some of the parameters are also user defined. These parameters of FinFET structure are as listed in the following Table 7.1.

Table 7.1. Device parameters undertaken for the simulation study

Device parameters	**Values undertaken**
Physical Gate Length (L_g)	*20 nm*
Equivalent Oxide Thickness (EOT)	*1.2 nm*
V_{dd} (Power Supply Voltage)	*0.86 V*
Fin width (W_{ch})	*12.5nm*
*Channel Doping**	*4×10^{18} cm^{-3}*
*Drain/Source Doping**	*1×10^{21} cm^{-3}*
$I_{sd,leakage}$	*10 pA/µm*
*Extension length to Source /Drain (L_s & L_d)**	*30 nm*

**User defined values*

In the present study, device simulations have been carried out using PADRE simulator from MuGFET [220]. PADRE, which is based on the drift diffusion simulations, is being utilised for the device simulations, because of the fact that subthreshold characteristics of device are still diffusion dominated and reflect device characteristics in the subthreshold region well [221],[81]. The drift diffusion simulator is way faster than the quantum transport simulator that provides physical insight of the device. Also the quantum mechanical effects become negligible while simulating the transistor structures with lateral dimensions greater than 10nm. A comparison of experimental results obtained in [209] for the subthrehold I_d-V_g characteristics with the simulation results using MuGFET simulator has been given in [210], which clearly indicates the accuracy and validity of classical drift diffusion simulation results.

7.4. Simulation Results:

7.4.1. Threshold Voltage Variation with Metal Gate Work-Function:

As discussed earlier the work-function of the metal gate can be tuned to meet a given threshold voltage requirement. MOS transistors fabricated using Mo (Molebidinum) gate have been reported to have a gate work-function value of 5eV [218]. During the simulation work, the threshold voltage, V_t variation of FinFET has been studied for the

gate work function ranging from 4.291 to 5.2eV. It has been found that by increasing the Gate work-function of FinFET, the corresponding threshold voltage increases to a desired value as described in Fig. 7.2. Maintaining higher threshold voltage is a required condition for LSTP logic technologies and hence can be achieved more efficiently by increasing work-function of the metal gate material.

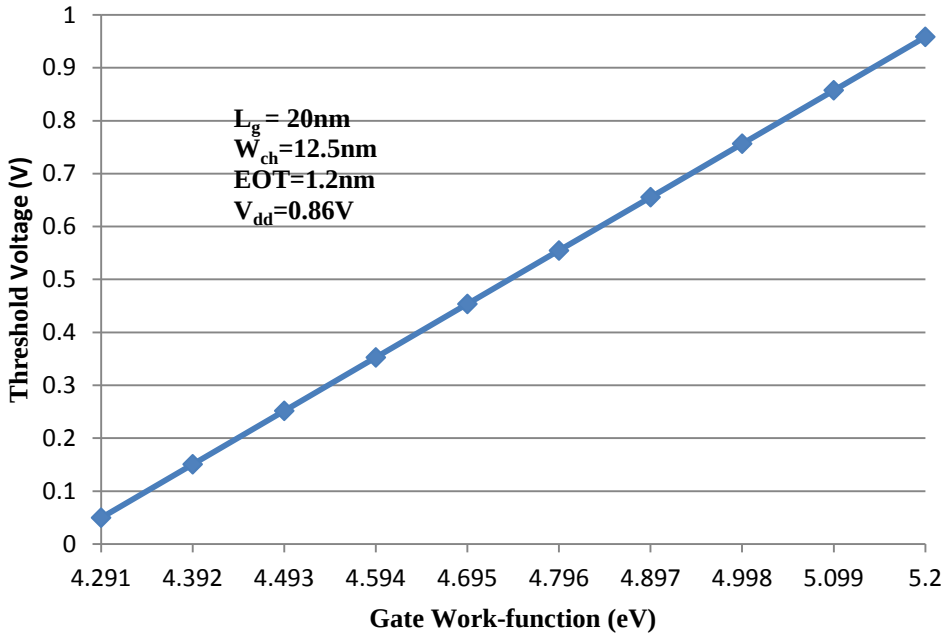


Fig. 7.2. Threshold Voltage versus gate work-function of n-FinFET

7.4.2. Performance Evaluation Based on Study of SCE's:

In the present study, while studying the threshold voltage variation with respect to metal gate work-function of FinFET device, the performance evaluation based on the effect of varying gate work-function on DIBL, SS, Off-current, On-Current and On/Off current ratio of device has been carried out. Furthermore the variation of transfer characteristics (I_{ds} versus V_{gs}) with respect to gate work-function has also been presented for analyzing the subthreshold behavior of device with respect to gate work-function.

(a) Transfer Characteristics:

Fig. 7.3 shows the variation of I_{ds} versus V_{gs} characteristics of finFET for different values of gate work-function, varying from 4.291 to 5.2eV. As depicted in the characteristic curves, subthreshold behaviour of device improves as the metal gate work-function is increased to higher values. It is because as the metal gate work-function increases, the corresponding threshold voltage increases, which further reduces the off-

state leakage current and improves the device performance in order to be used for LSTP applications.

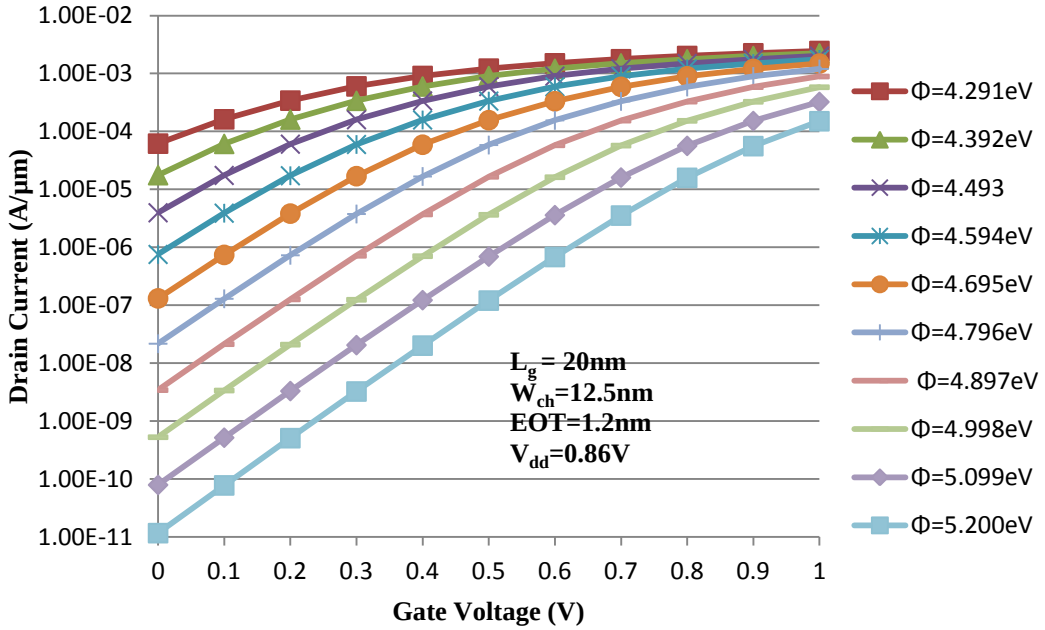


Fig. 7.3. Transfer characteristics of finFET for different values of gate work-function

(b) On Current:

The device on-current behavior as a function of gate workfunction has been illustrated as shown in Fig. 7.4. It is clear that device on-current is sacrificed for increased threshold voltage due to increased metal gate work-function of FinFET structure.

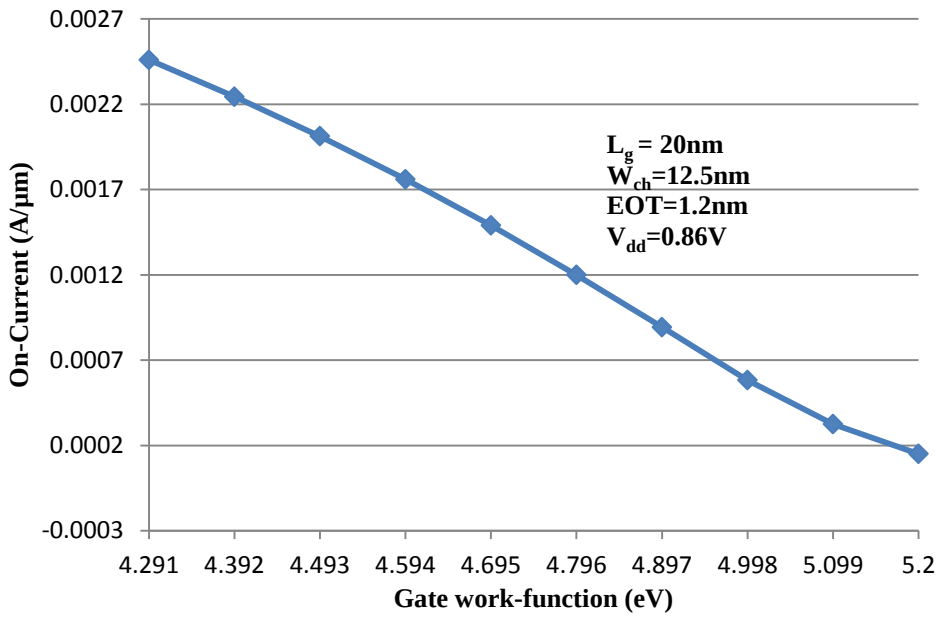


Fig. 7.4. On-current versus gate work-function of n-FinFET

(c) Off Current:

For LSTP technology logic, the off state leakage current requirement as projected by the ITRS 2011 report is of the order of 10pA/µm at room temperature. It is clear from the given off-state device characteristics shown in Fig. 7.5 that a higher gate work-function approximately 5eV can fulfil the tolerable off-current projection of the given FinFET structure.

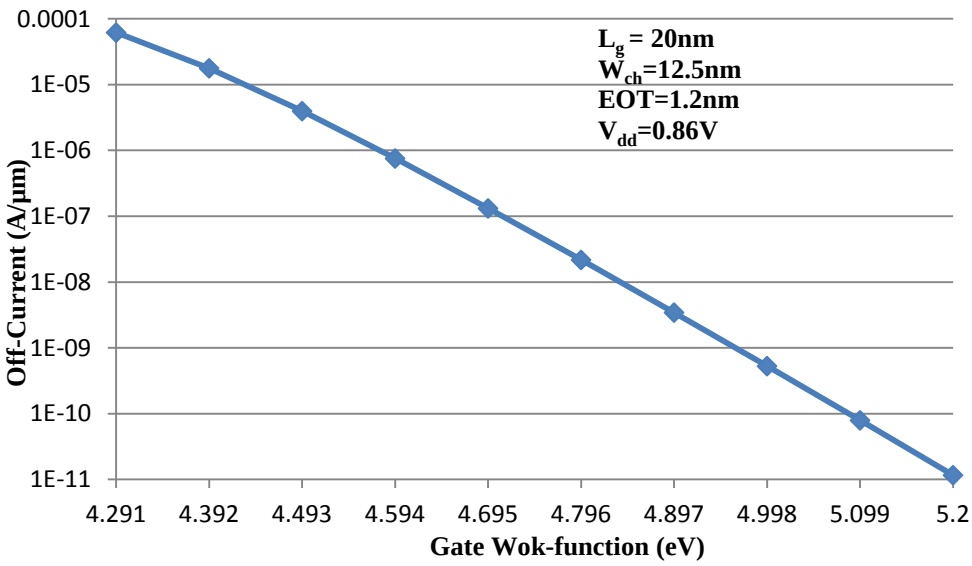


Fig. 7.5. Off-current versus gate work-function of n-FinFET

(d) On/Off Current Ratio:

As shown in Fig. 7.6, the on/off current ratio obtained from the device simulations has

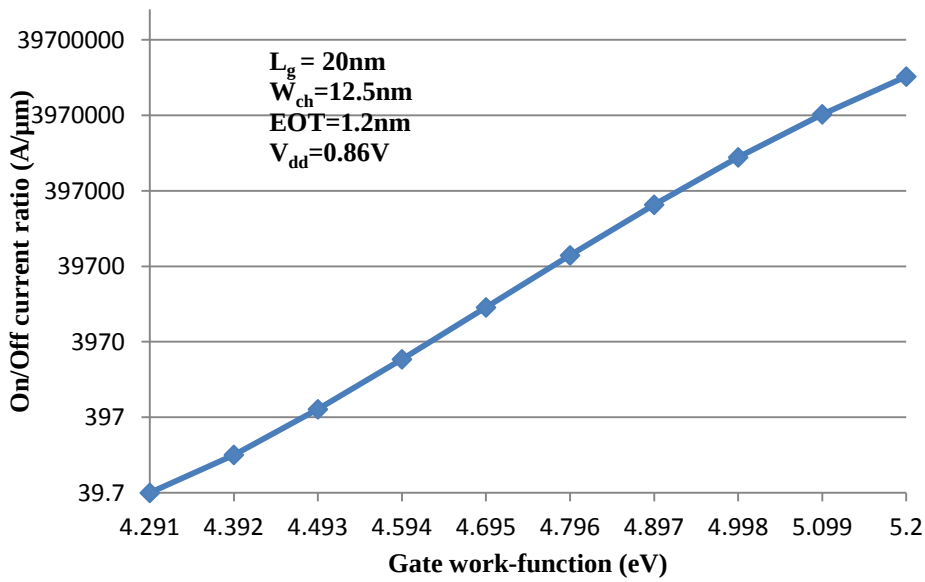


Fig. 7.6. On/Off current ratio versus gate work-function of n-FinFET

been found to improve significantly with the increase in metal gate work-function of FinFET. Although the device on current has been reduce to some extent with an increase in gate work-function, but an increase in on-off current ratio is a clear indication of overall improvement in drive current with a required low off-state leakage current for LSTP logic technology.

(e) Drain Induced Barrier Lowering (DIBL):

DIBL is one of the critical short channel effect parameter of nanoscale device structures, since it estimates the overall gate control of the device on the channel electrostatics of the device. The effect of DIBL is to reduce the threshold voltage in nanoscale MOS devices due to a modulation of the source to drain channel potential barrier by the drain voltage to make the conduction of device channel possible for smaller gate voltages. From Fig. 7.7, it is clear that DIBL gets reduced with the increase in gate work function. It is because with increase in threshold voltage due to increased gate work-function, barrier lowering effect is reduced for a given drain source voltage in short channel FinFET devices.

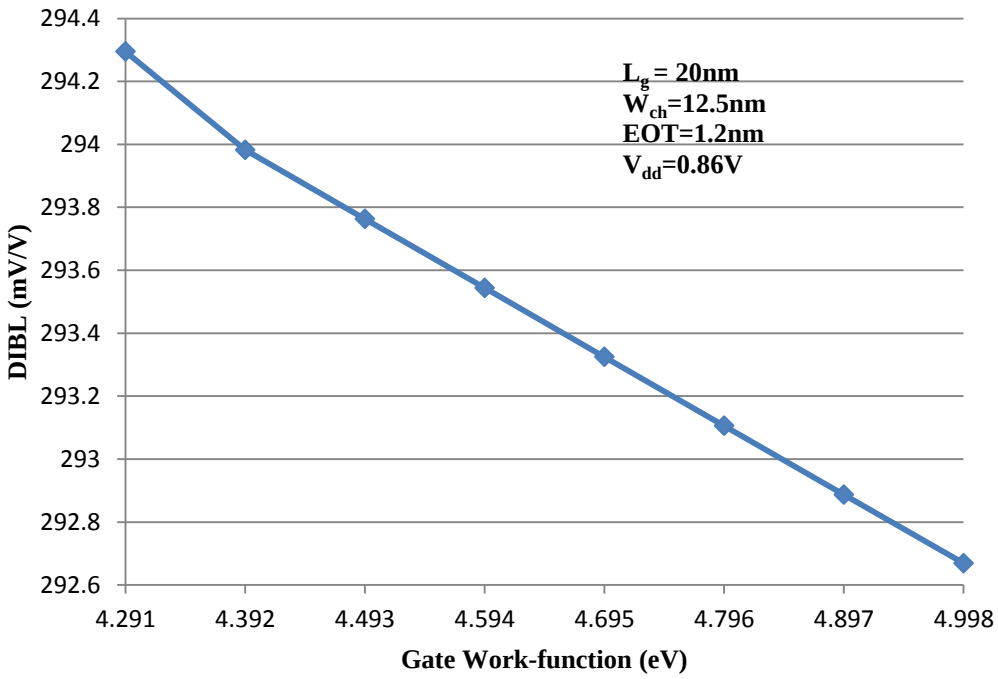


Fig. 7.7. DIBL versus gate work-function of n-FinFET

(f) Subthreshold Slope (SS):

The plot of subthreshold slope versus gate work-function of FinFET is as shown in Fig. 7.8. It is clear that subthreshold slope of given FinFET structure improves with the

increase in gate work–function of the device. The improved SS characteristic is as a result of increased device threshold voltage.

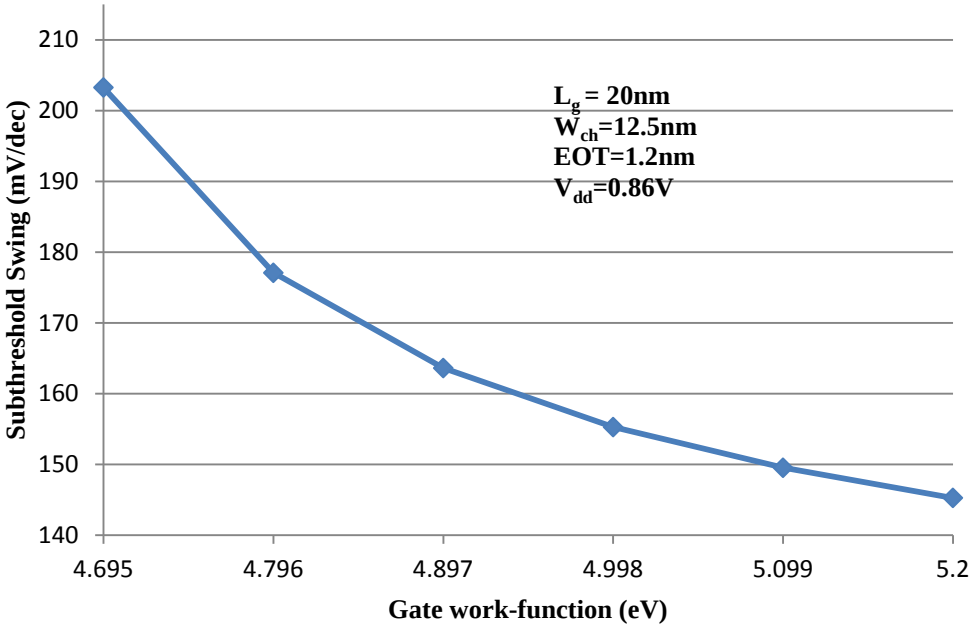


Fig. 7.8. Subthreshold Swing versus gate work-function of n-FinFET

7.5. Conclusion:

The study presents the effectiveness of gate work-function engineering for the adjustment of threshold voltage in nanoscale FinFET structures. Utilization of metal gates have been proposed for nanoscale FinFET devices due to their capability to withstand high-k gate dielectric materials that are very much essential for the continuous downscaling of device structures. The efficiency of utilizing metal gates has been presented by studying the variation of threshold voltage in FinFETs with respect to metal gate work-function. An analysis based on the evaluation of corresponding SCE's and device performance has been presented that supports utilization of metal gate work-function performance for such devices to be used for LSTP logic technology applications. During the simulation study, it has been observed that engineering threshold voltage through variation of metal gate work-function of FinFET can produce FinFETs that may have reduced SCE's and higher device performance. Varying the device gate work-function is found effective in adjusting the threshold voltage to a desired value. The increased gate work-function improves the DIBL, SS, Off-current, On/Off current ratio, but causes a reduction in device On-current.

Chapter 8
Simulation Tool used for Study of FinFET Structures

8.1. Introduction to nanoHUB:

Simulation and modelling in the advancement of nanoscience and nanotechnology enable researchers and device engineers to produce innovative theories, novel ideas of future research and education that have very close relation with the experimental research and to education. Nanotechnology involves developing materials, structures, or devices where at least two dimensions are between 1 and 100 nanometers in size. Nanoscale engineering, science, and technology have captured the imagination of many scientists and engineers. Electrical engineers tend to think of nanotechnology as the "science of making things small." For example, smaller to make transistors run faster, use less power, and allow engineers to put more of them in the same space. Therefore, a whole device may now "just" have 10 million atoms, or it might even be as small as 50,000 atoms.

The website nanoHUB.org is the place for computational nanotechnology research, education, and collaboration. nanoHUB hosts a rapidly growing collection of simulation programs for nano-scale phenomena that run in the cloud and are accessed through web browser. It aims facilitating pioneering research, education, outreach, and support for nanotechnology community formation and growth. The community use nanoHUB.org to spark new modes of discovery, innovation, learning, and engagement that will accelerate the transformation of nanoscience to nanotechnology. Established in 2002, the Network for Computational Nanotechnology (NCN) is funded by the National Science Foundation to support the National Nanotechnology Initiative with nanoHUB.org, a cyber-community for theory, modeling, and simulation now serving over 170,000 researchers, educators, students, and professionals annually. NCN seeks to 1) engage an ever-larger and more diverse cyber-community sharing novel, high-quality research and educational resources that spark new modes of discovery, innovation, learning, and engagement; 2) accelerate the transformation of nanoscience to nanotechnology through tight linkage of simulation to experiment; 3) develop open-source software; and 4) inspire and educate the next workforce generation. nanoHUB provides online simulation for over 160 tools right from web browser. All of these tools appear to run as applets in

browser window, but they are actually powered by a much more sophisticated middleware that lets transparently tap into Purdue and national grid resources [222].

8.2. MuGFET Device Simulator:

"MuGFET" is a simulation tool for nano-scale multi-gate FET structure available on nanoHUB [209]. MuGFET users can either use PROPHET or PADRE simulators which provide self-consistent solutions to the Poisson and drift-diffusion equation. At the nanometer scale, quantum transport approaches that are based on a full 3D Poisson-Schrödinger solution like the "nanowire Lab" or the atomistically resolved "Bandstructure Lab" are needed to provide insight into transport. However, for devices that are 10nm or larger, semi-classical approaches can provide some significant insight. For device domains 30nm or larger, quantum approaches as implemented in today's simulators, may not contain enough physics of scattering and dephasing (mechanism that recovers classical behaviour from a quantum system). Therefore, there are some advantages in using classical simulation approaches over quantum simulation approaches for certain classes of device regimes. The drift-diffusion type simulator works well enough to demonstrate characteristics of relatively long and large devices. Further the subthreshold characteristic is still diffusion dominated. The on-current can never be overestimated by the drift diffusion simulation. Drift diffusion simulations are significantly faster than quantum ballistic simulations and also fairly well fitted to experimental results [223]. A comparison of experimental results obtained in [220] for the subthrehold I_d-V_g characteristics with the simulation results using MuGFET simulator have been given in [221], which clearly indicates the accuracy and validity of classical drift diffusion simulation results.

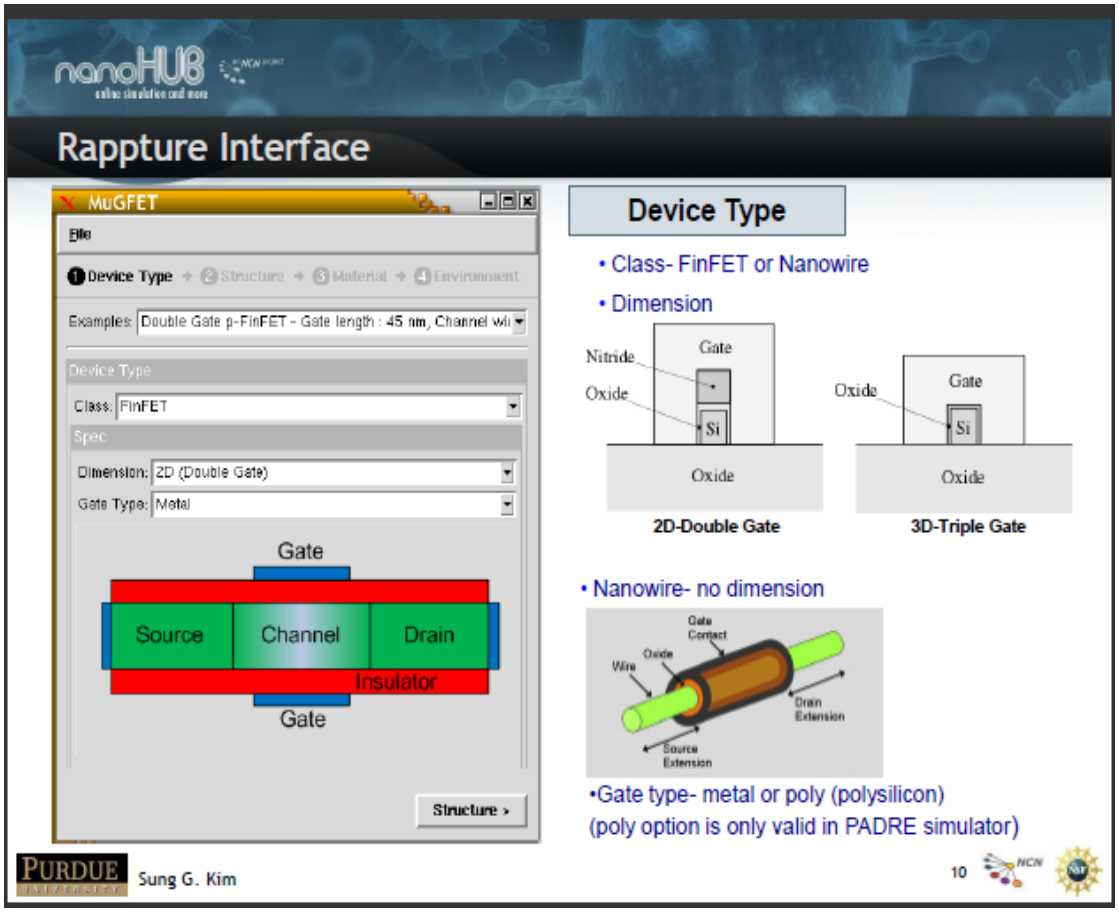
PROPHET is a general PDE (partial differential equation) solver for 1, 2, or 3 dimension. It is developed in Bell Laboratories as a process simulator [224]. Because of its capability of adopting new simulation modules to the core solver, it is used in various semiconductor device simulations.

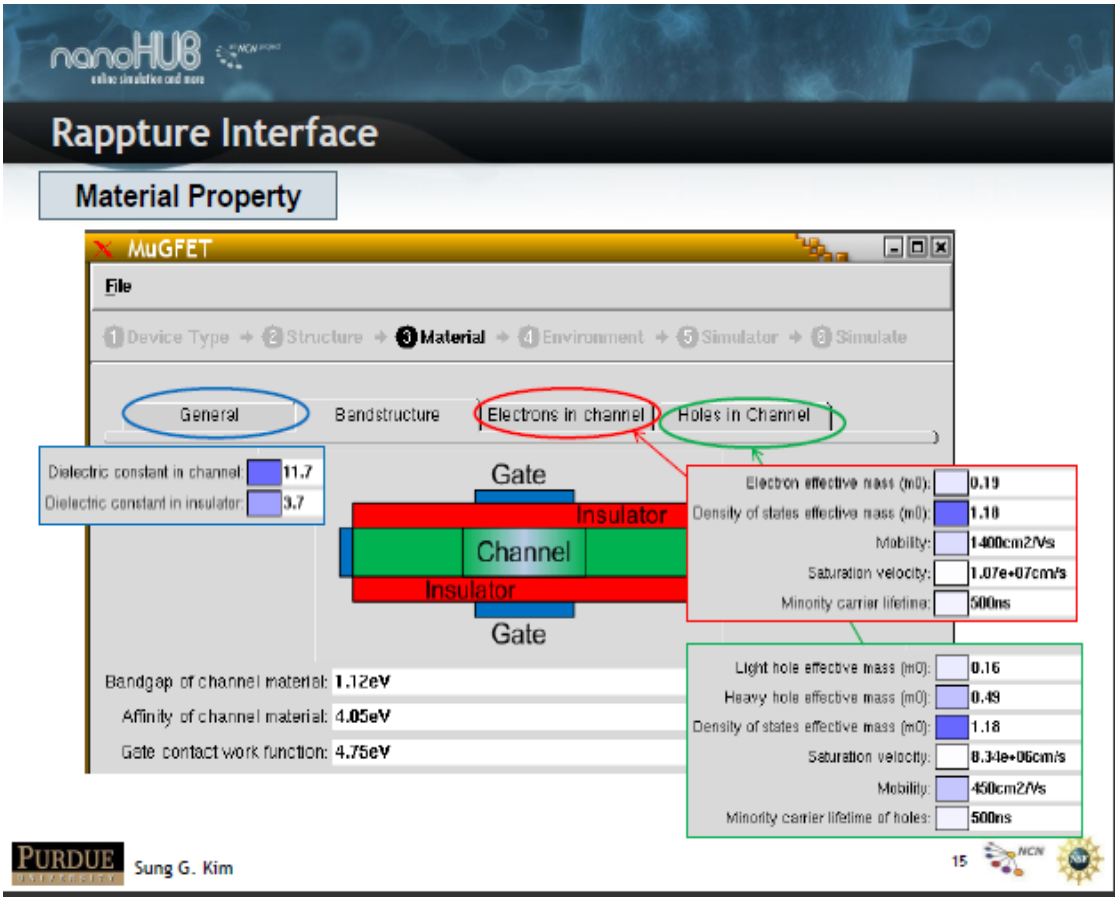
PADRE is a device-oriented simulator for 2D/3D devices with arbitrary geometries which has also been developed at Bell Telephone Laboratories. It provides many useful plots for engineers and deep understanding of physics of devices. Many options are provided with respect to the numerical methods and semiconductor device physics. The numerical methods in PADRE are extremely robust. It can include hot-carrier transport

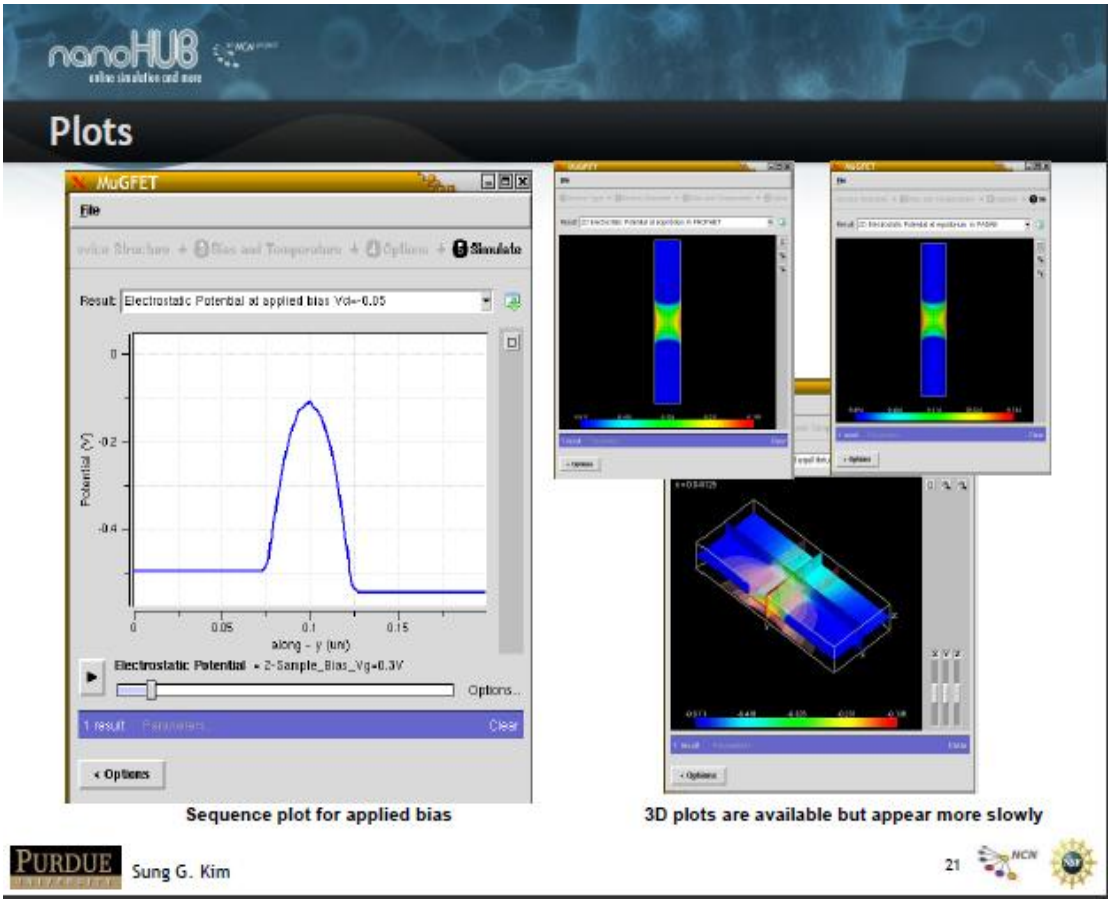
by solving energy balance equation. The velocity of carriers in the channel region is fitted to the Monte Carlo simulation results [225].

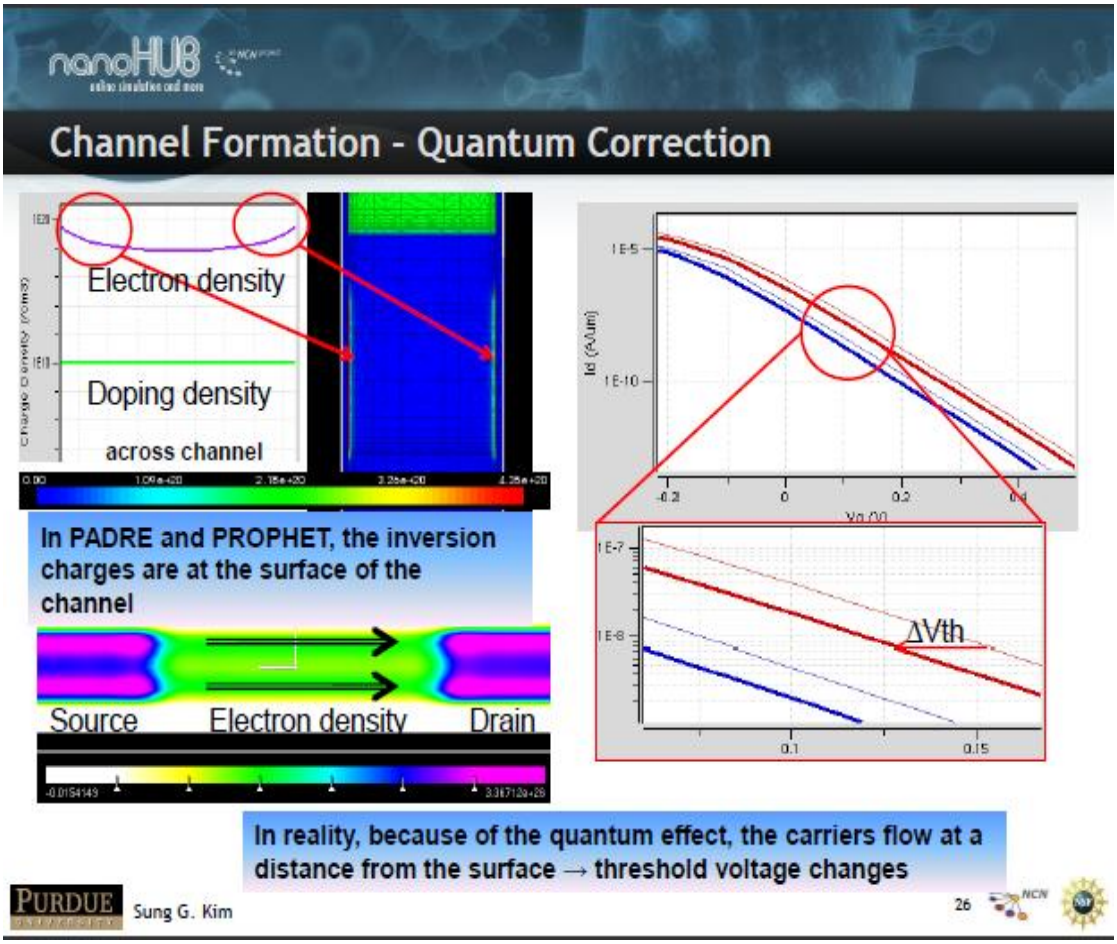
MuGFET tool is user-friendly graphical user interface for users to simulate FinFET (both double gate and triple gate) and nanowire-FET structure using either PROPHET or PADRE. It provides a lot of useful plots such as device I-V characteristics , threshold voltge, Subthreshold Slope (SS), Drain Induced Barrier loweing (DIBL), device on current, off current, on/off current ratio, etc. and hence can provide insight of the various SCE's (Short Channel Effects) in MuGFET devices.

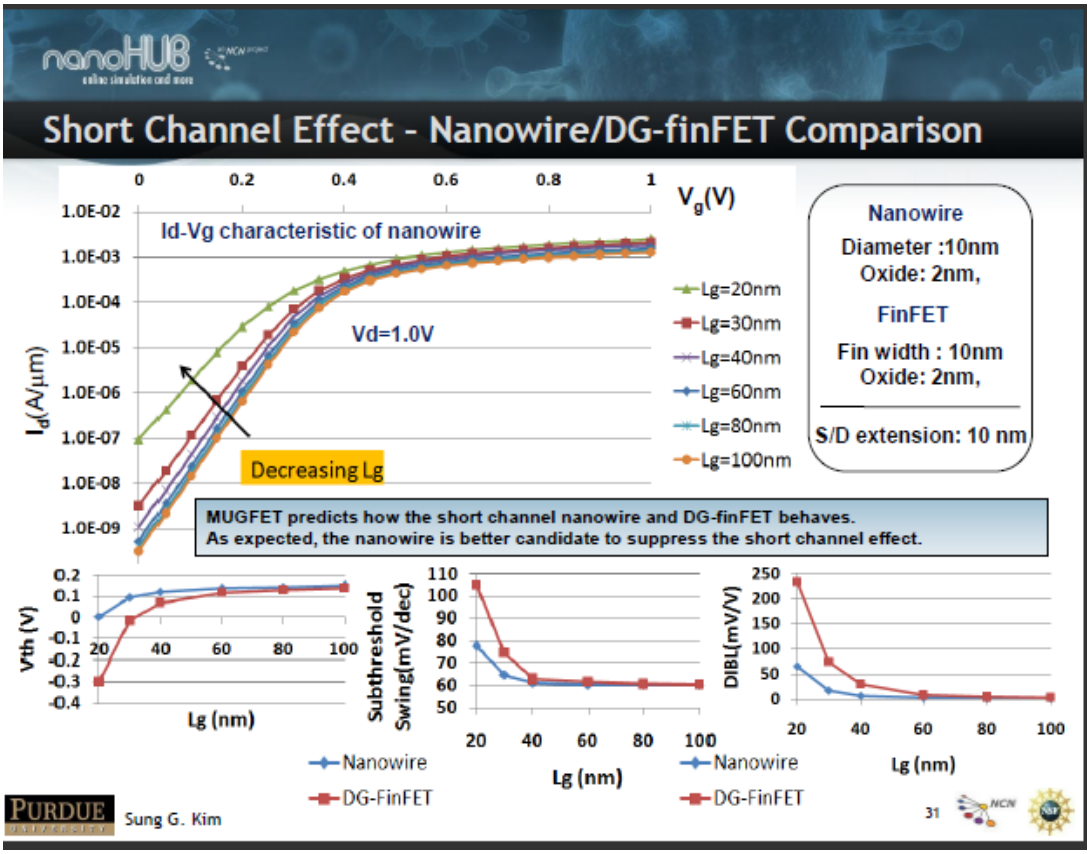
FinFET structures with scaling and process parameter variations can be simulated both as n-channel and p-channel structures, as required using MUGFET tool from nanoHUB. The simulation results that can be obtained from MUGFET simulations can be interpreted in 2 and 3-dimensional plots. The three dimensional view of the FinFET structure can also be obtained in the simulation results, which include a graphics view of electron and hole concentration in the device structure, potential contour distributions inside the device etc. Various scaling parameters as well as process parameters for these devices can be given as input in order to simulate the different variants of FinFET device structure. The scaling parameters that one can input for a particular simulation study are gate length, channel width or fin thickness (in case of triple gate structures), fin height, extension length to source and drain, equivalent oxide thickness etc. All these parameters are provided as input for a given device structure in nanometre (nm) units. Similarly various process parameters that can be used as input are doping concentration in channel and source/drain region, doping type viz., p-type or n-type. Further doping profiles can be selected as constant or Gaussian doping profiles. Gaussian doping profile with adjustable characteristic length starts from the end of the source/drain extension region, wherein the doping falls off exponentially towards the channel region. Characteristic length for Gaussian doping profile is the length to which the doping drops by the factor exp (-1) towards the channel region. As an illustration, some screen shots have been shown in Fig. 8.1 representing some of the features of MuGFET simulator.


nanoHUB
Rappture Interface
MuGFET
File
1 Device Type → 2 Structure → 3 Material → 4 Environment
Examples: Double Gate p-FinFET - Gate length : 45 nm, Channel wi
Device Type
Class: FinFET
Spec
Dimension: 2D (Double Gate)
Gate Type: Metal
Gate
Source
Channel
Drain
Insulator
Gate
Structure >
Device Type
• Class- FinFET or Nanowire
• Dimension
Nitride
Oxide
Gate
Si
Oxide
2D-Double Gate
Oxide
Gate
Si
Oxide
3D-Triple Gate
• Nanowire- no dimension
Gate Contact
Oxide
Wire
Drain Extension
Source Extension
•Gate type- metal or poly (polysilicon)
(poly option is only valid in PADRE simulator)
PURDUE
Sung G. Kim
10


nanoHUB
Rappture Interface
Material Property
MuGFET
File
1 Device Type → 2 Structure → 3 Material → 4 Environment → 5 Simulator → 6 Simulate
General
Bandstructure
Electrons in channel
Holes in Channel
Dielectric constant in channel: 11.7
Dielectric constant in insulator: 3.7
Gate
Insulator
Channel
Insulator
Gate
Electron effective mass (m0): 0.19
Density of states effective mass (m0): 1.18
Mobility: 1400cm2/Vs
Saturation velocity: 1.07e+07cm/s
Minority carrier lifetime: 500ns
Light hole effective mass (m0): 0.16
Heavy hole effective mass (m0): 0.49
Density of states effective mass (m0): 1.18
Saturation velocity: 8.34e+06cm/s
Mobility: 450cm2/Vs
Minority carrier lifetime of holes: 500ns
Bandgap of channel material: 1.12eV
Affinity of channel material: 4.05eV
Gate contact work function: 4.75eV
PURDUE
Sung G. Kim
15


nanoHUB
Plots
MuGFET
File
Simulate
Result: Electrostatic Potential at applied bias Vd=-0.05
Potential (V)
along - y (um)
Electrostatic Potential - Z-Sample_Bias_Vg=0.3V
Options...
1 result
Clear
< Options
Sequence plot for applied bias
3D plots are available but appear more slowly
PURDUE
Sung G. Kim
21


nanoHUB
Channel Formation - Quantum Correction
Electron density
Doping density
across channel
Charge Density (/cm3)
In PADRE and PROPHET, the inversion charges are at the surface of the channel
Source
Electron density
Drain
Id (A/um)
ΔVth
In reality, because of the quantum effect, the carriers flow at a distance from the surface → threshold voltage changes
PURDUE
Sung G. Kim
26



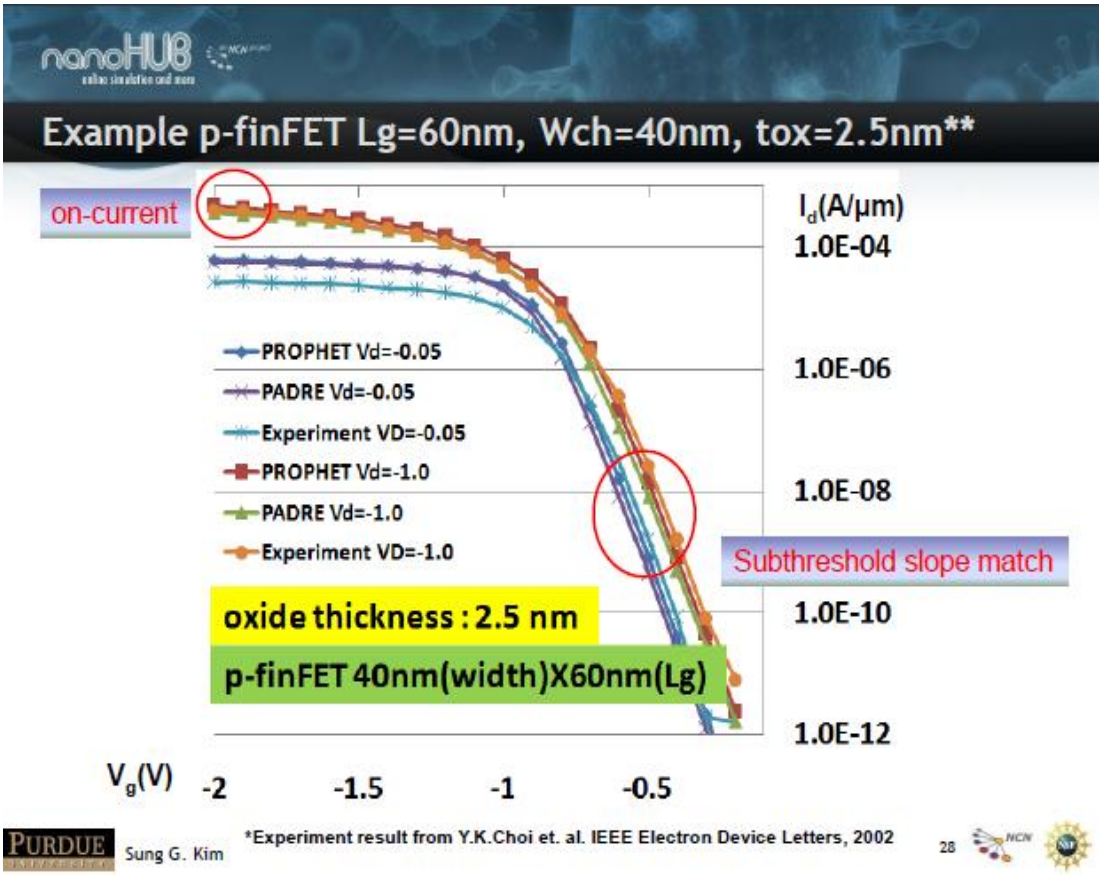


Fig. 8.1. Screen shots of MuGFET device simulator.

8.3. Theory of Drift Diffusion Modeling of Semiconductors:

Numerical simulations provide to be the main tool for reducing the time of a design cycle. For this purpose hierarchy of models is employed, which range from microscopic, like the Boltzmann-poisson or the winger-Poisson model, to macroscopic models, like the energy transport, the hydrodynamic and the drift diffusion model (DD). Most popular and widely used in commercially available simulation packages is the DD, which allows for a very efficient numerical study of the charge transport in many cases of practical relevance, since it allows for an accurate description of the underlying physics in combination with low computational cost.

There are three basic equations that constitute the DDE model. Firstly *Poisson's equation* which is derived from the fundamental laws of electromagnetics, and must always be satisfied. Thus all approaches to device modelling must solve *Poisson's equation* in some form. It is basically the relationship between the local charge density ρ and the electric field, E that the charge produces [226].

$$\nabla.(\varepsilon\, E) = \rho \qquad (1)$$

where ε is the dielectric constant, E is the electric field and ρ is the net charge density. Since $E = -\nabla\psi$, therefore Equation (1) can be represented as,

$$\nabla^2(\psi) = -\frac{q}{\varepsilon}[p - n + N_D^+ - N_A^-] \qquad (2)$$

where ψ is the electric potential, q is the elemental charge, n and p are electron and hole charge carrier concentrations and N_D^+, N_A^- are donor and acceptor doping concentrations.

The two *continuity equations* complete the set of partial differential equations describing the DDE set. They ensure that charge conservation is maintained in the device irrespective of the device material to be used. They can be stated in their general form as:

$$\frac{\partial n}{\partial t} = Gn - Un + \frac{1}{q}(\nabla.Jn) \qquad (3)$$

$$\frac{\partial p}{\partial t} = Gp - Up + \frac{1}{q}(\nabla.Jp) \qquad (4)$$

for electrons and holes respectively.

where G_n, and G_p are the electron and hole generation rate (cm^{-3}/s), respectively, caused by external influences such as the optical excitation with high-energy photons or impact ionization under large electric fields. The electron recombination rate in p-type semiconductors is U_n. Under low injection conditions (i.e, when the injected carrier

density is much less than the equilibrium majority carrier density), U_n can be approximated by the expression: $\frac{n_p - n_{p0}}{\tau_n}$, where n_p is minority carrier density, n_{p0} the thermal equilibrium minority carrier density, and τ_n the electron (minority) lifetime. There is a similar expression for the hole recombination rate with life time τ_p. If the electrons and holes are generated and recombined in pairs with no trapping or other effects, $\tau_n = \tau_p$. Several different recombination and generation mechanisms such as Schockley-Read-Hall (SRH), Auger recombination mechanisms are incorporated in to the DD simulations to model the recombination generation events.

The electron and hole carrier concentrations denoted by n and p can be described by Boltzmann statistics:

$$n = n_i \, exp \frac{q(\psi - \Phi_n)}{kT} \qquad (5)$$

where ψ is electric potential, Φ_n and Φ_p are quasi-fermi potentials for electrons and holes respectively [227].

In the drift diffusion model the currents of electrons and holes are described as the sum of two contributions, namely the drift component, proportional to the electrostatic field (E=-$\nabla\psi$), and a diffusion component, proportional to the gradient of carrier density.

$$J_n = q\mu_n n(\nabla\psi) + q\, D_n\, \nabla(n) \quad \textit{(electron current density)} \qquad (6)$$

$$J_p = q\mu_p p(\nabla\psi) - q\, D_p\, \nabla(p) \quad \textit{(hole current density)} \qquad (7)$$

In equations (6) and (7) the diffusion component ($q\, D_n\, \nabla n$, $q\, D_p\, \nabla p$) dominate before the inversion channel is formed and the drift component ($q\mu_n n(\nabla\psi) = q\mu_p p(\nabla\psi)$) dominate beyond the inversion channel formation.

The charge transport properties are described using mobilities, μ_n and μ_p and the corresponding diffusivities, D_n and D_p, which are assumed to be related by the Einsteins relationships,

$$D_n = \frac{kT}{q}\mu_n \quad \textit{(for electrons)} \qquad (8)$$

$$D_p = \frac{kT}{q}\mu_p \quad \textit{(for holes)} \qquad (9)$$

As mentioned before the conventional drift diffusion model solves the three partial differential equations for the three variables *viz.*, potential, electron and hole concentration ($\psi, n, and\ p$) using Newton method. The Newton method is preferred because of its usefulness for the system of equations which are strongly coupled. The Poisson equation is always solved, and optionally one can specify that continuity and/or energy balance partial differential equation (PDE's) be solved for the carriers [228].

8.3.1. Energy Balance Equation:

The conventional drift-diffusion model of charge transport neglects non-local transport effects such as velocity overshoot, diffusion associated with the carrier temperature and the dependence of impact ionization rates on carrier energy distributions. These phenomena can have a significant effect on the terminal properties of submicron devices. The energy balance model implemented in PADRE introduces two new independent variables T_n and T_p, the carrier temperature for electrons and holes. The energy balance equations consist of an energy balance equation with the associated equations for current density, $\boldsymbol{J}_{n,p}$ and an energy flux $\boldsymbol{S}_{n,p}$. For electrons, the energy balance equation consists of [228]

$$\nabla.\boldsymbol{S}_n = -\boldsymbol{J}_n.\nabla\psi - W_n - \frac{3k}{2}\frac{\partial}{\partial t}(\lambda_n^* n T_n^*) \quad (10)$$

$$\boldsymbol{J}_n = qD_n\nabla n - \mu_n n\nabla\psi + qnD_n^T\nabla T_n \quad (11)$$

$$\boldsymbol{S}_n = -k_{\boldsymbol{n}}\nabla T_{\boldsymbol{n}} - (\frac{\boldsymbol{\kappa}\delta_n}{q})\boldsymbol{J}_n T_n \quad (12)$$

where $\boldsymbol{J}_n$ is current density equation**,** $\boldsymbol{S}_n$ is the energy flux density associated with electrons, W_n is the energy density loss rate for electrons, K_n is the thermal conductivity for electrons, D_n is the thermal diffusivity and μ_n is the electron mobility. The remaining terms are defined by the following equations:

$$D_n = \frac{\mu_n k T_n}{q}\lambda_n \quad (13)$$

$$\lambda_n = \frac{F_{\frac{1}{2}}(\eta_n)}{F_{-\frac{1}{2}}(\eta_n)} \quad (14)$$

$$\eta_n = \frac{E_{Fn} - E_c}{kT_n} \quad (15)$$

$$D_n^T = \left(\mu_{2n} - \frac{3}{2}\lambda_n\mu_n\right)\frac{k}{q} \quad (16)$$

$$\mu_{2n} = \mu_n\left(\frac{5}{2} + \xi_n\right)\frac{F_{\xi_n+3/2}(\eta_n)}{F_{\xi_n+1/2}(\eta_n)} \quad (17)$$

$$K_n = qn\mu_n\left(\frac{k}{q}\right)^2 \Delta_n T_n \quad (18)$$

$$\Delta_n = \delta_n\left[\left(\frac{7}{2} + \xi_n\right)\frac{F_{\xi_n+5/2}(\eta_n)}{F_{\xi_n+3/2}(\eta_n)} - \left(\frac{5}{2} + \xi_n\right)\frac{F_{\xi_n+3/2}(\eta_n)}{F_{\xi_n+1/2}(\eta_n)}\right] \quad (19)$$

where, $\lambda_n = 1$ (20)

$$\Delta_n = \delta_n = \left(\frac{5}{2} + \xi_n\right) \quad (21)$$

$$\xi_n = \frac{T_n}{\mu_n}\left(\frac{\partial\mu_n}{\partial T_n}\right) \quad (22)$$

Similar equations hold for holes.

8.4. Conclusion:

"MuGFET" is a drift diffusion simulator, which provides self-consistent solutions to the Poisson and drift-diffusion equation. The drift-diffusion type simulator works well enough to demonstrate characteristics of relatively long and large devices. For devices that are 10nm or larger, quantum mechanics is not dominant. So it is advantageous to use classical simulations over quantum mechanical simulations because the quantum approaches as implemented in today's simulators, may not contain enough physics of scattering and dephasing (mechanism that recovers classical behaviour from a quantum system). The subthreshold characteristics of these devices are still diffusion dominated. The on-current can never be overestimated by the drift diffusion simulation. Furthermore the drift diffusion simulations are significantly faster than quantum ballistic simulations and also fairly well fitted to experimental results. To account for hot carrier transport due to large electric fields, the energy balance equation is solved to yield accurate device simulations results.

Chapter 9
Conclusion and Scope for Future Work

9.1. Conclusion:

The performance of different FinFET devices structures to meet the scaling trend of nanoscale device structures has been evaluated. To begin with, various multi-gate MOSFET device structures have been discussed in the first chapter. These devices are non-planar structures which have the capability to replace planar MOSFET devices due to their scaling potential and very good characteristics in the nanometer regime. Multigate MOSFETs are the best promising device structures that outperform the conventional single gate transistors by providing near ideal sub-threshold slope, higher transconductance and minimized short-channel effects (SCE's). FinFET, which is considered as the most viable implementation of the multigate or MuGFET device structure for continuing the scaling trend of MOS transistors, has evolved from the DELTA, a fully DEpleted Lean-channel TrAnsistor introduced by Hisamoto et al. in 1989 and is widely open for research and development in order to follow the Moore's law and the projections of ITRS roadmap for the future generations. Several variants of FinFET that have been introduced in the beginning include double gate, triple gate and surrounded gate device structures etc. A very brief discussion of FinFET technology has been presented. It has been demonstrated that the quasi planar nature of the novel folded channel transistor, introduced by Hisamoto et al. has simplified fabrication process for double gate transistor. Different technologies of fabricating FinFET devices have been overviewed. Furthermore, departure from long channel to short channel behavior of transistor characteristics due to short channel effects has been introduced in the introductory chapter.

A systematic review of related literature based on the study of FinFET structures as carried out by various authors has been presented. This provides background knowledge and step wise progress of research work that has been already done by researchers in the field and acquaints with lot of new ideas that may be elaborated to carry out future studies in the field.

Physical modelling approaches based on analytical solutions to various device equations that govern the behaviour of multi-gate device structure have been

overviewed. Due to their higher scaling potential, researchers are continuously working to accurately propose physical modeling approaches of such novel device structures.

The dissertation has been mainly concerned with evaluation of the scaling potential of FinFETs based on its characteristics and to assess the short channel effects that impinge the device characteristics. Keeping this in consideration, the various characteristics have been simulated using the drift-diffusion model based simulator, MuGFET, because of the fact that subthreshold characteristics of device are diffusion dominated and reflect device characteristics in the subthreshold region in consistent with the experimentally observed characteristics of the device.. The drift-diffusion simulator is way faster than the quantum transport simulator that provides physical insight of the device. Also the quantum mechanical effects become negligible while simulating the transistor structures with lateral dimensions greater than 10nm. To evaluate the performance of simulator, several FinFET structures for which the device parameters have been taken from the experimentally fabricated structures from various authors, have been simulated. There has been a very good agreement between the simulated data and that of experimental data available in the literature. In order to carry out device simulations of FinFET, the various parameters of FinFET have been undertaken as per the projections of International Technology Roadmap for semiconductors (ITRS), while only few of the parameters are user defined.

The effect of various scaling and process parameters on the device I-V characteristics of FinFET has been studied. From the simulation study of I_d-V_d characteristics, it has been found that drain current increases with the decrease in gate length, L_g of the device due to the reduction in channel resistance of the device. The subthreshold behavior of FinFET has been observed to improve as the fin width decreases due to increase in multiple gate control of the device. Higher doping concentration of fin body have been found to reduce the device on- current due to reduced channel mobility of device while at the same time has resulted in improvement of subthreshold behavior. The effect of gate length and fin thickness on transconductance characteristics have been simulated and presented. It has been observed that transconductance degrades with an increase in gate length due to reduced carrier mobility in long channel devices. An improvement in transconductance characteristics has been observed for wider fin devices due to reduced parasitic source /drain resistance of device.

Effect of fin size and cross sectional shape on output conductance and transconductance of FinFET as carried out by various authors have been presented. From

this study, it has been observed that output conductance, g_d , values are lower in long channel devices due to lower drain influence on the total channel length. Furthermore, the study of transconductance, g_m, with respect to various fin sizes and shapes reveals that for a trapezoidal fin structure, as the top fin width is increased, the channel charges become well coupled to the gate and less coupled to the substrate, and so the current will be better controlled by the gate (higher transconductance). As the top fin width of trapezoidal fin of a FinFET is decreased, the channel is more exposed to the substrate potential rather than being controlled by gate bias, and so the transconductance of the device is degraded. Coupling effects in FinFETs, as studied by various authors has been presented. From this study, it has been observed that it is difficult to de-correlate the front and lateral conduction because they both coexist. There is a clear influence of the back gate: lateral shift of the characteristics and hump on transconductance (g_m) due to the gradual activation of the back channel.

In order to assess the scaling potential of the FinFET device, a detailed and systematic study based on the theoretical discussion and the simulation results obtained for various FinFET structures has been presented. The parameters of SCE's that have been discussed and simulated are: Drain Induced Barrier Lowering (DIBL), Subthreshold Slope (SS), roll-off characteristics of Threshold Voltage (V_t). These SCE parameters have been evaluated with respect to various physical scaling and process parameters of the devices. To maintain a proper threshold voltage in ultrathin devices like FinFET is a challenging task due to various limitations imposed on the device characteristics. Adjustment of threshold voltage with proper channel doping and gate work-function of FinFETs has been presented through theoretical discussion followed by various simulation results. It is observed that gate work-function engineering should be preferred compared to adjustment through fin body doping as the later has the limitation that it reduces the carrier mobility and presents bandgap narrowing effect in extremely scaled devices. Threshold voltage roll-off with scaling parameters viz., gate length, fin thickness and fin height has been presented through simulations of various structures.

A very critical aspect, threshold voltage roll-off in scaled ultrathin devices has been presented. For this the roll-off characteristics of threshold voltage with channel length, fin thickness and fin height have been presented. It has been shown that threshold voltage rolls-off with gate length scaling due to increased drain influence which reduces the barrier of conduction from source to drain. Roll-off characteristics of threshold voltage versus fin thickness has shown that reducing fin thickness can increase the gate

control of device towards channel electrostatics and maintains threshold voltage at higher level. Further it has been presented that threshold voltage rolls-off with increasing fin height of device due to the fact that the top gate loses control over the entire channel region and the two vertical side gates mainly govern current conduction.

Two major short channel effects viz., DIBL and SS have been theoretically discussed, following which a simulation study of these SCE's with respect to physical scaling parameters of device has been presented. Simulation results have shown that both DIBL and SS increase sharply with the decrease in gate length which is because the drain electric field encroachment on channel region increases for shorter gate-length devices. Variation of DIBL and SS with respect to fin thickness has shown that both DIBL and SS increase with increasing fin-thickness. It is because with increasing the fin thickness the vertical self aligned gates weekly control entire channel region of device and drain electric field penetration becomes more effective to control the device conduction. Also it has been demonstrated that in order to achieve acceptable SS behaviour, fin thickness of device should be such that $T_{fin} < \frac{2}{3} L_g$. Study of DIBL and SS with respect fin height has shown that both DIBL and SS increase with increasing fin height. It is because the top gate loses control over the channel with increase in fin height, while as the two lateral gates become the dominant to control the device channel conduction. Not only DIBL and SS degradation occurs but the threshold voltage also degrades with increasing fin height. It is degradation in SCE's in general. Furthermore it has been recommended that triple gate devices should be designed with lower aspect ratios ($AR=H_{fin}/T_{fin}$) in order to reduce SCE's.

Parasitic channel conductions are a challenging aspect in triple gate FinFETs which causes the device to conduct at subthreshold voltages and affects their performance in case of LSTP logic technology requirements. These parasitic corner effects in FinFETs as studied by various authors have been presented and discussed. From these studies it has been found that the corner effects deteriorate the subthreshold behaviour of triple gate FinFET devices due to parasitic channel conduction of these devices. The various corner effects on the characteristics of FinFET as observed by various authors are: kink effect in the transfer characteristics; multiple threshold voltages of device; hump in the transconductance characteristics. Higher fin body dopings have been reported to show more kink effects compared to lower body dopings. Furthermore it has been discussed that various techniques such as utilizing undoped fin body devices, corner rounding of

fins and corner implantation as proposed by various authors can eliminate the corner effects in FinFET devices. While utilising both rounded corners and corner implantation, the kink effect in the characteristics of FinFET is strongly eliminated.

A very unique comparative simulation study of short channel effect performance of Si, GaAs, GaSb and GaN channel FinFET structures has been presented. These SCE's have been studied with respect to scaling parameters viz., gate length, L_g and channel width, W_{ch}. The results obtained show that both GaAs and GaN channel devices show better DIBL characteristics with respect to L_g, however for L_g< 46nm, GaN FinFET offers better DIBL characteristics with respect to L_g. The DIBL characteristics with respect to W_{ch} show that GaN is better choice, however for W_{ch}< 25nm, the DIBL characteristics are almost same for Si, GaAs and GaN FinFET.

On studying the effect of gate length, L_g, and channel width, W_{ch}, on subthreshold slope (SS) characteristics, it has been found that Si and GaAs FinFET have almost identical SS characteristics with respect to L_g while as GaN FinFET device offers better SS characteristics compared with other three channel materials studied. At a channel width of 18nm, FinFET devices based on Si, GaAs and GaSb exhibit same value of SS, however, for L_g >18nm, SS behaviour Si and GaAs FinFET is almost same throughout the range of simulation study. Furthermore GaN FinFET has shown better SS characteristics with respect to W_{ch}.

Study of threshold voltage roll-off characteristics with respect to L_g and W_{ch} has shown that Si channel FinFET has better V_t roll-off characteristics. It is worth noting that GaSb FinFET has shown the worst case for all plots, however for W_{ch}< 18nm, GaSb has shown good SS characteristics.

Threshold voltage being an important parameter of ultrathin devices like FinFET has been studied with respect to gate work-function engineering. Metal gate technology with adjustable work-function has been proposed to be utilised for FinFET devices due to their capability to withstand high-k gate materials that are very much essential for the continuous downscaling of device structures. The efficiency of these metal gates in FinFET devices has been evaluated by studying the variation of threshold voltage in FinFETs with respect to metal gate work-function. Evaluation of corresponding SCE's and device performance has been presented that supports utilization of metal gate work-function adjustment for threshold voltage in FinFETS. It has been found that to meet the requirements of higher threshold voltage (low off-current) for LSTP logic technology, metal gates with adjustable work-function is a very good solution.

9.2. Scope for Future Work:

Based on the work carried in this dissertation, several important studies have been identified that may be continued for future research work in the field. It has been found that in order to continue the scaling potential of FinFET devices to follow the projections of ITRS and Moore's law, the modern VLSI devices should be fabricated by utilizing new channel materials. A comparative study of short channel effects for different III-V channel material FinFETs and Si FinFET has shown that there is a great scope of study in the field. As the different logic technologies determine the requirements of MOS devices to be used in digital IC's, FinFET devices should be fabricated based on different channel materials to meet the particular requirement of logic technology. High-performance (HP) logic refers to chips of high complexity, high speed, and relatively high power dissipation, such as microprocessor unit (MPU) chips for desktop PCs, servers, etc. Low Operating Power (LOP) chips are typically for relatively high-performance mobile applications, such as laptop computers, where the battery is likely to be of high capacity and the focus is on reduced operating power dissipation. Low Standby Power (LSTP) chips are typically for lower-performance, lower-cost consumer type applications, such as consumer cellular telephones, with lower battery capacity and an emphasis on the lowest possible static power dissipation, i.e., the lowest possible leakage or off-current. The HP logic requirement of increase in drive currents for faster switching speeds at lower supply voltages can be achieved largely at the expense of an exponentially growing leakage current, which leads to a large standby power dissipation. There is an important need to explore novel channel materials and device structures that would be much efficient to reduce the leakages associated with HP logic device design. Due to their significant transport properties, high mobility materials are very attractive for being researched as channel materials for future highly scaled CMOS and for ultrathin devices like FinFET. The significantly lower bandgap of high mobility materials should be resolved through advanced technologies in order to make them fully efficient for being utilised in HP logic devices.

The threshold voltage roll-off in highly scaled devices presents a very challenging task that has been studied in the dissertation to some extent. Various techniques of adjusting threshold voltage of FinFET devices have been presented and compared. It has been found that controlling threshold voltage through proper doping concentration faces serious challenges in ultrathin devices like FinFETs. In our study, sensitivity of

threshold voltage to metal gate work-function has been studied to meet the requirements of low leakage current (off-current) for LSTP logic design. Metal gate work-function based threshold voltage adjustment has been proposed as an efficient technique that reduces the device SCE's considerably. Metal gate materials should be researched to meet the higher gate work-function and hence the higher threshold voltage of ultrathin FinFET devices. The work has a very good scope for future study.

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List of Publications

1. M. Mustafa, Tawseef A. Bhat, M. Rafiq Beigh, "Study of Threshold Voltage Dependence on Doping Concentration and Physical Scaling in FinFET Structures", *Proceedings of 7th Jk Science Congress, University of Jammu, Jammu*, 13-15 Oct., 2011.
2. M. Mustafa, M. Rafiq Beigh, Tawseef A. Bhat, "Implementation and Verification of Majority Logic Reduction Techniques for Quantum Cellular Automata", *Proceedings of 7th Jk Science Congress, University of Jammu, Jammu*, 13-15 Oct., 2011.
3. M. Mustafa, Tawseef A. Bhat, "A Comparative Simulation Study of Short Channel Effects in n-FinFET Structure for Si, GaAs, GaSb and GaN Channel Materials", *Communicated for Publication*
4. M. Mustafa, Tawseef A. Bhat, "Performance Evaluation and Threshold Voltage Sensitivity to Metal Gate Work-Function in Double-Gate n-FinFET Structures For LSTP", *Communicated for Publication*