SOME APPLICATIONS OF SWITCHED CURRENT CIRCUITS

By

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CERTIFICATE

This is to certify that **Mr. FAISAL BASHIR** has worked under my supervision for the dissertation entitled, "***SOME APPLICATIONS OF SWITCHED CURRENT CIRCUITS***" and the work is truly worthy of consideration for the award of the degree of Master of Philosophy in Electronics.

It is further certified that

(i). The dissertation embodies the work of the candidate.

(ii). The candidate worked under my supervision for the period required under statues.

(iii). The candidate has put in the required attendance in the department.

(iv). The conduct of the candidate remained very good during the period of the research.

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ABSTRACT

Some Application of Switched Current Circuits

A complete digital signal processing system requires analog circuits acting as an interface between the digital system and the outside analog world. Various techniques have been proposed to implement these circuits, but the one compatible with digital technology is switched capacitor (SC) technique. However, there are still some problems with SC circuits which are as follows: (i) The process technology used for these circuits is not compatible with the standard digital process technology due to extra poly-silicon layer, (ii) the performance of these circuits worsens for low voltage operations, because lower supply voltage will tend to increase power consumption for the same dynamic range, and in order to maintain the same dynamic range on a low supply voltage requires a quadratic increase in sampling capacitance to reduce thermal noise. The required increase in bias current to maintain circuit bandwidth results in a net increase in the overall power consumption. To overcome these problems, a new technique called the switched current (SI) technique has been proposed. The technique utilizes the ability of an MOS transistor to maintain its drain current, when its gate is open circuited, through the charge stored on its gate oxide capacitance. In this technique signals are represented by currents instead of voltages and, therefore, the signal

swing is only indirectly limited by a reduction of the available voltage range. In a traditional voltage mode circuit, the supply voltage imposes a direct limitation on signal swing. Switched current circuits could therefore be a better for low voltage operation.

The application of switched current systems is much same as for switched capacitor systems viz. filters, A/D and D/A converters, general signal processing etc. but the prime aim is that switched current circuits should be implemented using a standard VLSI.

In this work, the SI technique has been studied and several reported SI circuits have been simulated for their performance. Specifically, the work was aimed at the study of developing SI technique for the design of high performance circuits such as Integrators, Differentiators, Programmable filters, A/D and D/A converters, Sigma Delta Modulators, Multipliers, Delays etc.

All the investigations are based on the PSPICE simulations using model parameters of the BISIM335 MOS transistors. The investigations match the theoretical interpretations and predictions. The entire gamut of this dissertation has been to study the already reported SI circuits and to investigate them for improved accuracy, dynamic range, bandwidth, linearity and low voltage operation.

Dedication

To my Parents and Guide

CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation "**Some Application of Switched Current Circuits**" in partial fulfillment of the requirements for the degree of **Master of Philosophy** and submitted in the Department of Electronics and Instrumentation Technology, Faculty of Applied Sciences and Technology, University of Kashmir, Srinagar, has entirely been done by me under the supervision of **Prof. N. A. Shah**.

I, further, declare that the work contained in the dissertation is the original research work conducted by me and has not been submitted in part or full, to any other university or Institute for the award of any degree.

(FAISAL BASHIR)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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NOMENCLATURE

SI	Switched Current
SC	Switched Capacitor
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
OTA	Operational Trans-conductance Amplifier
VLSI	Very Large Scale Integration
FIR	Finite Impulse Response
IIR	Infinite Impulse Response
DSP	Digital Signal Processing
A/D	Analog to Digital
D/A	Digital to Analog
S/H	Sample and hold
IT	Information Technology
IC	Integrated Chip
FE	Forward Euler
BE	Backward Euler
LDI	Lossless Discrete Integrator
BD	Backward Difference
W/L	Width to Length ratio
biquad	Bi-quadratic
∑ΔM	Sigma Delta Modulator

CT	Continuous Time
DT	Discrete Time
Q	Quality Factor
LP	Low-pass
BP	Band-pass
HP	High-pass
AP	All-pass
BR	Band-rejected
LSB	Least Significant Bit
MSB	Most Significant Bit
CFT	Clock Feed-through
β	Current gain
λ	Channel Length Modulation
g	Trans-conductance
g_o	Drain conductance
c_{gs}	gate-source capacitance
c_{dg}	drain-gate overlap capacitance
g_{mQ}	small-signal trans-conductance
g_{oQ}	equivalent output conductance
i_{ds}	drain-source current
v_{ds}	drain-source voltage
v_{gs}	gate-source voltage
V_T	Threshold voltage

M	Memory Transistor
$\Delta \mathbf{V_t}$	error voltage

PUBLICATIONS/PROCEEDINGS

1. *N. A. Shah, F.A. Khanday and F. Bashir,* "Some Application of switched current circuits" *6th–JK Science Congress, 2-4 December 2010, University of Kashmir*.
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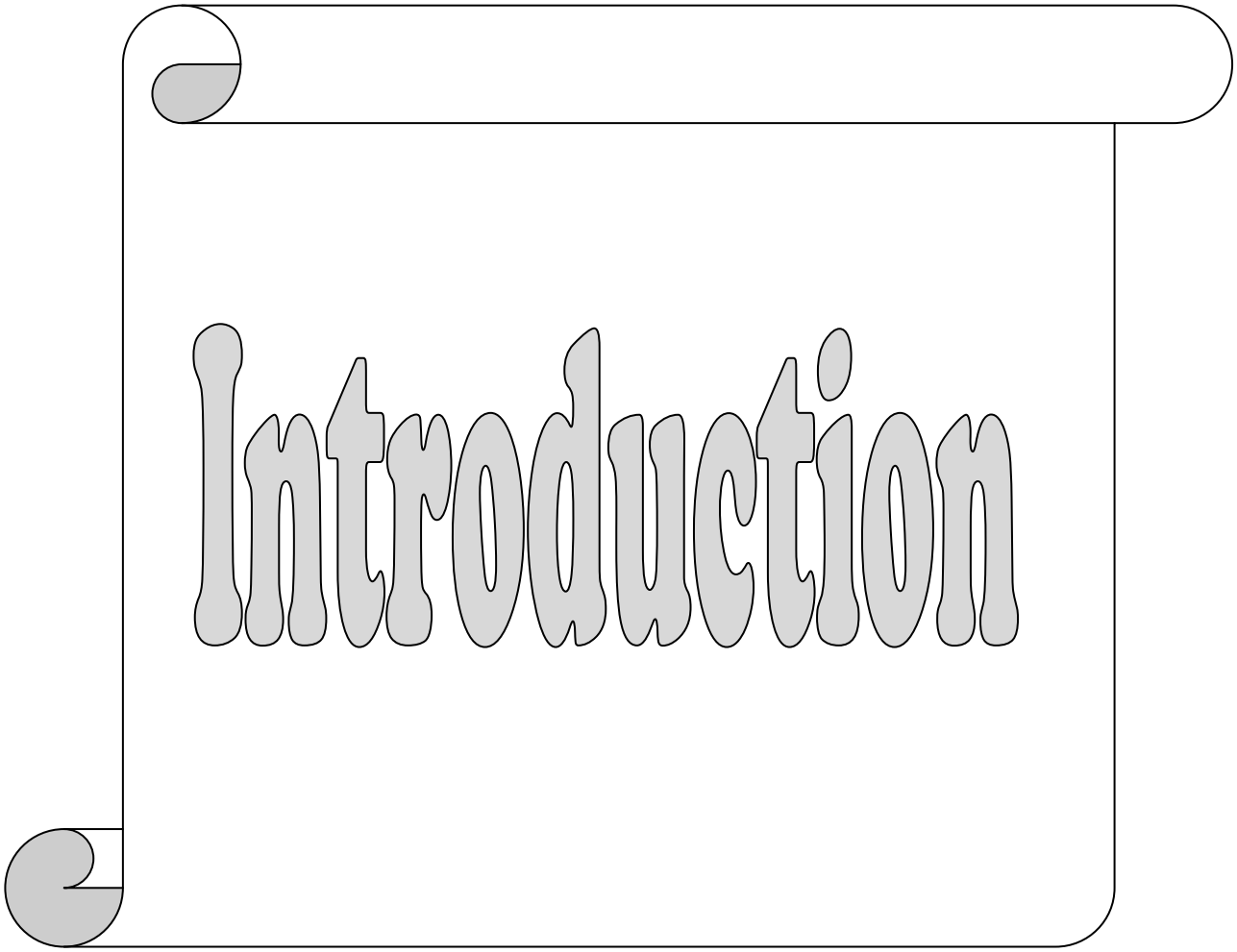

Introduction

1.1. General

The switched-current technique (SI) was introduced in the late 1980s at a time when switched capacitors (SC) could not be easily implemented with the digital CMOS IC processes available at that time. This came about for two main reasons. First, SC operated by charge transfer and this could only be performed efficiently with the linear floating capacitors that came with special process options (e.g. double poly silicon layers). SI, on the other hand, uses charge storage and this requires only grounded, nonlinear capacitances of the sort that occur naturally at the gate of any MOS transistor. Second, SI uses current rather than voltage to represent its signals [1, 2]. This makes it much better placed to contend with the diminishing power supply voltages needed for emerging digital circuits. The basic current memory requires only a pair of complementary MOS transistors, one as the storage device and the other to provide its bias current, and a few MOS switches to affect sampling. The cell merges the properties of storage and buffering into the same physical device (the memory transistor), whereas SC required separate storage (usually linear floating capacitors) and buffering (closed-loop OTAs). So, as well as the economies resulting from the use of the most basic process, further cost savings could be expected through reduction of chip area. The simplicity of the circuits also suggests that SI could be capable of higher sampling frequencies than SC, which may be limited by compensation and slewing in its closed-loop OTAs. The SI technique thus promises a good future for video and higher frequency applications [3, 4].

During the 1980s and the 1990s there was trend towards replacing analog-based solutions by digital-based ones. Year by year the border between the analog and the digital has shifted to become closer and closer to the very analog signal interfaces. This trend has been parallel to the exponential increase of the capabilities of digital VLSI

circuits, fueled by the evolution of microelectronic technologies towards deep submicron. Particularly in the area of telecommunications, electronic systems are mostly digital, basically only the analog circuits strictly needed to interface the front- and back-end analog signals. Many electronic communication systems are realized by connecting different chips on a PCB (printed circuit board). For the analog interface circuitry designers basically rely on what is available in the different semiconductor catalogues. However, the trend is towards integrating the analog circuitry on the same silicon substrate in which the digital core circuitry is realized. Thus, new generations of on-chip mixed mode signal communication systems are coming into the picture. Together with reduced price, size and power consumption, these systems feature greater functionality through the closer interaction between the analog and the digital. For instance, the digital implementation of some functions such as channel selection and the demodulation of the signals coming from the antenna in a wireless transceiver facilitate the programmability of these functions, thus allowing their adaptability to a great number of communication systems. Basic tasks realized at the interfaces of mixed-signal chips include data conversion, signal conditioning, amplification, driving, etc. SI circuits employ the MOS transistor as the basic primitive for the operations of delay and signal scaling. Because of the capacitive nature of the MOS gate, it is possible to store a voltage in it during a sampling phase, and to take the associated current during later hold phase. In addition, it is easy to transmit and to scale these retained currents using only MOS transistors, which guarantees a total compatibility with CMOS technologies.

Recent advances in integrated circuit technologies have meant that state-of-the-art analog IC design is now able to explore the potential of current-mode analog signal processing, providing attractive and elegant solutions for many circuit and system problems. A current-mode circuit may be taken to mean any circuit in which current is used as the active variable in preference to voltage, either throughout the whole circuit or only in certain critical areas [7][8]. The SI technique is a current mode technique and thus offers other advantages such as:

1. **Higher bandwidth capability:** bipolar junction transistors and field effect transistors are both current output devices. A key performance feature of the current-mode processing is inherent wide bandwidth and a current amplifier the transistor is useful almost up to its bandwidth f_T. The stray capacitances can be usefully employed as gain element at higher frequencies [12], whereas they limit the bandwidth in voltage-mode circuits.
2. **Higher operating speed:** the shrinking dimensions of integrated circuit techniques lead to circuits whose parasitics are predominately capacitive. Current-mode circuit can achieve high speed signaling at low impedance internal nodes and low voltage swing due to minimal capacitive charging and discharging.
3. **Low circuit complexity for analog arithmetic computations:** in the current domain, computations like addition and subtraction can be performed directly by joining the terminals at a single point. With the current mirror structure, the basic functions of inversion, scaling and summation can be implemented conveniently. In contrast to the voltage-mode counterpart, this needs an operational amplifier for realizing the same functions. It is clear that current-mode realization possesses low circuit complexity and the possibility of low power consumption.
4. **Greater operating dynamic range:** as the shrinking device feature size of integrated technology, the supply voltage has to be reduced in order to ensure device reliability. The reduced voltage supply levels result in reduced dynamic range. An attempt to overcome this problem is simply to change the signal representation from a voltage to current. In this way the signal range is no longer directly restricted by the supply voltage but dependent on the impedance level chosen by the designer [5].

This fact makes the SI technique especially appropriate for low supply voltages. As the operational amplifiers are not required for its implementation (as in the case of SC), high speeds can be achieved with a low power consumption.

Current memories are the most fundamental of all switched-current cells. They are used in feedback pairs to make the integrators for leapfrog or state-variable filters or in the modulators of sigma-delta data converters. They are also used in pairs as the unit-

delay cells of FIR filters and in cascades for pipeline data converters [6]. So, the current memory has been the natural choice for circuit development over the past decade.

In the past two decades, the field of digital signal processing (DSP) has experienced a very rapid growth and recognition in many areas of science and engineering such as telecommunication, robotics, geophysics, medicine etc. The upsurge in DSP related activities can be attributed mainly due to the recent development in the very large scale integration (VLSI) technology that has allowed the integration ever powerful DSP system into in an expensive chip. The increasing performance and reduced cost of integrated circuits DSP have brought universal acceptance of the usefulness of the area of DSP. A single chip DSP system is a mixed analog and digital integrated circuit that requires analog circuit, such digital to Analog (D/A) and analog to digital (A/D) converters, sample and hold (S/H) circuits, pre-filters, post –filters etc acting as a interface between the digital systems and the outside analog world [9][10]**.** Figure 1.1 shows the Block diagram of complete DSP system

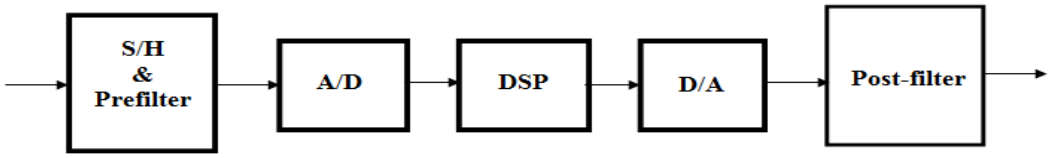


Fig. 1.1: A complete signal processing system

1.2. Need and Importance Switched Current Technique:

To overcome the limitations of the SC circuits mentioned above, researchers have proposed many new techniques that are mostly current mode circuits for analog signal processing [7, 11, 12]. Specifically, the Switched current (SI) technique proposed by J.B. Hughes, N.C. Bird and L.C. Macbeth in 1989 [13] and similar technique called current copier technique, proposed by S. J. Daubert, D.Vallancourt and Y. P. Tsividis in 1988[11] are analog sampled data circuits, in which signals are represented by currents

rather than voltages. The SI technique relies on the ability of MOS transistors to maintain its drain current with its gate opened by the charge stored on its gate capacitor. This means that the SI circuits do not require linear floating capacitors and the double poly process technology. This makes the SI circuits fully compatible with the standard digital VLSI process technology. Further, since SI circuits work in the current domain, the power supply voltage can be reduced.

The SI circuits are still less attractive than the SC circuits due to problems of low accuracy, nonlinearity etc. Since the SI technique is a new technique, there are still many application problems not yet resolved. Furthermore, in the area of VLSI design, the design automation is an important evaluation parameter of any new design technique. if its automation level is low, it will be less attractive to designers. A wide range of application of SI circuits in VLSI will, to greater extend depend on the automation level of the design technique used.

Information technology (IT) has demonstrated a tremendous growth in the market value as well in technical performance. The technical catalyst in the IT explosion is the constantly improved digital VLSI technology, where packing density, low power, low cost are the key issues. As a result of this development, it has become possible to integrate extremely complex digital systems on a single chip. The next goal is to enable one chip system solutions by successfully integrating interfacing circuits such as A/D and D/A converters on the same chip. Here a new method used for this purpose is mixed mode integration, but there exist some technical challenges for mixed mode integration. When manufacturing technology is optimized digital VLSI, the result is that analog circuit designs become even more difficult. Analog interfacing circuits that are to be integrated with the state of art digital circuits should therefore preferably not require anything but MOS transistors and their dynamic range should not be limited by the supply voltage. The current mode approach and the switched current technique were proposed in order to meet these demands.

1.3. History and State of Art of Switched Current Circuit:

The SI technique is a current mode signal processing technique which utilize the ability of an MOS transistor to maintain its drain current, when its gate is open circuited, though the charge stored on its gate oxide capacitance. Although early attempts to exploit this property were made as early as 1972 [12, 13, 14], it was not until the late 1980s that it was revived independently by a number of researchers [15, 16, 17, 18]. During the time when switched capacitors (SC) could not be easily implemented with the available digital CMOS IC processes, the SI technique has attracted considerable attention [1, 5].

Initially, Switched current was described in terms of so-called 'first generation' circuit module [19]. This module was based on a memory cell developed from the simple current mirror but suffered from inevitable errors resulting from transistor mismatch. Due to these errors new configuration were presented in order to have accuracy, linearity, bandwidth etc. In order obtain necessary results the Second generation SI memory cell was presented by J. B. Hughes and *et al* [20, 21] which overcomes few problems associated with first generation memory cell. But there remain problems associated with Second generation SI memory cell. Some of the problems are: charge injection error, Clock feed-through, Conductance Ratio Error, Steering Switch-On Resistance etc. In year 1992 U. Gatti and F. Maloberti presented "Fully Differential Switched Current Building Blocks" [22]. The circuit not only reduces the effect of clock feed-through but also improves linearity. But the problem associated with the Fully Differential block is that it increases the circuit complexity. Therefore to increase the performance of the SI memory cell, it is important to reduce circuit complexity as well as errors, this can be achieved by reducing the error in second generation SI memory cell, because second generation SI memory cell has least complexity. The main problem in switched-current applications is clock feedthrough (CFT), which occurs when a switch transistor is connected to a holding capacitor. CFT is caused by carriers released from the channel and from coupling of the clock through the gate diffusion-overlap capacitances of the switch. Due to the square-law characteristic of the memory MOS transistor, every signal-dependent error voltage on the gate produces both a signal-dependent offset and

harmonic distortion of the output current. Besides the well-known dummy switch compensation or the addition of extra gate–source capacitances (physical enlargement or Miller-type techniques [23]), a number of suggestions have been presented to solve the CFT problem. In general, they propose: the cancellation of only the signal dependent part of the CFT [24, 25], both parts [26], or a reduction to some extent, by using, e.g., algorithmic [27], two-step [28], or differential structures [29]. Thus, they basically rely on transistor mismatch, on a repeated sampling of the input current and/or the CFT error itself, or on differential techniques. Recently a new clock-feedthrough compensation scheme for switched current circuits is proposed by Markus Helfenstein and George S. Moschytz "Improved Two-Step Clock-Feedthrough Compensation Technique for Switched-Current Circuits" [30]. The scheme is especially suited for the design of delay lines for high-frequency operation. The circuit operates by using an improved two-step technique, in which the input is sampled in a parallel combination of a coarse and a fine memory transistor. Since both transistors are of the same type, large switching transients compared to the conventional SI scheme can be avoided.

The use of SI technique in designing the integrators, differentiators, delays, multiplier etc, which are important for designing the higher order filters. Due to problems associated with the first generation SI memory cell its use becomes restricted. The use of second generation SI cell gains interest in designing basic building blocks. To increase the frequency response and the frequency warping effect in basic integrator Shen-luan Liu *et al* put forward "A Switched Current Modified Bilinear Integrator" [31]. A bilinear integrator (BI) and a lossless discrete integrator (LDI) are well known in digital and sampled data design. However, the inherent frequency warping effects of these two integrators limit the circuit performance in high frequency filter application [32]. The main idea of this new integrator is to combine bilinear and lossless discrete integrator (LID) transformation to achieve combined transformation. The integrators are used to design high order biquads and filter. In the same way differentiator also play their role in designing discrete time filters. There exists several methods for designing IRR and FIR filters some methods are based charge coupled device (CCD), digital circuits, and

switched capacitor technique[33, 34]. But Shen-luan Liu *et al* presented a new design "Switched Current differentiator based IRR and FIR filters" [35]. The realization of these circuits requires differentiatiors, current mirrors and analogue switches. Due to enormous potential advantages Mariusz Jankowski, Zygmunt Ciota, Andrzej Napieralski presents "CMOS Realization of Switched Current Discrete-Time Filter" [36]. Its main features are ability to operate at high frequencies and at a low power supply, simplicity of implementing various mathematical operations as summation, inversion, and multiplication. Additional practical advantage of switched current circuits is the structure composed of only NMOS and PMOS transistors, which enable implementation in standard digital CMOS technologies, so popular nowadays. Owing to these features the SI signal processing method is used in discrete-time analog signal processing, like neural networks, A/D and D/A conversion. Furthermore Mourad Fakhfakha and Mourad Loulou, put forward "A novel design of a fully programmable switched current filter" [88] the characteristics of the filter are fully programmable by simply varying the values of out-of-chip DC current sources. The programmable switched current filter mainly consists of SI delay cells and SI multipliers.

Filtering is a major application of SI circuits. In addition to their intrinsic advantages, the use of SI circuits is easier than that of SC circuits for programmable filter design (Toumazou *et al*. 1993) [89]. Programming the coefficient values in a SI filter allows programming the filter characteristics. In the literature some approaches are proposed. For instance, Omair and Wang (1999) [90] and Wang and Ahmed (1995) [91], presents programmable filters using MOS transistors. The goal was realized by using a transistor array. This array uses three different sizes of transistors that present the ones, tens and hundreds of decimal places. By programming the connection of the coefficient transistor array, one can obtain the required coefficient value. Neji *et al* (2003) [92] and Neji, Fakhfakh *et al* (2003) [93]. By changing the aspect ratio one can adjust (band pass) filter characteristics by varying the sampling frequency, since the central frequency and bandwidth are linearly dependent on the clock signal frequency. Dlugosz (2006) [94] used current mirrors to perform the coefficient multiplication operation for designing

finite impulse response (FIR) SI circuits. Consequently, the proposed filters cannot be programmable or flexible enough. Besides, the proposed solution needs the design of complicated clocks and additional blocks to perform both positive and negative multiplications, since a class A cell is used. Farag *et al* (2000) [95]; Farag *et al* (1999)[96]; Goncalves *et al* (1996) [97]; and Goncalves, *et al*(1995) [98] proposed designs for programmable SI filters.

As multipliers also play their important role in filtering, it is also the basic element in filter designing. There is a variety of existing current domain multiplier principles, such as the trans-linear multiplier [36], current domain multiplier based on a Gilbert cell [37], pulse modulation multiplier [38], multiplication based on A/D (Analog to Digital converter) or D/A(Digital to Analog converter) conversion [39], and quarter square multiplier [40], [41]. But D. M. W. Leenaerts *et al* [99] presents a switched-current multiplier, designed for 3.3 V supply voltage, performing 0.625 M multiplications per second with a maximum nonlinearity of 0.94%. The main advantage of this multiplier is that consists of only one current squarer and two SI memory cells. It is based on a slightly altered version of the "quarter square" principle. In this way, the problem of matching of two current squarer's is circumvented.

Now days, analog circuits must operate with supply voltages below 1 V because battery operated personal and mobile equipment is increasing rapidly. High-frequency operation and high-quality analog signal processing are still needed even with lower supply voltages. Reducing the supply voltage while maintaining high speed and precision is a major challenge for analog circuits. Signal voltage instead of signal current has usually been processed in analog circuits [42]. The lower the supply voltage, the smaller the dynamic range becomes. This makes signal voltage processing difficult. As a result, the use of current mode and switched-current circuits has been studied intensively [43]. These circuits process a signal current which is applied to a low impedance node and produce only a small voltage swing at each node. This enables circuits to operate at low voltages, high frequency and/or high speed [42].

1.4. Objectives of the Study:

The work focused on the following areas of Switched current circuits:

1. Survey and Collection of relevant printed/online material in various national, international journals/Magazines/Books etc.
2. The reported SI-circuits were thoroughly investigated in respect of various performance features (Bandwidth, Dynamic Range, Sensitivity, Frequency of Operation, Non-idealities, Number of Components, Power Dissipation, Electronic Tunability, Magnitude, Phase, Transient and Time Responses, DC Instability, cost etc.
3. The various building blocks needed to implement the SI-circuits were thoroughly investigated.
4. The already reported SI building blocks and circuits were simulated and verified for their theoretical predications.
5. The possible changes to already reported SI-circuit realizations that may improve their performance and enable more accurate measurements were also studied.
6. Finally, the work was concluded with a study of some possible areas of future work.

1.5. Dissertation Outline:

This dissertation will describe the synthesis of Switched current Circuits.

Chapter 2 presents the design of Switched current circuits. The First and Second generation SI memory cell have been discussed, but due to lack of accuracy in first generation memory cell, second generation memory cell is used to implement the important blocks, which are required for the design of higher order circuits. The chapter concludes with discussion of Switched Current design techniques.

Chapter 3 discusses the effects of transistor non-idealities on Switched Current Circuits. The Chapter draws the light on the basic error in MOS switch and the effects of MOS transistor errors which degraded the performance of Switched Current memory cell.

The chapter concludes with the discussion of the effects of Clock Feed-through effect on Switched current circuits.

Chapter 4 includes conclusions of the dissertation and scope for future work.

Switched Current Circuit Design

2.1. Introduction

An SI system may be thought of as a system using analog sampled data circuits in which signals are represented by current samples. The basic circuit element of a SI system is called the SI memory cell. It can sample and hold the current signals through the charge stored on the gate capacitor of a MOS transistor. Using this current memory cell, SI integrators, differentiator, and delay blocks. SI filter can be designed using these blocks. As with Switched Capacitor (SC), the SI technique can also be used for the design of A/D and D/A. In this Chapter, the principle of operation of a SI memory cell is discussed, followed by an introduction of integrators and differentiators. Next, SI filters using these blocks are discussed. The applications of the SI technique in A/D and D/A are also given through some examples.

Switched current (SI) technique for analog signal sampled-data system has attracted considerable attention due to adopting VLSI technique. SI memory cells have the great potential in developing analog interfacing circuits for mixed analog-to-signal integration [44]. Switched current approach is an attractive signal processing method. Among main features deciding on the method attractiveness, the ability to operate at high frequencies or with low power supply is very important. Additional advantage is the simplicity of implementing various mathematical operations, such as summation, inversion and multiplication. Moreover, the switched current circuits can be easily manufactured in standard CMOS technology. Owing to the above advantages the SI technique is commonly used in discrete-time analog signal processing, neural networks, A/D and D/A conversion [45, 46].

The switched-current (SI) circuits were chosen as an "analog counterpart" of the digital filters, with respect to their full compatibility to the digital VLSI-CMOS technologies, lower supply voltage and wide dynamic range. In addition, principle of SI-circuit signal processing is rather similar to the digital ones, therefore arises possibility to

use a "digital prototype" for the SI filter design. On the other hand, some procedures applied in SI filter design can be successfully applied in the optimized design of digital filters, especially digital biquadratic sections [47, 48].

2.2. Principle of the SI Technique:

2.2.1. First Generation Switched Current Memory Cell:

Switched-currents (SI), as the latest technique for sampled-data analogue circuits, play an important role in modern electronic system design. In comparison to SC circuits, SI has some important advantages, particularly full compatibility to the digital VLSI-CMOS technologies, lower supply voltage and wider dynamic range [49, 50]. Fig. 2.1 (a) shows the diagram of first generation memory cell. The time domain response of first generation SI memory cell is shown in Fig. 2.1 (b). Its operation can be stated as: It is a simple current mirror with a switch S separating the gates of two transistors. When the switch S is closed by using clock Φ, the circuit works in sample mode and both gate capacitors C_{g1} and C_{g2} are charged to v_{gs}, establishing the drain current $i_{d1}=J+i_{in}$. By normal current mirror action, we have $i_{d2}=Ai_{d1}$ and this results in the output current $i_o= -Ai_{in}$. Therefore, the current i_o is available simultaneously with the input sample. When S is opened, the circuit is in hold mode, a voltage close to v_{gs} is held on C_{g2} and the circuit maintains the output current i_o close to value $-Ai_{in}$.

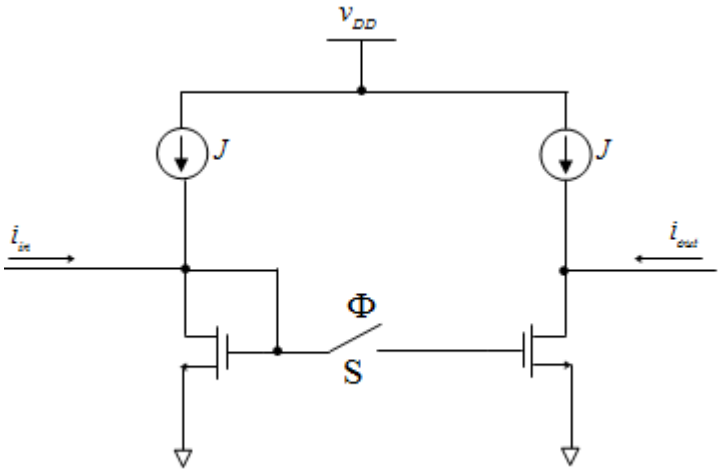


Fig. 2.1 (a): First generation SI memory cell.

2.2.2. Second Generation Switched Current Memory Cell:

The second generation SI memory cell is shown in Fig. 2.2 (a). Switches S_1–S_3 are controlled by 2-phase switching signal.

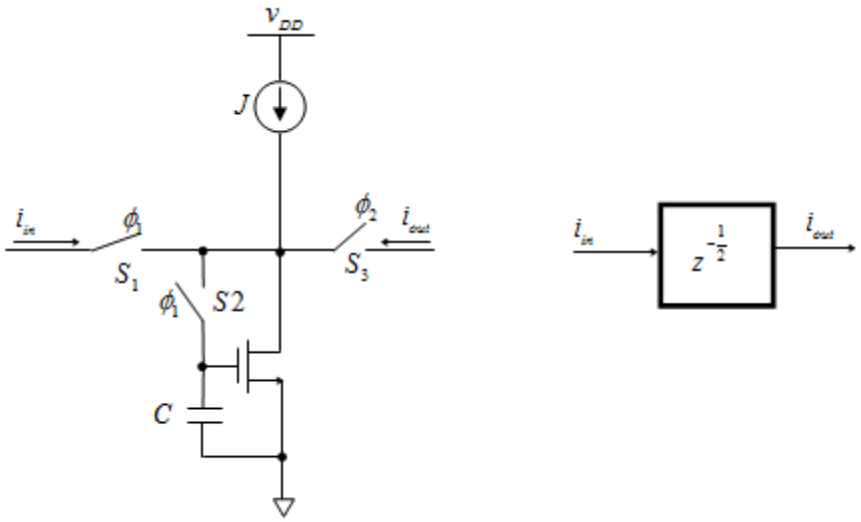


Fig. 2.2 (a): Second generation SI-cell and its equivalent.

The principle of operation is as follows: S_1 and S_2 are switched ON during phase Φ_1 circuit operates as the input of current mirror with low input resistance (input current $i_{in}(nT)$). The second phase Φ_2 is a storage (or output) phase – S_3 is closed and output current $i_{out}(nT+1/2)$ flows into load. The function is characterized by Eqs. (2.1) and (2.2) which shows half delay performed by simple memory cell.

$$i_{out}(nT+1/2) = i_{in}(nT) \tag{2.1}$$

$$H(z) = \frac{i_{out}(z)}{i_{in}(z)} = z^{-1/2} \tag{2.2}$$

The output time domain response for half delay simulated using PSPICE and model parameter of BISIM335 MOS transistor are shown in Fig. 2.2 (b)

To obtain transfer function for full delay i.e $H(z) = z^{-1}$, it is necessary to use two basic cells connected in cascade, as shown in Fig. 2.3 (a). The circuit also depicts as, how to realize multiple outputs with different transfer gain constants. The output time

domain response for full delay simulated using PSPICE and model parameter of BISIM335 MOS transistor are shown in Fig. 2.34 (b).

Output terminal i_{out1} pertains to the "pure" memory cell, created by transistors M_1 and M_2 and switches S_1 to S_5. Outputs i_{out2} and i_{out3} combine the second basic cell (transistor M_2) together with transistors M_3 and M_4 creating "conventional" current mirrors. Such arrangement allows setting the gain constant α_i, i=1,2 in the form Eq. (2.3) and Eq. (2.4), where W_k, L_k denote the channel width and length of transistor M_k, k=2,3,4. Note that ratios W/L can be normalized with respect to the channel parameters of the basic cell transistor.

$$H_2(z) = \frac{i_{out2}(z)}{i_{in}(z)} = \alpha_1 z^{-1}; \alpha_1 = \frac{w_3 / L_3}{w_2 / L_2} \tag{2.3}$$

$$H_3(z) = \frac{i_{out3}(z)}{i_{in}(z)} = \alpha_2 z^{-1}; \alpha_2 = \frac{w_4 / L_4}{w_2 / L_2} \tag{2.4}$$

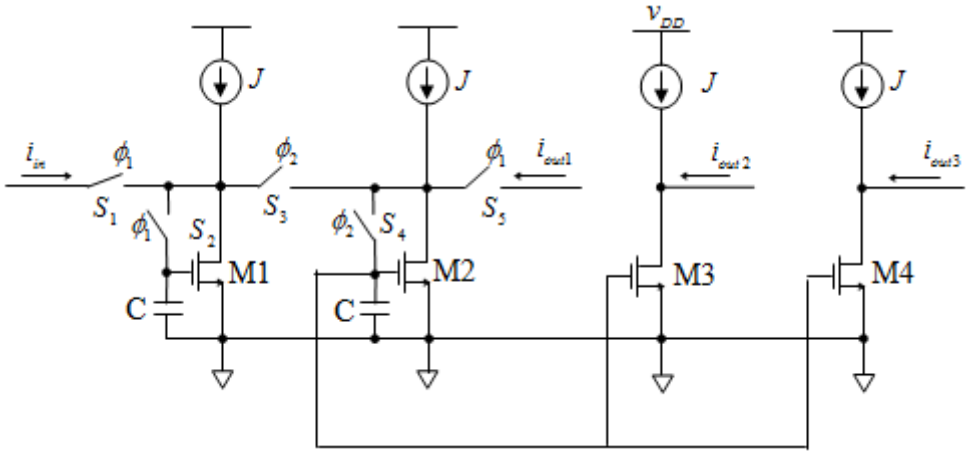


Fig. 2.3 (a): Multiple output SI memory cell (Full Delay)

2.3. SI Integrators and Differentiator:

Higher-level blocks, as integrator and differentiator, can be derived from the memory cell by simple modification. In the case of integrator the output current samples

are added to input, together with input signal. Using the SI memory cells discussed in section 2.2, with proper switch clock sequence, we can build SI integrators or SI differentiators. In [51] and [52] several different SI integrators and differentiators have been introduced. Either the first generation or second generation SI memory cells can be used to design a SI integrators or differentiators. Fig. 2.4 (a) shows a non-inverting SI integrator [23] which is constructed using the second generation memory cell and it equivalent is shown in Fig. 2.4 (b).

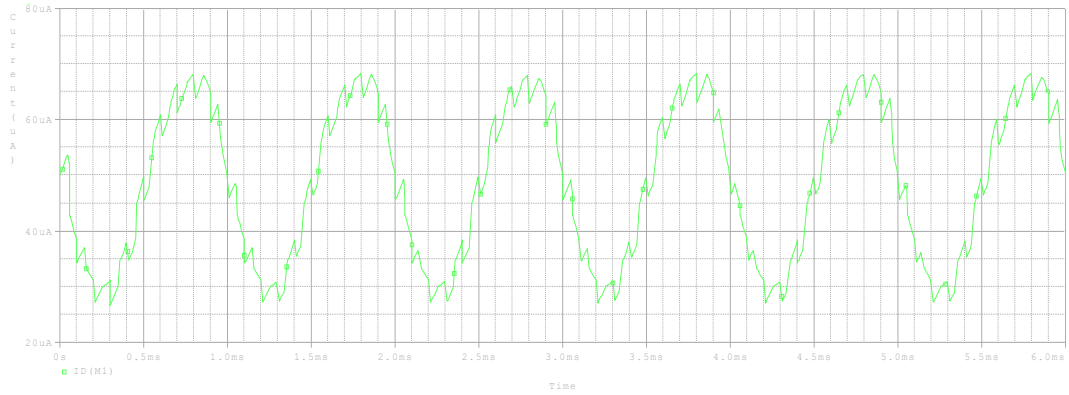


Fig. 2.1 (b): Time Response of First Generation SI Memory cell.

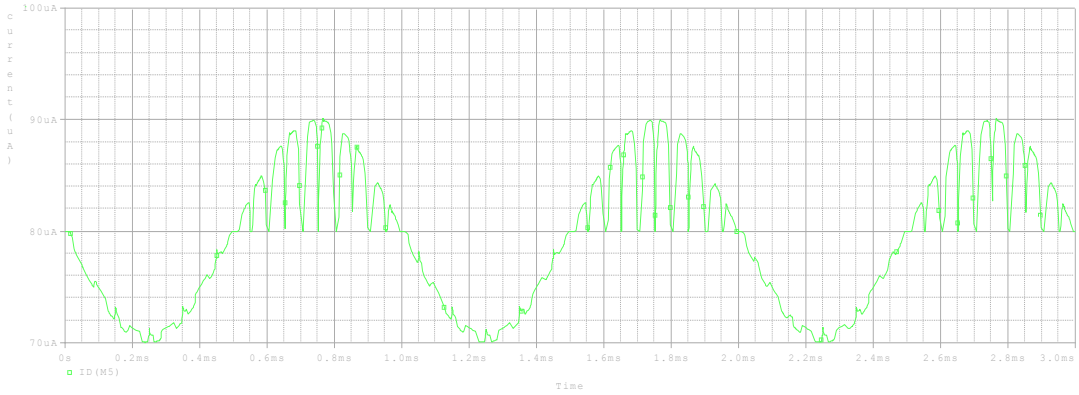


Fig.2.2 (b): Time Response of Basic second generation SI-memory cell.

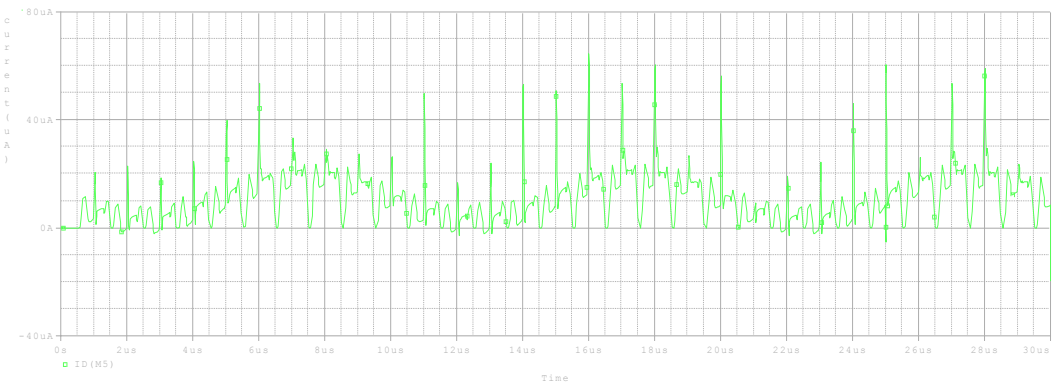


Fig. 2.3 (b): Time domain response of SI full delay.

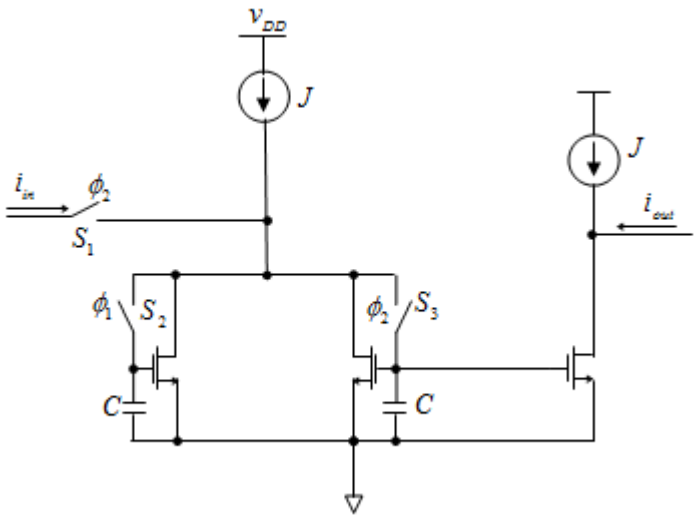


Fig. 2.4 (a): SI Non-inverting backward difference integrator

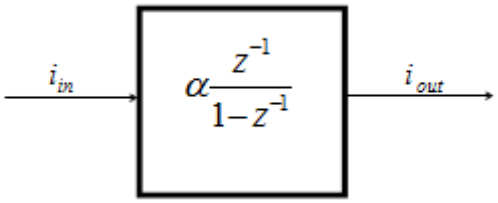


Fig. 2.4 (b): Equivalent circuit for SI Non-inverting backward difference integrator

The operation of the circuit is as fallows. On phase Φ_2 of the clock period (n-1), transistor M_2 is diode connected and its drain current i_2 is given by

$$i_2(nt) = 2I + i_{in}(nT-1) + i_{out}(nT-1) = \sum_{n=1}^{\infty} i_{in}(nT) \tag{2.5}$$

Eq. (2.6) shows the transfer function corresponding to a forward-Euler z-transform function of a lossless integrator [51].

$$H_{FE}(z) = \frac{i_2(z)}{i_{in}(z)} = \alpha \frac{z^{-1}}{1-z^{-1}} \tag{2.6}$$

By changing the input current sampling phase, the non-inverting SI integrator becomes an inverting integrator. Fig. 2.5(a) shows the second generation inverting SI integrator and its block diagram is shown in Fig. 2.5(b). The z-domain transfer function is given by.

$$H_{BD}(z) = \frac{i_2(z)}{i_{in}(z)} = -\alpha \frac{1}{1-z^{-1}} \tag{2.7}$$

This transfer function corresponds to a backward-Euler z-transform transfer function of a lossless integrator [51].

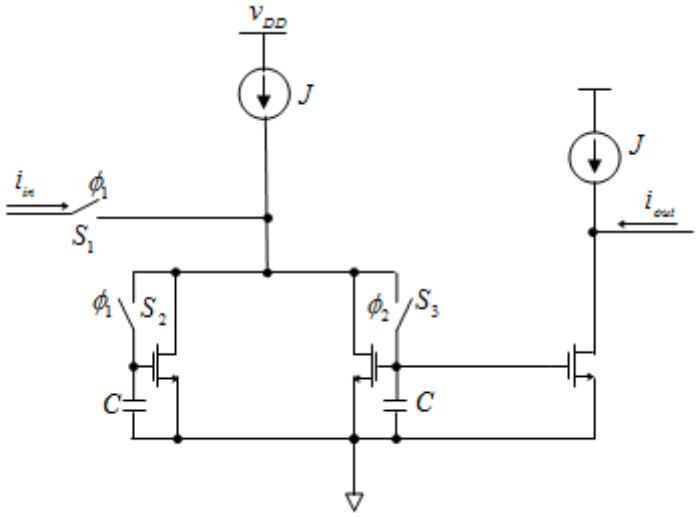


Fig. 2.5 (a): SI Inverting backward-Euler integrator

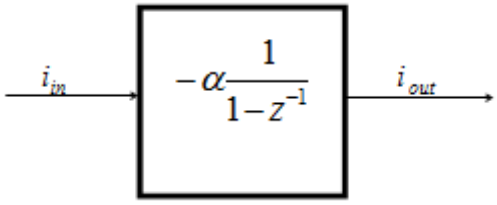


Fig. 2.5 (b): Equivalent circuit for SI Inverting backward-Euler integrator

Fig 2.6 shows a SI integrator with multiple inputs. The forward-Euler, backward-Euler and feed-forward input currents are weighted with α_1, α_2 and α_3 by scaling the W/L ratios of the output stages supplying these input currents. The output stage has a unit weight. The output current in the z-domain is given by

$$i(z) = \frac{\alpha_1 z^{-1}}{1-z^{-1}} i_1(z) - \frac{\alpha_2}{1-z^{-1}} i_2(z) - \frac{\alpha_3(1-z^{-1})}{(1-z^{-1})} i_3(z) \tag{2.8}$$

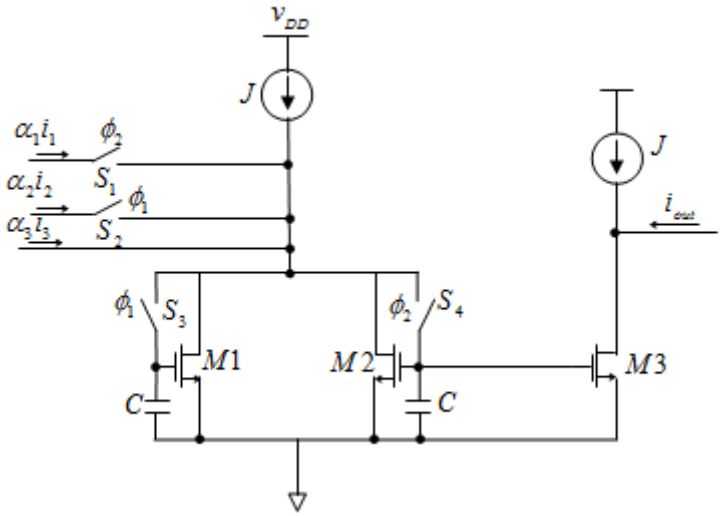


Fig. 2.6: SI multiple input integrator

Fig. 2.7 (a) and 2.7 (b) respectively shows the time and frequency domain responses for Fig. 2.4. (a).

Using the SI memory cells, the SI differentiator can also be built. Fig. 2.8 (a) and (b) shows a second-generation SI non-inverting and inverting differentiator.

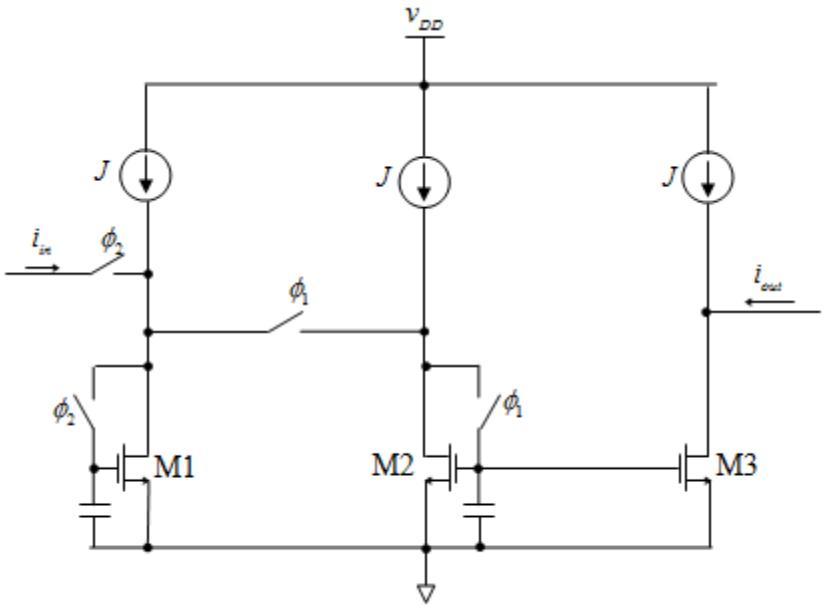


Fig. 2.8 (a): SI Non-inverting differentiator

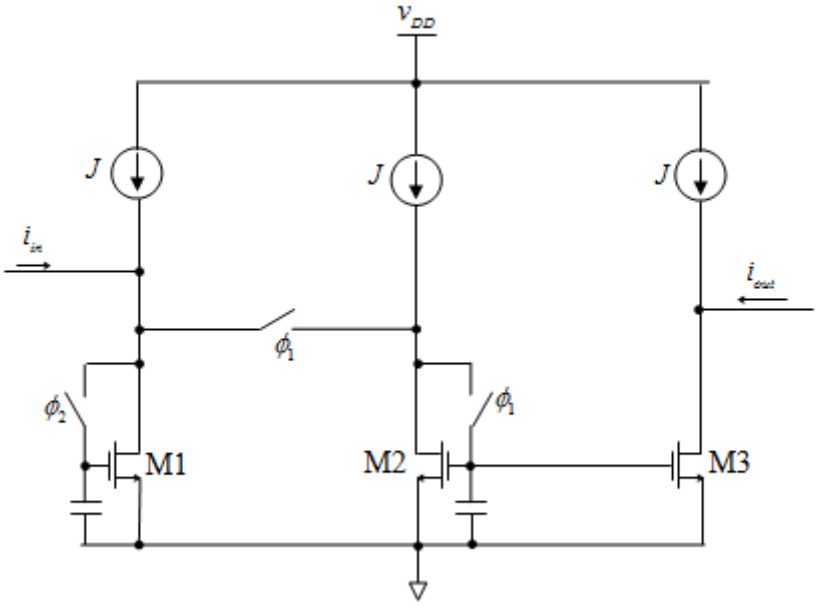


Fig 2.8 (b): SI inverting-differentiator

The operation of the differentiator is as fallows. On phase Φ_2 of the clock period (n-1), transistor M_1 is a diode connected and its drain current i_1 (current flowing through M_1) is given by

$$i_1 = J + i_{in}(n-1) \tag{2.9}$$

On the next clock phase Φ_1 of clock period n, transistor M_2 is a diode connected and its drain current i_2 (current flowing through M_2) is given by

$$i_2 = J + i_{in}(n) - I_{in}(n-1) \tag{2.10}$$

By current mirror operation of M_3, the output current i_o is given by

$$i_o = (-A)[i_{in}(n) + i_{in}(n-1) \tag{2.11}$$

and thus, the z-domain transfer function of the differentiator is obtained as

$$H(z) = \frac{i_{out}(z)}{i_{in}(z)} = -A(1-z^{-1}) \tag{2.12}$$

This equation represents a backward-Euler lossless differentiator [6]. As with the SI integrator, or a multi-input application, all input currents can be connected to the input of the differentiator directly. Fig. 2.9 shows a differentiator with multiple inputs [6].

The output current of the differentiator is given by

$$i_o(z) = -\alpha_1(1-z^{-1})i_1(z) + \alpha_2(1-z^{-1})i_2(z) - \alpha_3 i_3(z) \tag{2.13}$$

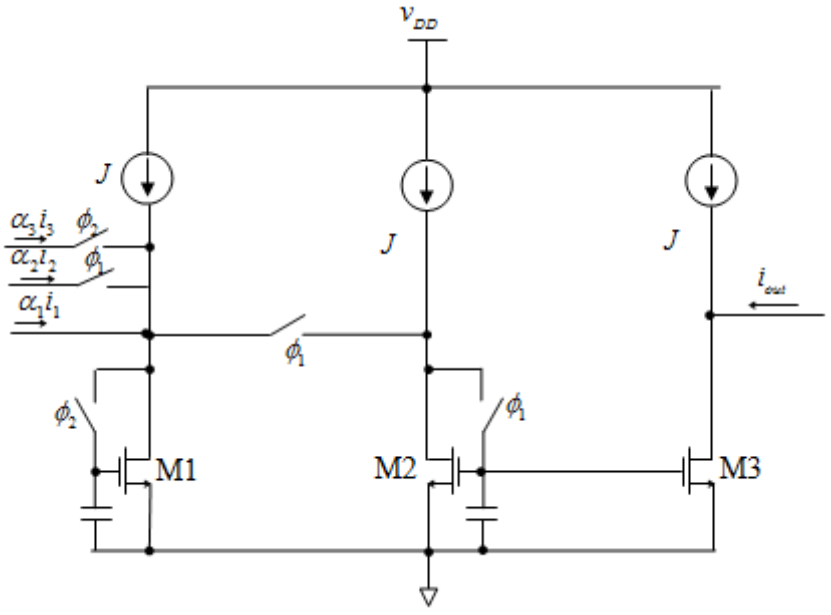


Fig. 2.9: SI multiple input inverting-differentiator

The first term of the equation corresponds to the backward Euler mapping of a lossless differentiator, the second term to a unit delay and third term to inversion and feed-forward operations.

Fig. 2.10 (a) and (b) shows the time domain and frequency domain response for Fig. 2.8 (a) respectively.

2.4. Basic Design of Sigma Delta Modulators (∑ΔMs):

Sigma-Delta (ΣΔ, or Delta-Sigma (ΔΣ)) modulation is a method for encoding high-resolution analog signals into lower-resolution digital signals. The conversion is done using error feedback, where the difference between the two signals is measured and used to improve the conversion. The low-resolution signal typically changes more quickly than the high-resolution signal and it can be filtered to recover the high-resolution signal with little or no loss of fidelity. This technique has found increasing use in modern electronic components such as A/D and D/A converters, frequency synthesizers, switched-mode power supplies and motor controllers. A very popular application of delta-sigma conversion is in audio applications where a digital audio signal, as from an MP3 player, is converted into the analog audio signal which will be amplified and output to speakers or headphones. Since the output of this modulator typically has only two levels, the generation of the analog output signal is power efficient.

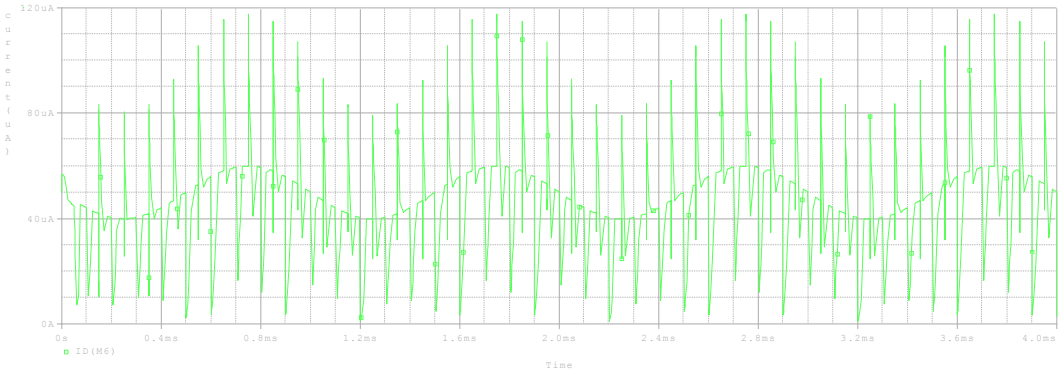


Fig. 2.7 (a): Time response of SI integrator

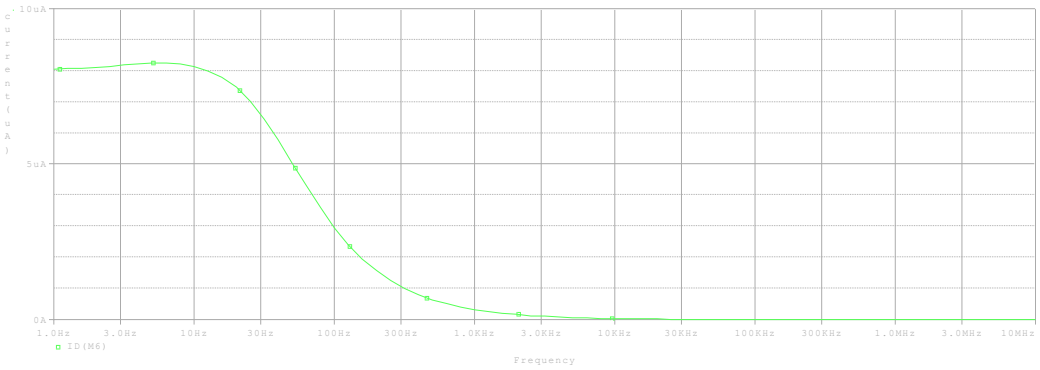


Fig.2.7 (b): Frequency response of SI integrator.

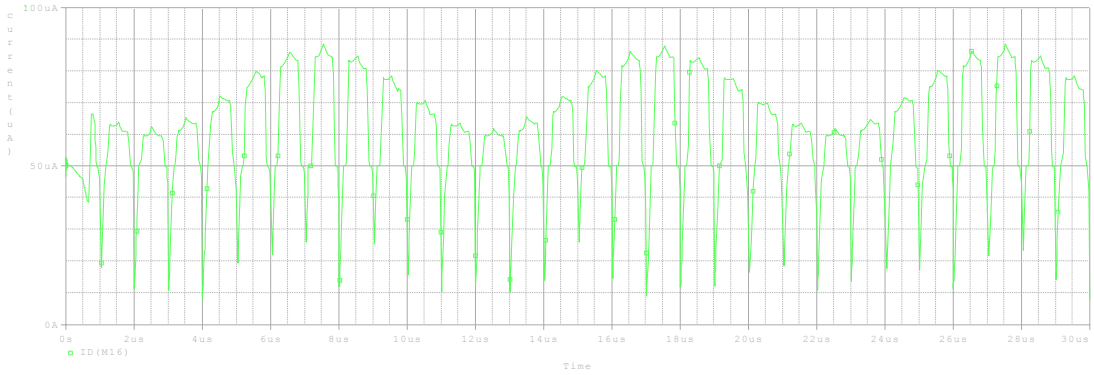


Fig. 2.10

(a): Time Domain Response of Differentiator

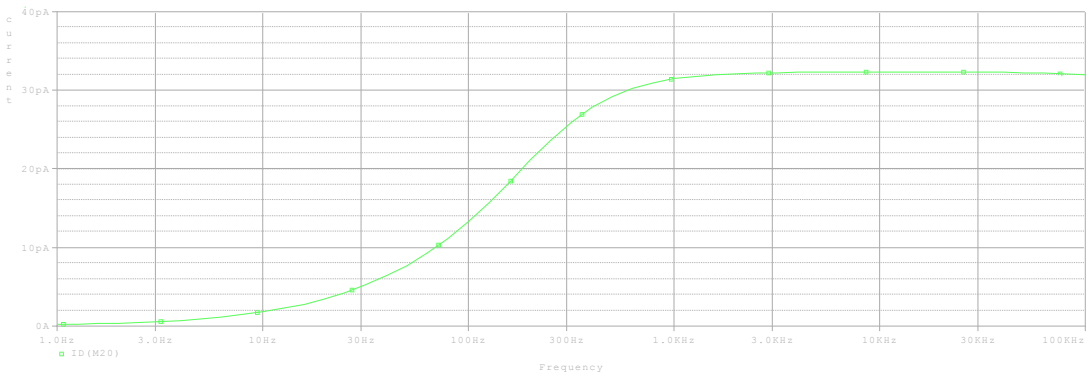


Fig. 2.10

(b): Frequency Domain Response of Differentiator.

Further, because the modulator's output signal changes much faster than the desired audio signal, it can be heavily filtered and the resulting analog signal has high enough fidelity for use in professional applications. Low cost, low power and high fidelity make delta-sigma modulators very popular. So SI technique seems to be much feasible for the design of ∑ΔMs [100, 101].

The basic ∑Δ modulator is shown in Fig. 2.11 (a) and its linear model is shown in Fig. 2.11. (b).

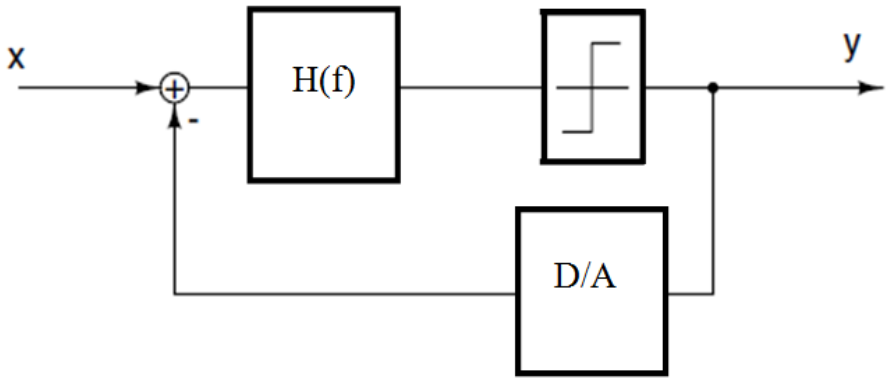


Fig. 2.11. (a): Block diagram of a ∑Δ modulator.

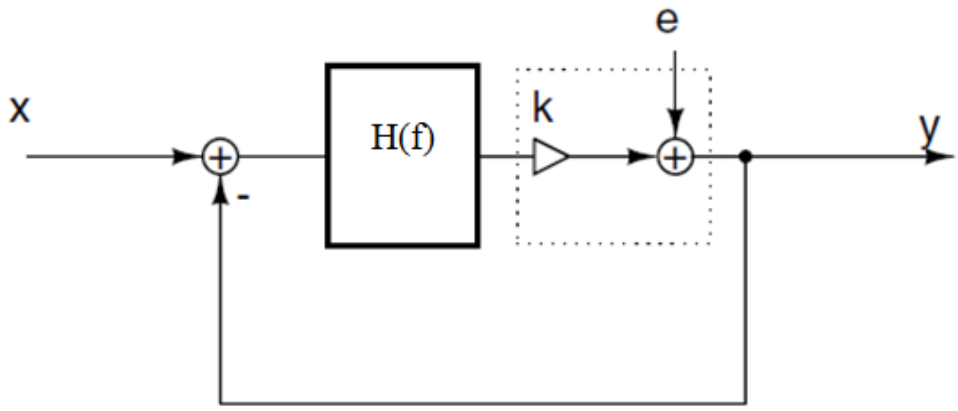


Fig. 2.11 (b): Linear model of a ∑Δ modulator.

The basic ∑Δ modulator consists of a loop filter, a quantizer and a feedback loop. There should be a digital to analog converter inside the feedback loop since the output of the quantizer is a digital signal. The linear model of a ∑ΔM models the quantizer with a quantization gain *k* and a noise source.

It is assumed that the D/A inside the feedback loop is an ideal one. In this system, there are two input signals, $x(n)$ and $e(n)$, and one output signal $y(n)$. The output of the ∑Δ modulator can be expressed as:

$$Y(Z) = H_x(z)X(z) + H_e(z)E(z) \tag{2.14}$$

Where $H_x(z)$ represents the signal transfer function and $H_e(z)$ represents the quantization noise transfer function in the domain. The signal and noise transfer function can be calculated as:

$$H_x(z) = \frac{H(z)}{1+H(z)} \tag{2.15}$$

$$H_e(z) = \frac{1}{1+H(z)} \tag{2.16}$$

It is seen that the signal transfer function is different from the noise transfer function. By properly choosing the loop filter transfer function H(z), the desired signal and noise transfer function can be obtained within a certain band of interest. If the loop filter transfer function H(z) is designed to have a large gain inside the band of interest and small gain outside the band of interest, then the signal and noise transfer functions become:

$$H_x(z) = 1 \tag{2.17}$$

$$H_e(z) = \frac{1}{1+H(z)} << 1 \tag{2.18}$$

The signal can pass through ∑Δ modulator directly and the noise is greatly reduced inside the band of interest. This is called noise shaping.

For example, if an integrator is chosen to be the loop filter, its transfer function is:

$$H(z) = \frac{z^{-1}}{1+z^{-1}} \tag{2.19}$$

Then the signal and noise transfer functions of the ∑ΔM can be calculated as:

$$\begin{aligned} H_x(z) &= z^{-1} \\ H_e(z) &= 1 - z^{-1} \end{aligned} \tag{2.20}$$

2.5. Switched Current Filter:

Filtering is a major application of the switched current technique. There are a number of papers dealing with the SI filter design [52, 53, 54]. Since the SI integrator and differentiator, from the transfer function point of view, correspond directly to the switched capacitor integrator and differentiator, respectively, all the synthesis technique developed for the design of switched capacitor filter can be used for the synthesizing switched current filters. Mapping from a SC filter to a SI filter is a straight forward process with the second generation integrator, as there is a direct correspondence between capacitor ratio in SC filter and the aspect ratios W/L in the SI counterpart.

As an example, a z-domain block diagram of a biquadratic section [55] is shown in Fig. 2.12 and its transfer function is given by

$$H(z) = \frac{i_o(z)}{i_{in}(z)} = \frac{(a_5 + a_6)z^2 + (a_1a_3 - a_5 - 2a_6)z + a_6}{(1+a_4)z^2 + (a_2a_3 - a_4 - 2)z + 1} \tag{2.21}$$

The circuit implementation with second generation SI inverting and non-inverting integrators is shown in Fig. 2.13[56].

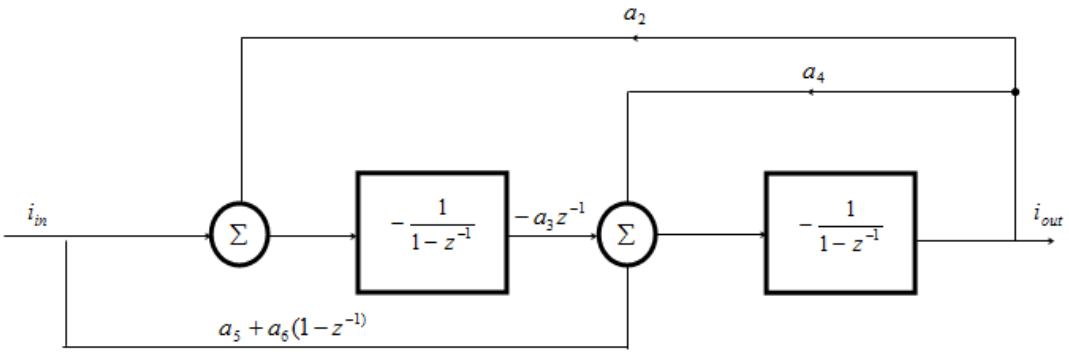


Fig. 2.12: A z-domain block diagram of an integrator based biquadratic section

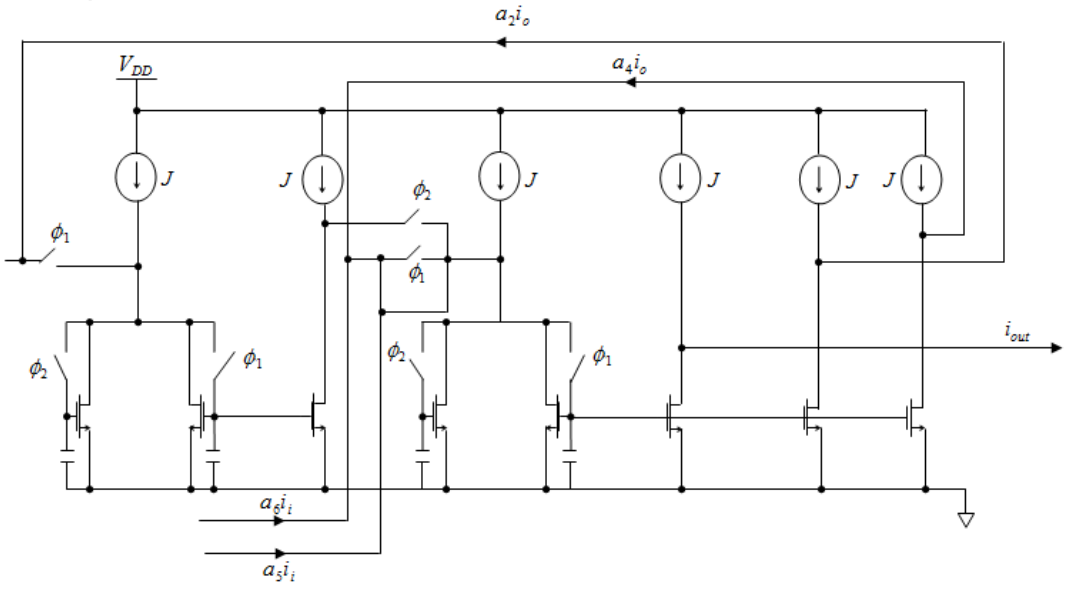


Fig. 2.13: A second-generation SI integrator based biquadratic section.

2.5.1. Switched Current Resonators:

Resonators are second-order filter sections (also called *biquads)* which realize a band-pass transfer function. Resonators play the same role in Band Pass (BP) Sigma Delta modulators (∑ΔMs) as integrators in Low Pass∑ΔMs. For this reason, the synthesis and design of this block is crucial in order to get a good performance of the BP∑ΔMs. This section explores all possible topologies of resonators which use SI circuits (integrators, differentiators and delay cells). As in the case of integrators and differentiators, the most appropriate SI resonator structures can be obtained by emulating

the well-known CT (continuous time) resonators. Therefore, as a starting point, the basic properties of biquads will be reviewed and fundamental design parameters used in the design process will be defined.

2.5.1.1 Biquad Filter Background:

Biquad filters are more flexible and universal than first-order filters since they can realize all types of filtering functions: low-pass, high-pass, band-pass, band-stop and all-pass. A discrete time (DT) biquad can be described in the *Z*-domain by a transfer function of the form [57]

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{2.22}$$

Substituting $z=e^{ST_s}$ in Eq. (2.22), and assuming that the frequencies which are of interest are much lower than $1/T_s$, it can be shown that the continuous-time biquadratic transfer function corresponding to Eq. (2.22) can be expressed, after some manipulations, as [57]

$$H(s) = \frac{k_2 s^2 + k_1 s + k_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0} \tag{2.23}$$

Where Q is the pole quality factor and ω_0 is the resonant angular frequency. It is interesting to note that Q describes the selectivity of the biquad. Thus, if Q is high, the magnitude of the transfer function H(s) will have a sharp peak near ω_0. Specifically, let us assume that the transfer function has two conjugate-complexes poles at $s_{p1,2}= -\sigma \pm j\omega_p$ then, it can be shown that they are related to the parameters ω_0 and Q as

$$\begin{aligned} \sigma_p &= \frac{\omega_0}{2Q} \\ \omega_p &= \omega_0 \sqrt{1 - \frac{1}{4Q^2}} \end{aligned} \tag{2.24}$$

By analogy with the continuous-time case, for any pair of conjugate-complex poles in the *Z*-domain we can represent the denominator of Eq. (2.22) in canonic form as

$$D(z) = 1 - 2r\cos\phi . z^{-1} + r^2 z^{-2} \tag{2.25}$$

It can be easily derived that the roots of the above equation (the poles of Eq. (2.22)) can be expressed as $z_{p1,p2}=re^{\pm j\Phi}$ being

$$r = e^{\frac{-\omega_0 T_s}{(2Q)}}$$
$$\phi = \omega_0 T_s \sqrt{1-\frac{1}{4Q^2}} \qquad Q \geq 1/2 \tag{2.26}$$

The above relationships provide considerable simplification in the analysis and design of biquads. However, more exact formulae can be obtained by applying the bilinear s-z transformation to Eq. (2.22). After some algebraic manipulation and identifying Eq. (2. 26), it can be shown that

$$\omega_0 = \frac{2}{T_s}\sqrt{\frac{1+a_2+a_1}{1+a_2-a_1}}$$
$$Q = \frac{\sqrt{(1+a_2)^2-a_1^2}}{2(1-a_2)} \tag{2.27}$$

On the other hand, the DT resonant angular frequency, denoted by ω_0 can be derived giving

$$\omega_0 = \frac{2}{T_s} a\tan\left(\frac{\omega_0 T_s}{2}\right) \tag{2.28}$$

If the biquad is composed of SC circuits, the scaling coefficients of Eq. (2.22), i.e., a_i and b_i, are realized by capacitor ratios. On the other hand, if the biquad is made up of SI circuits, a_i and b_i are physically implemented through current mirrors by weighting the aspect ratio between the input and the output currents. Let α be a parameter which represents the capacitor ratio (in SC realization) or the transistor aspect ratio (in SI realization). The sensitivity of Q with respect to α, represented by S_α^Q is a critical parameter which is often used as a measure for different filter configurations. It can be derived from Eq. (2.27) that.

$$S_\alpha^Q = \frac{\alpha}{Q}\frac{\partial Q}{\partial \alpha} = \alpha\left[\frac{-a_1\left(\frac{\partial a_1}{\partial \alpha}\right)+[(2+2a_2-a_1^2)/(1-a_2)]\left(\frac{\partial a_2}{\partial \alpha}\right)}{(1+a_2)^2-a_1^2}\right] \tag{2.29}$$

The transfer function of Eq. (2.23) is quite general, and in fact, different filter functions (low-pass, high-pass, band-stop and band-pass) can be derived by appropriately selecting the numerator coefficients [30]. Here we are interested only in a particular type of biquads, often called resonators, which realize a band-pass filter function, given by:

$$H(s) = \frac{Ks}{s^2 + (\omega_0 / Q)s + \omega_0^2} \tag{2.30}$$

Depending on the s to z transformation used, different z-domain resonator transfer functions can be derived whose denominator can be expressed in the form of Eq. (2.25). In the following, we will refer to resonators as DT resonators which can be described by the following transfer function

$$H(z) = \frac{Kz^{-a}}{1 - 2r\cos\phi.z^{-1} + z^{-2}} \tag{2.31}$$

Where $0 < a < 2$

2.5.1.2. Resonator Structures Based On Differentiators and Integrators:

There are many filter structures which implement the transfer function shown in Eq. (2.32) [58]. The integrators which form the loop filter in the original modulator become resonators which are described by the following transfer function:

$$H_{res}(z) = \frac{\pm z^{-a}}{1 + z^{-2}} \tag{2.32}$$

Assuming an ideal realization of the resonator, all these structures would provide identical behavior. However, in the presence of errors, the scaling coefficients which are used to build the mentioned structures deviates from their nominal values due to either capacitor ratio errors – for SC circuits – or to transistor size ratio errors – in the case of SI circuits. This causes different resonator structures to behave differently. The most important effect is that the position of the filter poles is affected in different ways by the errors. In some structures the filter poles move around the unity circle in the *Z*-plane. This results in the resonant frequency not being properly placed. In other structures the

effect of errors will move the resonator poles off the unit circle (in the *Z*-plane), causing unstable behavior. If the poles move inside the unit circle, then the *Q* factor will be reduced, thus reducing the gain of the filtering at the resonant frequency.

Fig. 2.14 (a) shows a resonator structure made up of Lossless Discrete Integrators (LDI). This topology, often called LDI-loop resonator [58], has a transfer function of the form:

$$\frac{Y(z)}{X(z)} = \frac{A_F z^{-1}}{1-(2+A_F A_{FB})z^{-1}+z^{-2}} \tag{2.33}$$

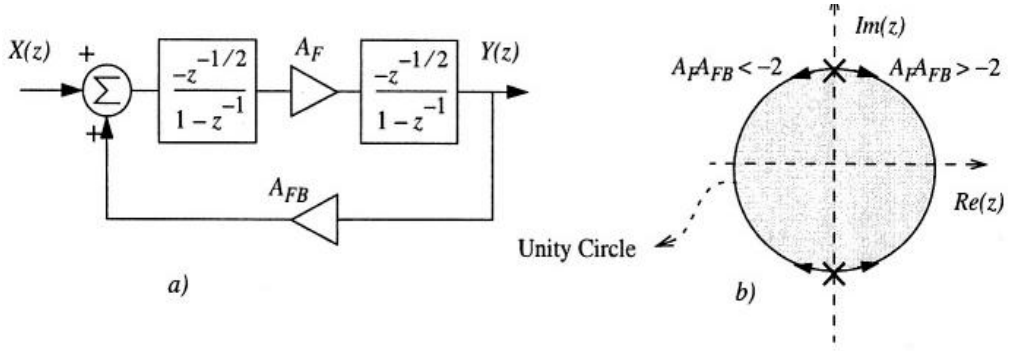


Fig. 2.14: LDI-loop resonator. (a) Block diagram. (b) Movement of poles with errors.

Which for the nominal values of the scaling coefficients A_F=1 and A_{FB}= -2 results in the transfer function of Eq. (2.32) with a=1. As was mentioned in the previous section, *Q* and ω_{0d} are crucial parameters which define the selectivity and the resonant frequency of the resonator. For the resonator in Fig. 2.14, nominally, $\omega_{0d}= \pi/ (2T_s)$ and $Q \to \infty$ (Infinite Q is reached if LDIs are considered ideal), however, in the presence of errors, a finite Q is obtained). In practical cases, the errors associated to the scaling coefficients in Fig. 2.14 (a) will shift the resonant frequency $\omega_{0d} = 1/T_s \text{acos}\ (1+(A_F A_{FB})/2)$. However, *Q* will remain at its nominal value. This is illustrated in Fig. 2.14. (b) by plotting the movement of the resonator poles in the *Z*-plane for changes in A_F and A_{FB}. It can be seen how the poles move around the unity circle thus guaranteeing that this structure will be stable.

Fig. 2.15 (a) shows another resonator structure which realizes the transfer function in Eq.(2.32), with a=2. It is made up of two non-inverting Forward Euler (FE) integrators. The first integrator has to be damped with a feedback scaling gain, named A_{FB2}. The transfer function of this resonator is given as

$$\frac{Y(z)}{X(z)} = \frac{A_F z^{-2}}{1-(2+A_{FB2})z^{-1}+(1+A_{FB2}-A_{FB1})z^{-2}} \tag{2.34}$$

For the nominal values of the scaling coefficients: A_{FB}= 1 and A_{FB1} = A_{FB2} = -2 yields z_p= exp (±jπ/2) giving the same values of ω_{0d} and *Q* as with the LDI-loop resonator. However, the main drawback of the circuit in Fig. 2.15. (a) is that errors in scaling coefficients can move poles outside the unit circle as illustrated in Fig. 2.15. (b). Note that only the errors in A_{FB2} will force poles to move around the unity circle thus causing $\acute{\omega}_{0d}$ to shift from its nominal position.

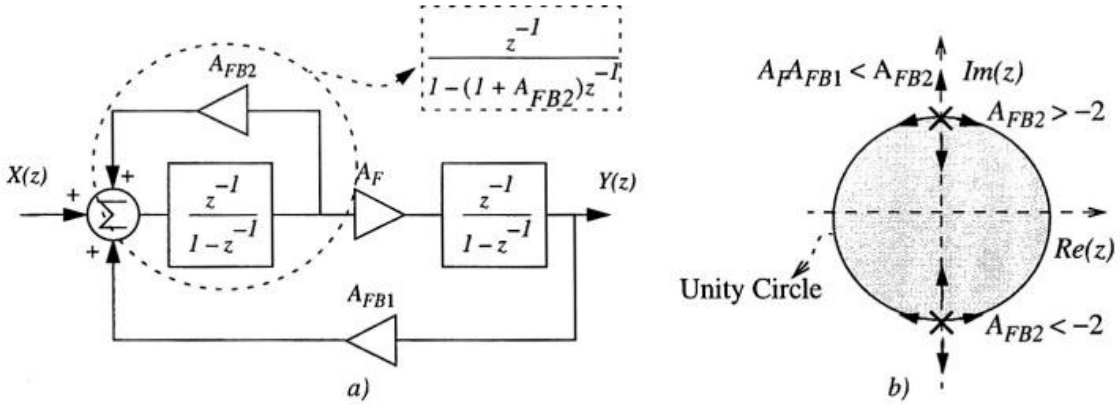


Fig. 2.15: FE-loop resonator. (a) Block diagram. (b) Movement of its poles with errors.

The FE-loop resonator becomes unstable if $A_{FB}A_{FB1}<A_{Fb2}$. Although this fact appears to be a drawback as compared to LDI-loop resonators, some authors propose to design filters with a small instability with the objective of reducing idle tones in ∑Δ modulators [59]. In fact, the authors in [60] reported similar experimental results from two second-

order BP∑ΔMs one of them based on LDI-loop resonators and the other one using FE-loop resonators.

The resonator in Fig. 2.16 can also be realized using a differentiator with the transfer function given as:

$$\frac{Y(z)}{X(z)} = \frac{z^{-1}}{1+z^{-1}} \tag{2.35}$$

It can be illustrated in Fig. 2.16(a), whose transfer function is

$$\frac{Y(z)}{X(z)} = \frac{A_F z^{-2}}{1-(1+A_{FB2})z^{-1}+(A_{FB2}-A_F A_{FB1})z^{-2}} \tag{2.36}$$

Which for the nominal values: A_F=1, A_{FB}=-2 and A_{FB}=-1 results in the transfer function in Eq. (2.32) with a=2. As Fig. 2.15 (b) illustrates, the resonator in Fig. 2.16 (a) presents similar degradation to the resonator of Fig. 2.15 (a) under errors on the scaling coefficients, the only difference being the nominal value of A_{FB2}.

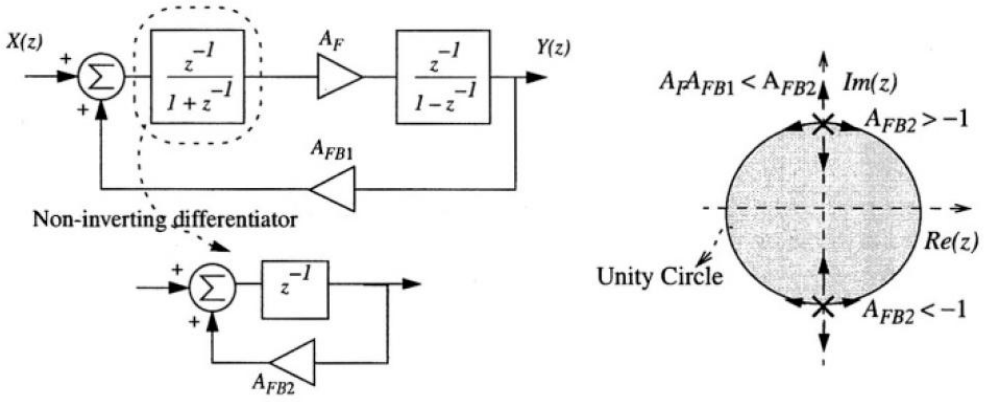


Fig. 2.16: Resonator Based on a differentiator and an integrator. (a) Block diagram (b) Movement of its poles with errors

2.5.1.3 Design of SI Resonators:

The growing interest in LP∑ΔMs in the last years has motivated the development of many different topologies for SI building blocks such as integrators and differentiators. However, very little has been done in the field of BP∑ΔMs [61]. As a consequence, there has not been so much interest in the design of SI resonators – the basic building block of BP∑ΔMs. The objective of this section is to describe different ways of realizing these blocks with SI circuits. As was explained in the previous section, the resonator block can be realized through the interconnection of smaller sub-blocks as delay units and integrators using different alternative structures.

2.5.1.3.1. SI Lossless Discrete Integrator (LDI)-Loop Resonators:

The LDI-loop resonator is represented by the block diagram of Fig. 2.14 (a). This structure can be realized using SI circuits by connecting in a single loop two LD SI integrators as shown in Fig. 2.17 Applying the expressions used for integrators; it can be shown that the finite-difference equations which govern the resonator behavior are:

$$\begin{aligned} i_{01,n} &= -A_F\,(i_{i,n-1/2} + A_{FB} i_{o,n-1/2}) + i_{o1} \\ i_{o,n} &= -i_{o1,n-1/2} + i_{o,n-1} \end{aligned} \tag{2.37}$$

Where i_{o1} and i_o are the output currents of the first and second integrators, respectively. Rearranging the above equations and taking the *Z*-transform, the transfer function for the resonator in Fig. 2.17 results in Eq. (2.32). Note that an additional current mirror (not shown in Fig. 2.16) is required to implement the inversion of the nominal value of the scaling feedback coefficient.

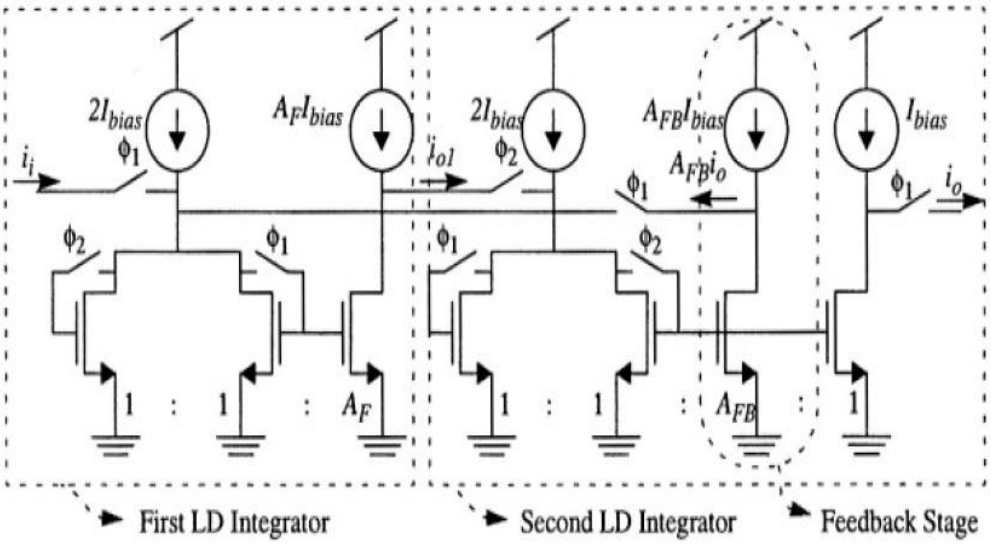


Fig. 2.17: Conceptual realization of an SI LDI-loop resonator.

2.6. SI A/D and D/A Converter:

The switched current technique is a striking technique for implementing data conversion schemes, since switched-current circuits do not require linear capacitors and, in general, are capable of working with low supply voltages.

Some SI A/D and D/A converters have been proposed that use algorithmic structure or ∑ΔMs [62, 63, 64]. Fig. 2.18 shows a simple example of an algorithmic D/A converter.

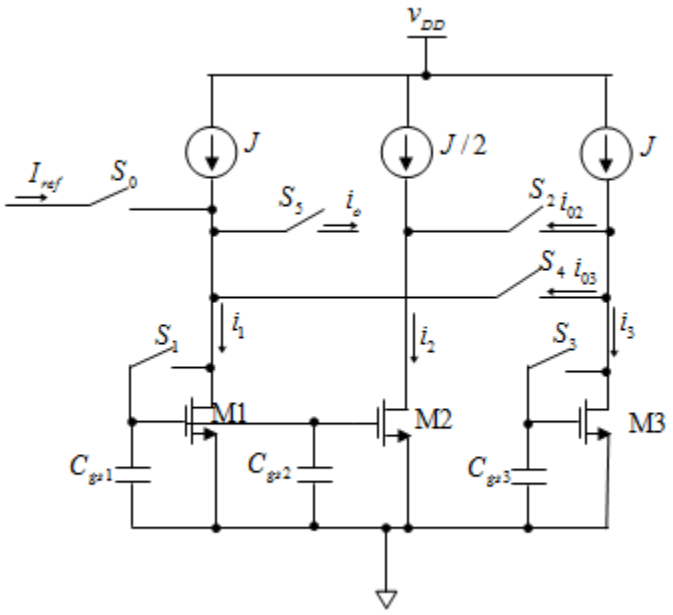


Fig. 2.18: A SI algorithmic D/A converter

The circuit consists of two memory cells. The cell M_1 has an extra ½ scaling stage used for the implementation of divide by two functions. The operation of the conversion is stated from the least significant bit (LSB). Conversion of each bit (one conversion cycle) needs 2 clock cycles. The operation of the converter is as follows. In the first clock cycle, switches S_0 and S_1 are closed if the first digital bit is '1'; the current i_1 is set to $(J + I_{ref})$. The current i_2 becomes $(J + I_{ref})/2$ and therefore, i_{02} equals $I_{ref}/2$. The reference current is divided by two at this point. If the first digital bit is '0', so is opened. The current i_1 equals J, i_2 equals J/2 and therefore, i_{02} is zero. the transistor M_3samples and hold I_{02} by closing the switches S_2 and S_3 and $i_3=J+I_{02}$. Next, S_1 and S_4 are closed, $I_{03}=J - i_3=i_{02}$. If the second digit bit is '1', S_0 is closed, M_1 samples and holds the reference current and the current from M_3, the current i_1 is set to $J+I_{ref}+i_{03}$. If the second digital bit is '0'. M_1 only samples and holds the current from M_3, and i_1 will be set to $(J+i_{03})$. The operation is repeated until the most significant digital bit (MSB) is converted. In contrast, M_1 adds and holds the current signal from switches S_0 and S_4 at every conversion cycle the previous conversion current is divided by two and added with the reference current or the zero current. The algorithm of the D/A converter, therefore is given by

$$i_o(n) = I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k \tag{2.38}$$

At the end of the conversion, switch S_5 is closed to present the converted current to the output. The accuracy and resolution of the D/A converter is limited by the ratio of M_1 and M_2.

Fig. 2.19 gives an example of an A/D converter that uses ratio-independent algorithmic conversion operation [52]. The advantage of the circuit is that the conversion accuracy is not dependent on the ratio of transistors. The conversion starts with MSB. The operation of A/D converter is as follows: At the beginning, switches S_1, S_2, S_3 closed the current $i_1=I_t$. Then switches S_2 and S_3 are opened while S_4 and S_5 are closed and the current $i_2=I_i$. Both the currents i_1 and i_2 are loaded into M_3 by opening S_1 and S_5 and closing S_4, S_5, S_6 and S_7. The current i_3 becomes $2I_t$, then opening the switch S_2,S_4 and S_7 and closing S_6 and S_8, the doubled input signal $2I_t$ is compared with the reference current I_{ref}. If the signal exceeds the reference, the MSB is '1' otherwise it is '0'. To convert the next bit, the signal current, which is stored in M_3 is loaded in $M_1$by closing S_2, S_3, and S_6. If the previous output digital bits are '1', S_8 is closed and the signal current in M_3 is subtracted by the reference current. If the previous output digital bit is '0'. S_8 is opened, and the signal in M_3 remains unchanged. Once M_1 is set, M_2 is also set in a similar way. The conversion is then repeated with the same operation as with MSB operation and it continues until the desired resolution is achieved.

The conversion speed of the circuit is 4 clock cycle for each bit of conversion. Thus, an N-bit conversion requires 4N clock cycle. The maximum conversion accuracy and resolution is limited by the switch charge injection and finite impedance of the MOS transistors.

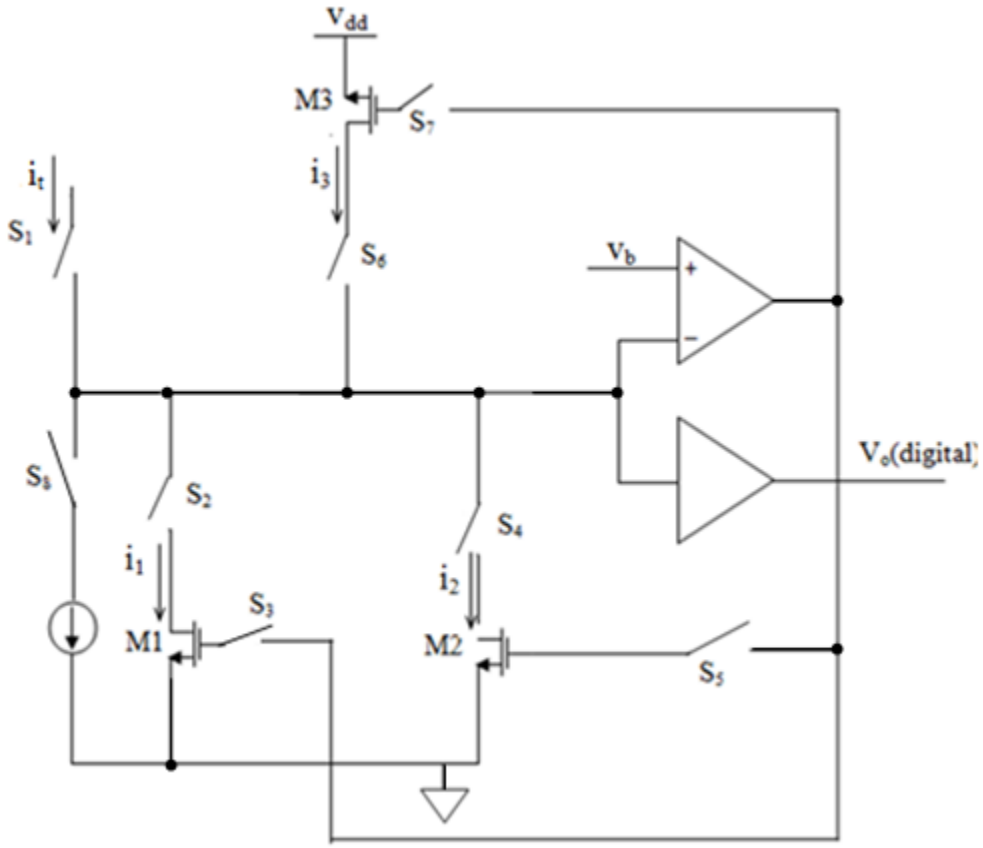


Fig. 2.19: A current mode ratio-independent algorithmic A/D converter

2.7 Summary:

In this chapter, SI first and second generation memory cell is simulated using PSPICE, but for higher order circuits we only use SI second generation memory cell. The SI circuit can sample and hold the current signals through the charge stored on the gate capacitor of a MOS transistor. Therefore, a SI circuit can perform the analog sample data processing without requiring linear capacitors. Since the signals in a SI circuit are presented as current, it is possible to work with low power supply voltages.

The design technique relies on digital filter synthesis technique for obtaining the filter structure as well as the SI circuits. The coefficients of the transfer function are matched to the coefficient transistors of the filter directly. By just changing the size ratios of the coefficient transistors, different frequency characteristics of the filters can be

obtained. In this chapter various circuits are simulated and their result shows how variation of W/L ratio changes the characteristics of circuit.

Error Analysis in Switched Current Circuits

3.1. Introduction:

The behaviour of Switched current (S.I) circuit's blocks deviates from the ideal performance as a consequence of MOS transistor imperfections. Although the main non-idealities which degrade the performance of SI circuits have been identified and described in literature [37, 38], very little has still been done in the analysis and modeling of these errors as well as their influence on the performance of building blocks. The analysis of basic block SI non-idealities is treated in this chapter with two well-differentiated objectives: on the one hand, the obtainment of behavioural models that support a fast and precise time-domain simulation; on the other hand, the attainment of approximate equations which, in closed form, express the effect of each non-ideality on the performance of the cell, as a function of itself and other design variables. Those equations will provide the quantitative knowledge on the cell parameters for each SI error. This will allow the designer to control the non-idealities either through the choice of MOS transistor sizes and bias current (sizing) or by means of proper circuit techniques. Special emphasis will be put on signal-dependent errors since they have been demonstrated as one of the main performance limitations in practical circuits such as filtering [37,39,40] and Analog-to-Digital Converters (A/D) [38,41].The performance of these SI circuits is based on the assumptions of employing ideal MOS devices, but a MOS device in practice is never ideal. A SI circuit will suffer from degraded performance through analog errors resulting from the non-ideal MOS transistor characteristics. In this section we will study the effects of using non-ideal MOS devices through the analysis of the second generation SI memory cell.

The non-ideal characteristics of MOS transistors stem from:

(1) Channel length modulation caused by the drain voltage variation resulting from the changes in the drain current.

(2) Gate-drain and gate-source parasitic capacitances and channel charge that produce the switch charge injection resulting in memory current error and harmonic distortion.

(3) Non-zero closure resistance of MOS switches causing incomplete charging of the memory transistor gate capacitor when the transistor is diode-connected and thus leading to settling time error.

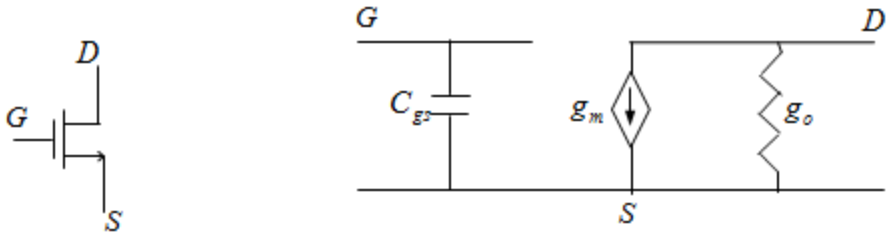
(4) Process of mismatch between the memory transistor and scaling transistor (current mirror transistors) causing current gain error, offset and harmonic distortion.

(5) MOS transistor thermal noise and I/F noise resulting in memory current error.

Since the thermal noise and I/F noise are not significant in SI circuits [23] as compared to others errors, so they are not discussed

3.2 Effect of Channel Length modulation and Non-Zero Closure Resistance:

The channel length modulation, also called the finite impedance problem, is caused by the channel shortening of the MOS transistor. When the simple SI (Second generation memory cell) memory cell works in the sample mode, the memory transistors drain voltage is forced to be of the same value as gate voltage. When the memory cell works in the hold mode, the gate voltage held almost constant and the memory transistor outputs a current to its load. If the drain voltage changes, the output current also changes because of the channel length modulation. The change in drain voltage causes an error in the output current.



(a) An NMOS transistor **(b) Equivalent circuit**

Fig 3.1: An NMOS transistor equivalent circuit.

Fig 3.1 shows the small signal equivalent circuit of an NMOS transistor. When considering the channel length modulation effect, the drain current of a MOS transistor is given by

$$I_d = \frac{\beta}{2}(V_{gs} - V_t)^2(1 + \lambda V_{ds}) \tag{3.1}$$

Where λ is the cannel length modulation factor, $\beta = h_p(W/L)$, and $h_p = \mu_0 C_{ox}$ is the process gain factor. This effect may be modified for small signals by a drain conductance g_o, and it is given by

$$g_o = \frac{\partial I_d}{\partial V_d} = \lambda I_d \tag{3.2}$$

Where I_d is the ideal drain current. When considering a cascade SI memory cell application, a current error is produced due to the output conductance g_{o1} of the previous stage, the output conductance g_{o2} of the present stage, and the non-zero closure resistance of MOS switch. Fig. 3.2 illustrates the effects of the finite output impedance of MOS devices. With the finite output impedance of MOS transistor, the input current i' to the next SI memory cell is given by

$$i' = \frac{i}{\left(1 + \frac{g_{01} + g_{02}}{g_{m2}} + \frac{g_{01}}{g_3}\right)} \tag{3.3}$$

Letting $g_{01}=g_{02}=g_0$ and since in typical applications, $g_0<<g_m.g_{03}$ in Eq.3.3 can be written as

$$i' = i\left[1-\frac{2g_0}{g_{m2}}-\frac{g_0}{g_{03}}\right] \tag{3.4}$$

Hence, the error current ΔI due to the finite impedance is given by

$$\Delta I = i - i' = i\left[\frac{2g_0}{g_{m2}}+\frac{g_0}{g_{03}}\right] \tag{3.5}$$

Thus, it is obvious that the channel length modulation of the memory MOS transistor and non-zero closure resistance of MOS switch produce a current gain error. Usually, when the signal current is small, the effect of the non-zero closure resistance $1/g_{03}$ of the switch can be ignored. The error current becomes

$$\Delta I = i - i' = i\left[\frac{2g_0}{g_{m2}}\right] \tag{3.6}$$

However, when signal current is large, such as in D/A or A/D converter application, the non-zero closure resistance affects the SI circuit performance. To reduce the effect of channel length modulation, there are two solutions. The first is to keep the drain voltage constant and second is to increase the output resistance of the memory cell.

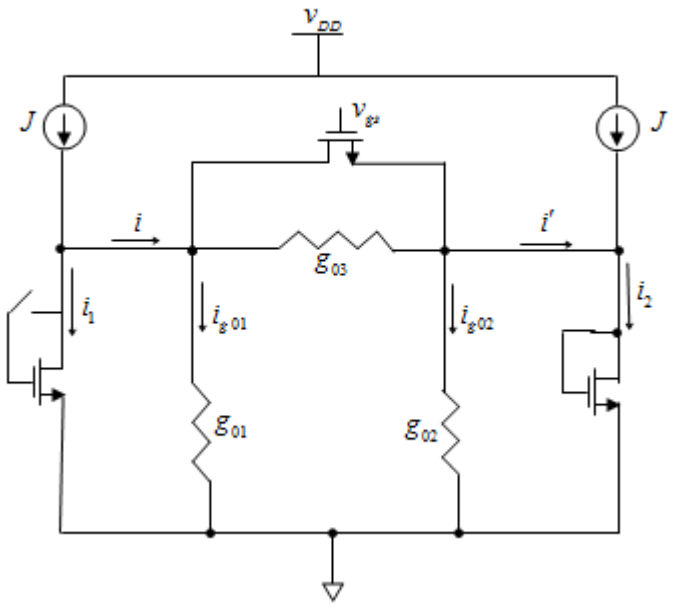


Fig. 3.2: An illustration of the effect of the finite output impedance of MOS transistor.

3.3 Finite Output-Input Conductance Ratio Error:

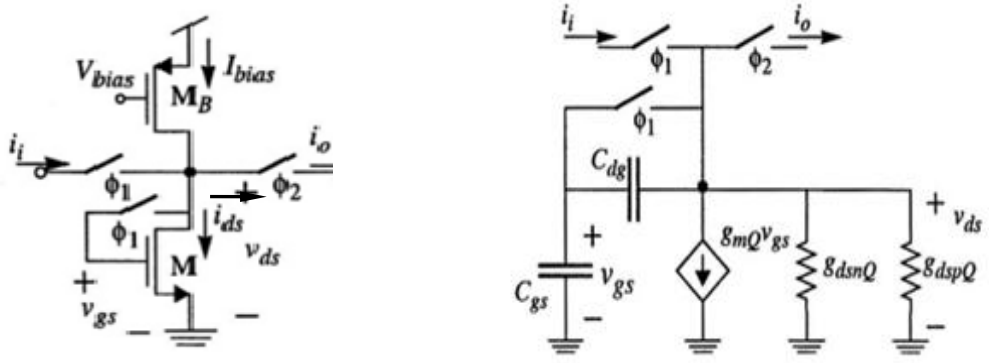
Simple second-generation memory cells like those shown in Fig. 3.1(a) behave as either the input or the output stage of a current mirror depending on the clock phase in which they are operating. During the sampling phase, the drain of the memory transistor is connected to its gate and the input current flows through it. On the hold phase, the connection between the drain and the gate of the memory transistor is split and the cell delivers its output through the load. As a consequence of this dual operation, the drain of the memory transistor will be at different voltages on both clock phases 1. This voltage variation is translated into an error on the memorized drain current basically through two mechanisms [42]. The first is caused by the channel length modulation effect of both the memory transistor and the bias current source transistor. The second one is due to the charge which flows through the drain gate overlap capacitance into the gate capacitance, thus causing an error on the gate voltage and consequently on the memorized drain current.

These two mechanisms of error can be modeled as a finite output conductance connected in parallel with the memory transistor [42, 43]. Thus, when a memory cell is in its hold phase and it delivers its output to another cell (in sampling phase), the drain current memorized by the latter will contain an error caused by the parallel connection of its finite input conductance and the output conductance of the former. This error – often represented through the parameter ε_g is referred to as the finite output-input conductance ratio error [37].

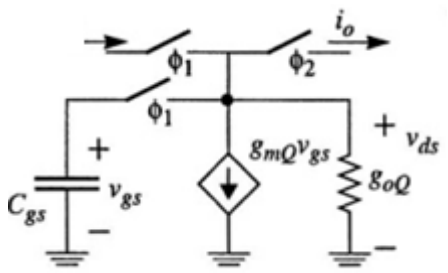
3.3.1 Linear analysis:

Let us consider the simple second-generation memory cell shown in Fig. 3.3(a). Assuming that the memory switches are ideal and that the amplitude of the input signal, i_i is small as compared to the bias current source I_{bias}, the memory cell can be modelled by its small signal equivalent circuit, shown in Fig. 3.3(b). In this circuit, C_{gs} is the gate-source capacitance of the memory transistor M; C_{dg} is the drain-gate overlap capacitance; g_{mQ} is the small-signal trans-conductance of the memory transistor (evaluated at the operating point), given by

$$g_{mQ} = \left.\frac{\partial i_{ds}}{\partial v_{gs}}\right|_Q \cong \sqrt{\frac{2\varepsilon_{ox}\mu_o}{t_{ox}}\frac{W_M}{L_M} I_{bias}} = \sqrt{2\beta_M I_{bias}} \tag{3.7}$$



(a) (b)



(c)

Fig. 3.3: Linear model for the memory cell with finite out-input conductance error. (a) Simple Second generation memory cell. (b) Small signal equivalent circuit. (c) Simplified equivalent circuit including g_{oQ}

And g_{dsnQ} and g_{dspQ} are respectively the drain-source conductances of the memory transistor and the bias source transistor at the operating point, given by:

$$g_{dsnQ} \equiv \left.\frac{\partial i_{ds_M}}{\partial v_{ds_M}}\right|_Q \cong \lambda_n I_{bias} \tag{3.8}$$

$$g_{dspQ} \equiv \left.\frac{\partial i_{ds_B}}{\partial v_{ds_B}}\right|_Q \cong \lambda_p I_{bias} \tag{3.9}$$

where λ_n and λ_p are respectively the channel length modulation parameter for the memory transistor and the bias source transistor, M_B. The circuit in Fig. 3.3(b) includes both mechanisms responsible for the error in the memory transistor drain current due to the variation of the drain-source voltage between two clock phases. Observe that this circuit can be simplified into that shown in Fig. 3.3(c) where g_{oQ} represents the equivalent output conductance of the memory cell given by

$$g_{oQ} = g_{dsnQ} + g_{dspQ} + \frac{g_{mQ}C_{dg}}{c_{dg} + c_{gs}} \tag{3.10}$$

Eq. (3.4) contains both the static and the dynamic parts of the output conductance. Observe that, while the static one is always present, the dynamic one appears only during the transitions between two clock phases.

3.3.2 Non-linear analysis

Practical SI circuits operate at signal amplitudes close to the bias current level I_{bias} in order to maximize the dynamic range. In such cases, the linear model fails to predict the real behaviour of the memory cell. To overcome this problem it will be necessary to employ a large signal model. Let us consider again the memory cell of Fig. 3.3(a). For the following analysis, it will be assumed that both the memory and the bias transistors can be described by the hand-analysis model of the MOS transistor in the saturation region, i.e,

$$i_{ds} = \frac{w}{2L}\mu_0 C_{0x}(v_{gs} - V_T)^2(1+\lambda v_{ds}) \tag{3.11}$$

Where i_{ds},v_{ds} and v_{gs} are respectively the drain-source current, the drain-source and the gate-source voltages of the MOS transistor; *W* and *L* are respectively the channel width and length; μ0 the carrier mobility in the channel; C_{ox} is the gate oxide capacitance per unit area and V_T is the threshold voltage. The only second order effect included is the channel length modulation modeled by λ [44].

From Eq. (3.2), Eq.(3.3) and Eq.(3.10) it can be derived that

$$g_m = \left.\frac{\partial i_{ds}}{\partial v_{gs}}\right|_{Qi} \cong \sqrt{2\beta i_{ds}|_{Qi}} \tag{3.12}$$

$$g_{ds} = \left.\frac{\partial i_{ds}}{\partial v_{ds}}\right|_{Qi} \cong \lambda i_{ds}|_{Qi} \tag{3.13}$$

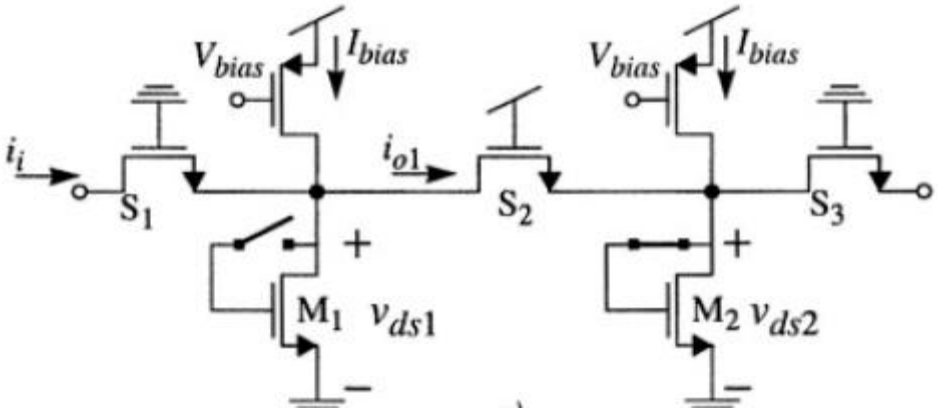
Where $\beta=h_p$ W/L and $i_{ds}/_{Qi}$ denotes that i_{ds} is evaluated at the operating point corresponding to the input signal amplitude I_i. In practice, that operating point will depend on the input signal amplitude and may change significantly between two periods of the clock signal.

3.4 Effect of the Finite Steering Switch-On Resistance:

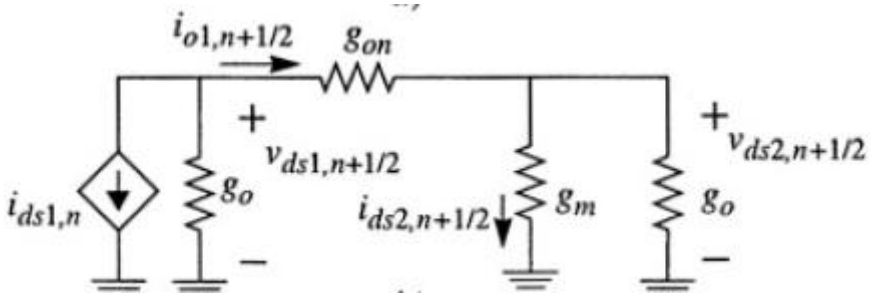
In SI circuits we can differentiate between two types of switches: memory and steering switches. The first ones realize the connection of the input node to the memory transistor gate. They do not carry currents in the steady state, and thus do not contribute to the error caused by the finite output-input ratio error. Their main non-ideal effect is that caused by their channel charge injected on the memory transistor gate capacitance during the transition between the sampling phase and the hold phase. The second type of switches drive stationary currents in the connection between two memory cells. As they are usually biased in the ohmic region of the MOS transistor, their main non-ideal effect is the finite switch on resistance. This section is devoted to analyzing the impact of this error on the performance of SI memory cells. For our analysis, we will consider that the steering switches are NMOS transistors. A similar analysis can be carried out for the case of either PMOS or CMOS switches.

Fig. 3.4(a) shows the connection of two memory cells during the clock phase (of period $(n+1/2)\ T_s$) in which the information is transmitted from one cell to another. Note that, during this phase, the steering switches named S_1 and S_3 are switched off while switch S_2 is switched on. As the gate node of S_2 is connected to the upper supply voltage, this switch is operating in the ohmic region. Assuming that the input signal amplitude is small as compared to the bias current, we can substitute the circuit in Fig. 3.4(a) by its small-signal equivalent circuit; this is shown in Fig. 3.5(b). Note that S_1 and S_3 have been replaced with open circuits while S_2 is modeled by a linear drain-source conductance represented by g_{on}. Solving that circuit for $i_{01,\,n}$ yields:

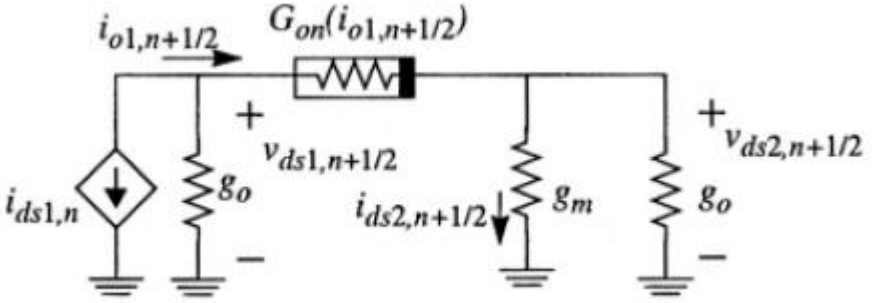
$$i_{o1,n} = \frac{-i_{i,n-1/2}}{1+\frac{g_0}{g_m}+\frac{g_0}{g_{0n}}\left[1+\frac{g_0+g_{0n}}{g_m}\right]} \tag{3.14}$$



(a)



(b)



(c)

Fig.3.4: Transmission error caused by steering switch-on resistance (a) Connection of two memory cells. (b) Equivalent circuit for linear switch-on resistance. (c) Equivalent circuit for non-linear switch-on resistance.

Assuming that $g_0/g_m << 1$ and $g_0/g_{0n} << 1$ the above expression simplifies into:

$$i_{o1,n} \cong \frac{-i_{i,n-1/2}}{\left(1+\frac{2g_0}{g_m}\right)\left(1+\frac{g_0}{g_{on}}+\frac{2g_0}{g_m}\right)} \cong -(1-\in_g -\in_{g_{on}})i_{i,n-1/2} \quad (3.15)$$

Where $\varepsilon_{g_{on}} = g_o/g_{on}$ represents the linear error due to the finite steering switch-on resistance.

3.5 Charge Injection Error:

When a MOS transistor switch is turned on, a quantity of charge is stored in its channel. When the switch is turns off, the charge is injected into its surrounding circuit nodes. In addition to the charge from the intrinsic channel, the charge associated with the feedthrough effect of the gate overlap capacitance also adds to the charge injection effect [45].The switch charge injection creates an error voltage in the gate of the memory transistor of the SI memory cell as shown in Fig. 3.5(a). The analysis of switch charge injection is quite complicated.

When the memory switch is closed (sampling mode), the drain of the memory transistor is connected to its gate thus charging the gate-source capacitance to a voltage capable of conducting the input current. When the memory switch is open, the gate of the memory transistor remains isolated and ideally the gate source voltage is held at the same value as that reached at the end of the sampling phase.

In practice, the memory switch is implemented by a MOS transistor. Fig. 3.5(a) shows a memory cell in which the memory switch is implemented by an NMOS transistor, M_s. Its gate is connected to the clock phase signal Φ_1 and its drain and source are connected to the drain and gate of the memory transistor, respectively. Clock signal Φ_1 periodically switches between a high voltage, V_H normally close or equal to the higher supply voltage and a low voltage V_L close or equal to the lower supply voltage. Therefore, M_s switches between the ohmic region for $\Phi_1 = V_H$ and the cut-off region for $\Phi_1 = V_L$. Because of the switching, its channel inversion layer is periodically created

during the sampling phase ($\Phi_1 = V_H$) and destroyed during the hold phase ($\Phi_1 = V_L$) as illustrated in Fig. 3.5(b).

During the turn-off transient, the channel mobile charges of M_s flow out of its drain, substrate, and source (Fig. 3.5(c)). Thus, part of this charge is dumped on the memory transistor gate-source capacitance (the source of M_s). In addition, the fast changing of the gate voltage causes the channel charge to flow through the gate diffusion overlap capacitances into both the source and drain of M_s. These two phenomena cause a variation on the memory gate-source voltage, and consequently an error in the memorized drain current. This non-ideal effect is known as a charge injection or clock feedthrough error and is often represented in the SI context by then parameter ξ_q[37,46]. From its detection, at the early stage of SC circuit development[47,48,49], there have been many attempts to analyze and model this error [50,51,52,] and a large number of circuit strategies have been proposed to attenuate it[53,54,55,56,57].

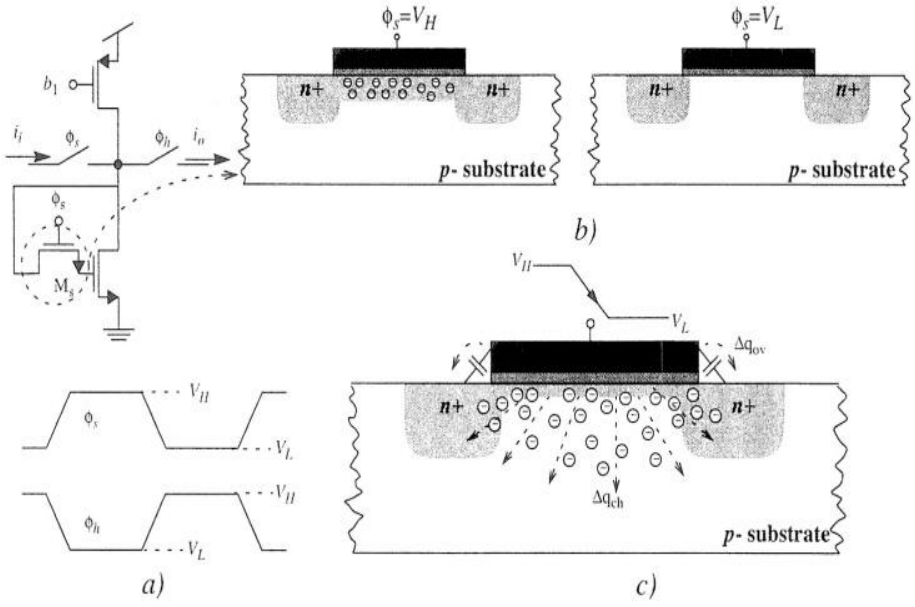


Fig. 3.5: The charge injection error mechanism. (a) Simple memory cell (b) Regions of operation of M_s. (c) Turn-off transient of Φ_1.

Fig. 3.9 shows a circuit which is used for switch charge injection analysis. Capacitance C_s is the lumped capacitance at the data holding node. The resistance R_s is the output resistance of the signal source, and C_s is the lumped capacitance associated

with signal source output capacitance. A numerical solution [24] shows that charge injected into the data holding capacitor C_L depends on the ratio of the capacitors, C_s/C_L and on the value of channel charge parameter B given by

$$B = (V_H - V_{li})\sqrt{\beta / UC_l} \tag{3.16}$$

Where $V_{li} = V_l + V_{in}$ and U is the falling rate dV/dt of the switching clock.

(1) When switch turn off time is much smaller than the time constant R_s C_s, the channel charge is shared between C_s and C_L. It is independent of the ratio of C_s/C_L.

(2) When the switch turn off time is much larger than the time constant, the majority of channel charge goes to the node with large capacitance. The charge splits according to the ratio of C_s/C_L.

(3) When the switch turn off time is comparable to the time constant, the charge sharing depends on the value of B.

(4) When ratio C_s/C_L =1, the channel charge is shared equally regardless of the value of B.

The switch charge injection error causes an error in the output current of a SI memory cell. Fig 3.6 illustrates the error current caused by the switch charge injection error δV. The drain current $I_d^{'}$ contains three parts: a dc current J, an ideal signal current *i*, and an error current i_e. The dc current J is given by

$$J = \frac{\beta}{2}(V_{GS} - V_T)^2 \tag{3.17}$$

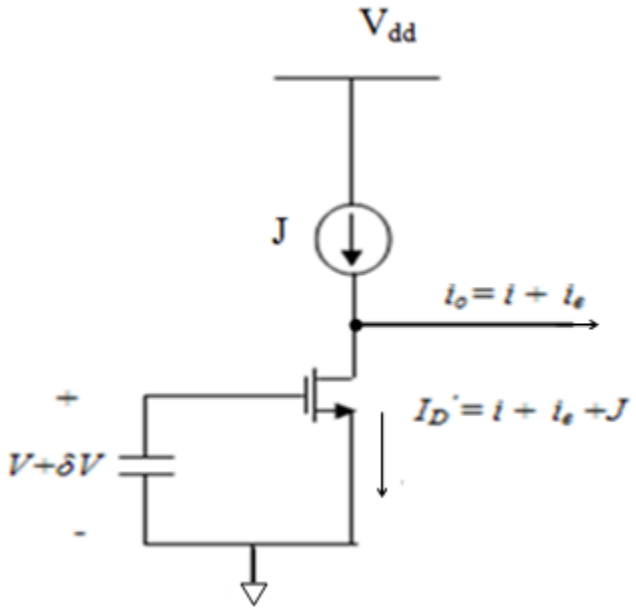


Fig. 3.6: Memory Cell With charge Injection.

Where $\beta=h_p(W/L)$ and V_T is the threshold voltage. In ideal case, the drain current is given by

$$I_D = \frac{\beta}{2}(V_{GS} - v_{gs} + \delta V) \tag{3.18}$$

By considering the switch charge injection error voltage δV, the drain current of the memory transistor is given by

$$I_D^{'} = J + i + i_e = \frac{\beta}{2}(V_{GS} + V_{gs} - V_T + \delta V)^2 \tag{3.19}$$

By comparing the ideal and non-ideal cases, we have

$$\frac{I_D^{'}}{I_D} = \left(\frac{V_{GS} + V_{gs} - V_T + \delta V}{V_{GS} + V_{gs} - V_T}\right)$$
$$= 1 + \frac{2\delta V}{V_{GS} + V_{gs} - V_T} + \frac{\delta V^2}{V_{GS} + V_{gs} - V_T} \tag{3.20}$$

From Eq. (3.17) and (3.18) we have

$$\frac{1}{V_{GS}+V_{gs}-V_T}=\frac{1}{V_{GS}-V_T}\sqrt{\frac{J}{J+i}} \tag{3.21}$$

3.6 Settling Error:

The operation of the SI memory cell involves charging of its gate capacitor to the gate voltage of a diode connected memory transistor. If the charging is not completed during the sample period in which switches S_1 and S_2 are closed, a residual error voltage results. At the end of the sample period, the switches S_1 and S_2 are opened, the error voltage is stored in the gate capacitor and results an output current error as illustrated in Fig.3.7. Where g_m is the signal source output conductance, g_0 is the memory cell output conductance, and R_1 and R_2 are the closure resistance of the switches S_1 and S_2 respectively.

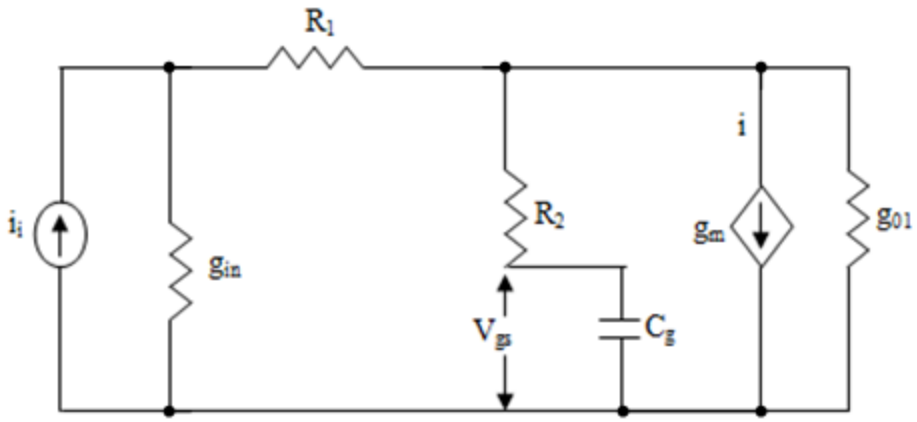


Fig. 3.7: (a) Equivalent circuit of the simple SI memory cell with switches S_1 and S_2 closed, S_3 opened.

In practical circuit, g_{in} and g_0 are very small than g_m. The resistance R_1 and R_2 can also be ignored. Therefore, the s-domain transfer function of the circuit is simplly given by

$$\frac{i_o(s)}{i_{in}(s)}=\frac{1}{s\tau+1} \tag{3.22}$$

Where τ is the time constant and it is approximately equal to C_g/g_m. This time constant causes a non-zero settling time error described by

$$i = i_{in}\left(1 - e^{\frac{-1}{\tau}}\right) \tag{3.23}$$

For low frequency application, the effect of non-zero settling time error is not significant. However, for high frequency application, non-zero settling time error causes current distortion [25].

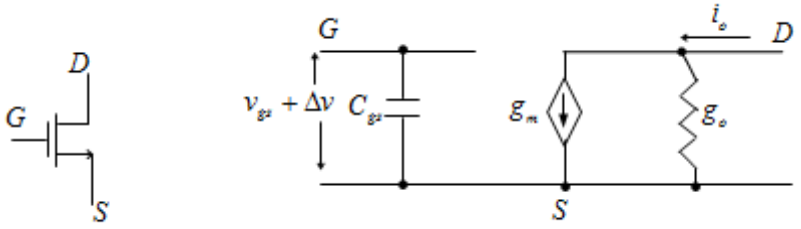


Fig. 3.8: (b) Equivalent circuit of the simple SI memory cell with switches S_1 and S_2 opened, S_3 closed.

3.7 Process Mismatches Between the current Mirror Transistors:

When a scaled output current is required, a current mirror circuit is used. The process mismatch between current mirror transistors produces scaled output current errors. The mismatches between transistors could be in threshold voltage V_t, the device aspect ratio W/L, the process gain factor K_p, or in the channel length modulation parameters λ. Most process mismatches result only in the current gain error in a SI memory cell, but threshold voltage mismatch causes dc error, current gain error, and harmonic distortion. The threshold voltage mismatch between the mirror transistors creates an error voltage ΔV_t as shown in Fig. 3.9. Thus, the effect of the ΔV_t is the same as that of the charge injection error voltage.

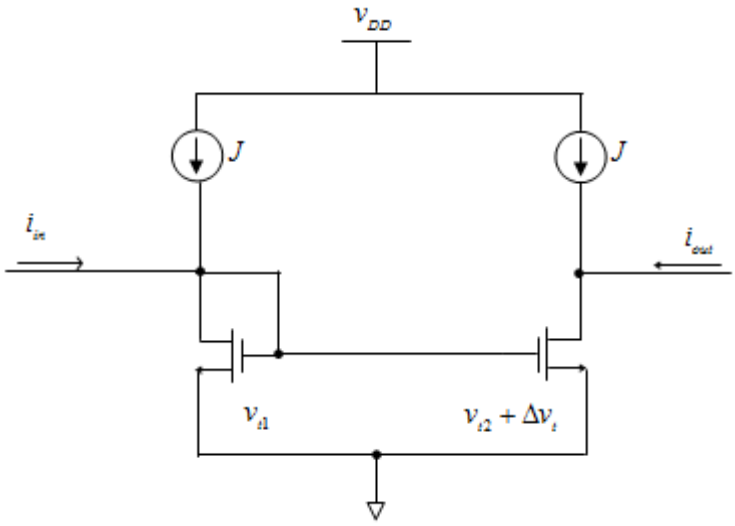


Fig. 3.9: An illustration of the effect of the threshold voltage mismatch

Summary:

The effect of non-ideal characteristics of the MOS device in the second generation memory cell has been analyzed. From the analysis, it is seen that the performance of the simple SI memory cell is strongly dependent on the characteristics of the MOS transistor used in the cell. Since a SI memory cell is the key building block of a SI circuit, the non-ideal MOS transistors can significantly affect the performance of the performance of the SI circuits. Because of the non-ideal characteristics of the MOS transistors, the simple SI memory cell can produces unacceptable large amount of errors. To reduce the effect of non-ideal MOS devices, we need to improve the performance of SI memory.

Conclusion & Suggestion

4.1 Conclusion:

The role of traditional analog circuits has changed from a main signal processor to an interface between a DSP system and the outside analog world. Thus, in their new role, they must be made to acquire all the characteristics needed for them to co-exist with the dominant digital environment. The performance of analog circuits has to be matched with that of digital circuits and they have to be implemented using a process technology that has been optimized for the implementation of digital circuits.

The SI technique is a possible solution to make the analog circuits matched with the digital circuits both in performance and implementation process technology. The Switched Current techniques are finding an increasingly greater role in the design and implementation of analog circuits, since they don't require linear capacitors and are capable to work with low power supplies. Since linear capacitors are not required, a SI integrated circuit is not dependent on special analog process technology and it is fully compatible with the digital process technology. In SI circuits, lowering the power supply voltage will not reduce its dynamic range or signal-to- ratio. However, the non-ideal characteristics of MOS transistor affect the performance of the SI circuits significantly, and have made use of the SI circuits still less attractive in comparison with SC circuits. This work has been concerned with applications of switched current circuit design for signal processing taking into consideration the effects of non-ideal characteristics of MOS transistor. To reduce the effects of non-ideal characteristics of MOS transistor, a high performance differential SI memory cell design has to be used.

4.2 Scope for Future Investigation:

The future requirements of the analog interface circuits in a DSP system could be those of lower cost, higher operating speed, higher bandwidth, greater operating dynamic range and further decrease in power supply voltage.

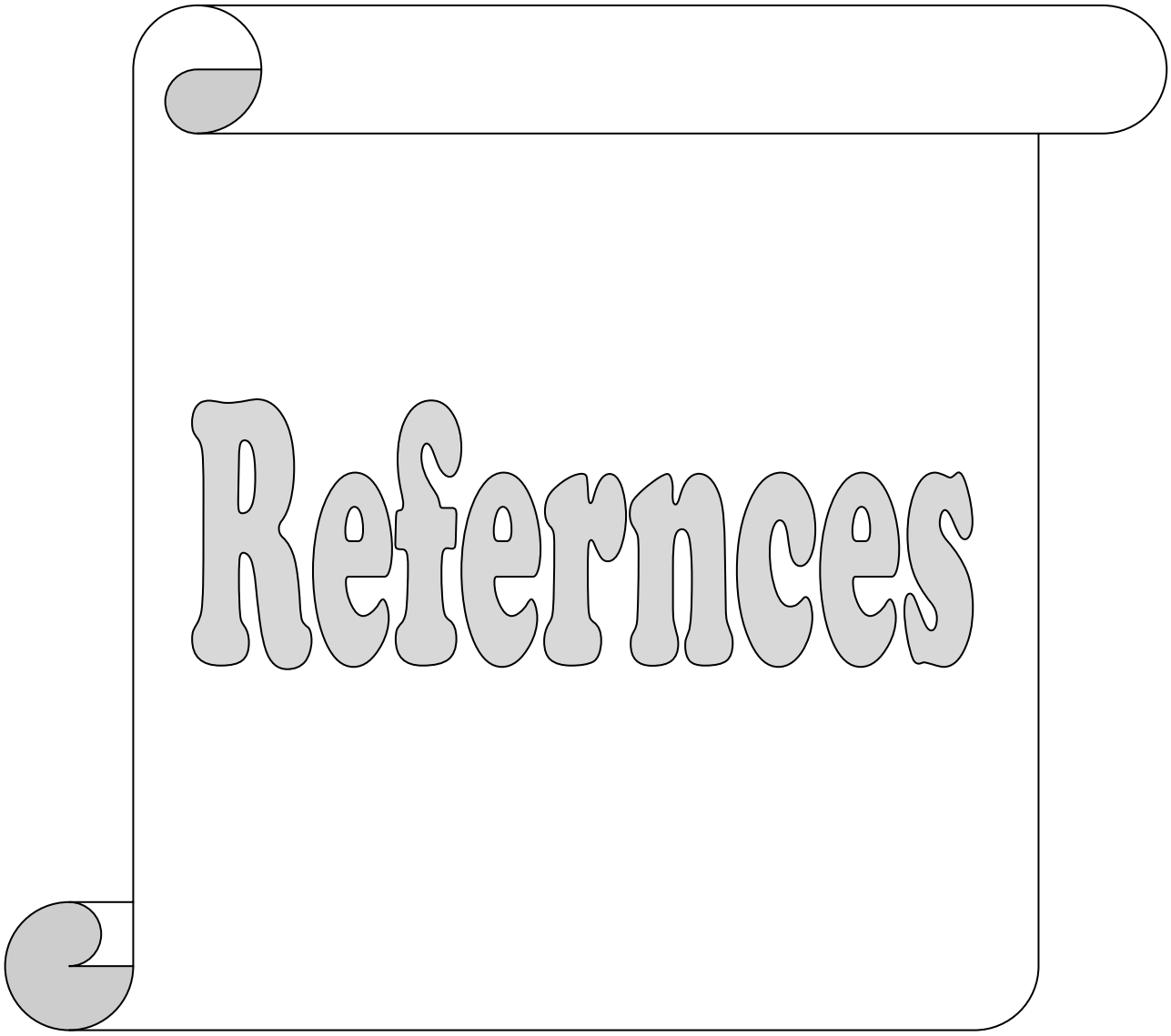
By changing the size ratios (W/L) of the coefficient transistors, different frequency characteristics of the filters can be obtained, this is important feature of SI circuits, with help of this SI circuits can be programmed for different filter responses.

The process technology presently used for the SI circuits is the same as those used for digital circuits. However, future decrease in the cost of analog circuits would heavily rely on our capability to develop new analog design techniques that are compatible with emerging new digital process technologies.

The present SI circuits cannot be used in high frequency applications processing. In order for this to happen, the SI design technique has to be developed to be compatible with the sub-micron process technology for increasing the frequency bandwidth of the MOS transistors.

The present SI circuits cannot operate with supply voltage lower than 1V.The industry has proposed lowering of the supply voltage lower than 1V for the next generation digital VLSI/ULSI circuits. Therefore, for the next generation DSP systems, SI technique ought to be evolved to provide non-degraded performance at low power supply voltage.

Further the MOS transistors can be replaced by other structures in order to have best possible results.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