

## Charge transport through In-pSi (100) Schottky barrier

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**Abstract** Schottky barrier devices on p-type silicon were fabricated using indium as contacting metal. Barrier heights and ideality factors of the prepared devices were evaluated by analyzing the V-I data at room temperature. The results have been discussed for the type of charge transport. They have also been compared with expected values on some basic models for SBHs.

**Keywords** : Schottky barrier, saturation current, barrier height, ideality factor

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Even after investigations spreading over more than a century, Schottky devices still elude a clear understanding of the mechanisms and their exact contribution in the over all observed barrier heights. It is known that observed barrier heights are a result of band line up and accompanying charge transfers across the interface. As a result, barrier heights should correspond to that predicted by Mott Schottky model [1]. But observed deviations from the above predictions and the scatter in the reported experimental barrier heights have led to the proposition that more than one single mechanism may be making contribution to the experimentally obtained value. Some influencing factors of these mechanisms [2], found after a critical examination and evaluation of the observed data regarding barrier heights of such contacts, are: (a) intrinsic surface states and metal induced gap states (b) defects, impurities and chemical mismatch at the interface (c) crystallography, epitaxy and orientations at the interface *etc.* Presence of spatial inhomogeneities at the interface giving rise to lateral distribution in barrier heights have been proposed as a reason for difference between the observed and the expected values [2]. In this note, we report our work on characterisation of charge transport, ideality factor and barrier height of indium Schottky diode on p-type silicon(100).

In this work, silicon crystal of resistivity around one ohm cm. and acceptor density around  $10^{16} \text{ cm}^{-3}$  have been used to

fabricate In-pSi Schottky diodes. The crystal was first etched in 4:1:3 solution of  $\text{HNO}_3$ , HF and  $\text{CH}_3\text{COOH}$ , [3] to remove silicon dioxide and impurities. After thorough washing in distilled water, it was quickly dried and loaded in the vacuum system. A thick aluminium coating of  $3000 \text{ \AA}$  was made on the rough side of the crystal by evaporation and it was heated around  $500^\circ\text{C}$  in the coating unit itself in vacuum for nearly 30 minutes to make ohmic back contact. The polished surface was again etched in the same solution for ~30 sec. After thorough washing and quick drying, it was loaded in a vacuum system to evaporate pure indium through a suitable mask. This evaporation was done in a vacuum of around  $10^{-6}$  torr to obtain indium deposition of area  $0.089 \text{ cm}^2$ . The crystal with deposited diodes was mounted on a PCB and suitable contacts were made to connect the diode using coiled silver wire and silver paste (Eltecks Corporation, Bangalore). This was connected to an arrangement for obtaining V-I characteristics at 305 K, 288K and 273 K using a voltage source and Keithley electrometer. The temperature variation was done using a cryostat.

The V-I characteristics at all the three temperatures are found to exhibit good rectifying nature. A representative V-I plot at 305 K is shown in Figure 1. The V-I characteristics of the Schottky diodes is representative of the charge transport across the interface. In general, the charge transport across Schottky barriers may belong fully or partly to one or more of the thermionic emission (TE), thermionic field emission (TFE) or pure field

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emission [tunneling (FE)] mechanisms [4]. However, under forward bias condition, tunneling in Schottky diodes made from nondegenerate semiconductors, as in present case, is ruled out. This leaves thermionic and thermionic field emission as the

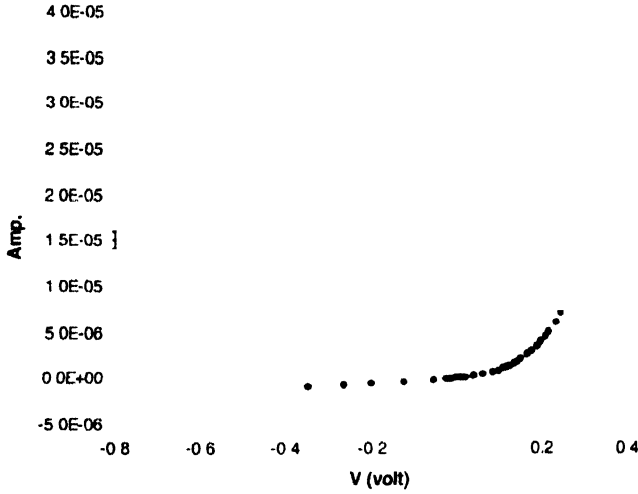


Figure 1. I-V characteristics of In-pSi Schottky contact at 305 K.

possible charge transport mechanisms. A distinction between these two mechanisms can be made with the help of the characteristic energy parameter  $E_{00}$  defined as,

$$E_{00} = \left( \frac{q\hbar}{2} \right) \left[ \frac{N_A}{m^* \epsilon_s} \right]^{\frac{1}{2}} \tag{1}$$

Here,  $\hbar (= h/2\pi)$  is the reduced Plank constant,  $m^*$  is the effective mass of the charge carriers and  $\epsilon_s$  is the permittivity of the semiconductor. If  $E_{00} \approx kT$ , then thermionic field emission is expected to be the dominant charge transport mechanism and when  $E_{00} \ll kT$  thermionic emission is expected to be the dominant charge transport mechanism at the temperatures of measurement. In present case, with  $N_A \sim 10^{16} \text{ cm}^{-3}$ ,  $E_{00}$  comes out to be lower by more than an order of magnitude from  $kT$ . Thus in the present case, the thermionic emission is expected to be the dominant mechanism of charge transport across the interface. Therefore, the observed V-I characteristic should follow the equation,

$$I_F = I_0 \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right], \tag{2}$$

with,  $I_0 = AA * T^2 \exp \left( -\frac{q\phi_b}{kT} \right)$

Here,  $I_0$  is the saturation current, A is the area of diode,  $A^*$  is the Richardson constant and  $\Phi_b$  is the barrier height. However, chemically-etched practical Schottky diodes are generally known to exhibit voltage-dependent barrier heights and in such cases, the I-V characteristic are expected to follow the equation,

$$I_F = I_0 \exp \left( \frac{qV}{nkT} \right) \left[ 1 - \exp \left( -\frac{qV}{kT} \right) \right]. \tag{3}$$

Here,  $n$  is the ideality factor. Using eq. (3), the barrier heights in the present case have been evaluated from saturation currents obtained by plotting variation of function  $\ln \left[ I_f / \left[ 1 - \exp(-qV/kT) \right] \right]$  with forward bias. Such a plot for  $T = 305\text{K}$  is given in Figure 2. The ideality factor  $n$  is evaluated by using the equation,

$$n = \left( \frac{q}{kT} \right) \left[ dV / d(\ln I) \right]. \tag{4}$$

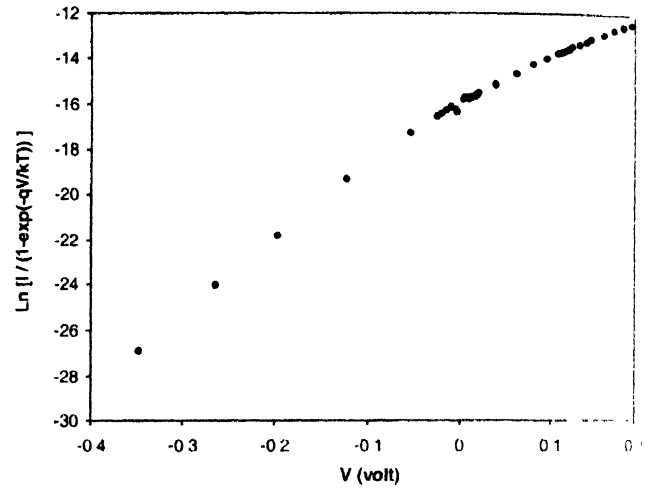


Figure 2.  $\ln [ I / (1 - \exp(-qV/kT)) ]$  vs  $V$  characteristics of In-pSi Schottky contact at 305 K

The results of above kind of analysis at the three temperatures are given in Table 1. The results given in Table 1 show that the value of ideality factor is around 1.2 to 1.3.

Table 1. Barrier height and ideality factor for In pSi(100) Schottky diode at various temperatures (diode area= 0.089cm<sup>2</sup>)

Temperature (K)	Barrier height $\Phi_b$ (eV)	Ideality factor $n$
305	0.75	1.17
288	0.73	1.20
273	0.71	1.29

The higher values of  $n$  is related to the interfacial effects, most likely from the presence of oxide layer where interfacial states in equilibrium with the semiconductor may be dominant. Most probable reason for the presence of oxide layer at the interface may be insufficient etching of the face on which indium was evaporated or growth of oxide at this face in the time elapsing between etching and deposition of indium. It also indicates that the Schottky diodes might have deviated from the thermionic-emission theory and that other current transport processes may also be contributing to the total observed charge transport [5,6].

In order to evaluate the contribution of the tunneling transport of charges, we have made a quantitative estimate of the relative importance of the thermionic emission current and the tunneling current for the material used in the present study. As discussed earlier,  $E_{00}$  calculated from eq. (1) comes out to be lower by more than an order of magnitude from  $kT$ . Therefore, the influence of the tunneling current is insignificant in the I-V measurement of this Schottky diode.

The leakage current may in general, have some influence on the I-V characteristics of Schottky diodes. But in our case, shunt conductance is estimated to be  $10^{-7}$  mho and thus, the leakage current should not have significant influence on saturation currents and hence on barrier heights.

The recombination current in the depletion region, has been reported to be an important factor responsible for the deviation of the I-V characteristics from the behaviour described by the thermionic emission theory [6]. The recombination of the electrons and holes normally takes place through localized centers with energies which are near the center of the band gap and it is expected in Schottky diodes with high barriers, at low temperature, and at low forward-bias voltage [4,7]. However, in present measurements, the temperatures are not low and  $\Phi_b$  is also not very high. Therefore, the recombination current contribution also seems to be insignificant. Hence, in the case of present study, the thermionic emission seems to be the

dominant charge transport mechanism and the higher value of  $n$  is probably related to interfacial oxide layer.

The barrier height value obtained in present work, is around 0.71 to 0.75 eV and it neither agrees with the expected on M-S model (1.03 eV) nor with Bardeen model (0.36 eV). The values expected on MIGS model is 0.6 eV. Moreover, the reported values of barrier height for In-pSi Schottky diode is around 0.75 eV [8]. Our value is near this value. Therefore, it indicates that interfacial conditions might be making significant contribution to band line up in present Schottky devices. However, a more clear view requires more precise measurements over larger temperature ranges.

#### References

- [1] S M Sze *Physics of Semiconductor Devices*, (2nd edn) (New York: Wiley Eastern) (1993)
- [2] J H Werner and U Rau *Schottky Contacts on Silicon* (Springer Series in Electronics and Photonics) (eds ) L J Luy and P Russier Vol. 32 ( Berlin: Springer Verlag) p 89 (1994)
- [3] S M Sze *VLSI Technology* (New York: McGraw- Hill) (1998)
- [4] E H Rhoderick and R H Williams *Metal Semiconductor Contacts* ( Oxford: Clarendon Press) (1988)
- [5] D Donoval, M Barus and M Zdimal *Solid State Electron* **34** 1365 (1991)
- [6] M Wittmer *Phys Rev* **B42** 5249 (1990)
- [7] A Y C Yu and E H Snow *J Appl Phys* **39** 3008 (1968)
- [8] M Hirose, N Altaf and T Arizumi *Jpn J Appl Phys* **9(3)** 260 (1970)