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Investigation on porous silicon/CdTe system

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Abstract : CdTe layer was electro-chemically deposited over porous silicon layer formed by standard anodization process. The PL spectrum shows no change in peak position (630 nm) or the line shape (FWHM = 140 nm) but the intensity is increased by a factor of two. FTIR studies of the porous silicon surface before and after CdTe deposition shows that the Si-H bonds formed during anodization are replaced to a large extent by S O and Si OH bridges. Pore filling by CdTe revealed no major changes in the I-V and C-V characteristics except a small decrease in barrier capacitance

Keywords : Porous silicon, CdTe electrodeposition, I-V measurement, C-V measurement

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1. Introduction

Since the discovery of efficient room temperature visible photoluminescence of porous silicon by Canham [1], porous silicon has attracted a lot of attention for optoelectronic, electronic and sensor applications. Porous silicon (PS) can thus be viewed as a new material of interest for future microelectronic applications. Made from the anodic dissolution of Si in HF electrolyte, the important feature is that the material with more than 50% porosity remains a single crystal. Recent emphasis has been on the utilization of the large surface area offered by porous material. Extensive efforts have been made to incorporate other materials into the nanopores of porous silicon for fabrication of nanocomposite materials [2] and sensors [3]. Electrodeposition is known to covers the inner surfaces of porous materials and the pores can be completely filled. Embedded in a high resistivity Si-skeleton, semiconducting nanowires/nanotubes can be formed [4].

Deposition of various metals *e.g.* Al, Au, In, Ni, Cu *etc.* were investigated for making ohmic contacts and diode structure fabrication [5,6]. It is assumed that wet chemical processes like electrodeposition introduce damage to the porous silicon surface, although pore filling is very effective, Cu electrodeposition is reported to quench both PL and EL [7]. Several studies on semiconductor incorporation into the pores were made. Montes *et al* [8] have shown that CdTe can be deposited over porous silicon using acidic electrolyte, however the photoluminescence was quenched after deposition and sample drying. In the present investigation the porous silicon / CdTe structure prepared by electrodepositing CdTe over porous silicon were further investigated by photoluminescence and FTIR. *I-V* characteristics and capacitance voltage measurements on Au/PS/Si structure and Au/CdTe/PS/Si structure were obtained and compared. Results obtained from *I-V* curves showed nonlinear behavior in both cases. The *C-V* characteristics in both cases are similar to that of metal-insulator-semiconductor structure and are modelled accordingly, assuming that air gaps existing in porous silicon are filled by CdTe monocrystals in CdTe/PS sample.

2. Experimental

Mechanically polished boron doped (100) oriented p-type silicon wafers were used for preparing porous silicon. Aluminium was vacuum evaporated and annealed at 680°C for 10 min in flowing argon, to form good ohmic contact on the back side. Anodization was carried out at a current density of 80 mA cm^{-2}, for 5 min, in an electrolyte, consisting of a 2 : 1 mixture of HF and H_2O_2. After the anodization, the films were washed in ethanol and finally in deionized water and dried in air. The porosity of the PS layer so obtained was about 70%. To fill the pores, CdTe films were electro-deposited over porous silicon substrates using the acidic aqueous solution. Composition of the electrolytic bath was 2.5 M Cd^{2+}, 120 ppm ($HTeO_2$) + pH = 1.6. Standard calomel electrode was used as reference and deposition was carried out at –0.58 V for 30 min. The solution was stirred and kept at a temperature of

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80°C during deposition. CdTe electrodeposition conditions were optimized through initial cyclic voltammetry studies on Si and SnO_2 coated glass substrates. At the optimum deposition potential conditions CdTe layer was deposited on porous silicon substrate.

After CdTe deposition the samples were washed with deionized water, then with ethanol and left to dry. PL measurements were recorded using a system consisting of a two stage monochromator, a PMT with lock in amplifier for PL detection and an Ar ion laser operating at 488 nm for excitation. All measurements were carried out with a laser power of 10 mW. The Fourier transform infrared (FTIR) absorption spectra on the PS layer and the PS/CdTe structure were recorded by a spectrometer in the range 400–4000 nm. The current voltage characteristics were measured with the help of a pico-ammeter and constant voltage source and the C-V measurements with an impedance bridge at 1 M Hz.

3. Results

3.1. Photoluminescence :

PS is considered as a material which consists of Si nanocrystallites and has a larger band gap (1.9–2 eV) than c-Si due to the quantum confinement effect. This is sometimes referred to as quantum confined Si (Qc-Si). The surface of as formed porous silicon is covered with Si-H (1-3) and Si-O-H bonds. Generally, the photoluminescence is attributed to the direct gap nature of quantum confined Si nano crystallites. However, formation of a thin a-Si : O : H layer with a band gap of 2.5 eV is also claimed to be responsible.

Figure 1 shows the PL spectrum of a porous sample before and after CdTe deposition. A broad photoluminescence peak centered around 630 nm was observed in porous silicon sample. The large FWHM of ~ 120 nm may be associated with the inhomogeneous distribution of the nanopores or wires and the complex nature of surface states present at the large internal surface of the PS.

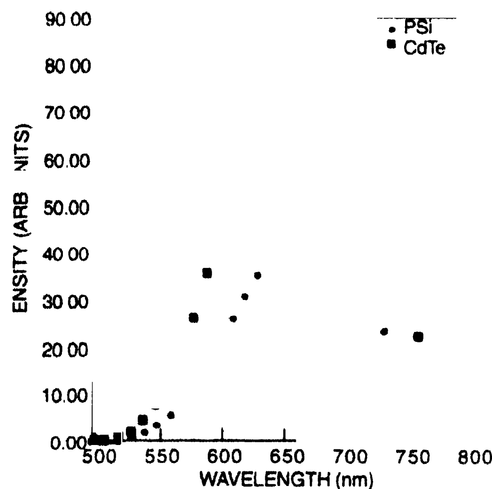

Figure 1. Photoluminescence for porous silicon layer as formed and pore filled by CdTe.

After depositing CdTe on the porous silicon sample the photoluminescence intensity was increased by a factor of two. However no appreciable spectral shift is observed. Increased intensity was previously observed by depositing CdS/ZnS layers over PS and is explained as due to reduction in the non-radiative recombination centers, due to the formation of interface between PS and nanoparticles of CdS/ZnS [9]. In the present case the nanopores of PS have been filled by CdTe instead of CdS/ZnS. Since an electrodeposition in aqueous solution was used to deposit CdTe, similar explanation may be assumed for PL intensity enhancement *i.e.* OH species may be helping in forming new interface states which act as radiative recombination centres.

The present results are in contrast to the results by Montes *et al* [8], who showed a decreased photoluminescence in CdTe layer after drying. However their results on electroless CdTe showed no such PL quenching even after air drying and was attributed to PS oxidation *via* the corrosion mechanism, which passivates the surface. Formation of oxide layers during chemical and electrochemical deposition of metals has also been observed by others [6]. In the present investigations CdTe was deposited over PS samples in an aqueous medium, and were stored in air for a long duration before measurement. This may also contribute to passivation.

3.2. FTIR measurements :

FTIR spectra of the as prepared PS layer and after CdTe pore filling are shown in Figure 2. Deposition of CdTe in the pores caused a major change in FTIR pattern. The IR absorption peaks around 2000 cm^{-1} have completely disappeared in CdTe coated sample. The doublet at 2115–2090 cm^{-1} has been identified as silicon monohydride and silicon dihydride stretches respectively. A sharp absorption near 910 cm^{-1} and a strong absorption in 630–680 cm^{-1} range are reported to be due to Si-H$_x$ species. The peak at 623.49 cm^{-1} is due to Si-H bending in Si$_3$SiH. In case of CdTe deposited PS sample intensity of all hydride related peaks are absent or intensity is suppressed. Absence of

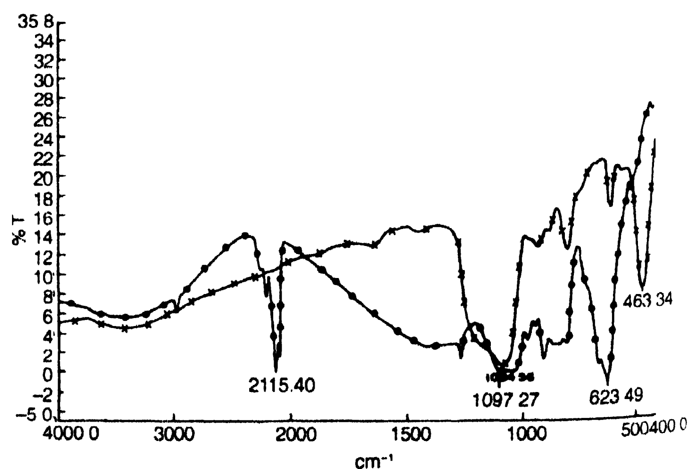

Figure 2. FTIR measurements for porous silicon layer as formed (•) and pores filled by CdTe (*).

hydrogen related peaks means Si-H bonds have been replaced by other bonds in CdTe impregnated sample. Oxygen related stretching modes (SiO in O-SiO and C-SiO) are found in the 1056–1160 cm^{-1} range. A broad peak observed around 1097 cm^{-1} in unfilled PS sample is still present after CdTe coating but a slight shift towards higher wavelength side is observed (1094.56 cm^{-1}) and intensity is enhanced. Presence of oxygen related stretching modes even in as deposited sample is due to the oxygen adsorption. This peak is more intense in the CdTe filled sample. CdTe electrodeposition was performed in aqueous media and as discussed above, intensity of the Si-H lines has decreased. Other peaks due to Si-O bonds at 668 and 630 cm^{-1} have overlapped in PS sample with bulk Si-Si stretch mode at 616 cm^{-1}. Thus a peak at 623 cm^{-1} is observed in PS sample.

3.3. I-V and C-V measurements :

I-V characteristic of the PS is shown in Figure 3(a). The heterostructure shows rectifying behavior. The forward current is several orders of magnitude higher than the reverse current. The rectification ratio at 1 V is about 200 for PS at room temperature. The reverse current does not appear to be saturating but shows voltage dependence, indicating carrier transport through the hetero-structure. The log $I*V^{-1/2}$ *vs* $1/V$ curve (Fowler-Nordheim plot) curve is shown in Figure 3 (b), this curve clearly shows two different slopes, one in the region 0 to 0.5 V and the other at higher voltage, The slope in 1st region is 2.8 which changes to 4.2 in the second region. In case of CdTe impregnated sample, a similar non linear *I-V* relationship is observed. The rectification ratio is however 100 at 1V and the slope changes at a voltage of 0.2. V. The slope in the lower voltage region is higher (about 3.6) and changes to 2.4 in the higher voltage region. The *C-V* plots were obtained for both the samples. These are shown in Figure 4. No hysteresis was observed in either case.

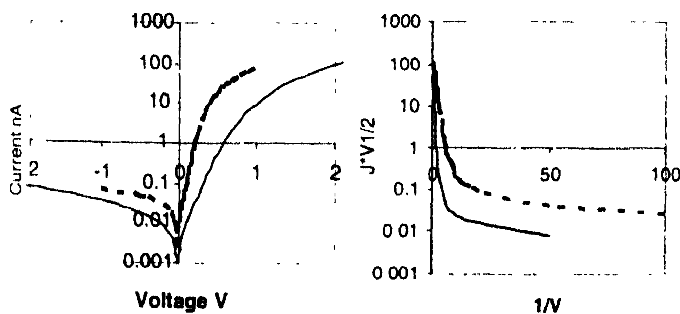

Figure 3. (a) *I-V* and (b) $I*V^{-1/2}$ *vs* $1/V$ curve for Au/PS/Si (--) and Au/CdTe/PS/Si (- - -).

The *I-V* plots are similar to earlier reported results on PS samples [10,11]. The power law behavior with a high exponential factor indicates space charge limited current in the presence of traps. It is surprising that similar results are obtained even after CdTe deposition. Normally electrodeposited CdTe is highly insulating and a change in the conduction process would be expected. It is possible that the porous silicon surface on which electrodeposited CdTe layer is formed is itself highly insulating. Due to this high insulating surface of porous silicon, the Au/PS junction itself behaved as MIS structure. Thus the non linear *I-V* behaviour is strongly controlled by the presence of Si : O : H bond configurations on the porous silicon surface. This is further confirmed by capacitance-voltage measurement shown in Figure 4. *C-V* curves for both samples can be explained in terms of MIS (metal-insulator-semiconductor) structure. With the change in voltage the semiconductor goes from an accumulation to depletion region. The increase in the current in *I-V* curve and a decrease in the capacitance in *C-V* curve both can be explained with the formation of a leaky insulator layer in between the Au and PS. The Si-O and Si-OH bonds formed on the porous silicon surface can be responsible for this behavior. However an increase in the current in *I-V* curve and a small decrease in the capacitance in *C-V* curve both indicate that CdTe filling have decreased the resistance.

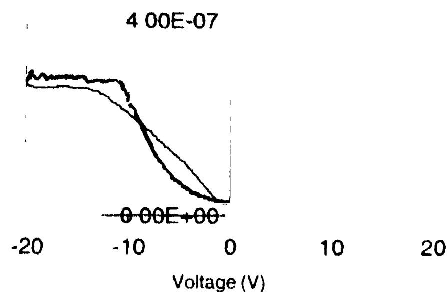

Figure 4. Capacitance *vs* voltage Au/PS/Si (-) and Au/CdTe/PS/Si (- - -)

4. Conclusion

CdTe layer was electro-chemically deposited over porous silicon layer formed by standard anodization process. The PL spectrum shows no change in peak position or the line shape but the intensity is increased by a factor of two. FTIR studies of the porous silicon surface before and after CdTe deposition shows that the Si-H bonds formed during anodization are replaced to a large extent by S-O and Si-OH bridges. I-V studies indicated the formation of a rectifying junction. Both Au-PS as well as Au-CdTe-PS junctions behaved as MIS structure.

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