Aerosol-Jet Printed Interconnects for 2.5 D Electronic and Photonic Integration

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***Abstract*—We demonstrate a flexible face-up 2.5 D packaging technique for a hybrid electro-photonic integration. The process is based on an aerosol-jet technology to print the high-speed electrical interconnects between electronic and photonic chips as a potential alternative for the traditional bonding wires. The technology is realized by creating a transparent mechanical polymer support to bridge the gap between the photonic and electronic chips and subsequently printing the electrical interconnects on top. First, the daisy-chain test chips were used to prove the functionality of the technology by printing the electrical interconnects between the test chips. Then, a standard 85 ° C/85 RH test was performed to investigate the reliability of the printed interconnects and no failure or degradation was observed over 700 h. Afterwards, the technology was successfully applied on functional chips. An optical transmitter based on vertical cavity surface emitting lasers (VCSELs) was demonstrated at 50 Gb/s by printing 200-μm-long high-speed silver interconnects between a 4-channel SiGe BiCMOS driver and four VCSELs. In addition, the technology showed the potential to interconnect silicon photonics chips. An assembly of an electro-absorption modulator (EAM) and a CMOS driver was successfully demonstrated. Clear open eye diagrams were obtained at 40, 50, and 56 Gb/s for the EAM-driver assembly even after 2 km of a standard single-mode fiber.**

***Index Terms*—Aerosol-jet printing (AJP), electro-photonic integration, electrical interconnects, VCSEL, CMOS driver, electro-absorption modulator (EAM).**

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I. Introduction

HIGH speed electro-optical modules require low-parasitic and efficient packaging technologies to sustain the massive increase in data rates for optical links. The conventional packaging technologies for electro-photonic integration such as wire bonding techniques are reaching their limits, but are still widely being used because of their flexibility (in assembly) and proven reliability. Therefore, new integration and packaging techniques which not only sustain higher operating frequencies, but also maintain the flexibility in assembly and reliability are essential. Some reports are presented in which the wire bonding technology is replaced by a 3D stacking method [1], [2] via stacking the optoelectronic chips (vertical cavity surface emitting laser (VCSEL) or photodiode (PD) arrays) over the electronic chips (driver or transimpedance amplifier (TIA)). A flip-chip interconnection [3] was developed for an electro-absorption modulator integrated with a distributed feedback (EADFB) laser array transmitter. A 12-channel optical transmitter and receiver subassembly was recently demonstrated at 10 Gb/s based on wet etched silicon interposer [4]. Although flip-chip [5] in combination with through-silicon vias can be a good alternative at high frequency, the approach is much less flexible than wire bonding. Hence, there is a need for interconnecting chips with a higher degree of freedom, comparable to traditional wire bond technologies, but at the same time providing high frequency capabilities. Therefore, in this work we developed a process based on aerosol-jet printing (AJP) which flexibly integrates photonic and electronic chips at 50 Gb/s and beyond. To the best of our knowledge, this is the first time the AJP technology is used to integrate electronic and photonics chips.

Over the last decade, the aerosol-jet printing (AJP) has shown great potential in different research aspects. The AJP was used to print the front side metallization for silicon and organic solar cells [6], [7]. A thin-film transistor made using single-walled carbon nanotube was printed using AJP [8], [9]. Aerosol-jet printed sensors onto pre-packaged integrated circuits (IC's) were recently developed [10]. In addition, 3D multi-layer transmission lines were developed by stacking multiple layers of polyimide and silver using AJP [11], [12]. Furthermore, the AJP technology has already been reported to enable 3D printed electronics such as resistors, capacitors, and antennas, sensors [13]. AJP is an additive manufacturing technique which allows depositing features directly on planar and non-planar surfaces, with micrometer resolution, and can deposit an extremely wide

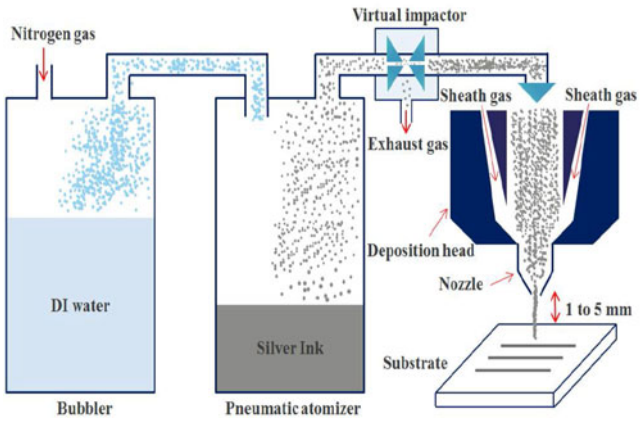


Fig. 1. The aerosol-jet printing setup.

range of materials, including metals and dielectrics, enabling co-planar transmission lines from "pad-to-pad" with the freedom to tune the characteristic impedance. This means that the dimensions (width & thickness) of the electrical interconnects can be tuned to achieve a desired characteristic impedance (e.g., 50 Ω to minimize signal reflections) or to obtain well-controlled parasitics (e.g., for bandwidth enhancement through inductive peaking), thus improving the transceiver performance.

II. Aerosol-Jet Printing Process

As a material for the electrical interconnects, we used a water-based silver nano-flakes ink from Novacentrix (Metalon HPS030 AE1). The ink has a viscosity of 187 cP and is mainly developed for using with the pneumatic atomizer (PA), which is well-suited for high viscosity inks. The aerosol-jet process is mainly based on creating an aerosol from a functional liquid ink by means of atomization, then transporting the aerosol to the deposition head and finally focusing the aerosol stream on the substrate by a nitrogen (N_2) flow. Fig. 1 shows the aerosol-jet printing setup. The silver ink is placed into the pneumatic atomizer in which the aerosol is generated. A bubbler containing DI water is added to the setup to compensate the loss of the most volatile solvent during the atomization process. Since water is the most volatile solvent in the used ink so the bubbler is filled with deionized (DI) water. In this case the nitrogen flow entering the PA is wetted with DI water. As a result, an aerosol of droplets between 1–5 μm in diameter is generated. Drops larger than about 5 microns cannot overcome the force of gravity and drop back into the ink and are recycled. Then, the aerosol is transported by the nitrogen stream to the deposition head. Before reaching the deposition head, the virtual impactor removes the excess air (exhaust gas) and increases the aerosol density. Within the deposition head, the aerosol is focused by a second N_2 flow called the sheath gas which surrounds the aerosol as an annular ring. The resulting high-velocity converging particle stream is deposited onto the substrate creating the very fine features. The aerosol stream exiting the nozzle remains focused over a working distance between 1–5 mm. This feature enables the 3D printing capability of the technology.

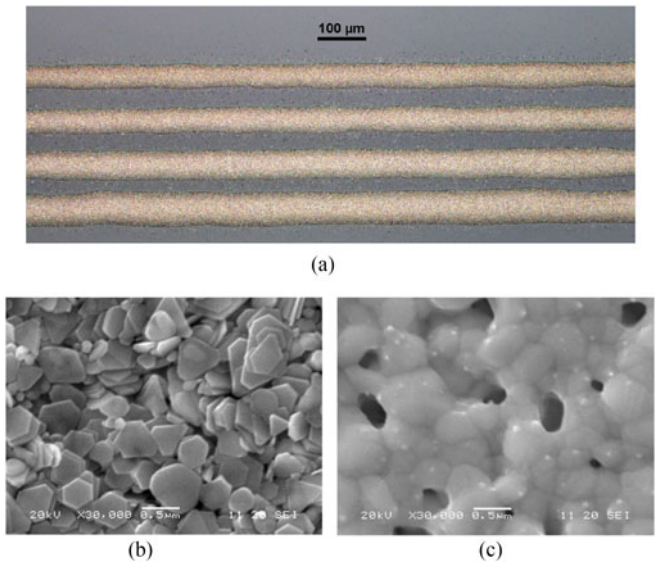


Fig. 2. (a) Aerosol-jet printed traces of different width (b) SEM micrograph of the trace before sintering (c) after sintering.

Fig. 2(a) shows pictures of the printed silver traces on a glass substrate. The printed silver traces were sintered in a convection oven at 200 °C for 2 hours in order to evaporate the solvents and reach the required conductivity for the electrical interconnects. Fig. 2(b) and (c) show scanning electron microscope (SEM) micrographs of the printed structures before and after sintering. Before sintering, the silver nano-flakes are shown as separate stacked particles and after the thermal sintering the flakes are welded together. The sheet resistance of the printed silver traces was found to be 0.025 Ω/square.

The aerosol-jet process requires control of some process parameters [14] in order to obtain uniform traces. These parameters include carrier gas flow, sheath flow, substrate temperature, nozzle diameter, working distance and printing speed. The influence of the process parameters was investigated for the used silver ink in order to have a good control over the dimensions of the printed traces. During the optimization process, the substrate was heated to 60 °C and the printing nozzle was about 3 mm above the substrate. The 200 μm-diameter nozzle was used during all the tests.

Fig. 3 shows the influence of the stage speed on the dimensions of the printed lines. Increasing the stage speed reduces both the line width and thickness. The dimensions are also influenced by the ratio between the sheath flow and the carrier flow which is called the focusing ratio.

$$\text{Focusing Ratio (FR)} = \frac{\text{Sheath flow rate}}{\text{Carrier flow rate}}$$

Where the carrier flow rate is the difference between the atomizer flow rate and the exhaust flow rate. Fig. 4 shows the effect of the focusing ratio on the line width and thickness. As the focusing ratio increases, the line width decreases while the thickness increases.

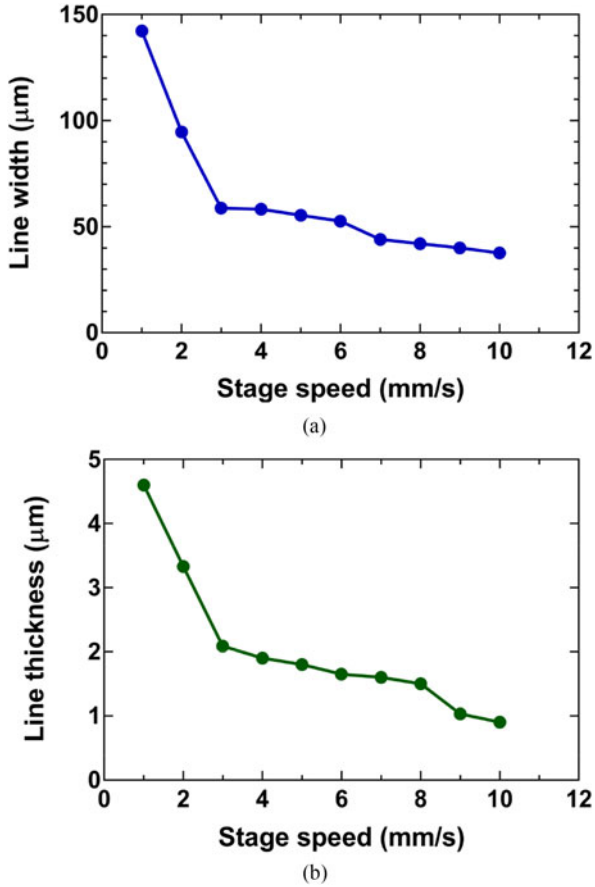


Fig. 3. The influence of the stage speed on (a) the line width (b) the line thickness.

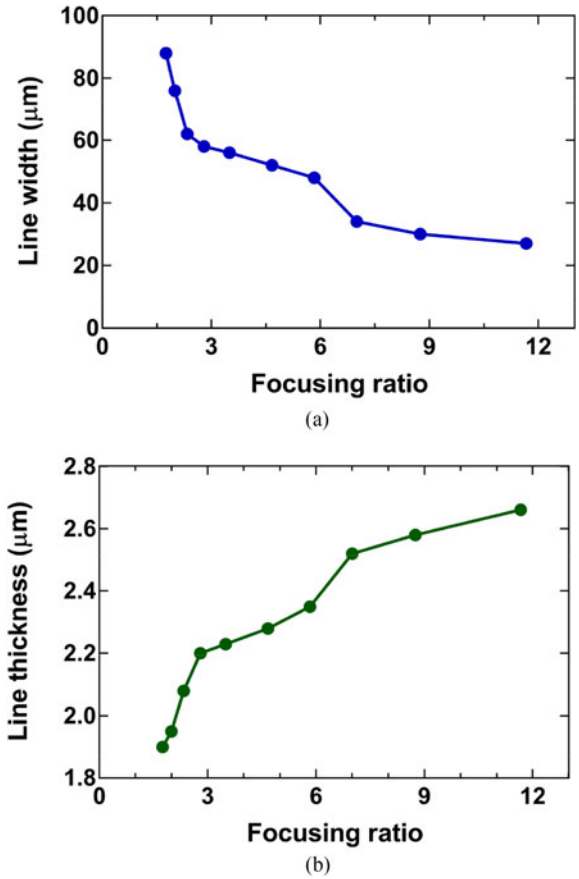


Fig. 4. The influence of the focusing ratio on (a) the line width and (b) the line thickness.

III. Experimental Process Flow

The complete process flow is shown in Fig. 5. It can be summarized in 3 main steps; (i) creating a mechanical polymer support by covering the gap between the photonic and electronic chips, (ii) opening the contact pads, and (iii) aerosol-jet printing of silver interconnects between the chips. First, the chips were die-bonded to the PCB followed by an epoxy polymer dispensing (Epotek OG 142-112). The epoxy was locally dispensed on the chips by a fine needle. Next, a flat PDMS stamp (residing on glass substrate) was gently pressed onto the dispensed epoxy. Then, the epoxy was cured using a UV lamp at 30 mW/cm^2 for 2 minutes. The stamp was released after UV exposure since the epoxy does not adhere to PDMS. The thickness of the epoxy layer on top of the chips is less than 10 μm. Hence vias can be easily opened on the contact pads by excimer laser ablation. At last the electrical interconnects were precisely printed between the chips (pad-to-pad) using aerosol-jet printing. In order to ensure that the vias were completely filled, two printing passes at least (5 μm per pass) were applied to connect between the chips. The epoxy covering the electronic and photonic chips is required to be transparent so that it would have no negative effect on the coupling efficiency of the light in or out of the photonic chips.

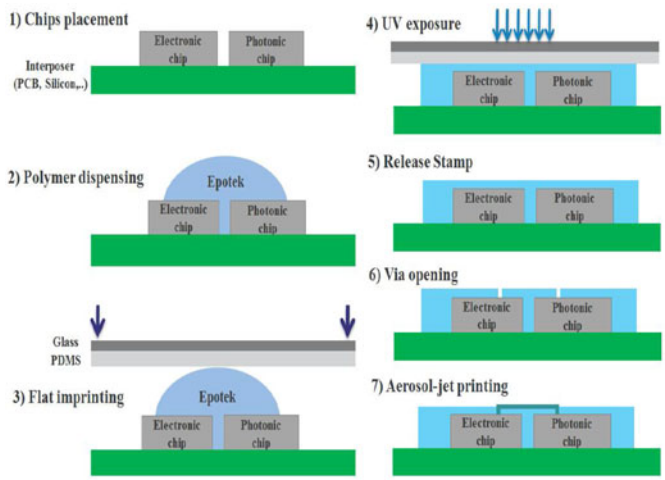
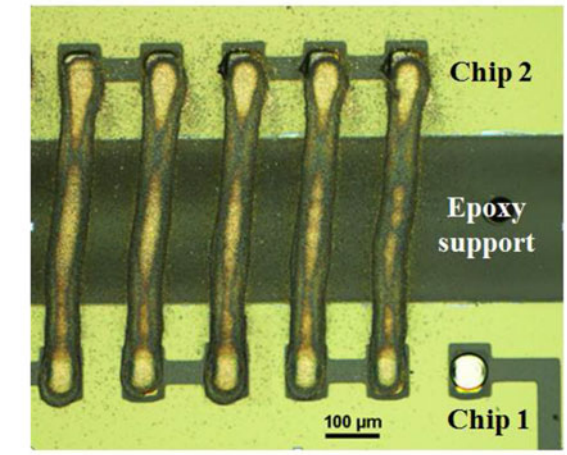


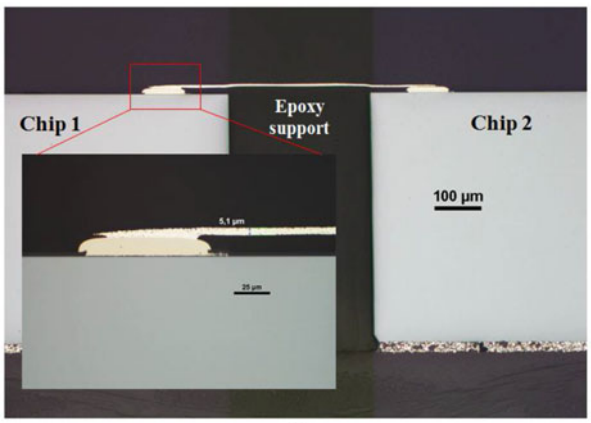
Fig. 5. The fabrication process flow.

IV. Interconnection Between Daisy-Chain Test Chips

The functionality of the technology was first proven on test chips (daisy chain). The interconnection between the two daisy-chain chips was successfully printed and tested. The resulting printed interconnects have a width of about 50 μm and thickness of 5 μm per pass. The total length of the aerosol-jet printed



(a)



(b)

Fig. 6. The aerosol-jet printed daisy chain interconnects between the test chips (a) top view (b) cross-section view.

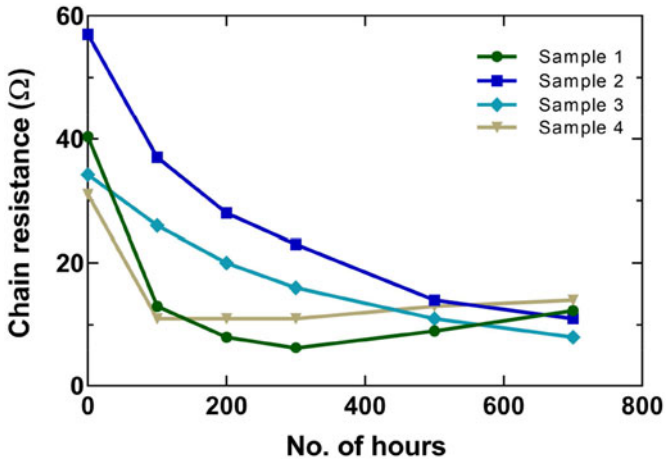


Fig. 7. The effect of performing 85 °C/85 RH reliability test for 700 hours on the daisy-chain resistance.

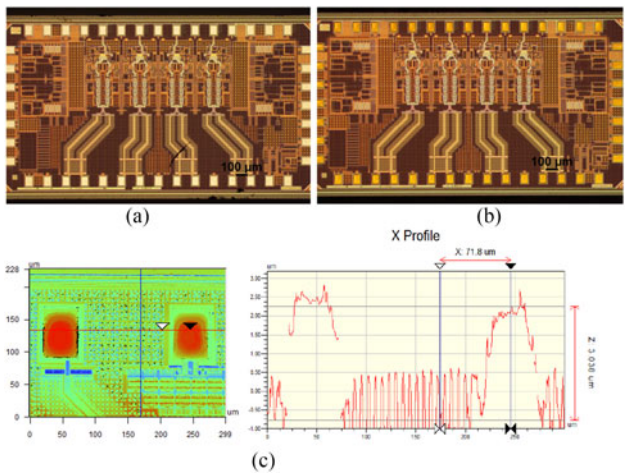


Fig. 8. (a) the SiGe BiCMOS driver IC before NiAu plating (b) the SiGe BiCMOS driver IC after NiAu plating (c) optical profiler measurements of the plated NiAu bumps.

tracks for the complete daisy-chain was about 7.5 mm and 30 vias were opened. The printed tracks have a resistance of around 6 Ω/mm. Fig. 6 shows pictures of the top view for the connection between the test chips and the cross-section view from pad-to-pad. Moreover, the printed interconnects showed no failure even after running 85 °C/85 RH tests for 700 hours. Afterwards, the test was stopped since no failure was observed. The reliability test was performed for 4 different daisy-chain links and the complete daisy-chain resistance was measured every 100 hours as illustrated in Fig. 4. Due to the fact that there is a polymer covering the chips, the sintering temperature for the sample was decreased from 210 °C to 150 °C to avoid any excessive difference in thermal expansion during heating due to CTE mismatch of the different materials. This means that the printed interconnects did not reach the maximum possible conductivity and hence the 85 °C temperature of the test gradually contributed to evaporate the remaining solvents and increasingly joins the silver flakes in the printed traces. Therefore, the resistance was decreasing during the first 500 hours of the reliability test as shown in the graph until it stabilizes roughly after 500 hours.

V. VCSEL Transmitter Assembly

After proving the basic technology on test chips, an optical transmitter was successfully developed as the first demonstrator to the technology. The optical transmitter consists of a 4-channel driver and 4 single-mode VCSELs. The VCSELs emit at a wavelength of 1550 nm with a small signal bandwidth around 22 GHz. These VCSELs were developed by the Technical University of Munich (TUM) [15]. We observed from the first experiments that the contact resistance between the printed silver interconnects and the Aluminum finished contact pads of the driver was relatively high [16]. In addition, the probing with the RF probe on the Al contact pads was not repeatable. This issue was overcome by plating NiAu bumps on the Al contact pads of the chip. Fig. 8 shows pictures of the driver chip before and after Ni-Au plating. The thickness of the Ni-Au bumps was around 3 μm as obtained from the optical profiler measurements shown in Fig. 8(c). The VCSELs have gold contact pads and therefore did not require adding NiAu bumps. The driver was

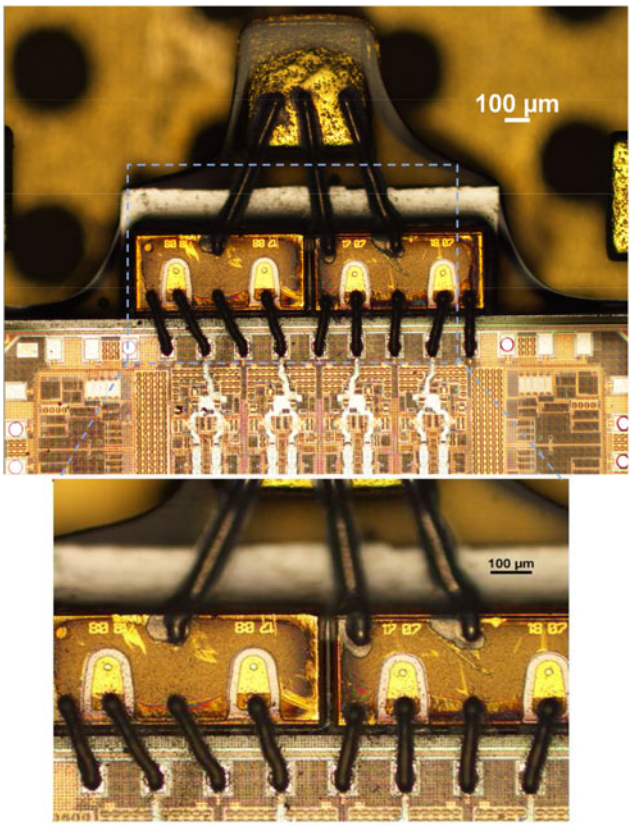


Fig. 9. The assembly of the 4-channel driver IC and 4 single-mode VCSELs.

fabricated in a 0.13 μm SiGe BiCMOS process [17] and can directly modulate a 4 common-anode VCSELs. Since the driver chip has a thickness of 375 μm and the VCSEL is 75-μm thick, the VCSELs were mounted on a silicon interposer with a thickness of 300 μm in order to obtain the same height for all chips. Then, the chips were glued to the PCB using a non-conductive adhesive and decoupling capacitors were glued to the PCB using electrically conductive adhesive. Next, the chips were covered with the transparent epoxy and vias were opened on the contact pads using the process described above.

Finally, the high-speed interconnects were printed from the driver to the VCSEL and also from the VCSELs anode to the decoupling capacitor as shown in Fig. 9. The distance between the driver and the VCSELs were kept as short as possible by mounting the chips very close to each other to minimize the parasitics. This enabled making the interconnects from the driver to the VCSELs as short as 200 μm. The aerosol-jet printed interconnects have a width of 40 μm, a thickness of 15 μm and a length of 200 μm. The other interconnects for providing the supply voltage for the driver chip were wire-bonded to speed up the process as the electrical DC connections have no effect on the high-speed performance of the assembly. However, a complete printed assembly is feasible if a ramp is created at the chip edges. In this case the interconnects would be printed up till the traces on the printed circuit board (PCB). The VCSELs were biased at an average current of 8.7 mA for all the experiments. The light is coupled out of the VCSELs using lensed fibers. The measured optical eye-diagrams at 50 Gb/s for 3 channels

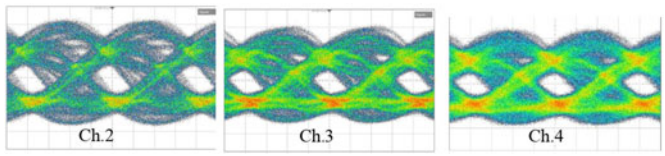


Fig. 10. The measured back to back eye diagram at 50 Gb/s for 3 channels.

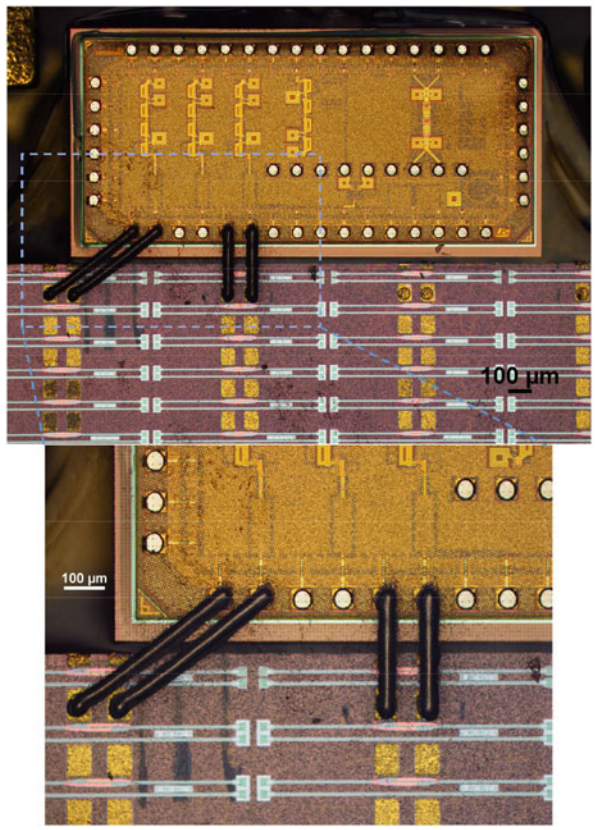


Fig. 11. The assembly of the EAM modulator and CMOS driver interconnected by aerosol-jet printing.

are shown in Fig. 10. The 4th VCSEL was damaged during the testing process.

VI. CMOS Driver and Electro-Absorption Modulator (EAM) Assembly

Next, we extended our interconnection technology to include silicon photonic chips. Imec's silicon photonics platform [18] was selected which includes high-speed EAMs among many other devices. The driver chip was fabricated in a 28 nm fully depleted silicon-on-insulator (FDSOI) CMOS process [19]. Since the driver and the modulator chips have Al contact pads, they were electro-plated with NiAu bumps for the same reason as discussed above. Since the driver chip has a thickness of 250 μm and the modulator is 500 μm-thick, the modulator chip was thinned-down to 250 μm to achieve the same height as the driver chip. The modulator, driver and decoupling capacitors were die-bonded to the PCB using electrically conductive adhesive. The high speed interconnects were realized using the same printing process as described above. The printed interconnects

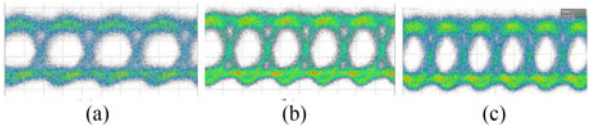


Fig. 12. The measured back to back eye diagrams (a) 40 Gb/s, (b) 50 Gb/s, and (c) 56 Gb/s.

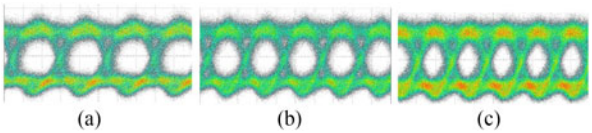


Fig. 13. The measured eye diagrams after 1 km of fiber (a) 40 Gb/s, (b) 50 Gb/s, and (c) 56 Gb/s.

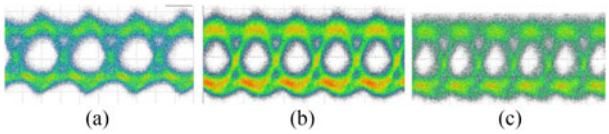


Fig. 14. The measured eye diagrams after 2 km of fiber (a) 40 Gb/s, (b) 50 Gb/s, and (c) 56 Gb/s.

have a width of 45 μm, a thickness of 15 μm and a length of 300 μm. Fig. 11 shows the resulting assembly of the EAM modulator and the driver. The light is coupled into and out of the EAM modulator by two grating couplers at 1560 nm. Fig. 12 shows the measured back to back optical eye-diagrams at 40 Gb/s, 50 Gb/s and 56 Gb/s. The eyes are clearly open even after transmission distances of 1 km and 2 km standard single-mode fiber as illustrated in Figs. 13 and 14. An extinction ratio (ER) of 2.83 dB was achieved while applying a drive voltage of 1 V_{pp}. The driver uses an RC bias tee to reverse-bias the EAM to -0.8 V. The resulting ER is close to the value obtained in [18].

VII. Conclusion

In this paper, we presented a 2.5 D interconnection method for electro-photonic integration. The method is based on developing electrical interconnects using aerosol-jet printing (AJP) technology. Silver electrical interconnects were precisely printed from pad-to-pad after creating a polymeric mechanical support between the electronics and photonic chips. The technology was first proven on daisy-chain test chips. The printed interconnects showed no failure or degradation even after performing a standard 85 °C/85 RH test over 700 hours. Afterwards, a 4-channel VCSEL transmitter was successfully demonstrated at 50 Gb/s. Moreover, an assembly of a silicon photonic EAM and a CMOS driver was developed and eye diagrams were obtained at 40 Gb/s, 50 Gb/s and 56 Gb/s. The eye diagrams were clearly open even after 2 km of standard single-mode fiber.

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