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Physical mechanism of progressive breakdown in gate oxides

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The definition of the basic physical mechanisms of the dielectric breakdown (BD) phenomenon is still an open area of research. In particular, in advanced complementary metal-oxide-semiconductor (CMOS) circuits, the BD of gate dielectrics occurs in the regime of relatively low voltage and very high electric field; this is of enormous technological importance, and thus widely investigated but still not well understood. Such BD is characterized by a gradual, progressive growth of the gate leakage through a localized BD spot. In this paper, we report for the first time experimental data and a model which provide understanding of the main physical mechanism responsible for the progressive BD growth. We demonstrate the ability to control the breakdown growth rate of a number of gate dielectrics and provide a physical model of the observed behavior, allowing to considerably improve the reliability margins of CMOS circuits by choosing a correct combination of voltage, thickness, and thermal conductivity of the gate dielectric. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4882116>]

I. INTRODUCTION

The studies on dielectric breakdown (BD) belong to a long record of major advancements in science and technology. Though the progress in this field has been impressive, the BD phenomenon taking place when voltage differences of the order of 1 V are applied to short distances, of the order of nanometers, i.e., with very large electric fields but insufficient energy to produce either impact-ionization, or plasmonic loss, H release, or other quantum effects, is still not well understood. Nevertheless, this is a major area for the progress of nanotechnology. For example, the reliability of ultrathin gate dielectrics is a crucial issue for the scaling of transistors of very large scale integrated (VLSI) circuits realized in complementary metal-oxide-semiconductor (CMOS) technology. Ultra-thin gate oxides exhibit a gradual loss of their insulating properties when a breakdown path is generated by a high voltage stress. In CMOS circuits, at their operation voltages, this progressive BD (PBD) can be very slow with respect to the conditions of standard high voltage gate stack wear-out accelerated tests. Under operation conditions it may take many years to reach gate leakage levels large enough to appreciably disturb the circuit operation, improving thus the reliability margins of CMOS applications.^{1–3} Moreover, a new area of application of the BD in thin dielectrics is the resistive switching phenomenon,^{4,5} of large interest for the realization of new generations of ultra-scaled low power non-volatile semiconductor memories.

Despite the success to predict the statistics,^{6,7} the conduction,^{8,9} and the micro-structural damage within the transistor structures during the progressive BD regime,^{3,10–12} all these phenomenological descriptions do not reveal the fundamental physical mechanism that drives the progressive increase of the current after the initial BD event. One of the

major features of the rate of increase of the BD current is that it is characterized by a strong voltage dependence at low voltages.^{1,3,9} Such an effect, initially observed only in Poly-Si/SiO_xN_y/Si MOS systems, was later found to occur also in Si CMOS gate stacks with metal gate and high permittivity (high-K)³ dielectric. It is therefore most likely a general physical phenomenon taking place in dielectric breakdown at relatively low voltages.

At high voltages, the BD transients are extremely fast. In the case of Poly-Si/SiO_xN_y/Si MOS stacks, it was shown that there is a voltage threshold at about 4.5 V above which the dynamics of the BD growth changes abruptly, with BD growth rates above $1 \times 10^{+6}$ A/s.¹³ At a lower voltage, the BD growth rate becomes many orders of magnitude lower. In this regime, the dissipated power is below ≈ 1 mW; by using three-dimensional heat flow simulations it has been shown that the BD cannot produce complete melting in the BD spot region. This is consistent with the onset of slow BD transients below the above mentioned voltage threshold.¹⁴

The initial works on poly-Si/SiO_xN_y/Si gate stacks were later extended to the area of MOS stacks with metal gates and gate oxides such as SiO₂, SiO_xN_y, and/or high k dielectrics on Si substrates.^{3,15,16} On large area capacitor samples with tungsten metal gates on SiO₂ dielectrics during CVS (constant voltage stress) experiments, it was found that the PBD phase is observed only when the current level through the BD spot during the CVS is below 1–10 μ A,^{15–17} barely distinguishable from the background gate leakage current. When such a level of BD current is reached, a fast BD runaway takes place and the BD current suddenly jumps to the mA level. This is very different from the case of poly-Si/SiO_xN_y/Si gate stacks, where the PBD is seen even at current levels of the order of 100 μ A.¹ Later on, on small area silicon nFET samples with TiN metal gates on HfO₂ dielectrics with an ultra-thin interfacial SiO₂ layer, during

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CVS experiments the PBD phase was much more clearly manifested and studied since the background gate leakage current was smaller because of the smaller gate area and of the presence of the high- k dielectric.^{15,18} In any case, also in these systems when the BD current reached the 1–10 μA level, the PBD was overwhelmed by a fast BD runaway and the BD current suddenly jumps to the mA level. So the PBD phenomenology, though with differences in the various cases, appears to be a general effect in dielectrics stressed at large electric fields, at least in the case of samples with Si substrates.

In this paper, we show that the same type of PBD phenomenology is observed also in samples with InGaAs substrates with high- k dielectrics and metal gates. From this further observation, and considering that therefore the PBD phenomenology is found with different electrodes such as Poly-Si and metal, with different gate oxides such as SiO_2 , SiO_xN_y , or high- k dielectrics, and with different substrates such as Si or an InGaAs, we conclude that PBD is a very general physical effect. While the phenomenology is therefore quite well defined, and observed with many different materials, the understanding of what is the leading physical mechanism at low voltage causing the progressive BD growth is still lacking. To clarify such a mechanism, it is therefore particularly interesting to investigate the energy transfer mechanism from the BD path to its surroundings. To achieve this objective, the BD transients on different dielectric layers in MOS structures were compared to provide direct experimental information about the BD transient. The difference in the thermal properties of the dielectric layers should reveal the real impact of the thermal properties on the BD event. In this work, we demonstrate and model this aspect, providing for the first time a physical model of progressive BD.

II. EXPERIMENTAL

A number of MOS structures were fabricated with different dielectric layers: Al_2O_3 , Si_3N_4 and HfO_2 . In all cases, an n-type InGaAs substrate (epitaxially grown on InP wafers) and gate metallization of Ti(1 nm)/Au(200 nm) were used. The area of the devices was $1.1 \times 10^{-4} \text{ cm}^2$.

For the MOS structure with Al_2O_3 dielectric layer, a pre-dielectric deposition treatment (PDT) was performed by a NH_4OH solution, and then a 9 nm thick Al_2O_3 layer was prepared by atomic layer deposition (ALD) using trimethylaluminum (TMA) and H_2O precursors at 300°C . For the MOS structures with Si_3N_4 , the dielectric was deposited by plasma enhanced chemical vapor deposition (PECVD) with NH_3 pre-deposition treatments. For the MOS structures with HfO_2 , a PDT was performed and then a 10 nm HfO_2 layer was prepared by ALD. For all types of samples, post deposition annealing (PDA) at 400°C in vacuum (10^{-8} Torr) for 30 min was carried out. In all cases the oxide thicknesses were measured by ellipsometry and TEM microscopy. Further details about the samples can be found in our previous works, Refs. 19–21.

Regarding the electrical measurements, the capacitors were subjected to CVS where the gate current was measured as function of the time at different voltages using an Agilent

Parameter Analyzer 4155C with a resolution in time of some milliseconds. In all cases, the measurements were performed at room temperature (300 K), and the bias was applied on the gate with the other terminal (wafer's back contact) grounded. Further details about the measurements of the BD transient can be found in Refs. 1–3.

III. RESULTS AND DISCUSSION

Figure 1 shows a typical BD transient of gate current for metal gate (MG)/ Al_2O_3 /InGaAs stacks, taken without applying a current compliance limit on the gate current, and observed under a CVS. Each curve corresponds to a different stress voltage ranging from +5 V to +6 V. At least two distinctive phases can be observed in these curves. The first part, which is not a topic of this paper and was extensively studied in Ref. 19, is characterized by a decrease of the current due to negative charge trapping. Once the formation of one percolation path in the overall MOS capacitor sample is completed by generation of defects within the dielectric layer, the BD event takes place, and the gate current (I_G) changes trend and starts increasing.^{1,3,13} It is a noisy and progressive process well in agreement with those reported in the literature for the cases of HfO_2 ^{3,9,15} and SiO_2 .^{1–3,16} The duration of the progressive increase of the current shows a strong voltage dependence and reaches current levels of the order of 1–10 μA , where the gate current jumps abruptly to very high levels in times of the order of microseconds, i.e., limited by the bandwidth of the equipment (see Figure 1). It is worth to note that the current level where the gate current jumps abruptly is quite similar for all cases with different CVS voltages. Therefore, as reported in our previous work in Ref. 15, if the stress voltage or area is large enough to increase the background current above such a level, only a fast runaway will be observed. Figures 2 and 3 show some typical BD transients of gate currents for the MG/ HfO_2 (10 nm)/InGaAs and the MG/ Si_3N_4 (9 nm)/InGaAs MOS stacks, respectively.

It is widely accepted that the evolution of the progressive BD current may be quantified by the slope of the current

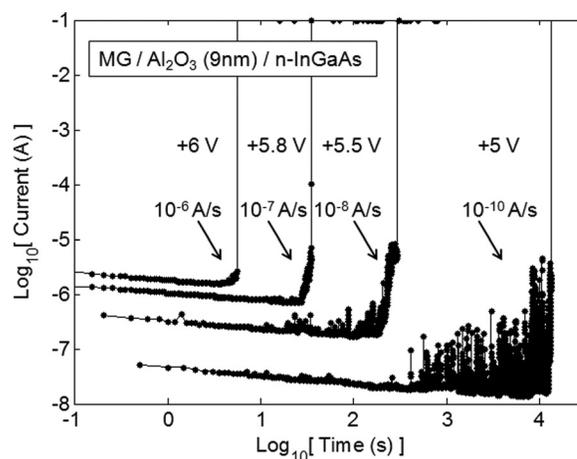


FIG. 1. Typical measurements of current as function of the time under constant voltage stress for the metal gate/ Al_2O_3 (9 nm)/n-InGaAs MOS stacks for constant voltage stress values ranging from +5 V to +6 V.

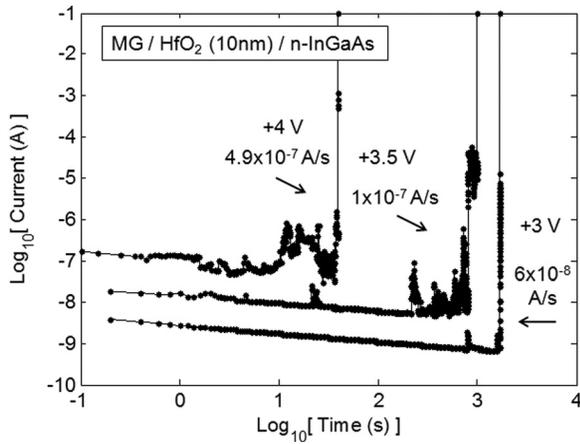


FIG. 2. Typical measurements of current as function of the time under constant voltage stress for the metal gate/HfO₂(10 nm)/n-InGaAs MOS stacks for constant voltage stress values ranging from +3 V to +4 V.

during the BD event (I_{BD}), i.e., dI_{BD}/dt , as defined in Ref. 1. Figure 4 shows the dI_{BD}/dt values for different MOS stacks, calculated in the range of 1 nA to 10 μ A (marked as “data”). The entire set of samples includes MOS capacitors with the same substrate (InGaAs), metal gate (Au/Ti), and oxide thickness, but different dielectrics: Al₂O₃(9nm), Si₃N₄(9nm), and HfO₂(10nm). It also includes experimental data of poly-Si/SiO_xN_y (2nm)/Si from Refs. 1 and 13 (marked as “Linder” or “Lombardo”, respectively). In the case of SiO_xN_y, the dI_{BD}/dt values at and above 10⁺² A/s of Ref. 13 are limited by the bandwidth of the experimental set-up. By using an experimental set-up with higher time resolution, it is shown that those data actually correspond to much faster BD transients.³ For this reason in Figure 4, the data at 10⁺² A/s from Ref. 13 are shifted to higher values ($\geq 1 \times 10^{+6}$ A/s).

Since the discussed effect is local, taking place only in the BD spot and not evenly distributed along the MOS area, it is important to note that gate area has no effect on dI_{BD}/dt ,^{1,3} hence, the differences in the gate area of the devices used in this work will not affect neither the analysis nor the conclusions. It is clear from the figure that the data for Al₂O₃ and Si₃N₄ are almost overlapping, while HfO₂ and

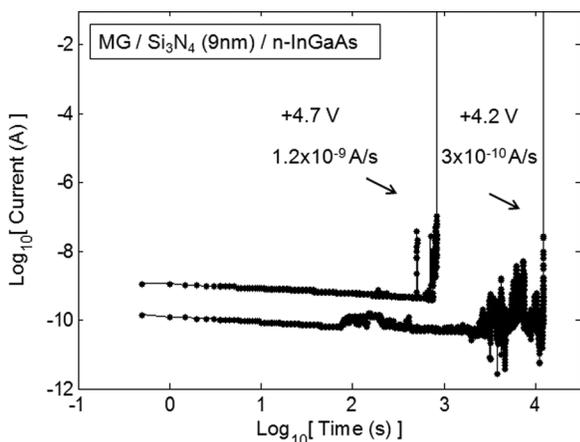


FIG. 3. Typical measurements of current as function of the time under constant voltage stress for the metal gate/Si₃N₄(9 nm)/n-InGaAs MOS stacks for constant voltage stress values ranging from +4.2 V to +4.7 V.

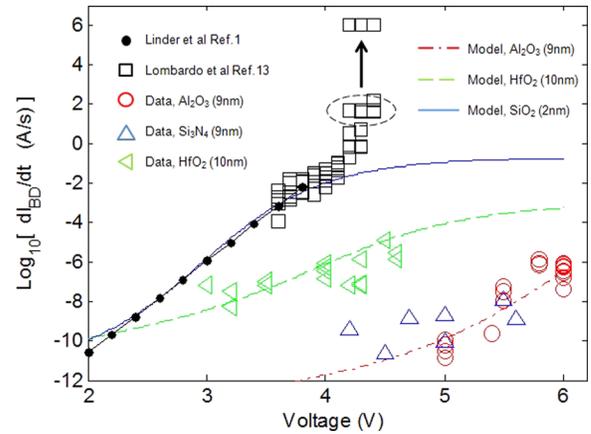


FIG. 4. Rate of the BD current increase, dI_{BD}/dt , as function of the stress voltage measured in MOS stacks with different dielectrics. The symbols \circ , \triangle , and ∇ , correspond to Al₂O₃ (9 nm), Si₃N₄(9 nm) and HfO₂(10 nm), respectively. The experimental data of Poly-Si/SiO_xN_y (2 nm)/Si from Refs. 1 and 13, marked by \bullet and \square , respectively, and the calculations according to Eq. (3) are also included.

SiO_xN_y show a faster progressive BD, with an increased dI_{BD}/dt of 4 and 12 orders of magnitude respectively. A strong dependence on voltage is observed in all cases. The dI_{BD}/dt values reported in Figure 4 reflect the evolution of the current during the BD event observed experimentally. For example, in the case of Al₂O₃ (Fig. 1), the time to reach a current level of the order of 1 μ A ranges from few seconds at +6 V, up to 10⁺⁴ seconds at +5 V, while in the case of HfO₂ (Fig. 2) the time to reach a current level of the order of 1 μ A ranges from a few seconds at +4 V up to 10⁺³ seconds at +3 V. It is observed that the duration of the breakdown transient decreases dramatically for HfO₂ even though the stress voltage is lower, and the oxide is slightly thicker. Such a drastically different behavior among these various dielectric layers raises the question about the cause of the difference.

It is worth to mention that the results of Figure 4 do not depend on the polarity of the stress voltage. A negative bias will only modify the degradation phase of the dielectric but not the duration of the progressive increase of the current.³

It is very important to compare our data measured on samples with InGaAs substrates with similar cases studied on samples with Si substrates. For example, the present case of the HfO₂ gate dielectric can be compared with Ref. 15, referring to the case of a TiN/HfO₂/interfacial SiO₂/Si substrate, with a 2.5 nm thick HfO₂ film and 1 nm SiO₂ layer. In this case, the dI_{BD}/dt values were of about 10⁻⁸–10⁻¹⁰ A/s at 2.5–3 V, very close to those reported here (Fig. 4). So, though the substrate material is very different (Si vs. InGaAs), very similar dI_{BD}/dt values are found. We then conclude that the presence of Si atoms is not a requirement for the occurrence of the PBD phenomenon, since this is found with gate electrodes such as poly-Si or metal, with different gate oxides such as SiO₂, SiON, or high-k dielectrics, and even with different substrates such as Si or InGaAs. The basic physics of PBD is not related to some kind motion of silicon atoms, but rather another effect is playing the major role, as proposed in the model here presented. The similarities of dI_{BD}/dt values here found compared to Ref. 15 are

well explained by the model we propose in the following part of the paper.

Since a high- k /InGaAs interface with a low density of defects is difficult to achieve and is currently under intensive investigation,^{19–22} one may argue that a poor structural quality is responsible for the results observed in Figure 4, particularly in the case of the relatively fast BD transient observed for the HfO₂. In fact, we observe that the gate stack quality in terms of interface states, border traps, and leakage current affects only the first phase of the current-time measurements, and does not influence the progressive BD regime.^{3,19,23} In our samples, the initial defect density is sufficiently low and the MOS samples have to be stressed at high voltage for long times to increase the defect density within the dielectrics beyond the percolation threshold for BD^{24–26} in order to observe within reasonable times the onset of progressive BD.

Since in Figure 4, the dI_{BD}/dt values are compared to those of ultra-thin SiO_xN_y layers (1.5–2.5 nm), a more accurate way is to compare the data taking into account the oxide thickness dependence found by Linder *et al.*¹ They report that the degradation rate increases by one order of magnitude for every 0.3 nm of scaling.¹ By comparing Linder's data with our results of the Al₂O₃ films, which are 7 nm thicker, the difference in dI_{BD}/dt should be $7/0.3 = 23$ orders of magnitude. The direct comparison of the experimental data (Figure 4), however, gives a difference of only 9 orders of magnitude, far much smaller difference than expected. It is clear that simple data extrapolation is unable to predict the dI_{BD}/dt behavior. Therefore, a detailed physical understanding is necessary.

IV. ANALYSIS

Summarizing the experimental results, as shown in Figure 4, the behavior of the breakdown growth rate dI_{BD}/dt as a function of the gate voltage in the high permittivity dielectrics studied in this work, Al₂O₃ (9 nm), HfO₂ (10 nm), Si₃N₄ (9 nm), ALD deposited on InGaAs substrates with a Au/Ti (1 nm) metal gate, is many orders of magnitude different compared to the well known baseline of poly-Si/SiO_xN_y/Si.^{1,13} The high permittivity materials show a much lower dI_{BD}/dt , implying a considerably improved reliability margins in CMOS applications compared to the Poly-Si/SiO_xN_y/Si classical system. However, such an improvement is not as large as expected on the basis of the thickness dependence reported by Linder *et al.*¹ Such an important experimental result calls for some basic understanding. We now propose a model which can explain such remarkable differences, and shows good agreement with the experimental results. The basic idea is that the progressive BD transient is due to an electro-migration effect providing atomic diffusion of the cathode or anode atoms into the gate dielectric in the region of the BD spot. A number of authors^{3,9,11,12} have shown that under BD conditions in poly-Si/SiO_xN_y/Si or in metal/HfO₂/SiO_xN_y/Si gate stacks the BD spot is characterized by the formation of a Si-rich (in the case of poly-Si/SiO_xN_y/Si stacks), or a metal-rich region (in the case of metal gate/high- K /Si stacks) in the gate dielectric in correspondence with the BD spot.^{3,11,12} This is a

clear evidence of atomic diffusion/electro-migration forming conductive channels/filaments in the gate dielectric. Moreover, the post-BD I - V characteristics under progressive BD are quite well explained by physical models invoking either co-tunneling^{9,27,28} or conductive filaments in the Landauer-Buttiker regime.^{29,30} These models postulate nanometric filaments or islands acting as stepping stones in the dielectric made of metallic or semiconducting materials. The reduced dimensionality and nanometric size of the filament/islands produce the relatively low conductance of the BD spot. For the model assuming embedded nanometric islands, the conductance regime which may explain the BD spot conductance is co-tunneling,²⁸ close to the boundary of single electron tunneling. For the model assuming metallic filaments, the regime is that of a constriction of lateral size smaller than that accommodating the first 1D Landauer conductance channel.³¹ In both cases, the BD spot resistance is larger but close to the value of a quantum of resistance $R_Q = h/q^2 \approx 25.8$ k Ω , with q being the elementary charge and h Plank constant. Note that R_Q corresponds to a current of ≈ 100 μ A at 3 V, relatively close to the conditions here experimentally studied.

Such current levels may trigger diffusion/electro-migration of atomic species in the BD spot,^{3,11} and this suggests a basic simple model to interpret the experimental results. According to Huntington³² and to Ho and Kwok,³³ by following a theoretical approach of irreversible thermodynamics, the flux J_{EM} of atoms moving by electro-migration is the sum of the gradients of the chemical potentials of the various atomic species present and of the electrostatic potential gradients weighted by suitable coefficients proportional to the relative atomic species diffusivities, plus crossed terms each proportional to the charge carrier flux (electron and hole fluxes) J times the atomic species diffusivity. In the cases investigated here, the BD conductance is most likely dominated by electrons, so we assume simply an electron flux (no holes). The model however can be simply extended to include the case of hole conduction.

Since A_{BD} (area of the BD spot) is of the order of 1–50 nm², J is in the range of 200–10 000 MA/cm², i.e., a regime of intensive electro-migration.^{3,11,33} Given such large J values, we assume that simply one term, proportional to $D \times J$, where D is the fastest (dominant) diffusivity, is the main contribution to J_{EM} .

Let us derive the leading equation with some details. According to Ho and Kwok,³³ the crossed-term linking the atomic flux J_{EM} to the density of electrons transferring momentum to the diffusing metallic ions is

$$J_{EM} = q^2 \frac{N_{at} D}{k_B T} n_e \lambda_e \sigma_e E, \quad (1)$$

where E is the electric field, N_{at} is the atomic density of the metal, D is the atomic diffusivity, k_B is the Boltzmann constant, T is the temperature, n_e is the electron density of the metal assumed to be the responsible for the intensive electro-migration taking place, λ_e is the electron mean free path, σ_e is the cross-section for the electron-atom collision, i.e., the basic mechanism responsible for the transfer of

momentum from the conduction electron of the metal to the diffusing atom and therefore of the electro-migration. As mentioned above, the I–V characteristics under progressive BD are quite well explained by well known physical models, for example, by invoking co-tunneling.^{9,27,28} According to this, it is easy to show that I_{BD} is given by the product $C_1(A) \times C_2(V, t_{ox})$ where C_1 is a monotonically increasing function of A , the BD spot base area, and C_2 is a function of V , the voltage, and t_{ox} , the oxide thickness. In particular, in the co-tunneling regime with low conductance C_1 is equal to A^α , with $\alpha = 4$. From such power law dependence it follows that $\frac{dI_{BD}}{dt} = \frac{\alpha I_{BD}}{A} \frac{dA}{dt}$. As the BD spot area A grows, the BD becomes harder, i.e., I_{BD} increases, and so it approaches the simpler Ohm's law limit where, by assuming a cylindrical geometry for the BD filament, $\frac{dI_{BD}}{dt} = \frac{V}{\rho_{ox}} \frac{dA}{dt} = \frac{I_{BD}}{A} \frac{dA}{dt}$, where ρ is the metal resistivity. Namely, we obtain the same expression as above but with $\alpha = 1$.

So we can in general assume that

$$\frac{dI_{BD}}{dt} = \frac{\alpha I_{BD}}{A} \frac{dA}{dt} \quad (2)$$

and for simplicity we take $\alpha = 1$.

For mass conservation the BD spot growth is due to the flux J_{EM} , i.e., $\frac{dA}{dt} = \frac{J_{EM}}{q} \frac{A}{t_{ox} N_{at}}$. So, by using Eqs. (1) and (2), and with some straightforward re-writing one finds the following very concise equation

$$\frac{dI_{BD}}{dt} = \frac{qV}{k_B T} \frac{f_1}{t_{ox}^2} D I_{BD}, \quad (3)$$

where $f_1 = n_e \lambda_e \sigma_e$. Clearly f_1 is larger or equal to 1, but of the order of 1 since the defect concentration in the metallic filament is most likely very high. Equation (3) satisfies the experimental finding of Linder *et al.*¹ that $dI_{BD}/dt = I_{BD}/\tau$, where τ is a time constant. In addition, Eq. (3) gives a direct physical explanation for τ .

According to Eq. (3), dI_{BD}/dt is proportional to $D \times I_{BD}$. This means that the BD growth rate grows either by increasing the charge carrier (usually electron) flux or by increasing the dominant diffusivity D of the fastest atomic species. The particular species may change, depending on the system. It may consist of Si atoms, or metal atoms coming from the gates, etc, as suggested by the electron microscopy studies on the BD spot nanostructure.^{3,11,12,34,35} There is also a strong dependence on t_{ox} , and on V and T . So, according to Eq. (3), since V , T , and t_{ox} are known, to evaluate dI_{BD}/dt we need to model the two parameters I_{BD} and D . I_{BD} is quite well described by the models mentioned above assuming co-tunneling of charge carriers due to one or few conductive islands embedded in the gate dielectric in correspondence with the BD spot^{9,11} or a quantum size metallic filament modeled according to the Landauer-Buttiker formalism.^{29,30} These models contain numerous parameters, the values of which are difficult to predict and require data fitting. To simplify the approach, we have preferred to model the BD spot I_{BD} - V curve by assuming the following simple analytical dependence:

$$I_{BD} = I_1 \exp \left[\log \left(\frac{I_2}{I_1} \right) \left(\frac{V - V_1}{V_2 - V_1} \right)^\alpha \right], \quad (4)$$

where I_1 , I_2 , V_1 , V_2 , and α are parameters chosen by best fit to the experimental I_{BD} - V data. To determine the parameters we choose two points (I_1, V_1) and (I_2, V_2) in the experimental I_{BD} - V curve at low and high voltage, respectively, and we set α by data fitting. Figure 5 shows typical experimental data of the current-voltage characteristics of the BD spot during the PBD regime for HfO_2 and Al_2O_3 . At low voltages, the I_{BD} - V curves were measured after interrupting the CVS, in between one stress and the following, while at high voltages, the current level of I_{BD} was determined just before the abrupt jump to very high levels (Figure 1) for different values of CVS bias. Figure 5 also shows the comparison of the experimental data with the model of Eq. (4), indicating that the best fit to the experimental data is generally found for $\alpha \approx 0.5$.

To model D, we need first to model the temperature in the BD spot and for that we need to solve the heat diffusion equation. We make a strong simplification of spherical symmetry around an inner sphere of radius r_1 in which there is a source power density q_1 constant over the inner sphere surface. q_1 is the electrical power, dissipated in heat, proportional to $I_{BD} \times V$ at the BD spot center. This assumption is reasonable: for example, Takagi *et al.*³⁶ have shown that the electrons tunneling through defects responsible for stress induced leakage current (SILC) in thin oxynitrides do lose a large fraction of their energy in the oxide. That is, the electron tunneling through SILC defects is inelastic, with a large fraction of electron energy lost due to defect relaxation, as shown by Blöchl and Stathis.³⁷ It is reasonable to assume that a similar effect takes place during electron transport through the BD spot. The other boundary condition for the heat diffusion equation concerns the temperature at an outer

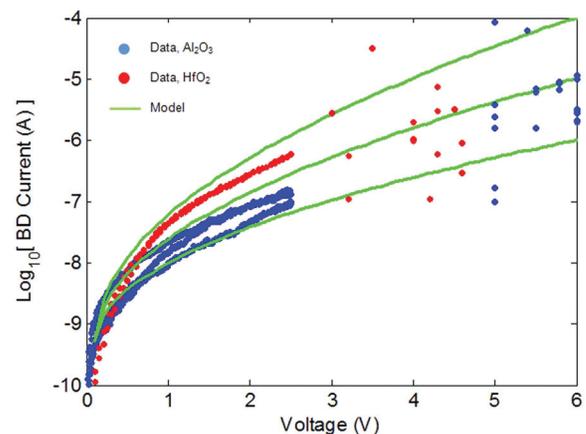


FIG. 5. Typical experimental data of the current-voltage characteristics of the BD spot during the PBD regime for HfO_2 and Al_2O_3 . At low voltages, the I_{BD} - V curves are measured after interrupting the CVS, in between one stress and the following, while at high voltages, the current level of I_{BD} was determined just before the abrupt jump to very high levels (Figure 1) for different values of CVS bias. The continuous curves are the calculation according to the model of Eq. (4), indicating that the best fit to the experimental data is generally found for $\alpha = 0.5$.

sphere of radius r_2 , set constant and equal to T_2 , the ambient temperature T_{amb} . Then, for $r_1 < r < r_2$ the temperature $T(r)$ is

$$T(r) = \frac{q_1 r_1^2}{\kappa} \left(\frac{1}{r} - \frac{1}{r_2} \right) + T_2, \quad (5)$$

where κ is the thermal conductivity of the dielectric, with the further simplifying assumption of neglecting the thermal influence of the other materials present in the gate stack.

We assume that $q_1 = \frac{f_2 V I_{\text{BD}}}{4\pi r_1^2}$ where f_2 is the fraction of the energy qV per electron lost at the BD spot, that $r_1 = t_{\text{ox}}/2$ and that $r_1 \ll r_2$. Then at a distance $r = r_1$ from the source of the diffusing atoms contributing to the BD spot growth, according to Eq. (5) the temperature T is

$$T = \frac{f_2 V I_{\text{BD}}}{2\pi t_{\text{ox}} \kappa} + T_{\text{amb}}, \quad (6)$$

where T is the local temperature at the electrode which provides the dominant diffusing atomic species, at the boundary with the BD spot. Then, the diffusivity D is simply $D = D_0 \exp(-E_{\text{act}}/k_B T)$, where D_0 is a pre-exponential term, and E_{act} is the diffusion activation energy.

We have applied this model (Eqs. (3), (4), (6), and $D = D_0 \exp(-E_{\text{act}}/k_B T)$) to fit the experimental data of dI_{BD}/dt vs. gate voltage reported in Figure 4 for a number of MOS systems: Poly-Si/SiO_xN_y/Si (from Refs. 1 and 13), taken as baseline, compared to the high permittivity dielectrics studied in this work: Al₂O₃ (9 nm), HfO₂ (10 nm), Si₃N₄ (9 nm), ALD deposited on InGaAs substrates with a Au/Ti (1 nm) metal gate.

Clearly such a fit cannot accurately establish the parameter values, but rather it allows to find the order of magnitude of the various parameters. The fit parameters are in fact four: E_{act} , D_0 , f_1 , and f_2 . The other five I_1 , V_1 , I_2 , V_2 , and α are directly quite accurately evaluated by comparison with the experimental $I_{\text{BD}}-V$ curves of the BD spot (such as Figure 5). In all cases, as shown by comparison of Eq. (4) with the data reported in Figure 5, α can be estimated to be 0.5. The thermal conductivities κ are not fit parameters and have been taken from the literature. The values are reported in Table I. It is important to emphasize the very different values of κ explored in this work.

The f_1 parameter (where $f_1 = n_e \lambda_e \sigma_e$) has been fixed in all cases to be 1. This is a reasonable assumption; by considering the fact that the BD spot metallic filament is most likely a densely defect populated material, so $f_1 \approx 1$. f_2

(the fraction of the energy per electron dissipated in the dielectric as heat at the BD spot) has been assumed to be 0.5 in the cases of Al₂O₃, Si₃N₄, and HfO₂, and 0.25 in the case of SiO_xN_y. The chosen value for SiO_xN_y has been estimated by considering the results of Takagi *et al.*³⁶ on SILC loss, while the larger value assumed for the high-K materials has been taken to consider the larger thickness (about 10 nm for the high-K materials vs. 2 nm for the SiO_xN_y). So, in fact, in the chosen fit conditions, there are only two parameters to fit, those describing the atom diffusivity D , i.e., E_{act} and D_0 . The model provides a quite good fit to the experimental data, as shown in Figure 4. In all the cases the best fit diffusivities are quite large, of the order of 10^{-13} cm²/s at 1000 K, with low activation energies ranging from 0.7 to 0.3 eV. Such large D values may be reasonable by considering that the diffusivity is evaluated under high electric field application. It has been found that the diffusivity of metals ions in dielectrics (SiO₂) is strongly influenced by the electric field strength. In conditions comparable to those here studied, the diffusivities of metals in dielectrics are in a range coincident to that here reported,^{38–41} see for example, the case of Cu diffusion into SiO₂ layers.⁴¹

The very different behaviour of the various materials shown in Figure 4 is explained by the very different combinations of t_{ox} and κ in the various cases. Note in particular the cases of Si₃N₄, Al₂O₃, and HfO₂, which share the same type of metal gate and substrate, and have essentially the same t_{ox} . Nevertheless HfO₂ shows a much lower dI_{BD}/dt . The only main difference is κ , and this results in a completely different behaviour of dI_{BD}/dt , well explained by the model (Eq. (6)). On the contrary, Si₃N₄ and Al₂O₃, which have similar thermal conductivity, show very similar dI_{BD}/dt .

At large voltages/currents the BD spot temperature estimated through the present model exceeds 1000–2000 K, i.e. local melting of the gate stack takes place. This voltage/current/temperature region is clearly beyond the range of applicability of the present model since a solid-liquid phase transition takes place, and it is where the dI_{BD}/dt vs. V model curve starts to saturate. So, the saturation region of the model curves of Figure 4 is beyond the model validity range and has no meaning.

V. SUMMARY AND CONCLUSIONS

In this paper, we have shown that the progressive BD event occurs in the case of metal gates, high-K dielectrics and InGaAs substrates. Therefore, taking into account previous literature we find that the progressive BD in MOS structures occurs with Poly-Si or metal gate electrodes, with SiO₂, SiO_xN_y or high-k dielectrics as gate oxides, and with Si or InGaAs substrates. Namely, it is a very general physical effect which does not necessarily requires the motion of Si atoms.

We therefore propose that the PBD is due to the energy transfer from the BD path to its surroundings which promotes electro-migration of the fastest atomic species among those available, providing the build-up of the BD filament. Our results unambiguously relate the breakdown growth rate dI_{BD}/dt to heat dissipation properties during the atomic diffusion of the cathode or anode atoms into the gate dielectric in

TABLE I. Description of samples studied.

Dielectric layer	ϵ_{ox}^a	Thermal conductivity ^b [W/m K]	Melting temperature [K]	Substrate	Gate
Al ₂ O ₃	~10	30	2300	InGaAs	Au
Si ₃ N ₄	7	~30	2100	InGaAs	Au
HfO ₂	~20	1.1	3000	InGaAs	Au
SiO ₂	3.9	1.4	1900	Si	Poly-Si

^aReference 42.

^bReferences 43–47.

the region of the percolation path. In dielectrics layers with higher thermal conductivity the power dissipated in the vicinity of the BD spot can be transferred to the environment at a speed large enough to maintain the temperature low, and, hence, to decrease the breakdown growth rate. The model proposed in this work captures the main physical mechanisms responsible for the progressive increase of the current when a gate dielectric loses its insulating properties. This physical interpretation provides a quite good fit to the experimental data with only two free parameters, related to the diffusivity of the faster atomic diffuser present in the gate stack (substrate, dielectric, and gate). The demonstrated ability to reduce the breakdown growth rate dI_{BD}/dt in MOS structures by increasing the thermal conductivity of the gate oxides is a key for improving considerably the reliability margins in CMOS applications. Besides their relevance for the scaling of gate dielectrics of transistors in modern CMOS integrated circuits, our results may provide a basic framework also for different applications of ultra-thin dielectrics, in particular for the electrically induced resistive switching effects which have been proposed as the basis for future semiconductor non-volatile memories.

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