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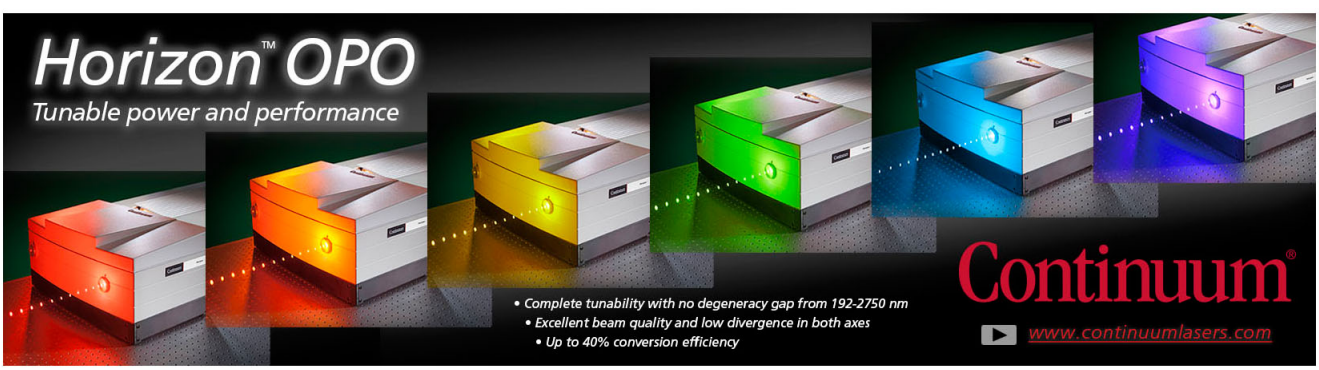

Characteristics of the dynamics of breakdown filaments in Al_2O_3/InGaAs stacks

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In this paper, the Al_2O_3/InGaAs interface was studied by X-ray photoelectron spectroscopy (XPS) after a breakdown (BD) event at positive bias applied to the gate contact. The dynamics of the BD event were studied by comparable XPS measurements with different current compliance levels during the BD event. The overall results show that indium atoms from the substrate move towards the oxide by an electro-migration process and oxidize upon arrival following a power law dependence on the current compliance of the BD event. Such a result reveals the physical feature of the breakdown characteristics of III-V based metal-oxide-semiconductor devices. © *2015 AIP Publishing LLC*.
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The dielectric breakdown (BD) phenomenon is still an open area of research, in particular, for nanostructures such as MOS (metal-oxide-semiconductor) and MIM (metal-insulator-metal) stacks. In such structures, the BD of the dielectric layer occurs in the regime of relatively low voltage and very high electric field; this is of enormous technological importance, and thus is widely investigated but still not well understood.[1,2]

In a recent paper, it has been demonstrated that the BD event for MOS stacks is controlled by the energy transfer from the BD path to its surroundings, which promotes electro-migration of the fastest atomic species among those available, providing the build-up of the BD filament.[3,4] However, other authors working with MIM stacks for Resistive Random-Access Memory (ReRAM) applications, suggest that the BD event is an intrinsic effect related to the bulk oxide material, and does not involve movement of metal ions from the contacts.[5,6]

In this paper, the influence of the BD event in metal/Al_2O_3/InGaAs stacks is studied by X-ray photoelectron spectroscopy (XPS), a suitable technique to detect surface oxides of InGaAs.[7]

MOS structures were fabricated on p-type $In_{0.53}Ga_{0.47}As$ substrates epitaxially grown on p-type InP wafers. The dopants concentration of the InGaAs was 3×10^{16} cm^{-3}. All samples were chemically cleaned in 10:1 diluted $(NH_4)_2S$ for 10 min, followed by de-ionized (DI) water rinse and blown dry with N_2, prior to their being loaded into the molecular-atomic-deposition (MAD) system.[8,9] The samples received forming gas ($95\%N_2 + 5\%H_2$) plasma treatment at room temperature, followed by Al_2O_3 deposition (4 nm) in a N_2 ambient. All samples received post-deposition anneal in N_2 at 500 °C for 3 min. Au was used as the gate electrode and Ti/Au was used as the back contact. All metals were deposited by e-beam evaporation. This methodology has been implemented previously and yielded good capacitors.[10] The area of the devices was chosen to be larger than the area of the probing spot of the XPS technique.

To study the evolution of the oxide-semiconductor interface after electrical breakdown using the XPS technique, identical capacitors were subjected to different constant voltage stresses (CVS) at positive bias, until the occurrence of BD event for different maximum levels of current compliance. Since the mean free path of the emitted photoelectrons in XPS leads to an escape depth of less than 10 nm in most cases, the analysis cannot be carried out through the metal electrode, which is typically 40 nm thick or more. To overcome this issue, the contacts were removed by selective chemical etching using a I_2/KI (4:1w:w) solution. The sample was then rinsed in DI water and dried with N_2.

Samples A, B, and C were stressed with CVS at 100 mA, 10 mA, and 1 mA, respectively. Sample D was stressed with CVS, but the BD was not reached. For reference, fresh capacitors (with no CVS) were analyzed as well (sample E).

XPS spectra were collected in a Thermo VG Scientific Sigma Probe system using a monochromatic Al Ka (1486.6 eV) X-ray source. In *3d* spectra were collected with pass energy of 50 eV. Curve fitting was done by XPSPEAK 4.1 software using a 15% Gaussian–Lorentzian convolution with a Shirley-type background.

Figure 1 shows a typical BD transient of gate current observed under CVS.[7] In this case, a stress voltage of +5 V with a compliance limit of 100 mA were used. As reported in our previous papers,[3,11] the transient I vs. time curves during CVS are characterized by at least two distinctive phases. The first regime is characterized by a noisy process which is attributed to charge trapping and generation of defects, while the second is the breakdown event that occurs when a certain critical density of defects is reached, and it is characterized

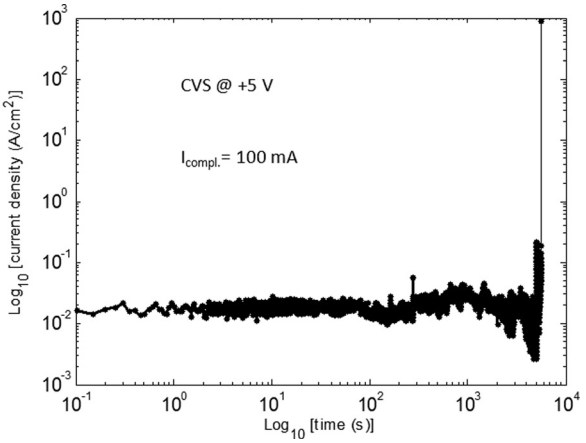

FIG. 1. Typical curves of current density as function of the time under constant voltage stress for +5 V with compliance limit of 100 mA. Reprinted with permission from Appl. Phys. Lett. **105**, 102908 (2014). Copyright 2014 AIP Publishing LLC.

by a progressive increase of the current and an abrupt increase of the current to very high levels.[1,12]

It is worth to note that the magnitude of the stress applied on the metal gate is not an important parameter in our experiments. A change in the magnitude of the voltage will only affect the onset time of the BD event, but not the characteristics of the BD spot, thanks to the similarity in current during BD. Therefore, the relevant parameter that defines the characteristic of the BD event is the current compliance limit.

Figure 2 presents the results of the XPS measurements for samples E (fresh), D (stressed with no BD event), and A (BD with 100 mA current compliance). The deconvolution of the In*3d* spectra of the fresh and the two broken samples reveals the presence of two types of bonds of indium. The first signal, at 447.2 eV, corresponds to In in InGaAs. For all samples, this peak has a similar intensity, indicating an even oxide thickness before and after breakdown. The second signal is found at a higher binding energy and is related to the In-O bond. The ratio between the oxide peak and the InGaAs peak changes drastically after breakdown under a positive bias with a current compliance of 100 mA (see Fig. 2(c)).

These results show that after the breakdown event at positive bias, there is an increase in the intensity of the In-O oxide bonds. Formation of an additional oxide layer underneath the existing Al_2O_3 layer would have caused a significant drop in the bulk signals, which is not observed. Therefore, we suggest that under breakdown at positive bias, a substantial amount of elements from the InGaAs substrate moves into the dielectric Al_2O_3 layer and oxidizes. In contrast, for samples E (fresh) and D (stressed with no BD), such a phenomenon is not observed (see Fig. 2).

Although the investigated area under the XPS technique is much larger than the area of the BD spot, it is possible to deduce the composition of the volume of the oxide containing the BD filaments. It is well known that after the BD event a localized damage occurs within the oxide layer.[1] In this context, due to the absence of an additional oxide layer in the interface, the In atoms that migrate into the Al_2O_3 layer can be considered as the material that occupies the percolation path through the gate oxide after the BD event.

Figure 3 shows the evolution of the In*3d*5/2 XPS spectra for the fresh sample and the samples after BD at different current compliance limits. It is clear that the intensity of the signal related to the In-O bond changes drastically as function of the current compliance of the breakdown event at positive bias. Figure 4(a) presents the dependence of the

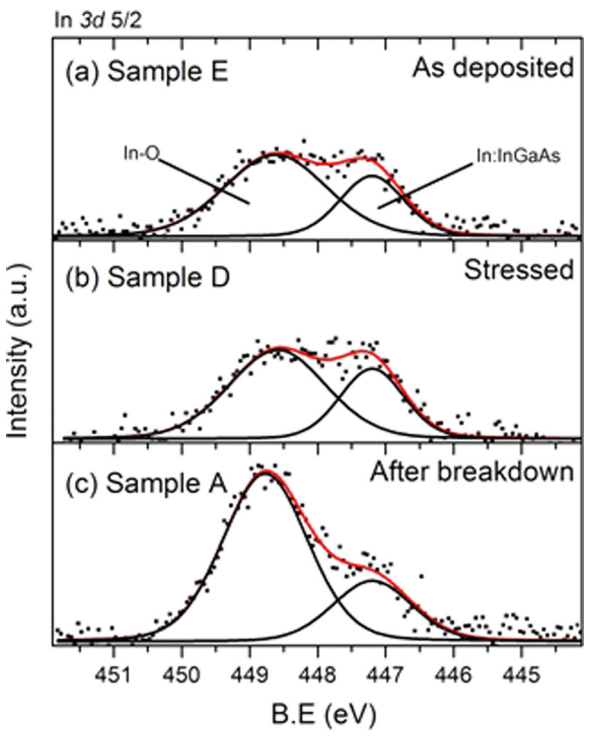

FIG. 2. XPS spectra of In*3d*. The XPS spectra correspond to the as deposited (a), stressed (b), and after breakdown (c) samples.

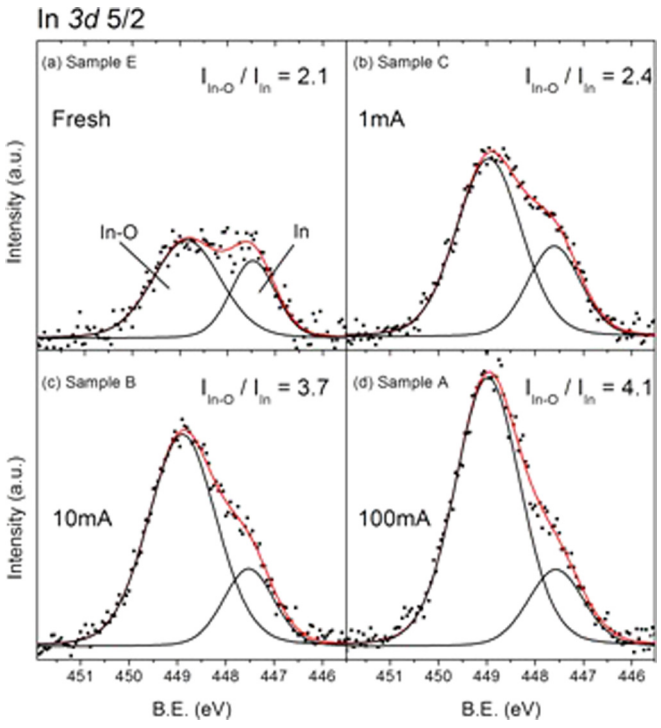

FIG. 3. XPS spectra of In*3d*. The XPS spectra correspond to the as deposited (a), and after breakdown samples for different current compliances. 1 mA, 10 mA, and 100 mA correspond to (b)–(d), respectively.

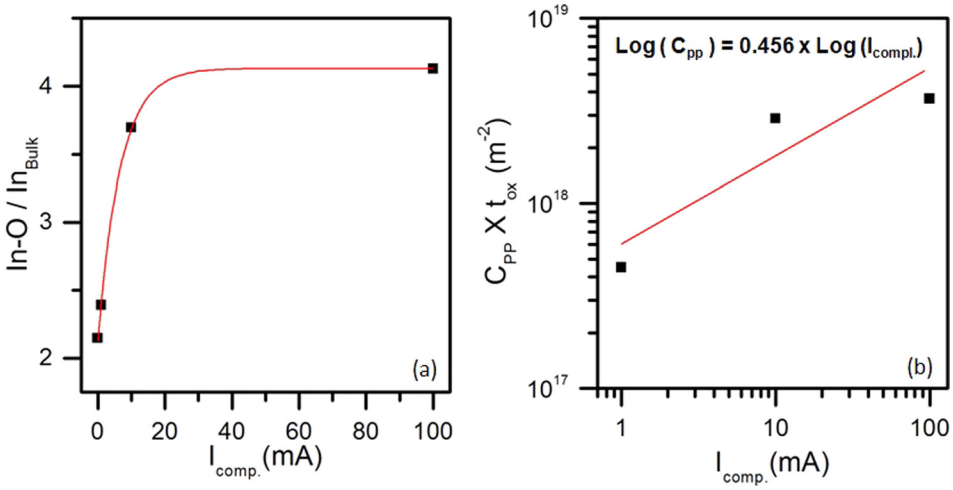

FIG. 4. The ratio between the In-O signal and the bulk In signal from XPS spectra of In*3d* for samples after breakdown with different compliance limit. (a) The ratio between the In-O signal and the bulk In signal as function of the compliance limit; (b) C_{pp} (the concentration of In-O bonds in the percolation path times the overall area of paths) as function of the compliance limit during breakdown.

ratio between the oxide peak and the InGaAs peak (named, $In\text{-}O/In_{bulk}$ in Fig. 4(a)) as function of the compliance limit (marked $I_{compl.}$ in Fig. 4). This analysis allows us to see the amount of In that migrates into the Al_2O_3 layer and so understand the degree to which the oxide has been degraded.

The diffusion of atoms from the contacts into the gate dielectric is the main aspect of the physical damage associated with gate-oxide BD.[3] However, based on the present results, it is clear that some differences occur between stacks with different materials. For the case of MOS stacks with Si/SiO_2 interfaces, it has been experimentally demonstrated that under positive bias, the local surge current after the BD event can generate hillocks nucleated at one of the Si contacts, epitaxially aligned to the Si lattice.[1] While for the MOS stacks studied in this paper, with Al_2O_3/InGaAs interfaces, under positive bias a substantial amount of elements from the InGaAs substrate moves into the Al_2O_3 dielectric layer and oxidizes.

In order to reach an analytical expression for the different intensities of indium we assume that the only source for In-O bonds in the sample that did not undergo breakdown ("Fresh" sample) is the Al_2O_3/InGaAs interface. Furthermore, we assume that the concentration of In-O through the $Al_2O_3$is constant.[13] Under these assumptions, we can get that the intensities of In in bulk InGaAs (In_{bulk}), In-O in the fresh sample, and In-O in every sample that underwent breakdown are, respectively,

$$I_{Bulk} = I_0\left(e^{\left(\frac{-t}{\lambda_{Al_2O_3}}\right)} - \frac{I_{Noise}}{I_{Bulk}}\right)\lambda_{InGaAs}C_{bulk}, \quad (1)$$

$$I_{In-O}|_{Fresh} = I_{IL} = I_0 e^{\left(\frac{-t}{\lambda_{Al_2O_3}}\right)}C_{IL}, \quad (2)$$

$$I_{In-O}|_{BD} = I_{IL} + I_{Oxide} = I_0\left(C_{PP}\lambda_{Al_2O_3} + (C_{IL} - C_{PP}\lambda_{Al_2O_3})e^{\left(\frac{-t}{\lambda_{Al_2O_3}}\right)}\right), \quad (3)$$

where I_0 is the intensity of the main beam multiplied by the emission efficiency of the In *3d* signal, t is the thickness of the Al_2O_3 film (4 nm), $\lambda_{Al_2O_3}$ and λ_{InGaAs} are the mean free paths of the emitted electrons in the Al_2O_3 and InGaAs, respectively, $\frac{I_{Noise}}{I_{Bulk}}$ is the noise level (the standard deviation of the noise) with respect to the intensity that originates from the bulk, that was estimated here as 3%, C_{bulk} is the concentration of In in the InGaAs bulk, C_{IL} is the concentration of In-O bonds at the Al_2O_3/InGaAs interface, and C_{PP} is the concentration of In-O bonds in the volume of the Al_2O_3 averaged between the percolation paths and the undamaged Al_2O_3. $\lambda_{Al_2O_3}$ and λ_{InGaAs} were found to be 2.04 nm and 2.3 nm using the TPP-2M equation.[7]

In order to remove the contribution of the main beam, the ratios between the two different In-O and bulk In signals can be used

$$\frac{I_{In-O}|_{Fresh}}{I_{Bulk}} = \frac{e^{\left(\frac{-t}{\lambda_{Al_2O_3}}\right)}C_{IL}}{\left(e^{\left(\frac{-t}{\lambda_{Al_2O_3}}\right)} - \frac{I_{Noise}}{I_{Bulk}}\right)\lambda_{InGaAs}C_{bulk}}, \quad (4)$$

$$\frac{I_{In-O}|_{BD}}{I_{Bulk}} = \frac{C_{PP}\lambda_{Al_2O_3} - (C_{PP}\lambda_{Al_2O_3} + C_{IL})e^{\left(\frac{-t}{\lambda_{Al_2O_3}}\right)}}{\left(e^{\left(\frac{-t}{\lambda_{Al_2O_3}}\right)} - \frac{I_{Noise}}{I_{Bulk}}\right)\lambda_{InGaAs}C_{bulk}}. \quad (5)$$

Assuming that the concentration of the In-O bonds at the interface is constant, the value of C_{IL} can be carried from the fresh sample to the samples after breakdown. This assumption is with accordance with previous results.[13]

Obtaining the correlation between the $I_{In\text{-}o}/I_{bulk}$ (the ratios between the two different In-O and bulk In signals) and C_{pp} (the concentration of In-O bonds in the percolation path times the overall area of paths) (Equation (5)), we can plot C_{pp} as function of the current compliance ($I_{compl.}$) using the experimental data of $I_{In\text{-}o}/I_{bulk}$ vs. $I_{compl.}$, as observed in Figure 4(b).

This result describes the amount of material that moves towards the oxide layer by the electro-migration effect. From Fig. 4(b), it is clear that the amount of In atoms that move by electro-migration and oxidize upon arrival, follow a power law dependence with the current compliance of the BD event ($\text{Log}C_{pp} \sim \text{Log}\ I_{compl.}$). It is worth to note that even though a power law dependence can be reasonable, three data points are only enough to show a trend but not sufficient to obtain the precise exponential dependence. Such an observation agrees with independent results about the dependence of BD hardness on current compliance in different ultra-thin oxide layers. Lombardo[14] reported for SiO_2 layers for CMOS applications, a power law dependence of the leakage current as a function of the compliance limit imposed on the gate

current during stress. On the other hand, in the case of MIM stacks ($Pt/HfO_2/Pt$) for ReRAM memories, it has been reported that the HRS (high resistance state) shows a power law dependence with the current compliance of the forming step.[15] This similar behavior in connection with the current compliance, suggests a common physical feature between such diverse stacks, which is characterized by the XPS results as function of the current compliance (Fig. 3).

In this context, power law dependence is reasonable since the atomic diffusion of the cathode or anode atoms into the gate dielectric during the BD event is the main feature of the physical damage associated with gate-oxide breakdown.[3]

Intrinsic BD of ultra-thin gate oxides occurs when the oxide reaches a critical defect density for which the defects form in a point of the MOS stack a percolative path joining cathode and anode.[16,17] After the BD instant, current begins to flow through the path and the BD spot can evolve in a thermally damaged region. In this context, the basic idea is that the modifications observed by XPS (Figs. 2 and 3) are due to an electro-migration effect providing atomic diffusion of the cathode or anode atoms (depending on the stress bias) into the gate dielectric in the region of the BD spot.

For the case where the sample is stressed without occurrence of a BD event (Fig. 2(b)), there is no change compared to the fresh sample (Fig. 2(a)). In the absence of current flowing through the dielectric (i.e., BD event), there is no momentum transfer to the metallic ions. While for the case where the gate oxide is subjected to BD, the high density of carriers though the BD spot[18,19] (i.e., electro-migration regime[20]) provides atomic diffusion of the cathode atoms into the gate dielectric (Fig. 2(c)).

The drastic evolution of the In*3d*5/2 signal with increasing breakdown compliance can be easily observed (Fig. 3). While the bulk In signal retains its intensity, with a 5% margin, the In-O integrated intensity increases significantly to almost twice its original value for 100 mA. This result indicates that during the formation of the percolation path through the dielectric, paths/filaments with different compositions can be formed under different breakdown conditions. By increasing the current compliance during the BD event, an increasing amount of In atoms electromigrate into the oxide and oxidize upon arrival. It can be observed from the evolution of the concentration of In-O bonds in the percolation path (named, C_{pp} in Fig. 4(b)). Such migration of substrate atoms into the dielectric is consistent with a filament growing (due to In-O bonds in this case) from the substrate. Note that the In concentration is an appropriate parameter to underline the dependence on the current compliance since it is an averaged concentration. Either the relative area of the paths becomes larger or the concentration of defects (in the shape of In-O bonds) in the paths increases. Both options mean an increase in damage.

This result is in agreement with previous compliance current studies and provides a more precise characterization of the BD process. Further strong experimental evidence in favor of the above description is given by recent electron microscopy and XPS works. Pey *et al.*[21] have shown evidence of filaments formed in the gate oxide in samples subjected to progressive breakdown, both in the case of Poly-Si/SiON/Si and metal gate/high-k/Si MOS stacks.[21] Privitera *et al.*[2] have shown filament presence in the case of HfO_2based ReRAM MIM devices after forming.

In summary, the Al_2O_3/InGaAs interface was studied by XPS after the breakdown event at positive bias applied to the gate contact. It is observed an increase of the In-O bonds following a power law dependence with the current compliance of the BD event. Our findings show a better understanding of the breakdown characteristics of III-V based MOS devices.

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[1]S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, J. Appl. Phys. **98**, 121301 (2005).
[2]S. Privitera, G. Bersuker, B. Butcher, A. Kalantarian, S. Lombardo, C. Bongiorno, R. Geer, D. C. Gilmer, and P. D. Kirsch, Microelectron. Eng. **109**, 75 (2013).
[3]F. Palumbo, S. Lombardo, and M. Eizenberg, J. Appl. Phys. **115**, 224101 (2014).
[4]F. Palumbo, M. Eizenberg, and S. Lombardo, IEEE Int. Reliab. Phys. Symp. (2015) p. 5A.1.1.
[5]F. Zhou, Y.-F. Chang, B. Fowler, K. Byun, and J. C. Lee, Appl. Phys. Lett. **106**, 063508 (2015).
[6]A. Mehonic, M. Buckwell, L. Montesi, L. Garnett, S. Hudziak, S. Fearn, R. Chater, D. McPhail, and A. J. Kenyon, J. Appl. Phys. **117**, 124505 (2015).
[7]P. Shekhter, F. Palumbo, K. C. Weinfeld, and M. Eizenberg, Appl. Phys. Lett. **105**, 102908 (2014).
[8]T. P. Ma, IEEE Trans. Electron Devices **45**, 680 (1998).
[9]W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, IEEE Electron Device Lett. **23**, 649 (2002).
[10]Z. Liu, S. Cui, P. Shekhter, X. Sun, L. Kornblum, J. Yang, M. Eizenberg, K. S. Chang-Liao, and T. P. Ma, Appl. Phys. Lett. **99**, 222104 (2011).
[11]F. Palumbo and M. Eizenberg, J. Appl. Phys. **115**, 014106 (2014).
[12]G. Condorelli, S. Lombardo, F. Palumbo, K. L. Pey, C. H. Tung, and L. J. Tang, IEEE Trans. Device Mater. Reliab. **6**, 534 (2006).
[13]S. Tanuma, C. J. Powell, and D. R. Penn, Surf. Interface Anal. **21**, 165 (1994).
[14]S. Lombardo, Microelectron. Eng. **59**, 33 (2001).
[15]F. Palumbo, E. Miranda, G. Ghibaudo, and V. Jousseaume, IEEE Electron Device Lett. **33**, 1057 (2012).
[16]J. H. Stathis, J. Appl. Phys. **86**, 5757 (1999).
[17]R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, IEEE Int. Electron Devices Meet. 863 (1995).
[18]R. Pagano, S. Lombardo, F. Palumbo, P. Kirsch, S. A. Krishnan, and C. Young, Microelectron. Reliab. **48**, 1759 (2008).
[19]F. Palumbo, G. Condorelli, S. Lombardo, K. L. Pey, C. H. Tung, and L. J. Tang, Microelectron. Reliab. **45**, 845 (2005).
[20]P. S. Ho and T. Kwok, Rep. Prog. Phys. **52**, 301 (1989).
[21]K. L. Pey, C. H. Tung, R. Ranjan, V. L. Lo, M. MacKenzie, and A. J. Craven, Int. J. Nanotechnol. **4**(4), 347 (2007).