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F. Palumbo, R. Winter, I. Krylov, and M. Eizenberg

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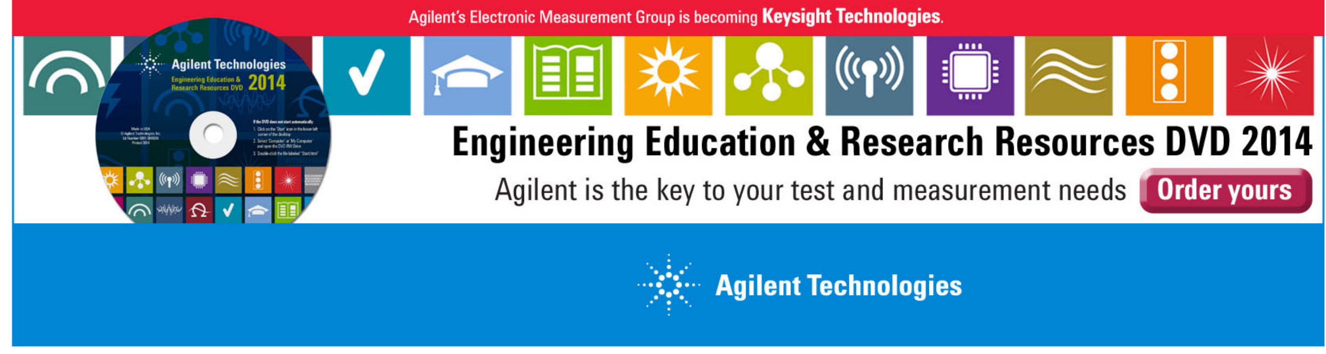

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Characteristics of stress-induced defects under positive bias in high-k/InGaAs stacks

F. Palumbo,[a] R. Winter, I. Krylov, and M. Eizenberg
Department of Materials Science and Engineering, Technion-Israel Institute of Technology, 32000 Haifa, Israel

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The introduction of InGaAs as a channel material for complementary metal-oxide-semiconductor technology presents major challenges in terms of the characterization of the various defects that affect the performance and reliability. Understanding the generation of defects by constant voltage stresses is crucial in terms of their concentration profiles and energy levels. In particular, we want to understand the real nature of the defects responsible for the dispersion of C-V in strong accumulation. Here, we show that the degradation under positive bias of metal/Al_2O_3/n-InGaAs capacitors reveals two contributions depending on the temperature that affects the C-V curves in a different way. Based on features of stressed C-V curves, it is possible to estimate the onset point of the distribution of border traps near the midgap condition. The results suggest that these defects are strongly related to the characteristics of the InGaAs substrate. © *2014 AIP Publishing LLC*.
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InGaAs is an attractive candidate to be used as a channel material beyond Si thanks to its high electron mobility. Lacking a good native oxide interface, a major challenge in using it is the characterization and the understanding of the various defects components that affect the high-k dielectric/InGaAs performance and long term reliability.[1] One of the most common approaches for defect characterization is the capacitance–voltage (C-V) measurement over a wide range of frequencies.[2] In the inversion regime, the defects create a significant deviation from "standard" MOS C-V characteristics which is frequency dependent and defined in literature as "weak inversion hump"; it is attributed to high-k/InGaAs interface state densities around the semiconductor mid-gap energy.[3–5] In addition, in the strong accumulation regime, defects produce a frequency dispersion that cannot be explained by conventional interface states whose time constant in such bias regions is far shorter than the period of typical measurements frequencies (1 KHz–1 MHz).[5,6] Some authors attributed this dispersion to defects located within the oxide near the oxide/InGaAs interface (referred in the literature as "border traps"), which can communicate with the conduction and valence bands of the InGaAs by tunneling.[7] However, recent results show a temperature dependence of the frequency dispersion in accumulation induced by the so called "border traps."[8,9] On the other hand, some authors attribute the frequency dispersion in strong accumulation to a disordered interface layer due to substrate oxidation.[10,11] Such observations pose a question on the real nature of the defects responsible for the dispersion of C-V in strong accumulation. In this work, we study the generation of defects in strong accumulation by constant voltage stresses as function of the dielectric deposition process (i.e., quality of the interface) and the type of the dielectric layer used.

Different sets were used on n-type InGaAs substrates epitaxially grown on InP wafers. In set A, a pre-dielectric deposition treatment (PDT) was performed by a 36% NH_4OH solution. Then a 9 nm-Al_2O_3 layer (the most common dielectric for InGaAs) was prepared by atomic-layer-deposition (ALD). In set B, a 9 nm-Al_2O_3 film was deposited by the same ALD process but without the NH_4OH PDT. For set C, a different dielectric was used—following the PDT a 10 nm-HfO_2 layer was deposited by ALD. In all sets, the area of the devices was 1.1×10^{-4} cm^2, and the gate metallization consisted of Ti(1 nm)/Au(200 nm) deposition. In all cases, the metal deposition was followed by annealing at 400 °C in N_2 flow for 30 min. Description of the samples is summarized in Table I.

Capacitance–Voltage (C-V) measurements were carried out at different frequencies from inversion to accumulation. During constant voltage stress (CVS), the stress was periodically interrupted to measure the V_{FB} by the inflection point technique.[12] In order to avoid recovery-related artifacts, we kept constant values of the delay time between the C-V measurements and the CVS pulses. It is worth to note that in this work the CVS experiments were performed at room temperature (27 °C) and at 125 °C, while the C-V measurements between CVS pulses were performed at room temperature.

Figures 1(a) and 1(b) show typical consecutive C-V curves for set A after CVS pulses at negative bias (−4.8 V) and positive bias (+4 V), respectively, with an accumulated stress time of 10 min in both cases. Although the degradation at negative bias is not a topic of this paper, it is clear from

TABLE I. Description of samples studied.

Samples	Dielectric layer	Pre-dielectric deposition treatment	t_{ox} (nm)	Metal gate
A	Al_2O_3	Yes	9	Ti/Au
B	Al_2O_3	No	9	Ti/Au
C	HfO_2	Yes	10	Ti/Au

[a]E-mail: palumbo@mt.technion.ac.il. Phone: +972-4-829 2779

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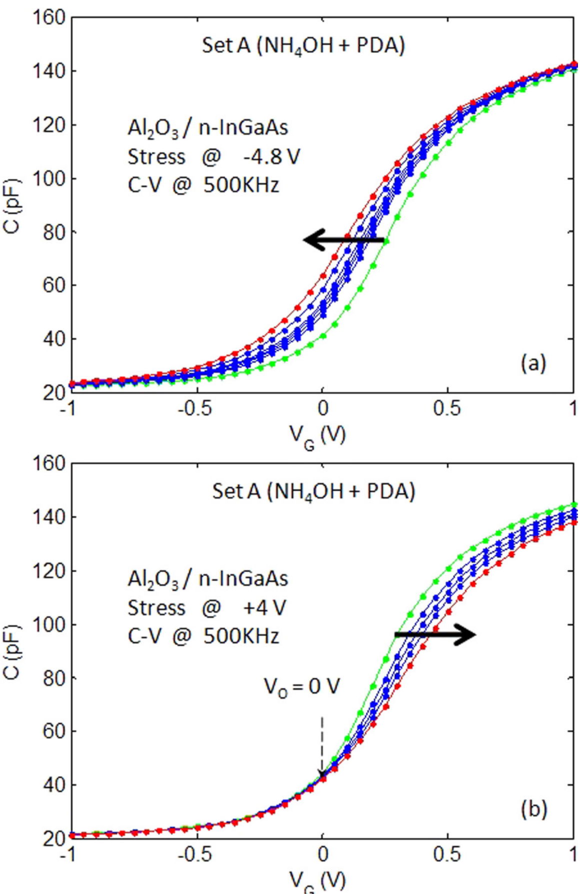

FIG. 1. Consecutive C-V curves at 500 KHz for set A (treated with NH_4OH) at room temperature after (a) CVS at −4.8 V, and (b) CVS at +4 V. Both cases correspond to an accumulation time of CVS of 10 min. The main feature is the non-uniform shift of the C-V curves showing that only the upper part of the C-V is affected by the positive stress.

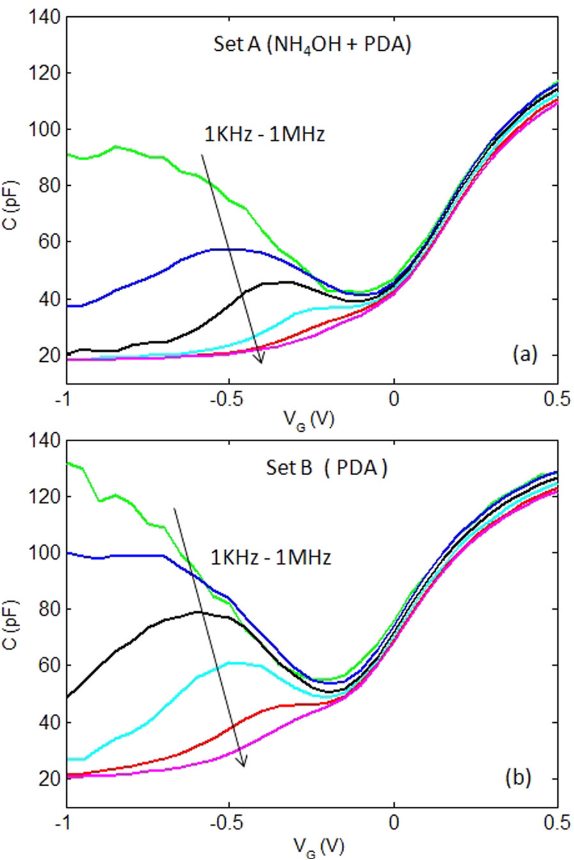

FIG. 2. Typical multi-frequency capacitance-voltage curves from 1 KHz to 1 MHz. (a) Set A (treated with NH_4OH). (b) Set B (without treatment). Arrows mark the direction of frequency increase. In contrast of set B, set A shows a relatively small increase of the capacitance in the inversion regime.

Figure 1 that positive and negative stress bias behave differently, in agreement with previous works.[13,14] At negative CVS, the whole set of C-V curves shifts towards negative bias indicating accumulation of positive charge (Fig. 1(a)), while at positive CVS, the C-V curves shift towards positive bias indicating accumulation of negative charge (Fig. 1(b)). The main feature of the experiment under positive CVS on which we focus is the non-uniform shift of the C-V curves showing that only the upper part of the C-V is affected by the positive stress. This feature is characterized by an onset point, marked as V_O in Fig. 1(b), from which the shift of the C-V curves is observed.

In order to explore the origin of such a particular feature, we decided to study the influence of the oxide/semiconductor interface on this phenomenon. CVS experiments were performed on samples of set A (treated with NH_4OH) and of set B (without treatment). Such differences are clearly observed in the typical multi-frequency C-V curves of the two sets given in Figure 2. Set A, (Fig. 2(a)), shows a relatively small increase of the capacitance in the inversion regime; while in set B, (Fig. 2(b)), the capacitance is increased significantly in this regime. As reported in our previous works, the area under the C-V "weak inversion hump" (Q_{hump}) is related to the density of interface states.[5,15] In our case, the area Q_{hump} under the C-V measured at 100 kHz shows a reduction from $4.7 \times 10^{-7}\,C/cm^2$ for set B to $2.5 \times 10^{-7}\,C/cm^2$ for set A, indicating the efficiency of the NH_4OH treatment for reducing the density of interface states for Al_2O_3/InGaAs gate stacks. Moreover, it is observed that the dispersion with frequency of the accumulation capacitance is small and similar for both sets of samples, indicating no influence of the NH_4OH treatment on the traps responsible for the dispersion in accumulation, mentioned in the literature as "border traps."[16,17] The latter observation together with a similar C-V hysteresis at flat band condition for both sets ($\Delta V_{FB}^{Hyst} = 0.10\,V$ and $\Delta V_{FB}^{Hyst} = 0.09\,V$ for sets A and B, respectively) indicate a similar density of this kind of traps.[18]

Figure 3 shows a comparative analysis of consecutive C-V curves after CVS at +4 V with an accumulated stress time of 10 min for both sets. We recall that set A is with a lower density of interface states than set B, but both have similar density of border traps. In both cases, there is a shift towards positive bias of the upper part of the C-V curves with a similar onset point V_O. An interesting aspect is the equal difference between the onset point V_O with respect to V_{FB} in the C-V curves ($V_{FB} - V_O = 0.15\,V$) for both samples. It indicates that the Fermi level position at the oxide/semiconductor interface for the V_O condition is similar in both cases, hence independent of the characteristics of the oxide/semiconductor interface.

To clarify the influence of the dielectric layer, additional measurements were performed on a similar MOS stack using a different dielectric layer (set C). Figure 4 shows consecutive C-V curves after CVS pulses at positive bias (+3 V)

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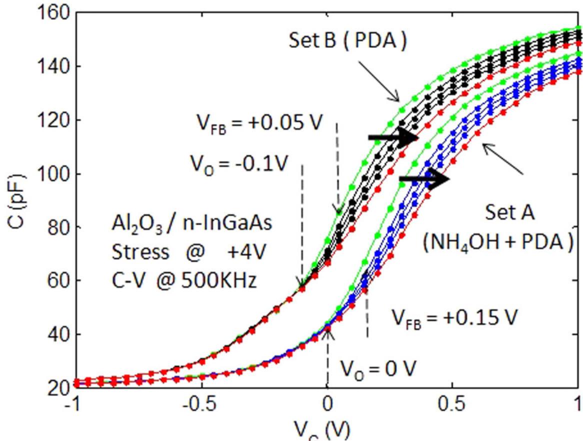

FIG. 3. Consecutive C-V curves at 500 KHz after CVS at +4 V at room temperature with an accumulated stress time of 10 min for sets A and B (with and without NH_4OH treatment, respectively). An interesting aspect is the equal difference between the onset point V_O with respect to V_{FB} in the C-V curves ($V_{FB} - V_O = 0.15$ V) for both samples.

with an accumulated stress time of 10 min for the case of MG/HfO_2/n-InGaAs. For a better description, we included only the first and the last C-V curve of the consecutive C-V series. A shift of the C-V curves towards positive bias is observed only on the upper part of the C-V curve with a similar onset point. This indicates an accumulation of negative charge. It is worth that similarly to the other cases, the difference between the onset point V_O with respect to V_{FB} in the C-V curves is $V_{FB} - V_O = 0.15$ V. The occurrence of this particular feature during the CVS at positive bias is independent of the quality of the interface and of the type of dielectric layer. It is a clear indication that the accumulation of negative charge is only related to characteristics of the substrate (InGaAs).

It is important to note that the occurrence of such a particular feature is not an artifact and is observed in a large range of bias in the CVS experiments and frequencies in the C-V curves. The observation of the onset point is independent of the frequency of the C-V curves in the range of 1 MHz–100 KHz. At low frequencies (near 10 KHz), the influence of the interface states in the C-V curves through the "weak inversion hump" makes it difficult to identify the onset point, V_O. Therefore, most of the analyses reported here are based on C-V curves measured at 500 KHz to avoid influence of interface states.[2] Moreover, the occurrence of the onset point, V_O, was verified over a large range of bias during the CVS (from +3 V to +5 V) showing the same behavior until a breakdown event, indicating that V_O is also independent of the stress time.

Figure 5 shows the typical C-V curves of set A after CVS pulses at high temperature. After the first CVS pulse at +3 V for 10 min at 125 °C, the C-V curve (curve 1) shows a shift of the upper part towards positive bias, however, the lower part of the C-V curve shifts towards negative bias increasing the stretch-out. After the second CVS pulse at +3 V for 10 min at 125 °C, the C-V curve (curve 2) shifts towards positive bias without an additional stretch-out indicating accumulation of negative fixed charge, likely due to electron trapping in the stress-induced defects.

Contrary to what is observed with CVS at room temperature, the conductance also increases significantly in this case. The inset in Figure 5 shows an increase of the conductance peak after the first CVS pulse at 125 °C, while the magnitude of the peak after CVS at RT remains similar to the fresh device. Therefore, the overall results show that the degradation under positive bias consists of two contributions depending on the temperature. At room temperature, the changes of the electrical characterizations are dominated by electron-trapping into traps located in energy levels in the upper part of the semiconductor gap. We believe that electron trapping is the main mechanism due to the absence of any modification of the hysteresis (Table II) and the conductance peak during the CVS (inset in Fig. 5). Regarding the distribution in energy, the particular features of the C-V curves after the CVS show an onset point for the distribution that does not depend on neither the quality of the oxide-semiconductor interface (based on the comparison of sets A and B), nor on the dielectric layer (comparison of sets A and C). Since the onset point maintains a constant difference

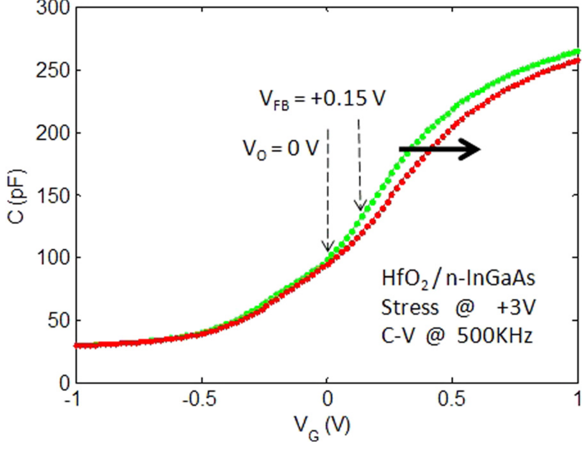

FIG. 4. Consecutive C-V curves at 500 KHz after CVS at +3 V at room temperature with an accumulated stress time of 10 min. It is worth to note that also in this case, the difference between the onset point V_O with respect to V_{FB} in the C-V curves is $V_{FB} - V_O = 0.15$ V.

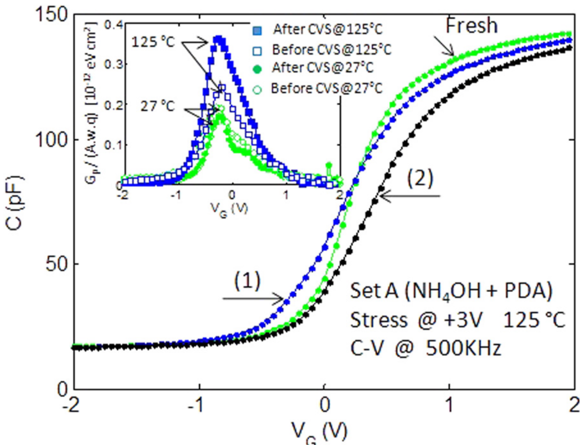

FIG. 5. Consecutive C-V curves at 500 KHz at room temperature after CVS pulses at high temperature on set A (treated with NH_4OH). Curves 1 and 2 correspond to pulses of +3 V at 125 °C for 10 min. The inset shows the normalized parallel conductance peak after stress at +3 V at room (27 °C) and high temperature (125 °C). It is worth to note that the measurements between CVS pulses were performed at room temperature.

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TABLE II. Description of C-V hysteresis.

	Fresh	After CVS for 10 min @ +3 V & 27 °C	After CVS for 10 min @ +3 V & 125 °C
Set	ΔV_{FB}^{Hyst} (V) ± %10	ΔV_{FB}^{Hyst} (V) ± %10	ΔV_{FB}^{Hyst} (V) ± %10
Set A	0.10	0.11	0.15

with respect to V_{FB} ($V_{FB} - V_O = 0.15$ V), this point may correspond to the position of the Fermi level in the bandgap of the semiconductor near the midgap condition. This onset point would agree well with the calculated as anti-site (As_{Ga}) defect level.[19]

At a high temperature, a different behavior is found for CVS, giving indication that a new component contributes to the degradation of the MOS stack. Contrary to the previous case, the C-V curves show an increase of the stretch-out, the hysteresis, and the conductance peak, indicating that the generation of defects at the oxide-semiconductor interface contributes to the degradation. In our previous work, we have reported that the V_{FB} does not show a temperature dependence after CVS at positive bias,[5] therefore, one may conclude that the increase of the stretch-out is generated by defects that only contribute when the V_G range is in the lower part of the C-V (i.e., in the lower part of the semiconductor gap). However, the increase of the hysteresis in the same CVS condition (Table II) is a clear indication that the generation of border traps also contributes to the degradation.

This increase of the density of border traps does not result in an increase of the frequency dispersion in accumulation (results not shown). It may occur since the oxide thickness of the samples is relatively thick (9 nm), and hence the capacitance contribution of such defects is not significant to be measured.

The non-uniformity of generation of defects after CVS is in agreement with recent results. Jiao *et al.*[20] showed on Al_2O_3/InGaAs that the stress-induced trap density under positive bias could be understood in terms of acceptor and donor traps in the upper and lower part of the gap, respectively.

Our results show that border traps and interface stated are the main contributors in the upper and lower part of the semiconductor bandgap, respectively. Based on the features of the stressed C-V curves, it is possible to estimate the onset point of the distribution of border traps near the midgap condition, while comparing different MOS stacks with different dielectrics it is reasonable to suggest that the border traps are strongly related to the characteristics of the InGaAs. Regarding the generation of interface estates, the main characteristic is their thermal activation during CVS experiments.

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